

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES) INC.

Petitioner

v.

INTELLECTUAL VENTURES II LLC

Patent Owner

Case No.: IPR2024-01226

U.S. Patent No. 7,646,835

Title: METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING
INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR
AN INTEGRATED CIRCUIT DEVICE

**DECLARATION OF TERRY R. LEE
IN SUPPORT OF PATENT OWNER'S RESPONSE**

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I. INTRODUCTION

1. My name is Terry R. Lee. I have been retained as an expert witness by Intellection Ventures II, LLC (“Patent Owner”) for this *Inter Partes* Review IPR2024-01226 of U.S. Patent No. 7,646,835 (“’835 Patent” or the “Patent”) filed by Lenovo (United States), Inc. (“Lenovo” or “Petitioner”).

2. In the Petition, I understand that Petitioner is challenging the validity of Claims 1-23 (the “Challenged Claims”) of the ’835 Patent (Ex. 1001), constituting all the claims of the ’835 Patent, on the grounds of obviousness. I have been asked to prepare the present Declaration to be submitted with Patent Owner’s Preliminary Response.

3. I have been asked to consider whether the Challenged Claims of the ’835 Patent would have been obvious to a person of ordinary skill in the art (“POSITA”) as of the date of the invention. I was also asked to review and comment on several technical statements made by Petitioner in the Petition and by its expert, Dr. R. Jacob Baker.

4. In this Declaration, all emphasis in boldface has been added unless otherwise noted.

II. BACKGROUND AND QUALIFICATIONS

5. This section summarizes my educational background, career history, publications, and other relevant qualifications. My curriculum vitae is attached as

Patent Owner's Exhibit 2002, which includes my detailed employment background, professional experience, and list of publications.

6. I have over 40 years of industry experience in integrated circuits, PCB design, and memory subsystem design. This experience includes both product development and product definition with a long-term focus on next generation DRAM technologies.

7. I received a Bachelor of Science Degree in Electrical Engineering from the University of Missouri - Columbia in 1983, a Master of Science Degree in Electrical Engineering from the University of Southern California - Los Angeles in 1985, and a Master's Degree in Business Administration from the University of Washington - Seattle in 2004.

8. Since 2016, I have been the President and Subject Matter Expert at IdaTech Consulting, which provides electrical engineering expert services to intellectual property firms. These services include research, reverse engineering, claim charting, patent assessment, and patent litigation support. My previous industry experience includes 26 years of employment at Micron Technology, Inc., a Fortune 500 memory semiconductor company.

9. From 1980 to 1983, I was employed by Texas Instruments, Inc, as a co-op student for CMOS integrated circuit design.

10. From 1983 to 1989, I was employed by Hughes Aircraft Co. as an electrical engineer and engineering manager. My responsibilities included RF digital integrated circuit design, and subsystem design for aerospace and electronic warfare systems. This work included the development of an advanced Digital RF Memory (DRFM) subsystem and custom bipolar integrated circuits for serializing and deserializing data words.

11. From 1989 to 2015, I was employed at Micron Technology, Inc. in various engineering roles of progressive responsibility. These roles involved DRAM Integrated Circuit Design, Applications Engineering, DRAM Product Definition, Strategic Marketing, Signal Integrity, Logic Design, PCB Design for memory modules (DIMMs) and Solid State Drives (SSDs), advanced semiconductor packaging, engineering tester development, and Managed NAND development.

12. While working for Micron, I was involved in many standards-setting groups and industry consortiums focused on defining the next-generation DRAM products. My first involvement with the JEDEC Solid State Technology Association (formerly known as Joint Electron Device Engineering Council, or just JEDEC) was in 1992, and my JEDEC involvement continued at various levels through my tenure at Micron Technology, Inc. In 1996, I became involved in the SLD RAM Consortium (formerly known as SyncLink) for developing the

specification of a next generation high-speed DRAM technology. Around 1999, I was involved in the Advanced DRAM Technology Consortium (ADT) for defining a next-generation DRAM technology. The consortium included several DRAM manufacturers and Intel Corporation. At different times, I was the Technical Leader for both the SLD RAM Consortium and the ADT Consortium. My area of focus and expertise in these organizations involved high-speed signaling and bus communication, physical design, and memory subsystem design.

13. At various times while working for Micron, I was a member of IEEE and part of the Memory Paper Selection Subcommittee for IEEE International Solid State Circuits Conference (ISSCC). I gave various presentations and keynote addresses in support of memory industry conferences while at Micron. I also served time on Micron committees for patent disclosure approval and for the Technical Career Ladder.

14. In June 2015, I retired from Micron and started my own company in 2016 to provide expert services in support of intellectual property firms.

15. I am the named inventor of 97 patent families, all of which are directed in general to memory integrated circuits, memory module design, high-speed interfaces, and packaging.

16. I have served as an expert witness for investigations before the Federal Trade Commission, proceedings at the European Commission, and for patent litigation lawsuits.

III. COMPENSATION

17. I am being compensated for my work in this case at the rate of \$500 per hour. I am also reimbursed for all reasonable expenses that I incur during the course of this case. My compensation does not depend upon the results of my analysis or the substance of my testimony, nor does my compensation depend on the outcome of this or any related proceeding. I have no personal interest in the outcome of this matter. I have no financial interest in Patent Owner or affiliation with any of the real parties in interest, the Patent Owner, or the named inventor of the '835 Patent. It is conceivable that I may own mutual funds whose portfolios include stock in Petitioner. If this is the case, the value of such holding would not constitute a material part of my net worth.

18. The statements made and opinions provided in this Declaration are based on my own personal knowledge and, if called as a witness, I could and would testify in a manner consistent with this Declaration.

IV. MATERIALS CONSIDERED

19. I have reviewed the following documents in forming the opinions expressed in this Declaration I have considered all the materials cited herein and all materials filed in this IPR up to and including August 28, 2024.

Exhibit Number	Contents
1001	US 7,646,835 (Rozas)
1002	Declaration of R. Jacob Baker
1003	US 7,646,835 File History
1004	US 6,434,081 (Johnson)
1005	US 6,629,222 (Jeddeloh)
1006	US 6,115,318 (Keeth)
1007	Claim Construction Order
1008	SDRAM Architectures, Organizations, and Alternative Technologies (Jacob)
1009	RAM Guide Part I: DRAM and SRAM Basics (Stokes)
1010	Design and PCB Layout Considerations for Dynamic Memories Interfaced to the Z80 CPU (Olmstead)
1011	A Performance Comparison of Contemporary DRAM Architectures (Jacob)
1012	How to Use DDR SDRAM (Elpida)
1013	Hyundai Press Release
1014	SLDRAM: High-Performance, Open-Standard Memory (Gillingham)
1015	How Memory Works With The Processor (Asuni)
1016	Memory Access Scheduling (Rixner)
1017	Computer System Operation
1018	Coarse-to-fine Estimation of Visual Motion (Simoncelli)
1019	Modern Dictionary of Electronics (Graf)
1020	Merriam Webster's Collegiate Dictionary
1021	JEDEC DDR SDRAM Specification

1022	Declaration of Duncan Bauserman
1023	Petition
2002	Curriculum Vitae of Terry R. Lee
2003	A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line (Dudek)
2004	US 5,781,766 (Davis)
2005	US 6,016,282 (Keeth)
2006	US 6,101,197 (Keeth)
2007	US 6,553,472 (Yang)
2008	US 2002/0078316A1 (Nakamura)
2009	US 2003/0122696A1 (Johnson)
2010	US 2003/0231543A1 (Matsui)
2011	US 2004/0160833A1 (Suzuki)

20. I have also relied on my education, skill, training, and experience in the relevant fields of technology in forming my opinions. I have further considered the viewpoint of a person of ordinary skill in the art (“POSITA”) as of the time of the inventions of the ’835 Patent.

21. I reserve the right to supplement my opinions as expressed in this Declaration to address any new information obtained in the course of this proceeding, or based on any new positions taken by Petitioner.

V. SUMMARY OF MY OPINIONS

22. It is my understanding that the following table summarizes the grounds of challenge to the Challenged Claims raised in the Petition:

Ground	Invalidity Challenge	References	Challenged Claims
1	§ 103	Johnson, Jeddeloh	1-23

2	§ 103	Johnson, Keeth	1-3, 7, 8, and 12
3	§ 103	Johnson, Keeth, Jeddeloh	4-6, 9-11, and 13-19

23. After a review of the alleged prior art asserted by Petitioner and by Dr. R. Jacob Baker (Ex. 1002), it is my opinion that Petitioner has not demonstrated that the claims are unpatentable.

24. My opinions, and the bases, therefore, are detailed throughout this Declaration.

VI. LEGAL FRAMEWORK

25. Counsel for Patent Owner has informed me of the legal principles that apply in this proceeding.

26. I have been informed that Petitioner has the burden to prove that the claims challenged in the Petition are not patentable by a preponderance of the evidence, which I understand to be just enough evidence to make it more likely than not that Petitioner's argument is correct.

A. Anticipation and Obviousness

27. A claim is invalid as obvious under 35 U.S.C. § 103 if the differences between the subject matter sought to be patented and the prior art are such that the subject matter of the claim as a whole would have been obvious at the time of the invention to a person having ordinary skill in the art to which the invention pertains. I have been informed that the following factors are used to determine

whether or not the claimed subject matter would have been obvious: (i) the scope and content of the prior art; (ii) the differences, if any, between the prior art and the claimed invention; (iii) the level of ordinary skill in the field of the invention; and (iv) any relevant objective considerations of non-obviousness.

28. A party asserting obviousness based on a combination of prior art references must demonstrate that one of ordinary skill in the art would have been motivated to combine the teachings of those references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so. It is my understanding that it is not enough to show that one skilled in the art could combine elements of multiple references, but instead there must be some reason that would have prompted a person of ordinary skill in the art to combine the elements in the way the claimed invention does. I understand that there must be some reasoned explanation as to why one of ordinary skill in the art would combine the references.

29. I understand that obviousness may be shown by considering more than one item of prior art and by considering the knowledge of a person of ordinary skill in the art, and that obviousness may be based on various rationales including: (i) combining prior art elements according to known methods to yield predictable results; (ii) simple substitution of one known element for another to obtain predictable results; (iii) use of known techniques to improve similar

devices in the same way; (iv) applying a known technique to a known device ready for improvement to yield predictable results; (v) “obvious to try” – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; (vi) known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art; and (vii) some teaching, suggestion, or motivation in the prior that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

30. A combination of references would not have been obvious if the alleged modification(s) to be made to the reference(s) would have been inconsistent with the reference’s stated goals or method of operation or would have rendered the combination inoperable for its intended purpose. I further understand that for something to have been obvious, the party asserting obviousness must explain why a POSITA would have selected components for combination in the manner claimed.

31. I further understand that a claim is not obvious over a combination of prior art references if such references “teach away” from the claimed combination, if there is no motivation to combine such references, or if the combination would

lead to waste and inefficiencies not present in one or more of the references in isolation.

32. It is my further understanding that obviousness cannot be based on a hindsight combination of components selected from prior art references. For example, the challenged Patent itself cannot be used as a basis for combining prior art references absent such a teaching in the Patent. I also understand that an invention would not have been obvious simply because all of the elements of the invention may have been known separately in the prior art.

33. The concept of incorporation by reference was also explained to me. Incorporation by reference is a key mechanism in U.S. patent law that allows a patent applicant to incorporate material from an external document into a patent application by referring to it. This method is beneficial for including material that is too extensive to be included directly in the application or has already been described in a prior patent or application. The aim is to simplify the application process and eliminate the need for repeating information. The material incorporated by reference is considered an integral part of the patent application, which helps in fully describing the invention and supporting the patent's claims.

B. Level of a Person of Ordinary Skill in the Art

34. I understand that the hypothetical person of ordinary skill in the art (POSITA) is considered to have the normal skills and knowledge of a person in a

certain technical field, as of the time of the invention at issue. I understand that factors that may be considered in determining the level of ordinary skill in the art include: (1) the types of problems encountered in the art; (2) the prior art solutions to those problems; (3) rapidity with which innovations are made; (4) the sophistication of the technology; and (5) the education level of active workers in the field. I also understand that “the person of ordinary skill” is a hypothetical person who is presumed to be aware of the universe of available prior art. Therefore, no such person actually exists. Petitioner has proposed that a POSITA for the '835 Patent “would have had bachelor’s degree in electrical engineering, computer engineering, or the equivalent, and two to three years of experience designing high-speed computer memory devices..” (Petition, 34) Petitioner further alleged that “More practical experience could qualify one not having the aforementioned education as a POSITA, while a higher level of education could offset lesser experience.” (Id).

35. I agree with Petitioner that these would be the minimum qualifications for a POSITA.

36. The opinions I express herein are from the viewpoint of such a POSITA as of November 17, 2003.

VII. THE '835 PATENT AND THE CHALLENGED CLAIMS

37. After having read the '835 Patent in its entirety, I find no reason that any of the claim terms should be construed to have a meaning that is different than the plain and ordinary meaning as understood by a POSITA at the time of invention. Accordingly, when evaluating the terms recited in the claims of the '835 Patent, I have applied their plain and ordinary meaning.

VIII. BACKGROUND OF THE TECHNOLOGY

A. Synchronous DRAM (SDRAM)

38. SDRAM was a successor to mainstream asynchronous DRAM interfaces such as Page Mode, Fast Page Mode, and Extended Data Out (EDO). SDRAM was standardized in the Joint Electronic Device Engineering Council (JEDEC) in 1993 and was the first standardized DRAM technology with a synchronous interface. In this standard, the Command/Address bus and the Data bus signals (DQs) were held valid and sampled at the rising edge of a free running clock signal. (Ex. 1011, Figs. 1-5). Sampling data, strobing data, capturing data, latching data, or registering data are all synonymous terms for using a timing signal to latch and hold the data received from a bus.

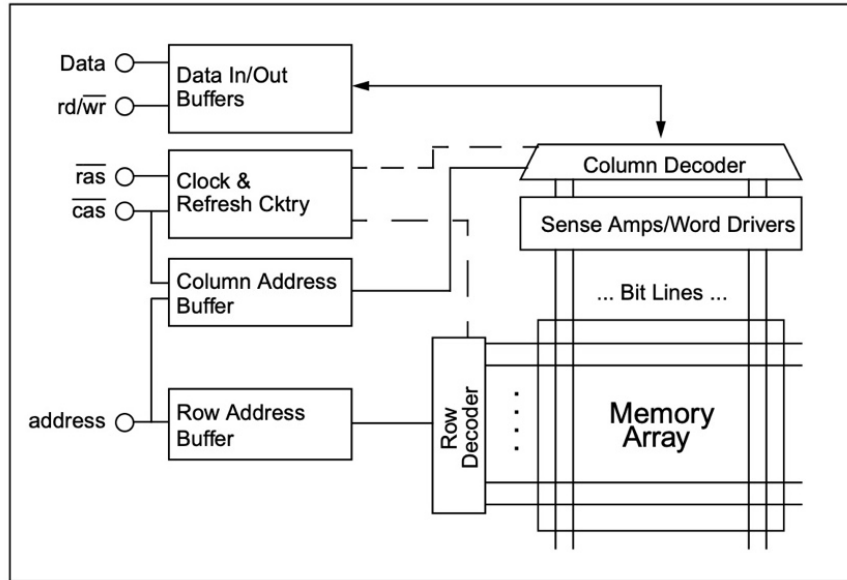


Figure 1: Conventional DRAM block diagram. The conventional DRAM uses a split addressing mechanism still found in most DRAMs today.

Exhibit 1011, Fig. 1

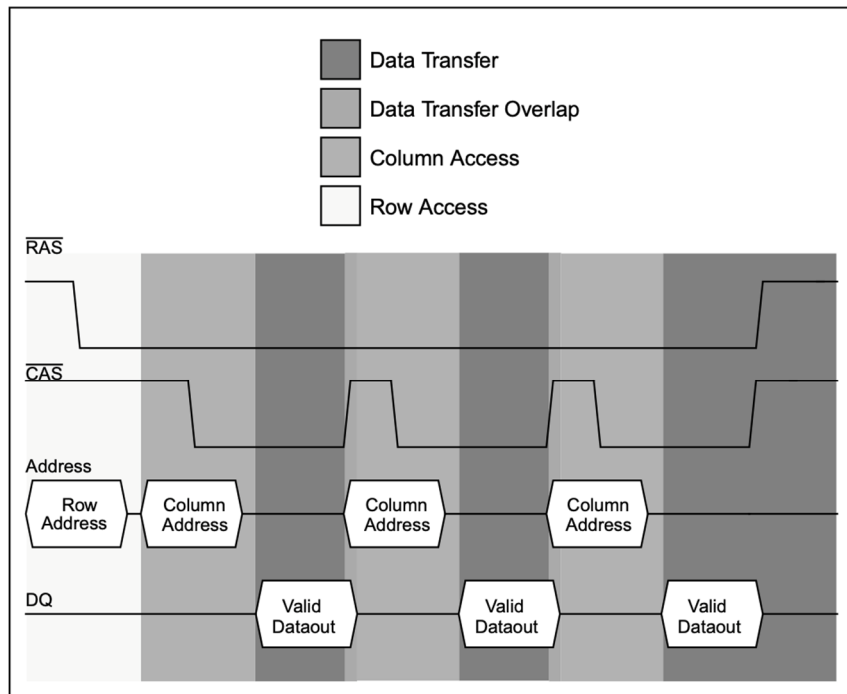


Figure 2: FPM Read Timing. Fast page mode allows the DRAM controller to hold a row constant and receive multiple columns in rapid succession.

Exhibit 1011, Fig. 2

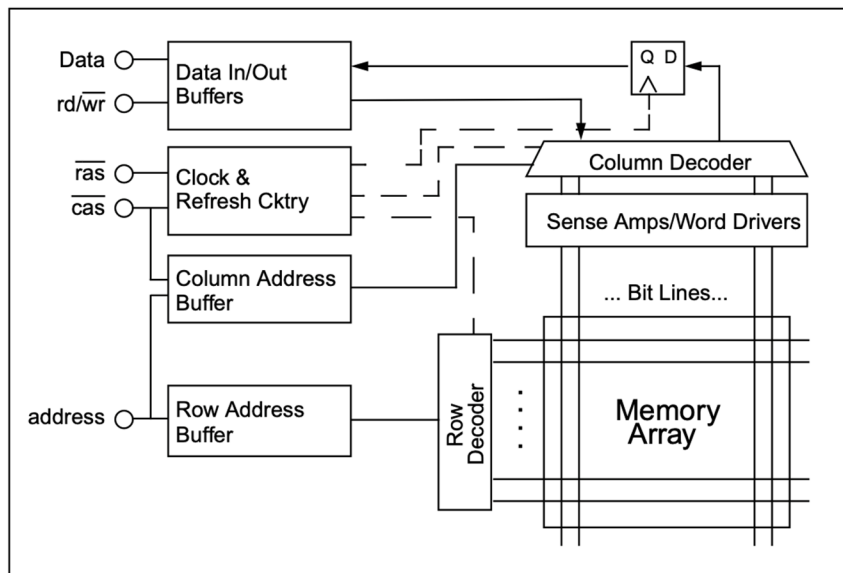


Figure 3: Extended Data Out (EDO) DRAM block diagram. EDO adds a latch on the output that allows CAS to cycle more quickly than in FPM.

Exhibit 1011, Fig. 3

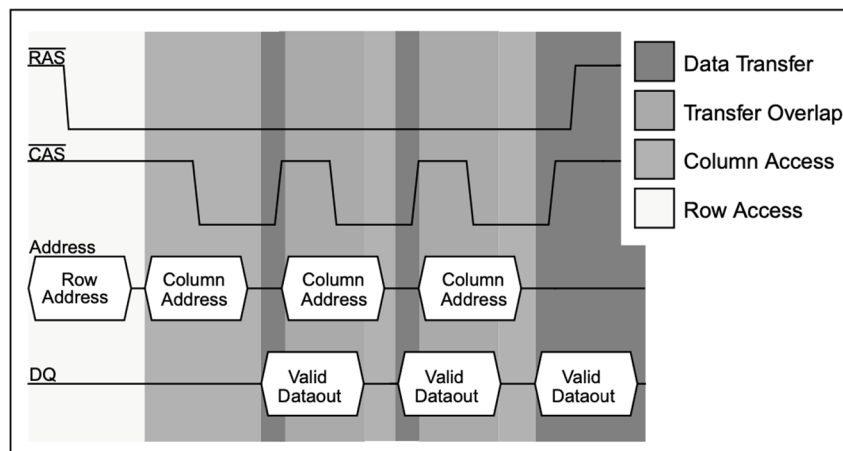


Figure 4: EDO Read Timing. The output latch in EDO DRAM allows more overlap between column access and data transfer than in FPM.

Exhibit 1011, Fig. 4

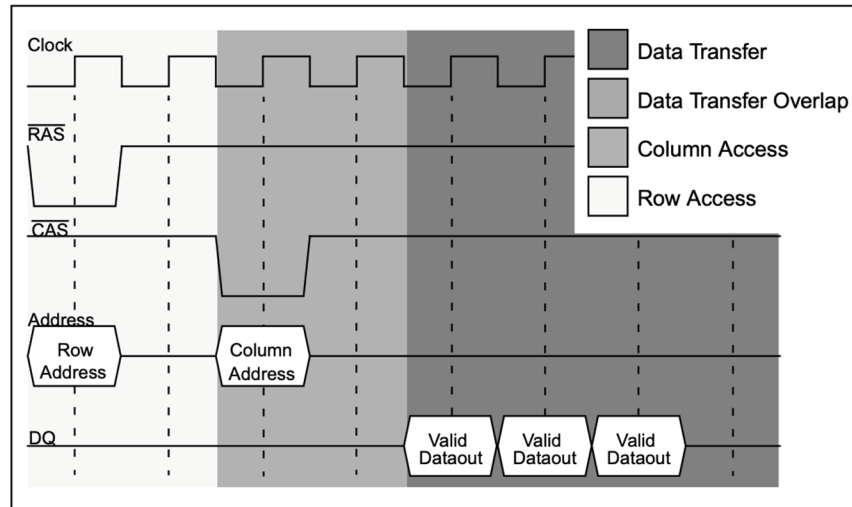


Figure 5: SDRAM Read Operation Clock Diagram. SDRAM contains a writable register for the request length, allowing high-speed column access.

Exhibit 1011, Fig. 5

39. SDRAM memory systems typically employed a memory controller that communicated with a plurality of SDRAMs. Two different clock topologies were typically used. In a conventional synchronous interface, a global clock is routed to the controller and DRAMs through a clock buffer device so the clock signals arrives at all devices at essentially the same point in time (with the same clock phase). Within one clock period, an output from the controller passes through an output buffer delay, propagated to the DRAMs at the other end of the bus, and meets the setup time requirement at the DRAM input. The setup time is the time which the DQ signal must transition to the valid logic state prior to the rising clock edge to guarantee accurate data capture. The same data timing occurs when the DRAM outputs data to be sent to the memory controller.

40. An alternate clocking topology that was sometimes deployed used a clock forwarding technique, where the controller forwarded a clock to the DRAM. The forwarded clock reduced the impact of propagation delay, commonly called flight time, because the forwarded clock traveled in the same direction as the DQs during write operations, so they essentially propagated together. However, forwarding the clock made the read data capture and timing more difficult, because two bus flight times (clock/command and read data) occurred during the clock period, and the controllers would sometimes include a first-in-first-out (FIFO) and other logic to capture data and then transfer the received data to the zero degree phase of the global clock.

B. Double Data Rate (DDR) DRAM

41. In a broader sense, DDR technology sometimes refers to the collection of JEDEC DDR standard devices including DDR, DDR2, DDR3, DDR4, and DDR5.

42. Double data rate DRAM was standardized in JEDEC in June, 2000. DDR used a command/address bus similar to SDRAM, where the commands were sent to a plurality of DRAMs and were sampled by the rising edge of the clock signal. To increase the transfer rate of data, the DQs were sampled on both edges of a timing reference Data Strobe, or DQS. DQS operated at the same frequency as the clock, but it was gated off and only used during data transfer times. (Ex.

1012, Fig. 1-4). DQS was essentially a replicate DQ line. It used the same drivers as DQs and was routed alongside the DQs (flew with the data). The DQS timing reference relaxed the DQ bus timing by eliminating absolute propagation delay from the bus timing budget and replacing it with differences in propagation delay. This topology is considered a source synchronous design in that the data is synchronized at the controller (source), although the data is received at the same frequency at the DRAM but with a different phase relative to the source. This is analogous to a running race where all runners must tie. The absolute time of the race is less relevant than the differences in finishing times. Eliminating the propagation delay within a clock period from the timing budget allowed for higher data transfer rates.

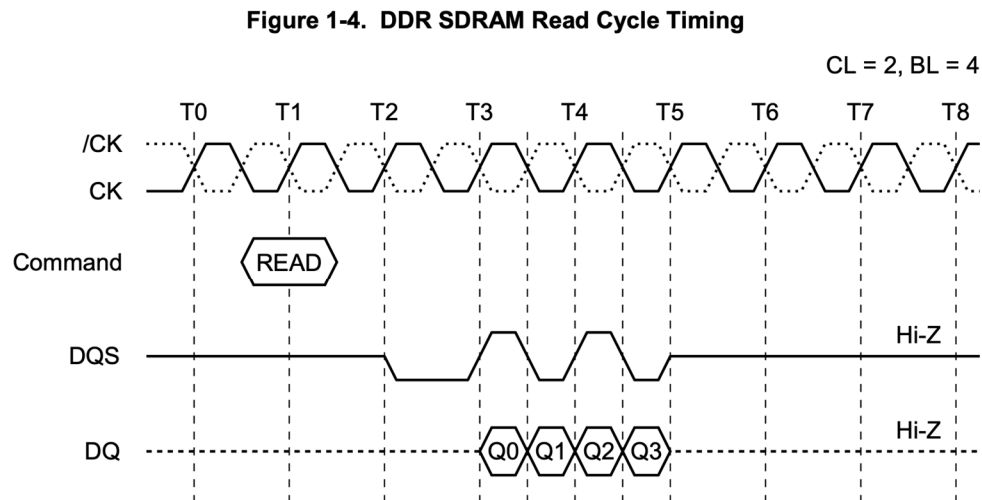


Exhibit 1012, Fig. 1-4

43. In a computer motherboard, there are many sources of timing skew on the data bus. Even if all DQs exit the transmitting device at precisely the same

time, the time at which the bits are received is influenced by inter-symbol interference, induced power supply noise, crosstalk, termination impedance mismatch, load capacitance differences, route length differences, and many other factors. An ideal signal stream transmitted from a driver can appear as a fuzzy edge at the receiver indicating a variance in arrival time due to these signal integrity issues (Ex. 1006, Fig. 8 and 9:51-60).

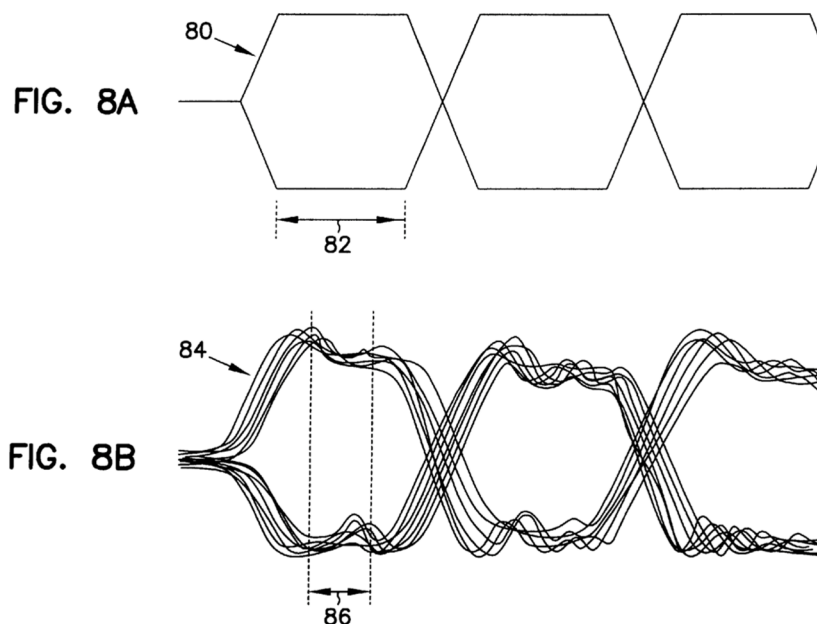


Exhibit 1006, Fig. 8

44. Due to the tight timing budget at high data rates (short clock periods), centering the DQS signal in the data eye was a challenge of precision. Once the DQs were correctly captured on the bus, it was necessary to transfer them back to the time domain of the internal device clock which is used for the logic state machine of the device. This transfer was relatively easy to accomplish at these

data rates. The DRAM specification that defined this arrival time of DQS relative to the clock is referred to as tDSS and tDSH, which is the setup time and hold time, respectively, of DQS to clock. (Ex. 1021, p62). The arrival time of DQS relative to commands is tDQSS. These two sets of specifications combined accounted for about 40 to 50 percent of the clock period. The controller performs a similar clock domain transfer on reads. There were no training modes included in the DDR specification, but controllers needed to shift the DQS signal on reads by 90 degrees to convert an edge aligned DQS signal to an internal signal aligned with the center of the data eye.

45. Computer memory system data busses in this timeframe were 64 or 128 bits wide, and processor cache line sizes were typically 64 bytes (512 bits). Data was prefetched from the slower but wider DRAM array and then time division multiplexed to provide a sequential burst of data at the DRAM pins. A burst length of four was required to fill a 64-byte cache line with a 128-bit wide memory data bus. (Ex. 1012, Fig. 1-4). A single read command at the DRAM results in four data transfers at the output, so the data rate requirements were higher than the command bus bandwidth requirements. A common DDR device used a 133 MHz clock to achieve 266 Mbps data rates at the DQ pins. The imbalance of command versus DQ bandwidth was embedded in the device protocol and bus architectures.

46. In computer systems, DDR memory components were typically mounted on dual inline memory modules, DIMMs. (Ex. 1008, Image 1). The DIMMS were 64 data bits wide and typically had one row of eight DRAMs for a single sided module, or two rows of eight DRAMs for a two-sided module. The command/address bus entered the DIMMs at the connector pins located along the bottom of the DIMM. This DIMM command/address lines branched out on the DIMM like a family tree and traveled vertically on the DIMM, so all DRAMs received the command/address signals at nearly the same time. In the single sided example, the command/address bus would have eight device loads per signal. This routing method was commonly called a T- or H-topology due to the branches.

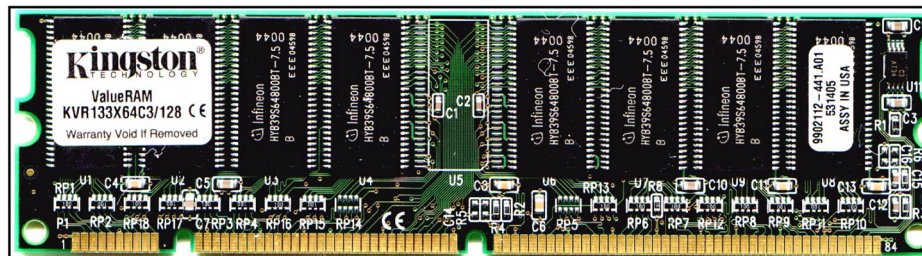
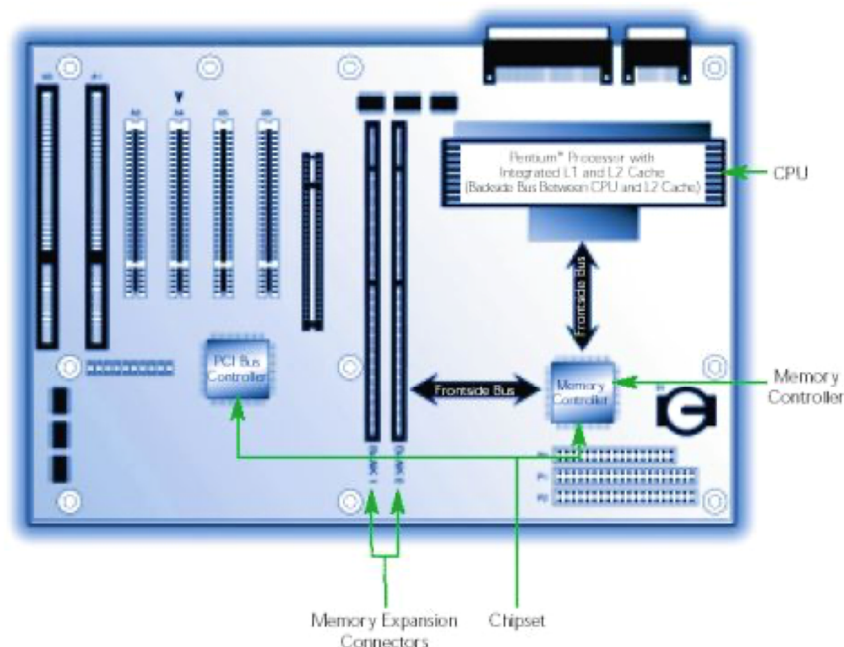


Exhibit 1008, Image 1

47. The DIMM DQ lines were routed to a single DRAM in this example, with eight DQ bits connecting to each DRAM, so each DQ bus signal would have a single device load. The lighter loading of the DQs facilitated the higher data rates required on this bus. A typical computer motherboard would have two or

four memory expansion slots for inserting the DIMMs. There were various design choices, but the DQ and command busses would typically be connected to two DIMMs. (Ex. 1015, P1).



Main components of a computer system.

Exhibit 1015, P1

C. Double Data Rate 2 (DDR2)

48. It was a general goal at JEDEC to double the data rates for each evolution of the DDR technology. The DDR2 standard, which was released in September, 2003, was an evolutionary progression of DDR to achieve higher bandwidths. Improvements in DRAM process technology enabled a reduction in device input capacitance while on-die active termination was used on the DQ lines to achieve higher data rates. A device clock frequency of 266 MHz and data rates

of 533 Mbps was common. The physical bus topologies were essentially the same as DDR.

D. Double Data Rate 3 (DDR3)

49. The DDR3 standard was released in June, 2007. Even with improvements in DRAM process technology, it was determined that lower input capacitance on the command/address lines alone would not provide adequate signal integrity necessary for higher clock rates due to a bus physics limitation preventing higher operating frequencies. The 8 device loads in parallel on the DIMM appear as a low impedance discontinuity on the bus which results in a non-flat frequency response which limited the upper frequency limit. The DIMM bus routing had to be changed.

50. Referring again to Ex. 1008, Image 1, the command/address signals at the bottom of the DIMM are now routed to the left of the module, and they are connected in a daisy chain fashion to the DRAMs as they travel from left to right on the module. The clock signal traverses a similar path to the command bus, while DQs are routed vertically in a similar manner to DDR2 and are now orthogonal to the command bus on the module. This routing method is commonly referred to as a fly-by topology, as the command/address and clocks fly by the DRAMs and no longer arrive at the DRAMs all at the same time. The capacitive load at the DRAMs now appears as a distributed capacitance along the bus

transmission line as opposed to a lumped, low impedance load. The result is a higher operating frequency but with a new timing problem – precise alignment of command, data, and data strobes.

51. Each DDR3 DRAM receives its commands at slightly different times (early commands on the left and late commands on the right of the module) due to flight time differences, and the arrival time of commands relative to the DQs and their strobes (DQS) is different for each DRAM on the module. At high transfer rates the alignment was more difficult, so new training mode was added to DDR3 to allow the controller to detect when the DQS is received relative to the clock signal (and therefore commands) at each DRAM. The controller enters a training sequence where the clock input is sampled by the DQS at the DRAM, and the result is fed back to the controller on the DQ lines. This mode allows the controller to adjust the phase delay of the DQS relative to the commands and clock to meet the tDQS, tDSS, and tDSH specifications for each device. This training mode is referred to as write leveling.

E. Double Data Rate 5 (DDR5)

52. DDR5 was standardized in July, 2020 and is the most recent version of DDR technology. Data rates up to 8800 Mbps are expected for DDR5. To achieve these high data rates, the device requires more training and sophistication, and training modes were added to facilitate controller adjustment of command,

DQ, and DQS phase delays. DDR5 also incorporates a fly-by command bus and write leveling training.

F. SDRAM

53. Although SDRAM was not standardized formally at JEDEC, it was standardized among the SDRAM Consortium members. DDR, SDRAM, and RDRAM were all alternatives as a migration path from SDRAM with DDR ultimately becoming the mainstream DRAM device. SDRAM used narrower command/address and data paths than DDR with higher transfer rates. (Ex. 1006, Fig. 1). The busses achieved 400 Mbps transfer rates using both edges of the timing reference to capture the signals.

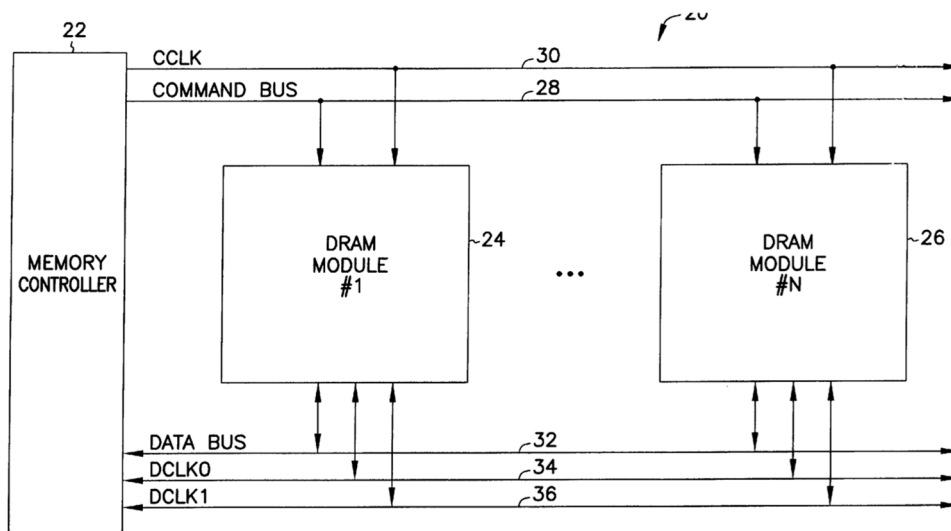


Exhibit 1006, Fig. 1

54. The commands (CA) were captured using the master clock (CCLK), the data (DQ) was captured using a gated clock (DCLK), and both busses were source synchronous. The gated clock is another name for a strobe, and it differs

from the free running clock in that it is used only during data transfers and gated on and off. Some early DDR proposals at JEDEC used the term “data clock,” but the terminology was ultimately standardized as “DQS.” The gated clock (DCLK) and DQS are one and the same; however, SDRAM uniquely had two DCLKs. A redundant DCLK allowed alternate use of DCLK0 by one device and DCLK1 by the next device ready to perform a bus transfer. This alternation improved bus efficiency by reducing the handoff time of one device driving the DCLK signal versus another device.

IX. OVERVIEW OF '835 PATENT

55. U.S. Patent No. 7,646,835 (“Rozas” or “the '835 patent”), titled *Method and system for automatically calibrating intra-cycle timing relationships for sampling signals for an integrated circuit device* was filed on November 17, 2003 and issued on January 12, 2010. The '835 patent lists Guillermo J. Rozas as the inventor and Intellectual Ventures II LLC as Assignee. (Ex. 1001). Rozas teaches a method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device by systematically altering the phases of these signals to determine a valid operating range for the integrated circuit device. Rozas uses a DDR memory system and DDR DRAMs as the exemplary embodiment, but the independent

claims are limited to command, data, and sampling signals of either an integrated circuit, a DRAM component, or a DDR DRAM component.

56. Rozas uses a simplified DDR system block diagram in Fig. 1 (Ex. 1001, Fig. 1) to show the system and the bus signals that are the focus of the invention. Rozas describes the benefits of the patent to include “the automatic calibration process as provided by embodiments of the present invention adds a significant amount of ‘extra margin’ to the specifications of a memory system.” (Ex. 1001, 3:49-51). And, “an additional benefit provided by the automatic calibration embodiments of the present invention is fact that the variable operating parameters of an integrated circuit device can be efficiently explored (e.g., varied about a specified point of operation) even in those cases where no stable initial condition is known.” (Ex. 1001, 3:65-4:3).

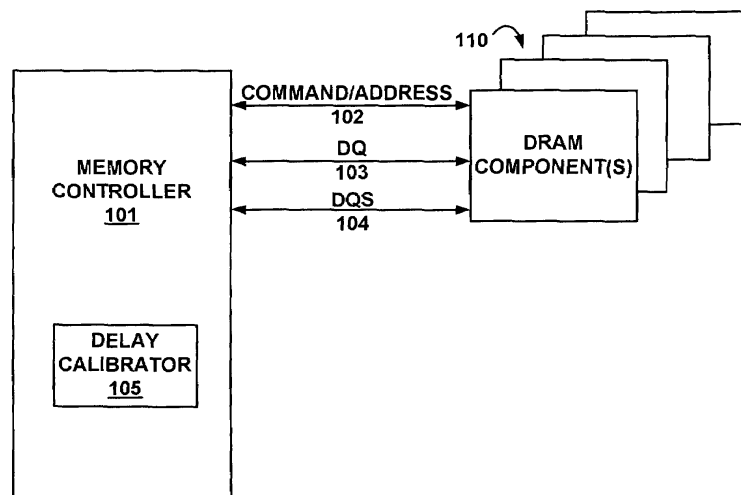


Exhibit 1001, Fig. 1

57. In Fig. 3, Rozas illustrates how the data strobe signal (DQS), which operates as a synchronizing data clock (Ex. 1012, p65), performs the shift required at the controller on memory read transactions and its timing relationship to DQ. It is understood that this example is regarding data capture timing. (Ex. 1001, Fig. 3).

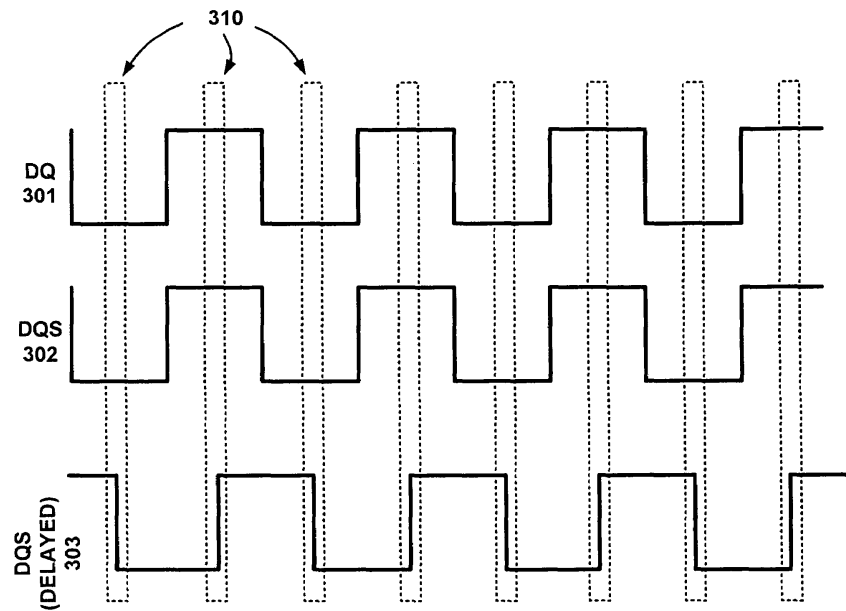


Exhibit 1001, Fig. 3

58. Rozas explains, “Embodiments of the present invention search for and find the valid region of operation within the configuration space without requiring knowledge, a-priori, where the valid region is. Thus, for example, embodiments of the present invention can automatically search the configuration space for a device (e.g., DRAM, PCB, etc.) by altering device parameters (e.g., the phase relationship between command signals, data signals, sampling signals,

etc.) to find an optimal operating point even when the device is inoperable at its supposed specified initial operating point.” (Ex. 1001, 4:10-19). Rozas shows an embodiment with the delay calibrators used to calibrate the system residing on the memory controller.

59. Rozas uses pseudo code to describe the systematic phase altering and search process used. The pseudo code is a nested for loop which moves all combination of phases until a passing eye edge is found using a three-variable systematic search. Fig. 5 depicts a drawing of the systematic search process where each of the three phase variables are plotting orthogonally to each other, and a multivariate search produces a three-dimensional window of valid operation of relative phases within the range of the phase limits. Rozas goes on to describe a multivariate coarse calibration followed by a univariate fine calibration.

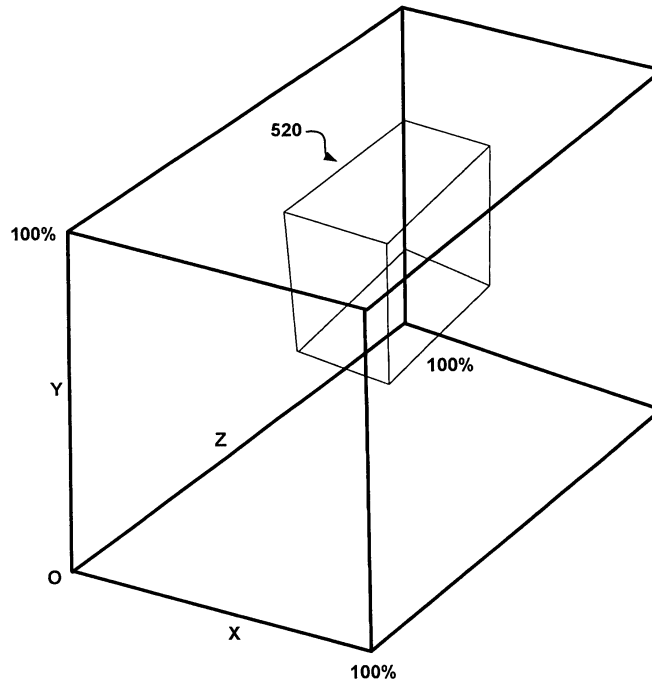


Exhibit 1001, Fig. 5

60. In this manner, Rozas systematically alters the phases of the command signal, data signals, and data sampling signals to determine the valid operation range for an integrated circuit.

X. SUMMARY OF CITED REFERENCES

A. Johnson

61. U.S. Patent No. 6,434,081 (“Johnson” or “the ’081 patent”), titled *Calibration Technique for Memory Devices*, was filed on May 12, 2000 and issued on August 13, 2002. (Ex. 1004). The ’081 patent lists Brian Johnson and Brent Keeth as the inventors and Micron Technology, Inc. as Assignee. (Ex. 1004 at 1). Johnson discloses an improved method for data capture by bit-wise aligning

the received signal bits one-by-one to improve their alignment at the input latch of a DRAM device. Johnson relies on an SLD RAM memory system and an SLD RAM device in its preferred embodiments but uses the broader application of “memory device” in the independent claims. For example, the preamble to claim 1 sets out, “a method of calibrating data paths of a *memory device*, said method comprising,” (Ex. 1004, emphasis added). Johnson describes Fig. 3 below as an exemplary SLD RAM system which the techniques can be applied,

“An SLD RAM system with which the present invention may be used is illustrated in FIG. 3. It includes a plurality of SLD RAM modules 11 *a* . . . 11 *n* which are accessed and controlled by a memory controller 13. Memory controller 13 provides a command link to each of the SLD RAM modules 11 *a* . . . 11 *n* which includes a clock signal CCLK on inverted and non-inverted clock signal paths, a 1 bit FLAG signal on a FLAG data path, and a 10 bit command bus data path CA0-9. In addition, SLD RAM input/output enabling signals SO, SI are provided from memory controller 13 in daisy chain fashion to the SLD RAM modules 11 *a* . . . 11 *n*. In addition, a bi-directional data bus DQ0-17 is provided between memory controller 13 and each of the SLD RAM modules 11 *a* . . . 11 *n*, as are bi-directional data clocks DCLK0 and DCLK1. The clock DCLK0 is used to strobe input/output data into and out of the SLD RAM modules, a process for which the DCLK1 signal path is also intermittently used.”

Ex. 1004, 3:29-47. Here, the term “intermittently used” refers to the alternation of DCLK0 and DCLK1 as described in the Background of the Technology section

(Section VIII).

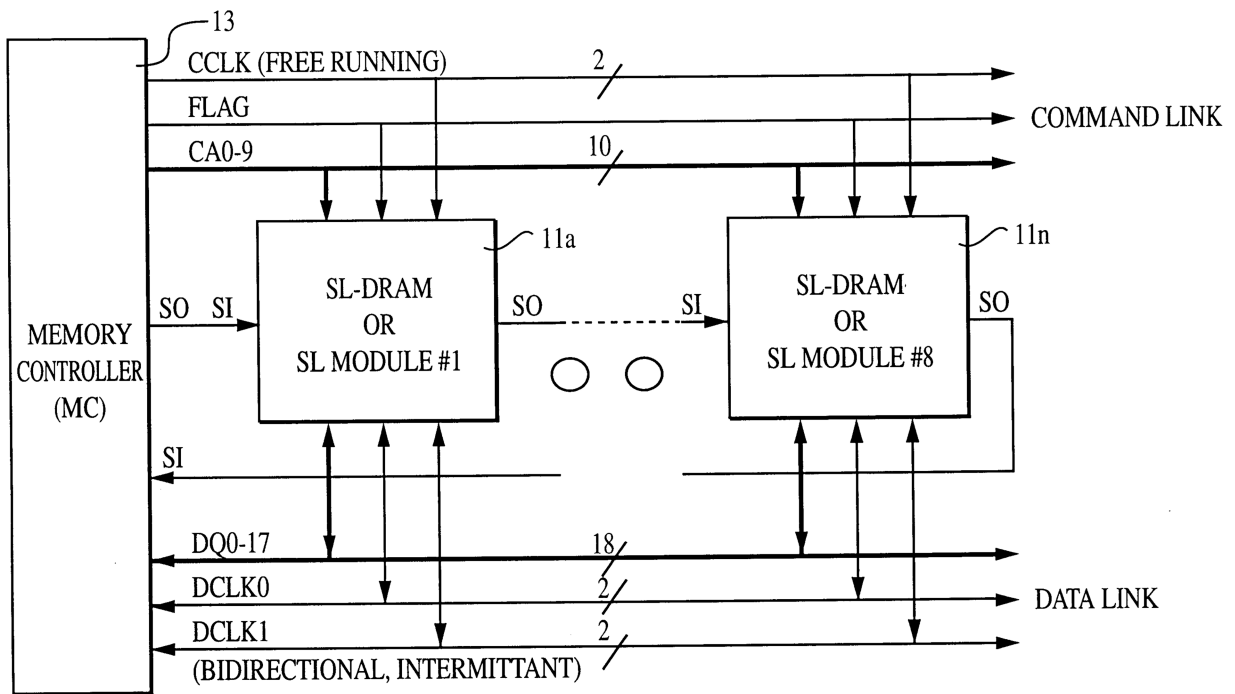


Exhibit 1004, Fig. 3

62. Johnson describes a calibration operation for the command bus, CA, and uses Fig. 1 (included below) to describe the alignment needed. In summary, Johnson aligns a received command link signal, FLAG, to the command clock, CCLK, by inserting a ring delay in the FLAG signal path. A known pattern is transmitted by the memory controller, and the calibration experiments with successive values of the ring delay to determine passing and failing delay regions by comparing the resulting latched data against the known pattern. Once the range of delays that result in correct sampling of the input signal (matches the known pattern) is known, Johnson's method determines the best delay value by

establishing the middle of the passing region, “Once a “window” of acceptable delays is found for each of the ring delays 27 and for the ring delay 29, the control logic circuit 21 determines the ‘best’ delay value as that value which is approximately in the middle of the window.” (Ex. 1004, 4:44-48). Johnson refers to this operation as serial alignment. Johnson first performs the alignment on the FLAG signal which is then used as the reference point for CA alignment. The FLAG signal is included in the same command link (bus) as the CA signals.

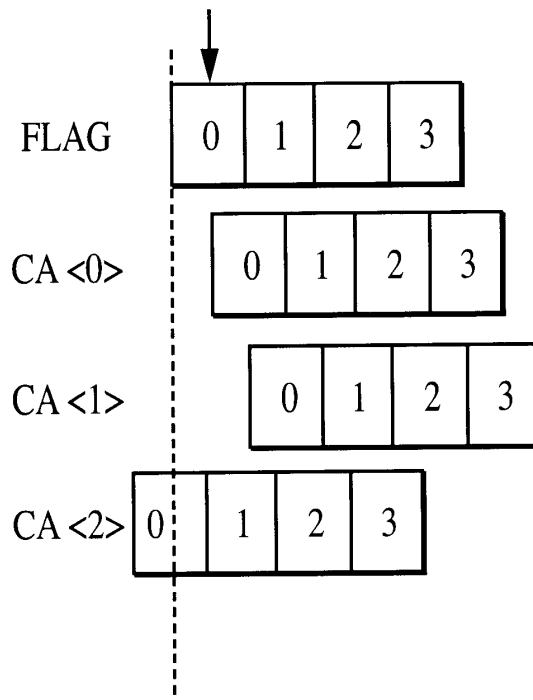


Exhibit 1004, Fig. 1

63. Instead of repeating the same alignment process for the CA signals, Johnson teaches a subsequent parallel alignment approach to eliminate the possibility of aligning the CA signals to different clock edges (rising versus

falling). Johnson accomplishes the parallel alignment by comparing the resulting captured symbols from latch 23 for the FLAG bit, to the CA signal under calibration to make sure the latch 23 and latch 25 outputs are the same. (See Ex. 1004, Fig. 4). The ring delay 27 is adjusted to match the outputs of the latch from the FLAG and CA paths. Johnson repeats this process for the remaining CA signals, so that they are all aligned in parallel to the FLAG bit. In doing so, Johnson has altered the delays of the CA signals relative to the CCLK in order to ensure proper signal bus capture.

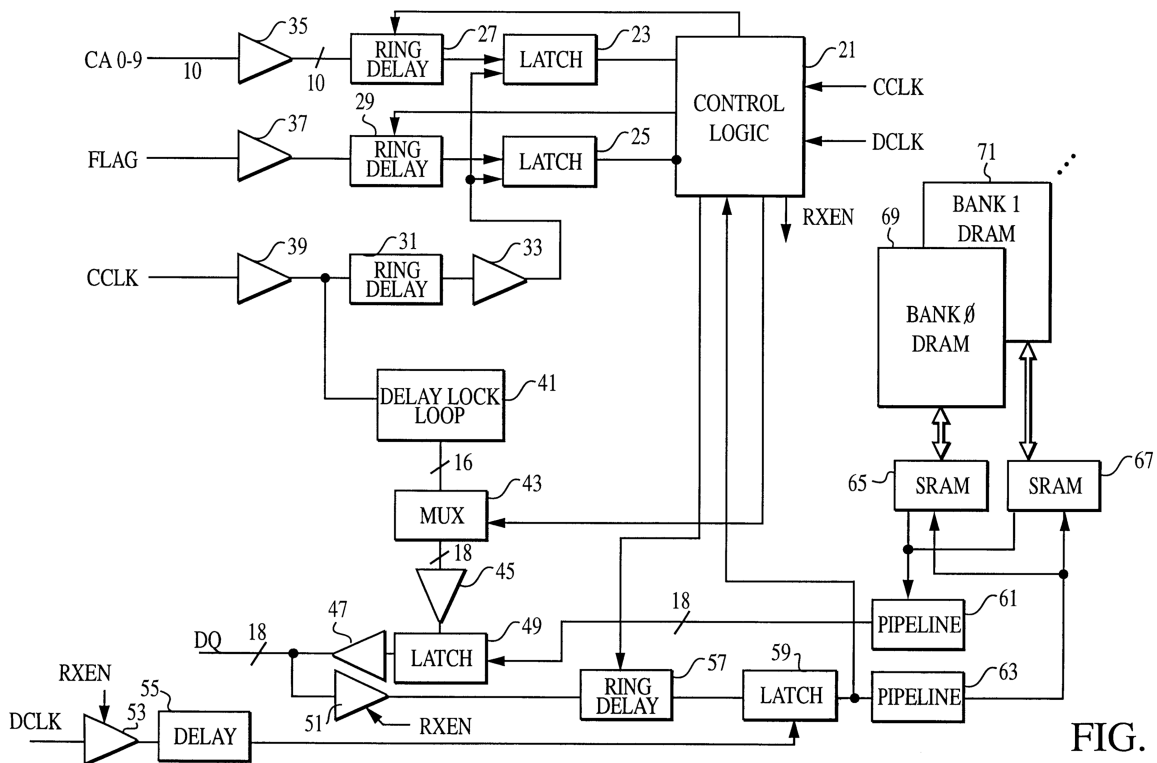


FIG. 4

Exhibit 1004, Fig. 4

64. Johnson repeats this same process for aligning the first data bit, DQ0, relative to its timing reference, DCLK. He describes this same approach at “Once a first data path, e.g., DQ0, is serially aligned to DCLK using the technique described with reference to FIGS. 1-7, the remaining DQ1-17 data paths can then be aligned by comparing the calibration pattern of a subsequent non-aligned data path to the calibration pattern which exists on a previously aligned data path.” (Ex. 1004, 7:36-43). In doing so, Johnson has altered the delays of the DQ signals relative to the DCLK in order to ensure proper signal bus capture.

B. Jeddeloh

65. U.S. Patent No. 6,629,222 (“Jeddeloh” or “the ’222 patent”), titled *Apparatus for synchronizing strobe and data signals received from a RAM*, was filed on July 13, 1999 and issued on September 30, 2003. (Ex. 1005 at 1). The ‘222 patent lists Joseph Jeddeloh as the inventor and lists Micron Technology, Inc. as Assignee. Jeddeloh teaches “a memory interface that automatically adjusts the timing between read data and an associated strobe signal returning from a memory during a read operation. The present invention also adjusts timing between the read data and an input driver enable signal.” (Ex. 1005, 1:18-23). Jeddeloh also teaches using both a coarse and a fine delay for performing the timing adjustment. Jeddeloh mentions that the memory interface “Memory 104 may be any type of memory with a clocked interface that returns data along with a strobe signal for

latching the data during read operations. This may include memory implementing the DDR interface standard.” (Ex. 1005, 3:52-55). Jeddeloh also uses DDR signal terminology in Figs. 2-4. All independent claims are limited to RAM configured to adhere to the DDR memory interface standard.

66. Jeddeloh describes a controller in Fig. 2 which receives a data and a data strobe from the memory during a read operation. In Fig. 2, Jeddeloh shows input drivers which receive the data 202 data strobe signal 206 and drive receive circuit 212.

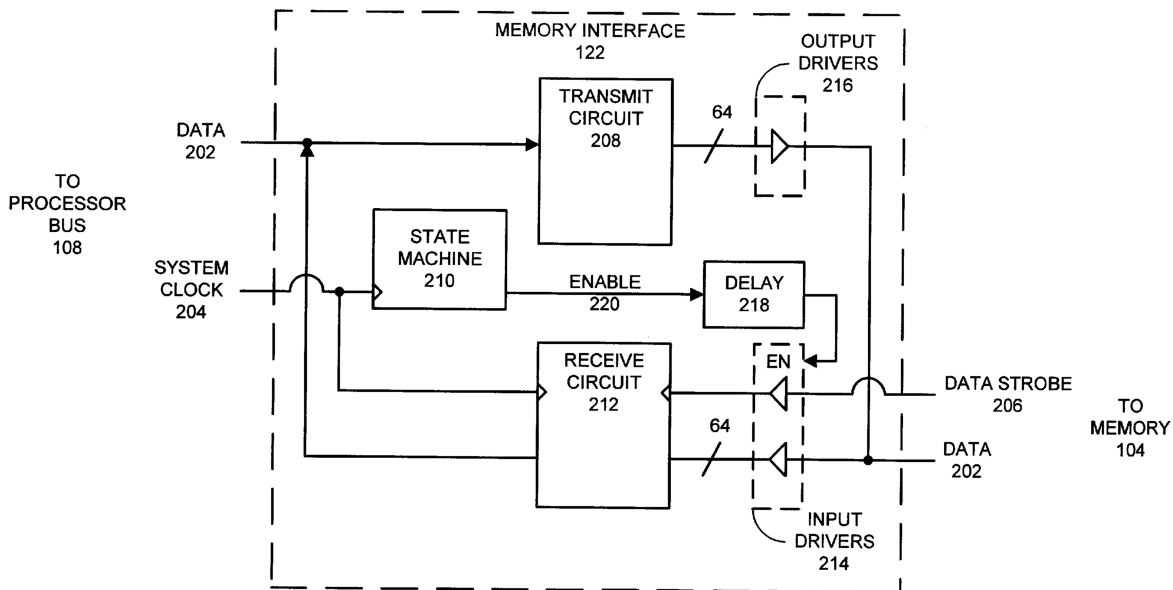


Exhibit 1005, Fig. 2

67. Jeddeloh’s Fig. 3 details the receive circuit 212 and includes the data strobe and an inverted data strobe passing through delay elements 314 and 316 before latching the data signal in a series of D flip flops (D-FFs) used for both

rising and falling edge data capture. The data signal has no delay in its path and goes directly into the data input port of the D-FF.

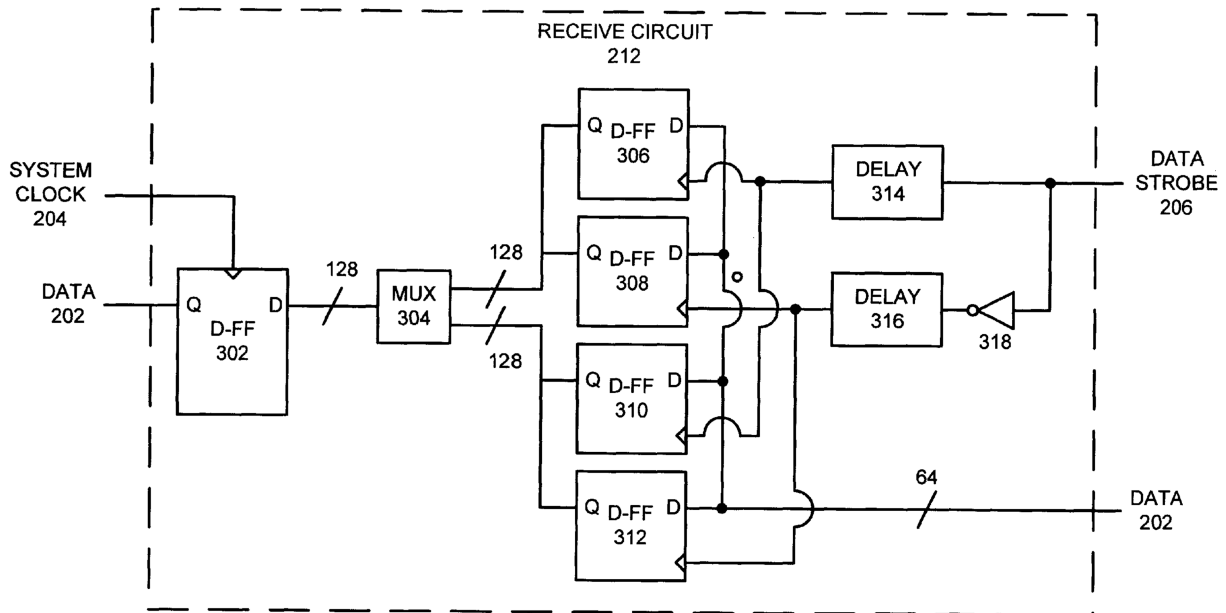


Exhibit 1005, Fig. 3

68. Jeddelloh's Fig. 4 details the delay circuit. The data strobe or the internal enable signal are passed through a series of coarse delay elements, and multiplexer (MUX) 410 which selects which coarse delay output is passed on to the fine delay block. The fine delay block is similar but uses fine delay values for the delay elements. Programmable delay registers 424 and 426 are used to choose the multiplexer settings, and therefore, the group delay of the circuitry.

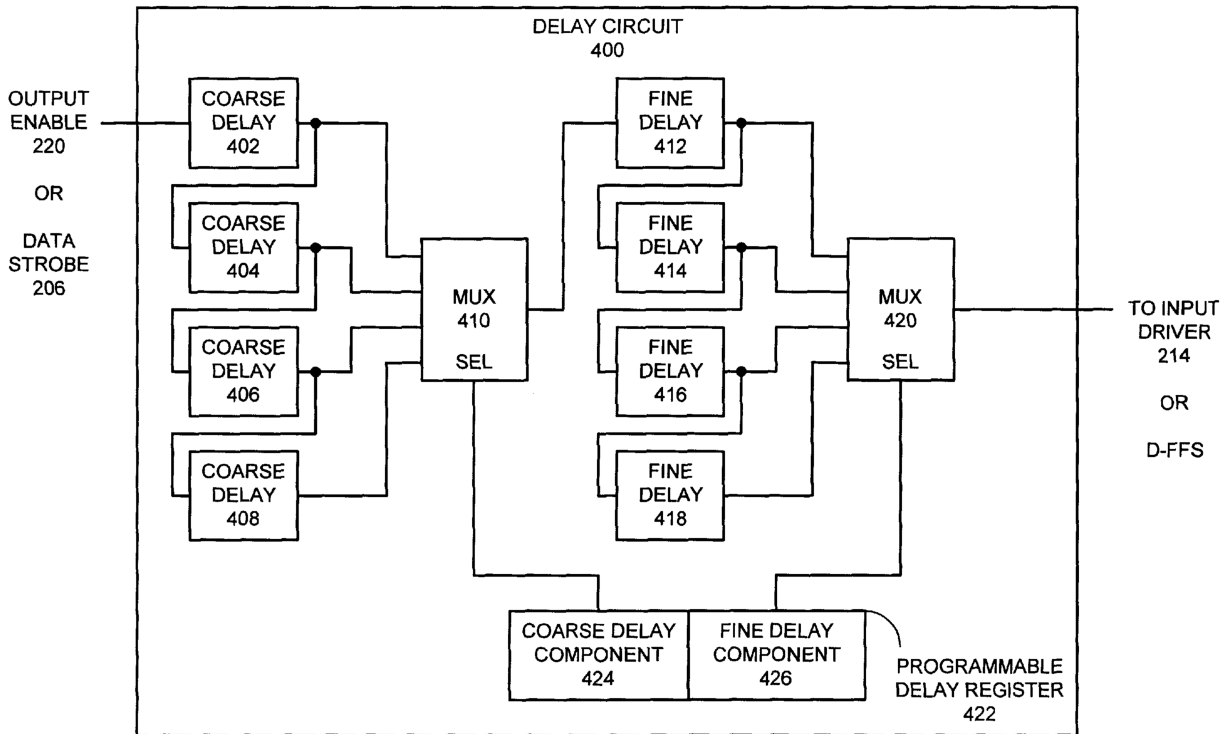


Exhibit 1005, Fig. 4

69. Jeddeloh describes how the delay values are set:

“The system first initializes the first delay value and the second delay value to their lowest possible values (step 602). Next, the system writes a random value to a target address in memory 104(step 604). The system next attempts to read the random value from the target address (step 606) and keeps a record of whether the read operation was successful. In the inner loop in FIG. 6, the system increments the second delay value (step 608) to cycle through all second delay values. In the outer loop, the system increments the first delay value (step 610) to cycle through all first delay values. After cycling through all inner and outer loops, the system has tested all possible combinations of delay values. Next, the system selects a first delay value in the middle of a valid range of first delay values, and similarly selects a second delay value from the middle of a valid range of second delay values (step 612).”

(Ex. 1005, 7:8-24). In this description, the first delay value refers to the delay setting for the enable signal. This signal is used to turn the input driver on and off

and is not primarily responsible for data capture. The second delay value refers to the delay setting of data strobe, DQS.

70. In this manner, Jeddelloh has altered the phase delay of DQS relative to DQ to find a passing region of correct data capture. Similar to Johnson, Jeddelloh chooses the center of the range to ensure accurate data capture.

C. Keeth

71. U.S. Patent No. 6,115,318 (“Keeth” or “the ’318 patent”), titled *Clock Vernier Adjustment* was filed on December 3, 1996 and issued on September 5, 2000. (Ex. 1006 at 1). The ’318 patent lists Brent Keeth as the inventor and lists Micron Technology, Inc. as Assignee. Keeth teaches,

“The vernier clock adjustment circuitry and method according to the present invention more accurately and precisely compensates for the effects of duty cycle variation, bus position of a given memory device, timing drift, loading variations, clock jitter, clock skew, noise, overshoot, and ringing by individually adjusting both the rising-edge and falling-edge timings, either independently or interdependently from each other. As a result, data is accurately clocked in the memory devices even at higher data transmission rates.”

(Ex. 1005, 2:46-55).

72. Keeth’s Fig. 1 shows the block diagram of an SDRAM memory system with controller and SDRAM modules and is essentially the same as Johnson’s Fig. 3, although Johnson’s Fig. 3 provides slightly more detail. Keeth describes essential details of an SDRAM system in agreement with Johnson, such as,

“A command bus 28 is an unidirectional bus for carrying address and control information from memory controller 22 to the DRAM modules. Address and control information is typically transferred from memory controller 22 on command bus 28 in uniform packets. For example, if a packet is four times the width of command bus 28, a command packet is transferred in four cycles on each edge of a free-running clock (CCLK) provided on a clock line 30 from memory controller 22. A data bus 32 is a bidirectional bus carrying write data from memory controller 22 to the DRAM modules and further carrying read data from the DRAM modules to memory controller 22. Two bidirectional data clocks, DCLK0 and DCLK1, are respectively provided on clock line 34 and clock line 36.”

(Ex. 1006, 3:43-56).

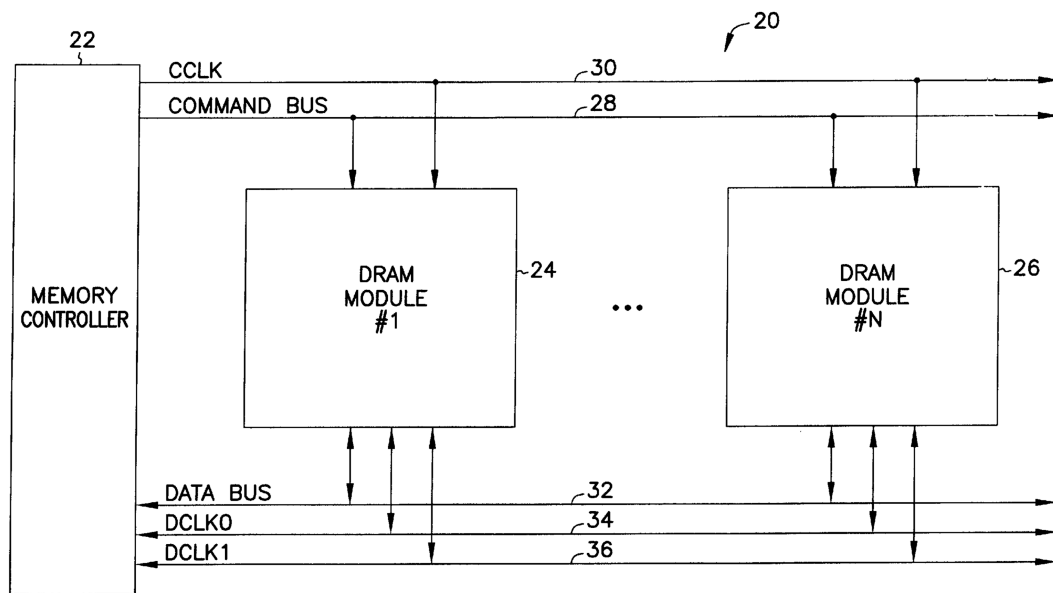


Exhibit 1006, Fig. 1

73. Keeth continues,

“Data clocks DCLK0 and DCLK1 are used to precisely transfer read data timing from the DRAM modules to the memory controller 22 and to further precisely transfer write data timing from memory controller 22 to the DRAM

modules. Both rising edge and falling edge transitions of the selected DCLK are employed to clock the input latches of the DRAM modules and memory controller receiving data. The data clocks DCLK0 and DCLK1 follow the same path as data provided on data bus 32 to reduce the effects of clock jitter, duty cycle variation, bus position, drift timing, and loading variations.”

(Ex. 1006, 3:57-67).

74. Keeth uses Figs. 3 and 5 to describe how an SLD RAM system can insert buffers in the command or data path to increase the memory capacity of the system. Keeth describes “CCLK has a falling or rising edge transition every T nanoseconds (Nsec).” (Ex. 1006, 4:20-21). A 1T period is understood to be a transfer cycle which is equal to one-half clock period for a dual-edge clocking system. Keeth goes on to inform how a system with command or data buffers will add a 2T (two transfer cycles) to the command or data path. Keeth discloses the use of the write or read verniers to add a pipeline delay in the appropriate path to equalize the delay of the inserted buffers. For example, a 2T delay can be added with a read vernier for an unbuffered data module to equalize the buffering delay of a data buffered module (see Ex. 1006, Fig. 6) so the data arrives at a similar time at the controller from any module in the system, “Thus, the read0 data arrives at the memory controller at 30 T whether or not command buffers and whether or not data buffers are used in the memory system.” (Ex. 1006, 6:42-44).

75. A vernier adjustment is a tapped delay line with fine delay resolution, “Vernier adjustment circuits 66, 70, 74, and 60 are typically implemented with

tapped delay lines. In one preferred embodiment of the invention, inverters are staged and various tapped points along the tapped delay lines provide the required variations in vernier adjustment delays. The vernier delays are optionally provided with phase-lock loop (PLL) or delayed-lock loop (DLL) circuitry where various phases are selected from different places to provide the required variations in vernier adjustment delays. The vernier clock adjustment circuits can be implemented in any suitable programmable delay elements. (Ex. 1006, 7:55-65). “A high resolution is obtained by utilizing a logic buffer delay as a time unit, and a delay-locked loop (DLL) is used to stabilize the value of the buffer delay against process variations, temperature, and power supply changes.” (Ex. 2003, p1). The vernier provides improved bus efficiency with the data driven from different DRAM modules arriving at the controller at a similar time. (See Id.).

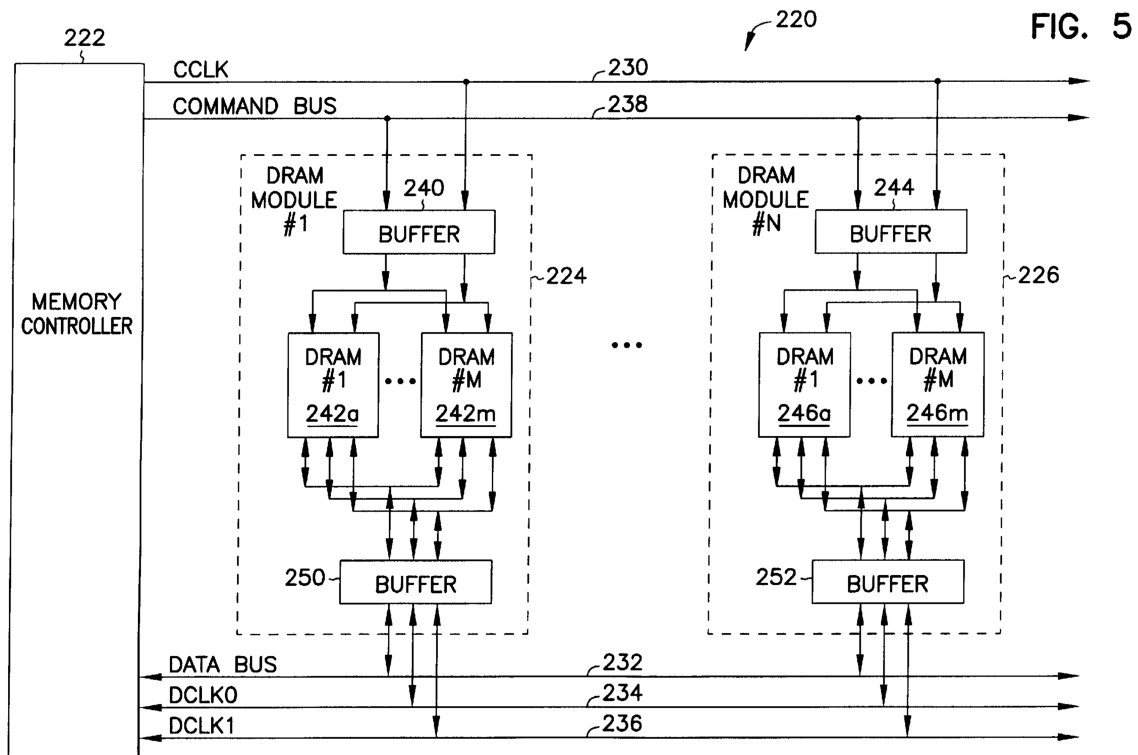


Exhibit 1006, Fig. 5

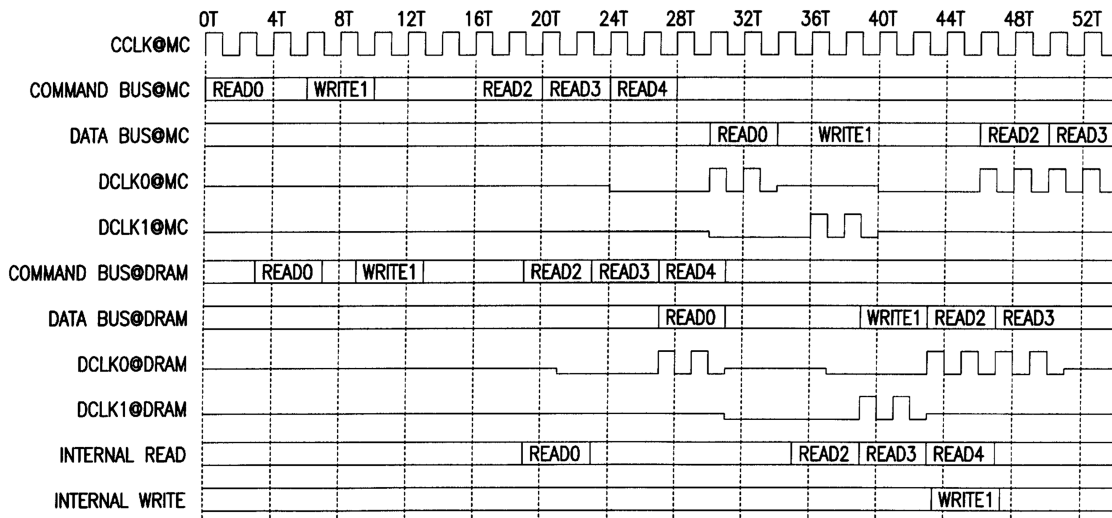


Exhibit 1006, Fig. 6

76. Referring to Keeth's Fig. 7, Keeth discloses verniers to adjust the delay of CCLK internally to align to the command bus or to clock the write and read FIFO buffers,

“DRAM module 24 includes a command latch 64 which receives commands from command bus 28. Command latch 64 receives a delayed CCLK clock from a command vernier clock adjustment circuit 66. Command vernier clock adjustment circuit 66 receives the CCLK clock signal from clock line 36. A write first-in, first-out (FIFO) buffer 68 receives the DCLK0 and DCLK1 clock signals from lines 34 and 36 and the write data from data bus 32 and provides write data to a DRAM core 76. Write FIFO buffer 68 receives a delayed CCLK clock from a write vernier clock adjustment circuit 70. Write vernier clock adjustment circuit 70 also receives the CCLK clock signal from clock line 36. A read FIFO buffer 72 receives read data from DRAM core 76 and provides the read data to data bus 32 along with the DCLK0 and DCLK1 clock signals to clock lines 34 and 36. Read FIFO buffer 72 receives a delayed CCLK clock from a read vernier clock adjustment circuit 74. Read vernier clock adjustment circuit 74 also receives the CCLK clock signal from clock line 30.”

(Ex. 1006, 7:4:23).

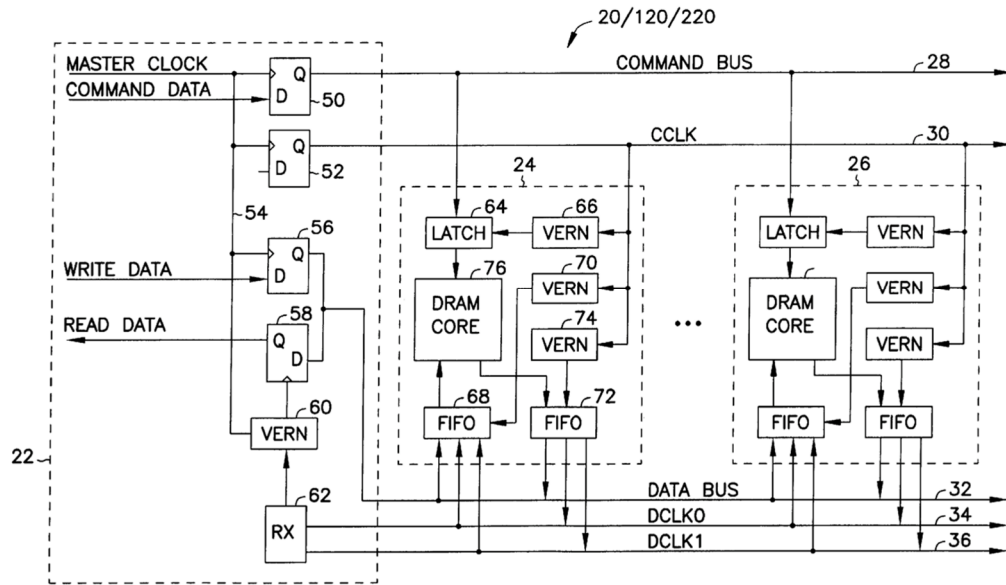


Exhibit 1006, Fig. 7

77. Keeth also describes the use of a vernier at the controller to adjust the phase of DCLK for the purpose of capturing read data at “A read data register 58 receives read data from data bus 32 and receives its clock from an optional vernier clock adjustment circuit 60. Vernier clock adjustment circuit 60 receives the master clock from line 54 and the active one of the data clocks DCLK0 or DCLK1 via a register multiplexer 62, which receives DCLK0 and DCLK1 from clock lines 34 and 36.” (Ex. 1006, 6:64-7:3).

78. Keeth describes the use of separate delays for the timing reference for falling edges versus rising edges, “In order to compensate for such problems and to properly latch incoming data into each DRAM, a second tier of vernier adjustment is added according to the present invention to the vernier adjustment circuitry in

each DRAM module to individually adjust both a clock's falling-edge timing independent of or interdependent on the clock's rising edge.” (Ex. 1006, 9:61-67).

79. In this manner, Keeth has altered the DQ phase delay relative to CCLK and independently altered the CCLK phase delay relative to commands.

XI. THE PETITION FAILS TO DEMONSTRATE THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Petition Fails to Prove That Independent Claim 1 is Obvious Over Johnson and Jeddeloh

80. The Petitioner fails to prove that independent claim 1 is obvious over Johnson and Jeddeloh for at least the following reasons.

81. First, the Petitioner relies on an incorrect mapping of command/address signals as the proposed combination’s data signals which would render the claim elements redundant. This invalid association is used to build an argument that the command/address signals phases are shifted relative to the data signal and the data sampling signal, which they are not. As such, there is no relationship identified between the three variables (command phase, data phase, and data sampling phase).

82. Second, the Petitioner fails to prove that there is a systematic altering of the three variables used to determine a valid operating point for the integrated circuit. The prior art cited moves one variable against a fixed signal independently, that is, it alters one phase shift relative to another signal to ensure correct data

capture from the signal bus. The combination of Johnson and Jeddeloh never consider or discuss a systematic way to alter the phase relationships between the three signals (variables) to determine a valid operation point for the integrated circuit.

83. Third, the Petitioner provides no plausible argument for motivation to combine these inventions of bus signal capture into a three dimensional interdependent phase alteration that includes altering the command phase to determine a valid operation point within the ranges of the three phase delays.

84. The Petitioner has redundantly mapped the command signal as both a data signal and a command signal. This association is then used to infer that the command timing reference signal, CCLK, is a data sampling signal, and then used to build an argument that there is some dependency of the command phase altering to the data and data sampling signals. The Petitioner's annotated Johnson Fig. 3, Ex. 1023, p18, highlights some of the problem. First, the annotation depicts an integrated circuit as an entire memory subsystem. Petitioner cites that Fig. 3 depicts an SDRAM system that "includes a plurality of SDRAM modules 11a...11n which are accessed and controlled by a memory controller 13." This could be a simple error when the annotation should commit to either the controller or the SDRAM as "an integrated circuit" rather than the SDRAM memory subsystem. It is not clear what the Petitioner has mapped as an integrated circuit.

85. Most importantly, the annotation to Johnson Fig. 3 incorrectly maps the CCLK signal as a sampling signal (highlighted in light blue) and the Petitioner's arguments rely on this faulty map. The Petitioner's confusion with Johnson may be due to Johnson's use of "data" in the more general sense. For example, Johnson refers to "One of the several calibration procedures which is performed in current SDRAM devices is a timing synchronization of clock signals CCLK (command clock signal) and DCLK (data clock signal) with *data* provided on an incoming command path CA and FLAG path (for the CCLK signal) and on the *data paths DQ* (for the DCLK signal)." (Ex. 1004, 1:42-47). Note that Johnson uses "data" in the general sense when he states "data provided," but he uses "data" specifically when he states "incoming *command path CA* and FLAG path (for the CCLK signal) and on the *data paths DQ* (for the DCLK signal)." (Id. emphasis added). Johnson could have used an alternate terms in the first instance such as "signal" paths, or "information," or "bus." Even in the 1990's, standardized DRAMs have had separate command and address signals from data signals, and the separation of command paths from data paths continued through the SDRAM standard which preceded SDRAM and DDR, and includes the entire DDR Technology of standards. (Ex. 1001, Figs. 3-5). A POSITA would know that RAS and CAS are command signals in the figures. (See e.g. Ex. 1012, p22, "The row address strobe (/RAS), column address strobe (/CAS), and write enable (/WE) functions are same

as those used for SDR SDRAM. Each combination of /RAS, /CAS and /WE in conjunction with chip select (/CS) at the rising edge of the clock (CK) determines the DDR SDRAM operation.”). A POSITA would know that command/address signals, such as RAS and CAS, are not data signals, and therefore, CCLK can not be a sampling signal to control sampling of the data signals. (See e.g. Id. at p22, noting the distinction between input signals classified as command/address signals (e.g., RAS and CAS) which are synchronized (captured) with the clock and data-related signals (e.g., DQ and DQS) which are not synchronized).

86. Any confusion with Johnson’s use of the “data” term would have been clarified in his detailed description. Johnson states “In addition, a bi-directional data bus DQO-17 is provided between memory controller 13 and each of the SLDRAM modules 11 a . . . 11 n, as are bi-directional data clocks DCLKO and DCLKI. The DLCK0 is used to strobe input/output data into and out of the SLDRAM modules, a process for which the DCLK1 signal path is also intermittently used” (Ex. 1004, 3:39-47). Johnson also states “Control logic circuit 21 receives and analyzes commands on the CA0-9 bus and controls the input/output (I/O) access operations of the memory banks 69, 71.” (Ex. 1004, 3:57-62). And, “The signals on each of the command bus paths CA0-9 are passed through respective adjustable ring delay circuits 27 and into respective latches 23 where the signals are latched by a CCLK signal.” (Ex. 1004, 3:63-67). A POSITA would

know that CCLK is not a sampling signal to control sampling of the data signals; rather, it is a signal that samples the command bus path. (See e.g. Ex. 1012, p22). A POSITA would know that DCLK0 and DCLK1, as data clock signals (Ex. 1004, 3:48-51), are signals used to control sampling of the data signals in an SLDRAM device. (See e.g. Ex. 1004, 1:43-48 Johnson itself noting the timing synchronization of clock signals “a timing synchronization of clock signals CCLK (command clock signal) and DCLK (data clock signal) with data provided on an incoming command path CA and FLAG path (for the CCLK signal) and on the data paths DQ (for the DCLK signal) so that incoming data is correctly sampled.”). Johnson uses “data provided” in the general sense, but it is very specific that the data path DQ signals are captured with the DCLK signal.

87. The first element of claim 1 in the '835 patent states “generating command signals to access an integrated circuit component,” which is followed by the second claim element, “accessing data signals to convey data *for* the integrated circuit component,” and the third claim element “accessing sampling signals to control sampling of *the* data signals . . .” (Ex. 1001, 6:60:65) (emphasis added). Command signals are used to access an integrated circuit component while data signals convey data for the integrated circuit component; these are two different signals with different functions. (See e.g. Ex. 1012, p22 noting the distinction between command signals and data signals; and Ex. 1008, p2 explaining bus

organization is split up between data, address, control, and chip-select). If Rozas intended command signals to also be data signals, the second claim element would be redundant. Also, had Rozas intended to include command signals as data signals, the correct language in claim element 2 would be to convey data *to*, not for, the integrated circuit component indicating a unidirectional path from controller to memory. This fact is reinforced by the specification: “The calibration process also includes accessing data signals (e.g., DQ signals) that convey data for the DRAM components, in both a data read transaction (e.g., data driven from the DRAM components 110 to the memory controller 101) and a data write transaction (e.g., data driven from the memory controller 101 to the DRAM components 110)”, Ex. 1001, 3:19-24. Also, the use of “*the* data signals” (emphasis added) in the third claim element must refer to the data signals set out in the second claim element and not the command signals described in the first claim element.

88. In the background, Rozas uses DDR memory as the exemplary memory integrated circuit device, “For example, with respect to high-performance memory integrated circuit devices (e.g., DDR memory), ensuring the reliability in the design and fabrication of high performance memory modules has become problematic for many OEMs.” and “A stable DDR memory module must provide reliability, speed, and proper timing to insure the overall system (e.g., CPU, bridge components, peripheral busses, etc.) operates at peak performance.” (Ex. 1001,

1:26-31). A POSITA would know that in a DDR memory, the DQ signals are the data signals, the DQS signals are the data sampling signals, and the Command/Address signals are the command signals. (See e.g. Ex. 1012, p22, 24).

89. Rozas description of Fig. 1 states “The system 100 embodiment implements a method for automatically calibrating intra-cycle timing relationships between command signals of the command/address bus 102, data signals of the DQ bus 103, and sampling signals of the DQS bus 104.” (Ex. 1001, 3:2-3:7).

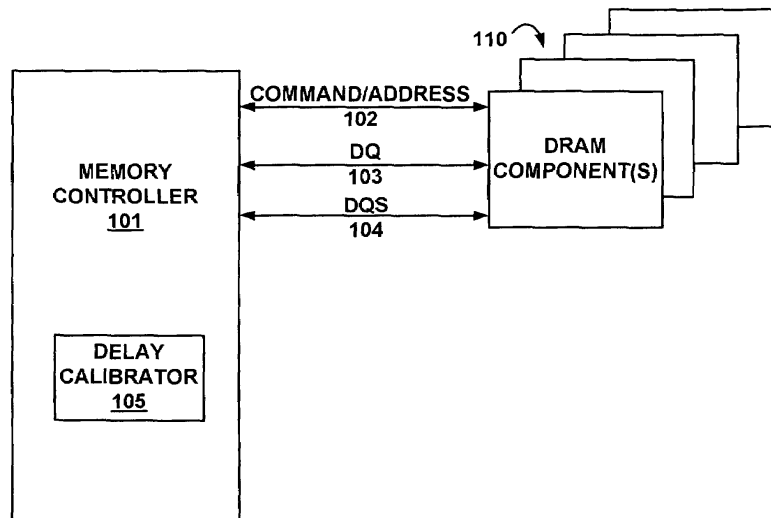


Exhibit 1001, Fig. 1

This figure would make no sense nor would the intra-cycle timing relationships make sense if the command/address bus is considered data signals. The command/address bus is called out separately. Since the command/address bus is not a data signal, then CCLK can not be considered as sampling signal that controls sampling of the data signals.

90. Rozas provides more description of the functions of these signals at “Generally, the calibration process includes generating command signals and address signals for accessing the DRAM components (e.g., DRAM chips of a memory module). The calibration process also includes accessing data signals (e.g., DQ signals) that convey data for the DRAM components, in both a data read transaction (e.g., data driven from the DRAM components 110 to the memory controller 101) and a data write transaction (e.g., data driven from the memory controller 101 to the DRAM components 110). The calibration process also includes accessing sampling signals (e.g., DQS signals) for controlling the sampling of the data signals.” (Ex. 1001, 3:15-27).

91. Rozas Fig. 5 is most representative of his invention. Rozas describes the signals which have their phases altered,

“FIG. 5 shows a diagram 500 of typical case where three parameters x, y, and z are varied across a range of adjustment to obtain valid windows for a DDR memory. As depicted in FIG. 5, the three axes of the parameters are plotted orthogonal to one another. In the case of a DDR DRAM component, for example, the x parameter can correspond to a phase range of command/address signals, the y parameter can correspond to a phase range of DQ signals, and the z parameter can correspond to a phase range of DQS signals.”

(Ex. 1001, 5:25-34). There is no doubt about the which signals would have their phases altered, and there is no mention of the clock signal. Further, if command/address were also a data signal, the figure would collapse to a two-dimensional representation of two parameters. Command/address signals are

separate and distinct from data signals. (See e.g. Ex. 1012, p22 noting the distinction between input signals classified as command/address signals (e.g., RAS and CAS) which are synchronized with the clock and data-related signals (e.g., DQ and DQS) which are not synchronized (captured) with clock).

92. Finally, the Petitioner concedes that that DCLK is the SLDRAM sampling signal for memory data in their argument at p48, “Similarly to the DCLK described in Johnson, Jeddeloh describes a “strobe signal for latching the data” for memory “implementing the DDR interface standard.” (Ex. 1005, 3:53-56; Ex. 1002, ¶16). The Petitioner also states, “For example, a POSITA would have understood that the DDR standard was already widely adopted as of November 2003” at Ex. 1023, p43. For verification, the DDR standard is recited here “Bidirectional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver.” (Ex. 1021, p5). Another concession occurs at Ex. 1023, p45, “Further, a POSITA would have been motivated to ensure that the data signals transmitted on data bus DQ0-17 adhere to the DDR DRAM standard to ensure proper compatibility with Jeddeloh’s DDR DRAM component.” The Petitioner acknowledges the equivalence of DCLK (SLDRAM) to DQS (DDR) as the sampling signal that controls data capture of the data signals DQ0-17. A POSITA would also know that the SLDRAM signals CA0-9, DQ0-17, and DCLK0-1 correspond to the DDR signals of C/A (A0-11), DQs and DQS, respectively. (See e.g. Ex. 1012, p22, 24

noting the various signals for command (CA), data (DQ) and data strobe (DQS) all have roots in DDR SDRAM).

93. The Petition fails to prove that a combination of Johnson and Jeddeloh would predict “systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device, wherein the valid operation range includes an optimal operation point for the integrated circuit device.” Johnson teaches delaying data signals to realign the bus signals to arrive the receiver at the same point in time to improve data capture, and Jeddeloh teaches delaying the data strobe at the receiver to improve the capture of data. Johnson also realigns the command signals to ensure they are captured correctly with CCLK. Both of these are simply data capture techniques to improve the margin of data setup and hold times, t_{DS} and t_{DH} , respectively (See e.g. Ex. 1021, p63 showing tabulated data set up times for various data signals). The equivalent parameter for DDR commands is t_{IS} and t_{IH} , respectively, but hereinafter, I will refer to setup and holds generally as t_{DS} and t_{DH} . (See e.g. Id. showing t_{IS} and t_{IH}). The ideas of Johnson and Jeddeloh are limited to improving data capture between two signals and neither invention or in combination addresses three-dimensionally and systematically adjusting phase delays to determine a valid operation range of an integrated circuit.

94. Johnson states

“The present invention provides correct alignment of data entering a memory module, e.g., an SDRAM module, on a plurality of incoming data paths in both a serial and parallel direction. Serial data alignment is first acquired for one of the incoming data paths, and then the remaining data paths are bit wise aligned in parallel to a previously aligned data path.”

Ex. 1004, 2:44-53. Note that Johnson also uses “data” in the general sense here. Johnson has aligned a data (DQ) to its sampling signal (DCLK) by altering the delay of the DQ signals to improve data capture of the data bus.. Nowhere does Johnson discuss altering commands relative to these signals in order to determine a valid operation range of the integrated circuit device.

95. Rozas describes how the three signal phases are systematically altered:

“FIG. 5 shows a diagram 500 of typical case where three parameters x, y, and z are varied across a range of adjustment to obtain valid windows for a DDR memory. As depicted in FIG. 5, the three axes of the parameters are plotted orthogonal to one another. In the case of a DDR DRAM component, for example, the x parameter can correspond to a phase range of command/address signals, the y parameter can correspond to a phase range of DQ signals, and the z parameter can correspond to a phase range of DQS signals.”

(Ex. 1001, 5:25-33). And,

```
“For (x=0, x<=x_limit, x+=x_step)
  For (y=0, y<=y_limit, y+=y_step)
    For (z=0, z<=z_limit, z+=z_step)
      If test(x,y,z) passes, then abort loop and remember x,y,z”
```

(Ex. 1001, 6:25-28).

96. For the sake of simplicity, we can use shorthand to describe the pseudo code. Rewritten, the code becomes:

```
For Starting at 0 degrees, increment C/A phase through its range
  For Starting at 0 degrees, increment DQ phase through its range
    For Starting at 0 degrees, increment DQS phase through its range
      If test (C/A phase, DQ phase, DQS phase) passes, then abort loop
        and remember.
```

This pseudo code is a nested For loop that searches for the early edge (closest to 0 degrees phase) of all signals in order to identify the edge of a valid operating region. This pseudo code will try every combination of phases *for all three signals until it finds a valid operation point*. This process is repeated for the late edge of the signals.

97. What Johnson describes is different. Using the shorthand pseudo code, Johnson teaches,

“this optimal delay is achieved by adjusting the temporal position of the received data bits to achieve a desired bit alignment relative to the clock. This is accomplished by adjusting a delay in the receiving path of the received data until the received data is properly sampled by the clock and recognized internally.”

(Ex. 1004, 1:59-64). It teaches this algorithm:

```
For Starting at 0 degrees, increment DQ phase through its range for one DQ
If test (DQ phase) passes, record Pass or Fail.
```

Later, Johnson aligns the remaining DQs to the first DQ which has been calibrated. Separately Johnson repeats the same pseudo loop for the CA signals, but the phase is adjusted relative to CCLK and not DQ or DCLK (DQS). Johnson then chooses

a value at the middle of a passing region at “Once a ‘window’ of acceptable delays is found for each of the ring delays 27 and for the ring delay 29, the control logic circuit 21 determines the ‘best’ delay value as that value which is approximately in the middle of the window.” (Ex. 1104, 4:44-48). Johnson has moved one variable against the data sampling signal. Independently, Johnson moves the command phase but not in reference to data or the data sampling signal. Johnson does not discuss adjusting phases of commands (or their associated CCLK) relative to DQ or to DCLK (DQS) or a systematic method for doing so, nor has he described a method for testing for the valid operating phase of commands relative to either DQ or DCLK. Further, Johnson does not discuss the necessary relationship to establish a valid operating point for the integrated circuit. Johnson also does not identify a motivation for doing so. Johnson never discusses a method of automatically calibrating intra-cycle timing relationships *between the three signals*. Instead, method is limited to adjusting a DQ phase relative to its sampling signal to improve data capture.

98. A combination with Jeddeloh does not cure the deficiencies of Johnson. Arguably, Jeddeloh alters the delay of a DQS signal after its reception from the bus; Jeddeloh does not alter the delay of DQ or commands and only alters the delay of DQS with delay element 314 or 316. (Ex. 1005, Fig. 3). There is no delay in the path of the data signal, 202, nor is this discussed.

99. Even a combination of Johnson plus Jeddeloh does not contemplate a systematic way to alter a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device. Importantly, neither Johnson nor Jeddeloh describe how phase shifts of commands are altered in relation to DQ or DQS in order to determine a valid operation region for the integrated circuit, nor do they identify a motivation for doing so. Certainly, there is no systematic adjustment of command phases to DQ (data) and DQS (data sampling signals) to determine the valid operation of a device.

100. The Petitioner states that the primary motivation to combine Johnson and Jeddeloh is for “improving alignment of signals in a memory device, as taught by Johnson”, Ex. 1023, p34 and “at least to improve synchronization of data signals and sampling signals”, Ex. 1023, p36. This makes no sense, and the Petitioner has provided no explanation for this conclusion. Johnson states that all data paths have been calibrated with his invention at Ex. 1014, 2:44-53, “Serial data alignment is first acquired for one of the incoming data paths, and then the remaining data paths are bit wise aligned in parallel to a previously aligned data path. In this way, serial and parallel calibration of all data paths is achieved”. A POSITA would know that when you align the signals relative to its timing reference (sampling signal), that all signals and its sampling signal are aligned. (See e.g. Ex. 1004, 1:42-48). There is

no additional alignment gained by altering the phase of DQS relative to the data as in Jeddeloh after the data is already properly aligned to DQS by Johnson, and doing so would be a duplication of effort involving no alteration of the already calibrated phases. As an analogy, if you align all soldiers in a rank to one target soldier, there is no need to move the position of the target soldier afterwards. Every soldier is in a line, and every signal on the bus and its sampling signal are aligned. There is no further improvement of alignment available.

101. For the sake of argument, even if it were true that subsequently adjusting the phase of DCLK relative to DQ as in Jeddeloh offered some improved alignment, these are independent delays of a signal pair, and the adjustment does nothing for aligning DQ or DQS relative to command/address. For the sake of argument, if the Petitioner argues that moving these phases plus the phase of the command/address signal against CCLK (argued by the Petitioner as a sampling signal) anticipates Rozas, the phase altering is certainly in no systematic manner. Further, neither Jeddeloh or Johnson have unveiled a motivation for doing so. These patents have demonstrated a method for capturing data from a bus and have not addressed how to systematically alter the phase of the three signals to determine a valid operation point of the integrated circuit.

102. Some corrections and clarifications should be noted to the Petition in the section for Ground 1, Claim 1. The annotation of Fig. 3 at p18 (Ex. 1023)

indicates CCLK as a sampling signal. CCLK is not a sampling signal, such as DQS, to control sampling of the data signals as explained above. All arguments relying on command signals aligning to CCLK as a data sampling signal are incorrect. (See e.g. Ex. 1012, p22 noting the distinction between sampling signals and clock input).

103. At p19, the Petitioner states “The calibration process is performed on the data paths of the command bus CA0-9 and the receive data paths of the data bus DQ.” (Ex. 1023, 4:56-58; Ex. 1002, ¶111). As a result, timing relationships between all of the command signals, data signals, and sampling signals are calibrated. (Ex. 1002, ¶111). This conclusion is incorrect. The phase delay of the command signals have been adjusted relative to CCLK (not considered a data sampling signal), and the phase delay of the data signals (DQs) have been adjusted. (See e.g. Ex. 1012, p22 noting the distinction of functions of sampling signals and clock input). There is no discussion of the timing relationship of commands to data or its strobe or how to calibrate that timing as discussed above. The timing relationships between all the command signals, data signals, and sampling signals are not calibrated.

104. The annotation of Fig. 3, Ex. 1023, p21, has modified the map of “an integrated circuit” from the mapping on p18. The mapping has changed within the independent claim. Here, the SLDRAM or SLDRAM module becomes the integrated circuit.

105. Petitioner states “Johnson discloses providing clock signals CCLK, DCLK0, and DCLK1 (the recited ‘sampling signals’).” (Ex. 1023, p26). CCLK is not a recited sampling signal as explained above.

106. Also, Fig. 3’s innotation maps CCLK as a sampling signal. Id. CCLK does not control the sampling of data as explained above.

107. At Ex. 1023, p28, Fig. 4’s innotation maps CCLK as a sampling signal. CCLK does not control the sampling of data as explained above.

108. At Ex. 1023, p28, Petitioner attempts to argue a qualified use of CCLK makes CCLK a data sampling signal at “The output data latched in latches 49” is passed “to memory controller 13 [] via data bus DQ.” (Ex. 1004, 4:5-11). CCLK therefore controls sampling of data signals at least when the data signals are output from the memory banks onto the data bus DQ. Nowhere in the ’081 patent does Johnson describe how the DLL and multiplexer cited by the Petitioner is used to make delay adjustments to sample data in his invention. Rather, Johnson uses ring delays, such as 27 and 29 in Ex. 1023, Fig. 4 to alter phase shifts, “The control logic circuit 21 steps through all possible delay positions of ring delays 27 and 29 as the data sampling is performed and stores patterns representing which delay values for the ring delays 27 and 29 provide for a correct sampling and recognition of the 2N bit pattern.” (Ex. 1004, 4:36-41). CCLK is not a sampling signal that controls the sampling of the data signals.

109. A POSITA would know that the data signals for memory devices are DQs. Johnson states,

“One of the several calibration procedures which is performed in current SLDRAM devices is a timing synchronization of clock signals CCLK (command clock signal) and DCLK (data clock signal) with data provided on an incoming command path CA and FLAG path (for the CCLK signal) and on the data paths DQ (for the DCLK signal) so that incoming data is correctly sampled”.

(Ex. 1004, 1:42-48). Again, Johnson used the general term ‘data paths’ and could have instead used ‘signal paths’ but chose not to. A POSITA would know the DCLK signal is the signal associated with the DQ sampling, CCLK is associated with the command path sampling, DCLK is the DQ sampling signal for an SLDRAM, and that DCLK is a data strobe. (See e.g. Ex. 1012, p22, 24 noting the various functions the data signal and clock input perform). A POSITA would also know that the SLDRAM DCLK is equivalent to the DDR DQS. (See Id. at 24 noting the similar functions of DQ from SDR in DDR SDRAM).

110. Also at Ex. 1023, p26, Fig. 3's innotation maps CCLK as a sampling signal. CCLK does not control the sampling of data as explained above.

111. At Ex. 1023, p29, Petitioner states “By latching or clocking data, the sampling signals CCLK, DCLK0, and DCLK1 control the sampling of the data signals.” CCLK is not a data sampling signal as discussed above.

112. Annotated Fig. 4 at Ex. 1023, p31 improperly maps CCLK as a data sampling signal. The Petitioner has changed the map to the independent claim again

by adding a plurality of internal signals as data sampling signals. This is a misunderstanding of a data sampling signal. CCLK and its derivatives are not sampling signals that control the sampling of data as previously discussed.

113. At Ex. 1023, p33, the Petitioner incorrectly states, “To the extent Patent Owner argues that Johnson does not explicitly describe stepping through delays for its CCLK or DCLK signals (each a “sampling signal”), as shown in annotated Fig. 4 above”. CCLK is not a sampling signal as defined in claim 1 of the ’835 patent as discussed above.

114. At Ex. 1023, p36, The Petitioner argues that “A POSITA would have recognized the advantages of applying Jeddeloh’s defined technique of systematically altering a phase shift of sampling signals to the delays of Johnson.” As described above, the combination of Johnson and Jeddeloh does not cure the deficiencies of Johnson. The ideas of Johnson and Jeddeloh are limited to improving data capture between two signals and neither invention addresses three-dimensionally and systematically adjusting phase delays to determine a valid operation range of an integrated circuit.

B. Petition Fails to Prove That Dependent Claims 2-6 are Obvious Over Johnson and Jeddeloh

115. Petition fails to prove that independent claim 1 is obvious, so by dependency, the Petition fails to prove obvious dependent claims 2-6.

C. Petition Fails to Prove That Independent Claim 3 is Obvious Over Johnson and Jeddeloh

116. Petition fails to prove that independent claim 1 is obvious, so by dependency, the Petition fails to prove obvious dependent claim 3. To the extent the Petitioner argues that claim 1 is anticipated, Johnson does not describe the altering the phase shifts being performed by a memory controller coupled to the DRAM component. The Petitioner concedes that “Johnson discloses that a control logic circuit 21 in each SLDRAM module ‘steps through all possible delay positions of ring delays’ to determine delay values for correct sampling and recognition of the synchronization pattern.” (Ex. 1023, p39 internal citations omitted). Petitioner also states that “Johnson explains that the memory controller ‘achieves this timing calibration at system initialization[.]’ Id. at 1:48-50.” (Ex. 1023, p39). However the Petitioner has truncated this referenced sentence. It continues after “system initialization,” “by sending continuous CCLK and DCLK transitions on those clock paths and transmitting inverted and non-inverted versions of a 15 bit repeating pseudo random SYNC pattern ‘111101011001000’ on each of the data paths DQ, the command path CA, and the FLAG path.” (Ex. 1023, p39). The full sentence explains that while the controller sends the SYNC pattern, it is the logic within the SLDRAM module that alters the phase shift by stepping through all possible delay positions of ring delays to determine delay values for correct sampling. Therefore the SLDRAM module, not the controller, is performing the phase altering.

D. Petition Fails to Prove That Independent Claim 7 is Obvious Over Johnson and Jeddeloh

117. The combination of Johnson and Jeddeloh does not anticipate a system automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device. See *supra* Section XI(A).

118. The Petitioner states, “Johnson discloses and renders obvious systematically alter a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device.” (Ex. 1023, p56). This is false. See *supra* Section XI(A).

119. The Petitioner also states, “Further, a POSITA would have understood that the delay calibrator of the Jeddeloh-modified system of Johnson would be configured to systematically alter phase shifts of all of the command signals, data signals, and sampling signals.” (Ex. 1023, p56). This is false. A Jeddeloh-modified system of Johnson does not systematically alter the phase shifts of all three signals. See *supra* Section XI(A).

E. Petition Fails to Prove That Dependent Claims 8-11 are Obvious Over Johnson and Jeddeloh

120. Petition fails to prove that independent claim 7 is obvious, so by dependency, the Petition fails to prove obvious dependent claims 8-11. See supra Section XI(D).

F. Petition Fails to Prove That Independent Claim 12 is Obvious Over Johnson and Jeddeloh

121. A combination of Johnson and Jeddeloh does not find an operating mode by altering intra-cycle timing relationships *between command* signals, data signals, and sampling signals. The combination also does not systematically alter the phase shift of the three signals to determine the valid operating range of the DRAM component. See supra Section XI(A).

G. Petition Fails to Prove That Dependent Claims 13-19 are Obvious Over Johnson and Jeddeloh

122. Petition fails to prove that independent claim 12 is obvious, so by dependency, the Petition fails to prove obvious dependent claims 13-19. See supra Section XI(F).

H. Petition Fails to Prove That Independent Claim 14 is Obvious Over Johnson and Jeddeloh

123. Petition fails to prove that independent claim 12 is obvious, so by dependency, the Petition fails to prove obvious dependent claim 14. See supra Section XI(F). Additionally for claim 14, the Petitioner states that “A POSITA would have also understood that Johnson’s phase shift calibration for the respective

signals would occur “simultaneously.” Ex. 1002, ¶209. Johnsons’s calibration technique is performed at initialization (e.g., start-up or reset). Ex. 1004, 1:36-40; Ex. 1002, ¶209. Thus, such calibration would occur all at once and before the memory system is used to ensure proper functionality of the memory system.” (Ex. 1023, p65). Johnson never discusses the calibrations on the CA signals relative to CCLK occurring simultaneously with DQ calibrations relative to the data sampling signal. The Petitioner’s sole explanation is that calibration occurs at memory initialization. A POSITA would know that DRAM calibration involves a sequential series of tasks and not a parallel execution of tasks. The Petitioner later contradicts themselves at Ex. 1023, p67, “Additionally, a POSITA would have recognized that varying the phase shifts ‘one at a time’ would conserve system resources during the calibration process and would allow the system to test delay values independently of other system changes”, Ex. 1023, p67. But this subsequent hindsight argument ignores the fact that Johnson’s calibration would only happen at memory initialization and had no indication of requiring or favoring the ‘varying phase shifts’ to one at a time.

I. Petition Fails to Prove That Independent Claim 20 is Obvious Over Johnson and Jeddeloh

124. A combination of Johnson and Jeddeloh does not find an operating mode by altering intra-cycle timing relationships *between command* signals, data signals, and sampling signals. The combination also does not systematically alter

the phase shift of the three signals to determine the valid operating range of the DRAM component. See supra Section XI(A).

J. Petition Fails to Prove That Dependent Claims 21 and 22 are Obvious Over Johnson and Jeddeloh

125. Petition fails to prove that independent claim 20 is obvious, so by dependency, the Petition fails to prove obvious dependent claims 21 and 22. See supra Section XI(I).

K. Petition Fails to Prove That Independent Claim 23 is Obvious Over Johnson and Jeddeloh

126. A combination of Johnson and Jeddeloh does not find an operating mode by altering intra-cycle timing relationships *between command* signals, data signals, and sampling signals. The combination also does not systematically alter the the phase shift of the three signals to determine the valid operating range of the DRAM component. See supra Section XI(A).

XII. GROUND 2 – JOHNSON AND KEETH

A. Petition Fails to Prove That Independent Claim 1 is Obvious Over Johnson and Keeth

127. The Petitioner uses the same arguments for Claim 1 as with Johnson in view of Jeddeloh for Claim 1. The same counter-arguments from Section XI(A) apply and are summarized below.

- a. The Petitioner relies on a faulty mapping of command signals as a data signal which creates a redundant map with a three variable claim

becoming a two variable claim. The invalid use of command as a data signal is used to imagine CCLK as a data sampling signal and therefore create a false association between command phases, data phases, and data sampling phases.

- b. Second, the Petitioner fails to prove that there is a systematic altering of the three variables used to determine a valid operating point for the integrated circuit.
- c. Third, the Petitioner fails to prove that there is a plausible motivation to combine the two inventions.

The counter-arguments have been provided in detail. See *supra* Section XI(A).

128. Some specific differences and shortcomings of the combination of Johnson-Keeth vs Johnson-Jeddeloh should be pointed out. The Petitioner again maps CCLK as a data sampling signal using Keeth Fig. 1 (Ex. 1006, Fig. 1) at Ex. 1023, p75. This figure is an SDRAM memory subsystem and is essentially the same as Johnson's Fig. 3. (Ex. 1004, Fig. 3). CCLK is the identical signal as Johnson's CCLK with the same SDRAM function, to capture commands on the command bus. Keeth confirms at

“A command bus 28 is an unidirectional bus for carrying address and control information from memory controller 22 to the DRAM modules. Address and control information is typically transferred from memory controller 22 on command bus 28 in uniform packets. For example, if a packet is four times the width of command bus 28, a command packet is transferred in four cycles

on each edge of a free-running clock (CCLK) provided on a clock line 30 from memory controller 22.”

(Ex. 1006). DCLK and the data bus have the identical functions as in Johnson, and Keeth confirms,

“Data clocks DCLK0 and DCLK1 are used to precisely transfer read data timing from the DRAM modules to the memory controller 22 and to further precisely transfer write data timing from memory controller 22 to the DRAM modules. Both rising edge and falling edge transitions of the selected DCLK are employed to clock the input latches of the DRAM modules and memory controller receiving data.”

(Ex. 1006, 4:57-63). And, “A data bus 32 is a bidirectional bus carrying write data from memory controller 22 to the DRAM modules and further carrying read data from the DRAM modules to memory controller 22.” (Ex. 1006, 4:51-54).

129. The descriptions of the functions of DQ and DQS in the '835 patent and in Keeth's description (above) of DCLK and DQS are nearly identical:

“The intra-cycle timing relationships between the command/address signals, the DQ signals, and the DQS signals are calibrated to ensure the optimal operation of the DRAM components 110. Generally, the calibration process includes generating command signals and address signals for accessing the DRAM components (e.g., DRAM chips of a memory module). The calibration process also includes accessing data signals (e.g., DQ signals) that convey data for the DRAM components, in both a data read transaction (e.g., data driven from the DRAM components 110 to the memory controller 101) and a data write transaction (e.g., data driven from the memory controller 101 to the DRAM components 110). The calibration process also includes accessing sampling signals (e.g., DQS signals) for controlling the sampling of the data signals.”

(Ex. 1001, 3:13-27). As explained above, a POSITA would understand the equivalence of data bus as the DQs, DCLK as DQS, and the commands as

commands for SDRAM vs DDR. (See e.g. Ex. 1021). Command is not a data signal, and CCLK is not a signal that controls the sampling of data.

130. The Petitioner attempts to justify the mapping of CCLK as a data sampling signal:

“Keeth states that a ‘write first- in, first-out (FIFO) buffer 68 receives the DCLK0 and DCLK1 clock signals from lines 34 and 36 and the write data from data bus 32 and provides write data to a DRAM core 76.’ (Ex-1006, 7:9-12). During write operations, write FIFO buffer 68 samples data signals from data bus 32 before the data is written to DRAM core 76. Ex-1006 at 7:10-12. Similarly, a ‘read FIFO buffer 72 receives read data from DRAM core 76 and provides the read data to data bus 32 along with the DCLK0 and DCLK1 clock signals to clock lines 34 and 36.’ Id. at 7:15-18. The read FIFO buffer 72 ‘receives a delayed CCLK clock from a read vernier clock adjustment circuit 74,’ which is used to clock read FIFO buffer 72. Id., 7:20-22; 9:15-18. Because write FIFO buffer 68 and read FIFO buffer 72 are both clocked by CCLK, CCLK controls, at least in part, sampling of the data signals read from and written to DRAM core 76. Id. at 7:12-20. CCLK is therefore a ‘sampling signal.’ Ex-1002, ¶249.”

(Ex. 1023, p77). The Petitioner’s conclusion is false. When Keeth states that a “write first- in, first-out (FIFO) buffer 68 receives the DCLK0 and DCLK1 clock signals from lines 34 and 36 and the write data from data bus 32 and provides write data to a DRAM core,” that indicates that the data bus has already been sampled and data captured by DCLK0 and DCLK1, per Keeth’s original description of the signal function. To the extent this isn’t already clear, refer back to Keeth’s explanation that “Both rising edge and falling edge transitions of the selected DCLK are employed to clock the input latches of the DRAM modules and memory controller receiving data.” (Ex. 1006, 3:60-63). From this citation, a POSITA

would understand that the data is first captured from the data bus with an input latch using its sampling signal DCLK. (See e.g. Ex. 2009, ¶ [0029]). Also, refer to Keeth's explanation of the FIFOs at "vernier adjustment circuits 70 and 74 provide delayed versions of the free-running CCLK clock to respectively clock the write FIFO buffer 68 and the read FIFO buffer 72." (Ex. 1023, 9:15-18). A POSITA would understand that Keeth is describing a data pipeline internal to the DRAM that is clocked by a derivative of its free running system clock, CCLK.

131. The Petitioner then builds on the conclusion above by stating at Ex. 1023, p78 that "A POSITA would have recognized that delaying the CCLK signal is "altering a phase shift of...the sampling signals." Annotated Fig. 7 below shows the vernier clock adjustment circuits 70 and 74 and corresponding CCLK signals. This statement is incorrect, and the Fig. 7 annotation is also incorrect.

132. For the sake of argument, if CCLK were considered a data sampling signal, then what the Petitioner describes is adjusting the phase of CCLK at "Keeth teaches that a vernier clock adjustment circuit 60 is used to adjust the timing of DCLK0 or DCLK1 for a read operation. Ex-1002, ¶247. Keeth teaches:

"rising edge and falling edge transitions of the selected DCLK are employed to clock the input latches of the [] memory controller receiving data." Ex-1006, 3:61- 63. Vernier clock adjustment circuit 60 is configured as shown in Fig. 9 to produce a delayed version of the active DCLK used for rising edge clockings and a delayed version of the active DCLK used for falling edge clockings. Id., 10:6-17; Ex-1002, ¶245."

(Ex. 1023, p76). The Petitioner fails to prove how a combination of Johnson with Keeth systematically alters the phase between all three signals to determine a valid operation point of the integrated circuit. In fact, with Keeth the Petitioner has described altering a phase of CCLK (argued as a sampling signal) relative to DCLK (also argued as a sampling signal).

133. The Petitioner uses a dictionary definition to propose that Keeth systematically alters the vernier delays and then suggests that a combination of Johnson and Keeth systematically alters the phase shift of sampling signals. This conclusion is incorrect for three reasons. The claim calls for “automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals” and “systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device.” (Ex. 1023, Claim 1).

134. First, the Petitioner has not explained how '318 or '081 calibrate intra-cycle timing relationships between all three signals. How the command phase is altered relative to data and the data sampling signal is not clear. In '081, command has been independently delayed relative to its capture signal, CCLK, but there is no discussion about the necessary phase relationship of an adjusted command signal relative to an adjusted data or data sampling signal, DCLK in either patent. Again,

Rozas calls for calibrating a three-way relationship of phases within a cycle, per its Fig. 5. (Ex. 1001, Fig. 5). Further, there is no explanation of how this adjustment is performed to find a valid operation of the integrated circuit, and certainly there is no plausible argument of how these three relationships are explored systematically to find a valid operation point.

135. Finally, since there has been no explanation in the patents about the need to find the three-way relationship, the necessary phase adjustment of Command relative to Data and DCLK, or how to explore those three variables systematically to find a valid operating point, then there would be no motivation to combine the two patents in order to cure this deficiency.

B. Petition Fails to Prove That Dependent Claims 2-3 are Obvious Over Johnson and Keeth

136. Petition fails to prove that independent claim 1 is obvious, so by dependency, the Petition fails to prove obvious dependent claims 2-3. See *supra* Section XII(A).

C. Petition Fails to Prove That Independent Claim 7 is Obvious Over Johnson and Keeth

137. See *supra* Sections XI(D), XII(A).

D. Petition Fails to Prove That Dependent Claim 8 is Obvious Over Johnson and Keeth

138. Petition fails to prove that independent claim 7 is obvious, so by dependency, the Petition fails to prove obvious dependent claim 8. See supra Sections XII(A), (C).

E. Petition Fails to Prove That Independent Claim 12 is Obvious Over Johnson and Keeth

139. See supra Sections XI(F), XII(A).

XIII. GROUND 3 – JOHNSON AND JEDDELOH AND KEETH

A. Petition Fails to Prove That Independent Claims 4-6, 9-11, and 13-19 are Obvious Over Johnson and Keeth

140. Neither Jeddeloh or Keeth, or their combination cure the deficiencies of Johnson. Specifically:

- a. The Petitioner relies on a faulty mapping of command signals as a data signal which creates a redundant map with a three variable claim becoming a two variable claim. The invalid use of command as a data signal is used to imagine CCLK as a data sampling signal and therefore create a false association between command phases, data phases, and data sampling phases. See supra Sections XI(A), XII(A).
- b. Second, the Petitioner fails to prove that there is a systematic altering of the three variables used to determine a valid operating point for the integrated circuit. See supra Sections XI(A), XII(A).

- c. Third, the Petitioner fails to prove that there is a plausible motivation to combine the three inventions. See supra Sections XI(A), XII(A).

XIV. OPINION ON THE '835 PATENT

141. One aspect of the '835 patent is arguably about optimizing data capture from a bus which is the focus of Fig. 3. Accordingly, the Petitioner has identified data capture patents as representative prior art. However, it is my opinion that '835 goes beyond optimizing the data capture of a data signal referenced to its strobe. It is remarkable that using the context of DDR, Rozas has identified the signals to be phase altered as Command, Data, and DQS. Had this been strictly a data capture patent, it would have been expected that Rozas would have used Commands referenced to CLK which is the timing reference for DDR commands, and Data referenced to DQS. Adjusting these two signal pairs could optimize the signal capture of each bus, such as in Johnson. However, Rozas is systematically optimizing the phase relationships *between the three signals* to determine a valid operating range for the integrated circuit. The phase of the Command signal does not include its timing reference clock (used to capture Command) in the signal phases to be systematically altered. I think it is quite possible that Rozas anticipated the challenge of optimizing the relationship of these signals to achieve a valid operation point at high clock rates to realize a system such as DDR3 (see Section VIII) with disparate bus topologies. Rozas invention would provide some benefit

in establish an operating point compliant with the tDSS, tDSH, and tDQSS (see Section VIII) specifications of DDR3.

XV. COMMENTS REGARDING THE PRIOR ART USED IN THE PETITION

142. A final note should be made regarding the Examiner's exposure to the prior art provided in the Petition as determined from the file history of '835 (Ex. 1003). At least as early as January, 2007, the Examiner cited patent US 6,016,282, to Keeth. It should be noted that this patent shares the identical specification to the '318 patent relied upon here, also to Keeth. In a subsequent response, the Examiner cited the '318 patent, so it was already scrutinized as relevant prior art. In fact, these patents were referenced in some of the Examiner's responses. At least as early as January, 2008, the Examiner cited patent US 2003/0122696, Johnson and Keeth ('696 patent). There is significant overlap in the specifications of this patent with Johnson '081, including sharing the same figure as '081, Fig. 3 (Ex. 1004, Fig. 3) and Fig. 4 (Ex. 1004, Fig. 4). These figures were repeatedly used and annotated by the Petitioner. The Examiner also referenced the '696 patent in multiple responses. By my count, there were six rounds of submission before '835 was allowed, and the Examiner stated his reasons for allowance:

“Claims 1-20, 22, and 25, and 26) are allowable over prior art references because related references do not disclose altering [intra]-cycle relationships between signals by altering a phase shift of command signals, a phase shift of data signals, and a phase shift of sampling [signals] to determine a valid operation range of an integrated circuit device (DRAM or DDR DRAM).”

(Ex. 1003, p19). The claim language had been adjusted multiple times to get the rather precise and specific language that avoided the prior art and led to the allowance. If the precise language is precisely mapped against prior art, this patent should survive. In my opinion, the Petition didn't exercise this precision.

XVI. CONCLUSIONS

143. Relying on my education, experience, skill and training in the relevant field of art, and after reviewing the materials identified above, it is my opinion that Petitioner has not demonstrated that the Challenged Claims are obvious based on the grounds identified in the Petition.

Executed November 27, 2024 at McCall, Idaho.


Terry R. Lee