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United States Patent [19]

Keeth

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[45] Date of Patent: Jan. 18, 2000

[54] **CLOCK VERNIER ADJUSTMENT**

[75] Inventor: **Brent Keeth**, Boise, Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[21] Appl. No.: **09/086,401**

[22] Filed: **May 28, 1998**

[51] **Int. Cl.**[7] **G11C 13/00**

[52] **U.S. Cl.** **365/233**; 365/189.05; 365/230.06; 365/230.08

[58] **Field of Search** 365/233, 189.01, 365/230.06, 230.08

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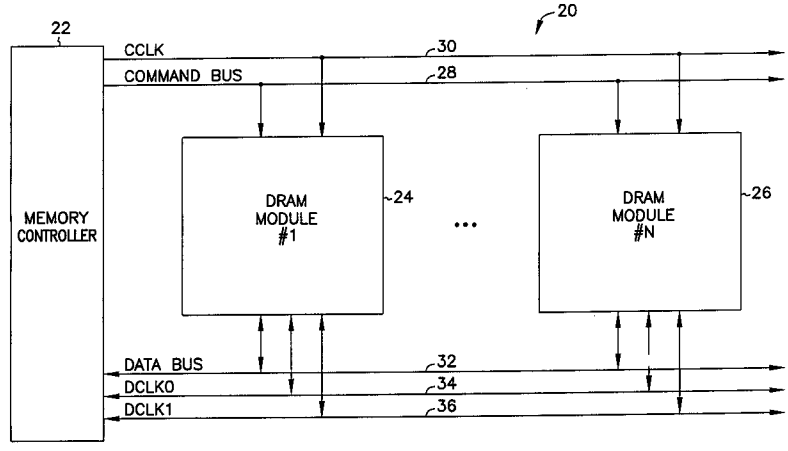
Attorney, Agent, or Firm—Seed and Berry LLP

[57] **ABSTRACT**

A integrated circuit, such as a memory integrated circuit, includes a vernier clock adjustment circuit receiving an input clock signal and providing a rising-edge clock signal representing the input clock signal delayed by a rising-edge delay and providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay. An edge triggered circuit receives data and the rising-edge and falling-edge clock signals, and stores data at the rising-edge of the rising-edge clock signal and at the falling-edge of the falling-edge clock signal. One form of the invention is a memory system having a memory controller coupled to memory modules through data and command busses. Each memory module includes the vernier clock adjustment circuitry.

62 Claims, 9 Drawing Sheets



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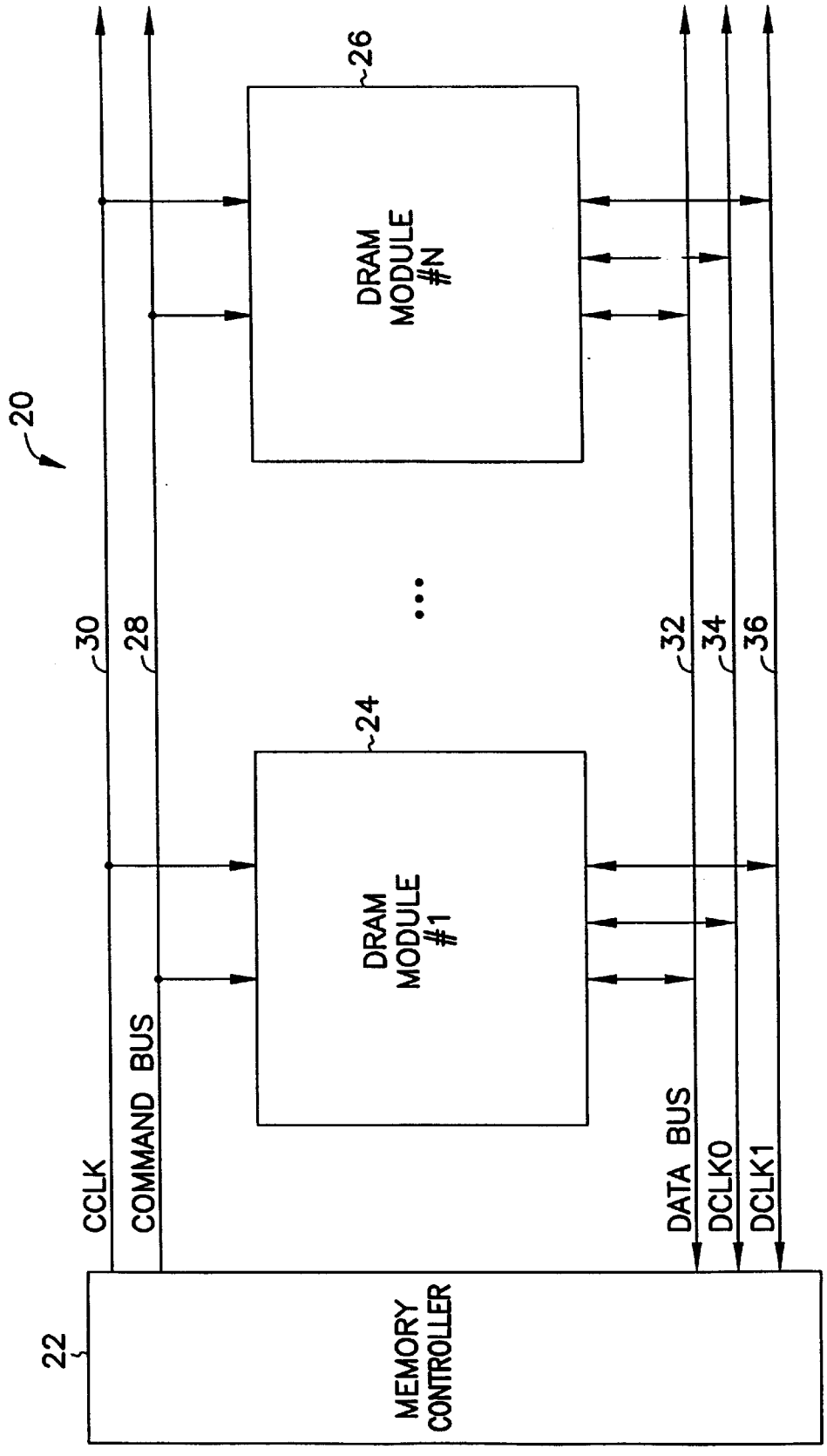

20
22
MEMORY CONTROLLER
CCLK
COMMAND BUS
DATA BUS
DCLK0
DCLK1
30
28
32
34
36
24
DRAM MODULE #1
26
DRAM MODULE #N

FIG. 1

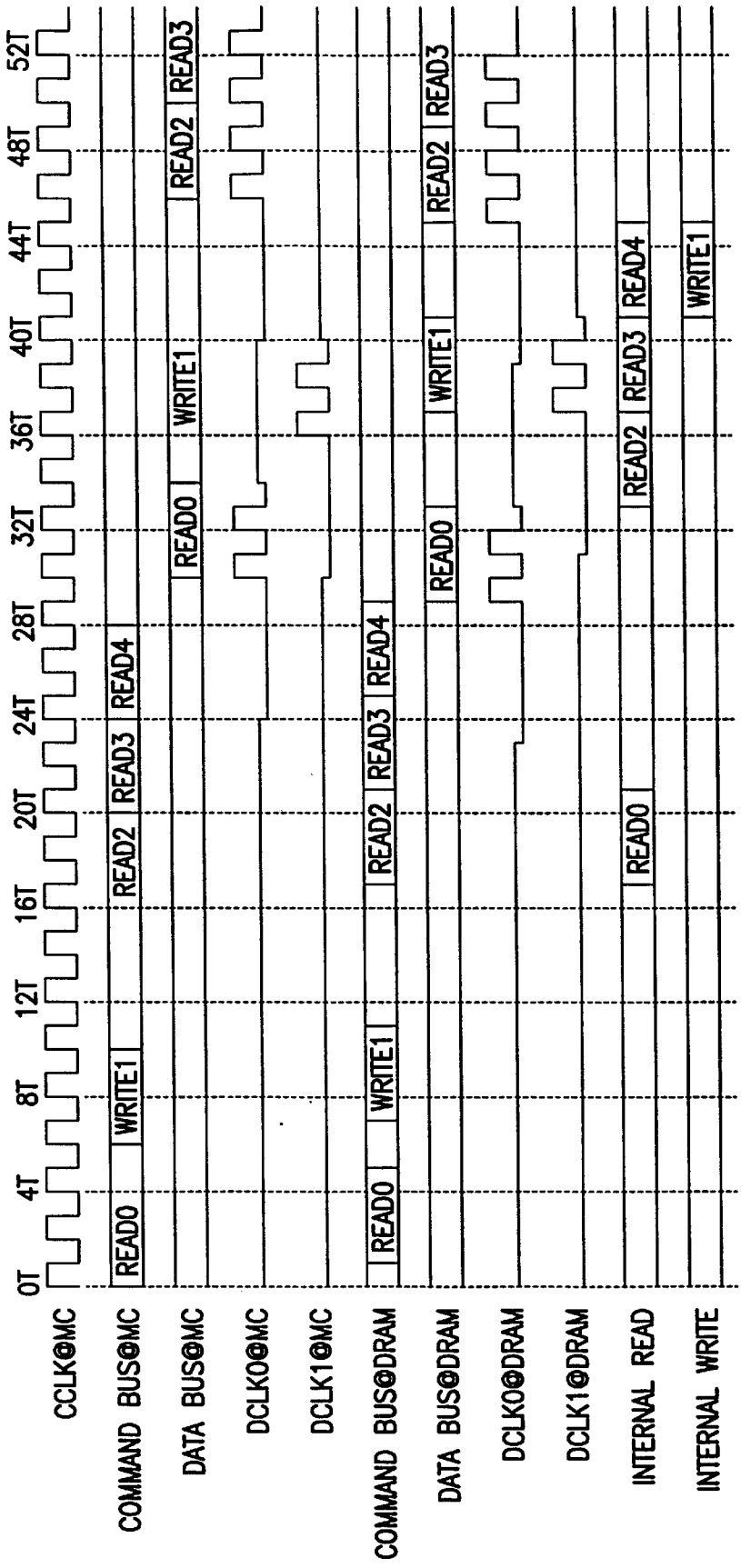

0T
4T
8T
12T
16T
20T
24T
28T
32T
36T
40T
44T
48T
52T
CCLK@MC
COMMAND BUS@MC
DATA BUS@MC
DCLK0@MC
DCLK1@MC
COMMAND BUS@DRAM
DATA BUS@DRAM
DCLK0@DRAM
DCLK1@DRAM
INTERNAL READ
INTERNAL WRITE
READ0
WRITE1
READ2
READ3
READ4
READ0
WRITE1
READ2
READ3
READ4
READ0
WRITE1
READ2
READ3
READ4
READ0
WRITE1
READ2
READ3
READ4
READ0
WRITE1

FIG. 2

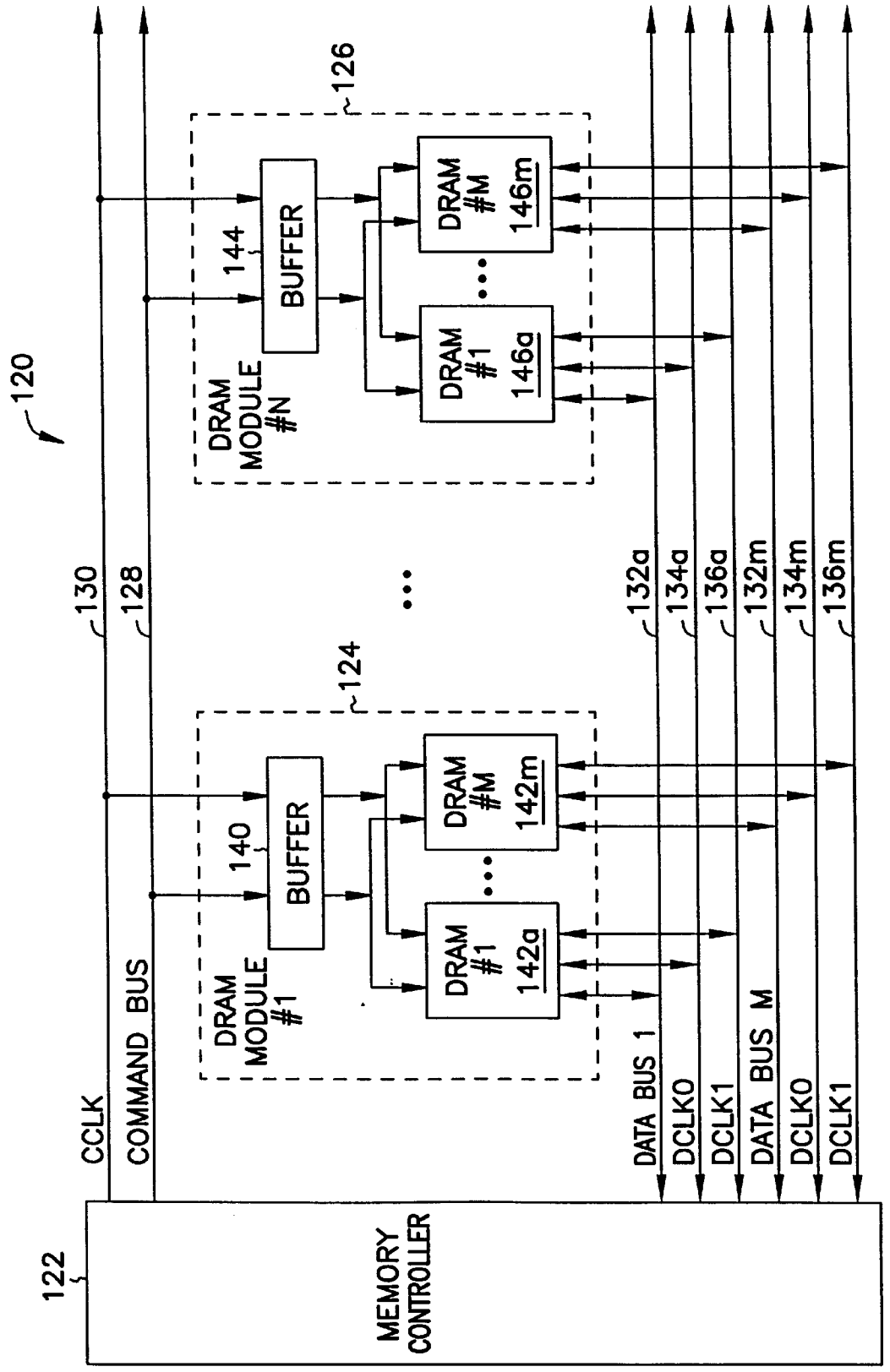

120
122
MEMORY CONTROLLER
CCLK
COMMAND BUS
130
128
DRAM MODULE #1
140
BUFFER
DRAM #1 142a
DRAM #M 142m
124
DRAM MODULE #N
144
BUFFER
DRAM #1 146a
DRAM #M 146m
126
DATA BUS 1
DCLK0
DCLK1
DATA BUS M
DCLK0
DCLK1
132a
134a
136a
132m
134m
136m

FIG. 3

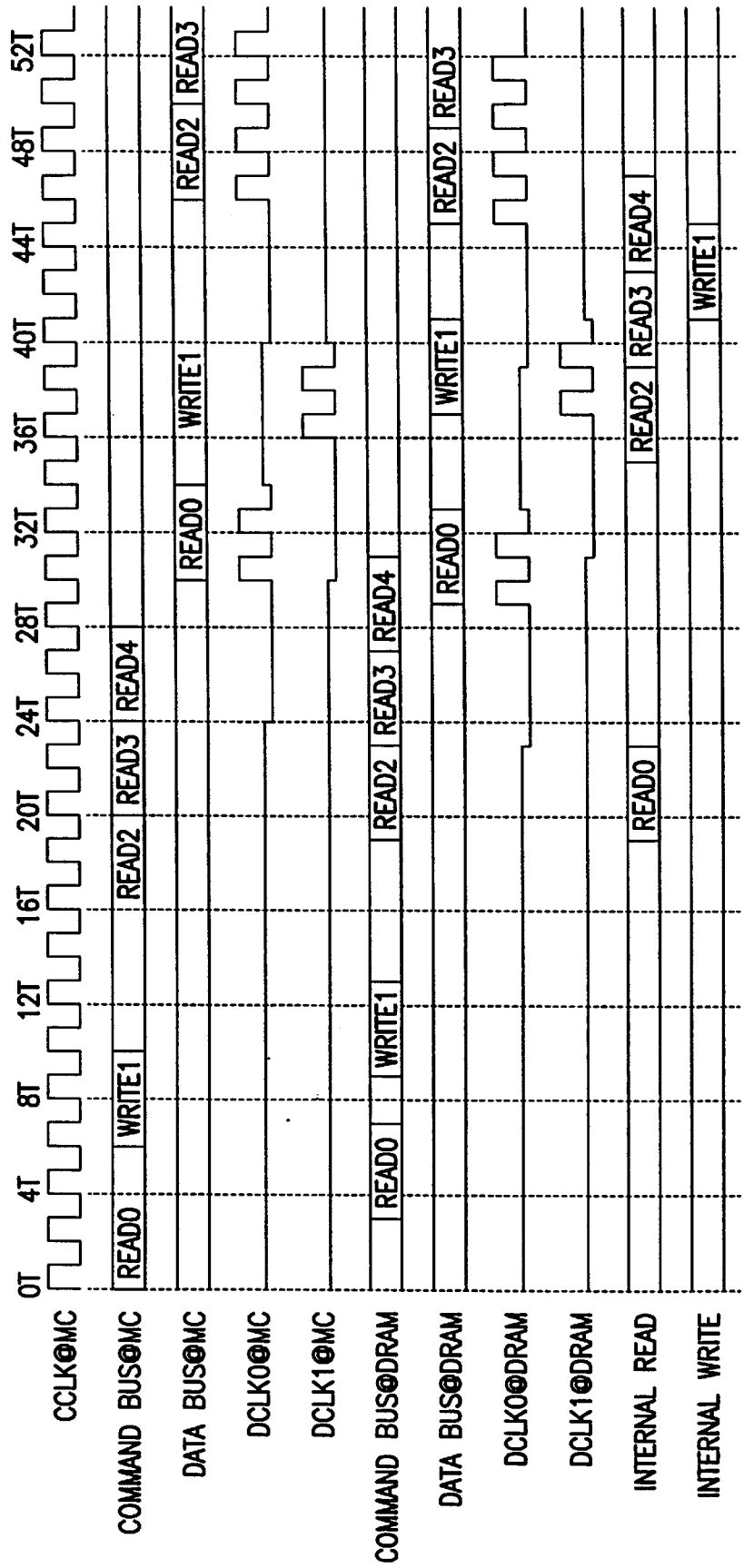
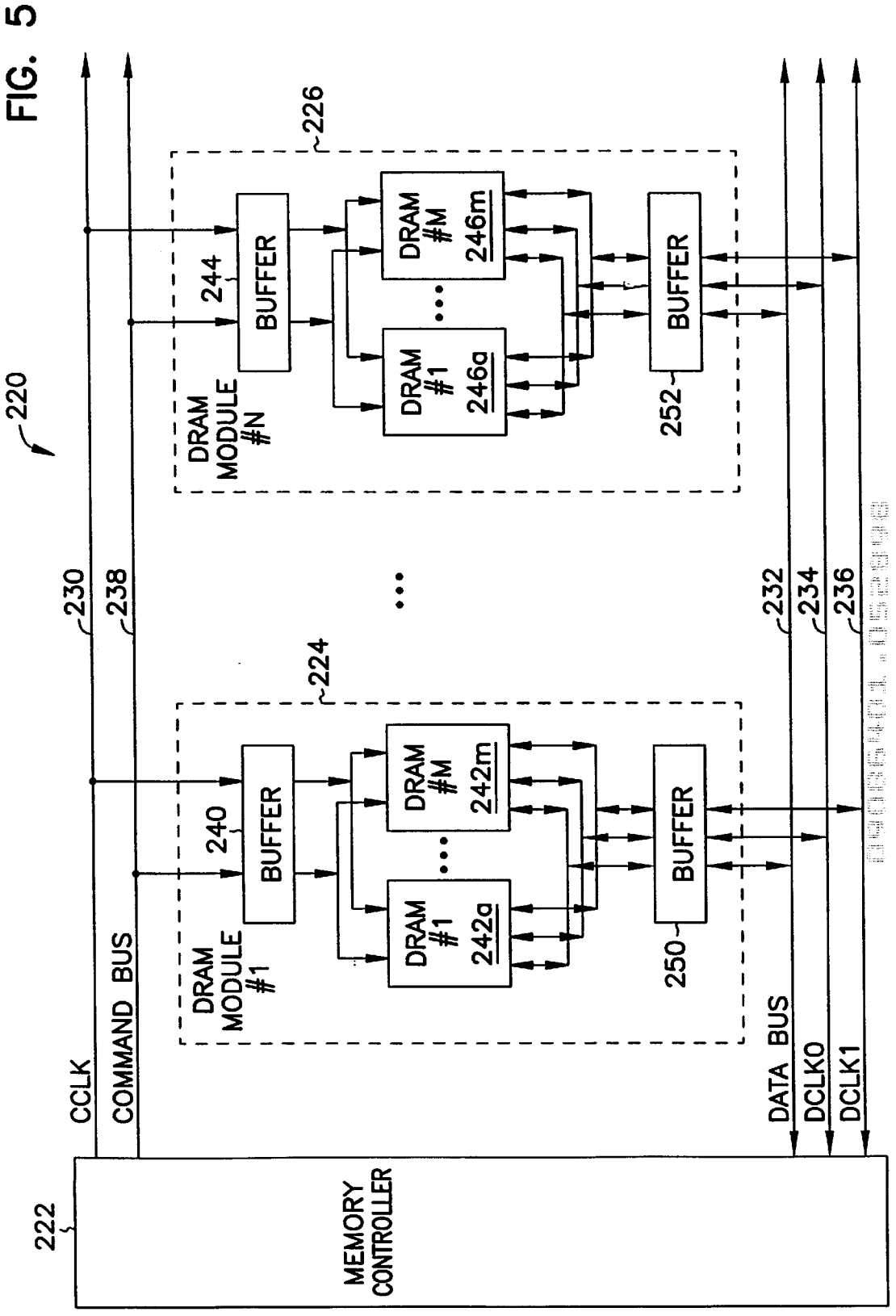

0T
4T
8T
12T
16T
20T
24T
28T
32T
36T
40T
44T
48T
52T
CCLK@MC
COMMAND BUS@MC
READ0
WRITE1
READ2
READ3
READ4
DATA BUS@MC
READ0
WRITE1
READ2
READ3
DCLK0@MC
DCLK1@MC
COMMAND BUS@DRAM
READ0
WRITE1
READ2
READ3
READ4
DATA BUS@DRAM
READ0
WRITE1
READ2
READ3
DCLK0@DRAM
DCLK1@DRAM
INTERNAL READ
READ0
READ2
READ3
READ4
INTERNAL WRITE
WRITE1

FIG. 4

FIG. 5


220
222
MEMORY CONTROLLER
CCLK
COMMAND BUS
230
238
DATA BUS
DCLK0
DCLK1
232
234
236
DRAM MODULE #1
224
240
BUFFER
DRAM #1 242a
DRAM #M 242m
250
DRAM MODULE #N
226
244
BUFFER
DRAM #1 246a
DRAM #M 246m
252

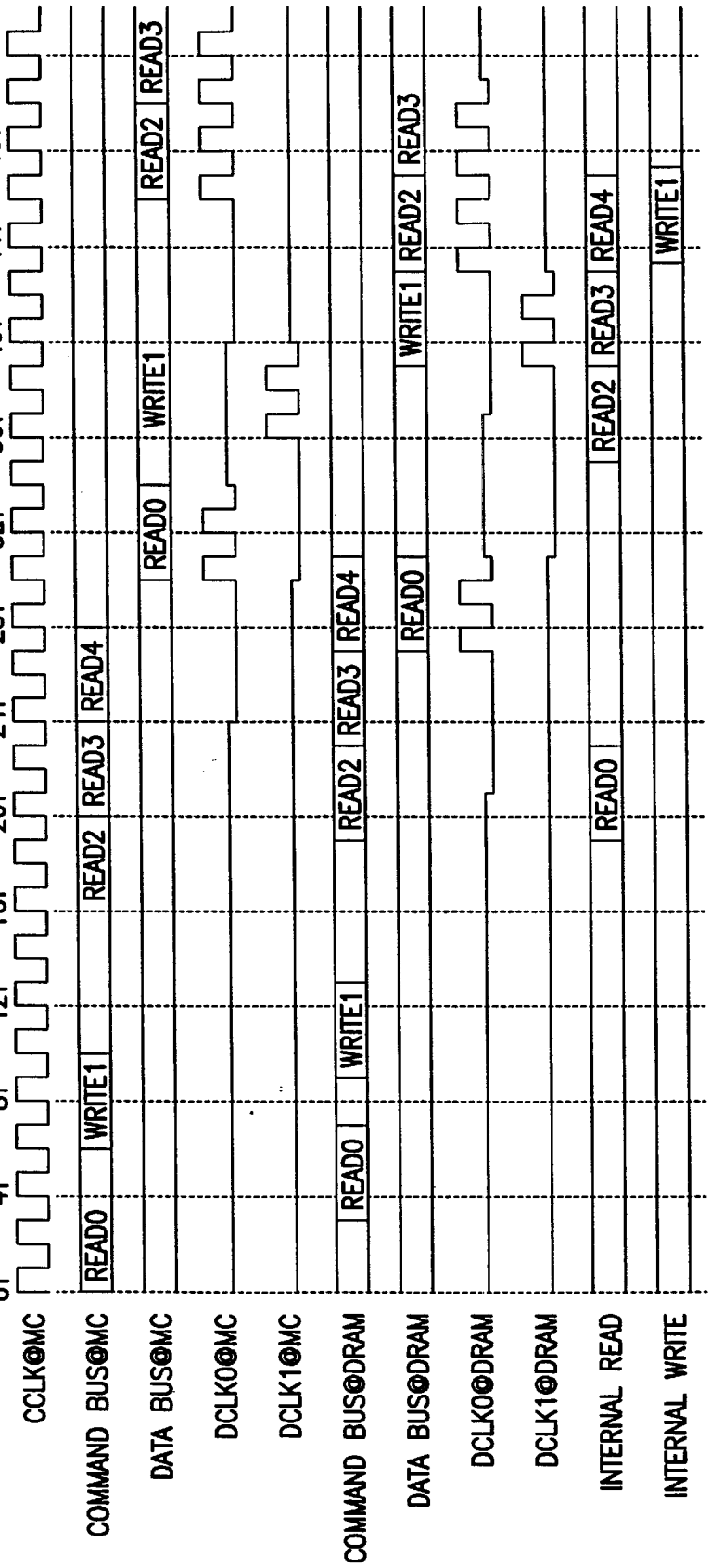

0T
4T
8T
12T
16T
20T
24T
28T
32T
36T
40T
44T
48T
52T
CCLK@MC
COMMAND BUS@MC
READ0
WRITE1
READ2
READ3
READ4
DATA BUS@MC
READ0
WRITE1
READ2
READ3
DCLK0@MC
DCLK1@MC
COMMAND BUS@DRAM
READ0
WRITE1
READ2
READ3
READ4
DATA BUS@DRAM
READ0
WRITE1
READ2
READ3
DCLK0@DRAM
DCLK1@DRAM
INTERNAL READ
READ0
READ2
READ3
READ4
INTERNAL WRITE
WRITE1

FIG. 6

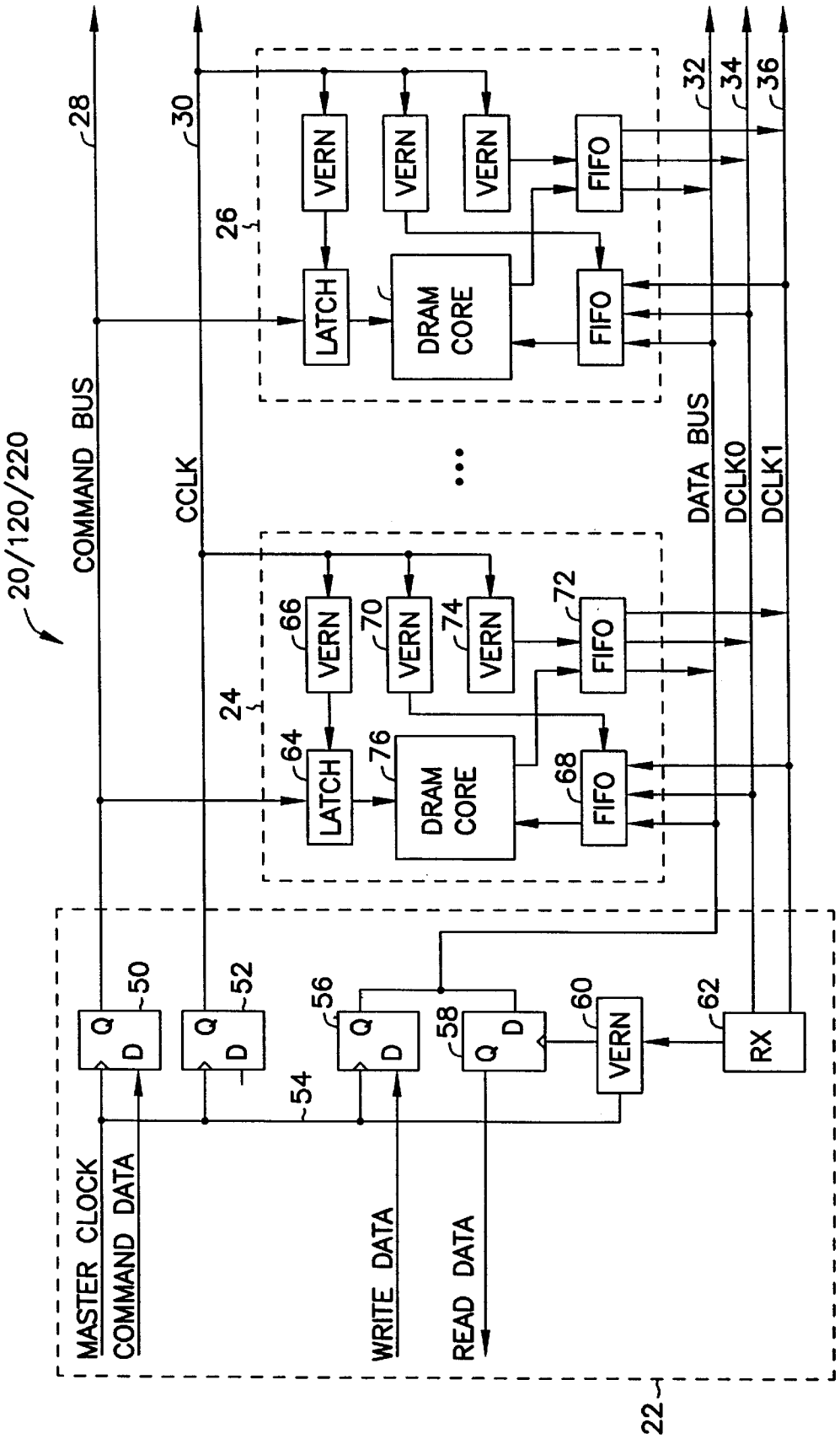

20/120/220
COMMAND BUS
CCLK
DATA BUS
DCLK0
DCLK1
28
30
32
34
36
26
24
VERN
FIFO
LATCH
DRAM CORE
64
66
68
70
72
74
76
50
52
54
56
58
60
62
RX
MASTER CLOCK
COMMAND DATA
WRITE DATA
READ DATA
22

FIG. 7

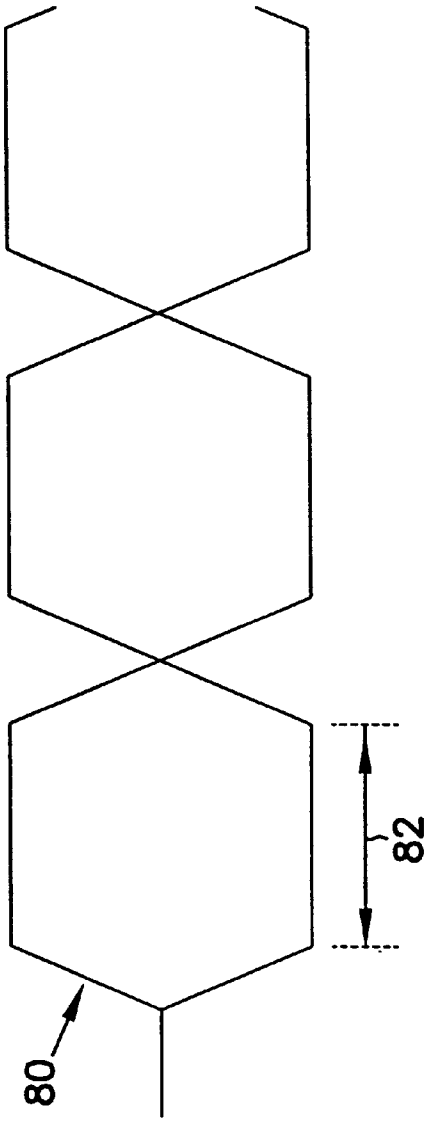


FIG. 8A

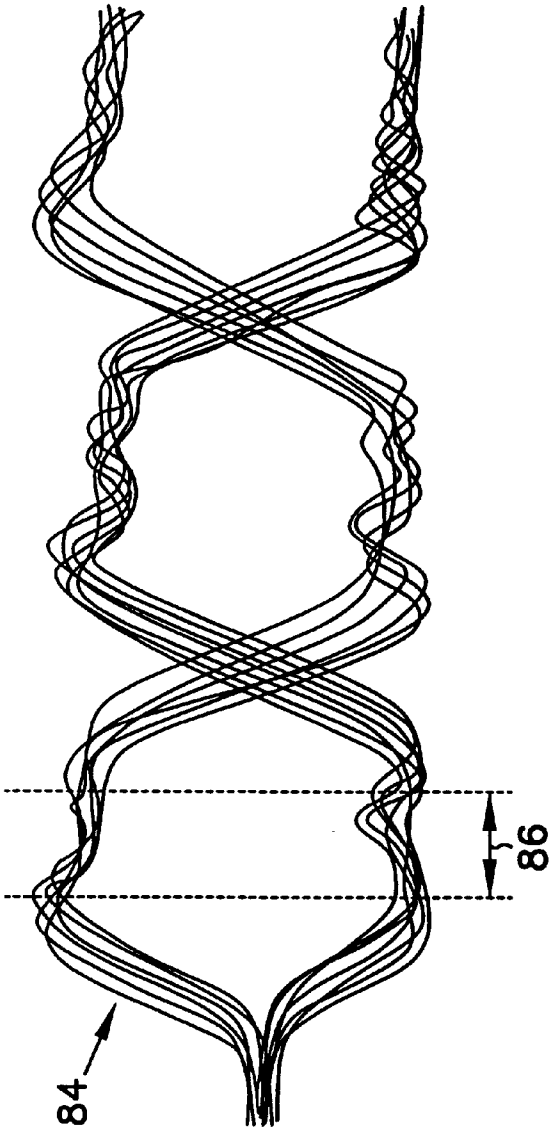


FIG. 8B

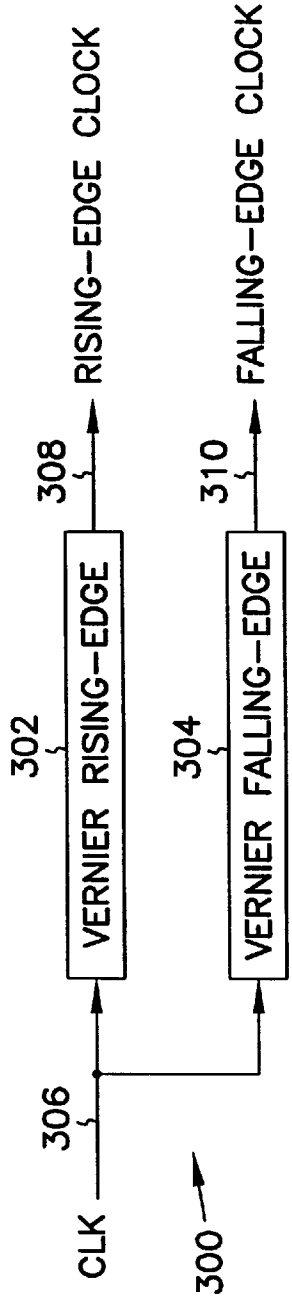

CLK
300
306
VERNIER RISING-EDGE
302
308
RISING-EDGE CLOCK
VERNIER FALLING-EDGE
304
310
FALLING-EDGE CLOCK

FIG. 9

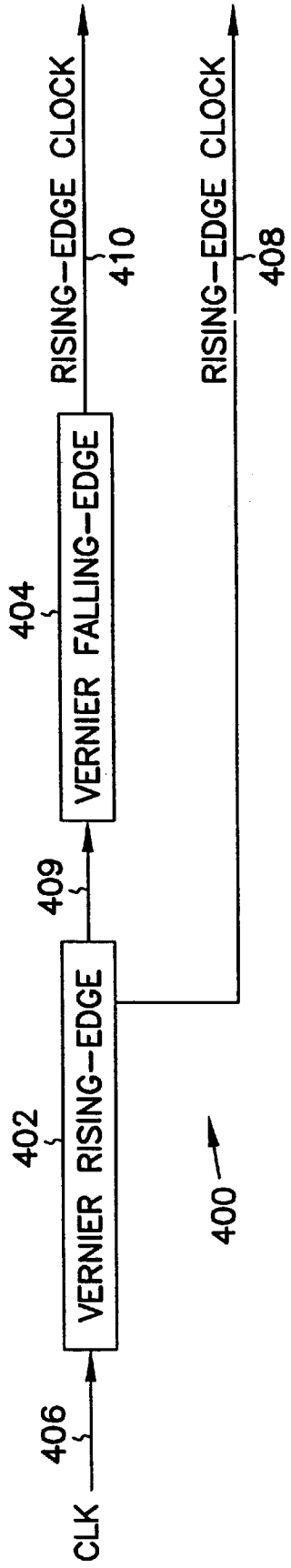

CLK
406
VERNIER RISING-EDGE
402
409
VERNIER FALLING-EDGE
404
RISING-EDGE CLOCK
410
RISING-EDGE CLOCK
408
400

FIG. 10

CLOCK VERNIER ADJUSTMENT

THE FIELD OF THE INVENTION

The present invention relates generally to integrated circuits, and more particularly to clock adjustments in memory systems, such as memory systems including dynamic random access memories (DRAMs).

BACKGROUND OF THE INVENTION

Integrated circuits typically include a number of input/output pins which are used for communication with additional circuitry. For example, an integrated memory device, such as a dynamic random access memory (DRAM), includes both control inputs for receiving memory operation control signals, and data pins for bi-directional data communication with an external system or processor.

The data transmission rate of modem integrated circuits is primarily limited by internal circuitry operating speeds. That is, communication networks have been developed which can transmit signals between circuitry at a rate that is faster than the capacity of many integrated circuits. To address the need for faster circuits, a group of integrated circuits can be combined on a common bus and be controlled by a common controller. In this configuration, each integrated circuit operates in a coordinated manner with the other integrated circuits to share data which is transmitted at a high speed. For example, a group of memory devices, such as DRAMs, static RAMs, or read only memories (ROM), can be connected to a common data bus and be controlled by a memory controller to form a memory system. The data rate of the bus may be substantially faster than the feasible operating speed of the individual memories. Each memory, therefore, is operated so that while one memory is processing received data, another memory is receiving new data. Such a memory system with an appropriate number of memory devices and an efficient memory controller can achieve very high speed data transmissions.

As the transmission rate of the data communication signals in such memory systems continues to increase, new circuitry and methods are needed to accurately clock command data, write data, and read data transmitted between the memory controller and the memory devices. The portion of a clock cycle which can be devoted to clocking valid data becomes quite small, and errors in clocking data can occur, at these increased transmission speeds because of known effects such as duty cycle variation, bus position of a given memory device, timing drift, loading variations, clock jitter, clock skew, noise, overshoot, and ringing.

Therefore, for the reasons stated above, and for other reasons presented in greater detail in the Description of the Preferred Embodiments section of the present specification, there is a need in the art for a memory system which more accurately and precisely compensates for such effects as duty cycle variation, bus position of a given memory device, timing drift, loading variations, clock jitter, clock skew, noise, overshoot, and ringing so that data can be accurately clocked in the memory devices.

SUMMARY OF THE INVENTION

The present invention provides a method and integrated circuit including a vernier clock adjustment circuit receiving an input clock signal and providing a rising-edge clock signal representing the input clock signal delayed by a rising-edge delay and providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay. An edge triggered circuit receives data and the rising-edge and falling-edge clock signals, and stores data at the rising-edge of the rising-edge clock signal and at the falling-edge of the falling-edge clock signal.

In one embodiment of the integrated circuit according to the present invention, the rising-edge and falling-edge delays are programmable delays.

In one embodiment of the integrated circuit of the present invention a rising-edge delay circuit receiving the input clock signal and independently provides the rising-edge clock signal, and a falling-edge delay circuit receiving the input clock signal and independently provides the falling-edge clock signal. In another embodiment of the integrated circuit, a rising-edge delay circuit receives the input clock signal and provides the rising-edge clock signal, and a falling-edge delay circuit receives the rising-edge clock signal and providing the falling-edge clock signal. In another embodiment of the integrated circuit, a falling-edge delay circuit receives the input clock signal and provides the falling-edge clock signal, and a rising-edge delay circuit receives the falling-edge clock signal and provides the rising-edge clock signal.

One form of the present invention is a memory system including a memory controller and memory modules for storing data. A data bus carries write data from the memory controller to the memory modules and carries read data from the memory modules to the memory controller. A command bus carries commands from the memory controller to the memory modules. A clock line carries an input clock signal from the memory controller to the memory modules. Each memory module includes at least one vernier clock adjustment circuit receiving the input clock signal and providing a rising-edge clock signal representing the input clock signal delayed by a rising-edge delay and providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay. Each memory module also includes at least one edge triggered circuit receiving read or write data and the rising-edge and falling-edge clock signals, and storing read or write data at the rising-edge of the rising-edge clock signal and at the falling-edge of the falling-edge clock signal. Such vernier adjustment circuitry can also be employed for clocking commands into the memory modules. The memory modules can include one or more memory integrated circuits, such as dynamic random access memories (DRAMs).

The vernier clock adjustment circuitry and method according to the present invention more accurately and precisely compensates for the effects of duty cycle variation, bus position of a given memory device, timing drift, loading variations, clock jitter, clock skew, noise, overshoot, and ringing by individually adjusting both the rising-edge and falling-edge timings, either independently or interdependently from each other. As a result, data is accurately clocked in the memory devices even at higher data transmission rates.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of one embodiment of a memory system.

FIG. **2** is a timing diagram illustrating the bus timing of the memory system of FIG. **1**.

FIG. **3** is a block diagram of another embodiment of a memory system.

FIG. **4** is a timing diagram illustrating the bus timing of the memory system of FIG. **3**.

FIG. **5** is a block diagram of another embodiment of a memory system.

FIG. **6** is a timing diagram illustrating the bus timing of the memory system of FIG. **5**.

FIG. **7** is a block diagram of a memory system having vernier clock adjustment circuitry.

FIG. **8**A is a timing diagram illustrating an ideal signal waveform.

FIG. **8**B is a timing diagram illustrating a non-ideal signal waveform.

FIG. **9** is a block diagram of an independent rising and falling edge vernier clock adjustment system.

FIG. **10** is a block diagram of an interdependent cascaded rising and falling edge vernier clock adjustment system.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present invention. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

The following described embodiments of the present invention are described as applied to a dynamic random access memory (DRAM) and memory systems including DRAMs. The present invention can, however, be implemented in any integrated circuit and other memory systems including other types of memory integrated circuits. The DRAM according to the present invention is similar in many respects to conventional DRAMs, such as those commercially available from Micron Technology, Inc. of Boise, Id. For clarity, only a portion of the well-known circuitry of the DRAM is described herein, while the new circuitry of the DRAM of the present invention is described in detail herein.

Overview of Memory Systems

A memory system is illustrated generally at **20** in FIG. **1**. Memory system **20** includes a memory controller **22** and N DRAM modules such as indicated at **24** and **26**. The DRAM modules, such as modules **24** and **26**, each comprise at least one DRAM device. A command bus **28** is an unidirectional bus for carrying address and control information from memory controller **22** to the DRAM modules. Address and control information is typically transferred from memory controller **22** on command bus **28** in uniform packets. For example, if a packet is four times the width of command bus **28**, a command packet is transferred in four cycles on each edge of a free-running clock (CCLK) provided on a clock line **30** from memory controller **22**. A data bus **32** is a bidirectional bus carrying write data from memory controller **22** to the DRAM modules and further carrying read data from the DRAM modules to memory controller **22**. Two bidirectional data clocks, DCLK**0** and DCLK**1**, are respectively provided on clock line **34** and clock line **36**.

Data clocks DCLK**0** and DCLK**1** are used to precisely transfer read data timing from the DRAM modules to the memory controller **22** and to further precisely transfer write data timing from memory controller **22** to the DRAM modules. Both rising edge and falling edge transitions of the selected DCLK are employed to clock the input latches of the DRAM modules and memory controller receiving data. The data clocks DCLK**0** and DCLK**1** follow the same path as data provided on data bus **32** to reduce the effects of clock jitter, duty cycle variation, bus position, drift timing, and loading variations.

When control of data bus **32** is transferred from one device in memory system **20** to another device in memory system **20**, such as from memory controller **22** to DRAM module **24**, from DRAM module **24** to memory controller **22**, or from DRAM module **24** to DRAM module **26**, one DCLK is deactivated and the other DCLK is activated. Memory controller **22** determines which DCLK is to be used for a given read or write operation and provides the information indicating which DCLK to use in the command packet provided on command bus **28**.

Memory system **20** accommodates for minimum and maximum delays from command at memory controller **22** to read data at memory controller **22** from the different DRAM modules by programming vernier clock adjustment circuits in each DRAM module. Preferably, the vernier adjustments in each DRAM module provide coarse steps defined in bit periods and fine steps to cover adjustments within a single bit period.

FIG. **2** is a timing diagram illustrating bus timing for memory system **20**. As illustrated in FIG. **2**, CCLK has a falling or rising edge transition every T nanoseconds (Nsec). For example, T is 2.5 Nsec in one embodiment of memory system **20**. FIG. **2** illustrates a sequence of four T read and write first operations. The bus propagation delay from command bus **28** at memory controller **22** to command bus **28** at a DRAM module is shown to be a maximum of one clock transition of the CCLK (1 T).

As illustrated in FIG. **2**, the DRAM module performs an internal Read0 operation at time 17 T. The DRAM module vernier clock adjustment is programmed to provide read data beginning at time 29 T, so that read data arrives at memory controller **22** at time 30 T. With the programmed vernier clock adjustment in each DRAM module, the loop-around delay from command to data burst at memory controller **22**, for both read and write operations is maintained at 30 T. The DRAM module provides a read data clock to memory controller **22** with the DCLK0 on clock line **34**.

A 2 T time gap is inserted between the read0 command burst operation and a write**1** command burst operation to permit control of data bus **32** to be transferred from memory controller **22** to the DRAM module. Thus, write data is provided at time 36 T at memory controller **22** which correspondingly arrives at the DRAM module at time 37 T. An internal write operation is performed immediately on the received write data at the DRAM module at time 41 T. Memory controller **22** provides a write data clock to the DRAM module with the DCLK1 on clock line **36**.

A sequence of gapless read burst commands (i.e., read2, read3, and read4) follow the write**1** command. The read2–4 burst commands are transmitted to a single DRAM module. Thus, timing gaps are not required in the sequence of read burst commands because the same device is driving data bus **32** during all of these read operations. A 6 T gap is inserted between the write1 command and the first read command of the sequence of read commands (i.e., read2 command) to permit bus settling.

Memory system **20** may include only one DRAM device per DRAM module. A memory system which includes several DRAM devices per DRAM module is illustrated generally at **120** in FIG. **3**. Memory system **120** includes a memory controller **122** and N DRAM modules, such as indicated at **124** and **126**. The DRAM modules, such as modules **124** and **126**, each comprise M DRAM devices. A command bus **128** is a unidirectional bus for carrying address and control information from memory controller **122** to the DRAM modules. Address and control information is typically transferred from memory controller **122** on

command bus **128** in uniform packets on both rising and falling edges of a free-running clock (CCLK) provided on a clock line **130** from memory controller **122**. Data busses **132***a–m* are bidirectional busses carrying write data from memory controller **122** to the DRAM modules and further carrying read data from the DRAM modules to memory controller **122**. Two bidirectional data clocks, DCLK**0** and DCLK1, are respectively provided on clock lines **34***a–m* and clock lines **36***a–m*.

DRAM module **124** includes a command buffer **140** for buffering commands from command bus **128** to be provided to M DRAM devices such as indicated at **142***a* and **142***m*. Similarly, the Nth DRAM module indicated at **126** includes a command buffer **144** which buffers commands from command bus **128** to M DRAM devices such as indicated at **146***a* and **146***m*.

As illustrated in FIG. **3**, memory system **120** does not include data buffers in the DRAM modules. Therefore memory system **20** includes M parallel data buses such as indicated at **132***a* and **132***m*. Corresponding data clocks are provided on 2M clock lines such as indicated at **134***a* and **134***m* for carrying DCLK0 and at **136***a* and **136***m* for carrying DCLK1. Memory system **120** is useful for memory applications requiring wider data buses for higher bandwidth, and yet not requiring command bus **128** to be duplicated for each data bus.

FIG. **4** is a timing diagram illustrating bus timing for memory system **120**. Again, as in FIG. **2**, a sequence of four T read and write burst operations are illustrated in FIG. **3**.

The command buffers such as indicated at **140** and **144** add an additional 2 T delay to get the command to the DRAM devices in the DRAM modules. Thus, the internal read operation starts at 19 T. Nevertheless, the vernier clock adjustment in the DRAM module is adjusted so that output read0 data is provided at 29 T to the corresponding data bus and the output data read**0** correspondingly arrives at memory controller **122** at time 30 T.

As to the write operation, write data is provided at time 36 T, and arrives at the DRAM module at time 37 T to permit the internal write operation to be performed at 41 T similar to the write timing of memory system **20**.

Another memory system which includes several DRAM devices per DRAM module is illustrated generally at **220** in FIG. **5**. Memory system **220** includes a memory controller **222** and N DRAM modules, such as indicated at **224** and **226**. The DRAM modules, such as modules **224** and **226**, each comprise M DRAM devices. A command bus **228** is a unidirectional bus for carrying address and control information from memory controller **222** to the DRAM modules. Address and control information is typically transferred from memory controller **222** on command bus **228** in uniform packets on both rising and falling edges of a free-running clock (CCLK) provided on a clock line **230** from memory controller **222**. A data bus **232** is a bidirectional bus carrying write data from memory controller **222** to the DRAM modules and further carrying read data from the DRAM modules to memory controller **222**. Two bidirectional data clocks, DCLK0 and DCLK1, are respectively provided on clock line **234** and clock line **236**.

The first DRAM module **224** includes a command buffer **240** which buffers commands to M DRAM devices, such as indicated at **242***a* and **242***m*. In addition, DRAM module **224** includes a data buffer **250** for buffering read and write data to be provided from and to the N DRAM devices **242***a–m*. Similarly, the Nth DRAM module **226** includes a command buffer **224** for buffering commands to M DRAM devices, such as indicated at **246***a* and **246***m*. In addition, DRAM module **226** includes a data buffer **252** for buffering read and write data from and to the M DRAM devices **246***a–m*. In the configuration of memory system **220** having the data buffers, only one data bus **232** and one set of DCLK clock lines are required. Thus, data buffers, such as data buffer **250** and data buffer **252**, send and receive data from data bus **232** and send and receive the DCLK0 clock signal from clock line **234** and the DCLK1 clock signal from clock line **236**.

The configuration of memory system **220** is useful where a very large memory configuration is required. For example, in one embodiment of memory system **220** where N=4 and M=8, up to eight DRAM devices are included in a single DRAM module and four DRAM modules are included in memory system **220** for a total of 32 DRAM devices in the memory system.

Because of the timing flexibility provided by the vernier clock adjustment circuitry in the individual DRAM devices, other embodiments of memory systems according to the present invention, such as memory system **20**, **120**, and **220**, can accommodate both buffered and unbuffered modules. For example, a memory system according to the present invention may actually include: one or more DRAM modules which include no command buffers and no data buffers; one or more DRAM modules which include command buffers but no data buffers; and one or more DRAM modules which include both command buffers and data buffers. Whether a particular DRAM module includes buffers or partial buffers is completely transparent to the memory controller of the memory system according to the present invention.

FIG. **6** illustrates, in timing diagram form, the bus timing for memory system **220**. As illustrated in FIG. **6**, the data buffers, such as data buffers **250** and **252**, add an additional 2 T delay to read data. Thus, the internal read operation still begins at time 19 T, just as in memory system **120**. However, the vernier clock adjustment circuitry in the DRAMA module is adjusted to provide output data to data bus **232** at the DRAM module at time 27 T to assure arrival of the output data to memory controller **222** at time 30 T (i.e., 27 T plus 2 T delay from the data buffer plus the 1 T propagation delay on data bus **232**). Thus, the read**0** data arrives at the memory controller at 30 T whether or not command buffers and whether or not data buffers are used in the memory system.

In memory system **220**, the write**1** operation provides write1 data at time 36 T at memory controller **222**, similar to the write1 operations illustrated in FIGS. **2** and **4** for memory systems **20** and **120**. However, because of the 2 T delay from the data buffers, the write1 data arrives at the DRAM module at time 39 T instead of 37 T. Correspondingly, the internal write1 operation is performed beginning at time 43 T in memory system **220** instead of at time 41 T.

Vernier Clock Adjustment Circuitry

The vernier clock adjustment circuitry and other related circuitry of memory system **20** (or memory systems **120** and **220**) is illustrated in block diagram form in FIG. **7**. As illustrated in FIG. **7**, memory controller **22** includes a command register **50** for providing commands to command bus **28** and a CCLK register **52** for providing the CCLK to clock line **30**. A master clock is provided on a line **54** to registers **50** and **52**. A write data register **56** is also clocked by the master clock on line **54** and provides write data to data bus **32**. A read data register **58** receives read data from data bus **32** and receives its clock from an optional vernier clock adjustment circuit **60**. Vernier clock adjustment circuit **60** receives the master clock from line **54** and the active one of the data clocks DCLK0 or DCLK1 via a register multiplexer **62**, which receives DCLK0 and DCLK1 from clock lines **34** and **36**.

DRAM module **24** includes a command latch **64** which receives commands from command bus **28**. Command latch **64** receives a delayed CCLK clock from a command vernier clock adjustment circuit **66**. Command vernier clock adjustment circuit **66** receives the CCLK clock signal from clock line **36**. A write first-in, first-out (FIFO) buffer **68** receives the DCLK0 and DCLK1 clock signals from lines **34** and **36** and the write data from data bus **32** and provides write data to a DRAM core **76**. Write FIFO buffer **68** receives a delayed CCLK clock from a write vernier clock adjustment circuit **70**. Write vernier clock adjustment circuit **70** also receives the CCLK clock signal from clock line **36**. A read FIFO buffer **72** receives read data from DRAM core **76** and provides the read data to data bus **32** along with the DCLK0 and DCLK1 clock signals to clock lines **34** and **36**. Read FIFO buffer **72** receives a delayed CCLK clock from a read vernier clock adjustment circuit **74**. Read vernier clock adjustment circuit **74** also receives the CCLK clock signal from clock line **30**.

Bus Initialization

When memory systems **20/120/220** are powered up, the command timing, read timing, and write timing of each individual DRAM is adjusted by the memory controller **22/122/222** so that bursts of data on the data bus originating from different devices are properly spaced. DRAM devices from different suppliers, manufactured at different points in a process spread, operating at different temperatures and supply voltages, and occupying different positions along the command bus and data bus, and operating with and without command buffers and/or data buffers necessarily comprise a range of loop-around delays from the read command provided on command bus **28** at memory controller **22** to input read data to memory controller **22** at the memory controller on data bus **32**. Similar variations occur in write data having a range of loop-around delays from the write command at memory controller **22** to write data to the selected DRAM device from data bus **32**.

As illustrated in FIG. **7**, each DRAM includes a variety of vernier adjustment circuits which compensate for all of these variables to permit read data from all DRAMs to arrive at memory controller **22** within fixed, deterministic timing, and similarly permit write data to arrive with fixed, deterministic timing to the selected DRAM devices.

In one embodiment of memory system **20/120/220**, the adjustments to vernier clock adjustment circuit **66**, **70**, **74** in each DRAM device is made by writing a delay value in a register located in each DRAM device. For example, the delay typically includes a coarse adjustment setting providing a number of bit periods of delay adjustment, and a fine adjustment including a fine step to cover adjustment within a single bit.

Vernier adjustment circuits **66**, **70**, **74**, and **60** are typically implemented with tapped delay lines. In one preferred embodiment of the invention, inverters are staged and various tapped points along the tapped delay lines provide the required variations in vernier adjustment delays. The vernier delays are optionally provided with phase-lock loop (PLL) or delayed-lock loop (DLL) circuitry where various phases are selected from different places to provide the required variations in vernier adjustment delays. The vernier clock adjustment circuits can be implemented in any suitable programmable delay elements.

During initialization, there are a variety of ways to adjust the vernier clock adjustment circuits. For example, one embodiment of memory system **20** runs through all delay steps of the vernier circuit and determines when data misses on low adjustments and on high adjustments and sets the vernier adjustment in an approximated optimal middle setting. Another embodiment of memory system **20** includes a feedback controller used to set the vernier settings by first selecting an estimated optimal setting and allowing the controller and feedback circuitry to arrive at the optimal delay setting for the vernier clock adjustment circuit.

The following is an example of vernier timing adjustments during initialization in one embodiment of memory system **20** without optional vernier clock adjustment circuit **60** in memory controller **22**. In this embodiment, memory controller **22** sends commands to the first DRAM module **24** and the command clock adjustment circuit **66** in DRAM module **24** is adjusted to optimally receive the command at command latch **64** from the command bus **28**. Then memory controller **22** starts a write command sequence and the write vernier adjustment circuit **70** in DRAM module **24** is adjusted to permit optimal receiving of the write data at write FIFO buffer **68** from data bus **32**. Next, a read command sequence is started by memory controller **22** and the read vernier clock adjustment circuit **74** is adjusted to permit optimal receiving of read data at read data register **58** from data bus **32**.

The command, write, and read vernier clock adjustment circuits are correspondingly adjusted with the above sequence of steps for each of the DRAM modules through the Nth DRAM module **26**. Upon completion of these sequences, alignments of clocks, commands, write data bursts, and read data bursts from all sources are optimally adjusted.

The following is an alternative example of a read timing adjustment for an alternate embodiment of memory system **20** which includes vernier adjustment circuit **60** in memory controller **22**. In this embodiment, at initialization, the read vernier delay is set to a minimum value in each of the DRAM devices. Then, memory controller circuit **22** sends out write data on data bus **32** and attempts to receive the write data at read data register **58**. In this embodiment, memory controller **22** adjusts memory controller vernier clock adjustment circuit **60** to the optimal sampling instant. This adjustment establishes a read data timing reference point for ensuring timing alignment between write data bursts and read data bursts on data bus **32**.

Memory controller **22** then sends read data instructions to the first DRAM module **24** and observes the corresponding DCLK pattern returning on the data clock line **34** or **36**. Memory controller **22** then writes the vernier delay control register of read vernier clock adjustment circuit **74** or otherwise sets the delay of the read vernier clock adjustment circuit to increase the delay until read delay data can be optimally sampled by the same internal memory controller clock timing that was used to read and write data in the previous step.

Memory controller **22** correspondingly adjusts the read vernier clock adjustment circuits of each of the DRAM modules through the Nth DRAM module **26**. Upon completion of this sequence, read data burst alignments from all sources are optimally adjusted.

With a similar initiation sequence performed for write operations and read operations, a constant delay from a command packet being provided on command bus **28** at memory controller **22** to read data or write data bursts at memory controller data bus I/O pins is established. In normal operation, one of DCLK0 or DCLK1 clocks is selected in vernier clock adjustment circuit **60** to latch the read data in read data register **58** instead of the master clock from line **54**. Vernier circuit **60** of memory controller **22** can, however, be used periodically to monitor the timing of data

from all sources and update DRAM vernier control registers as necessary to compensate for system timing drift.

At each DRAM device input, edges of CCLK clock and the DCLK clocks are coincident with data transitions on the command bus **28** and the data bus **32**, respectively. To compensate for this, the CCLK clock and the DCLK clocks are typically delayed by one-half of a bit period with the vernier clock adjustment circuits to optimally sample incoming data. As mentioned above, and in reference to FIG. **7**, the free-running CCLK is used to drive all internal DRAM timing. A delayed version of the CCLK is used to latch the command packets with vernier clock adjustment circuit **66**. Similarly, vernier adjustment circuits **70** and **74** provide delayed versions of the free-running CCLK clock to respectively clock the write FIFO buffer **68** and the read FIFO buffer **72**.

Individual Vernier Adjustment of the Rising and Falling Edge Clocks

Various problems occur in a memory system, such as memory systems **20**, **120**, and **220**, when faster clock rates are used for the CCLK clock signal. For example, such memory systems include 400 Mbps per pin which requires a 200 MHz CCLK clock. In fact, such systems can include even faster data rates per pin, such as systems with 600 Mbps, 800 Mbps, 1 Gbps, and 1.2 Gbps per pin. With these faster data transitions, effects of jitter, skew, noise, overshoot and ringing result in smaller and smaller portions of a whole clock period where valid data can be clocked into a DRAM device.

The following example timing budget for a 400 Mbps per pin memory system illustrates this problem. In the 400 Mbps per pin memory system, the CCLK is 200 MHz or 2.5 N between each edge of the clock which is allocated as follows:

1) 250 ps for timing skew due to VREF drift and noise;
2) 500 ps for setup and hold window;
3) 400 ps for across-the-bus driver skew;
4) 200 ps for across-the-bus load variations;
5) 100 ps for across-the-bus path matching (PCB traces);
6) 500 ps for pulse width dependent skew (data dependency);
7) 200 ps for clock and data jitter (noise induced); and
8) 350 ps for total data read variation from module to module after trimming. Data error primarily due to worst case trim resolution. Timing errors trimmed out include bus path length differences of modules on the bus and differing DRAM access times from the clock.

This problem is further illustrated by FIGS. **8**A and **8**B in timing diagram form. In FIG. **8**A, an ideal signal waveform is indicated at **80** having data valid between the times indicated between arrows **82**. As illustrated in FIG. **8**A, ideal signal waveform **80** forms a big eye pattern. By contrast, in FIG. **8**B a non-ideal waveform is indicated at **84**, which has a significantly reduced valid data period indicated by arrows **86**. The non-ideal waveform **84** is produced as a result of jitter, skew, noise, overshoot, ringing and other such known problems.

In order to compensate for such problems and to properly latch incoming data into each DRAM, a second tier of vernier adjustment is added according to the present invention to the vernier adjustment circuitry in each DRAM module to individually adjust both a clock's falling-edge timing independent of or interdependent on the clock's rising edge.

One embodiment of such a vernier clock adjustment system is illustrated generally at **300** in FIG. **9**. Vernier clock adjustment system **300** includes a rising-edge vernier adjustment circuit **302** and a falling-edge vernier adjustment circuit **304**. A clock signal (CLK) is provided to the vernier adjustment circuits **302** and **304** on a clock line **306**. Vernier clock adjustment circuit **302** independently delays the CLK signal from clock line **306** to provide a delayed version of the CLK signal on a clock line **308**. The delayed clock on clock line **308** is used for rising-edge clockings. Falling-edge vernier clock adjustment circuit **304** independently delays the CLK signal from clock line **306** to provide a delayed version of the CLK signal on a clock line **310**. The delayed clock signal on line **310** is used for falling-edge clockings. Thus, vernier clock adjustment system **300** includes two completely separate vernier circuits, one for independently delaying each clock edge.

Another embodiment of a vernier clock adjustment system according to the present invention is illustrated generally at **400** in FIG. **10**. Vernier clock adjustment system **400** includes cascaded vernier clock adjustment circuits **402** and **404**. A CLK signal is provided on a line **406** to vernier clock circuit **402**. Vernier clock circuit **402** provides a delayed version of the CLK signal on a clock line **408**. The delayed clock on line **408** is used for rising-edge clockings. Vernier clock adjustment circuit **402** also provides the same delayed version of the CLK signal to the second vernier clock adjustment circuit **404** via a line **409**. Vernier clock adjustment circuit **404** further delays the clock signal to provide a delayed clock signal on a clock line **410**. The delayed clock signal on line **410** is in used for falling-edge clockings. In the cascaded vernier adjustment system **400**, the falling-edge timing is based upon the rising-edge timing. An alternative embodiment (not shown) of the vernier clock adjustment system **400** is configured to make the rising edge timing be based on the falling edge timing.

Vernier clock adjustment systems **300** and **400** are preferably employed in command vernier clock adjustment circuit **66**, write vernier clock adjustment circuit **70**, and read vernier clock adjustment circuit **74** of DRAM module **24** and the other DRAM modules of memory systems **20**/**120**/**220**, such as illustrated in FIG. **7**. Optionally, vernier adjustment circuit **60** of the memory controller **22** also includes such individual edge adjustment as provided by either vernier clock system **300** or **400**.

In one embodiment of the memory system **20**/**120**/**220**, during system initialization, rising-edge clock data is first adjusted, followed by falling-edge clock data. The rising-edge clock data is adjusted by adjusting the delay provided by the rising-edge vernier adjustment circuit **302** of system **300** or circuit **402** of system **400**. The falling-edge clock data is then adjusted by adjusting the delay of falling-edge vernier adjustment circuit **304** of system **300** or circuit **404** of system **400**. Alternate embodiments of memory system **20**/**120**/**220**, first adjust the falling-edge time followed by the rising edge timing during system initialization.

The falling-edge and rising-edge adjustments provided by vernier clock adjustment systems **300** and **400** are especially beneficial to lessen memory system demands upon clock duty cycle. Specifically, the echo clock scheme employed for producing DCLK0 and DCLK1 in the memory systems **20**, **120**, and **220** is especially vulnerable to duty cycle problems since each DRAM device must receive a clock and retransmit the clock with the read data. Each time the clock is converted to and from the data bus, the duty cycle is affected. The memory system according to the present invention compensates for these duty cycle problems by employing the clock verniers to individually adjust both the rising and falling edges of the clock.

Moreover, a memory system, such as memory system **20**, **120**, or **220**, typically operates on an industry standard

protocol where the DRAM devices, whether or not manufactured from different suppliers, look the same to the memory controller. In addition, from the point of view of the memory controller, the DRAM devices may be at different points in the process spread, such as at 400 Mbps as compared to 800 Mbps. In addition, DRAM devices may be operating at different temperatures and supply voltages and be occupying different positions along the command bus and data bus, and at the same time the DRAM devices can be with and without command buffers and data buffers. The more precise adjustment of adjusting both falling and rising edge of the clocks better compensates for these problems.

Conclusion

By employing the vernier clock adjustment circuitry and method according to the present invention in memory systems, such as memory systems **20**/**120**/**220**, the effects of duty cycle variation, bus position of a given memory device, timing drift, loading variations, clock jitter, clock skew, noise, overshoot, and ringing are more accurately and precisely compensated for by individually adjusting both the rising-edge and falling-edge timings, either independently or interdependently from each other. In this way, data can be accurately clocked in the memory devices even at higher data transmission rates.

Although specific embodiments have been illustrated and described herein for purposes of description of the preferred embodiment, it will be appreciated by those of ordinary skill in the art that a wide variety of alternate and/or equivalent implementations calculated to achieve the same purposes may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. Those with skill in the mechanical, electromechanical, electrical, and computer arts will readily appreciate that the present invention may be implemented in a very wide variety of embodiments. This application is intended to cover any adaptations or variations of the preferred embodiments discussed herein. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. An integrated circuit, comprising:

a vernier clock adjustment circuit receiving an input clock signal, the vernier clock adjustment circuit including a rising-edge delay circuit receiving the input clock signal and providing a rising-edge clock signal representing the input clock signal delayed by a rising-edge delay, the vernier clock adjustment circuit further including a falling-edge delay circuit receiving the rising-edge clock signal and providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay; and

an edge triggered circuit receiving a binary signal, the rising-edge clock signal and the falling-edge clock signal, the edge triggered circuit performing a first operation on the binary signal at a first edge of the rising-edge clock signal and performing a second operation at a second edge of the falling-edge clock signal.

2. The integrated circuit of claim **1** wherein the first edge of the rising-edge clock signal comprises the rising-edge of the rising-edge clock signal.

3. The integrated circuit of claim **1** wherein the second edge of the falling-edge clock signal comprises the falling-edge of the falling-edge clock signal.

4. The integrated circuit of claim **1** wherein the first operation performed by the edge triggered circuit comprises storing the binary signal at the first edge of the of the rising-edge clock signal.

5. The integrated circuit of claim **1** wherein the second operation performed by the edge triggered circuit comprises storing the binary signal at the second edge of the of the falling-edge clock signal.

6. The integrated circuit of claim **1** wherein the edge triggered circuit comprises a First-In, First-Out buffer that transfers samples of the binary signal on each first edge of the rising-edge clock signal and each second edge of the falling-edge clock signal.

7. The integrated circuit of claim **1** wherein the edge triggered circuit comprises a latch that stores a respective samples of the binary signal on each first edge of the rising-edge clock signal and each second edge of the falling-edge clock signal.

8. An integrated circuit, comprising:

a vernier clock adjustment circuit receiving an input clock signal, the vernier clock adjustment circuit including a falling-edge delay circuit receiving the input clock signal and providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay, the vernier clock adjustment circuit further including a rising-edge delay circuit receiving the falling-edge clock signal and providing a rising-edge clock signal representing the input clock signal delayed by a rising-edge delay; and

an edge triggered circuit receiving a binary signal, the falling-edge clock signal and the rising-edge clock signal, the edge triggered circuit performing a first operation on the binary signal at a first edge of the falling-edge clock signal and performing a second operation at a second edge of the rising-edge clock signal.

9. The integrated circuit of claim **8** wherein the first edge of the falling-edge clock signal comprises the falling-edge of the falling-edge clock signal.

10. The integrated circuit of claim **8** wherein the second edge of the rising-edge clock signal comprises the rising-edge of the rising-edge clock signal.

11. The integrated circuit of claim **8** wherein the first operation performed by the edge triggered circuit comprises storing the binary signal at the first edge of the of the falling-edge clock signal.

12. The integrated circuit of claim **8** wherein the second operation performed by the edge triggered circuit comprises storing the binary signal at the second edge of the of the rising-edge clock signal.

13. The integrated circuit of claim **8** wherein the edge triggered circuit comprises a First-In, First-Out buffer that transfers samples of the binary signal on each first edge of the falling-edge clock signal and each second edge of the rising-edge clock signal.

14. The integrated circuit of claim **8** wherein the edge triggered circuit comprises a latch that stores a respective samples of the binary signal on each first edge of the falling-edge clock signal and each second edge of the rising-edge clock signal.

15. A signal coupling system, comprising:

a memory controller generating a clock signal on a clock terminal and a plurality of bits of a digital signal on a signal bus;

a vernier clock adjustment circuit having a clock input coupled to the clock terminal of the memory controller to receive the clock signal from the memory controller, the vernier clock adjustment circuit providing a rising-edge clock signal representing the input clock signal

delayed by a rising-edge delay and providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay, the vernier clock adjustment circuit further having a delay adjustment input adapted to receive delay control signals controlling the magnitude of the rising-edge delay and the falling-edge delay; and

a plurality of latches, each latch having an input terminal coupled to a respective bit of the signal bus and first and second clock terminals coupled to the vernier clock adjustment circuit to receive the rising-edge clock signal and the falling-edge clock signal, the latches being constructed to store respective bits of the digital signal from the memory controller on the rising-edge of the rising-edge clock signal and on the falling-edge of the falling-edge clock signal.

16. The signal coupling system of claim **15**, wherein the vernier clock adjustment circuit comprises:

a rising-edge delay circuit receiving the input clock signal and providing a rising-edge clock signal representing the input clock signal delayed by a rising-edge delay; and

a falling-edge delay circuit receiving the rising-edge clock signal and providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay.

17. The signal coupling system of claim **15**, wherein the vernier clock adjustment circuit comprises:

a falling-edge delay circuit receiving the input clock signal and providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay; and

a rising-edge delay circuit receiving the falling-edge clock signal and providing a rising-edge clock signal representing the input clock signal delayed by a rising-edge delay.

18. The signal coupling system of claim **15**, wherein the vernier clock adjustment circuit comprises:

a rising-edge delay circuit receiving the input clock signal and independently providing a rising-edge clock signal representing the input clock signal delayed by a rising-edge delay; and

a falling-edge delay circuit receiving the input clock signal and independently providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay.

19. A signal coupling system, comprising:

a memory controller generating a clock signal on a clock terminal and receiving or supplying a plurality of bits of a digital signal on a signal bus;

a vernier clock adjustment circuit having a clock input coupled to the clock terminal of the memory controller to receive the clock signal from the memory controller, the vernier clock adjustment circuit providing a rising-edge clock signal representing the input clock signal delayed by a rising-edge delay and providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay, the vernier clock adjustment circuit further having a delay adjustment input adapted to receive delay control signals controlling the magnitude of the rising-edge delay and the falling-edge delay; and

a plurality of First-In, First-Out ("FIFO") buffers, each having an input terminal coupled to a respective bit of the signal bus and first and second clock terminals coupled to the vernier clock adjustment circuit to receive the rising-edge clock signal and the falling-edge clock signal, the FIFO buffers being constructed to receive respective bits of the digital signal from the memory controller or supply respective bits of the digital signal to the memory controller on the rising-edge of the rising-edge clock signal and on the falling-edge of the falling-edge clock signal.

20. The signal coupling system of claim **19**, wherein the vernier clock adjustment circuit comprises:

a rising-edge delay circuit receiving the input clock signal and providing a rising-edge clock signal representing the input clock signal delayed by a rising-edge delay; and

a falling-edge delay circuit receiving the rising-edge clock signal and providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay.

21. The signal coupling system of claim **19**, wherein the vernier clock adjustment circuit comprises:

a falling-edge delay circuit receiving the input clock signal and providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay; and

a rising-edge delay circuit receiving the falling-edge clock signal and providing a rising-edge clock signal representing the input clock signal delayed by a rising-edge delay.

22. The signal coupling system of claim **19**, wherein the vernier clock adjustment circuit comprises:

a rising-edge delay circuit receiving the input clock signal and independently providing a rising-edge clock signal representing the input clock signal delayed by a rising-edge delay; and

a falling-edge delay circuit receiving the input clock signal and independently providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay.

23. A memory device comprising:

a data bus coupling data to and from the memory device;

a plurality of arrays of memory cells for storing data, the arrays of memory cells including a data path coupling data to and from the data bus;

a command bus receiving commands to generate control signals corresponding thereto;

a clock line receiving an input clock signal; and

a vernier clock adjustment circuit receiving the input clock signal, the vernier clock adjustment circuit including a rising-edge delay circuit receiving the input clock signal and providing a rising-edge clock signal representing the input clock signal delayed by a rising-edge delay, the vernier clock adjustment circuit further including a falling-edge delay circuit receiving the rising-edge clock signal and providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay; and

an edge triggered circuit receiving the rising-edge clock signal and the falling-edge clock signal, the edge triggered circuit performing a predetermined operation in the memory device at a first edge of the rising-edge clock signal and at a second edge of the falling-edge clock signal.

24. The memory device of claim **23** wherein the first edge of the rising-edge clock signal comprises the rising-edge of the rising-edge clock signal.

25. The memory device of claim 23 wherein the second edge of the falling-edge clock signal comprises the falling-edge of the falling-edge clock signal.

26. The memory device of claim 23 wherein the predetermined operation performed by the edge triggered circuit comprises storing data applied to the memory device at the first edge of the of the rising-edge clock signal and at the second edge of the of the falling-edge clock signal.

27. The memory device of claim 23 wherein the predetermined operation performed by the edge triggered circuit comprises outputting data from the memory device at the first edge of the of the rising-edge clock signal and at the second edge of the of the falling-edge clock signal.

28. The memory device of claim 23 wherein the predetermined operation performed by the edge triggered circuit comprises storing a command signal applied to the memory device at the first edge of the of the rising-edge clock signal and at the second edge of the of the falling-edge clock signal.

29. The memory device of claim 23 wherein the edge triggered circuit comprises a First-In, First-Out buffer that is operable to transfer a binary signal into and out of the buffer responsive to the first edge of the of the rising-edge clock signal and at the second edge of the of the falling-edge clock signal.

30. The memory device of claim 23 wherein the edge triggered circuit comprises a latch that is operable to store a binary signal responsive to the first edge of the of the rising-edge clock signal and at the second edge of the of the falling-edge clock signal.

31. A memory device comprising:

a data bus coupling data to and from the memory device;

a plurality of arrays of memory cells for storing data, the arrays of memory cells including a data path coupling data to and from the data bus;

a command bus receiving commands to generate control signals corresponding thereto;

a clock line receiving an input clock signal; and

a vernier clock adjustment circuit receiving the input clock signal, the vernier clock adjustment circuit including a falling-edge delay circuit receiving the input clock signal and providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay, the vernier clock adjustment circuit further including a rising-edge delay circuit receiving the falling-edge clock signal and providing a rising-edge clock signal representing the input clock signal delayed by a rising-edge delay; and

an edge triggered circuit receiving the rising-edge clock signal and the falling-edge clock signal, the edge triggered circuit performing a predetermined operation in the memory device at a first edge of the falling-edge clock signal and at a second edge of the rising-edge clock signal.

32. The memory device of claim 31 wherein the first edge of the failing-edge clock signal comprises the falling-edge of the falling-edge clock signal.

33. The memory device of claim 31 wherein the second edge of the rising-edge clock signal comprises the rising-edge of the rising-edge clock signal.

34. The memory device of claim 31 wherein the predetermined operation performed by the edge triggered circuit comprises storing data applied to the memory device at the first edge of the of the falling-edge clock signal and at the second edge of the of the rising-edge clock signal.

35. The memory device of claim 31 wherein the predetermined operation performed by the edge triggered circuit comprises outputting data from the memory device at the first edge of the of the falling-edge clock signal and at the second edge of the of the rising-edge clock signal.

36. The memory device of claim 31 wherein the predetermined operation performed by the edge triggered circuit comprises storing a command signal applied to the memory device at the first edge of the of the falling-edge clock signal and at the second edge of the of the rising-edge clock signal.

37. The memory device of claim 31 wherein the edge triggered circuit comprises a First-In, First-Out buffer that is operable to transfer a binary signal into and out of the buffer responsive to the first edge of the of the falling-edge clock signal and at the second edge of the of the rising-edge clock signal.

38. The memory device of claim 31 wherein the edge triggered circuit comprises a latch that is operable to store a binary signal responsive to the first edge of the of the falling-edge clock signal and at the second edge of the of the rising-edge clock signal.

39. A method of operating an integrated circuit, comprising:

receiving an input clock signal;

delaying the input clock signal by a rising-edge delay to provide a rising-edge clock signal;

delaying the rising-edge clock signal by a falling-edge delay to provide a falling-edge clock signal;

performing a first operation on the binary signal at a first edge of the rising-edge clock signal; and

performing a second operating at a second edge of the falling-edge clock signal.

40. The method of claim 39 wherein the first edge of the rising-edge clock signal comprises the rising-edge of the rising-edge clock signal.

41. The method of claim 39 wherein the second edge of the falling-edge clock signal comprises the falling-edge of the falling-edge clock signal.

42. The method of claim 39 wherein the first operation comprises storing the binary signal at the first edge of the of the rising-edge clock signal.

43. The method of claim 39 wherein the second operation comprises storing the binary signal at the second edge of the of the falling-edge clock signal.

44. A method of operating an integrated circuit, comprising:

receiving an input clock signal;

delaying the input clock signal by a falling-edge delay to provide a falling-edge clock signal;

delaying the falling-edge clock signal by a rising-edge delay to provide a rising-edge clock signal;

performing a first operation on the binary signal at a first edge of the falling-edge clock signal; and

performing a second operating at a second edge of the rising-edge clock signal.

45. The method of claim 44 wherein the first edge of the falling-edge clock signal comprises the falling-edge of the falling-edge clock signal.

46. The method of claim 44 wherein the second edge of the rising-edge clock signal comprises the rising-edge of the rising-edge clock signal.

47. The method of claim 44 wherein the first operation comprises storing the binary signal at the first edge of the of the falling-edge clock signal.

48. The method of claim 44 wherein the second operation comprises storing the binary signal at the second edge of the of the rising-edge clock signal.

49. A method of operating an integrated circuit, comprising:

receiving an input clock signal;

generating a first trigger signal subsequent to each rising-edge of the input clock signal, each first trigger signal being generated after a rising-edge delay has elapsed from each rising-edge of the input clock signal;

generating a second trigger signal subsequent to each falling-edge of the input clock signal, each second trigger signal being generated after a falling-edge delay has elapsed from each falling-edge of the input clock signal; and

performing a predetermined operation on the binary signal responsive to each of the first and second trigger signals.

50. The method of claim 49 wherein, the magnitude of the rising-edge delay is determined independently of the magnitude of the falling-edge delay.

51. The method of claim 49 wherein, the predetermined operation comprises storing a respective sample of the binary signal responsive to each of the first and second trigger signals.

52. The method of claim 49 further comprising adjusting the magnitudes of the rising-edge delay and the falling-edge delay.

53. A method of operating an integrated circuit, comprising:

receiving an input clock signal;

establishing a rising-edge delay value;

establishing a falling-edge delay value;

performing a first operation in the integrated circuit after a first delay has elapsed from each rising-edge of the input clock signal, the first delay corresponding to the rising-edge delay value; and

performing a second operation in the integrated circuit after a second delay has elapsed from each falling-edge of the input clock signal, the second delay corresponding to the falling-edge delay value.

54. The method of claim 53 wherein establishing the falling-edge delay value comprises establishing the falling-edge delay value independently of the magnitude of the rising-edge delay value.

55. The method of claim 53 wherein the first operation comprises storing a sample of a binary signal each time the first delay corresponding to the rising-edge delay value has elapsed from each rising-edge of the input clock signal.

56. The method of claim 53 wherein the first operation comprises storing a sample of a binary signal each time the second delay corresponding to the falling -edge delay value has elapsed from each falling-edge of the input clock signal.

57. The method of claim 53 further comprising adjusting the rising-edge delay value and the magnitude of the falling-edge delay value.

58. A method of operating an integrated circuit, comprising:

receiving an input clock signal;

establishing a falling-edge delay value;

establishing a rising-edge delay value;

performing a first operation in the integrated circuit after a first delay has elapsed from each falling-edge of the input clock signal, the first delay corresponding to the falling-edge delay value; and

performing a second operation in the integrated circuit after a second delay has elapsed from each rising-edge of the input clock signal, the second delay corresponding to the rising-edge delay value.

59. The method of claim 58 wherein the first operation comprises storing a sample of a binary signal each time the first delay corresponding to the rising-edge delay value has elapsed from each rising-edge of the input clock signal.

60. The method of claim 58 wherein the first operation comprises storing a sample of a binary signal each time the second delay corresponding to the falling -edge delay value has elapsed from each falling-edge of the input clock signal.

61. The method of claim 58 further comprising adjusting the magnitude of the rising-edge delay value and the magnitude of the falling-edge delay value.

62. The method of claim 58 wherein adjusting the magnitude of the rising-edge delay value and the magnitude of the falling-edge delay value comprising adjusting the magnitude of the rising-edge delay value independently of the magnitude of the falling-edge delay value.

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,016,282
DATE : January 18, 2000
INVENTORS : Keeth

It is hereby certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column	Reads	Should Read
Column 6, line 34	"DRAMA"	- -DRAM - -

Signed and Sealed this

Fifteenth Day of May, 2001

Attest:

NICHOLAS P. GODICI

Attesting Officer

Acting Director of the United States Patent and Trademark Office