

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES) INC.,
Petitioner,

v.

INTELLECTUAL VENTURES II LLC,
Patent Owner.

IPR2024-01226
Patent 7,646,835 B1

Before JAMESON LEE, THU A. DANG, and HYUN J. JUNG,
Administrative Patent Judges.

LEE, *Administrative Patent Judge.*

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Lenovo (United States) Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–23 (“challenged claims”) of U.S. Patent No. 7,646,835 B1 (Ex. 1001, “the ’835 patent”). Paper 2 (“Pet.”). Intellectual Ventures II LLC (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314 (2024); 37 C.F.R. § 42.4(a) (2024). An *inter partes* review may not be instituted unless the information presented in the Petition “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). The “reasonable likelihood” standard is “a higher standard than mere notice pleading” but “lower than the ‘preponderance’ standard to prevail in a final written decision.” *Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29 at 13 (PTAB Dec. 20, 2019) (precedential).

Upon consideration of the contentions and the evidence of record before us, we conclude Petitioner has not shown a reasonable likelihood that it would prevail in establishing unpatentability of any claim of the ’835 patent. Accordingly, we decline to institute *inter partes* review.

II. BACKGROUND

A. *Real Parties in Interest*

Petitioner identifies itself and Lenovo Group Ltd. as real parties in interest. Pet. 1. Patent Owner identifies itself as real party in interest. Paper 3, 2.

B. *Related Matters*

The parties each identify the following litigations as related matter:

Intellectual Ventures I LLC et al. v. OnePlus Technology (Shenzen) Co., Ltd., No. 6-23-cv-00290 (W.D. Tex.);

Intellectual Ventures I LLC et al. v. Zebra Technologies Corporation, No. 6-23-cv-00292 (W.D. Tex.);

Intellectual Ventures II LLC v. Lenovo Group Limited, No. 6-23-cv-00068 (W.D. Tex.).

Pet. 1–2; Paper 3, 2.

Patent Owner additionally identifies the following litigation as related matter:

Intellectual Ventures I LLC et al. v. Lenovo Group Limited, No. 6-23-cv-00307 (W.D. Tex.).

Paper 3, 2.

C. The '835 Patent

The '835 patent issued on January 12, 2010, from Application No. 10/716,320, filed November 17, 2003, which does not claim priority to any earlier filed application. Ex. 1001, codes (21), (22), (45).

The '835 patent relates to input and output signaling for digital integrated circuit devices. Ex. 1001, 1:9–10. The '835 patent explains that the design and fabrication of high-performance signaling mechanisms for digital integrated circuit devices has become a challenge because, for instance, modern memory integrated circuit designs require exacting control of critical timing specifications. *Id.* at 1:14–25. It explains that because of that requirement, design parameters must be strictly maintained to keep the entire system in balance. *Id.* at 1:22–25. Specifically, the '835 patent discloses a method for automatically calibrating intra-cycle timing

relationships between command signals, data signals, and sampling signals for an integrated circuit device. *Id.* at code (57).

Figure 1 of the '835 patent is reproduced below:

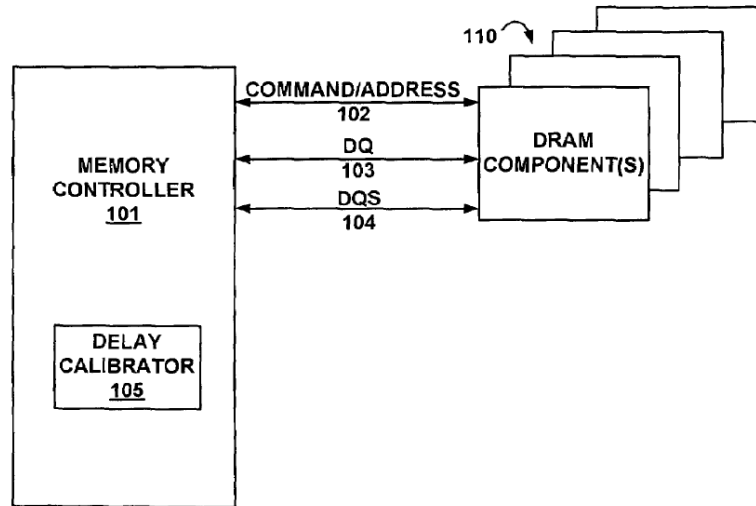


FIGURE 1

Figure 1 is a diagram of a memory system in accordance with an embodiment of the '835 patent. Ex. 1001, 1:46–47.

Memory system 100 (not labeled in Figure 1) includes memory controller 101 coupled to a plurality of DRAM components 110 via command/address bus 102, data bus (“DQ”) 103, and sampling signal bus (“DQS”) 104, and memory controller 101 includes delay calibrator 105.

Ex. 1001, 2:65–3:2. The '835 patent describes:

The system 100 embodiment implements a method for automatically calibrating intra-cycle timing relationships between command signals of the command/address bus 102, data signals of the DQ data bus 103, and sampling signals of the DQS bus 104. In the present embodiment, each of the DRAM components 110 comprise the integrated circuit device for which the calibration adjustments are performed. The actual adjustments are performed by the memory controller 101. The

particular amounts of phase delay, or phase calibration, is determined by the delay calibrator 105.

The intra-cycle timing relationships between the command/address signals, the DQ signals, and the DQS signals are calibrated to ensure the optimal operation of the DRAM components 110. Generally, the calibration process includes generating command signals and address signals for accessing the DRAM components (e.g., DRAM chips of a memory module). The calibration process also includes accessing data signals (e.g., DQ signals) that convey data for the DRAM components, in both a data read transaction (e.g., data driven from the DRAM components 110 to the memory controller 101) and a data write transaction (e.g., data driven from the memory controller 101 to the DRAM components 110). The calibration process also includes accessing sampling signals (e.g., DQS signals) for controlling the sampling of the data signals. A phase relationship between the command signals, the data signals, and the sampling signals is automatically adjusted to calibrate the operation of the DRAM components 110. In one embodiment, the adjusting is performed by the delay calibrator 105.

Ex. 1001, 3:3–31.

Figure 2 of the '835 patent is reproduced below:

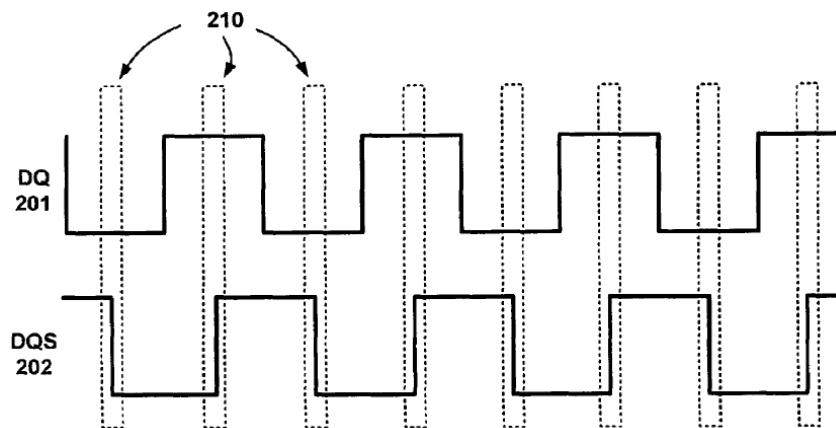


FIGURE 2

Figure 2 shows timing diagram 200 (not labeled) depicting a typical DQ (data bus) signal and a typical DQS (sampling signal bus) signal during a

write transaction and a plurality of sampling windows 210 in accordance with an embodiment of the '835 patent. Ex. 1001, 1:48–50, 4:29–33.

Sampling windows 210 are periods over which valid data can be read from DDR memory component. *Id.* at 4:35–36. The '835 patent describes:

Timing diagram 200 shows the DQ signal 201 and the DQS signal 202 during write transaction, as in a case where data is written from a memory controller to a DRAM array. Generally, with DDR DRAMs, the sampling windows 210 correspond to the rising and falling edges of the DQS signal 202. The rising and falling edges of DQS 202 need to be accurately placed at the center of the rise-and-hold times of DQ 201 as shown (e.g., phase shifted 90°). During the sampling windows 210, the logical value of the DQ signal is sampled and latched. As memory performance increases, the width of the sampling windows 210 correspondingly decreases (e.g., 2.5 nanoseconds for DDR 400 DRAM and 1.875 nanoseconds for DDR II 535 DRAM).

Id. at 4:40–52.

Figure 3 of the '835 patent is reproduced below:

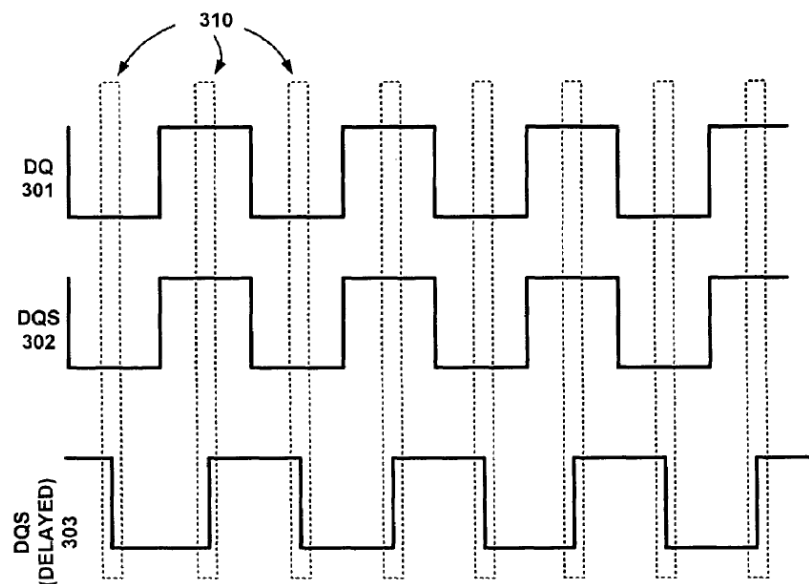


FIGURE 3

Figure 3 shows a timing diagram depicting a DQ signal and a DQS signal during a read transaction in accordance with one embodiment of the '835 patent. Ex. 1001, 1:51–53; 4:53–55.

The '835 patent describes:

During a read transaction, the rising and falling edges of DQS 302 needs to be accurately aligned with the rising and falling edges of the DQ signal 301 as shown. The memory controller then performs a 90° phase shift to place the sampling windows 310 at the center of the rise-and-hold times of DQ 301 (e.g., shown as DQS delayed 303). During read transactions, the memory controller is responsible for placing the sampling windows 310 at the correct locations.

Ex. 1001, 4:53–63.

Figure 5 of the '835 patent is reproduced below:

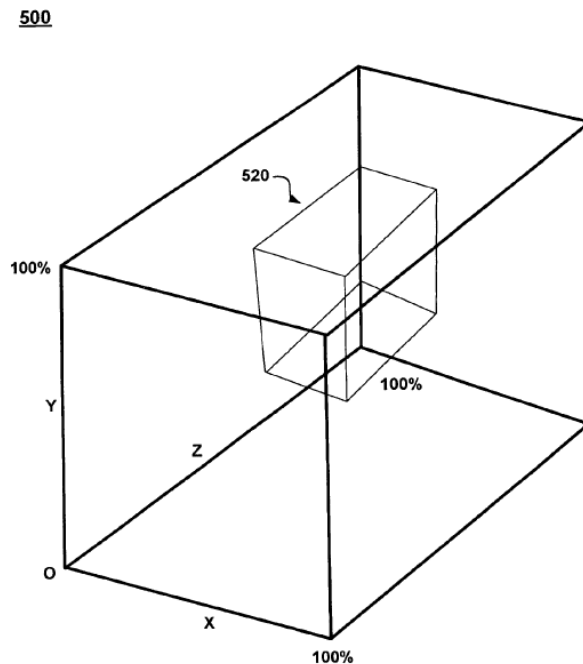


FIGURE 5

Figure 5 shows a diagram of a typical case where three parameters x, y, and z are varied across a range of adjustment to obtain valid windows for a DDR memory. Ex. 1001, 1:56–58; 5:25–27.

The '835 patent describes:

As depicted in FIG. 5, the three axes of the parameters [x, y, and z] are plotted orthogonal to one another. In the case of a DDR DRAM component, for example, the x parameter can correspond to a phase range of command/address signals, the y parameter can correspond to a phase range of DQ signals, and the z parameter can correspond to a phase range of DQS signals.

For a given device, there will be a valid region within which the values of the x, y, and z parameters result in the correct operation of the device. This is shown in FIG. 5 as the valid region 520.

Ex. 1001, 5:27–37.

The '835 patent further describes altering the x, y, and z parameters to find the boundaries of the valid region and then determining an optimal operating point for a device:

Embodiments of the present invention automatically alter the x, y, and z parameters (e.g., the intra-cycle command/address phase, DQ phase, and DQS phase) in order to determine the boundaries of the valid region 520. Once such boundaries are discovered, configuration choices can be intelligently made as to the optimal operating point for a given device.

Ex. 1001, 5:44–51.

The '835 patent also details a pseudo code example representation of the calibration process, which utilizes a function of the parameters x, y, and z:

A pseudo code example representation of the calibration process is now described. In the following pseudo code example, the terms x_limit, y_limit, and z_limit correspond to the maximum value of the parameter's range. [...]

For (x=x_limit, x>=0, x-=x_step)

For y=0, y<=y_limit, y+=y_step)

For (z=0, z<=z_limit, z+=z_step)

If test(x,y,z) passes, then abort loop and remember x,y,z.

Ex. 1001, 6:16–19, 35–38.

Claims 1, 7, 12, 20, and 23 are independent. Claims 1 and 7 are representative and are reproduced below:¹

1. [1.P] A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, the method comprising:

[1.1] generating command signals to access an integrated circuit component;

[1.2] accessing data signals to convey data for the integrated circuit component;

[1.3] accessing sampling signals to control sampling of the data signals; and

[1.4.a] systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device,

[1.4.b] wherein the valid operation range includes an optimal operation point for the integrated circuit device.

Ex. 1001, 6:56–7:4.

7. [7.P] A system for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, the system comprising:

[7.1] a controller configured to generate command signals for accessing an integrated circuit component;

[7.2.a] a delay calibrator integrated within the controller and

¹ The bracketed headings correspond to those used by Petitioner to reference the claim elements. *See* Pet. ix–x. We use the same headings here for ease of reference, understanding, and consistency.

[7.2.b] configured to access data signals conveying data for the integrated circuit device and

[7.2.c] to access sampling signals for controlling sampling of the data signals,

[7.3.a] wherein the delay calibrator is further configured to systematically alter a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device;

[7.3.b] and wherein the valid operation range includes an optimal operation point for the integrated circuit device.

Id. at 7:1–34.

D. The Applied Prior Art and Declarations

Petitioner relies on the following evidence:

Name	Patent Document/Publication	Exhibit
Keeth ²	US Pat. No. 6,115,318	1006
Johnson ³	US Pat. No. 6,434,081 B1	1004
Jeddeloh ⁴	US Pat. No. 6,629,222 B1	1005

Petitioner also relies on the Declaration of Jacob Baker, P.E., Ph.D.

Ex. 1002. Patent Owner relies on the Declaration of Terry R. Lee.

Ex. 2001.

E. The Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims of the '835 patent are unpatentable based on the following grounds (Pet. 17, 73, 85):

² Issued Sept. 5, 2000, based on Application No. 08/759,351, filed Dec. 3, 1996. Ex. 1006, codes (21), (22), (45).

³ Issued Aug. 13, 2002, based on Application No. 09/570,481, filed May 12, 2000. Ex. 1004, codes (21), (22), (45).

⁴ Issued Sept. 30, 2003, based on Application No. 09/352,719, filed on July 13, 1999. Ex. 1005, codes (21), (22), (45).

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1–23	103(a) ⁵	Johnson, Jeddeloh
1–3, 7, 8, 12	103(a)	Johnson, Keeth
4–6, 9–11, 13–19	103(a)	Johnson, Keeth, Jeddeloh

III. ANALYSIS

A. *Legal Standards*

A claim is unpatentable under 35 U.S.C. § 103(a) “if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a); *see KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations of nonobviousness.⁶ *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

⁵ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102 and 103. Because the ’835 patent was filed before March 16, 2013 (the effective date of the amendments), the pre-AIA version of § 103 applies.

⁶ The record does not include any evidence of secondary considerations of nonobviousness.

B. Level of Ordinary Skill in the Art

Citing testimony from Dr. Baker, Petitioner asserts a person of ordinary skill in the art (hereinafter “POSITA”) “would have had a bachelor’s degree in electrical engineering, computer engineering, or the equivalent, and two to three years of experience designing high speed computer memory devices.” Pet. 4 (citing Ex. 1002 ¶¶ 31–35). Patent Owner’s expert, Mr. Lee, testifies: “I agree with Petitioner that [Petitioner’s statement of the level of ordinary skill] would be the minimum qualifications for a POSITA.” Ex. 2001 ¶ 35.

On this record, we adopt Petitioner’s statement of the level of ordinary skill in the art, i.e., that a POSITA “would have had a bachelor’s degree in electrical engineering, computer engineering, or the equivalent, and two to three years of experience designing high speed computer memory devices.” Ex. 1002 ¶ 34. The stated level is supported by the testimony of Dr. Baker and not disputed by Patent Owner. Further, it appears consistent with what is reflected by the content of the applied prior art. *Cf. Okajima v. Bourdeau*, 261 F.3d 1350, 1354–55 (Fed. Cir. 2001) (the applied prior art may reflect an appropriate level of skill).

C. Claim Interpretation

We use the same claim construction standard that would be used to construe a claim in a civil action under 35 U.S.C. § 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. 37 C.F.R. § 42.100(b). The claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc) is applicable.

Claim terms are generally given their ordinary and customary meaning as would be understood by one with ordinary skill in the art in the context of the specification, the prosecution history, other claims, and extrinsic evidence including expert and inventor testimony, dictionaries, and learned treatises, although extrinsic evidence is less significant than the intrinsic record. *Phillips*, 415 F.3d at 1312–17. Usually, the specification is dispositive, and it is the single best guide to the meaning of a disputed term. *Id.* at 1315.

The specification may reveal a special definition given to a claim term by the patentee, or the specification or prosecution history may reveal an intentional disclaimer or disavowal of claim scope by the inventor. *Phillips*, 415 F.3d at 1316. “There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Thorner v. Sony Comput. Ent. Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

If an inventor acts as his or her own lexicographer, the definition must be set forth in the specification with reasonable clarity, deliberateness, and precision. *Renishaw PLC v. Marposs Societa’ per Azioni*, 158 F.3d 1243, 1249 (Fed. Cir. 1998). The disavowal, if any, can be effectuated by language in the specification or the prosecution history. *Poly-Am., L.P. v. API Indus., Inc.*, 839 F.3d 1131, 1136 (Fed. Cir. 2016).

Only those claim terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent

necessary to resolve the controversy.” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

Neither party has proposed a construction for any claim term. Petitioner states: “Petitioner believes that no express constructions of the claims are necessary to assess whether the Challenged Claims read on the prior art.” Pet. 16 (footnote omitted). In addition, Petitioner states:

In the co-pending litigation, the Court construed the preambles of claims 1, 7, 12, 20, and 23 as non-limiting. Ex-1007, 8. The Court also construed “the valid operation range includes an optimal operation point for the integrated circuit device” in claims 1 and 7 according to its plain and ordinary meaning and specified that “this claim element does not require determining the optimal operation point.” *Id.*

Id. at 15–16.

We find it appropriate to construe the term “valid operation range” within limitations [1.4.a] and [7.3.a], as well as the term “valid operating range” within limitations [12.4], [20.4], and [23.4].

At the outset, we find no basis for any distinction, based on the specification of the ’835 patent, the prosecution history of the ’835 patent as presented by either party, and the extrinsic evidence of record, between “operation range” and “operating range.” The two have the same meaning. Hereinbelow, when we refer to “operation range,” we likewise refer to “operating range.”

“valid operation range”

As background, the ’835 patent notes that the design and fabrication of high-performance signaling mechanisms for digital integrated circuit devices has become a significant challenge, and that modern memory integrated circuit designs require exacting control of critical timing

specifications, and design parameters must be strictly maintained to keep the entire system in balance. Ex. 1001, 1:14–16, 22–25. It is stated that “what is required is a solution that can ensure critical timing specifications remain within certain specified parameters.” *Id.* at 1:29–31.

Notably, the '835 patent describes that the intra-cycle timing relationships between three parameters are calibrated to ensure the optimal operation of disclosed DRAM components 110. Ex. 1001, 3:13–16. The three parameters are the command/address signals, the DQ (data) signals, and the DQS (sampling) signals. *Id.* For proper calibration, a delay calibrator circuit is provided to adjust the phase delays of all three command/address signals, data signals, and sampling signals. *Id.* at 3:3–12.

The '835 patent provides a single illustration of “a valid region” of the integrated circuit device, and it is via its Figure 5, reproduced below:

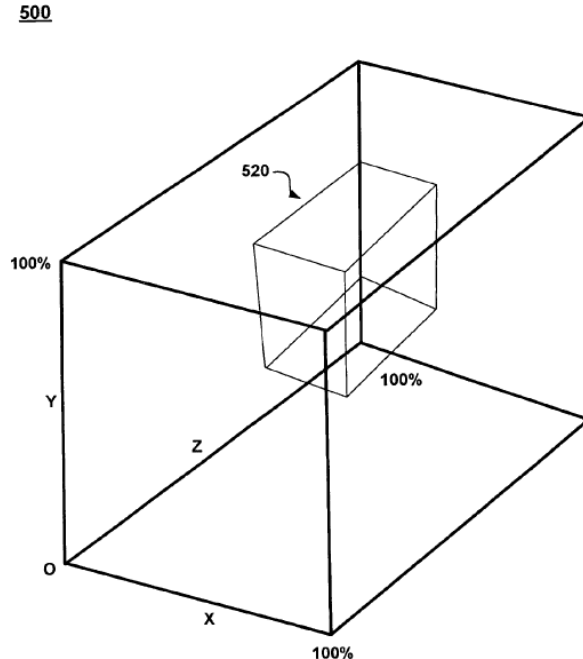


FIGURE 5

Figure 5 shows a diagram of a typical case where three parameters x, y, and z are varied across a range of adjustment to obtain valid windows for a DDR memory. Ex. 1001, 1:56–58; 5:25–27. The '835 patent describes:

FIG. 5 shows a diagram 500 of typical case where three parameters x, y, z are varied across a range of adjustment to obtain valid windows for a DDR memory. As depicted in FIG. 5, the three axes of the parameters are plotted orthogonal to one another. In the case of a DDR DRAM component, for example, the x parameter can correspond to a phase range of command/address signals, the y parameter can correspond to a phase range of DQ signals, and the z parameter can correspond to a phase range of DQS signals.

For a given device, there will be a valid region within which the values of the x, y, and z parameters result in the correct operation of the device. This is shown in FIG. 5 as the valid region 520. . . .

Embodiments of the invention automatically alter the x, y, and z parameters (e.g., the intra-cycle command/address phase, DQ phase, and the DQS phase) in order to determine the boundaries of *the valid region 520*. Once such boundaries are discovered, configuration choices can be intelligently made as to the optimal operating point for a given device.

Embodiments of the present invention determine the boundaries of the *valid region 520* by systematically altering the variable parameters. In one embodiment, a course calibration method is first used in order to determine whether or not *a valid region 520* exists, and a fine calibration method is subsequently used in order to determine[] the *precise boundaries of the valid region 520*.

Id. at 5:25–58 (emphasis added). Also, the '835 patent describes a pseudo code representation of the calibration process, which is a three-parameter test function of x, y, and z, “test(x,y,z).” *Id.* at 6:16–40. The “x,y,z” parameters are “remembered” if “test(x,y,z)” passes evaluation. *Id.*

As noted above, the specification consistently and repeatedly identifies and refers to a valid region of the integrated circuit memory device as having a three-dimensional boundary delimited by phase ranges in command/address signals, data signals, and sampling signals. Nowhere does the '835 patent specification indicate a valid region of the integrated circuit device as a whole can be represented by values for less than three parameters x, y, and z, all together, e.g., the command signals, the data signals, and the sampling signals. Also, the '835 patent describes that the purpose of determining the boundaries of a valid region is to configure an optimal operating point for the integrated circuit device. Ex. 1001, 5:48–51.

We have also considered other language in the claims. Each of independent claims 1 and 7 requires adjustment of the phase of all three command signals, data signals, and sampling signals, to determine the “valid operation range.” Ex. 1001, 6:56–7:4, 7:18–34. Each of independent claims 12, 20, and 23 requires adjustment of the phase of all three command signals, data signals, and sampling signals, to determine the “valid operating range.” Ex. 1001, 7:46–60, 8:28–44, 8:62–10:4.

Based on the foregoing, the specification informs us that “valid operation range” is a three-dimensional range. We recognize that the specification does not expressly exclude a two-dimensional range or multiple two-dimensional ranges from being a “valid operation range” of the integrated circuit device. However, that is why we construe the claims to determine what, if anything, may be required despite a lack of express recitation in the claims.

It is not a proper approach to claim interpretation to assume that what is not expressly excluded by statements in the specification necessarily is

encompassed by the scope of the claims. Our reviewing court has explained, in the context of what constitutes “broadest reasonable interpretation”:

The correct inquiry in giving a claim term its broadest reasonable interpretation in light of the specification is not whether the specification proscribes or precludes some broad reading of the claim term adopted by the examiner. And it is not simply an interpretation that is not inconsistent with the specification. It is an interpretation that corresponds with what and how the inventor describes his invention in the specification, *i.e.*, an interpretation that is “consistent with the specification.” *In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997) (citation and internal quotation marks omitted); *see also In re Suitco Surface*, 603 F.3d 1255, 1259–60 (Fed. Cir. 2010).

The Board emphasized that the patentee here did not act as a lexicographer, and that the specification neither defines nor precludes the examiner’s reading of the term “body.” Accordingly, the Board found that nothing in the specification would disallow the examiner’s interpretation, rendering it “reasonable.” However, following such logic, any description short of an express definition or disclaimer in the specification would result in an adoption of a broadest *possible* interpretation of a claim term, irrespective of repeated and consistent descriptions in the specification that indicate otherwise. That is not properly giving the claim term its broadest reasonable interpretation *in light* of the specification.

In re Smith International, Inc., 871 F.3d 1375, 1382–83 (Fed. Cir. 2017).

Although we apply the *Phillips* standard in an *inter partes* review proceeding, not the standard of broadest reasonable interpretation, a construction under the *Phillips* standard is no broader than that under the rule of broadest reasonable interpretation. *Facebook, Inc. v. Pragmatus AV, LLC*, 582 Fed. App’s 864, 869 (Fed. Cir. 2014) (unpublished).

We conclude that “valid operation range” of the integrated circuit device (claims 1 and 7), DRAM (claim 12), or DDR DRAM (claims 20 and

23) is a three-dimensional range including a boundary for each of three underlying parameters which, for example, may be the phases of the command signals, the data signals, and the sampling signals. The same interpretation applies to “valid operating range.”

D. Alleged Obviousness of Claims 1–23 over Johnson and Jeddeloh

1. Overview of Johnson (Exhibit 1004)

Johnson is a U.S. Patent titled “Calibration Technique for Memory Devices.” Ex. 1004, code (54). It relates to an improved binary calibration technique useful “for calibrating the timing of control and data signals in memory devices, for example, SLD RAM memory devices.” Ex. 1004, 1:5–8. Johnson begins with its Figure 1, reproduced below:

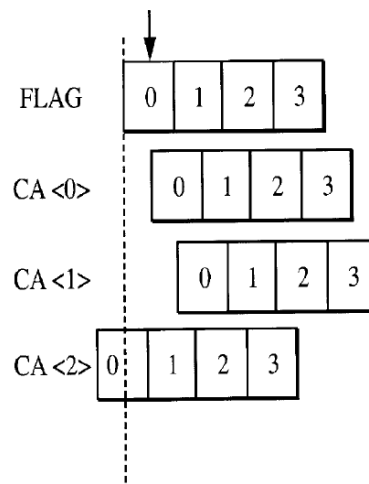


FIG. 1
PRIOR ART

Figure 1 of Johnson shows raw data coming into a SLD RAM module from a memory controller for a representative FLAG data path, and three of the command bus data paths CA<0>, CA<1> and CA<2>. Ex. 1004, 2:15–18.

Johnson describes preexisting synchronization as follows:

One of the several calibration procedures which is performed in current SLDRAM devices is a timing synchronization of clock signals CCLK (command clock signal) and DCLK (data clock signal) with data provided on an incoming command path CA and FLAG path (for the CCLK signal) and on the data paths DQ (for the DCLK signal) so the incoming data is correctly sampled. . . . The SLDRAM recognizes this pseudo random sequence by two consecutive “1” appearing on the FLAG bit and determines an optimal internal delay for CCLK and DCLK relative to the data each clocks to optimally sample the known bit pattern. *This optimal delay is achieved by adjusting the temporal position of the received data bits to achieve a desired bit alignment relative to the clock. This is accomplished by adjusting a delay in the receiving path of the received data until the received data is properly sampled by the clock and recognized internally.*

Ex. 1004, 1:42–64 (emphasis added). Johnson further explains the preexisting synchronization method:

In prior synchronization schemes using a calibration bit pattern as discussed above, all incoming data can properly be aligned with respect to the clock used to latch in the data by adjusting the data delays relative to the clock (CCLK or DCLK) to position a sampling clock edge at or near the center of the data “eye” or “window” where the data is valid on an incoming data path. However, this calibration procedure is *independently carried out for each incoming data path*, which may take some time and which also may, in extreme cases, cause the data “eye” on different incoming data paths to be aligned on different edges of the clock signal.

Id. at 2:3–9 (emphasis added).

Johnson also describes a problem with preexisting synchronization techniques: “However, as is also shown in FIG. 2, it is possible that the data bits in one data path are misaligned, or aligned to an edge of the clock

opposite to that of another data path.” *Id.* at 2:30–33. Figure 2 of Johnson is reproduced below:

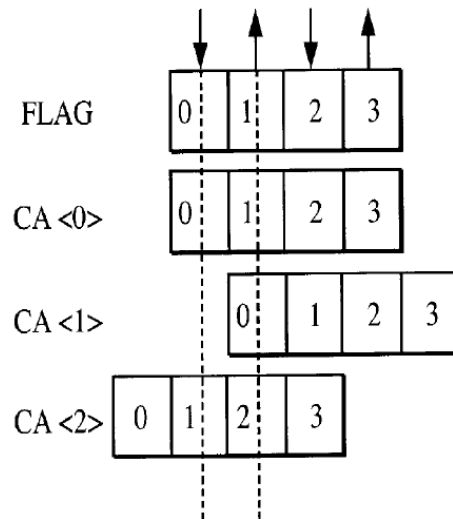


FIG. 2
PRIOR ART

Figure 2 illustrates a serial alignment of the data bits incoming on different data paths. *Id.* at 2:62–63.

Johnson further describes the problem:

For example, while the position of data on the CA<0> data path and the data on the FLAG data path are properly aligned with each other, these two are misaligned with respect to the data bits on the CA<1> and CA<2> data paths. Thus, even though serial calibration of each data line relative to the clock CCLK has been achieved, there is still a possibility for misalignment in a parallel direction across all of the data paths.

Ex. 1004, 2:33–41.

Johnson describes its solution as follows: “Serial data alignment is first acquired for one of the incoming data paths, and then the remaining data paths are bit wise aligned in parallel to a previously aligned data path.

In this way, serial and parallel calibration of all data paths is achieved.”

Ex. 1004, 2:47–51. Specifically, Johnson explains:

Accordingly, in the present invention, one of the data lines, e.g., FLAG, is first serially calibrated using the procedures described above with reference to FIGS. 1–7. Then, instead of calibrating the remaining data lines in the same manner, the remaining data lines are calibrated to a previously calibrated data line, e.g., the FLAG data path.

Id. at 6:34–39.

2. *Overview of Jeddeloh (Exhibit 1005)*

Jeddeloh is a U.S. Patent titled “Apparatus for Synchronizing Strobe and Data Signals Received from a RAM.” Ex. 1005, code (54). Jeddeloh refers to a DDR “Double Data Rate SDRAM.” *Id.* at 1:45. Jeddeloh describes a preexisting problem as follows:

Designing an interface that receives a data strobe signal from a DDR memory during a read operation presents challenges because a certain amount of skew typically arises between the data signal and the data strobe signal. If this skew is large enough, a data strobe edge, which is used to latch the data signal, can move from the center of the “data eye” of the data signal into a transitional region or into another data eye. This may cause spurious data to be latched during a read operation. Skew may additionally arise between the data signal and an enable signal for an input driver that is used to drive the data signal from a memory bus into a latch in the processor (or in the memory controller). This type of skew may also cause spurious data to be latched during read operations.

Ex. 1005, 1:54–67. Jeddeloh states that what is needed is (1) “a system that adjusts the temporal alignment between a data signal and an associated data strobe signal received from a memory during a read operation,” and (2) “a system that adjusts the temporal alignment between a data signal received

during a read operation and an associated input driver enable signal.” *Id.* at 2:1–6.

Jeddeloh explains its invention as follows:

One embodiment of the present invention provides an apparatus that synchronizes a data signal and a data strobe signal received from a random access memory. This apparatus includes a mechanism that initiates a read operation to the random access memory by sending a target address for the read operation to the random access memory. The apparatus also includes an input driver that receives the data signal containing data retrieved from the target address from the random access memory. Coupled to the input driver is a register that stores the data signal. A first programmable delay circuit is coupled to an enable input of the input driver in order to synchronize the driving of the input driver with the data signal received from the random access memory. *A second programmable delay circuit is coupled between the data strobe signal and a clock input of the register. This second programmable delay circuit is configured to delay the data strobe signal so as to synchronize the data strobe signal with the data signal received from the random access memory.*

Ex. 1005, 2:8–25 (emphasis added).

3. *Independent Claim 1*

a. *Preamble recitation [1.P]*

The preamble recites: “A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, the method comprising:”

Ex. 1001, 6:56–59. According to Petitioner, Johnson teaches this preamble recitation. Pet. 17–20. Patent Owner expresses no view on Petitioner’s accounting for the preamble. We need not determine whether this preamble recitation is limiting nor whether Petitioner’s accounting for the preamble is adequate because, as we discuss below, Petitioner has not sufficiently accounted for limitations [1.3], [1.4.a], and [1.4.b].

b. Limitation [1.1]

Limitation [1.1] recites: “generating command signals to access an integrated circuit component.” Ex. 1001, 6:60–61.

Petitioner explains:

Johnson discloses that a “plurality of SLDRAM modules 11a...11n [] are accessed and controlled by [] memory controller 13.” Ex-1004, 3:31-33. The memory controller 13 “provides a command link to each of the SLDRAM modules 11a...11n which includes [] a 10 bit command bus data path CA0-9” (the recited “command signals”). *Id.*, 3:33-38; Ex-1002, ¶113, Data on CA0-9” is clocked in by sequential positive and negative going transitions of the command clock signal CCLK.” Ex-1004, 4:67-5:3.

Pet. 20. Petitioner also explains that a control logic circuit of an SLDRAM module receives and analyzes commands on the CA0-9 bus and controls the input/output access operations of the memory banks. *Id.* at 21 (citing Ex. 1004, 3:57–60). On that basis, Petitioner asserts:

Accordingly, a POSITA would have understood that *Johnson’s* SLDRAM modules 11a...11n are integrated circuit components accessed by command signals generated by the memory controller. Ex-1002, ¶¶113, 117. A POSITA would have understood that *Johnson’s* memory controller performs the “generating,” at least because such controllers were well-known to manage the flow of information between memory and CPUs, and did so by generating and issuing commands to memory modules to execute read or write operations. *Id.*, ¶¶115, 117; Ex-1015, 2; Ex. 1016, 4; Ex-1017, 1.

Id. at 22–23. We need not make any determination with respect to limitation [1.1], because Petitioner has not sufficiently accounted for limitations [1.3], [1.4.a], and [1.4.b].

c. Limitation [1.2]

Limitation [1.2] recites: “accessing data signals to convey data for the integrated circuit component.” Ex. 1001, 6:62–63.

Petitioner asserts:

Johnson discloses that “a bi-directional data bus DQ0-17 is provided between memory controller 13 and each of the SDRAM modules 11*a*. . . 11*n*, as are bi-directional data clocks DCLK0 and DCLK1. The clock DCLK0 is used to strobe **input/output data into and out of the SDRAM modules[.]**” Ex-1004, 3:41-45. *Johnson* explains that data (the recited “data signals to convey”) to be input to a memory bank of an SDRAM module (the recited “integrated circuit component”) “is supplied by memory controller 13 (FIG. 3) on the DQ data bus.” *Id.*, 4:12-14; Ex-1002, ¶118.

Pet. 23. Petitioner also asserts:

Johnson further teaches that SDRAM modules include a latch to “latch in incoming data on the data bus DQ.” Ex-1004, 4:24-26. During a write operation, “[d]ata which is to be input[ted] to memory banks 69, 71 is supplied by memory controller 13 (FIG. 3) on the DQ data bus[.]” Ex-1004, 4:12-18. During a read operation, data output from memory banks 69 and 71 pass through the circuitry until it is “passed back to memory controller 13 (FIG. 3) via data bus DQ.” *Id.*, 4:5-11.

Id. at 24.

Petitioner further asserts that *Johnson*’s memory controller 13 accesses data signals output from memory banks of an SDRAM module and transmitted *via data bus DQ* during a read operation, and that *Johnson*’s SDRAM module accesses data signals transmitted from memory controller 13 *via data bus DQ* during a write operation. Pet. 25 (emphasis added) (citing Ex. 1002 ¶121; Ex. 1004, 4:12–18).

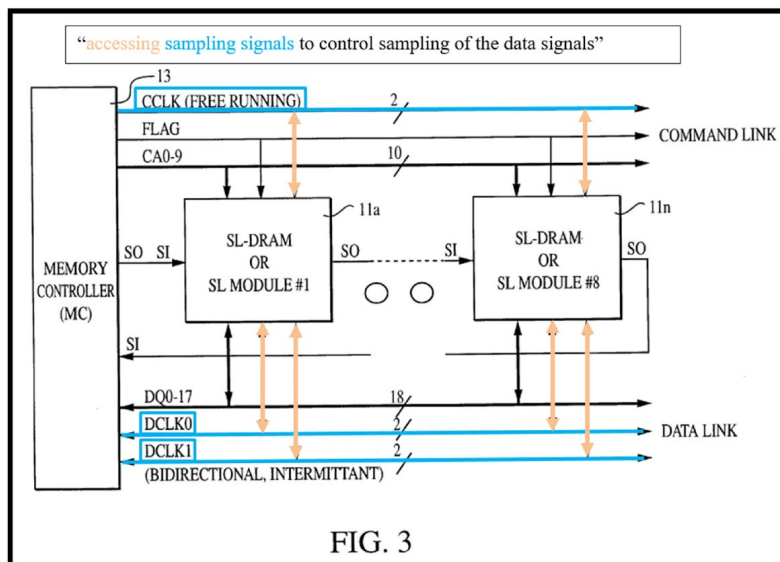
Petitioner concludes that Johnson discloses limitation [1.2]. Pet. 25. We need not make any determination with respect to limitation [1.2], because Petitioner has not sufficiently accounted for limitations [1.3], [1.4.a] and [1.4.b].

d. Limitation [1.3]

Limitation [1.3] recites: “accessing sampling signals to control sampling of the data signals; and.” Ex. 1001, 6:64–65.

Petitioner explains:

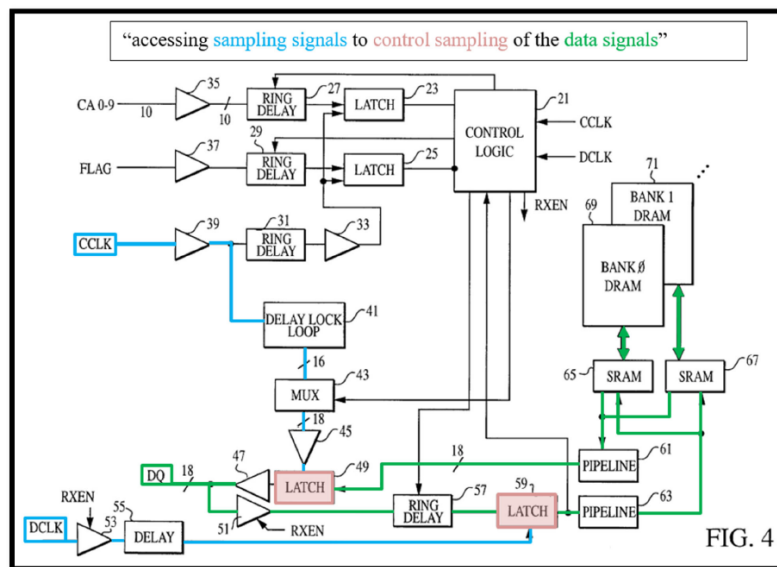
Johnson discloses providing clock signals CCLK, DCLK0, and DCLK1 (the recited “sampling signals”) to “strobe input/output data into and out of the SLDRAM modules” (the recited “to control sampling of the data signals”). Ex-1004, 3:44–45; Ex-1002, ¶123. Annotated Figure 3 below illustrates the clock signals CCLK, DCLK0, and DCLK1.



[Johnson’s Figure 3 illustrates an SLD RAM bus topology for use with Johnson’s invention. Ex. 1004, 2:64–65. Petitioner has color annotated CCLK, DCLK0, and DCLK1 as sampling signals and their connections to the memory modules.] Ex-1004, 3; Ex-1002, ¶124.

Johnson explains that “[m]emory controller 13 provides a command link to each of the SLDRAM modules 11a. . . 11n

which includes a clock signal CCLK.” Ex-1004, 3:33-36. In addition, “bi-directional data clocks DCLK0 and DCLK1” are provided “between memory controller 13 and each of the SDRAM modules 11a. . . 11n.” *Id.*, 3:42-44. DCLK0 and DCLK1 are used to “strobe input/output data into and out of the SDRAM modules” *Id.*, 3:44-45; Ex-1002, ¶125. The memory controller 13 therefore accesses data sampling signals when data is read from or written to the SDRAM modules. Ex-1002, ¶123. Each SDRAM module also accesses data sampling signals when data is read from or written to the respective SDRAM module. *Id.* Sampling of data signals is further discussed in reference to annotated Figure 4 below.



[Johnson’s Figure 4 illustrates a portion of the SDRAM module shown in Figure 3. Ex. 1004, 2:66–67. Petitioner has color annotated a path from input CCLK to latch 49, a path from latch 49 to data bus DQ, a path from input DCLK to latch 59, a path from incoming data on data bus DQ to latch 59, as well as paths from memory banks to the latches.] Ex-1004, 4; Ex-1002, ¶125.

Johnson explains that “[t]he signal CCLK [] passes from buffer 39 into a delay lock loop circuit 41” that provides clock signals into a multiplexer. *Id.*, 4:1[-]3. The multiplexer provides “clock output signals through respective buffers” to latches 49, which latch the data output from the memory banks. *Id.*, 4:3-5; Ex-1002, ¶126. “The output data latched in latches 49” is passed “to memory controller 13 [] via data bus DQ.” Ex-1004, 4:5-11.

CCLK therefore controls sampling of data signals at least when the data signals are output from the memory banks onto the data bus DQ. Ex-1002, ¶126.

Additionally, the data clock DCLK “passes through gated buffer 53, delay circuit 55 and is used to **control latch 59 to latch in incoming data on the data bus DQ.**” Ex-1004, 4:23-26. Johnson’s calibration process is implemented such that the circuit of Figure 4 is “synchronized to ensure that the incoming data is properly clocked in by the clock signals CCLK and DCLK.” *Id.*, 4:29-31. By latching or clocking data, the sampling signals CCLK, DCLK0, and DCLK1 control the sampling of the data signals. Ex-1002, ¶¶126-129.

Pet. 26–29.

Patent Owner asserts that clock signal CCLK is not a sampling signal for data signal DQ. Prelim Resp. 24. According to Patent Owner’s expert, Dr. Lee, DCLK is the sampling signal for data signal DQ. Ex. 2001 ¶64. We credit that testimony because (1) Petitioner clearly identifies data signals on data bus DQ0-17 of Johnson as the claimed “data signals” (Pet. 29), and (2) as shown in Johnson’s Figure 4, data bus DQ (same as DQ0-17 denoting 18 data lines) is on the input side of latch 59 (activated by DCLK) but on the output side of latch 49 (activated by CCLK). Petitioner has not shown that latch 49 samples anything on data bus DQ which, as shown in Johnson’s Figure 3 as DQ0-17, is external to the SLDRAM modules. We are not sufficiently persuaded even for institution purposes that Johnson’s CCLK is a sampling signal.

e. Limitation [1.4.a]

Limitation [1.4.a] reads: “systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device.” Ex. 1001, 6:66–7:2.

Petitioner identifies Johnson's clock signals CCLK and DCLK (both DCLK0 and DCLK1) as satisfying the sampling signals recited in claim 1. Pet. 26. We discussed above in the context of limitation [1.3] why Petitioner has not sufficiently shown that CCLK is a sampling signal. Even assuming that CCLK is a sampling signal, however, Petitioner still has not shown that Johnson and Jeddeloh teach or suggest limitation [1.4.a].

Petitioner explains:

Johnson discloses testing delay values of the command signals transmitted via data bus CA0-9 (the recited "a phase shift of the command signals") to determine values that result in alignment with CCLK and testing delay values of the data signals transmitted by data bus DQ0-17 (the recited "a phase shift of the data signals") to determine values that result in alignment with DCLK. Ex-1004, 1:42-48, Ex-1002, ¶130. *Johnson* identifies a range of delay values that result in valid sampling for the memory device (the recited "determine a valid operation range of the integrated circuit device"). Ex-1004, 4:41-43, Ex-1002, ¶130.

Pet. 29. Petitioner additionally explains that Johnson teaches "parallel calibration":

Johnson teaches "parallel calibration of all data paths[.]" by "aligning the ring delays of a path under calibration to an immediate previously calibrated data path until all data paths have been calibrated." *Id.*, 2:51-52. Based on the calibration, VALID signals are generated by compare circuits to "signal whether the synchronization pattern is properly recognized to the logic 81" (the recited "to determine a valid operation range of the integrated circuit device"). *Id.*, 6:48-54; Ex-1002, ¶¶135-136. A POSITA would have understood that Johnson's signals are cyclic signals having a phase such that a delay (i.e., shift) in timing of such signals is a phase shift. Ex-1004, 5 (showing cycles of CCLK, FLAG, CMD, DQ, and DCLK signals), 8:41-44; Ex-1002, ¶136.

Id. at 30.

Regarding adjustment of the phase of command signals, Petitioner asserts:

Regarding command signals, *Johnson* discloses that a “synchronizing pattern is applied to” data input paths CA0-9 “while the data pattern is sampled in latches 23 and 25 by the delayed clock signal CCLK” (“systematically altering a phase shift of the command signals”). Ex-1004, 2:33-36; Ex-1002, ¶134. Specifically, “[t]he control logic circuit 21 steps through all possible delay positions of ring delays 27 and 29 [] and stores patterns representing which delay values [] provide for a correct sampling and recognition” of the synchronization pattern. Ex-1004, 4:36-41. The synchronization pattern is used to establish “an ‘eye’ or ‘window’ of acceptable delays for each of the ring delays 27 for the command data paths CA0-9.” *Id.*, 2:41-43; Ex. 1002 ¶134.

Pet. 31–32.

Regarding adjustment of the phase of data signals, Petitioner asserts:

Regarding data signals, *Johnson* teaches that “[t]he same calibration process may be carried out on [] any one of the receive data paths of the data bus DQ.” Ex-1004, 4:55-59. While CA0-9 data paths are aligned to CCLK, “the data paths DQ0-17 are aligned to [DCLK].” *Id.*, 6:46-48. For example, *Johnson* discloses that the calibration discussed above may be used to align data path DQ<0> “until a final delay value is selected” (the recited “systematically altering [] a phase shift of the data signals”). *Id.*, 25-31; Ex-1002, ¶136. “Once a first data path, e.g., DQ0, is serially aligned to DCLK [] the remaining DQ1-17 data paths can be aligned.” Ex-1004, 7:36-42. The control logic 21 “steps through all possible delay values of ring delay 57*b*, and notes those delays which produce a coincidence of the calibration pattern on data paths D<0> and DQ<1>, and selects a final delay value for delay 57*b* which is at or near the center of acceptable delays.” Ex-1004, 7:52-57. A POSITA would have understood that *Johnson*’s methodical procedure for “step[ping] through” phase shifts to calibrate delays of both command signals and data signals is “systematically altering.” Ex-1002, ¶136.

Johnson further teaches that “control logic circuit 21 includes compare circuit 83*a*, which aligns the DQ1 data path including ring delay 57*b* to the previously aligned DQ0 data path which includes ring delay 57*a* by comparing the calibration pattern on aligned data path DQ0 with the calibration pattern on the DQ1 data path to generate an appropriate validity signal on signal lines VALID.” Ex-1004, 7:46-52. *Johnson*’s calibration is therefore used to “determine a valid operation range of the integrated circuit device.” Ex-1002, ¶135.

Id. at 32–33.

Regarding adjustment of the phase of the sampling signals, Petitioner asserts:

To the extent Patent Owner argues that *Johnson* does not explicitly describe stepping through delays for its CCLK or DCLK signals (each a “sampling signal”), as shown in annotated Figure 4 above, *Johnson* discloses that the “signal CCLK also passes from buffer 39 into a **delay lock loop circuit 41** which provides 16 clock signals into a multiplexer 43. The **multiplexer provides 18 clock output signals** through respective buffers 45 to 18 latches 49 which latch data output from the memory banks 69, 71.” *Id.*, 2:1–8; Ex-1002, ¶133. Figure 4 of *Johnson* shows that the data output from the memory banks 69, 71 does not pass through a delay before it reaches latches 49 where it is latched by CCLK. Ex-1004, 4; Ex-1002, ¶133. A POSITA would have therefore recognized a need for alignment between CCLK and the data signals at least at latches 49. *Id.* *Johnson* also shows that DCLK is delayed as it passes through “delay circuit 55” latching a data signal at latch 59. Ex-1004, 4:24-26.

Pet. 33–34.

Even assuming that all of the above-quoted assertions are correct, Petitioner still has not made a sufficient showing for limitation [1.4.a]. That is because Petitioner has, at best, identified only two 2-parameter valid operation ranges, i.e., an operation range involving just command and sampling signals, and an operation range involving data and sampling

signals. Pet. 29–34. This does not satisfy “valid operation range” as we have construed above in Section III.C. Specifically, we determined that “valid operation range” is a three-dimensional range including a boundary for each of three underlying parameters which, for example, may be the phases of the command signals, the data signals, and the sampling signals. Nowhere has Petitioner identified or explained how Johnson discloses a valid operation range that is a function of three parameters together, e.g., the respective phases of command signals, data signals, *and* sampling signals.

In addition to the foregoing, Petitioner’s reasoning for adjusting the phase of clock signals DCLK, which Petitioner regards as sampling signals, to synchronize with the phase of data signals on the DQ data bus is unpersuasive, because Johnson, as Petitioner has recognized, already adjusts the phase of data signals on the DQ data bus to synchronize with clock signals DCLK. Pet. 32 (citing Ex. 1002 ¶ 136; Ex. 1004, 4:55–59, 6:46–48, 7:25–31, 7:36–42). The proposed adjustment is redundant and serves little, if any purpose. Petitioner has not proposed to stop adjusting the data signals relative to DCLK. Nor has Petitioner articulated a reason to do the adjustment in both directions, i.e., adjusting the data signals relative to the sampling signals and adjusting the sampling signals relative to the data signals.

We have also determined above, in discussing limitation [1.3], that Petitioner has not sufficiently shown that Johnson’s CCLK signal is a sampling signal. Further, we agree with Patent Owner (Prelim. Resp. 24) that neither delay 55 nor delay lock loop 41 in Johnson’s Figure 4 is used for systematic calibration of any signal or in a signal calibration process. We

find that the mere presence of a delay element in a signal path does not reasonably suggest systematic calibration.

For the foregoing reasons, Petitioner has not sufficiently shown that Johnson alone teaches or suggests limitation [1.4.a].

Relying, in the alternative, on additional teaching from Jeddeloh, Petitioner asserts:

To the extent that *Johnson* does not explicitly explain or render obvious how CCLK or DCLK are synchronized to the data signals received from and sent to the DRAM banks, a POSITA would have had reason to look to *Jeddeloh* for specificity as to how to synchronize the signals. *Id.*, ¶144. *Johnson* does disclose applying delay circuits to the sampling signals CCLK and DCLK, albeit without intricate detail. Ex-1004, 1:57-5, 4:1-3; 4:24-26; Ex-1002, ¶¶141-142. A POSITA would have recognized the advantages of applying *Jeddeloh*'s defined technique of systematically altering a phase shift of sampling signals to the delays of *Johnson*. Ex-1002, ¶141. A POSITA would have been motivated to make such a modification at least to improve synchronization of data signals and sampling signals when both writing to and reading from DRAM banks. Ex-1002, ¶143.

Pet. 36. This “looking to Jeddeloh for more detail” argument is unavailing because, as discussed above, we find that Johnson’s CCLK signal is not a sampling signal. Also, for reasons discussed above in the context of Petitioner’s reliance on Johnson alone, adjusting the phase of DCLK to synchronize with data signals on the data bus DQ is redundant and makes little sense, because Johnson already discloses adjusting the phase of data signals to synchronize with DCLK. We are not sufficiently persuaded that synchronizing DCLK to data signals as Jeddeloh teaches, if adopted in Johnson, would improve synchronization, given that in Johnson data signals are already synchronized to DCLK.

In any event, even assuming that Johnson's CCLK is a sampling signal, that Johnson does disclose the idea of adjusting the phase of sampling signals, and that one of ordinary skill in the art would have looked to Jeddeloh with regard to more detail on adjusting the phase of CCLK and DCLK, Petitioner's showing still is deficient for institution purposes. The resulting combination as articulated by Petitioner does not cure the deficiency discussed above for Johnson alone. Petitioner still nowhere identifies or explains the determination of a valid operation range that is a three-dimensional range including a boundary for each of three underlying parameters which, for example, may be the phases of the command signals, the data signals, and the sampling signals. As Patent Owner correctly notes, Johnson at best determines two 2-parameter ranges, not a single 3-parameter range. Prelim. Resp. 29. This remains true notwithstanding the addition of Jeddeloh in combination with Johnson.

For the foregoing reasons, Petitioner has not shown that Johnson and Jeddeloh together teach or suggest limitation [1.4.a].

f. Limitation [1.4.b]

Limitation [1.4.b] recites: "wherein the valid operation range includes an optimal operation point for the integrated circuit device. Ex. 1001, 7:2–4.

Because Petitioner has not sufficiently met the "valid operation range" recitation of limitation [1.4.a], Petitioner equally has not sufficiently met the further requirement of an "optimal condition" included within the "valid operation range" as recited in limitation [1.4.b] for the integrated circuit device.

g. Conclusion for Claim 1

For the foregoing reasons, Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of claim 1 over Johnson and Jeddeloh.

4. Dependent Claims 2–6

Claims 2–6 each depend, directly or indirectly, from claim 1. Ex. 1001, 7:5–17. The above-discussed deficiency for claim 1 applies equally to claims 2–6. Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of any of claims 2–6 as obvious over Johnson and Jeddeloh.

5. Independent Claim 7

Claim 7 is an apparatus claim and includes a delay calibrator within a controller. Ex. 1001, 7:18–34. Claim 7 recites that the delay calibrator is “further configured to systematically alter a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device.” *Id.* at 7:27–32. Petitioner has identified this requirement of the claimed delay calibrator as limitation [7.3.a]. Pet. x. Limitation [7.3.a] corresponds to the step according to limitation [1.4.a] of claim 1.

To account for limitation [7.3.a], Petitioner relies on its arguments for limitation [1.4.a] of claim 1. Pet. 56 (citing Ex. 1002 ¶ 184). The above-discussed deficiency of the Petition in accounting for limitation [1.4.a] applies equally to limitation [7.3.a].

Limitation [7.3.b] recites “wherein the valid operation range includes an optimal operation point for the integrated circuit device.” Pet. x. Because Petitioner has not sufficiently met the “valid operation range”

recitation of limitation [7.3.a], Petitioner equally has not sufficiently met the further requirement of an “optimal condition” included within the “valid operation range” as recited in limitation [7.3.b] for the integrated circuit device.

We determine Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of claim 7 over Johnson and Jeddeloh.

6. *Dependent Claims 8–11*

Claims 8–11 each depend, directly or indirectly, from claim 7. Ex. 1001, 7:35–45. The above-discussed deficiency for claim 7 applies equally to claims 8–11. Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of any of claims 8–11 as obvious over Johnson and Jeddeloh.

7. *Independent Claim 12*

Claim 12 is a method claim and recites the following step: “systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operating range of the DRAM component.” Ex. 1001, 7:57–60. Petitioner has identified this step as limitation [12.4]. Pet. xi. Limitation [12.4] is the same as limitation [1.4.a], except that limitation [12.4] refers to “a valid operating range of the DRAM component” rather than to “a valid operation range of the integrated circuit device.”

To account for limitation [12.4], Petitioner relies on its arguments for limitation [1.4.a] of claim 1. Pet. 58. The above-discussed deficiency of the Petition in accounting for limitation [1.4.a] applies equally to limitation [12.4]. We determine Petitioner has not shown a reasonable likelihood that

it would prevail in establishing obviousness of claim 12 over Johnson and Jeddeloh.

8. *Dependent Claims 13–19*

Claims 13–19 each depend, directly or indirectly, from claim 12. Ex. 1001, 7:61–8:27. The above-discussed deficiency for claim 12 applies equally to claims 13–19. Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of any of claims 13–19 as obvious over Johnson and Jeddeloh.

9. *Independent Claim 20*

Claim 20 recites a computer readable media having stored thereon computer executable instructions that, if executed by a processor, causes the processor to perform a method. Ex. 1001, 8:28–44. The method includes the following step: “systematically altering a phase shift of the command signals, a phase shift of the DQ signals, and a phase shift of the DQS signals to determine a valid operating range of the DDR DRAM component.” *Id.* at 8:41–44. Petitioner has identified this step as limitation [20.4]. Pet. xiii. Limitation [20.4] is the same as limitation [1.4.a], except that limitation [20.4] refers to “a valid operating range of the DDR DRAM component” rather than to “a valid operation range of the integrated circuit device.”

To account for limitation [20.4], Petitioner relies on its arguments for limitation [1.4.a] of claim 1. Pet. 71. The above-discussed deficiency of the Petition in accounting for limitation [1.4.a] applies equally to limitation [20.4]. We determine Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of claim 20 over Johnson and Jeddeloh.

10. Dependent Claims 21 and 22

Claims 21 and 22 each depend, directly or indirectly, from claim 20. Ex. 1001, 8:45–61. The above-discussed deficiency for claim 20 applies equally to claims 21 and 22. Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of claim 21 or claim 22 over Johnson and Jeddeloh.

11. Independent Claim 23

Claim 23 is a method claim and recites the following step:
“systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals transmitted via a PCB to determine a valid operating range of the DDR DRAM component.” Ex. 1001, 10:1–4. Petitioner has identified this step as limitation [23.4]. Pet. xiv. Limitation [23.4] is the same as limitation [1.4.a], except that limitation [23.4] refers to “a valid operating range of the DDR DRAM component” rather than to “a valid operation range of the integrated circuit device,” and limitation [23.4] modifies “signals” by specifying that they are “transmitted via a PCB [printed circuit board].” Ex. 1001, 10:1–4.

To account for limitation [23.4], Petitioner relies on its arguments for limitation [20.4] of claim 20 for which Petitioner, in turn, relies on its arguments for limitation [1.4.a]. Pet. 71, 73. The above-discussed deficiency of the Petition in accounting for limitation [1.4.a] applies equally to limitation [23.4]. We determine Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of claim 23 over Johnson and Jeddeloh.

*E. Alleged Obviousness of Claims 1–3, 7, 8, and 12
over Johnson and Keeth*

1. Overview of Keeth (Exhibit 1006)

Keeth is a U.S. Patent titled “Clock Vernier Adjustment.” Ex. 1006, code (54). Keeth describes its invention as providing a method and integrated circuit “including a vernier clock adjustment circuit receiving an input clock signal and providing a rising-edge clock signal representing the input clock signal delayed by a rising-edge delay and providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay.” Ex. 1006, 1:63–2:1. Keeth also describes: “An edge triggered circuit receives data and the rising-edge and falling-edge clock signals, and stores data at the rising-edge of the rising-edge clock signal and at the falling-edge of the falling-edge clock signal.” *Id.* at 2:1–4. Keeth additionally describes: “In one embodiment of the integrated circuit according to the present invention, the rising-edge and falling-edge [clock] delays are programmable delays.” *Id.* at 2:5–7.

Keeth explains:

The vernier clock adjustment circuitry and method according to the present invention more accurately and precisely compensates for the effects of duty cycle variation, bus position of a given memory device, timing drift, loading variations, clock jitter, clock skew, noise, overshoot, and ringing *by individually adjusting both the rising-edge and falling-edge [clock] timings, either independently or interdependently from each other.* As a result, data is accurately clocked in the memory devices even at higher data transmission rates.

Ex. 1006, 2:46–55 (emphasis added).

Figure 7 of Keeth is reproduced below:

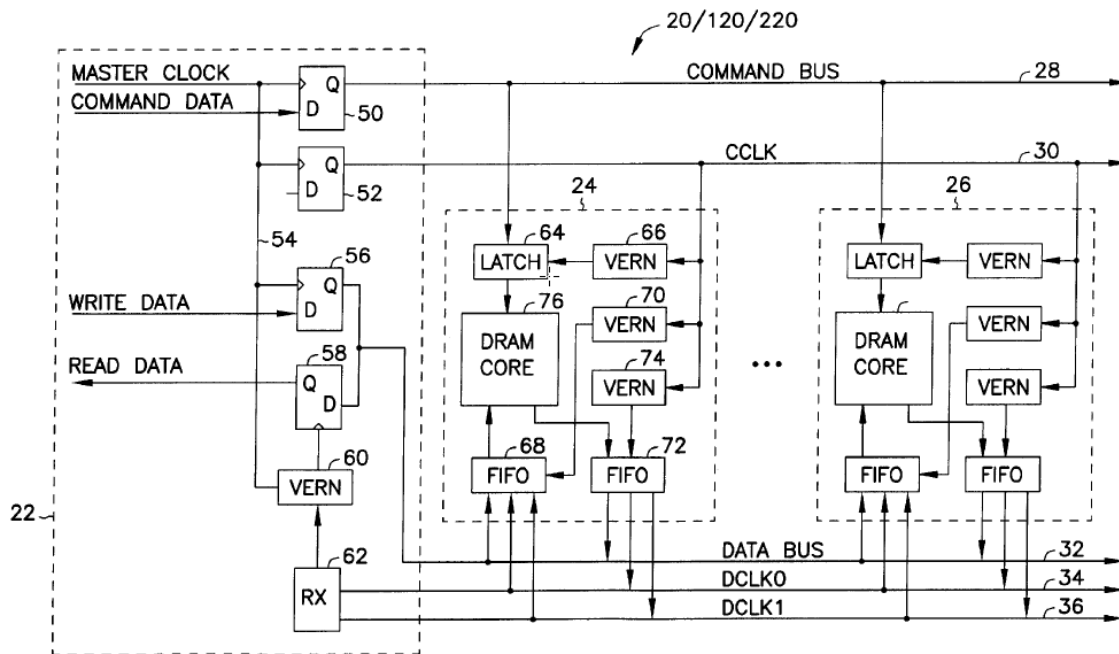


FIG. 7

Figure 7 is a block diagram of a memory system having vernier clock adjustment circuitry. Ex. 1006, 3:3–4.

Keeth explains:

As illustrated in FIG. 7, memory controller 22 includes a command register 50 for providing commands to command bus 28 and a CCLK register 52 for providing the CCLK to clock line 30. A master clock is provided on a line 54 to registers 50 and 52. A write data register 56 is also clocked by the master clock on line 54 and provides write data to data bus 32. A read data register 58 receives read data from data bus 32 and receives its clock from an optional vernier clock adjustment circuit 60. Vernier clock adjustment circuit 60 receives the master clock from line 54 and the active one of the data clocks DCLK0 or DCLK1 via a register multiplexer 62, which receives DCLK0 and DCLK1 from clock lines 34 and 36.

DRAM module 24 includes a command latch 64 which receives commands from command bus 28. Command latch 64 receives a delayed CCLK clock from a command vernier clock

adjustment circuit 66. Command vernier clock adjustment circuit 66 receives the CCLK signal from clock line 36. A write first-in, first-out (FIFO) buffer 68 receives the DCLK0 and DCLK1 clock signals from lines 34 and 36 and the write data from data bus 32 and provides write data to a DRAM core 76. Write FIFO buffer 68 receives a delayed CCLK clock from a write vernier clock adjustment circuit 70. Write vernier clock adjustment circuit 70 also receives the CCLK clock signal from clock line 36. A read FIFO buffer 72 receives read data from DRAM core 76 and provides the read data to data bus 32 along with the DCLK0 and DCLK1 clock signals to clock lines 34 and 36. Read FIFO buffer 72 receives a delayed CCLK clock from a read vernier clock adjustment circuit 74. Read vernier clock adjustment circuit 74 also receives the CCLK clock signal from clock line 30.

Ex. 1006, 6:57–7:22. Keeth further describes that when memory systems 20/120/220 power up, “the command timing, read timing, and write timing of each individual DRAM is adjusted by the memory controller 22/122/222 so that bursts of data on the data bus originating from different devices are properly spaced.” *Id.* at 7:24–28.

Keeth describes an example of the vernier clock adjustment operation as follows:

In this embodiment, memory controller 22 sends commands to the first DRAM module 24 and the command clock adjustment circuit 66 in DRAM module 24 is adjusted to optimally receive the command at command latch 64 from the command bus 28. Then memory controller 22 starts a write command sequence and the write vernier adjustment circuit 70 in DRAM module 24 is adjusted to permit optimal receiving of the write data at write FIFO buffer 68 from data bus 32. Next, a read command sequence is started by memory controller 22 and the read vernier clock adjustment circuit 74 is adjusted to permit optimal receiving of read data at read data register 58 from data bus 32.

Ex. 1006, 8:13–25.

2. *Independent Claim 1*

a. *Preamble recitation [1.P]*

For the preamble, Petitioner makes exactly the same arguments it does for the alleged ground of unpatentability based on Johnson and Jeddeloh. Pet. 73. Patent Owner expresses no view on Petitioner's accounting for the preamble. We need not make any determination here because, as we discuss below, Petitioner has not sufficiently accounted for limitation [1.4.a] and limitation [1.4.b].

b. *Limitation [1.1]*

Petitioner makes exactly the same arguments it does for the alleged ground of unpatentability based on Johnson and Jeddeloh. Pet. 73. We need not make any determination here because, as we discuss below, Petitioner has not sufficiently accounted for limitation [1.4.a] and limitation [1.4.b].

c. *Limitation [1.2]*

Petitioner makes exactly the same arguments it does for the alleged ground of unpatentability based on Johnson and Jeddeloh. Pet. 73. We need not make any determination here because, as we discuss below, Petitioner has not sufficiently accounted for limitation [1.4.a] and limitation [1.4.b].

d. *Limitation [1.3]*

Petitioner makes the same arguments it does for the alleged ground of unpatentability based on Johnson and Jeddeloh. Pet. 73. Patent Owner asserts that clock signals CCLK is not a sampling signal for data signal DQ. Prelim Resp. 24. For reasons discussed above in Section III.D.3.d, we agree with Patent Owner and find that Petitioner has not sufficiently shown that Johnson's CCLK signal is a sampling signal.

e. Limitation [1.4.a]

For the same reasons Petitioner asserts, in alleging obviousness of claim 1 over Johnson and Jeddeloh, that Johnson alone discloses or suggests limitation [1.4.a], Petitioner asserts here in alleging obviousness of claim 1 over Johnson and Keeth that Johnson alone discloses or suggests limitation [1.4.a]. Pet. 73. For the same reasons we rejected that contention in discussing alleged obviousness of claim 1 over Johnson and Jeddeloh, we reject that assertion here as well. *See* Section III.D.3.e.

Alternatively, Petitioner asserts that Johnson and Keeth together teach limitation [1.4.a]. Pet. 74–81. Petitioner explains:

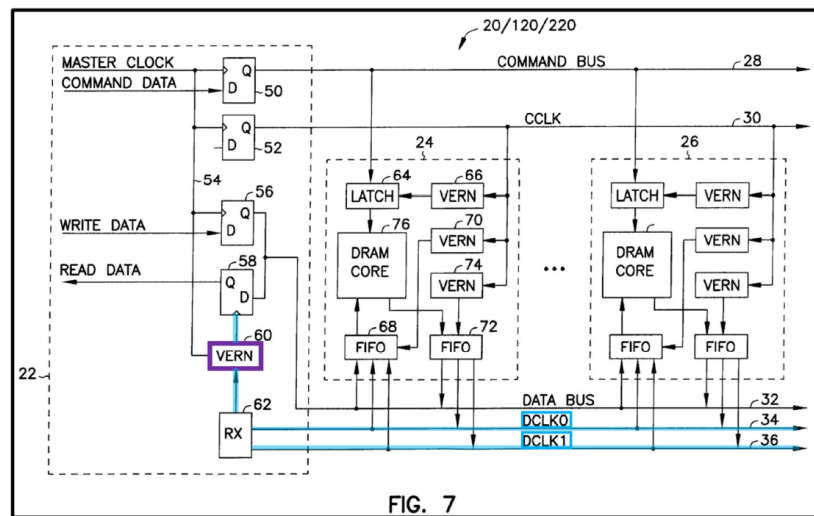
To the extent Patent Owner argues that *Johnson* does not explicitly disclose or render obvious the recited “systematically altering [] a phase shift of the sampling signals,” *Keeth* teaches this element. Ex-1002, ¶ 239. *Keeth* discloses a similar memory system, which includes a command bus 28 “for carrying address and control information from memory controller 22 to the DRAM modules,” and a bi-directional data bus 32 for “carrying write data from memory controller 22 to the DRAM modules and further carrying read data from the DRAM modules to memory controller 22.” Ex-1006, 3:44-56. A “free-running clock (CCLK) [is] provided on a clock line 30 from memory controller 22” (the recited “sampling signals”) and two bi-directional data clocks DCLK0 and DCLK1 (the recited “sampling signals”) “are respectively provided on clock line 34 and clock line 36.” *Id.*; Ex-1002, ¶241.

Pet. 74.

Petitioner also explains:

Keeth teaches that a Vernier clock adjustment circuit 60 is used to adjust the timing of DCLK0 or DCLK1 for a read operation. Ex-1002, ¶247. *Keeth* teaches that the “rising edge and falling edge transitions of the selected DCLK are employed to clock the input latches of the [] memory controller receiving data.” Ex-1006, 3:61-63. Vernier clock adjustment circuit 60 is

configured as shown in Figure 9 to produce a delayed version of the active DCLK used for rising edge clockings and a delayed version of the active DCLK used for falling edge clockings. *Id.*, 10:6-17; Ex-1002, ¶245, A POSITA would have recognized that delaying the active DCLK signals is “altering a phase shift of . . . the sampling signals.” Ex-1002, ¶248. Annotated Figure 7 below shows the vernier delays 60 (purple) that performs the altering and the sampling signals (blue).



[Figure 7 shows a memory system with vernier clock adjustment circuitry. Petitioner has framed vernier delay circuit 60 in purple and colored sampling signal lines blue.]

Ex-1006, 10; Ex-1002, ¶248.

Id. at 76–77.

Petitioner further explains:

Additionally, vernier clock adjustment circuits 70 and 74 are used in write and read operations, respectively, to adjust the timing of CCLK, which controls sampling of data signals at DRAM module 24. Ex-1002, ¶249. *Keeth* states that a “write first-in, first-out (FIFO) buffer 68 receives the DCLK0 and DCLK1 clock signals from lines 34 and 36 and the write data from data bus 32 and provides write data to a DRAM core 76.” Ex-1006, 7:9-12. During write operations, write FIFO buffer 68 samples data signals from data bus 32 before the data is written

to DRAM core 76. Ex-1006 at 7:10-12. Similarly, a “read FIFO buffer 72 receives read data from DRAM core 76 and provides the read data to data bus 32 along with the DCLK0 and DCLK1 clock signals to clock lines 34 and 36.” *Id.* at 7:15-18. The read FIFO buffer 72 “receives a delayed CCLK clock from a read vernier clock adjustment circuit 74,” which is used to clock read FIFO buffer 72. *Id.*, 7:20-22; 9:15-18. Because write FIFO buffer 68 and read FIFO buffer 72 are both clocked by CCLK, CCLK controls, at least in part, sampling of the data signals read from and written to DRAM core 76. *Id.* at 7:12-20. CCLK is therefore a “sampling signal.” Ex-1002, ¶249.

Vernier clock adjustment circuits 70 and 74 are configured to produce delayed versions of CCLK used to clock write FIFO buffer 68 and read FIFO buffer 72. Ex-1006, 10:6-17, Ex-1002, ¶251. The delayed versions of CCLK ensure proper timing of write FIFO buffer 68 and read FIFO buffer 72. *Id.* A POSITA would have recognized that delaying the CCLK signal is “altering a phase shift of . . . the sampling signals.” *Id.*

Id. at 77–78.

Petitioner then explains that Keeth describes its memory system adjusts the vernier delays by running through all delay steps of the vernier circuit and determining when data misses on low adjustments and on high adjustments, and then setting the vernier adjustment in an approximated optimal middle setting. Pet. 79 (citing Ex. 1006, 7:66–8:5). Petitioner further notes that Keeth describes an alternative where its memory system includes a feedback controller used to set the vernier settings by first selecting an estimated optimal setting and allowing the controller and feedback circuitry to arrive at the optimal delay setting for the vernier clock adjustment circuit. *Id.* (citing Ex. 1006, 8:5–9).

According to Petitioner, “[a] POSITA would have recognized the advantages of modifying *Johnson* to systematically alter a phase shift of sampling signals, as taught by *Keeth*.” Pet. 80. Petitioner asserts:

A POSITA would have been motivated to make such a modification at least to improve synchronization of data signals and sampling signals when both writing to and reading from DRAM banks. Ex-1002, ¶255. *Johnson* shows that CCLK passes through a delay lock loop 41. Ex-1004, 4; Ex-1002, ¶[133]. To the extent that *Johnson* does not explicitly explain how CCLK is synchronized to the data signals received from the DRAM banks, a POSITA would have had reason to look to Keeth for specificity as to how to synchronize data signals received from the DRAM banks to the sampling signals used to latch them. Ex-[1002], ¶254.

Id.

This “looking to Keeth for more specificity” argument is unavailing because, as discussed above, we find that Johnson’s CCLK signal is not a sampling signal. Also, for reasons discussed above in the context of Petitioner’s reliance on Johnson alone, adjusting the phase of DCLK to synchronize with data signals on the data bus DQ is redundant and makes little sense, because Johnson already discloses adjusting the phase of data signals to synchronize with DCLK. We are not sufficiently persuaded that synchronizing DCLK to data signals as Keeth teaches, if adopted in Johnson, would improve synchronization, given that in Johnson data signals are already synchronized to DCLK.

In any event, even assuming that Johnson’s CCLK is a sampling signal, that Johnson does disclose the idea of adjusting the phase of sampling signals, and that one of ordinary skill in the art would have looked to Keeth with regard to more detail on adjusting the phase of CCLK and DCLK, Petitioner’s showing still is deficient for institution purposes. The resulting combination as articulated by Petitioner does not cure the deficiency discussed above for Johnson alone. Petitioner still nowhere identifies or explains the determination of a valid operation range that is a three-

dimensional range including a boundary for each of three underlying parameters which, for example, may be the phases of the command signals, the data signals, and the sampling signals. Nowhere has Petitioner identified or explained how Johnson discloses a valid operation range that is a function of three parameters together, e.g., the respective phases of command signals, data signals, *and* sampling signals.

As Patent Owner correctly notes, Johnson at best determines two 2-parameter ranges, not a single 3-parameter range. Prelim. Resp. 29. This remains true notwithstanding the addition of Keeth in combination with Johnson.

f. Limitation [1.4.b]

Limitation [1.4.b] recites: “wherein the valid operation range includes an optimal operation point for the integrated circuit device.” Ex. 1001, 7:2–4.

Because Petitioner has not sufficiently met the “valid operation range” recitation of limitation [1.4.a], Petitioner equally has not sufficiently met the further requirement of an “optimal condition” included within the “valid operation range” as recited in limitation [1.4.b] for the integrated circuit device.

g. Conclusion for Claim 1

For the foregoing reasons, Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of claim 1 over Johnson and Keeth.

3. Dependent Claims 2 and 3

Claims 2 and 3 each depend, directly or indirectly, from claim 1. Ex. 1001, 7:5–17. The above-discussed deficiency for claim 1 applies

equally to claims 2 and 3. Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of any of claims 2 and 3 as obvious over Johnson and Keeth.

4. *Independent Claim 7*

Claim 7 is an apparatus claim and includes a delay calibrator within a controller. Ex. 1001, 7:18–34. Claim 7 recites that the delay calibrator is “further configured to systematically alter a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device.” *Id.* at 7:27–32. Petitioner has identified this requirement of the claimed delay calibrator as limitation [7.3.a]. Pet. x. Limitation [7.3.a] corresponds to the step according to limitation [1.4.a] of claim 1.

To account for limitation [7.3.a], Petitioner relies on its arguments for limitation [1.4.a] of claim 1. Pet. 84 (citing Ex. 1002 ¶ 274). The above-discussed deficiency of the Petition in accounting for limitation [1.4.a] applies equally to limitation [7.3.a].

Limitation [7.3.b] recites “wherein the valid operation range includes an optimal operation point for the integrated circuit device.” Pet. x. Because Petitioner has not sufficiently met the “valid operation range” recitation of limitation [7.3.a], Petitioner equally has not sufficiently met the further requirement of an “optimal condition” included within the “valid operation range” as recited in limitation [7.3.b] for the integrated circuit device.

We determine Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of claim 7 over Johnson and Keeth.

5. *Dependent Claim 8*

Claim 8 depends from claim 7. Ex. 1001, 7:35–36. The above-discussed deficiency for claim 7 applies equally to claim 8. Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of claims 8 as obvious over Johnson and Keeth.

6. *Independent Claim 12*

Claim 12 is a method claim and recites the following step: “systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operating range of the DRAM component.” Ex. 1001, 7:57–60. Petitioner has identified this step as limitation [12.4]. Pet. xi. Limitation [12.4] is the same as limitation [1.4.a], except that limitation [12.4] refers to “a valid operating range of the DRAM component” rather than to “a valid operation range of the integrated circuit device.”

To account for limitation [12.4], Petitioner relies on its arguments for limitation [1.4.a] of claim 1. Pet. 85. The above-discussed deficiency of the Petition in accounting for limitation [1.4.a] applies equally to limitation [12.4]. We determine Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of claim 12 over Johnson and Keeth.

F. *Alleged Obviousness of Claims 4–6, 9–11, and 13–19 over Johnson, Jeddeloh, and Keeth*

Claims 4–6 each depend, directly or indirectly, from claim 1. Claims 9–11 each depend, directly or indirectly, from claim 7. Claims 13–19 each depend, directly or indirectly, from claim 12. For these dependent claims, Petitioner relies on the assertions it has made against independent claims 1, 7, and 12, based on the combined teachings of Johnson and Keeth, and then

the teachings of Jeddeloh to account for the further features added by these dependent claims. Pet. 85.

As already discussed above, Petitioner has not sufficiently shown that Johnson and Keeth disclose or would have suggested the subject matter of independent claims 1, 7, and 12. That deficiency is not cured by the addition of Jeddeloh as proposed by Petitioner to account for the further features of the dependent claims.

Accordingly, Petitioner has not shown a reasonable likelihood that it would prevail in establishing obviousness of any of claims 4–6, 9–11, and 13–19 over Johnson, Jeddeloh, and Keeth.

G. Discretionary Denial Under 35 U.S.C. § 325(d)

Patent Owner contends that we should exercise discretion to deny institution under 35 U.S.C. § 325(d) “because the prior art and arguments presented in the Petition are substantially the same as those previously considered by the USPTO during prosecution.” Prelim. Resp. 40.

We have discretion to deny institution under 35 U.S.C. § 325(d) based on the framework set forth in *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (precedential). However, we need not reach the issue of discretionary denial under 35 U.S.C. § 325(d), because we have determined, as explained above, that Petitioner has not shown a reasonable likelihood that it would prevail in establishing unpatentability of any challenged claim under any asserted ground.

IV. CONCLUSION

For the foregoing reasons, we conclude that Petitioner has not shown a reasonable likelihood that it would prevail in establishing that at least one of claims 1–23 of the '835 patent is unpatentable.

V. ORDER

It is ORDERED that no *inter partes* review is instituted in this proceeding.

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