PTO/SB/80 (11-08)
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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☑ Practitioners associated with the Customer Number: 78408

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☑ The address associated with Customer Number: 78408

OR

☐ Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address:

Rambus Inc.
1050 Enterprise Way, Suite 700
Sunnyvale, CA 94089

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	3/22/11
Name	Wayne Sobon, Esq.	Telephone	408 462-8000
Title	Vice-President, Corporate Counsel, Rambus Inc.		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Rambus Inc.

Application No./Patent No.: unknown (con of 14/449610) Filed/Issue Date: Herewith (April 12, 2017)

Titled: Memory Controller For Micro-Threaded Memory Operations

Rambus Inc., a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 016044, Frame 0118, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

   2. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Marc Schuyler/	2017-04-12
Signature	Date
Marc Schuyler	35675
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Attorney Docket No.: <RA378.C3.US>

DECLARATION (37 CFR 1.63) FOR PROVISIONAL, UTILITY, DESIGN, OR NATIONAL STAGE OF PCT APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention: **MICRO-THREADED MEMORY**

As a below named inventor, I hereby declare that:

This declaration is directed to:

_____ The attached application, or

_____ United States Provisional Application Number **[Enter App #]** filed on **[Enter Date]**, or

__X__ United States Application Number **13/901,014**, filed on **May 23, 2013**.

The above-identified application was made or authorized to be made by me.

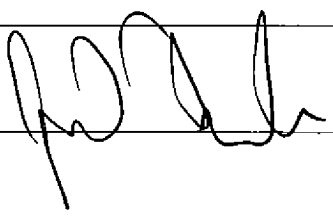
I have authorized and/or hereby do authorize my assignee to file patent applications claiming priority from the application referenced above, including provisional, non-provisional, design, divisional, continuation, continued prosecution, continuation-in-part, substitute, supplemental examination application, and other applications related to the subject matter of the application referenced above. I have authorized and/or hereby do authorize my assignee to make changes to the application for matters of formality.

I believe I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under Section 1001 of Title 18 of the United States Code by fine or imprisonment of not more than five (5) years, or both.

Warning: Declarant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent.

Legal Name of Inventor:

Inventor: **Frederick A. Ware**	Date: 5/31/13
Signature: 	

Attorney Docket No.: <RA378.C3.US>

DECLARATION (37 CFR 1.63) FOR PROVISIONAL, UTILITY, DESIGN, OR NATIONAL STAGE OF PCT APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention: **MICRO-THREADED MEMORY**

As a below named inventor, I hereby declare that:

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Legal Name of Inventor:

Inventor: **Craig E. Hampel**	Date: Jun 12, 2013
Signature: Craig E Hampel	

Attorney Docket No.: <RA378.C3.US>

DECLARATION (37 CFR 1.63) FOR PROVISIONAL, UTILITY, DESIGN, OR NATIONAL STAGE OF PCT APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention: **MICRO-THREADED MEMORY**

As a below named inventor, I hereby declare that:

This declaration is directed to:

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_____ United States Provisional Application Number **[Enter App #]** filed on **[Enter Date]**, or

__X__ United States Application Number **13/901,014**, filed on **May 23, 2013**.

The above-identified application was made or authorized to be made by me.

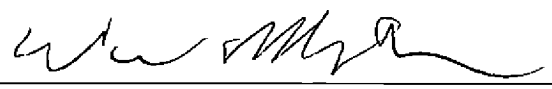
I have authorized and/or hereby do authorize my assignee to file patent applications claiming priority from the application referenced above, including provisional, non-provisional, design, divisional, continuation, continued prosecution, continuation-in-part, substitute, supplemental examination application, and other applications related to the subject matter of the application referenced above. I have authorized and/or hereby do authorize my assignee to make changes to the application for matters of formality.

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Warning: Declarant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent.

Legal Name of Inventor:

Inventor: **Wayne S. Richardson**	Date: 4 June 2013
Signature: 	

Attorney Docket No.: <RA378.C3.US>

DECLARATION (37 CFR 1.63) FOR PROVISIONAL, UTILITY, DESIGN, OR NATIONAL STAGE OF PCT APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention: **MICRO-THREADED MEMORY**

As a below named inventor, I hereby declare that:

This declaration is directed to:

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____ United States Provisional Application Number **[Enter App #]** filed on **[Enter Date]**, or

__X__ United States Application Number **13/901,014**, filed on **May 23, 2013.**

The above-identified application was made or authorized to be made by me.

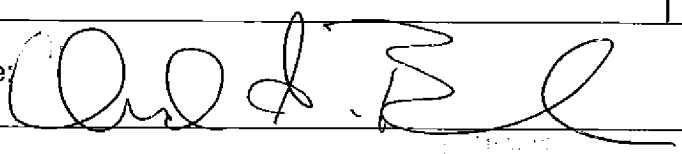
I have authorized and/or hereby do authorize my assignee to file patent applications claiming priority from the application referenced above, including provisional, non-provisional, design, divisional, continuation, continued prosecution, continuation-in-part, substitute, supplemental examination application, and other applications related to the subject matter of the application referenced above. I have authorized and/or hereby do authorize my assignee to make changes to the application for matters of formality.

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Warning: Declarant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent.

Legal Name of Inventor:

Inventor: **Chad A. Bellows**	Date: 6-5-13
Signature: 	

Attorney Docket No.: <RA378.C3.US>

DECLARATION (37 CFR 1.63) FOR PROVISIONAL, UTILITY, DESIGN, OR NATIONAL STAGE OF PCT APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention: **MICRO-THREADED MEMORY**

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This declaration is directed to:

____ The attached application, or

____ United States Provisional Application Number **[Enter App #]** filed on **[Enter Date]**, or

__X__ United States Application Number **13/901,014**, filed on **May 23, 2013**.

The above-identified application was made or authorized to be made by me.

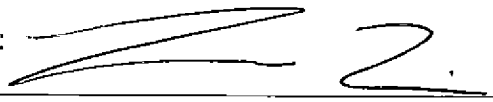
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Warning: Declarant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent.

Legal Name of Inventor:

Inventor: **Lawrence Lai**	Date: 6/12/13
Signature: 	

Electronic Acknowledgement Receipt

EFS ID:	28910449
Application Number:	15486068
International Application Number:	
Confirmation Number:	2908
Title of Invention:	Memory Controller For Micro-Threaded Memory Operations
First Named Inventor/Applicant Name:	Frederick A. Ware
Customer Number:	78408
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	2016091 / RA378C3C1C1US
Receipt Date:	12-APR-2017
Filing Date:	
Time Stamp:	17:34:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	1-aia0014-ADS-RA378C3C1C1US.pdf	1400738 949b327221da3286a0fa9c69d3ed09e4a5d82c25	no	7

Warnings:

Information:					
2		2-Application-as-filed-RA378C3C1C1US.pdf	362260 341071623c81dc003ba52b74b0e4e0e2118fc07b	yes	48
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	46	
	Claims		47	47	
	Abstract		48	48	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	3-Drawings-RA378C3C1C1US.pdf	764837 a7b5827c90aa8a6dbd1d1358760a173fb06d6f8c	no	25
Warnings:					
Information:					
4	Power of Attorney	4-2011-07-22-Rambus-General-POA-Customer-No-78408.pdf	369569 c41e0c2b4c551970e1e8517c946c243151de941f	no	1
Warnings:					
Information:					
5	Assignee showing of ownership per 37 CFR 3.73	5-aia0096-AssnStatement-RA378C3C1C1US.pdf	118186 fba47f48231495366a4abc430928981e25f787bc	no	3
Warnings:					
Information:					
6	Oath or Declaration filed	6-RA378C3Declaration.pdf	135072 b60e218dd9a7c154fd9aadeeff376c12f081dd46	no	5
Warnings:					
Information:					
		Total Files Size (in bytes):	3150662		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/14 (08-12)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	2016091 / RA378C3C1C1US
	Application Number	
Title of Invention	Memory Controller For Micro-Threaded Memory Operations	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Frederick	A.	Ware	

Residence Information (Select One) ● US Residency ○ Non US Residency ○ Active US Military Service

City	State/Province	Country of Residence
Los Altos Hills	CA	US

Mailing Address of Inventor:

Address 1	1050 Enterprise Way, Suite 700
Address 2	

City	State/Province	Postal Code	Country
Sunnyvale	CA	94089	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Craig	E.	Hampel	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	State/Province	Country of Residence
Los Altos	CA	US

Mailing Address of Inventor:

Address 1	1050 Enterprise Way, Suite 700
Address 2	

City	State/Province	Postal Code	Country
Sunnyvale	CA	94089	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Wayne	S.	Richardson	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	2016091 / RA378C3C1C1US
	Application Number	
Title of Invention	Memory Controller For Micro-Threaded Memory Operations	

City	Saratoga	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	1050 Enterprise Way, Suite 700		
Address 2			
City	Sunnyvale	State/Province	CA
Postal Code	94089	Country	US

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Chad	A.	Bellows	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Birmingham	State/Province	MI	Country of Residence	US

Mailing Address of Inventor:

Address 1	342 Henley Street		
Address 2			
City	Birmingham	State/Province	MI
Postal Code	48167	Country	US

Inventor 5 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Lawrence		Lai	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	San Jose	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	1050 Enterprise Way, Suite 700		
Address 2			
City	San Jose	State/Province	CA
Postal Code	94089	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	2016091 / RA378C3C1C1US
	Application Number	
Title of Invention	Memory Controller For Micro-Threaded Memory Operations	

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Application Information:

Title of the Invention	Memory Controller For Micro-Threaded Memory Operations		
Attorney Docket Number	2016091 / RA378C3C1C1US	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	25	**Suggested Figure for Publication (if any)**	8

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

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Prior Application Status	Pending			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	
	Continuation of	14/449610	2014-08-01	
Prior Application Status	Patented			Remove

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Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14/449610	Continuation of	13/901014	2013-05-23	9292223	2016-03-22

Prior Application Status: Patented — Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/901014	Continuation of	10998402	2004-11-29	8595459	2013-11-26

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Organization Name	Rambus Inc.		
Mailing Address Information:			
Address 1	1050 Enterprise Way, Suite 700		
Address 2			
City	Sunnyvale	**State/Province**	CA
Country	US	Postal Code	94089
Phone Number		Fax Number	
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Signature	/Marc Schuyler/			Date (YYYY-MM-DD)	2017-04-12
First Name	Marc	Last Name	Schuyler	Registration Number	35675

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Memory Controller For Micro-Threaded Memory Operations

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of US Patent Application No. 14/449,610, filed on August 1, 2014 for "Micro-Threaded Memory" on behalf of inventors Frederick A. Ware, Craig E. Hampel, Wayne S. Richardson, Chad A. Bellows and Lawrence Lai, which in turn is a continuation of US Patent Application No. 13/901,014, filed on May 23, 2013 for "Micro-Threaded Memory" on behalf of inventors Frederick A. Ware, Craig E. Hampel, Wayne S. Richardson, Chad A. Bellows and Lawrence Lai (now US Patent No. 9,292,223), which in turn is a continuation of US Patent Application No. 10/998,402, filed on November 29, 2004 for "Micro-Threaded Memory" on behalf of inventors Frederick A. Ware, Craig E. Hampel, Wayne S. Richardson, Chad A. Bellows and Lawrence Lai (now US Patent No. 8,595,459). Each aforementioned patent and/or application is hereby incorporated by reference.

FIELD OF THE INVENTION

[0002] The present invention relates generally to memory systems and components thereof.

BACKGROUND

[0003] Although dynamic random access memory (DRAM) remains the memory of choice for a broad class of computing and consumer electronics applications, DRAM core access times have not scaled with memory bandwidth demand. For example, the minimum time between activation of different storage rows in the same storage bank, t_{RC}, remains in the neighborhood of 40 nanoseconds for predominant core technologies; a substantial access time penalty for processors operating at gigahertz frequencies. Other core access times such as the minimum time between activation of rows in different banks of a multi-bank array, t_{RR}, and minimum time between column access operations (i.e., read or write operations at a specified column address) in the same row, t_{CC}, have also been slow to improve.

[0004] Designers have countered core timing limitations through a number of architectural and system-level developments directed at increasing the number of column access operations per row

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activation (e.g., paging, multi-bank arrays, prefetch operation), and maximizing the amount of data transferred in each column access. In particular, signaling rate advances have enabled progressively larger amounts of data to be transferred per column access, thereby increasing peak memory bandwidth. However, as signaling rates progress deeper into the gigahertz range and the corresponding core access times remain relatively constant, column transaction granularity, the amount of data transferred per column access, is forced to scale upwards and is approaching limits imposed by signal paths within the DRAM itself. Further, the trend in some classes of data processing applications, graphics applications for example, is toward smaller data objects (e.g., triangle fragments of a 3D scene) that are often stored in dispersed memory locations. In such applications, the additional power and resources expended to increase the column transaction granularity may provide only limited increase in effective memory bandwidth as much of the fetched data may not be used.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

[0006] Figure 1 illustrates partitioning of a data transfer interval and data transfer path to enable reduced column transaction granularity;

[0007] Figure 2 illustrates an embodiment of a memory device in which micro-threaded column operations may be performed;

[0008] Figure 3 illustrates more detailed embodiments of sub-banks, column decoders, and data interfaces that may be used within the memory device of Figure 2;

[0009] Figure 4 illustrates a single-threaded mode of operation within the memory device 100 of Figure 2;

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[0010] Figure 5 illustrates an embodiment of a request interface that may be used within the memory device of Figure 2 to enable single-threaded and micro-threaded memory transactions;

[0011] Figure 6 illustrates an exemplary timing of row and column strobe signal assertions by the request decoder of Figure 5 when the memory device of Figure 2 is operating in a single-threaded mode;

[0012] Figures 7 and 8 illustrate a memory device and an exemplary sequence of micro-threaded memory transactions that may be performed in the memory device when operated in a micro-threaded mode;

[0013] Figure 9 illustrates an exemplary timing of register strobe signal assertions by the request decoder of Figure 5;

[0014] Figure 10 illustrates exemplary link-staggered micro-threaded memory transactions that may be performed in an alternative embodiment of the memory device of Figure 2;

[0015] Figure 11 illustrates an alternative link-staggered data transfer mode that may be used in other memory device embodiments;

[0016] Figures 12A and 12B illustrate exemplary data path interfaces and that may be used to support the time-staggered and link staggered data transfers shown in Figures 8 and 10;

[0017] Figures 13 and 14 illustrate a memory device and an exemplary sequence of micro-threaded memory transactions that may be performed in the memory device when operated in an alternative micro-threaded mode;

[0018] Figure 15 illustrates an embodiment of a request interface that may be used within the memory device 100 of Figure 2 to enable the micro-threaded memory transactions described in reference to Figures 13 and 14;

[0019] Figures 16 and 17 illustrate a memory device and an exemplary sequence of micro-threaded memory operations in which separate row and column addresses are used to access sub-banks in each of four storage bank quadrants of the memory device within a single t_{CC} interval;

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[0020] Figure 18 illustrates an embodiment of a request interface that may be included within the memory device of Figure 16;

[0021] Figure 19 illustrates an exemplary timing of control signal assertions by the request decoder of Figure 18;

[0022] Figures 20A and 20B illustrate exemplary row request formats;

[0023] Figures 21A and 21B illustrate exemplary column request formats;

[0024] Figures 22 and 23 illustrate a memory device having a request interface and data path interface to interface with legacy request and data paths, and an exemplary sequence of micro-threaded memory operations in the memory device;

[0025] Figure 24 illustrates a more detailed example of address information provided via the request path shown in Figure 23;

[0026] Figure 25 illustrates exemplary configuration information that may be provided in conjunction with a load mode register command issued to the memory device of Figure 22;

[0027] Figures 26 and 27 illustrate a memory device having the data path interface described in reference to Figures 22 and 23, and an exemplary sequence of four-by-four micro-threaded memory operations in the memory device;

[0028] Figure 28 illustrates an exemplary timing signal arrangement that may be used to convey a fourth bank address bit to the memory device of Figure 26; and

[0029] Figure 29 illustrates an embodiment of a memory system that includes a memory controller and at least one micro-threaded memory device.

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DETAILED DESCRIPTION

[0030] In the following description and in the accompanying drawings, specific terminology and drawing symbols are set forth to provide a thorough understanding of the present invention. In some instances, the terminology and symbols may imply specific details that are not required to practice the invention. For example, the interconnection between circuit elements or circuit blocks may be shown or described as multi-conductor or single-conductor signal lines. Each of the multi-conductor signal lines may alternatively be single-conductor signal lines, and each of the single-conductor signal lines may alternatively be multi-conductor signal lines. Signals and signaling paths shown or described as being single-ended may also be differential, and vice-versa. Similarly, signals described or depicted as having active-high or active-low logic levels may have opposite logic levels in alternative embodiments. As another example, circuits described or depicted as including metal oxide semiconductor (MOS) transistors may alternatively be implemented using bipolar technology or any other technology in which a signal-controlled current flow may be achieved. With respect to terminology, a signal is said to be "asserted" when the signal is driven to a low or high logic state (or charged to a high logic state or discharged to a low logic state) to indicate a particular condition. Conversely, a signal is said to be "deasserted" to indicate that the signal is driven (or charged or discharged) to a state other than the asserted state (including a high or low logic state, or the floating state that may occur when the signal driving circuit is transitioned to a high impedance condition, such as an open drain or open collector condition). Multi-level signaling in which each transmitted symbol conveys more than one bit of information (i.e., bit rate is greater than baud rate) may also be used. A signal driving circuit is said to "output" a signal to a signal receiving circuit when the signal driving circuit asserts (or deasserts, if explicitly stated or indicated by context) the signal on a signal line coupled between the signal driving and signal receiving circuits. A signal line is said to be "activated" when a signal is asserted on the signal line, and "deactivated" when the signal is deasserted. Additionally, the prefix symbol "/" attached to signal names indicates that the signal is an active low signal (i.e., the asserted state is a logic low state). A line over a signal name (e.g., '$\overline{<\text{signal name}>}$') is also used to indicate an active low signal. The term "terminal" is used to mean a point of electrical connection. The term "exemplary" is used to express an example, not a preference or requirement.

[0031] In embodiments described herein, the data transfer capacity of a dynamic random access memory (DRAM) device over a given t_{CC} interval, a metric referred to herein as a t_{CC} envelope, is

subdivided and allocated to multiple column access transactions, thereby reducing the amount of data transferred in any one transaction, yet maintaining the peak memory bandwidth of the DRAM device. Referring to Figure 1, for example, instead of following a conventional, single-threaded approach of dedicating each t_{CC} envelope to a single column access transaction as shown at 90, the t_{CC} envelope is partitioned to enable transfer of multiple smaller sets of data in response to multiple micro-threaded column requests as shown at 92. By reducing the column transaction granularity in this manner, the effective bandwidth of the DRAM may be substantially increased over the single-threaded approach as multiple data objects of interest may be specifically addressed in different micro-threaded column access transactions and returned within a given t_{CC} interval, rather than merely a single data object and its potentially superfluous neighboring data.

[0032] In one embodiment, the t_{CC} envelope is partitioned temporally into a set of partial t_{CC} intervals (t_{CCp}) that are allocated respective micro-threaded column transactions. In another embodiment, the t_{CC} envelope is spatially partitioned, with data path resources between the memory device core and a host device (e.g., a memory controller) being subdivided and allocated to different micro-threaded column transactions. Referring again to Figure 1, for example, the data links, DQ, that form an external data path between a memory device and memory controller may be partitioned into two or more subsets of data links, DQ_p, that are allocated to different micro-threaded column access transactions. In other embodiments, both temporal and spatial partitioning is applied to further reduce the column transaction granularity. In Figure 1, for example, the t_{CC} envelope is partitioned temporally into two partial t_{CC} intervals, t_{CCp}, and spatially into two subsets of data links, DQp, thereby reducing the micro-threaded column transaction granularity to one-fourth of the single-threaded column transaction granularity. The t_{CC} envelope may be subdivided into more or fewer spatial and/or temporal partitions in other embodiments. Also, the multiple micro-threaded column access requests serviced in a partitioned t_{CC} interval may be directed to an open page of the same storage bank, to open pages of different storage banks, or any combination thereof. Also, in one embodiment, more densely pipelined row operations are used to enable sub-banks within a partitioned bank architecture to be separately addressed, in effect, increasing the number of banks within the memory device and enabling each of multiple micro-threaded column accesses, serviced within the same t_{CC} interval, to be directed to an independently selected bank, row and column.

Overview of an Exemplary Micro-Threaded Memory Architecture

[0033] Figure 2 illustrates an embodiment of a memory device 100 in which various types of micro-threaded column operations may be performed. The memory device 100 is assumed, for purposes of description, to be a DRAM device, but may alternately be any type of memory device having multiple storage arrays that share addressing and/or data path resources in a manner that imposes timing constraints on sequential accesses directed to the different storage arrays. Thus, t_{CC} constraints and t_{RR} constraints herein may alternatively be other types of memory access constraints that, together with signaling path bandwidth, define corresponding data transfer envelopes. For example, the t_{CC} envelope partitioning described herein is intended as an instance of more general partitioning of any data transfer envelope defined by an resource-imposed time constraint and signaling path bandwidth. Also, with regard to the timing constraint itself, such constraint may be defined to be a minimum time necessary to avoid resource conflicts within the memory device (e.g., to ensure proper operation), plus an optional tolerance time to account for statistical variation in the time required for circuits and/or signal paths to reach a desired state. A timing constraint may also be enforced or otherwise defined by a timing signal such as a clock signal or strobe signal and thus may be expressed as minimum number of transitions of such timing signal that are to transpire between back-to-back operations in order to avoid resource conflicts within the memory device.

[0034] In the particular example shown, the memory device 100 includes a request interface 101, column decoders 103_0-103_3, row decoders 113_0-113_3, data path interfaces 105A and 105B and eight storage banks, B0-B7. Each storage bank, B0-B7, is formed by a pair of A and B sub-banks (e.g., sub-banks B0-A and B0-B constitute bank B0, sub-banks B1-A and B1-B constitute bank B1, and so forth), with the sub-banks themselves being organized in four groups of four sub-banks each, referred to herein as quadrants. The four quadrants are designated Q0-Q3 in Figure 2. In the embodiment of Figure 2, sub-banks in the same quadrant share a row decoder and column decoder, and are all either A or B sub-banks from either the even bank set or odd bank set. For example, quadrant Q0 includes even-numbered, group A sub-banks (i.e., B0-A, B2-A, B4-A and B6-A) coupled to column decoder 103_0 via respective column paths (collectively designated 117_0) and to row decoder 113_0 via respective sets of word lines (collectively designated 115_0). In the remaining quadrants, Q1 includes odd-numbered, group A sub-banks coupled to column decoder 103_1 via column paths 117_1 and to row decoder 113_1 via word lines 115_1; Q2 includes even-numbered, group B sub-banks coupled column decoder 103_2 via

column paths 117_2 and to row decoder 113_2 via word lines 115_2; and Q3 includes odd-numbered, group B sub-banks coupled column decoder 103_3 via column paths 117_3 and to row decoder 113_3 via word lines 115_3. While the architecture of memory device 100 is carried forward in descriptions of various memory device embodiments described herein, in all cases such memory devices may have any number of banks, any number of sub-banks per bank, and any number of sub-banks per decoder-sharing group.

[0035] When operated as part of a memory system, the request interface 101 of memory device 100 receives a stream of requests (or commands or instructions) from a memory controller or other host device via a request path (not shown), and issues corresponding control and address signals to the row decoders 113 and column decoders 103 to carry out the requested operations. As a matter of terminology, the term "request" is used herein to mean a request, command or instruction issued to the memory device 100 to cause the memory device to take an action specified in the request or by the context in which the request is received. The action taken by the memory device in response to a given request is referred to as an operation, examples of which include row activation operations, column access operations (which may be read or write accesses) and precharge operations. A request and its corresponding operation are referred to collectively herein as a transaction. Also, some transactions may include multiple component requests and operations. In the case of a DRAM device, for example, a complete data access transaction may be specified by a row-activation request, one or more column access requests and a precharge request. A row activation request is directed to a bank and row of the memory device 100 (e.g., specified by bank and row addresses included with the request) and is serviced by enabling the contents of the row to be output onto the bit lines of the bank and thereby transferred into a page buffer (e.g., a storage structure formed by latching sense amplifiers coupled respectively to the bit lines). Column access requests are directed to a bank and column of the memory device 100 (e.g., specified by bank and column addresses included with the request) and are serviced by reading or overwriting data in column-address-specified sub-fields (columns) within the page buffer for the specified bank. After the column accesses directed to an open page (i.e., page buffer content) are completed, a precharge operation may be carried out to precharge the bit lines of the subject bank in preparation for subsequent row activation.

[0036] When a row activation request is received, the request interface 101 recovers bank and row address values from the request and forwards the address values via signal paths 111_1-111_3 to the row decoders 113_0-113_3 for the bank-address-specified quadrants. In one embodiment, each of the row

decoders 113 includes a first stage decoder to select the set of word lines coupled to a bank-address-specified sub-bank, and a second stage decoder to activate a row-address-specified word line within the selected set of word lines, thereby enabling the contents of the cells coupled to the activated word line onto the bit lines of the selected sub-bank. In other embodiments, the bank and row decoding operation may be carried out in more or fewer decoder stages. Also, one or more row address strobe signals may be issued by the request interface 101 or other control logic to control the timing of the word line activation.

[0037] When a column access request is received in the memory device 100, the request interface 101 recovers bank and column address values from the request and forwards the address values to the column decoders 103 for the quadrants specified by the bank address. In one embodiment, each of the column decoders 103 includes a bank multiplexer to enable access to the page buffer for a bank-address indicated sub-bank (i.e., via a selected one of column access paths 117), and a column multiplexer to select a column of page buffer storage elements for read or write access. Other circuit arrangements may be used resolve the column access location in alternative embodiments. Also, one or more column address strobe signals may be issued by the request interface 101 or other control logic in the memory device 100 to control the timing of the column access.

[0038] After column operations in the open page are completed (e.g., read or write operations carried out in response to corresponding column access requests), a precharge request and associated bank address may be received in the request interface 101 and serviced by deactivating a previously activated word line and precharging the bit lines for the specified bank. After the precharge operation is complete, the specified bank is in condition for another row activation operation.

[0039] Still referring to Figure 2, each of the data path interfaces 105A, 105B is coupled to respective pairs of column decoders 103 via column data paths 119 to enable transfer of read and write data between the column decoders and an external data path (not shown). More specifically, data path interface 105A enables data transfer between a first portion of the external data path and selected sense amplifiers within a page buffer (i.e., selected by column decoder 103_0 and 103_1) via column data paths 119_0 and 119_1, and data path interface 105B enables data transfer between a second portion of the external data path and selected sense amplifiers within a page buffer (i.e., selected by column decoders 103_2 and 103_3) via column data paths 119_2 and 119_3.

[0040] Figure 3 illustrates more detailed embodiments of the Q0 and Q1 sub-banks (i.e., sub-banks B0-A through B7-A), column decoders 103_0/103_1, and data interface 105A that may be used within the memory device 100 of Figure 2. The Q2 and Q3 sub-banks, column decoders 103_2/103_3 and data interface 105B may be implemented in embodiments similar or identical to those depicted in Figure 3 and therefore are not separately described.

[0041] In the embodiment of Figure 3, each of the sub-banks B0-A to B7-A includes a storage array 145 and page buffer 147 coupled to one another via bit lines 169. Referring to detail view 165, the storage array 145 is formed by memory cells 170 arranged in rows and columns. Each column of memory cells 170 is coupled via a bit line 169 to a respective sense amplifier 168 within page buffer 147, and each row of memory cells is coupled via a word line 166 to a row decoder 113 (or component thereof). In the particular embodiment shown, each memory cell 170 is a DRAM memory cell formed by a transistor switch (e.g., having a drain coupled to bit line 169 and a gate coupled to word line 166) and a capacitive storage element coupled between the source of the transistor switch and a cell plate reference or other reference node. Memory cells of other types and configurations may be used in alternative embodiments. As discussed above, during a row activation operation, a word line is activated, and contents of the storage cells 170 coupled to the word line (i.e., the word-line selected row) are enabled onto the bit lines 169 and thereby transferred to the page buffer 147. During a precharge operation, the open page (i.e., content of the page buffer) is closed and the bit lines 169 precharged in preparation for activation of another row. Refresh operations may be performed in rows of a given sub-bank or set of sub-banks through combinations of activation and precharge operations.

[0042] As discussed above, the column decoders 103_0 and 103_1 enable column operations (i.e., read or write operations) directed to open pages within the sub-banks of quadrants Q0 and Q1, respectively. In the embodiment of Figure 3, each of the column decoders 103_0, 103_1 includes a set of four column multiplexers 149, one for each sub-bank of the corresponding quadrant, and a bank multiplexer 151. The bank multiplexer 151 enables access to (i.e., selects) one of the column multiplexers 149 in response to a bank address, or at least the most significant bits (MSBs) or other subset of bits within the bank address. Referring to detail view 165, the selected column multiplexer 149 includes a set of multiplexer/demultiplexer circuits 164 that each enable read or write access to a respective column-address-selected column of storage elements within the page buffer 147 (column, for short); an operation referred to herein as a column access. In the case of a write operation, the bank

multiplexer 151 and column multiplexer 149 perform demultiplexing functions, routing data from the data path interface 105A to the selected column. In a read operation, the bank multiplexer 151 and column multiplexer 149 perform a multiplexing function by routing data from the selected column to the data interface 105A. Note that the bank multiplexer 151 and column multiplexers 149 may be interchanged in an alternative embodiment, so that the bank multiplexer 151 is coupled to the sub-bank bit lines 169 and a single column multiplexer is coupled between the output of the bank multiplexer 151 and the data path interface 105A.

[0043] In the embodiment of Figure 3, the data path interface 105A includes a pair of serdes transceivers 173 (i.e., serializing/deserializing transceivers that perform a parallel-to-serial conversion of outgoing data and a serial-to-parallel conversion of incoming data) each coupled between an external data path interface 171 and a respective one of column decoders 103_0 and 103_1. Each serdes transceiver 173 includes a data serializer 177, transmitter 175, data deserializer 181 and receiver 179. In a read operation, the data serializer 177 performs a multiplexing function by receiving a 128-bit read data value (i.e., column data) from the column decoder 103 via column data path 119 and delivering the read data to the transmitter 175 in the form of a sixteen byte stream. The transmitter 175, in turn, transmits each byte via the external data path interface 171 in successive data transmission intervals. The receiver 179 and data deserializer 181 perform the inverse functions of the data serializer 177 and transmitter 175. That is, the receiver 179 samples signals arriving via the external data path interface 171 during successive data reception intervals to deliver a stream of sixteen bytes to the data deserializer 181. The data deserializer 181 performs a demultiplexing function by gathering the incoming stream of bytes into a 128-bit data write data value to be delivered to the corresponding column decoder 103 via column data path 119. Although an 8-bit external data path interface 171 and a 128-bit column data path 119 are shown, different path widths may be used in alternative embodiments. In alternative embodiments in which data multiplexing/demultiplexing is unnecessary (e.g., external data path width matches the column data size of the memory device), the data serializer 177 and/or data deserializer 181 may be omitted.

[0044] Still referring to Figure 3, the transmitters 175 may be, for example, current-mode or voltage-mode output drivers for generating output waveforms having virtually any amplitude and any type of modulation. Also, the transmitters 175 may generate multi-bit symbols (i.e., bit rate greater than baud rate), perform various encoding operations (e.g., 8b/10b) and/or add error checking

information into the outgoing bitstream (e.g., parity bits, error-code correction (ECC) bits, checksum, cyclic-redundancy check values, etc.). The receivers 179, similarly, may be designed to sample current-mode or voltage-mode transmissions modulated in any manner, with each sample being resolved into one or more bits according to the number of bits conveyed in each transmitted symbol. The receiver may additionally perform decoding operations and error checking operations. Further, both the transmitter and receiver may be switched between different operating modes and/or frequencies, for example, operating on multi-bit symbols in one mode and single-bit symbols in another mode.

[0045] The signaling links that constitute the external data path may be point-to-point or multi-drop, differential or single-ended, and may be used to carry synchronous or asynchronous transmissions. The data path interface 105A, accordingly, may be a synchronous or asynchronous signaling interface. In the case of synchronous transmissions, the transmitted data signals may be self-timed (e.g., carrying clocking information within the data waveform) or accompanied by timing signals such as one or more clock signals, strobe signals or the like. In the case of self-timed transmissions, encoding circuitry may be provided in the transmitter 175 to encode each outgoing bit stream (i.e., the stream transmitted on any single link of the external data path interface in synchronism with one or more transmit clock signals) to ensure sufficient transition density for clock recovery (e.g., 8b/10b encoding), and corresponding clock-data recovery circuitry and decoding circuitry may be provided in the receiver 179 to recover clocking information and the un-encoded transmitted data. Such clocking information, whether received in the form of external timing signals (e.g., clock or strobe signals) or recovered from the incoming bit stream, may be used to control the phase of one or more sampling clock signals that are supplied to the receiver 179 to trigger sampling of the incoming data signals.

Single-Threaded Mode

[0046] Figure 4 illustrates a single-threaded mode of operation within the memory device 100 of Figure 2 and is provided, in part, for contrast with later micro-threaded operating modes described below. Referring to request path 201 (RQ), a pipelined stream of requests is received over a series of request intervals 200, with gray shaded blocks indicating requests that form part of a multi-access read transaction 205 directed to a selected bank. The striped blocks represent requests directed to other banks. In the exemplary embodiment shown, the request path is operated at a legacy signaling rate (i.e., lower than maximum supported signaling rate) of 0.8 Gigabits per second (Gb/s) per link. Each

command is transferred over a pair of transmit intervals, thereby establishing a 2.5 ns request interval. In alternative embodiments, higher or lower signaling rates may be used, and each request may be conveyed in more or fewer transmit intervals.

[0047] The request path 201 is shown as a set of logical pipelines 203A, 203B and 203C to help visualize the relative timing of different types of requests included in the multi-access read transaction 205. Pipeline 203A is referred to herein as the activation pipeline (RQ-ACT) and carries row activation requests (e.g., 207), each including a row activation command specifier together with bank and row address values to identify the specific row to be activated. Pipeline 203B is referred to herein as the column access pipeline (RQ-CA) and carries column access requests (e.g., 209), each including a column access command specifier, specifying either a read or write access, together with bank and column address values to identify the bank and column to be accessed. Pipeline 203C is referred to herein as the precharge pipeline and carries precharge requests (e.g., 213) each including a precharge command specifier and bank address to indicate the bank to be precharged.

[0048] The multi-access read transaction is initiated when a row activation request 207 directed to row 'z' of bank B0 (B0-Rz) is received. The memory device responds to the row activation request by issuing the bank address and row address to the row decoders for bank B0 (i.e., row decoders 113_0 and 113_2). In the particular embodiment shown, the minimum time between row activations in the same bank, t_{RC}, is assumed to be 40ns so that another row activation request directed to bank B0 is not received until sixteen request intervals later, as shown at 215. Also, the minimum time between row activations in arbitrarily different banks, t_{RR}, is assumed to be 10ns, so that another row activation request 217 is not received until four request intervals later.

[0049] The first column access request 209 of two column access requests that form part of the multi-access read transaction 205 is received a predetermined time after the activation request 207 (five request intervals later in this example) and specifies a read at column 'a' of the B0 open page (B0-Ca). As the minimum time between accesses to the same open page, t_{CC}, is assumed to be 5ns in this example, and the memory device is operating in single-threaded mode, the second of the two column access requests, 211, is received two request intervals after receipt of the first column access request (i.e., a t_{CC} interval later), and specifies a read at a different column, column 'b', of the B0 open page (B0-Cb). Referring briefly to Figure 2, the request interface 201 responds to the first column access request

209 by delivering bank and column address values via shaded column address paths 109_0 and 109_2 to the even bank column decoders 103_0 and 103_2 which, in turn, retrieve data from column 'a' of the B0-A and B0-B sub-banks as shown. The retrieved column 'a' data is then delivered to the data interface via the shaded column data paths 119_0 and 119_2. The request interface 201 similarly responds to the second column access request 211 by delivering bank and column address values to the even bank column decoders 203_0 and 203_2 which then retrieve data from column 'b' of the B0-A and B0-B sub-banks and output the data to the data path interfaces 105A and 105B.

[0050] Returning to Figure 4, the column data retrieved in response to the first column access request 209 is output onto external DQA and DQB signal paths 225 in a data transfer operation that begins, a predetermined time after receipt of the column access request 209. The correspondence between the column access request 209 and outgoing (or incoming) column data is illustrated by lead lines 227 extending from the column access request (i.e., in pipeline 203B) to a like-shaded data transfer over signal paths 225; a notation used in Figure 4 and other figures described below. In this single-threaded example, column data is transferred in response to the first column access request over the t_{CC} interval starting at 215. More specifically, column 'a' data is output from sub-bank B0-A over the DQA links (eight links in this example, though more or fewer links may be provided in alternative embodiments), and column 'a' data is output from sub-bank data B0-B over the DQB links, the transfer of column 'a' data from the two B0 sub-banks thus consuming the entire t_{CC} envelope as shown. As discussed above, the t_{CC} envelope is a product of the signaling bandwidth and t_{CC} interval so that, given a 5ns t_{CC} interval (a value assumed throughout the following description, though virtually any memory core technology having the same or different t_{CC} constraint may be used) and assuming a 3.2 Gb/s signaling rate in each of the 16 DQ links, the t_{CC} envelope is 32 bytes (i.e., [16 links * 3.2 Gb/s/link] * 5 ns = 256 bits = 32 bytes). In the single-threaded example shown, each column access request is serviced per t_{CC} interval so that the column transaction granularity, CTG, is also 32 bytes. Thus, the column transaction granularity is coextensive with the t_{CC} envelope.

[0051] The column 'b' data retrieved in response to the second column access request 211 is output onto the DQA and DQB signal paths over a t_{CC} interval that begins at the conclusion of the column 'a' data transfer operation. Thus, like the column 'a' transaction that precedes it, the column 'b' transaction consumes the entire t_{CC} envelope and therefore has a column transaction granularity of 32 bytes.

[0052] Still referring to Figure 4, a precharge request 213 is received a predetermined time after the second column access request 211 (three request intervals in this example) and includes a precharge command specifier (Pre Cmd) and bank address that indicates the bank to be precharged; B0 in this case. The request interface executes the requested precharge operation a predetermined time later (e.g., after the column 'b' data has been retrieved from the B0-A/B0-B page buffers) by issuing a disable signal to the row decoders for bank B0, and issuing a precharge-enable signal to the page buffers of sub-banks B0-A and B0-B to precharge the sub-bank bit lines. The precharge operation thus closes the page opened in response to the row activation request 207 and therefore concludes the multi-access read transaction 205. Because each of the two column access operations yielded 32 byte transfers, the row transaction granularity (i.e., amount of data transferred for a given row activation, RTG) is 64 bytes. More or fewer column access transactions may be performed for a given row activation in alternative embodiments, yielding correspondingly increased or decreased row transaction granularity.

[0053] Assuming that a steady stream of row activation requests and corresponding column access request pairs and precharge requests are received via the request path 201, the request path 201 may remain fully loaded (i.e., no unused request intervals) and the data path 225, similarly, may be fully consumed with the requested data transfers, each having 32-byte column transaction granularities and 64-byte row transaction granularities. When the signaling rate on the data path 225 is increased to the full rate of the memory device, however, the row and column transaction granularities also increase. For example, in one embodiment, the full signaling rate supported by the data path interface 105 of the Figure 2 memory device is 6.4 Gb/s (other signaling rates may be supported in alternative embodiments). Because the t_{CC} interval of the memory device remains unchanged, the t_{CC} envelope is doubled to 64 bytes and, if the single-threaded approach were followed, the column transaction granularity and row transaction granularity would also double to 64 bytes and 128 bytes, respectively. To support the increased column transaction granularity, a number of signal paths within the column decoders and data path interface may need to be increased. Referring to Figures 2 and 3, for example, because the 64 byte column transaction granularity corresponds to a 256-bit (32 byte) column access in each of the sub-banks, each of the 128-bit signal paths within the column decoders 103 (i.e., between the column multiplexer 149 and bank multiplexer 151) and the data path interfaces 105A, 105B would expand to 256-bit signal paths to support the increased data transfer rate. While potentially realizable, such increased path widths result in increased manufacturing cost and power consumption (i.e., the path widths being increased in each sub-bank and data interface of the memory device) and the

headroom available headroom for such increases is shrinking. Also, as discussed above, in applications that tend to access small, dispersed data objects, only a small portion of the data returned in a given column access may be useful. For example, a common triangle size in modern graphics applications is six bytes and, due to rendering order, successively rendered triangles are often unlikely to be acquired in the same column access. In such applications, doubling the column transaction granularity from 32 bytes to 64 bytes may provide little improvement in effective bandwidth.

[0054] Figure 5 illustrates a request interface that may be used to support a single-threaded mode of operation within the memory device as well as micro-threaded modes of operation discussed below. The request interface 300 includes a request decoder 301, even-bank row control registers 305A, 305B (EBRC), odd-bank row control registers 307A, 307B (OBRC), even-bank column control registers 309A, 309B (EBCC) and odd-bank column control registers 311A, 311B (OBCC). The even- and odd-bank row control registers 305, 307 are coupled to the request decoder 301 via a row bus 315, and the even- and odd-bank column control registers 309, 311 are coupled to the request decoder 301 via a column bus 317.

[0055] In one embodiment, incoming symbol streams received via request pads 303 (i.e., from an external request path) are deserialized in an optional request deserializer 304 to deliver a corresponding stream of n-bit wide requests to the request decoder 301. (Note that, while pads are referred to in a number of embodiments herein, in all such cases, capacitive-coupling nodes or any other interface to an external signaling path may be used.) The incoming requests may include virtually any type of requests including, without limitation, the row activation requests, column access requests and precharge requests discussed above, as well as other requests used, for example, to initiate refresh operations within one or more storage banks, program operating modes within the memory device (e.g., selecting between single-threaded mode and one or more of a number of different micro-threaded modes; and selecting between a number of different refresh modes, power modes, precharge modes, etc.), initiate signaling calibration and/or training operations, initiate self-tests and so forth.

[0056] The request decoder 301, which may be implemented by one or more state machines, microsequencers and/or other control circuitry, decodes each incoming request (e.g., by parsing a command specifier field or operation code field to identify the request) and issues various signals necessary to carry out the requested operation. For example, upon decoding a row activation request

having the bank address and row address fields shown in request 207 of Figure 4, the request decoder 301 may output the row address and bank address onto the row bus 315 along with a control value that indicates an activation operation and then, depending on whether the activation request is directed to an even or odd bank (e.g., determined by inspection of the least significant bit (LSB) or other bit or bits of the bank address), assert an even-row strobe signal 321A (ERS) or odd-row strobe signal 321B (ORS) to load the address and control values from the row bus 315 into the even-bank row control registers 305A, 305B or odd-bank row control registers 307A, 307B. Address and control values loaded into even-bank row control registers 305 are supplied to the even-bank row decoders for the group A and group B sub-banks (i.e., row decoders 113_0 and 113_2 of Figure 2) via signal paths 111_0 and 111_2, respectively, and address and control values loaded into odd-bank row control registers 307 are supplied to the odd-bank row decoders for the group A and group B sub-banks via signal paths 111_1 and 111_3. In one embodiment, the delivery of address and control values via paths 111 initiates the indicated row operation (e.g., activation or precharge) within the corresponding row decoder so that row operations are effectively initiated in response to assertion of the even-row strobe signal 321A and odd row strobe signal 321B (i.e., when the corresponding registers 305 and 307 are updated). In alternative embodiments, the even-row strobe signal 321A and odd-row strobe signal 321B (or other control signals derived therefrom or independently generated) may be output to the row decoders to initiate row operations therein.

[0057] In one embodiment, the request decoder 301 responds to incoming column access requests in substantially the same manner as row activation requests, except that bank address and column address values included with the requests are output onto the column address bus 317 together with a control value that indicates, for example, whether a read or write operation is to be performed. Thereafter, the request decoder 301 asserts either an even-column strobe signal 323A (ECS) or odd-column strobe signal 323B (OCS) to load the address and control values from the column address bus 317 into either the even-bank column control registers 309A, 309B or odd-bank column control registers 311A, 311B, thereby initiating the specified column access operation in the corresponding column decoder (i.e., the contents of the column control registers 309 and 311 are output to corresponding column decoders via paths 109 to initiate column access operations therein). As with row requests, the request decoder 301 may inspect one or more bits of the bank address to determine whether a given column access request is directed to an odd or even bank and assert either the even-column strobe signal 323A or odd-column strobe signal 323B accordingly. Alternatively, the request decoder 301 may

associate incoming column access requests with previously received row activation requests according to a predetermined protocol so that the bank address received in a row activation request is used to determine the set of banks, even or odd, to which a subsequently received column access request is directed. In such an embodiment, the LSB of the bank address (or other bit(s) used to specify the target set of banks) may be omitted from the column access request to enable other requests or information (e.g., precharge information) to be conveyed therein. In either case, bank and column address values (which may omit the LSB bit or other bit(s) of the bank address used to specify the target set of banks) loaded into even-bank column control registers 309 are output to the even-bank column decoders for the group A and group B sub-banks, respectively (i.e., column decoders 103_0 and 103_2 of Figure 7), and bank and column address values loaded into odd-bank column control registers 311 are output to the odd-bank column decoders.

[0058] Figure 6 illustrates an exemplary timing of row and column strobe signal assertions by the request decoder 301 of Figure 5 when the memory device 100 of Figure 2 is operating in a single-threaded mode. As shown, upon decoding a row activation request 207, the request decoder 301 asserts either an even-row strobe signal 321A (ERS) or an odd-row strobe signal 321B (ORS) to load either the even-row control registers 305A, 305B or the odd row control registers 307A, 307B, respectively, with the bank address, row address and control information provided in the request 207, thereby initiating a row activation operation in either the even or odd bank sets. Although assertion of even row strobe signal 321A is shown in Figure 6, odd row strobe signal 321B would be asserted to initiate row activation in an odd bank set. The least significant bit of the bank address may be used to control which of the two strobe signals 321A and 321B is asserted, and therefore need not be loaded into the selected control register. After a t_{RR} interval has elapsed, another row activation request directed to a different bank is received, and another strobe signal 321A or 321B is asserted to initiate a corresponding row activation operation.

[0059] Upon decoding a column access request 209 directed to the row activated in response to row activation command 207 (i.e., specifying the same bank address as row activation command 207), the request decoder asserts either an even-column strobe signal 323A (ECS) or odd-column strobe signal 323B (OCS) to load either the even-column control registers 309A, 309B or odd-column control registers 311A, 311B, respectively, with the bank address, column address and control information provided in the request 209, thereby initiating a column access operation (e.g., a read or write operation) within the

open page for the specified bank. Although assertion of even column strobe signal 323A is shown in Figure 6, odd column strobe signal 323B would be asserted to initiate a column access operation in a transaction directed to a bank in the odd bank set. Again, the least significant bit of the bank address may be used to control which of the two strobe signals 323A, 323B is asserted to initiate a column access operation. After a t_{CC} interval has elapsed, another column access request 211, directed to the same bank as request 209 but different column address, is received within the request decoder 301. Upon decoding the column access request 211, the request decoder asserts either the even-column strobe signal 323A or odd-column strobe signal 323B to load the corresponding pair of registers 309A/309B or 311A/311B (i.e., the same pair of registers loaded in response to decoding request 209, as both requests are directed to the same open page) and thereby initiate a second column access operation directed to the row activated in response to request 207. Thus, a column strobe signal (323A or 323B) is asserted once per t_{CC} interval to enable the specified data transfer to be carried out over the complete t_{CC} interval and using all the links of the DQ path. That is, when the memory device of Figure 2 is operated in single-threaded mode, the data transfer in response to a column access request consumes the entire t_{CC} envelope.

[0060] Reflecting on the operation of the request interface 300 of Figure 5, it should be noted that because both the even-row control registers 305A, 305B are operated in lock step (i.e., 305A and 305B are loaded in response to the same strobe signal 321A), registers 305A and 305B may be replaced by a single row control register which, when loaded, initiates the specified row operation (e.g., activation or precharge) in the sub-bank quadrants that form the even bank set (i.e., Q0, Q2). Similarly, the odd-row control register pair 307A/307B, even-column control register pair 309A/309B and odd-column control register pair 311A/311B may each be replaced by a respective single register. Further, if the request interface 300 did not include support for micro-threaded column operations, the entire register set could be reduced to a single row control register and a single column control register, the control and address information loaded into each register being provided to the row and column decoders in all four quadrants of the memory device 100. In such an embodiment, the row and column decoders within each quadrant may determine whether to initiate a row or column operation, for example, based on the least significant bit of the bank address (i.e., if BA[0] is a '0', row/column operations are initiated in the decoders of the even quadrants, Q0/Q2, and if BA[0] is a '1', row/column operations are initiated in the decoders of the odd quadrants, Q1/Q3). When the memory device 100 is operated in micro-threaded mode, however, the additional row control registers enable temporally overlapping row operations in

different regions of memory device 100 and the additional column control registers enable temporally overlapping column operations in different regions of memory device 100. In one embodiment, the different regions in which overlapping operations are performed are the even and odd bank sets of memory device 100. In another embodiment, the different regions are the four quadrants of the memory device 100. These embodiments and others are discussed in further detail below.

Micro-Threaded Memory Transactions

[0061] Figures 7 and 8 illustrate an exemplary sequence of micro-threaded memory transactions that may be performed in the memory device 100 of Figure 2 when operated in a micro-threaded mode at full signaling rate (e.g., data path and request path signaling rates increased to 6.4 Gb/s and 1.6 Gb/s, respectively; doubling the 3.2 Gb/s and 0.8 Gb/s legacy signaling rates described above). Rather than allocating the full t_{CC} envelope to a single column access (i.e., as in the single-threaded mode described in reference to Figures 2-6) and redesigning the memory device 100 to include double-width internal data path widths, the t_{CC} envelope is subdivided into sub-envelopes that are allocated to alternating transactions in the odd and even bank sets. That is, recognizing that the t_{RR} constraint applies to arbitrary bank selection and is imposed primarily to avoid conflicting use of resources shared by banks in the same bank set, (e.g., row decoders shared by even banks and row decoders shared by odd banks), it follows that row activation operations directed alternately to the odd and even bank sets may be executed in sub-intervals within the overall t_{RR} interval, referred to herein as partial t_{RR} intervals, t_{RRp}. Further, because distinct sets of column decoders and distinct data path resources are provided for the even and odd bank sets, micro-threaded column operations directed to the activated rows in alternate bank sets may be executed one after another within a single t_{CC} interval referred to herein as partial t_{CC} intervals, t_{CCp}. Through this approach, decoder and data path resources within the memory device 100 that are used at approximately 50% duty in single-threaded mode (i.e., using either the even-bank resources or the odd-bank resources for a given row or column operation) are used concurrently in the micro-threaded mode to support micro-threaded column access operations. Because the data transferred in each micro-threaded column access operation consumes only a portion of a t_{CC} envelope, reduced column transaction granularity is achieved relative to the granularity for single-threaded operation at the same signaling rate. Thus, data throughput is effectively doubled without having to double the widths of internal data paths of the memory device, while at the same time reducing column transaction granularity.

[0062] Referring to the depiction of memory device 100 in Figure 7 and the row activation pipeline 251A shown in Figure 8, a first row activation request 253 initiates activation of bank B0, row 'z' (i.e., "Rz" in Figure 7, "Act B0-Rz" in Figure 8). One t_{CC} interval later (i.e., four 1.25 ns request intervals later at the exemplary 1.6 Gb/s request path signaling rate shown), a second activation request 255 initiates activation of bank B1, row 'y' (Act B1-Ry). Note that, while two row activation requests 253, 255 are received within a single t_{RR} interval, the two requests are directed alternately to even and odd banks (B0 and B1 in this example) and therefore do not conflict. A predetermined time after receipt of the B0-Rz activation request 253, a first micro-threaded column access request 257 specifying a read at bank B0, column 'a' is received (i.e., Rd B0-Ca), as shown in column access pipeline 251B. Similarly, a predetermined time after receipt of the B1-Ry activation request 255, and before the t_{CC} interval for the first micro-threaded column access request 257 has elapsed, a second micro-threaded column access request 259 specifying a read at bank B1, column 'e' is received (Rd B1-Ce). Thus, two micro-threaded column access requests 257, 259 are received within a single t_{CC} interval and, because the requests are directed alternately to odd and even bank sets, are serviced without conflict. More specifically, as shown at 275, read data retrieved from column 'a' of sub-banks B0-A and B0-B is delivered to the data interfaces 105A and 105B for transmission on the DQA and DQB links, respectively, during the first half of the t_{CC} interval starting at 271, and read data retrieved from column 'e' of sub-banks B1-A and B1-B is delivered to the data interfaces 105A and 105B for transmission on the DQA and DQB links during a second half of the same t_{CC} interval. By this arrangement, the 64-byte t_{CC} envelope is effectively partitioned between two micro-threaded column access operations each having a 32-byte column transaction granularity, with the data for each micro-threaded column access operation being output onto the DQA and DQB links during a respective t_{CCp} interval as shown in expanded view 272. Additionally, because the t_{CC} envelope is partitioned between column accesses directed to odd and even bank sets, the data transmitted during either partial t_{CC} interval may be carried by the existing data path interfaces 105A/105B. Accordingly, the internal data path width of the memory device 100 need not be increased to accommodate the increased data path bandwidth, avoiding the added manufacturing/operating costs and headroom issues discussed above.

[0063] Still referring to Figures 7 and 8, a t_{CC} interval after receipt of the first B0-directed micro-threaded column access request 257, a second micro-threaded column access request 261 directed to B0 and specifying a read at column 'b' is received (i.e., Rd B0-Cb). Similarly, a t_{CC} interval after receipt of the first B1-directed micro-threaded column access request 259, a second B1-directed micro-threaded

column access request 263 specifying a read at column 'f' is received (i.e., Rd B1-Cf). The second B0-directed and B1-directed micro-threaded column access requests 261, 263 are serviced in the same manner as the first B0-directed and B1-directed micro-threaded column access requests 257, 259, resulting in transmission of B0, column 'b' data over the first half of the t_{CC} interval (i.e., first t_{CCp} interval) that immediately succeeds the transmission of the B1, column 'e' data, and transmission of B1, column 'f' data over the second half of the t_{CC} interval. Thus, four micro-threaded column operations are executed, resulting in four 32-byte data transfers over a single t_{RR} interval starting at 271. As each row activation yields two 32-byte column data transfers, each within a respective t_{RRp} interval as shown at 274, the row transaction granularity is 64 bytes, half the 128-byte data transfer capacity of the data path over the t_{RR} interval (i.e., half the 128-byte t_{RR} envelope).

[0064] Precharge requests 265 and 267 directed to banks B0 and B1 are received in the request interface 101 a predetermined time after receipt of the micro-threaded column access requests 261 and 263 directed to the same banks (i.e., as shown in precharge pipeline 251C). The precharge requests 265, 267 are serviced in the manner discussed above to close the open pages in the specified banks.

[0065] Figure 9 illustrates an exemplary timing of row and column strobe signal assertions by the request decoder 301 of Figure 5 when in a micro-threaded mode.. As shown, upon decoding a row activation request 253 directed to an even bank, the request decoder 301 asserts the even-row strobe signal 321A to load even-row control registers 305A, 305B and thereby deliver bank and address values to the row decoders for the even banks. After a partial t_{RR} interval (t_{RRp}) has elapsed, a row activation request 255 directed to an odd bank is received. Upon decoding the odd-bank row activation request 255, the request decoder 301 asserts the odd-row strobe signal 321B to load odd-bank row control registers 307A, 307B and thereby deliver bank and row address values to the row decoders for the odd banks. Thus, assuming a fully loaded row activation pipeline, the request decoder alternately asserts the even-row and odd-row strobe signals 321A, 321B after each t_{RRp} interval to deliver bank and row address values alternately to the row decoders for the odd and even bank sets.

[0066] Still referring to Figure 9, upon decoding a column access request 257 (i.e., a micro-threaded column access request) directed to an even bank, the request decoder 301 asserts the even-column strobe signal 323A to load even-bank column control registers 309A, 309B and thereby deliver bank and column address values to the column decoders for the even banks. After a partial t_{CC} interval (t_{CCp}) has

elapsed, a column access request 259 directed to an odd bank is received. Upon decoding the odd-bank column access request 259, the request decoder 301 asserts the odd-column strobe signal 323B to load odd-bank column control registers 311A, 311B and thereby deliver bank and column address values to the column decoders for the odd banks. Thus, assuming a fully loaded column access pipeline, the request decoder 301 alternately asserts the ECS and OCS signals after each t_{CCp} interval to deliver bank and column address values alternately to the column decoders for the odd and even bank sets. As shown in Figure 8, the alternating assertion of the ECS and OCS signals enables a time-staggered transfer of column data for multiple micro-threaded column access operations within a single t_{CC} interval. The ECS and OCS signals are asserted by the request decoder 301 during a second t_{CC} interval in response to column access requests 261 and 263, respectively, thereby enabling the time staggered data transfer to be repeated during a subsequent t_{CC} interval as shown in Figure 8.

[0067] Figure 10 illustrates exemplary link-staggered micro-threaded memory transactions that may be performed in an alternative embodiment of the memory device 100 of Figure 2. Row activation requests 253 and 255, micro-threaded column access requests 257, 259, 261 and 263, and precharge requests 265 and 267 are received in the request interface 101 and processed in generally the same manner as discussed above in reference to Figures 7-9. However, instead of subdividing the t_{CC} envelope temporally (i.e., time-staggering the column data output in response to micro-threaded column access requests received in the same t_{CC} interval), the t_{CC} envelope is subdivided spatially through concurrent data transfer of the column data for same-t_{CC}-interval micro-threaded column access requests on different portions of the DQA and DQB data paths as shown at 375; an operation referred herein to as link staggering. That is, the column data transferred in response to micro-threaded column access request 257 is transmitted via a first subset of the DQA links and a first subset of the DQB links (e.g., DQA[3:0] and DQB[3:0], while column data transferred in response to micro-threaded column access request 259 is concurrently (i.e., partly or completely overlapping in time) transmitted via a second subset of the DQA lines and a second subset of the DQB links (e.g., DQA[7:4] and DQB[7:4]). Similarly, the column data transferred in response to micro-threaded column access requests 261 and 263 is transmitted during a subsequent t_{CC} interval over the first and second subsets of DQ links, respectively. The t_{CC} envelope remains at 64 bytes, with the column transaction granularity and row transaction granularity being 32 bytes and 64 bytes, respectively, as in the temporally-staggered embodiment of Figure 8. Thus, the link-staggered approach provides effectively the same benefits as the temporally-staggered approach in terms of reduced row and column transaction granularity, but

does so by allocating respective portions of the DQ paths to service the micro-threaded column access requests, instead of respective portions of the t_{CC} interval.

[0068] Figures 12A and 12B illustrate exemplary data path interfaces 401 and 411 that may be used to support the time-staggered and link staggered data transfers shown in Figures 8 and 10, respectively. The data path interface 401 of Figure 12A corresponds generally to the data path interface 105A described in reference to Figure 3 and includes DQA pads 171 and a pair of transceivers 403 and 405 coupled between the pads 171 and respective column data paths 119_0 and 119_1. Each transceiver 403, 405 includes a data serializer 177 and transmitter 175 to generate an output data stream, and a receiver 179 and data deserializer 181 to receive an incoming data stream. More specifically, in the exemplary embodiment shown, the data serializer 177 converts 128-bit column data values received via the column data path 119 into a sequence of sixteen 8-bit values (e.g., picking off one byte at a time in round-robin fashion from each of sixteen different offsets within the 128-bit column data) which are delivered to the transmitter 175 for transmission in respective transmission intervals via the DQA pads 171. Conversely, a sequence of sixteen 8-bit values recovered by the receiver 179 are delivered to the data deserializer 181 which gathers the values into a 128-bit column data value that is provided to the column decoder via column data path 119. In the time-staggered data transfer operation illustrated in Figure 8, the data transfer path through transceiver 403 is used during a first partial t_{CC} interval, and the data transfer path through transceiver 405 is used during the second partial t_{CC} interval, as indicated by arrows 408A and 408B which are shaded to correspond to the column access transactions of Figure 8.

[0069] In the data path interface 411 of Figure 12B, the eight links of the DQA path are subdivided into two groups of four links, DQA[3:0] and DQA[7:4], and used to transfer data for respective micro-threaded column transactions. Accordingly, a first pair of transceivers 413A/415A is coupled to a first set of four DQA pads 171A and a second pair of transceivers 413B/415B is coupled to a second set of four DQA pads 171B, with each individual transceiver including an output data path formed by a data serializer 427 and transmitter 425, and an input data path formed by a receiver 429 and data deserializer 431. As each 128-bit column data value is transferred over half the number of signal links (e.g., four instead of eight), the data serializer is a 1:32 data serializer (i.e., converting the 128-bit column data value into a sequence of thirty-two 4-bit data values) instead of the 1:16 data serializer of Figure 12A, and the data deserializer is a 32:1 data deserializer (gathering a sequence of thirty-two 4-bit values into a 128-bit column data value) instead of the 16:1 data deserializer 181 of Figure 12A. Thus,

each transceiver 413A, 415A, 413B, 415B transfers a 128-bit column data between a column data path 119 and a smaller number of DQ links, but over twice the interval (i.e., over a full t_{CC} interval rather than a half t_{CC} interval).

[0070] As in the embodiment of Figure 12A, the micro-threaded column transactions serviced in the same t_{CC} interval are directed alternately to odd and even banks so that one set of four data path links is fed by data from (or feeds data to) one of the column data paths 119_0 and 119_1 over a given t_{CC} interval, and the other set of four data path links is concurrently fed by data from (or feeds data to) the other of the column data paths 119_0 and 119_1 during the t_{CC} interval. This data flow arrangement is shown, for example by arrows 418A and 418B which are shaded to correspond to the column access transactions of Figure 10.

[0071] Comparing Figures 12A and 12B, it can be seen that the data path interfaces 401 and 411 differ primarily in the operation of the data serializer and data deserializer circuits. That is, the two four-link transmitters 425 in transceivers 413A and 413B may be implemented and connected to the eight DQA pads (i.e., 171A and 171B) so as to be equivalent to the single eight-link transmitter 175 in transceiver 403, and the two four-link receivers 429 in transceivers 413A and 413B may likewise be equivalent to the eight-link receiver 179 in transceiver 403. The 1:16 data serializers 177 in transceivers 403 and 405 differ from the 1:32 data serializers 427 in transceivers 413A, 413B, 415A and 415B primarily by the manner in which incoming 128-bit column data is distributed to the DQA data pads; data deserializer 177 delivering 8-bit chunks of the 128-bit column data to eight DQA pads over 16 transmission intervals and, data deserializer 427 delivering 4-bit chunks of the 128-bit column data to four DQA pads over 32 transmission intervals. The 16:1 data deserializers and 32:1 data deserializers are similarly different in the manner of data distribution from DQA pads to column data values. Thus, in one embodiment, the data path interfaces 401 and 411 are implemented by a single data path interface circuit having data serializer and data deserializer circuits that are configurable (e.g., through mode register programming) to support either link-staggered or time-staggered data transfer in response to micro-threaded column access requests.

[0072] Referring to Figures 10 and 12B, it should be noted that, because column data retrieved in response to micro-threaded column access request 257 will become available for transfer before column data retrieved in response to micro-threaded column access request 259, the first-retrieved

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column data may be buffered (e.g., within the data path interface 411) until the second-retrieved column data is available, thereby enabling simultaneous (i.e., fully concurrent) transfer of the column data for the two access requests. Alternatively, as shown in Figure 11, the first-retrieved column data (i.e., retrieved in response to request 257) may be output as soon as it becomes available, thus resulting in a time-staggering of the same-row transmissions on the upper and lower partitions of the data path as shown at 385, with transfer of the second-retrieved column data being delayed relative to transfer of the first-retrieved column data by a partial t_{CC} interval (i.e., t_{CCp}). The transmissions over the signal path partitions are thus partially overlapped (but still concurrent over a partial t_{CC} interval). Such an approach may be desirable in some applications, as no buffering of column data is required and a single, deterministic memory access latency applies to each micro-threaded column access. By contrast, if column data retrieved in response to a first micro-threaded column access request is buffered to enable simultaneous, link-staggered transfer with column data retrieved in response to a second micro-threaded column access request, the two micro-threaded column access requests may have different, though still deterministic, memory access latencies.

[0073] Figures 13 and 14 illustrate an exemplary sequence of micro-threaded memory transactions that may be performed in the memory device 100 of Figure 2 when operated in an alternative micro-threaded mode at full signaling rate (e.g., data and request bandwidth doubled over the legacy 3.2 Gb/s and 0.8 Gb/s signaling rates described above). In the alternative micro-threaded mode, referred to herein as a sub-bank micro-threaded mode, the number of micro-threaded column transactions per t_{CC} envelope is doubled relative to the micro-threaded mode of Figures 7 and 8 by increasing the number of column addresses provided in each column access request, and by applying the pairs of column addresses delivered in each column access request to different sub-banks of the same bank. Referring to the row activation pipeline 461A, column access pipeline 461B and precharge pipeline 461C shown in Figure 14, for example, a sequence of row activation requests 253, 255 is received as in Figure 8 (i.e., with the pair of requests received within each t_{RR} interval being directed alternately to even and odd banks), and a sequence of micro-threaded column access requests 467, 469, 471, 473 are also received as in Figure 8, but with each access request including a bank address and two column addresses as shown at 480. By applying the two column addresses against alternating sub-banks of a specified even or odd bank (i.e., sub-bank micro-threading), two distinct 16-byte column data values may be retrieved per micro-threaded column access, thus achieving 16-byte column transaction granularity. In the particular example of Figures 13 and 14, for instance, a first micro-threaded column access request 467

specifies a read at column 'a' of sub-bank B0-A and a read at column 'c' of sub-bank B0-B (i.e., Rd B0-Ca/Cc), while a second micro-threaded column access 469 received within the same t_{CC} interval specifies read at column 'e' of sub-bank B1-A and a read at column 'g' of sub-bank B1-B (Rd B1-Ce/Cg). In a subsequent t_{CC} interval, two additional micro-threaded column access requests 471 and 473 are received, the first specifying a read at columns 'b' and 'd' of the B0-A and B0-B sub-banks (Rd B0-Cb/Cd), and the second specifying a read at columns 'f' and 'h' of the B1-A and B1-B sub-banks (Rd B1-Cf/Ch). As shown at 275, the t_{CC} envelope is temporally subdivided between successive t_{CCp} intervals and spatially subdivided between DQA and DQB data path links to accommodate the four column data transfers that correspond to the four column addresses received in each pair of micro-threaded column access requests. Thus, through sub-bank micro-threading, the column transaction granularity is reduced to 16 bytes without reduction in the aggregate amount of transferred data (i.e., peak bandwidth of the memory device is maintained). The row transaction granularity remains at 64 bytes as four 16-byte column data transfers are performed per activated row.

[0074] Figure 15 illustrates an embodiment of a request interface 500 that may be used within the memory device 100 of Figure 2 (i.e., to implement request interface 101) to enable the micro-threaded memory transactions described in reference to Figures 13 and 14. As in the embodiment of Figure 5, the request interface 500 includes a request decoder 501 to process an incoming stream of requests (i.e., received via pads 303 and deserialized, if necessary, by optional request deserializer 304), even-bank row control registers 305A, 305B, odd-bank row control registers 307A, 307B, even-bank column control registers 309A, 309B and odd-bank column control registers 311A, 311B. The request interface 500 also includes a row bus 315 coupled between the request decoder 501 and the even- and odd-bank row control registers 305, 307, a first column bus 503A coupled between the request decoder 501 and the even-bank column control registers 309 and a second column bus 503B coupled between the request decoder 501 and the odd-bank column control registers 311.

[0075] Upon decoding a row activation request, the request decoder 501 outputs the row address and bank address onto the row bus 315 and, as discussed in reference to Figure 5, asserts either an even-row strobe signal 321A or odd-row strobe signal 321B (i.e., depending on whether the request is directed to an even bank or odd bank) to load the bank and row address values into either the even-bank row control registers 305 or odd-bank row control registers 307. Upon decoding a micro-threaded column access request having a bank address and two column addresses (i.e., a sub-bank micro-

threaded column access), the request decoder 501 outputs the first and second column addresses on the first and second column buses 503A and 503B, respectively, then asserts either an even-column strobe signal 323A or odd-column strobe signal 323B (i.e., depending on whether the request is directed to an even bank or odd bank) to load the first column address into either the even-bank or odd-bank column control register (305A or 307A) for the group A sub-banks (i.e., referring to Figure 13, the sub-banks in quadrants Q0 and Q1), and to load the second column address into the corresponding even-bank or odd-bank column control register (305B or 307B) for the group B sub-banks (i.e., sub-banks in quadrants Q2 an Q3). In one embodiment, the bank address value received in the sub-banked micro-threaded column access request is output onto both the first and second column buses 503A and 503B and loaded, along with the first and second column addresses, into either the even-bank or odd-bank column control registers 309 or 311 in response to assertion of the even-column load or odd-column strobe signals 323A, 323B. In an alternative embodiment, a separate bank address bus may be provided and coupled in common to the even and odd-bank column control registers 309 and 311 (and to the request decoder 501) to enable a bank address supplied thereon to be loaded into bank address fields within those registers (or into separate bank address registers). Also, in another embodiment, a single column bus is coupled to all the column control registers 309, 311 and time-multiplexed to load the first column address into one of column control registers 309A and 311A, and the second column address into one of column control registers 309B and 309B in respective address transfer operations. In such an embodiment, distinct strobe signals may be provided to each of the four column control registers 309A, 309B, 311A, 311B to enable one column control register to be loaded at a time. Also, in all such embodiments, the two column addresses may be independently specified by the incoming micro-threaded column access request, or may be specified in relation to one another. For example, one of the two addresses may be specified as an arithmetic or logical offset from the other. The offset value may be specified in the column access request, or the column access request may include a value that is used indirectly to determine the offset value, for example, by indexing a lookup table of offset values.

[0076] In the embodiment of Figure 15, the request decoder 501 may assert the register strobe signals 321A, 321B, 323A and 323B at the times shown in Figure 9, thereby enabling the two column addresses received in each sub-bank micro-threaded column access request to be applied concurrently within each t_{CCp} interval (i.e., simultaneously or at least partly overlapping in time) to retrieve respective sets of data from different columns of the same bank. In an embodiment having a shared, time-multiplexed column bus, four column strobe signals (e.g., ECS1, ECS2, OCS1, OCS2) may be asserted in

succession to enable two column control register load operations per t_{CCp} interval. For example signals ECS1 and ECS2 may be asserted one after another during a first t_{CCp} interval, and OCS1 and OCS2 asserted one after another during a second t_{CCp} interval.

[0077] Figures 16 and 17 illustrate exemplary micro-threaded memory operations in which separate row and column addresses are used to access sub-banks in each of the four quadrants, Q_0-Q_3, of a memory device 530 within a single t_{CC} interval. More precisely, because the request interface 531 of memory device 530 delivers unique bank, row and column addresses to the address decoders (i.e., column decoders 103 and row decoders 113) for each quadrant, the storage arrays in each quadrant are effectively converted from sub-banks to banks, thereby yielding a sixteen bank architecture having banks B0-B15 as shown in Figure 16. As in the other memory device embodiments discussed above, memory device 530 may have more or fewer storage arrays in alternative embodiments, yielding correspondingly more or fewer banks. Also, any of the sixteen banks may include two or more constituent sub-banks.

[0078] Referring to Figures 16 and 17, the row activation pipeline 551A is more densely loaded than in previously described embodiments to deliver row activation requests 553, 555, 557 and 559 directed to banks within each of the four quadrants of the memory device 530 in a single t_{RR} interval. That is, the t_{RR} interval is sub-divided into four t_{RRp} intervals, with a row activation request being received in each. In the specific example shown in Figures 16 and 17, rows 'w', 'x', 'y' and 'z' are activated one after another in banks B0, B8, B9 and B1, respectively (i.e., Act B0-Rw, Act B8-Rx, Act B9-Ry and Act B1-Rz), though rows may be activated in each of the four quadrants in different order in subsequent transactions or in alternative embodiments.

[0079] Referring to column access pipeline 551B, a predetermined time after the first row activation request 553 is received, a pair of dual-address micro-threaded column access requests 561, 563 are received over a first t_{CC} interval 550, thereby delivering four bank addresses and four column addresses that may be applied against pages opened in the four quadrants in response to activation requests 553, 555, 557 and 559. In the particular example shown, the first dual-address micro-threaded column access request 561 includes a first pair of addresses, Bank Addr1 and Col Addr1 as shown at 577, that specify an access at column 'a' of bank B0 (i.e., in the open page thereof), and a second pair of addresses, Bank Addr2 and Col Addr2, that specify an access at column 'b' of bank B8 (i.e., Rd B0-Ca/B8-

Cb). The second dual-address micro-threaded column access request 563 specifies an access at column 'c' of bank B1 and column 'd' of bank B9 (Rd B1-Cc/B9-Cd). Because each of the four bank addresses provided in the pair of access requests 561 and 563 and specifies a bank in a different quadrant of the memory device 530, no column decoder or data path conflict arises in servicing the requests. Accordingly, a predetermined time after receipt of the four address values in the pair of access requests 561 and 563, four corresponding sets of column data are transmitted via the data path over a t_{CC} interval that begins at 577. As shown at 575, the four sets of column data are transmitted in both link-staggered manner (i.e., two sets of data transferred on the DQA links and two sets transferred on the DQB links) and time-staggered manner (the column data corresponding to the first and access requests 561 and 563 being transferred in first and second t_{CCp} intervals, respectively) within the 64-byte t_{CC} envelope, with each set of column data having a 16 byte column transaction granularity.

[0080] Still referring to Figures 16 and 17, a second pair of dual-address micro-threaded column access requests 565 and 567 are received in the t_{CC} interval that immediately follows interval 550. As in the first pair of access requests 561 and 563, the four bank addresses carried within the second pair of access requests specify accesses at selected columns of the previously activated rows of banks in each of the four quadrants of the memory device 530 (e.g., Rd B0-Ce/B8-Cf and Rd B1-Cg/B9-Ch). Accordingly, a predetermined time after receipt of the four address values in the second pair of micro-threaded column access requests 565 and 567, four corresponding sets of column data are transmitted via the data path. The four sets of column data are transmitted link-staggered and time-staggered within the 64-byte t_{CC} envelope, with each set of column data having a 16 byte column transaction granularity. The t_{RR} envelope remains at 128 bytes (i.e., twice the t_{CC} envelope as $t_{RR} = 2t_{CC}$ in this example), but, due to the four-way partitioning of the t_{RR} interval, the row transaction granularity is reduced to 32 bytes.

[0081] Still referring to Figure 17, the increased request density in row activation pipeline 551A may eliminate request intervals otherwise used to issue precharge requests. In one embodiment, precharge requests that would otherwise be transmitted during the intervals shown at 581 and 583 of a precharge request pipeline 551C, are instead handled by a sub-field within column access requests. For example, as shown in at 577 and 579, a precharge bit (or bits) may be included with each column access request to indicate whether a precharge operation is to be automatically performed upon conclusion of the requested access. Thus, in access request 561, the precharge bit is reset (e.g., "Prechg = 0" as shown at 577) to defer the precharge operation, leaving the pages of the specified banks (B0 and B8) open for

one or more subsequent column accesses. In access request 567, the precharge bit is set (e.g., "Prechg = 1" as shown at 579), thereby instructing the memory device 530 to perform precharge operations in the specified banks (B1 and B9) at the conclusion of the specified column accesses.

[0082] Figure 18 illustrates an embodiment of a request interface 600 that may be used to implement request interface 531 within the memory device 530 of Figure 16 and to support the four-way micro-threaded transactions described in reference to Figure 17. As in the embodiment of Figures 5 and 15, the request interface 600 includes a request decoder 601 to process an incoming stream of requests (i.e., received via pads 303 and deserialized, if necessary, by optional data deserializer 304), even-bank row control registers 305A, 305B, odd-bank row control registers 307A, 307B, even-bank column control registers 309A, 309B and odd-bank column control registers 311A, 311B. The request interface 600 also includes a row bus 315 coupled between the request decoder 601 and the even-bank and odd-bank row control registers 305, 307 and, as in the embodiment of Figure 15, first and second column buses 503A and 503B coupled to the even-bank column control registers 109 and odd-bank column control registers 11, respectively.

[0083] Upon decoding a row activation request, the request decoder 601 outputs the row address and bank address onto the row bus 315, then asserts one of four row-register strobe signals 605A, 605B, 607A or 607B (ERSA, ERSB, ORSA, ORSB) according to the quadrant specified in the least two significant bits (or other bits) of the bank address; an address field referred to herein as the quadrant address. Assuming, for example, that incoming stream of activation requests is directed in round-robin fashion to quadrants Q0, Q2, Q1 and Q4 of the Figure 16 memory device 530, then the row-register strobe signals 605A, 605B, 607A and 607B are asserted one after another in respective t_{RRp} intervals. Other quadrant address sequences may be used in alternative embodiments, resulting in a different sequence of row-register strobe signal assertions.

[0084] Upon decoding a dual-address micro-threaded column access (e.g., request 561 of Figure 17), the request decoder 601 outputs the first bank address and column address values therein onto the first column bus 503A and the second bank address and column address values therein (BA2, CA2) onto the second column bus 503B, then asserts either an even-column strobe signal 323A (ECS) or odd-column strobe signal 323B (OCS) according to whether the pair of addressed banks are odd or even. In alternative embodiments, to avoid restrictions on the pair of banks addressed in a given multi-threaded

column access request (e.g., enabling a column access directed to an odd bank to be paired with a column access directed to an even bank), separate column strobe signals and column address buses may be provided to each of the column control registers 309A, 309B, 311A and 311B, with any pair of the column strobe signals asserted to enable the corresponding column control registers to be simultaneously loaded. Also, as discussed above in reference to Figure 15, a single time-multiplexed column bus may be coupled to all the column control registers 309, 311 to enable sequential loading of selected column control registers in any order.

[0085] Figure 19 illustrates an exemplary timing of control signal assertions by the request decoder 601 of Figure 18. In the particular example shown, row activation requests 553, 555, 557 and 559 are received in respective t_{RRp} intervals, with each request being directed to a different quadrant in the exemplary order described in reference to sequence of Figures 16 and 17 (other row activation orders may be used). Thus, the request decoder 601 asserts the four row-register strobe signals ERSA, ERSB, ORSA, ORSB in respective t_{RRp} intervals, as shown, to transfer the bank and row address values received in the four activation requests to the address-specified row registers 305, 307. Assuming that the same pattern of row activation requests is received in subsequent t_{RR} intervals (i.e., same quadrant ordering, but arbitrary intra-quadrant bank address and row address), each of the four row-register strobe signals ERSA, ERSB, ORSA, ORSB may be asserted once per t_{RR} interval in round-robin fashion.

[0086] Still referring to Figure 19, column strobe signals ECS and OCS are asserted on partial t_{CC} intervals (i.e., t_{CCp}) as in the embodiment of Figure 9. As discussed, if the request decoder supports an arbitrary column control register loading sequence, four distinct column strobe signals may be generated by the request decoder and asserted in respective t_{CCp} intervals in any order. If the incoming column access requests specify the same quadrant access order in each t_{RR} cycle (or any group of t_{RR} cycles), each of the column strobe signals may be asserted in round-robin fashion once per t_{RR} interval or, in the case of the shared column strobe signals (ECS and OCS) shown in Figures 18 and 19, once per t_{CC} interval.

[0087] Figures 20A and 20B illustrate exemplary row requests that may be issued to the memory devices 100 and 530 described above to initiate row operations (e.g., row activation operations and precharge operations). More specifically, Figure 20A illustrates an exemplary ST-mode (single-threaded mode) row request that is issued when the memory devices 100, 530 are operated in a single-threaded

mode, and Figure 20B illustrates an exemplary MT-mode (micro-threaded-mode) row request issued when the memory devices are operated in a micro-threaded mode. In the particular embodiment shown, each row request is issued in two successive transfers (e.g., during odd and even phases of a clock signal or other timing signal) over a 12 bit request path (RQ0-RQ11) and therefore includes 24 bits. As shown, the ST-mode request includes a three-bit opcode formed by bits "OP," a three-bit bank address, BA0-BA2, and an eleven-bit row address, R0-R10. The opcode indicates the type of row operation to be performed (e.g., row activation or precharge), the bank address indicates which of the eight banks the row operation is directed to, and the row address indicates, at least in the case of a row activation operation, the row of the selected bank in which the operation is to be performed. The remaining seven bits of the ST-mode row request may be reserved (i.e., as indicated by the designation "rsrv") or used to carry information for controlling other functions within the memory device. The MT-mode row request of Figure 20B is substantially the same as the ST-mode row request, except that one of the reserved bits in the ST-mode request (e.g., the even phase bit transferred on request link RQ3) is optionally used to carry an additional bank address bit, BA3, thereby enabling selection of one of one of sixteen banks within the 16-bank memory device 530 of Figure 16. In alternative embodiments, row requests of Figures 20A and 20B may have different formats, different numbers of bits and may be transmitted in more or fewer transfers over a wider or narrower request path.

[0088] Figures 21A and 21B illustrate exemplary column requests that may be issued to the memory devices 100 and 530 described above to initiate column access operations (e.g., read operations and write operations). More specifically, Figure 21A, illustrates an exemplary ST-mode (single-threaded mode) column request that is issued when the memory devices 100, 530 are operated in a single-threaded mode, and Figure 21B illustrates an exemplary MT-mode (micro-threaded mode) column request issued when the memory devices are operated in a micro-threaded mode. In the embodiments shown, the ST-mode and MT-mode column requests are the same size as the corresponding ST-mode and MT-mode row requests (i.e., 24-bit requests formed by odd and even phase transfers over the 12 bit request path, RQ0-RQ11), but may be larger or smaller than the row requests in alternative embodiments. The ST-mode column request includes a five-bit opcode to specify the type of column access to be performed (e.g., read, write, masked write, etc.), a three-bit bank address, BC0-BC2, to specify one of eight open pages to be accessed (i.e., an open page for one of the eight banks), and a 6-bit column address, C4-C9, to specify one of 64 column locations (also called column offsets)

within the open page at which the specified column access operation is to be performed. Ten bits of the ST-mode column access request are reserved or allocated to other functions.

[0089] The MT-mode column request is similar to the ST-mode column access request except that the reserved bits of the ST-mode column access request are used to carry a second bank address BCy0-BCy2 and a second column address, Cy4-Cy9, the first bank address and first column address being carried in the same bits as the bank address and column address of the ST-mode column request, but designated BCx0-BCx2 and Cx4-Cx9. By this arrangement, each column request may carry the two distinct bank and column addresses used in the sixteen-bank memory device described in reference to Figures 16-19. In alternative embodiments, a second column address, but not a second bank address may be provided in the MT-mode column request (e.g., as in the embodiments described in reference to Figures 13-15) and in other alternative embodiments, a single column address and single bank address are provided per column access request (e.g., as in the embodiments described in reference to Figures 7-9). Also, in the embodiment described in reference to Figure 17, the higher density of row activation commands in the row activation pipeline consumes the request path bandwidth that might otherwise be used to transfer precharge commands. Accordingly, in the exemplary MT-mode column request of Figure 21A, one bit (i.e., odd phase bit transferred over the RQ11 link) is used to indicate whether an auto-precharge operation (AP) is to be performed at the conclusion of the indicated column access operation. In alternative embodiments, the ST-mode and/or MT-mode column requests may have different formats, different numbers of bits and may be transmitted in more or fewer transfers over a wider or narrower request path.

[0090] Figures 22 and 23 illustrate exemplary micro-threaded memory operations in a memory device 700 having a request interface 701 and data path interface 705A, 705B to interface with legacy request and data paths. Referring to Figure 23, the request interface receives row and column requests (including address components thereof) via a 19-bit request path 730 formed by a reset line (RESET), chip-select line (CS), row-address-strobe line (RAS), column-address-strobe line (CAS), write-enable line (WE), three bank address lines (BA[2:0]) and eleven address lines (A[10:0]). The data path interface is coupled to an external data path 732 formed by 32 data lines (DQ), four data-mask lines (DM), four read data strobe lines (RDQS), and four write data strobe lines (WDQS). The data-mask lines are used to carry respective mask bits during masked-write operations, with each mask bit indicating whether a corresponding byte carried on the DQ lines is to be written or not. The read data strobe lines carry read

data strobe signals output from the memory device to time reception of corresponding read data in the memory controller or other control device. The write data strobe lines carry write data strobe signals output from the memory controller (or other control device) to time reception of write data within the memory device 700. Each of the signal lines in the request path 730 and/or data path 732 may be single-ended or differential. Also, in alternative embodiments, different numbers and types of signals may be conducted via the request path 730 and/or data path 732.

[0091] In the embodiment of Figure 22, memory device 700 has substantially the same architecture as memory device 100 of Figure 1. That is, the memory device 700 has four quadrants, Q0-Q3, eight banks B0-B7 (each formed by a pair of A and B sub-banks), together with column decoders 703_0-703_3 and row decoders 713_0-713_3 that correspond to the column decoders 103_0-103_3 and row decoders 113_0-113_3 of Figure 1, though the banks may have different width and/or depth dimensions and the column and row decoders correspondingly revised to accommodate the differently-dimensioned banks. Also, signal paths 709_0-709_3, 711_0-711_3, 715_0-715_3, 717_0-717_3 and 719_0-719_3 correspond to the signal paths 109_0-109_3, 111_0-111_3, 115_0-115_3, 117_0-117_3 and 119_0-119_3 of Figure 1, though such signal paths may include different numbers of signal lines as necessary to accommodate the different bank dimensions. Further, as with the memory device 100, memory device 700 is assumed for purpose of description to be a DRAM device, but may be any type of memory device having multiple storage arrays that share addressing and/or data path resources in a manner that imposes timing constraints on sequential accesses directed to the different storage arrays. Also, the memory device 700 may have a different number of banks, sub-banks per bank and/or number of sub-banks per decoder-sharing group in alternative embodiments.

[0092] Turning to Figure 23, a row activation pipeline 731A, column access pipeline 731B, and precharge pipeline 731C illustrate an exemplary sequence of row activation requests, column access requests and precharge requests received in the request interface 701 via request path 730. Referring first to row activation pipeline 731A, a pair of row activation requests directed alternately to even and odd banks of the memory device 700, are received in each t_{RR} interval, starting with row activation requests 733 and 735. The request interface 701 responds to each pair of row activation requests by initiating row activation operations in the corresponding banks of the memory device 700.

[0093] A predetermined time after receipt of the row activation requests 733 and 735, a sequence of four multi-address, micro-threaded column access requests 737, 739, 741 and 743 are received, each pair of the column access requests being received in a respective t_{CC} interval and each individual column access request received within a given t_{CC} interval being directed the open page for the bank specified in a respective one of row activation requests 733 and 755. Referring to Figures 22 and 23, for example, column access request 737 is directed to the open page of bank B0 (opened in response to row activation request 733) and specifies accesses therein at column addresses 'a' and 'c.' Column access request 739, received in the same t_{CC} interval as column access request 737, is directed to the open page of bank B1 (opened in response to row activation request 735) and specifies accesses therein at column addresses 'e' and 'g.' Column access requests 741 and 743 are received in a second t_{CC} interval, with column access request 741 directed to columns 'b' and 'd' of the open page of bank B0, and column access request 743 directed to columns 'f' and 'h' of the open page of bank B1. The open pages are closed in precharge operations requested in precharge requests 745 and 747. In the particular embodiment shown, each request interval is 1 ns (i.e., requests are transferred over the individual signal lines of path 730 at 1Gb/s), so that an 8 ns t_{RR} constraint and a 4 ns t_{CC} constraint are assumed. Also, the t_{RC} constraint is assumed to be 40 ns, so that activation requests directed to the rows specified in requests 733 and 735 are not issued again until after a 40nS interval has elapsed. Other request transfer rates may be used and different t_{RR} , t_{CC} and/or t_{RC} constraints may apply in alternative embodiments.

[0094] The request decoder responds to the incoming column access requests 737, 739, 741 and 743 by issuing signals to the appropriate column decoders to perform the access operations (e.g., read or write operations), with data that corresponds to each column access being transferred via DQ links DQ[31:0] over a respective partial t_{CC} interval (t_{CCp}). More specifically, as shown in detail view 738, each t_{CC} envelope is spatially and temporally subdivided so that, over the t_{CCp} interval starting at 736, data that corresponds to column 'a' of column access request 737 (i.e., data being written to column 'a' or read from column 'a') is transferred via a first portion of the DQ links, DQ[31:16], and data that corresponds to column 'c' of column access request 737 is transferred via a second portion of the DQ links, DQ[15:0]. Similarly, during the next t_{CCp} interval, data that corresponds to columns 'e' and 'g' of column access request 739 is transferred via DQ links, DQ[31:16] and DQ[15:0], respectively. Thus, over the t_{CC} interval starting at 736, data transfers that correspond to four different micro-threaded column access transactions are carried out. In the exemplary embodiment shown, data is transferred over each of the DQ links at 2Gb/s, so that four bits per link are transferred over each 2 ns t_{CCp} interval.

Consequently, an 8-byte column transaction granularity is achieved in a device otherwise having a 32-byte t_{CC} envelope. During the t_{CC} interval that follows the Ce/Cg data transfer, four additional data transfers are carried out in response to the micro-threaded column access requests specified in requests 741 and 743. That is, during a first t_{CCp} interval, data that corresponds to columns 'b' and 'd' of column access request 741 is transferred via DQ links DQ[31:16] and DQ[15:0], respectively, and during the next t_{CCp} interval, data that corresponds to columns 'f' and 'h' of column access request 743 is transferred via DQ links DQ[31:16] and DQ[15:0], respectively. Thus, the total amount of data transferred over the t_{RR} interval starting at 736 is 64 bytes, with one half of the total t_{RR} envelope being allocated to data transfer for each of the rows activated in response to row activation requests 733 and 735. That is, the 64-byte t_{RR} envelope is temporally subdivided between the rows activated in response to requests 733 and 735 to achieve a 32-byte row transaction granularity.

[0095] Depending on the number of bits required to specify a column address within the memory device of Figure 23, the 19-bit request size (i.e., established by the width of request path 730) may be insufficient to carry two complete column addresses. In one embodiment, this circumstance is overcome by storing a set of offset values within the memory device 700 and including an offset select value within incoming multi-address column access requests to select one of the pre-stored offset values. The selected offset value may then be used directly as the second column address or may be combined with a fully specified column address to form a relative column address. For example, in the exemplary format shown at 740, column access request 737 includes an operation specifier, "Col Cmd," that specifies the type of column access (e.g., read, write, masked write, etc.); a bank address, "Bank Addr," that specifies the bank to which the column access is directed; a fully-specified column address, "Col Addr1," that specifies a first column address (e.g., column 'a' in request 737); and an offset select value, "OSEL," that specifies a pre-stored offset value to be summed (or otherwise arithmetically or logically combined) with the fully-specified column address to produce the second column address. That is, as shown at 742, the offset select value may be applied to the control input of a multiplexer 744 to select one of n offset values, Coff0-Coff(n-1), to be summed with column address, Ca, in adder 746, thereby producing the second column address, Cc.

[0096] Figure 24 illustrates a more detailed example of address information provided, via lines BA[2:0] and A[10:0] of request path 730, as part of a column access request. The BA[2:0] lines carry a three-bit bank address specifying one of eight banks, while address lines A9 and A7-A2 carry a fully-

specified, seven-bit column address, "Col Addr1." Address lines A1 and A0 carry a two-bit offset select value which is applied to select one of four column addresses, Coff0-Coff3 to be added to the fully-specified column address. The resulting relative column address constitutes the second column address, "Col Addr2," specified in the column access request. The signal carried on address line A8 indicates whether a normal precharge or auto-precharge is to be carried out (e.g., the auto-precharge occurring at the conclusion of the specified column access operation), and the signal carried on address line A10 is reserved. Different signal encodings on the bank address lines and address lines or other lines of the request path may be used in alternative embodiments. Also, more or fewer column offsets may be stored to enable a larger selection of column offset values. For example, bit A10 may be used to carry the most significant bit of an offset select value, thereby enabling selection of one of eight column offset values.

[0097] Figure 25 illustrates exemplary configuration information that may be provided in conjunction with a load mode register command issued to the memory device 700 of Figure 22. The load mode register command may be specified, for example, by driving the CS, RAS, CAS, and WE lines of the request path low during a request interval. As shown, the signals carried on lines BA[2:0] indicate the nature of the operation to be performed, with '000' and '001' codes indicating that bits A[10:0] (i.e., the signals carried on lines A[10:0]) are to be loaded into a device mode register or extended mode register, respectively, (e.g., to program device output latency, burst length and/or other device operating characteristics), codes '010-110' being reserved or used for other functions, and code '111' indicating that bits A[10:0] are to be loaded into a micro-thread mode register (i.e., uMode register). In a load to the micro-thread mode register, bits A9 and A7-A2 form a column offset value to be loaded into one of four column offset fields of the micro-thread mode register, and bits A1 and A0 indicate which of the four column offset fields, Coff0-Coff3, is to be loaded. Bits A8 and A10 are coded to one of four values (00, 01, 10, 11) to specify either a single-threaded mode (ST) within the memory device; a two-by-two micro-threaded mode (MT2x2) in which a single column address is provided in each micro-threaded column access request to enable two-way partitioning of the t_{CC} envelope and with the micro-threaded column accesses in each t_{RR} interval directed to two different banks(e.g., to enable micro-threading as described in reference to Figures 7-9); a four-by-two micro-threaded mode (MT4x2) in which two column address are provided in each micro-threaded column access request to enable four-way partitioning of the t_{CC} envelope and with the micro-threaded column access in each t_{RR} interval directed to two different banks (e.g., as described in reference to Figure 23); and a four-by-four micro-

threaded mode (MT4x4) in which four row activation requests are received per t_{RR} interval to enable each of four dual-address column access requests to be directed to a different bank, thereby achieving four-way partitioning of each t_{CC} interval and enabling four different banks to be accessed in each t_{RR} interval (e.g., as described in reference to Figure 17).

[0098] Figures 26 and 27 illustrate four-by-four micro-threaded memory operations in a memory device 750 having the data path interfaces 705A and 705B described in reference to Figures 22 and 23 to interface with a legacy data path, and having a request interface 751 that is substantially similar to the request interface 701, except that an additional bank address input is provided to receive a fourth bank address bit. By this arrangement, a sequence of row activation requests specifying a bank in each of the four quadrants (Q0-Q3) of the memory device may be received within a single t_{RR} interval, thereby enabling each of four dual-address column access requests to be directed to a respective one of the four quadrants. Because unique bank, row and column addresses may be delivered to the address decoders (i.e., column decoders 703 and row decoders 713) for each quadrant, the storage arrays in each quadrant are effectively converted from sub-banks to banks, thereby yielding a sixteen bank architecture having banks B0-B15 as shown in Figure 26. As in the other memory device embodiments discussed above, memory device 750 may have more or fewer storage arrays in alternative embodiments yielding correspondingly more or fewer banks. Also, any of the sixteen banks may include any number of constituent sub-banks.

[0099] Referring to Figure 27, the row activation pipeline 755A is more densely loaded than in the embodiment described in reference to Figure 23 to deliver row activation requests 763, 765, 767 and 769 directed to banks with each of the four quadrants of the memory device 750 in a single t_{RR} interval. That is, the t_{RR} interval is sub-divided into four t_{RRp} intervals, with a row activation request being received in each. In the specific example shown in Figures 26 and 27, rows 'w', 'y', 'x' and 'z' are activated one after another in banks B0, B1, B8 and B9, though rows may be activated in each of the four quadrants in different order in subsequent transactions or in alternative embodiments.

[0100] Referring to column access pipeline 755B, a predetermined time after the first row activation request 763 is received, a pair of dual-address micro-threaded column access requests 771, 773 are received one after another in a first t_{CC} interval. The first column access request 771 is directed to the same bank (B0) as the first row activation request 763 and specifies a pair of column locations 'a'

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and 'e' (e.g., a fully-specified column address and offset select value as discussed in reference to Figures 23-25) to be accessed one after another in successive t_{CC} intervals. The second column access request 773 is similarly directed to the same bank (B1) as the second row activation request 765 and specifies a pair of column locations 'c' and 'g' to be accessed one after another in successive t_{CC} intervals. Column data that corresponds to the first column address 'a' of column access request 771 is transferred a predetermined time later over the t_{CCp} interval starting at 770 and via the subset of DQ links, DQ[31:16] coupled to the data path interface 705A for banks B0-B7. Column data that corresponds to the first column address 'e' of column access request 773 is transferred via the same DQ link subset, DQ[31:16], over the t_{CCp} interval that starts at 772 (i.e., over the second half of the t_{CC} interval that starts at 770). During the succeeding t_{CC} interval, transfers from the open pages are repeated in respective t_{CCp} intervals to transfer B0, column 'e' data and B1, column 'g' data. Thus, data for the two column access requests directed to low order banks, B0-B7, are transferred in interleaved fashion (i.e., B0-Ca, B1-Cc, B0-Ce, B1-Cg) in respective t_{CCp} intervals and over a subset of the DQ links. Data for the two column access requests 775, 777 directed to high-order banks, B8-B15, are similarly transferred in interleaved fashion (i.e., B8-Cb, B9-Cd, B8-Cf, B9-Ch) in respective t_{CCp} intervals and over the DQ link subset, DQ[15:0]. Overall, the entire data transfer sequence in response to the column access requests 775, 777 occurs over a t_{RR} interval that starts at 772. In the embodiment of Figure 27, the data transferred in response to column access requests 777 and 775 is delayed by a t_{CC} interval relative to the data transferred in response to column access requests 771, 773 due to the receipt of the column access requests 777 and 775 one t_{CC} interval after requests 771 and 773. In an alternative embodiment, the data to be transferred in response to the earlier-received pair of column access requests may be buffered, then output over the same t_{RR} interval as the data transferred in response to the later-received pair of column access requests. In either case, because each 32-byte t_{CC} envelope is spatially halved and temporally halved to accommodate four micro-threaded column access transactions, an 8-byte column transaction granularity is achieved. Also, because each 64-byte t_{RR} envelope is subdivided to enable data transfer to or from four different banks, a sixteen byte row transaction granularity is achieved.

[0101] Still referring to Figures 26 and 27, the relative addressing scheme discussed in reference to Figures 23-25 may be used to convey the second column address in each of the column access requests 771, 773, 775, 777. Also, because an additional bank address bit is provided via line BA[3] of signal path 756, the operation encoding shown in the bank address field of Figure 25 may be different and/or include additional or different operations. Further, because bandwidth for specifying precharge

operations is consumed by the more densely loaded row request pipeline 755A, precharge operations may be specified by the auto-precharge option indicated in Figure 24 (i.e., A8=1). Such precharge operations are shown in cross-hatched request intervals in the precharge pipeline of 755C to provide an example of when such operations are carried out, but are specified in the corresponding column access requests 771, 773, 775 and 777, rather than in explicit precharge requests.

[0102] Figure 28 illustrates an exemplary timing signal arrangement that may be used to convey the fourth bank address bit used in the embodiments of Figures 26 and 27, thereby obviating the added BA signal link and enabling four-by-four micro-threaded operation using the legacy signal path 730 of Figure 23. In the particular example shown, instead of using a full-frequency timing signal 790 (i.e., clock signal or strobe signal) to time request transfer over the request path, a reduced-frequency timing signal 792 that exhibits alternating rising and falling edges at the start of every second request interval is used to convey the least significant bank address bit, BA[0], while the BA[2:0] signal lines are used to convey the most significant bank address bits BA[3:1]. If the first quadrant to be accessed in a given t_{RR} interval is an even quadrant (Q0 or Q2), the timing signal 792 is output with a rising edge that arrives at the memory device synchronously with respect to the corresponding row activation request (or column access request) to convey BA[0] = '0.' If the first quadrant to be accessed is an odd quadrant (Q1 or Q3), the timing signal is output with a falling edge that arrives at the memory device synchronously with respect to the corresponding row activation request to convey BA[0] = '1.' In the embodiment of Figures 26 and 27, the least significant bit of the bank address toggles with each successive row activation request (or column access request), so that edge of the timing signal that corresponds to the second row activation request (or column access request) within a given t_{RR} interval will select the appropriate odd or even bank set; the opposite bank set selected by the edge of the timing signal that corresponds to the first row activation request. In the particular example shown in Figure 28, a portion of the row request pipeline 755A containing row activation requests 763, 765, 767 and 769 is shown in edge alignment with the timing signal 792. The initial rising edge transition of the timing signal 792 indicates that BA[0] is a 0 so that, by delivering address values BA[3:1]=000 in row activation request 763 (i.e., via lines BA[2:0] of the request path), bank B0 is specified by the row activation request 763. The subsequent falling edge transition of the timing signal coincides with the arrival of row activation request 765 and indicates that BA[0] = 1. Accordingly, by delivering address values BA[3:1]=000 in row activation request 765, bank B1 is specified. Banks B8 and B9 are similarly specified in row activation requests 767 and 769 by specifying BA[3:1]=100 in conjunction with a rising-edge transition and falling-

edge transition, respectively, of timing signal 792. A clock recovery circuit such as phase-locked loop 794 may be used to generate an internal timing signal 795 that is phase aligned with transitions of timing signal 792 but having a frequency that corresponds, for example, to the frequency of signal 790. The internal timing signal 795, which may itself be a clock signal or strobe signal, may then be used to control sampling of signals conveyed on the request path in order to capture a new request in each request interval.

[0103] Figure 29 illustrates an embodiment of a memory system 800 that includes a memory controller 801 and at least one micro-threaded memory device 803. The micro-threaded memory device 803 may be implemented according to any of the above-described embodiments, but for present purpose is assumed to have at least two data path interfaces, DQA and DQB, for accessing respective sets of eight storage banks (i.e., DQA is used to transfer data to and from banks B0-B7, and DQB is used to transfer data to and from banks B8-B15), and a request interface, RQ, for receiving row and column requests and controlling execution of the requested row and column operations. The storage banks themselves are additionally organized in quadrants, Q0-Q3, as described above in reference to memory devices 100, 530, 700 and 750, though other storage bank organizations may be used. The DQA and DQB data path interfaces are coupled to the memory controller via respective subsets of DQ links 802a and 802b within data path 802, and the request interface is coupled to the memory controller via a request path 804. In the embodiment shown, the request path 804 is formed by a set of point-to-point links, while the data path 802 is formed by multi-drop links (i.e., data path interfaces of one or more other memory devices may be coupled to the data path or a subset of the DQ links thereof). In alternative embodiments, the request path 804 may be a multi-drop path coupled to request interfaces of one or more additional memory devices (not shown) and/or the data path 802 may be formed by point-to-point links between the memory controller 801 and memory device 803. Also, the memory device 803 may be one of multiple memory devices disposed on a memory module and coupled to a buffering circuit via a set of point-to-point links (or a multi-drop path). The buffering circuit may receive requests and/or data directed to any of the memory devices on the memory module, and retransmit the requests and/or data to the target memory device via the corresponding set of point-to-point links.

[0104] The memory controller 801 includes a read transaction queue 811 (RTQ), write transaction queue 815 (WTQ), read data buffer 819, queue control logic 817 and host interface 810. During an initialization or reconfiguration operation, system configuration requests are delivered to the memory

controller 801 which, in turn, programs the memory device 803 (including other memory devices if present) to operate in the specified mode, for example, by issuing programming information via request path 804, data path 802 and/or one or more other paths between the memory controller 801 and the memory device 803 (e.g., a sideband path, not shown). In one embodiment, for example, the memory controller 801 or other device may read a configuration memory associated with memory device 803 (e.g., a serial presence detect (SPD) or the like) to determine operating characteristics, constraints and modes of the memory device 803 (e.g., in the case of a dual-inline memory module (DIMM) or the like having the memory device 803 and one or more other like devices mounted thereto, the tCC, tRR and/or tRC constraints for memory device 803 may be recorded within the configuration memory), then pass such information back to a processor or other host. The processor may process such information (e.g., as part of basic input-output service (BIOS) code execution), then program the memory controller 801 to establish a desired memory configuration, including instructing the memory controller 801 to program the memory device 803. For example, the memory controller 801 may be instructed to issue micro-thread-mode register set commands as described in reference to Figure 25 to program the memory device 803 for single-threaded operating mode, or any of the micro-threaded operating modes described above (e.g., the MT2x2, MT4x2 and MT4x4 operating modes described above). The memory controller 801 may also include one or more internal configuration registers that are programmed in response to instructions received via host interface 810 to establish single-threaded control mode or micro-threaded control mode.

[0105] After the memory device 803 and memory controller 801 have been configured (or re-configured in the case where operating modes may be switched during run-time operation), one or more host devices such as a general purposes processor, graphics processor, network processor, and/or direct memory access (DMA) controller may issue memory access requests to the memory controller 801, including memory read requests, memory write requests, masked write requests, read-modify-write requests and so forth. The incoming memory access requests are received in the queue control logic 817 which, in turn, queues the requests in either the read transaction queue 811 or write transaction queue 815 according to whether they specify read or write access.

[0106] The read transaction queue (RTQ) 811 includes four sets of read queues, Qr0/2/4/6, Qr1/3/5/7, Qr8/10/12/14 and Qr9/11/13/15 that correspond to four quadrants of storage banks within the memory device 803. When read requests are received within the queue control logic 817, the

queue control logic 817 determines, based on address information included with the request, the memory device and storage bank to which the request is directed and stores the request in the corresponding read queue. For example, requests directed to bank 0 of the memory device 803 are stored in read queue Qr0, requests directed to bank 8 are stored in read queue Qr8 and so forth. By organizing the read requests within the read queues in this manner, the memory controller 801 is able to issue row activation and column access requests in an order that supports micro-threaded memory access transactions within the memory device 803. For example, assuming that each of the four sets of read queues includes at least one memory read request, then the queue control logic 817 may issue respective enable signals (i.e., EN_1, EN_2, EN_3, EN_4, only one of which is shown in Figure 29) to first stage multiplexers 823 to control the selection of one of the four read queues from each set during a given t_{RR} interval. The queue control logic 817 additionally issues a selection-enable signal (ENp) to second stage multiplexer 825 to select one of the four first stage multiplexers 823 to output a read request from a selected read queue during each t_{RRp} interval or, in the case of column access requests, during each t_{CCp} interval. That is, the queue control logic 817 may transition the ENp signal from one state to another at the end of each t_{RRp} or t_{CCp} interval to select another of the first stage multiplexers 823, thereby enabling requests to be directed to each of the four quadrants of the memory device in round robin fashion. The first stage multiplexer 825 outputs requests to read/write multiplexer 827 which passes requests from either the read transaction queue 811 or write transaction queue 815 onto request path 804 in response to a control signal (R/W) from the queue control logic 817. Read data output from the memory device 803 in response to the micro-threaded read requests are delivered to the memory controller 801 via data path 802 and buffered in a read data buffer 819. The queue control logic 817 associates the read data with corresponding host read requests and outputs the read data to the requesting host device via the host interface.

[0107] The write transaction queue 815 includes four sets of write queues (i.e., Qw0/2/4/6, Qw1/3/5/7, Qw8/10/12/14 and Qw9/11/13/15), first stage multiplexers 833 and second stage multiplexer 835, each of which operate in generally the same manner as their counterparts in the read transaction queue 811, except that the write queues store and output write data in addition to write requests. Thus, write requests may be issued to each of the four quadrants of the memory device 803 on even t_{RRp} or t_{CCp} intervals to initiate micro-threaded write transactions therein.

Embodiments in Computer-Readable Media

[0108] It should be noted that the various circuits disclosed herein (e.g., memory devices or component circuits thereof) may be described using computer aided design tools and expressed (or represented), as data and/or instructions embodied in various computer-readable media, in terms of their behavioral, register transfer, logic component, transistor, layout geometries, and/or other characteristics. Formats of files and other objects in which such circuit expressions may be implemented include, but are not limited to, formats supporting behavioral languages such as C, Verilog, and HLDL, formats supporting register level description languages like RTL, and formats supporting geometry description languages such as GDSII, GDSIII, GDSIV, CIF, MEBES and any other suitable formats and languages. Computer-readable media in which such formatted data and/or instructions may be embodied include, but are not limited to, non-volatile storage media in various forms (e.g., optical, magnetic or semiconductor storage media) and carrier waves that may be used to transfer such formatted data and/or instructions through wireless, optical, or wired signaling media or any combination thereof. Examples of transfers of such formatted data and/or instructions by carrier waves include, but are not limited to, transfers (uploads, downloads, e-mail, etc.) over the Internet and/or other computer networks via one or more data transfer protocols (e.g., HTTP, FTP, SMTP, etc.).

[0109] When received within a computer system via one or more computer-readable media, such data and/or instruction-based expressions of the above described circuits may be processed by a processing entity (e.g., one or more processors) within the computer system in conjunction with execution of one or more other computer programs including, without limitation, net-list generation programs, place and route programs and the like, to generate a representation or image of a physical manifestation of such circuits. Such representation or image may thereafter be used in device fabrication, for example, by enabling generation of one or more masks that are used to form various components of the circuits in a device fabrication process.

[0110] The section headings provided in this detailed description are for convenience of reference only, and in no way define, limit, construe or describe the scope or extent of such sections. Also, while the invention has been described with reference to specific embodiments thereof, it will be evident that various modifications and changes may be made thereto without departing from the broader spirit and

scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than restrictive sense.

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CLAIMS

What is claimed is:

1. (Original) A memory controller to control a memory device having storage arrays each including rows of storage cells, the storage arrays arranged into at least first and second bank groups, the storage arrays to be accessed using row activation commands and memory access read commands, where a minimum time interval that specifies a minimum number of clock cycles must elapse between successive read accesses to an open row of storage cells in a selected one of the storage arrays, the memory controller comprising:

at least one transaction queue to queue the memory access read commands, the memory controller to identify the bank group associated with each memory access read command; and

circuitry responsive to content of the at least one transaction queue to transmit the queued commands to the memory device;

where the memory controller is to send the memory access read commands in a manner such that, for an open first row in a storage array in the first bank group and a concurrently-open second row in a storage array in the second bank group and during respective portions of a first time interval, a first one of the memory access read commands can be sent to a storage array in the first bank group, and a second one of the memory access read commands can be sent to the storage array in the second bank group, where the first time interval is less than twice the minimum time interval.

ABSTRACT OF THE DISCLOSURE

A micro-threaded memory device. A plurality of storage banks are provided, each including a plurality of rows of storage cells and having an access restriction in that at least a minimum access time interval must transpire between successive accesses to a given row of the storage cells. Transfer control circuitry is provided to transfer a first amount of data between the plurality of storage banks and an external signal path in response to a first memory access request, the first amount of data being less than a product of the external signal path bandwidth and the minimum access time interval.

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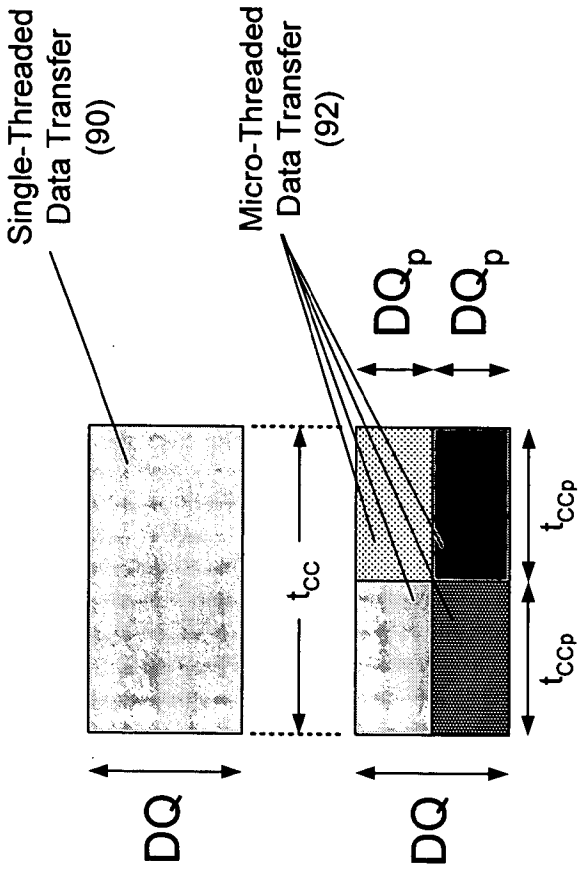

Single-Threaded
Data Transfer
(90)
Micro-Threaded
Data Transfer
(92)
DQp
DQp
tCC
tCCp
tCCp
DQ
DQ

FIG. 1

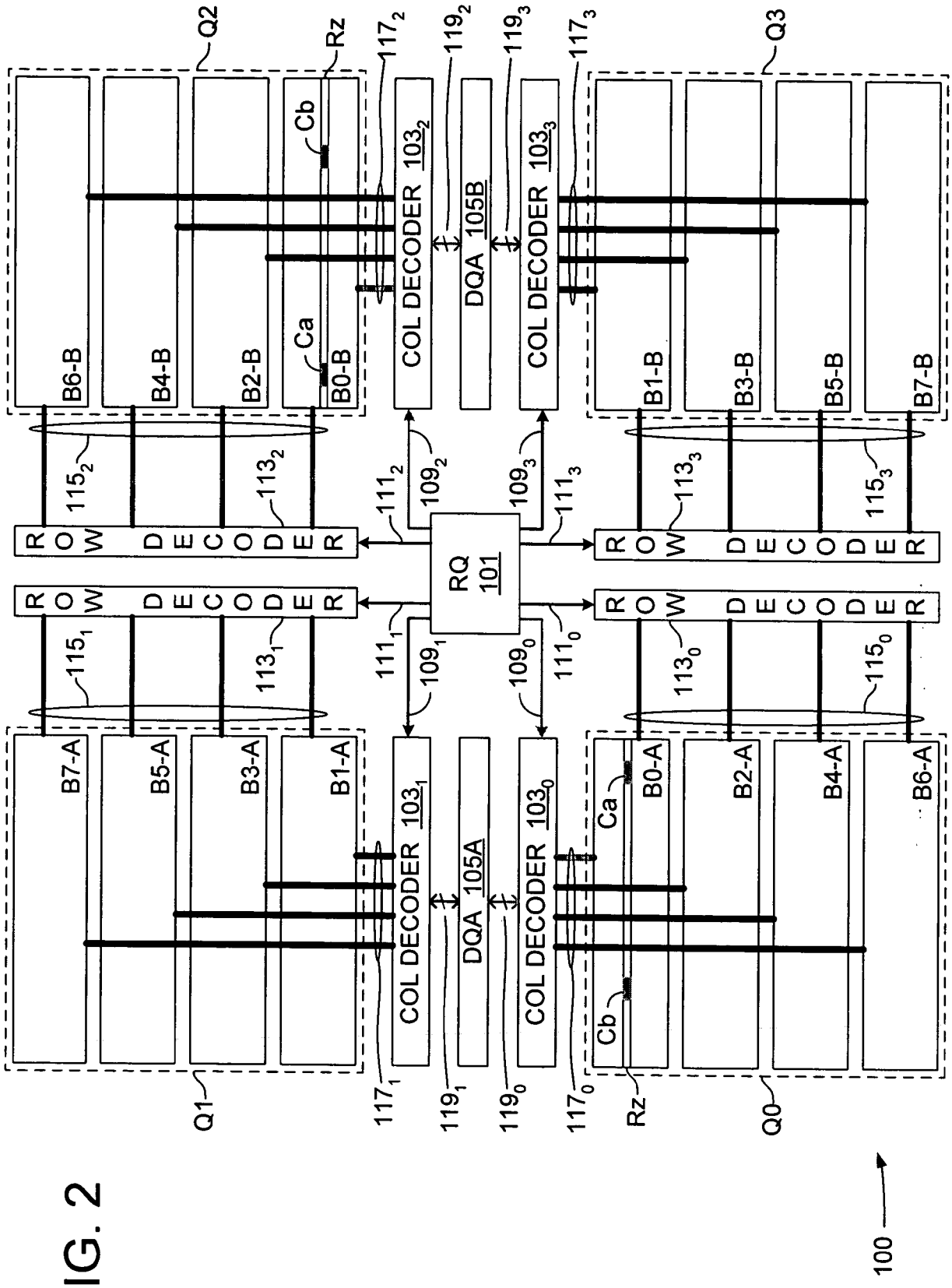

Q2
Rz
Cb
Ca
B6-B
B4-B
B2-B
B0-B
COL DECODER 103₂
DQA 105B
COL DECODER 103₃
Q3
B1-B
B3-B
B5-B
B7-B
RQ 101
ROW DECODER
Q1
B7-A
B5-A
B3-A
B1-A
COL DECODER 103₁
DQA 105A
COL DECODER 103₀
B0-A
B2-A
B4-A
B6-A
Q0
100

FIG. 2

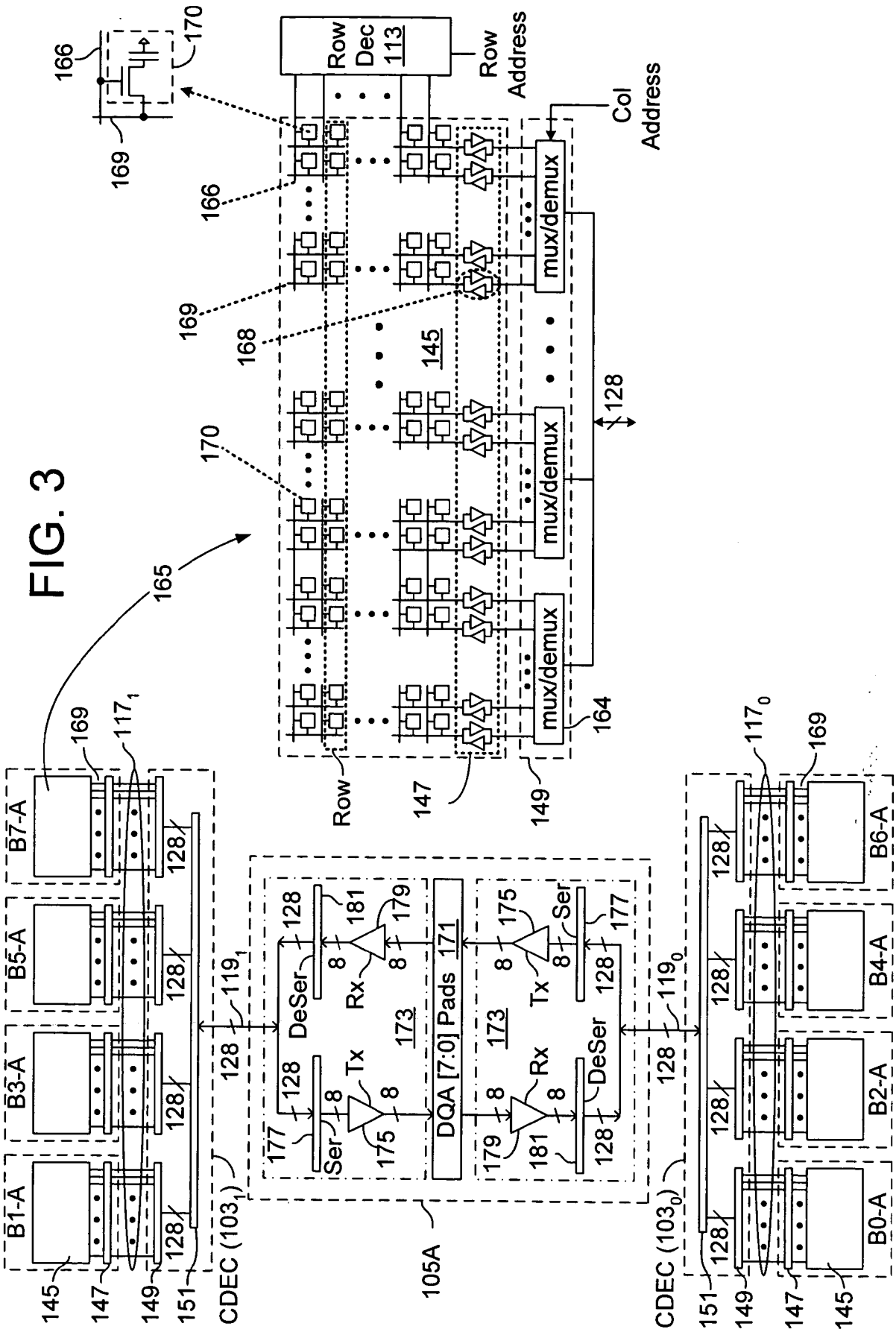
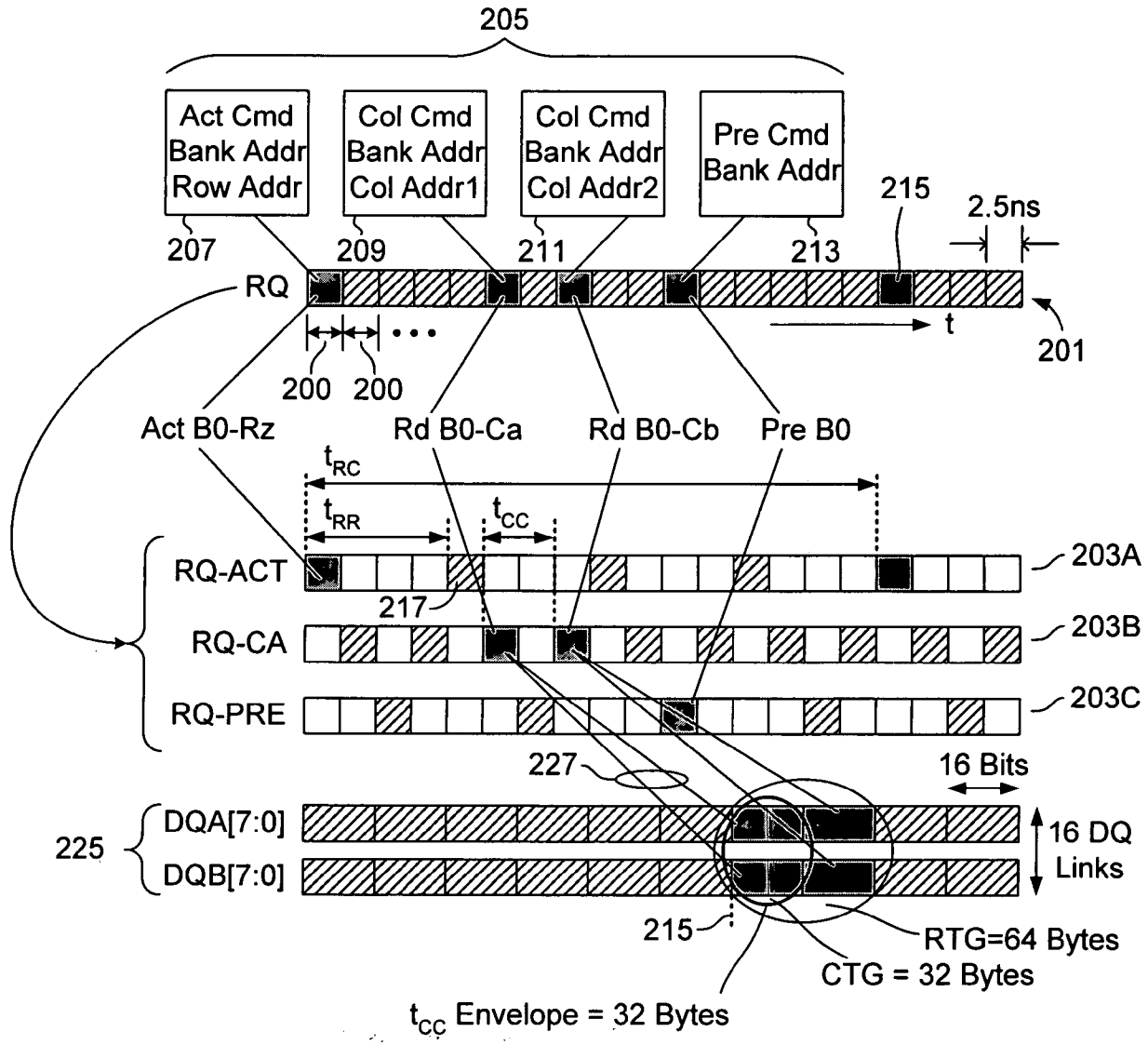

FIG. 3
Row Dec 113
Row Address
Col Address
mux/demux
DeSer
Ser
Tx
Rx
DQA [7:0] Pads 171
CDEC (103$_1$)
CDEC (103$_0$)
105A
B7-A
B5-A
B3-A
B1-A
B6-A
B4-A
B2-A
B0-A
Row
145
147
149
151
164
165
166
168
169
170
173
175
177
179
181

FIG. 4



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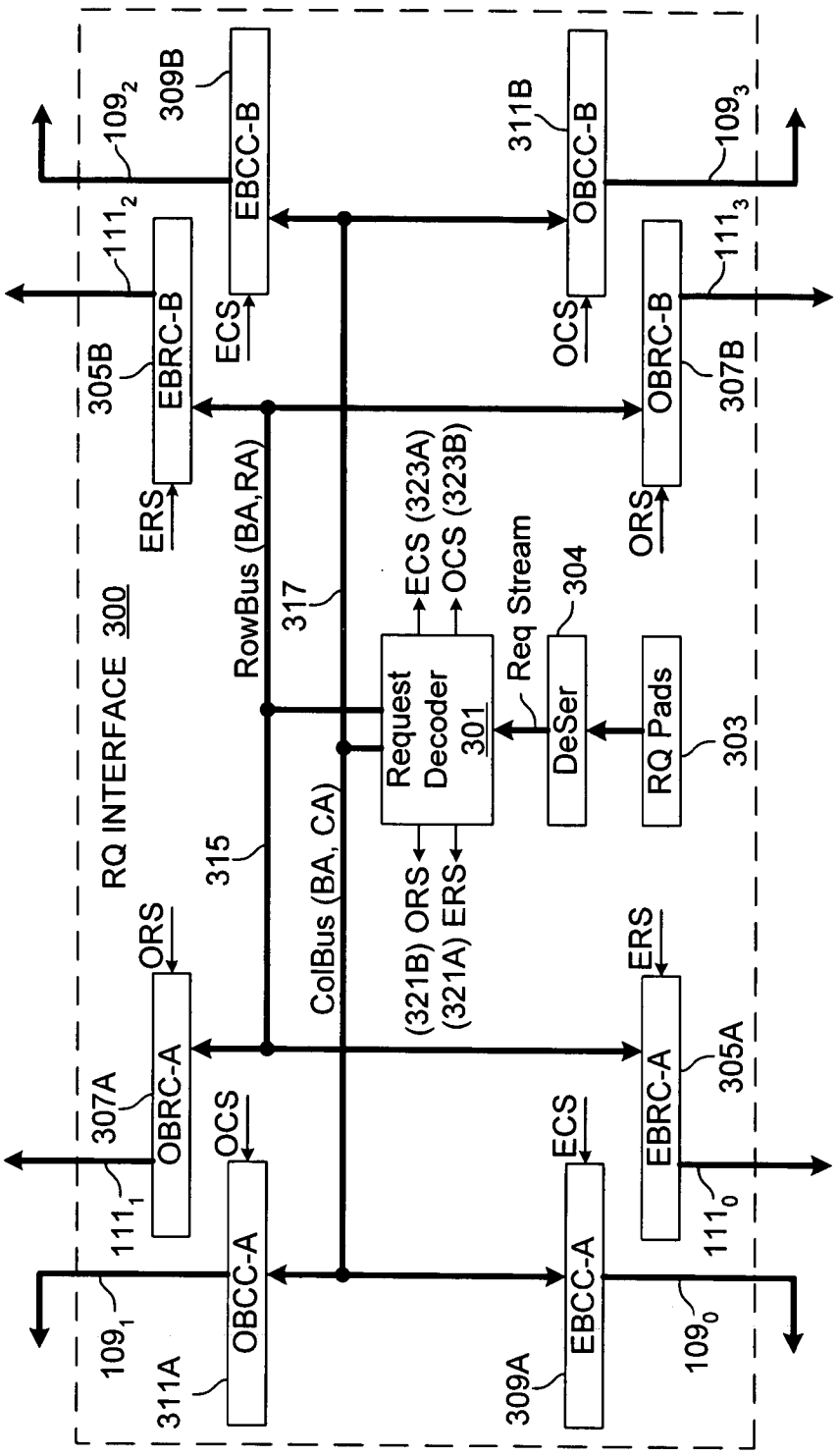

RQ INTERFACE 300
RowBus (BA,RA)
ColBus (BA, CA)
317
315
Request Decoder 301
Req Stream
304
DeSer
RQ Pads
303
ECS (323A)
OCS (323B)
(321B) ORS
(321A) ERS
EBRC-B
EBCC-B
OBRC-B
OBCC-B
EBRC-A
EBCC-A
OBRC-A
OBCC-A
305B
309B
307B
311B
305A
309A
307A
311A
ERS
ECS
ORS
OCS
111_2
109_2
111_3
109_3
111_1
109_1
111_0
109_0

FIG. 5

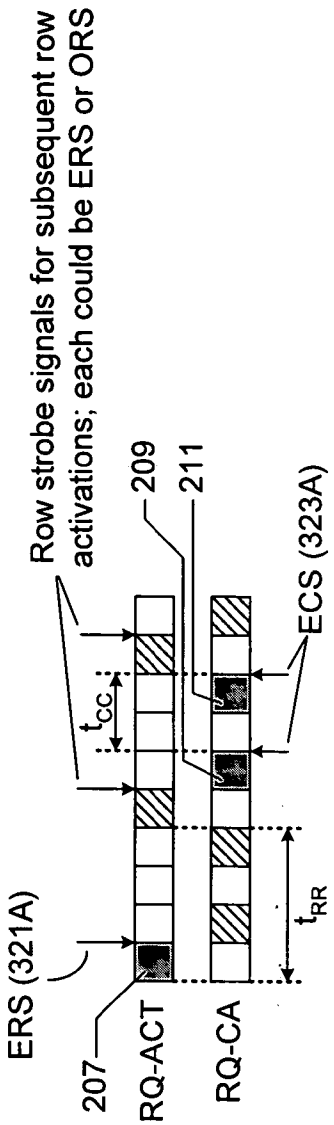

Row strobe signals for subsequent row activations; each could be ERS or ORS
209
211
ECS (323A)
t_{CC}
t_{RR}
ERS (321A)
207
RQ-ACT
RQ-CA

FIG. 6

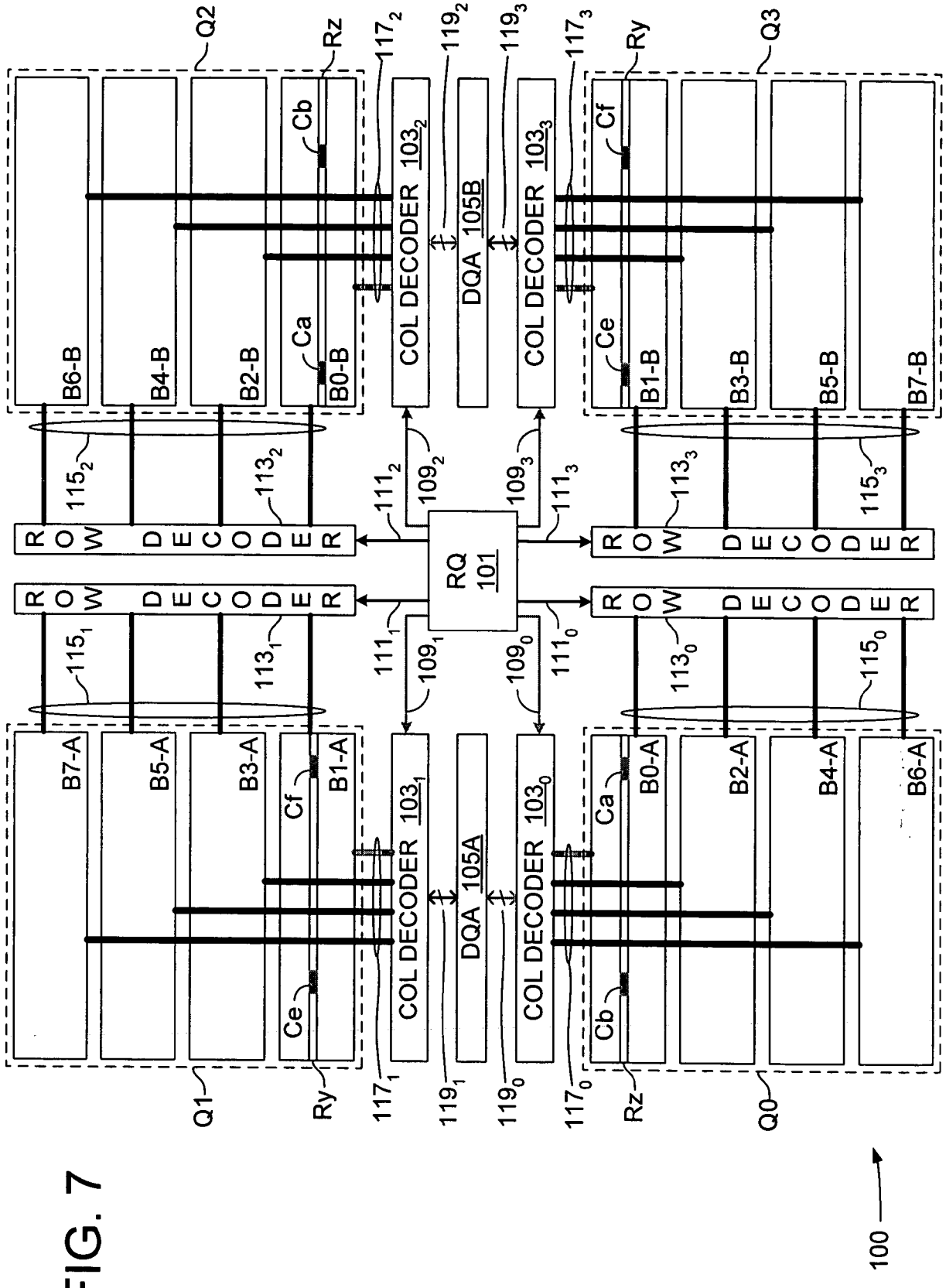
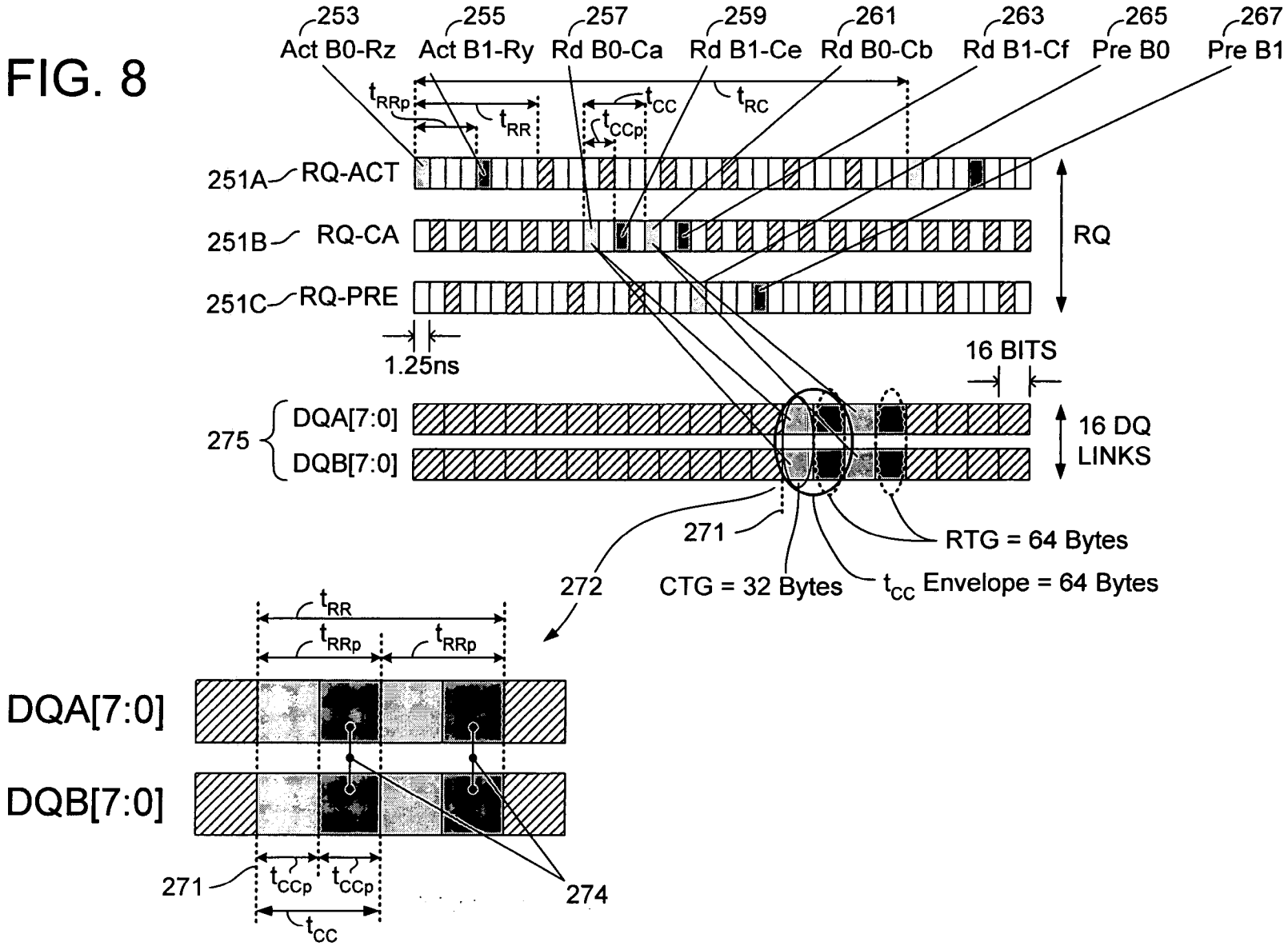

Q2
Rz
Cb
Ca
B6-B
B4-B
B2-B
B0-B
COL DECODER 103₂
DQA 105B
COL DECODER 103₃
Ry
Cf
Ce
B1-B
B3-B
B5-B
B7-B
Q3
RQ 101
ROW DECODER
Q1
Ry
Ce
Cf
B7-A
B5-A
B3-A
B1-A
COL DECODER 103₁
DQA 105A
COL DECODER 103₀
Rz
Cb
Ca
B0-A
B2-A
B4-A
B6-A
Q0
100

FIG. 7

FIG. 8



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FIG. 9

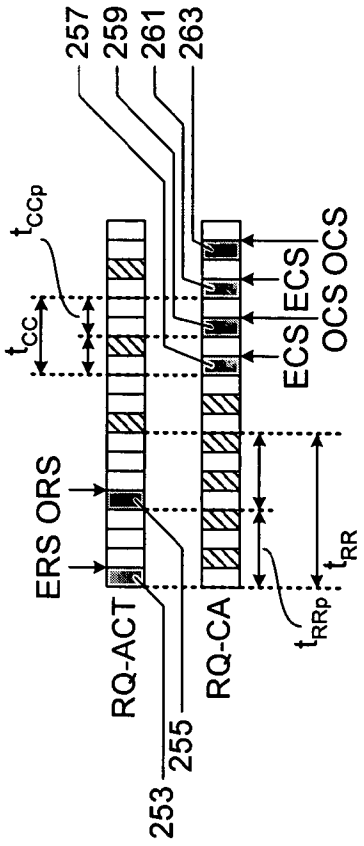

257
259
261
263
t_{CCp}
t_{CC}
ECS
ECS
OCS
OCS
ERS
ORS
RQ-ACT
RQ-CA
t_{RR}
t_{RRp}
253
255

FIG. 10

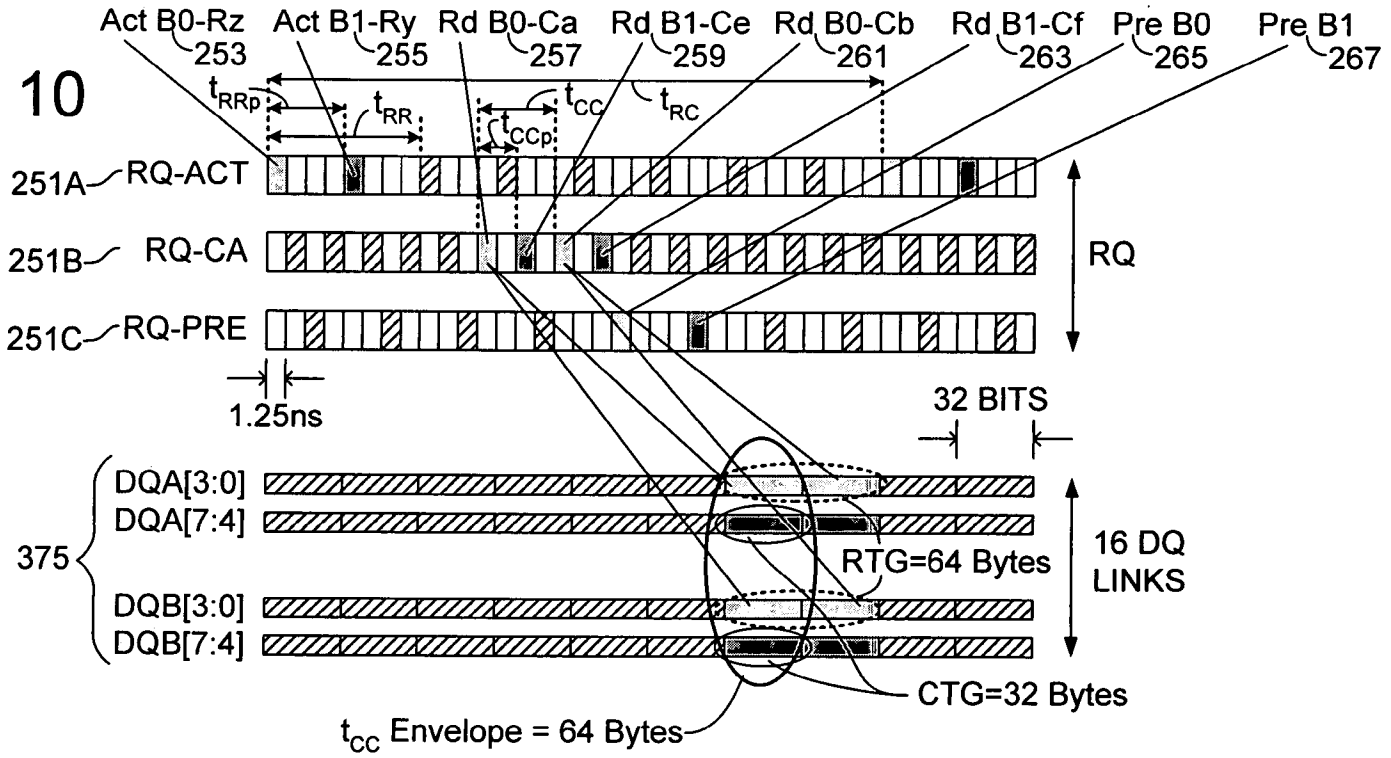
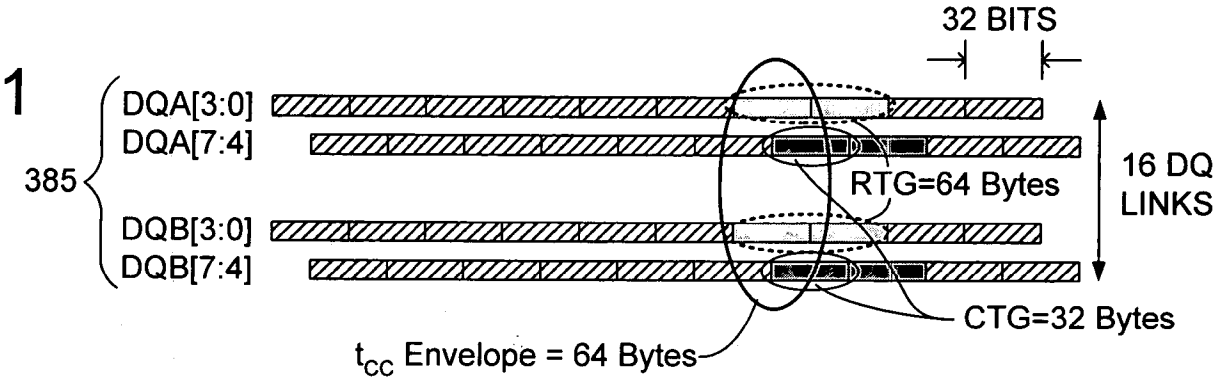


FIG. 11



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FIG. 12A

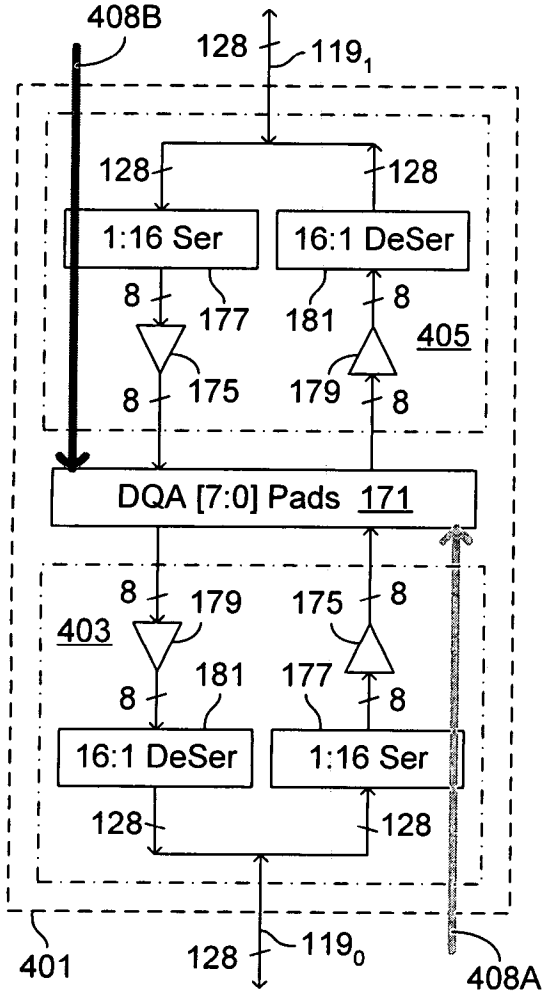
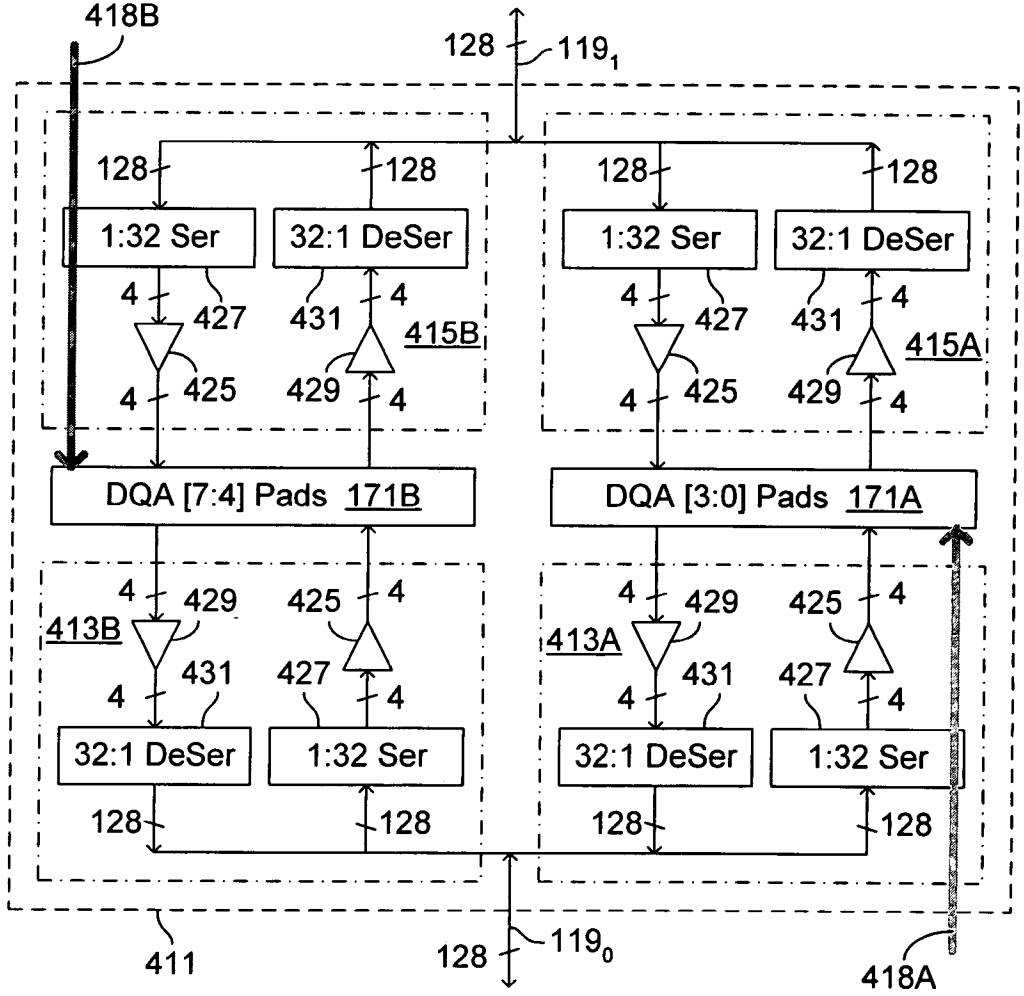


FIG. 12B



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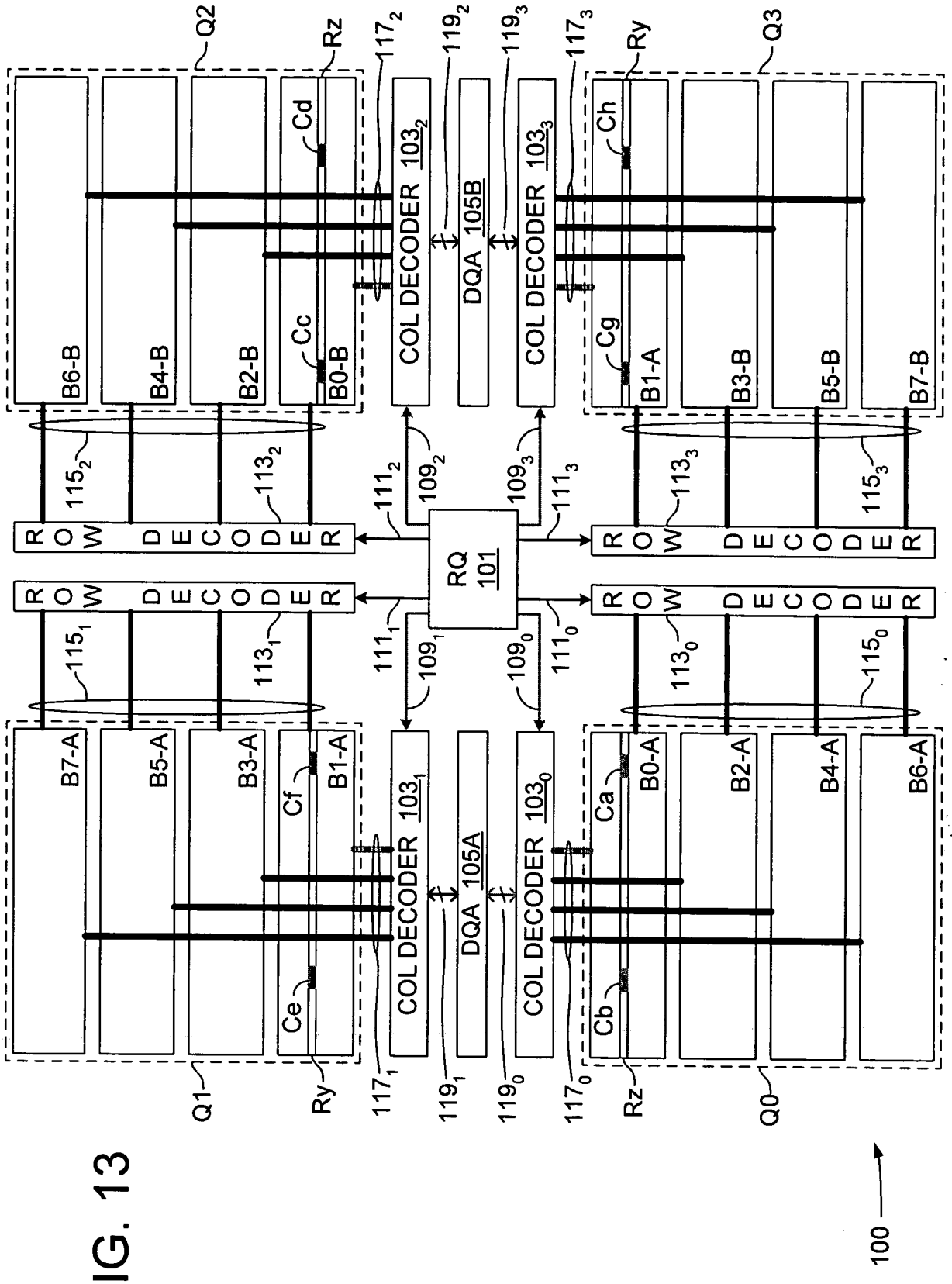

Q2
Rz
Cd
Cc
B6-B
B4-B
B2-B
B0-B
COL DECODER 103$_2$
DQA 105B
COL DECODER 103$_3$
Ch
Cg
Ry
Q3
B1-A
B3-B
B5-B
B7-B
RQ 101
ROW DECODER
Q1
Ry
Ce
Cf
B7-A
B5-A
B3-A
B1-A
COL DECODER 103$_1$
DQA 105A
COL DECODER 103$_0$
Ca
Cb
B0-A
B2-A
B4-A
B6-A
Rz
Q0
100

FIG. 13

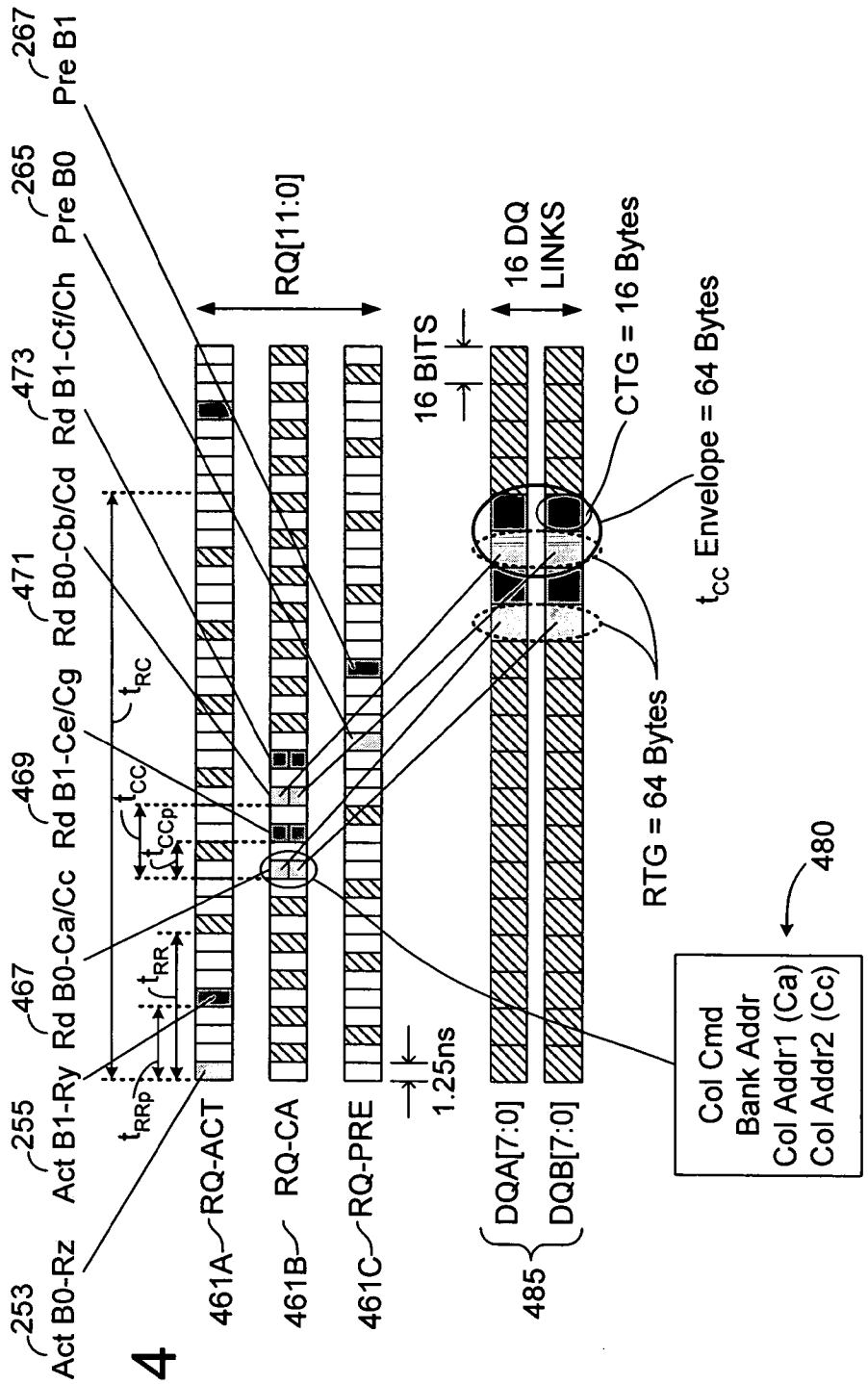
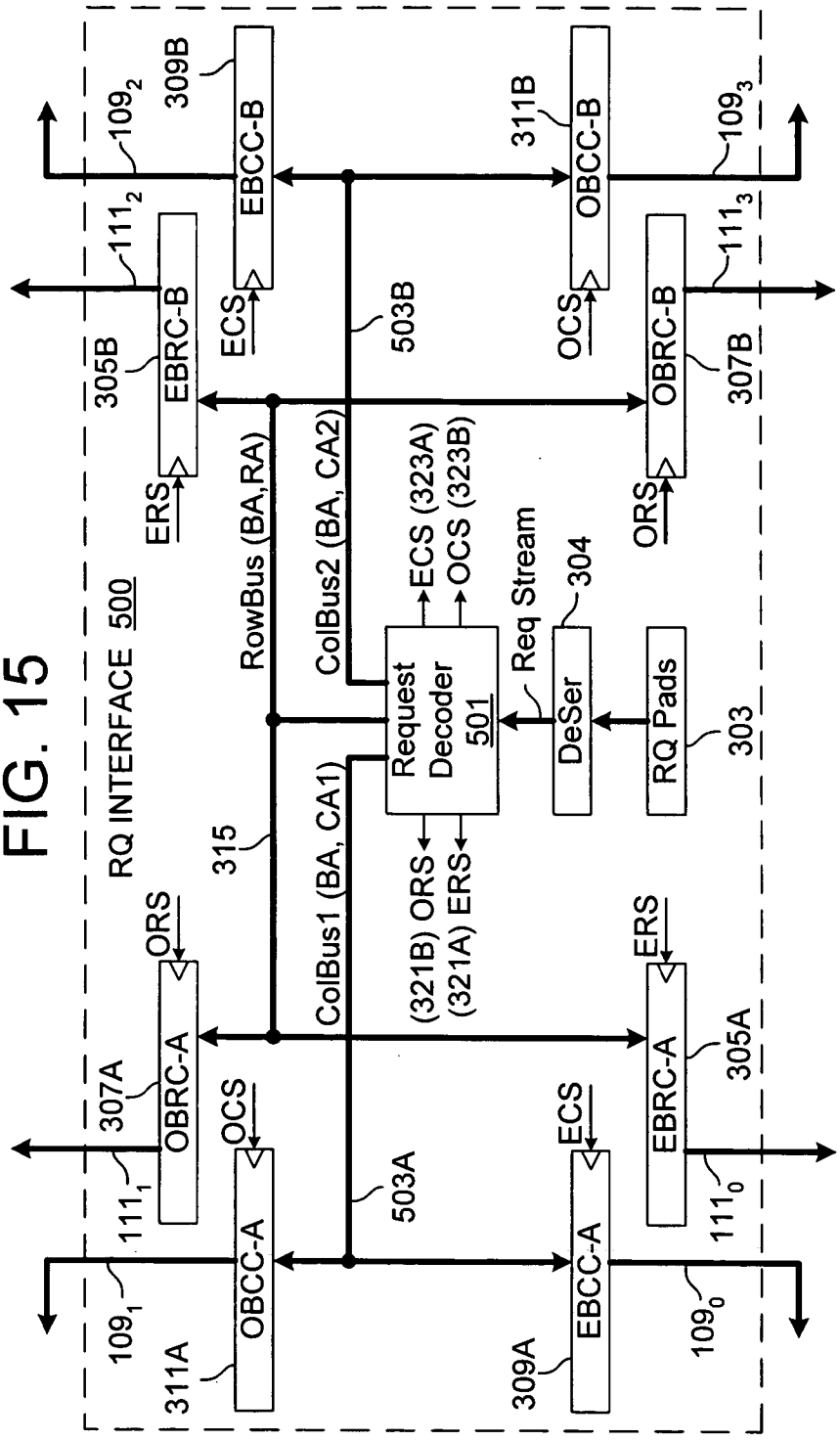

253
Act B0-Rz
255
Act B1-Ry
467
Rd B0-Ca/Cc
469
Rd B1-Ce/Cg
471
Rd B0-Cb/Cd
473
Rd B1-Cf/Ch
265
Pre B0
267
Pre B1
RQ[11:0]
461A
RQ-ACT
461B
RQ-CA
461C
RQ-PRE
1.25ns
16 BITS
16 DQ LINKS
CTG = 16 Bytes
t_{CC} Envelope = 64 Bytes
RTG = 64 Bytes
485
DQA[7:0]
DQB[7:0]
480
Col Cmd
Bank Addr
Col Addr1 (Ca)
Col Addr2 (Cc)
t_{RC}
t_{CC}
t_{CCp}
t_{RR}
t_{RRp}

FIG. 14

FIG. 15


RQ INTERFACE 500
309B
EBCC-B
311B
OBCC-B
109_2
109_3
111_2
111_3
305B
EBRC-B
307B
OBRC-B
ECS
OCS
503B
ERS
ORS
RowBus (BA,RA)
ColBus2 (BA, CA2)
ECS (323A)
OCS (323B)
Request Decoder 501
Req Stream
304
DeSer
RQ Pads
303
315
ColBus1 (BA, CA1)
(321B) ORS
(321A) ERS
307A
OBRC-A
305A
EBRC-A
503A
111_1
111_0
109_1
109_0
311A
OBCC-A
309A
EBCC-A

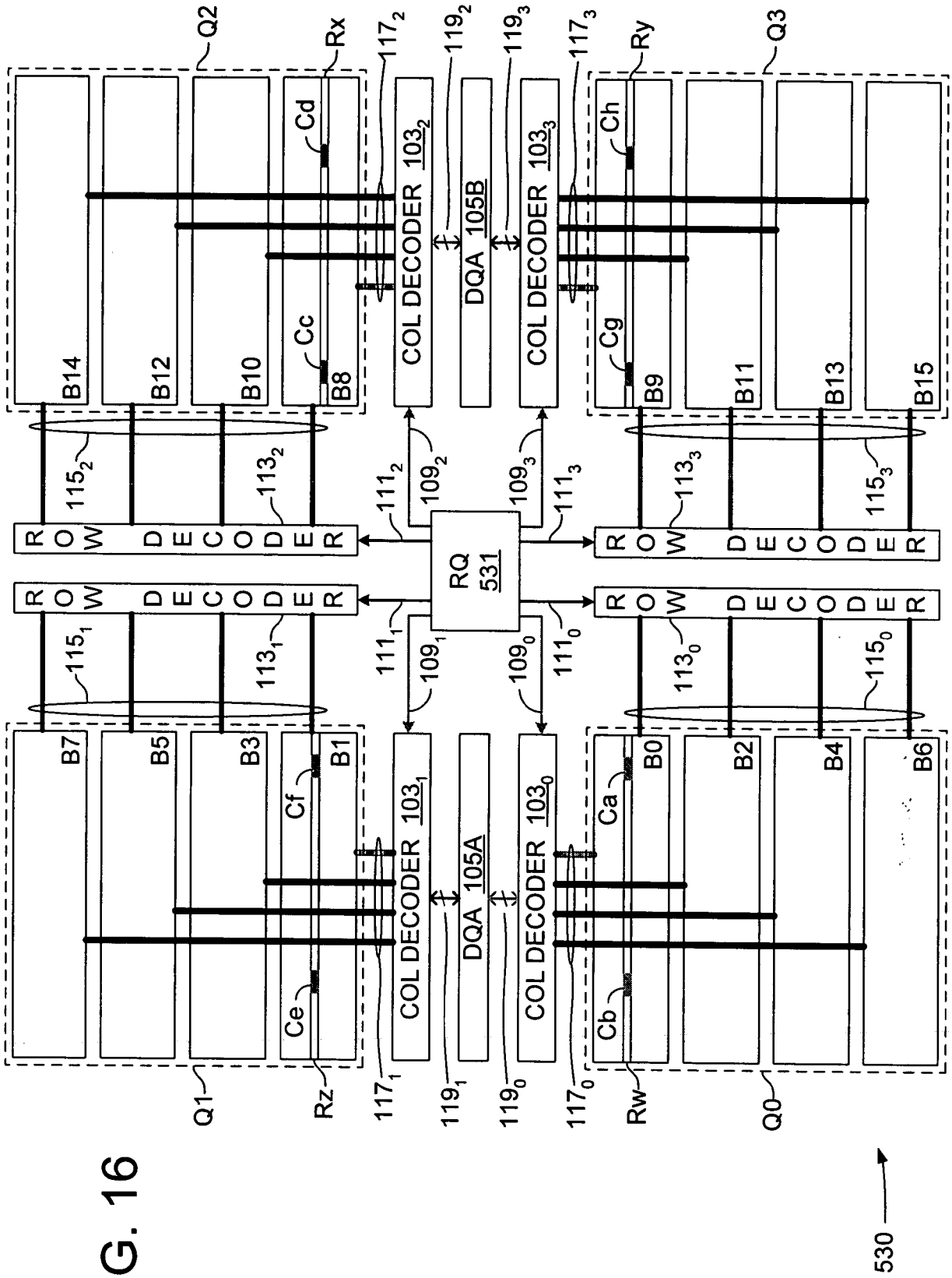

Q2
Rx
Cd
Cc
B14
B12
B10
B8
COL DECODER 103₂
DQA 105B
COL DECODER 103₃
Ch
Cg
Ry
Q3
B9
B11
B13
B15
ROW DECODER
RQ 531
B7
B5
B3
B1
Cf
Ce
COL DECODER 103₁
DQA 105A
COL DECODER 103₀
Ca
Cb
B0
B2
B4
B6
Q1
Rz
Rw
Q0
530

FIG. 16

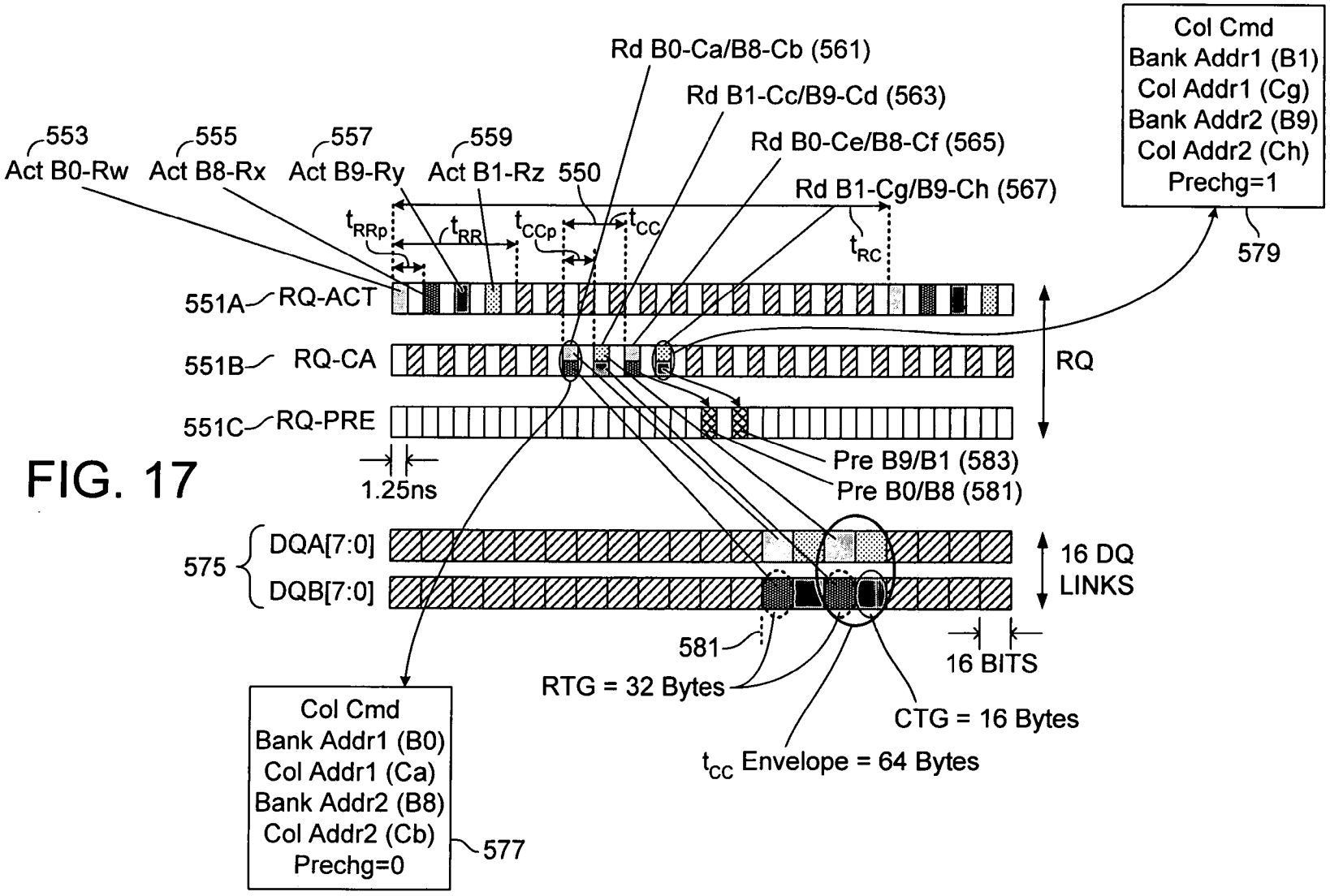
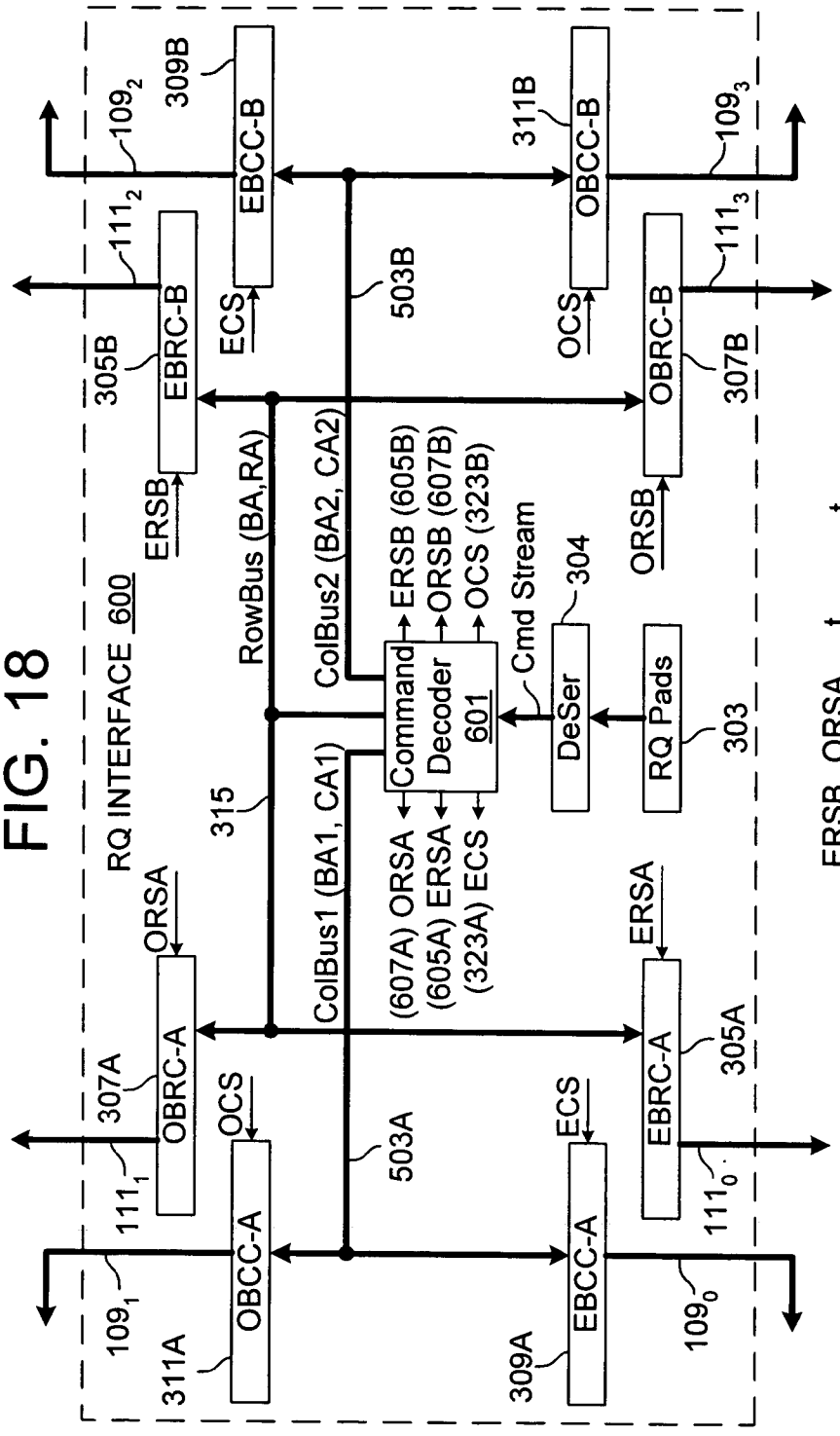
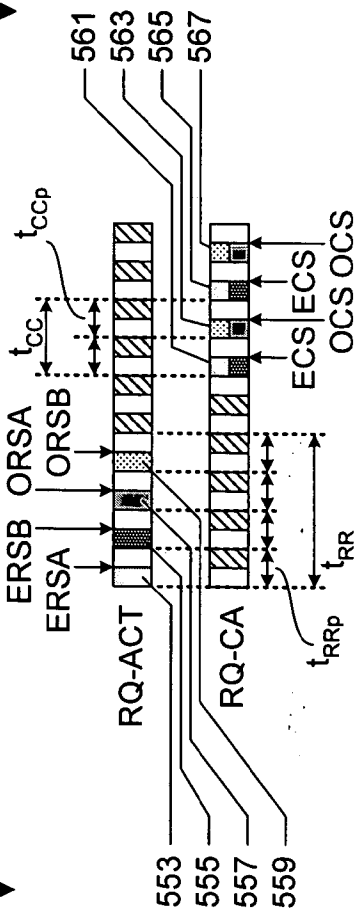


FIG. 17

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FIG. 18
RQ INTERFACE 600
EBCC-B
EBRC-B
OBCC-B
OBRC-B
OBRC-A
OBCC-A
EBRC-A
EBCC-A
309B
311B
307B
305B
307A
311A
309A
305A
503B
503A
315
RowBus (BA,RA)
ColBus2 (BA2, CA2)
ColBus1 (BA1, CA1)
Command Decoder 601
Cmd Stream
DeSer
304
RQ Pads
303
ERSB (605B)
ORSB (607B)
OCS (323B)
(607A) ORSA
(605A) ERSA
(323A) ECS
ORSA
ERSA
ERSB
ORSB
OCS
ECS
109_0
109_1
109_2
109_3
111_0
111_1
111_2
111_3


FIG. 19
561
563
565
567
553
555
557
559
RQ-ACT
RQ-CA
ERSB
ERSA
ORSA
ORSB
ECS
OCS
t_{CCp}
t_{CC}
t_{RR}
t_{RRp}

ST MODE
ROW REQ

	Even	Odd
RQ11	OP	OP
RQ10	OP	R8
RQ9	R9	R7
RQ8	R10	R6
RQ7	rsrv	R5
RQ6	rsrv	R4
RQ5	rsrv	R3
RQ4	rsrv	R2
RQ3	rsrv	R1
RQ2	BA2	R0
RQ1	BA1	rsrv
RQ0	BA0	rsrv

FIG. 20A

MT MODE
ROW REQ

	Even	Odd
RQ11	OP	OP
RQ10	OP	R8
RQ9	R9	R7
RQ8	R10	R6
RQ7	rsrv	R5
RQ6	rsrv	R4
RQ5	rsrv	R3
RQ4	rsrv	R2
RQ3	BA3	R1
RQ2	BA2	R0
RQ1	BA1	rsrv
RQ0	BA0	rsrv

FIG. 20B

ST MODE
COL REQ

	Even	Odd
RQ11	OP	rsrv
RQ10	OP	rsrv
RQ9	OP	rsrv
RQ8	OP	rsrv
RQ7	OP	C7
RQ6	C8	C6
RQ5	C9	C5
RQ4	rsrv	C4
RQ3	rsrv	rsrv
RQ2	BC2	rsrv
RQ1	BC1	rsrv
RQ0	BC0	rsrv

FIG. 21A

MT MODE
COL REQ

	Even	Odd
RQ11	OP	AP
RQ10	OP	Cy9
RQ9	OP	Cy8
RQ8	OP	BCy0
RQ7	OP	Cx7
RQ6	Cx8	Cx6
RQ5	Cx9	Cx5
RQ4	BCy2	Cx4
RQ3	BCy1	Cy7
RQ2	BCx2	Cy6
RQ1	BCx1	Cy5
RQ0	BCx0	Cy4

FIG. 21B

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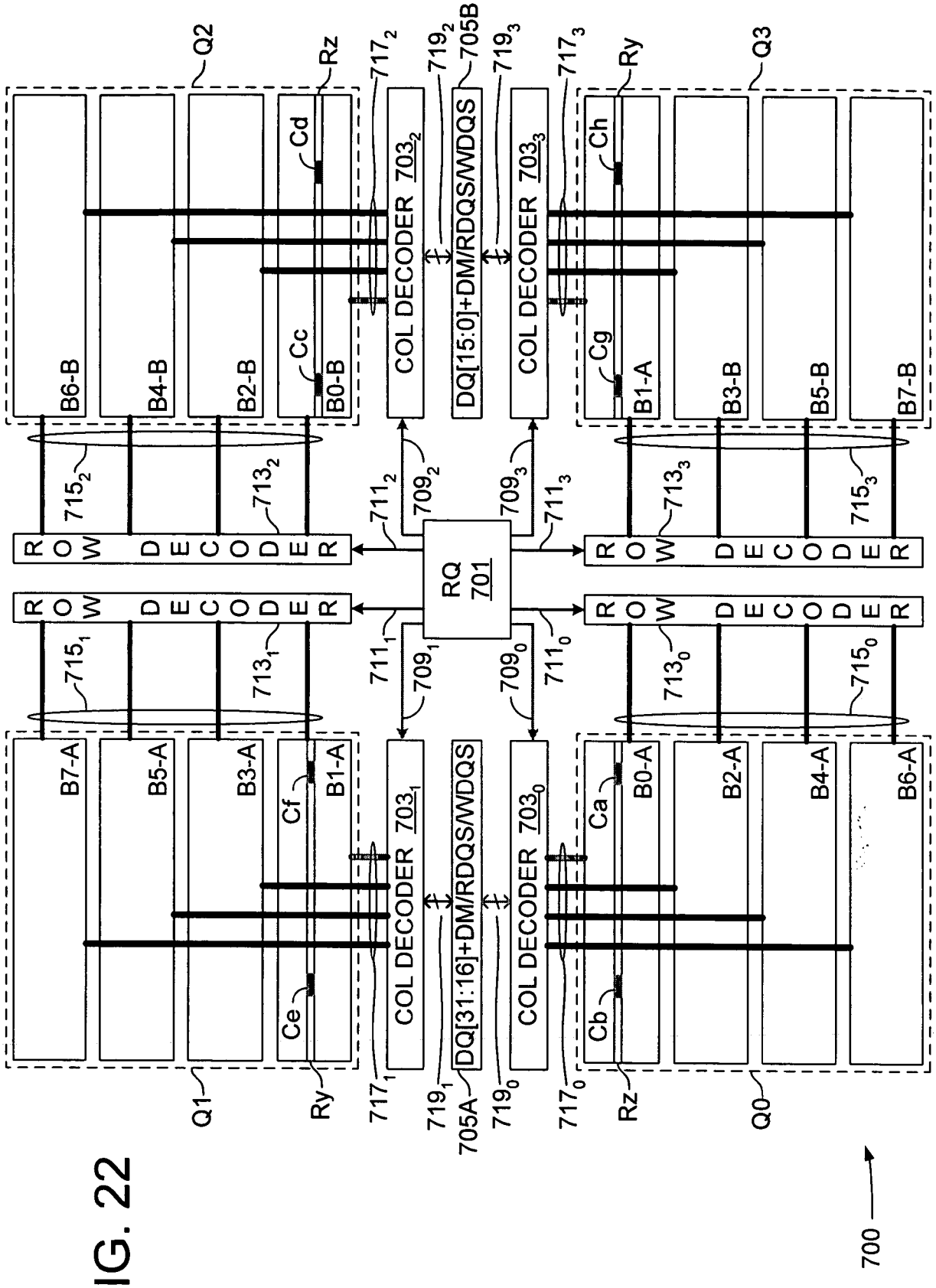
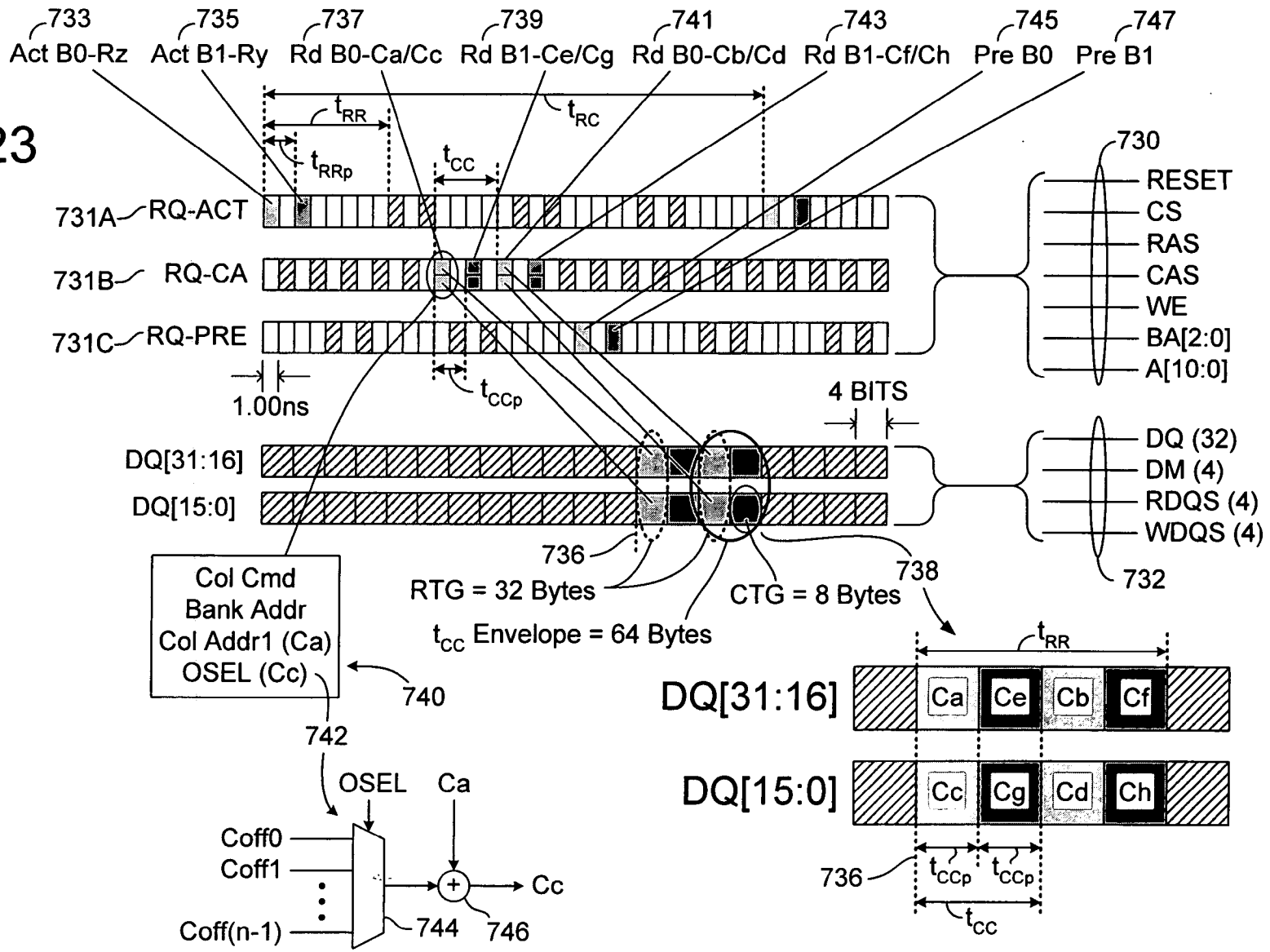
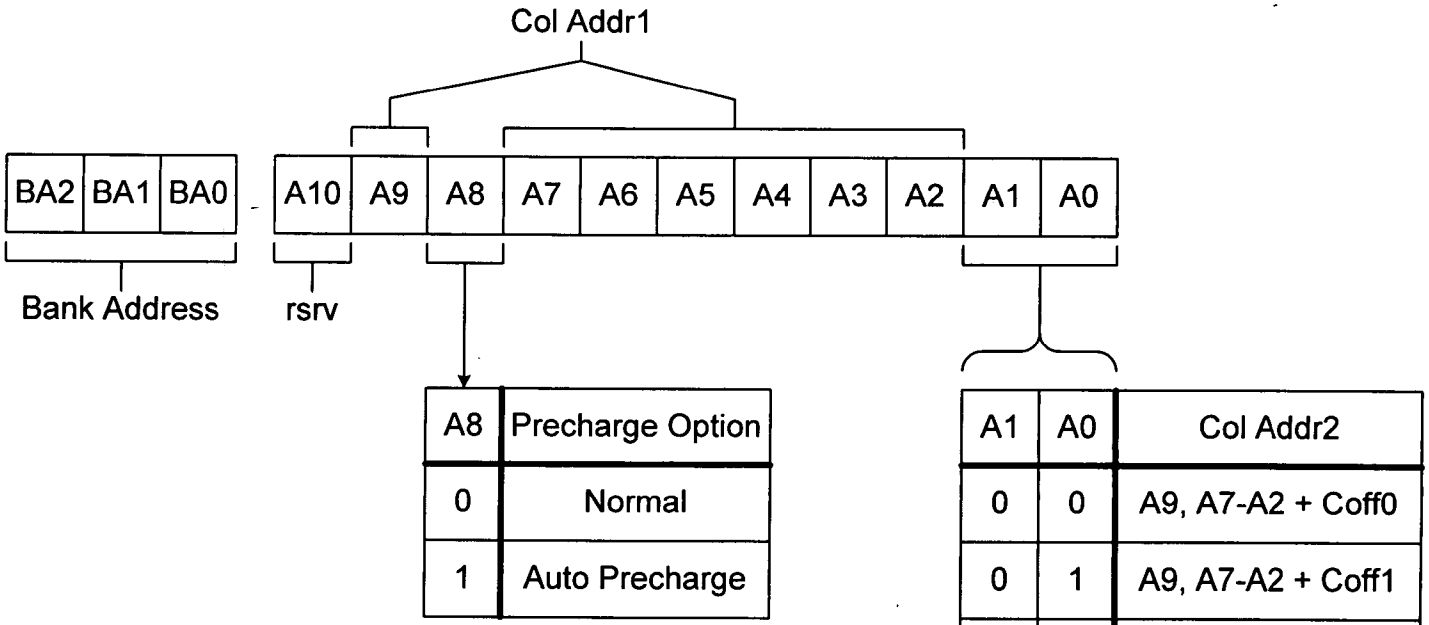

Q2
Rz
Cd
Cc
B6-B
B4-B
B2-B
B0-B
COL DECODER 703$_2$
DQ[15:0]+DM/RDQS/WDQS
COL DECODER 703$_3$
Ry
Ch
Cg
B1-A
B3-B
B5-B
B7-B
Q3
RQ 701
Q1
Ry
Ce
Cf
B7-A
B5-A
B3-A
B1-A
COL DECODER 703$_1$
DQ[31:16]+DM/RDQS/WDQS
COL DECODER 703$_0$
Rz
Cb
Ca
B0-A
B2-A
B4-A
B6-A
Q0
705A
705B
700

FIG. 22

FIG. 23



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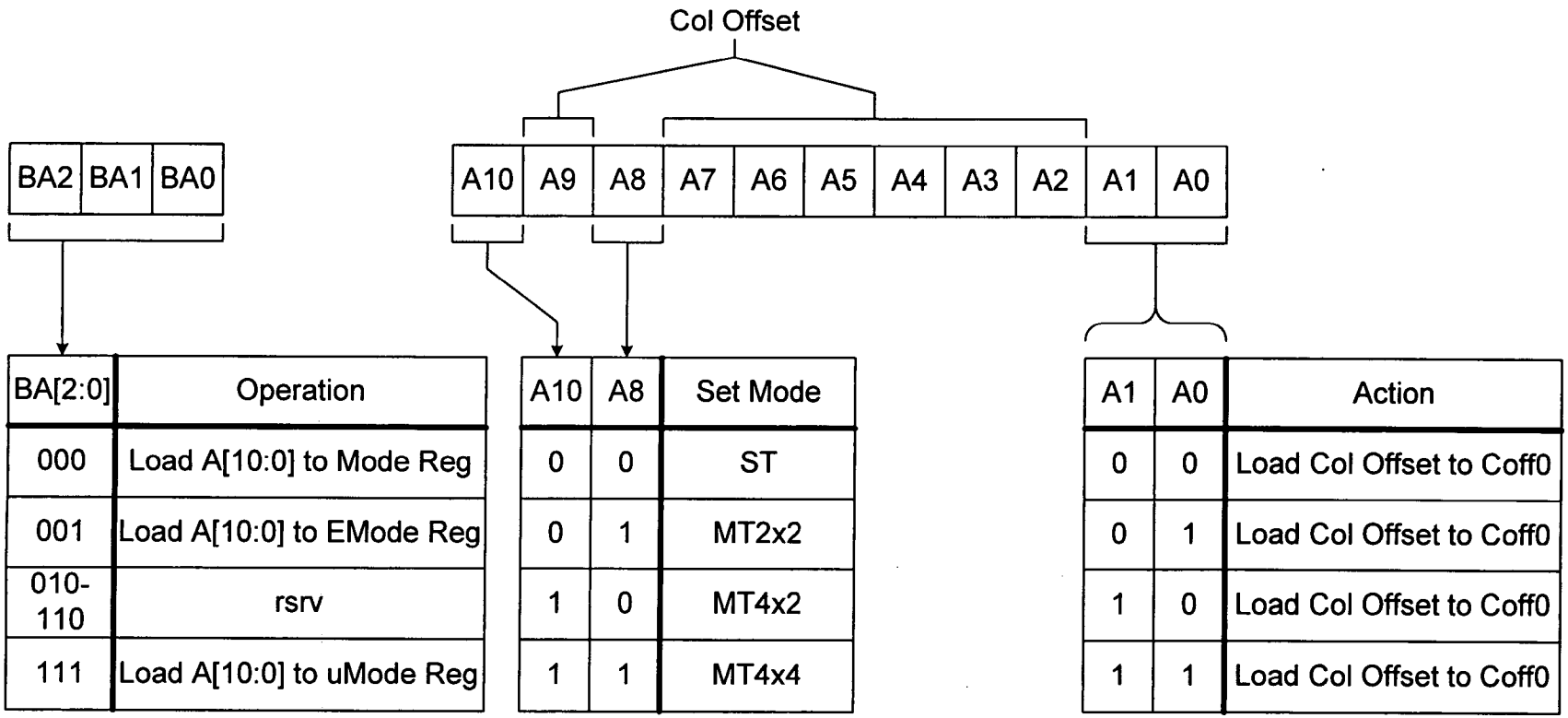


A8	Precharge Option
0	Normal
1	Auto Precharge

A1	A0	Col Addr2
0	0	A9, A7-A2 + Coff0
0	1	A9, A7-A2 + Coff1
1	0	A9, A7-A2 + Coff2
1	1	A9, A7-A2 + Coff3

FIG. 24

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BA[2:0]	Operation
000	Load A[10:0] to Mode Reg
001	Load A[10:0] to EMode Reg
010-110	rsrv
111	Load A[10:0] to uMode Reg

A10	A8	Set Mode
0	0	ST
0	1	MT2x2
1	0	MT4x2
1	1	MT4x4

A1	A0	Action
0	0	Load Col Offset to Coff0
0	1	Load Col Offset to Coff0
1	0	Load Col Offset to Coff0
1	1	Load Col Offset to Coff0

FIG. 25

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Silicon Motion Inc. v. K.Mizra LLC, IPR2024-01236

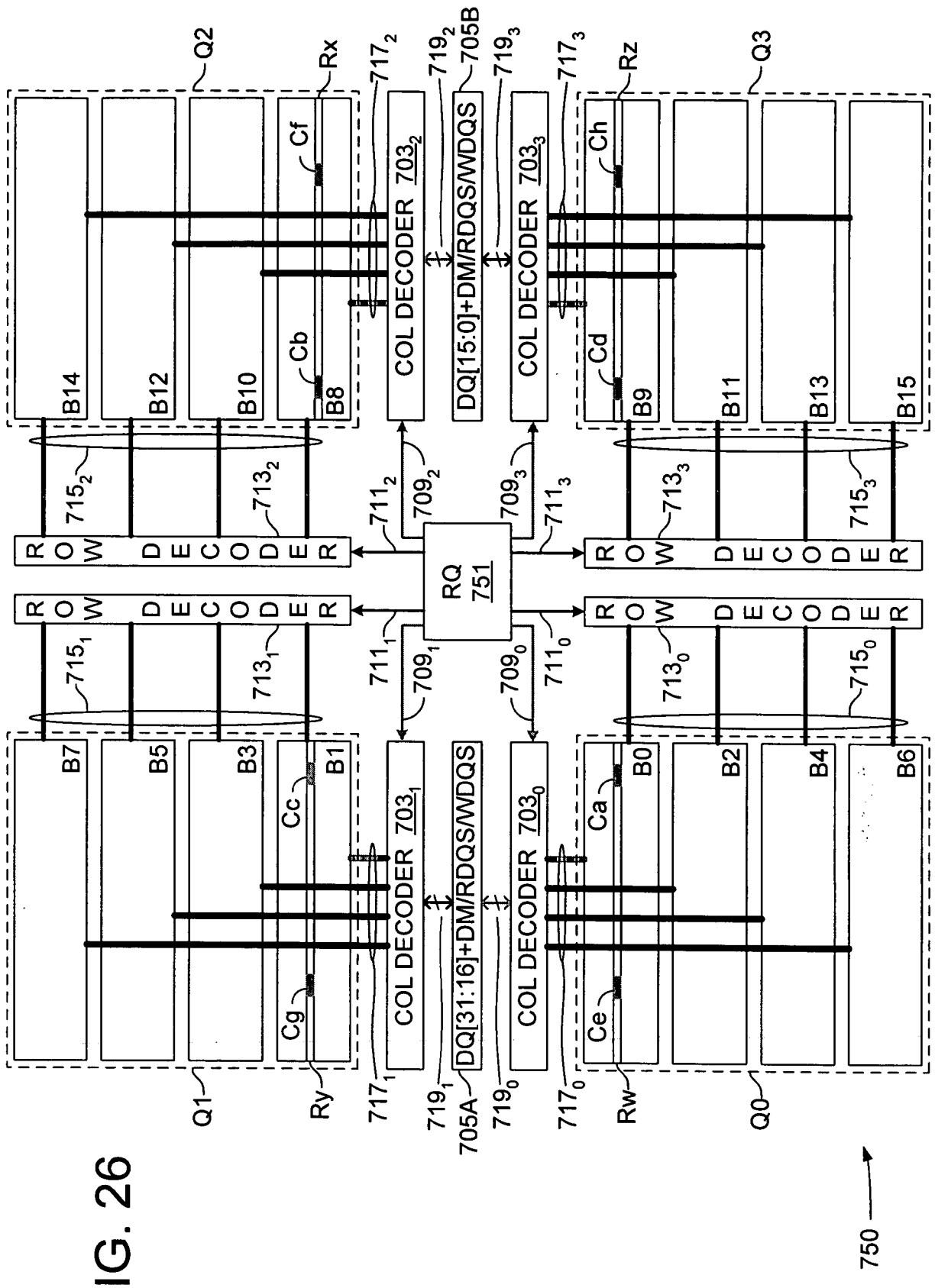

Q2
Rx
Cf
Cb
B14
B12
B10
B8
COL DECODER 703₂
DQ[15:0]+DM/RDQS/WDQS
705B
COL DECODER 703₃
Rz
Ch
Cd
B9
B11
B13
B15
Q3
RQ 751
Q1
Ry
Cc
Cg
B7
B5
B3
B1
COL DECODER 703₁
DQ[31:16]+DM/RDQS/WDQS
705A
COL DECODER 703₀
Ca
Ce
B0
B2
B4
B6
Rw
Q0
750

FIG. 26

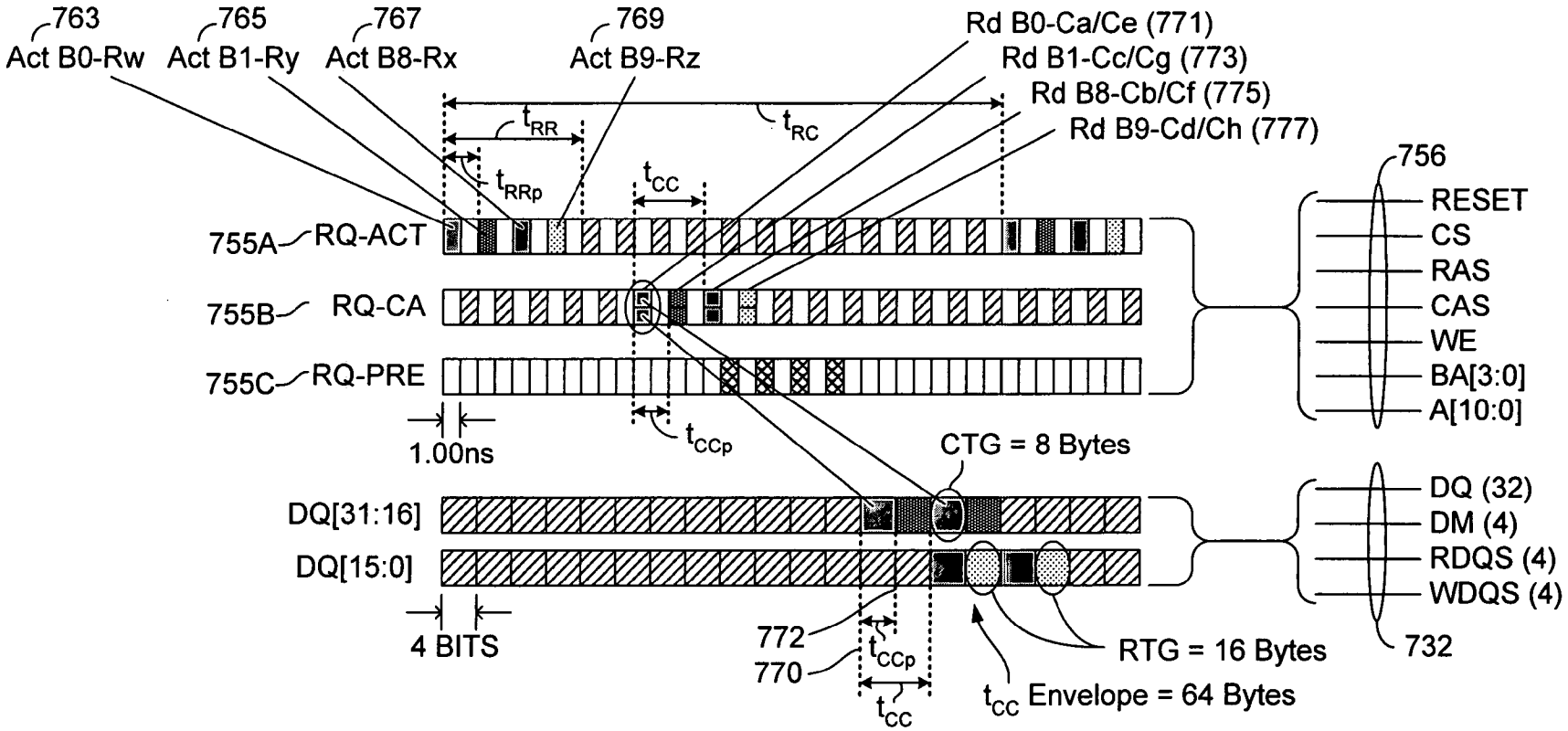


FIG. 27

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Silicon Motion Inc. v. K.Mizra LLC, IPR2024-01236

FIG. 28

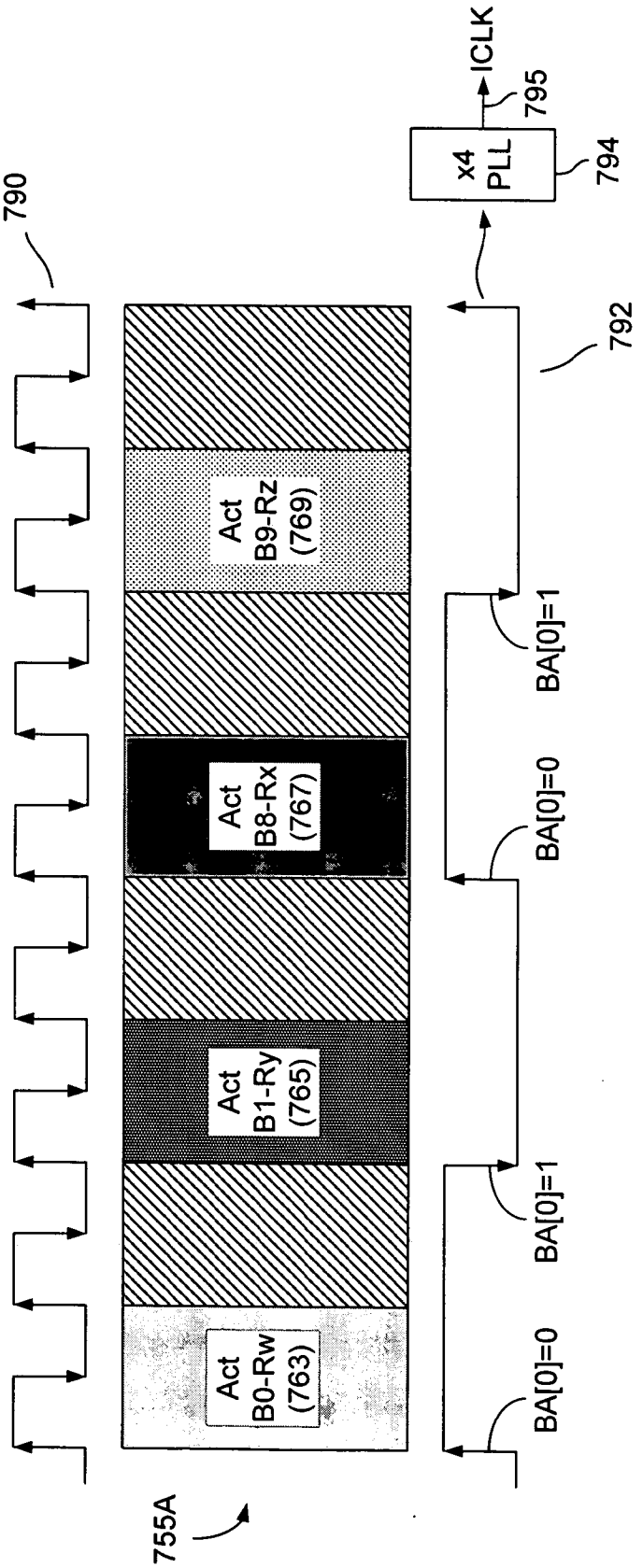
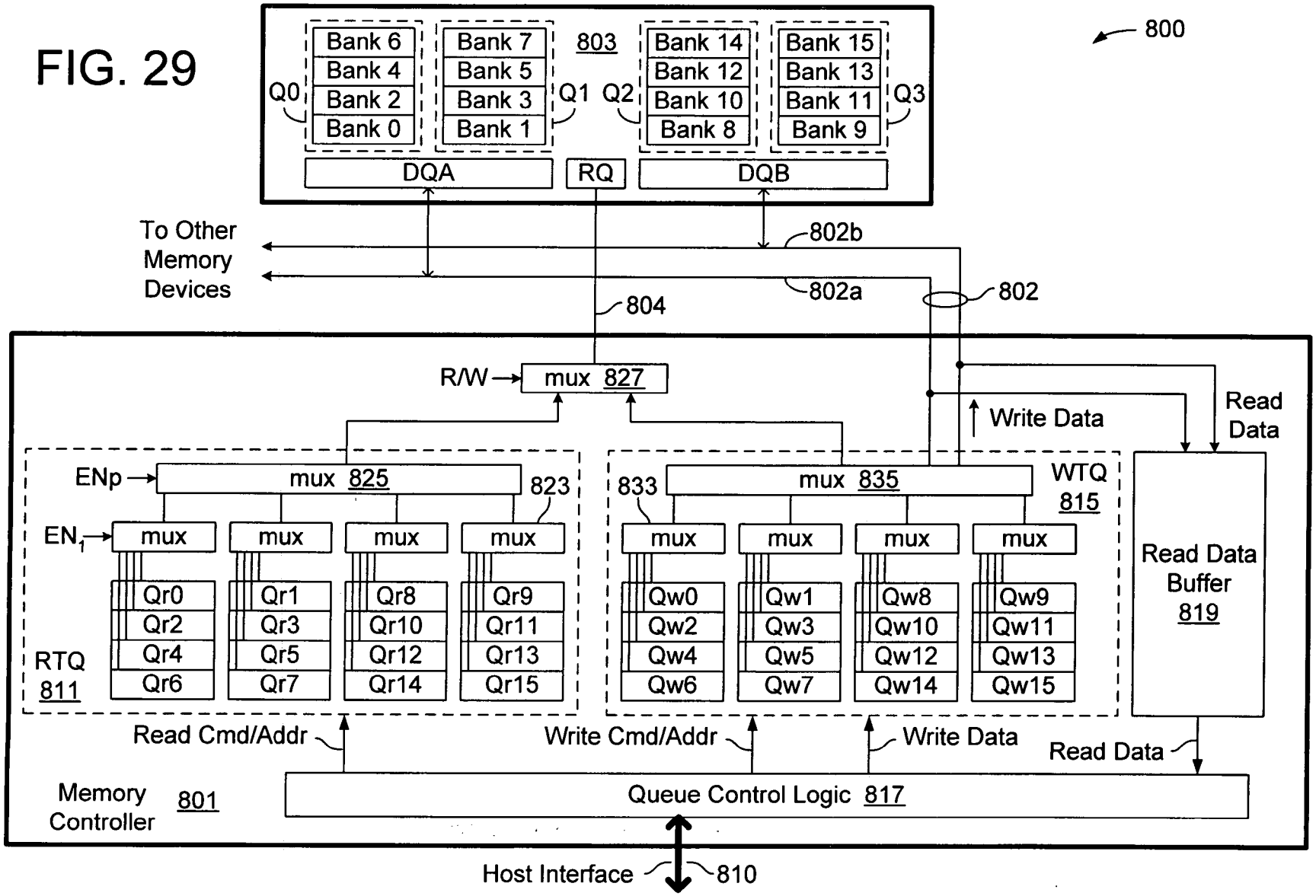

790
x4 PLL
794
795
ICLK
792
BA[0]=1
BA[0]=0
BA[0]=1
BA[0]=0
Act B9-Rz (769)
Act B8-Rx (767)
Act B1-Ry (765)
Act B0-Rw (763)
755A

FIG. 29



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Silicon Motion Inc. v. K.Mizra LLC, IPR2024-01236

Document Description: Application Data Sheet to update/correct info
Doc Code: ADS.CORR

CORRECTED ADS FORM

Application Number	15486068
Title of Invention	Memory Controller For Micro-Threaded Memory Operations

Inventor Information

****If no data is shown, no data has been corrected****

	Data of Record	Updated Data
Order Number	1	
Name	Frederick A. Ware	
Residence Information		
Residency	us-residency	
City	Los Altos Hills	
State	CA	
Country of Residence	US	
Mailing Address of Inventor		
Address 1	1050 Enterprise Way, Suite 700	
Address 2		
City,State/Province, Postal Code	Sunnyvale CA 94089	
Country	US	

	Data of Record	Updated Data
Order Number	2	
Name	Craig E. Hampel	
Residence Information		
Residency	us-residency	
City	Los Altos	
State	CA	
Country of Residence	US	
Mailing Address of Inventor		
Address 1	1050 Enterprise Way, Suite 700	
Address 2		
City,State/Province, Postal Code	Sunnyvale CA 94089	
Country	US	

	Data of Record	Updated Data
Order Number	3	
Name	Wayne S. Richardson	
Residence Information		
Residency	us-residency	
City	Saratoga	
State	CA	
Country of Residence	US	
Mailing Address of Inventor		
Address 1	~~1050 Enterprise Way, Suite 700~~	11890 Walbrook Drive
Address 2		
City,State/Province, Postal Code	~~Sunnyvale CA 94089~~	Saratoga CA 95070
Country	US	

	Data of Record	Updated Data
Order Number	4	
Name	Chad A. Bellows	
Residence Information		
Residency	us-residency	
City	Birmingham	
State	MI	
Country of Residence	US	
Mailing Address of Inventor		
Address 1	342 Henley Street	
Address 2		
City,State/Province, Postal Code	~~Birmingham MI 48167~~	Birmingham MI 48009
Country	US	

Document Description: Application Data Sheet to update/correct info
Doc Code: ADS.CORR

	Data of Record	Updated Data
Order Number	5	
Name	Lawrence Lai	

Residence Information

Residency	us-residency	
City	San Jose	
State	CA	
Country of Residence	US	

Mailing Address of Inventor

Address 1	~~1050 Enterprise Way, Suite 700~~	1133 Valley Quail Circle
Address 2		
City,State/Province, Postal Code	~~San Jose CA 94089~~	San Jose CA 95120
Country	US	

Application Information

	Data of Record	Updated Data
Title of Invention	Memory Controller For Micro-Threaded Memory Operations	
Attorney Docket Number	2016091 / RA378C3C1C1US	
Entity Type	Regular Undiscounted	

Domestic Benefit/National Stage Information

****If no data is shown, no data has been corrected****

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121,365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S. C. 119(e) or 120, and 37 CFR 1.78(a).

		Data of Record	Updated Data
	Prior Application Status		
	Application Number		
	Continuity Type		
	Prior Application Number		
	Filing Date (YYYY-MM-DD)		
	Patent Number		
	Issue Date (YYYY-MM-DD)		

Foreign Priority Information

****If no data is shown, no data has been corrected****

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

		Data of Record	Updated Data
	Application Number		
	Country		
	Filing Date		
	Access Code		

Applicant Information

****If no data is shown, no data has been corrected****
Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

	Data of Record	Updated Data
Applicant Type		

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is		
Name of the Deceased or Legally Incapacitated Inventor		
Applicant is an Organization		
Name		
Organization Name		
Address 1		
Address 2		
City,State/Province,Postal Code		
Country		
Phone Number		
Fax Number		
Email Address		

Assignee Information including Non-Applicant Assignee Information

****If no data is shown, no data has been corrected****
Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office

	Data of Record	Updated Data
Order		
Applicant is an Organization		
Name		

Organization Name		
Mailing Address		
Address 1		
Address 2		
City,State/Province,Postal Code		
Country		
Phone Number		
Fax Number		
Email Address		

Signature

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b).

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Marc P. Schuyler/	Registration Number	35675
First Name	Marc	Last Name	Schuyler

PTO/SB/122 (11-08)
Approved for use through 11/30/2011. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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CHANGE OF CORRESPONDENCE ADDRESS
Application

Address to:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	15486068
Filing Date	12 April 2017
First Named Inventor	Frederick A. Ware
Art Unit	unknown
Examiner Name	unknown
Attorney Docket Number	2016091 / RA378C3C1C1US

Please change the Correspondence Address for the above-identified patent application to:

☑ The address associated with Customer Number: 78408

OR

☐ Firm or Individual Name

Address

City	State	Zip

Country

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This form cannot be used to change the data associated with a Customer Number. To change the data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB/124).

I am the:

☐ Applicant/Inventor

☐ Assignee of record of the entire interest.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☑ Attorney or agent of record. Registration Number 35675.

☐ Registered practitioner named in the application transmittal letter in an application without an executed oath or declaration. See 37 CFR 1.33(a)(1). Registration Number_____.

Signature	/Marc P. Schuyler/
Typed or Printed Name	Marc P. Schuyler
Date 12 April 2017	Telephone 4086556375

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	28912619
Application Number:	15486068
International Application Number:	
Confirmation Number:	2908
Title of Invention:	Memory Controller For Micro-Threaded Memory Operations
First Named Inventor/Applicant Name:	
Customer Number:	73091
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	2016091 / RA378C3C1C1US
Receipt Date:	12-APR-2017
Filing Date:	
Time Stamp:	22:11:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet to update/ correct info	CorrectedADS.pdf	99472 b5913bd174224e403c0f0f9c032711bf29f2a0b5	no	8

Warnings:

Information:					
2	Miscellaneous Incoming Letter	000-sb0122_fill-ChangeofcorrespondenceAddress.pdf	43466 4384f103cd584ef37d840de4725cea23fe69372f	no	1
Warnings:					
Information:					
			Total Files Size (in bytes):	142938	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/486,068	04/12/2017	2827	0.00	2016091 / RA378C3C1C1US	1	1

CONFIRMATION NO. 2908

78408
MARC P. SCHUYLER / Rambus
P.O. BOX 2535
SARATOGA, CA 95070

FILING RECEIPT

OC000000090792085

Date Mailed: 04/24/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Frederick A. Ware, Los Altos Hills, CA;
Craig E. Hampel, Los Altos, CA;
Wayne S. Richardson, Saratoga, CA;
Chad A. Bellows, Birmingham, MI;
Lawrence Lai, San Jose, CA;

Applicant(s)

Rambus Inc., Sunnyvale, CA;

Power of Attorney: The patent practitioners associated with Customer Number 78408

Domestic Priority data as claimed by applicant

This application is a CON of 14/449,610 08/01/2014
which is a CON of 13/901,014 05/23/2013 PAT 9292223
which is a CON of 10/998,402 11/29/2004 PAT 8595459

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

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Silicon Motion Inc. v. K.Mizra LLC, IPR2024-01236

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 04/20/2017

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/486,068**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

Memory Controller For Micro-Threaded Memory Operations

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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Silicon Motion Inc. v. K.Mizra LLC, IPR2024-01236

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/486,068

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/486,068	04/12/2017	Frederick A. Ware	2016091 / RA378C3C1C1US

CONFIRMATION NO. 2908

78408
MARC P. SCHUYLER / Rambus
P.O. BOX 2535
SARATOGA, CA 95070

FORMALITIES LETTER

OC000000090792066

Date Mailed: 04/24/2017

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **280** basic filing fee.
- $ **140** surcharge.
- $ **600** search fee.
- $ **720** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1740** TOTAL FEE BALANCE DUE.

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Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/thaile/

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Frederick A. Ware	Filed:	12 April 2017
Title:	Micro-Threaded Memory	Art Unit:	2827
Serial No.:	15/486068	Conf.:	2908
Publ. No.:			
Docket:	2016091 / RA378C3C1C1	Examiner:	Unknown

PRELIMINARY AMENDMENT

Please enter the amendment set forth below. This amendment is submitted concurrently with missing parts, which should be considered timely as the two-month date for responding to missing parts fell on a Saturday, Sunday or Federal Holiday.

In The Claims.

Please amend the claims as set forth below. This listing replaces all prior listings of claims.

1. (Canceled)

2. (New) A memory controller to control a memory device, the memory device having a plurality of bank groups, the memory controller comprising:

circuitry to provide a clock signal to the memory device, the clock signal having clock transitions;

a command interface to transmit, to the memory device, row activation commands to instruct row activations and column access commands to instruct column accesses; and

circuitry to schedule issuance of the row activation commands and the column access commands from the command interface, such that

a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common bank group, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups, and

a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups.

3. (New) The memory controller of claim 2, wherein:

each bank includes a first sub-bank and a second sub-bank;

the first sub-bank is in a first bank group of the plurality of bank groups; and

the second sub-bank is in a second bank group of the plurality of bank groups.

4. (New) The memory controller of claim 3, wherein:

each sub-bank in the first bank group shares first row decoder circuitry and first column decoder circuitry with each other sub-bank in the first bank group; and

each sub-bank in the second bank group shares second row decoder circuitry and second column decoder circuitry with each other sub-bank in the second bank group.

5. (New) The memory controller of claim 3, wherein the circuitry to schedule is to schedule at least one column access command for each row activation command, in order to access a column within a row activated by a corresponding row activation command, and wherein the command interface is to transmit bank address information to the memory device for each row activation command and for each column access command, in order to select a bank and in order to select one of the bank groups in the plurality of bank groups.

6. (New) The memory controller of claim 3, wherein the circuitry to schedule is to schedule for a given row activation command, at least two column access commands, in order to access different columns within a row activated by the given row activation command.

7. (New) The memory controller of claim 2, wherein the memory controller also comprises a data interface to exchange data with the memory device via links, using respective, mutually-exclusive subsets of the links to exchange data in association with the back-to-back column accesses to banks within different bank groups.

8. (New) The memory controller of claim 2, wherein:

the memory controller further comprises a data interface to exchange data with the memory device via links, in association with each column access command; and

the memory controller further comprises serialization/deserialization circuitry to exchange serialized data with the memory device over each of the links in association with each column access command.

9. (New) The memory controller of claim 2, wherein the memory controller further comprises a data interface to exchange each of data, and write mask values with the memory device, via respective link subsets.

10. (New) The memory controller of claim 2, wherein the memory controller is to interleave row activation commands and is to interleave column access commands for back-to-back data accesses in

different bank groups, and is to transmit bank address information as part of each command of the row activation commands and column access commands, to select a bank group of the plurality of bank groups, and to select a bank within the selected bank group.

11. (New) A memory controller to control a memory device, the memory device having a plurality of bank groups, the memory controller comprising:

circuitry to provide a clock signal to the memory device, the clock signal having clock transitions;

a command interface to transmit row activation commands and column access commands to the memory device, via a command bus;

a data interface to exchange data with the memory device in association with each column access command; and

circuitry coupled to the command interface to schedule issuance of the row activation commands and the column access commands to banks within the plurality of bank groups, such that

a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common one of the bank groups, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different ones of the bank groups, and

a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common one of the bank groups, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different ones of the bank groups;

wherein the memory controller is to transmit bank address information as part of each command of the row activation commands and column access commands, to communicate selection of a bank group of the plurality of bank groups, and to communicate selection of a bank within the selected bank group.

12. (New) The memory controller of claim 11, wherein:

each bank includes a first sub-bank and a second sub-bank;

the first sub-bank is in a first bank group of the plurality of bank groups; and

the second sub-bank is in a second bank group of the plurality of bank groups.

13. (New) The memory controller of claim 12, wherein:

each sub-bank in the first bank group shares first row decoder circuitry and first column decoder circuitry with each other sub-bank in the first bank group; and

each sub-bank in the second bank group shares second row decoder circuitry and second column decoder circuitry with each other sub-bank in the second bank group.

14. (New) The memory controller of claim 12, wherein the circuitry to schedule is to schedule at least one column access command for each row activation command, in order to access a column within a row activated by a corresponding row activation command, and wherein the command interface is to transmit bank address information to the memory device for each row activation command and for each column access command, in order to select a bank and in order to select one of the bank groups in the plurality of bank groups.

15. (New) The memory controller of claim 12, wherein the circuitry to schedule is to schedule for a given row activation command, at least two column access commands, in order to access different columns within a row activated by the given row activation command.

16. (New) The memory controller of claim 11, wherein the memory controller also comprises a data interface to exchange data with the memory device via links, using respective, mutually-exclusive subsets of the links to exchange data in association with the back-to-back column accesses to banks within different bank groups.

17. (New) The memory controller of claim 11, wherein:

the memory controller further comprises a data interface to exchange data with the memory device via links, in association with each column access command; and

the memory controller further comprises serialization/deserialization circuitry to exchange serialized data with the memory device over each of the links in association with each column access command.

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18. (New) The memory controller of claim 11, wherein the memory controller further comprises a data interface to exchange each of data, and write mask values with the memory device, via respective link subsets.

19. (New) A method of operation in a memory controller, the memory controller to control a memory device, the memory device having a plurality of bank groups, the method comprising:

providing a clock signal to the memory device, the clock signal having clock transitions;

transmitting to the memory device, via a command interface, row activation commands to instruct row activations and column access commands to instruct column accesses; and

scheduling issuance of the row activation commands and the column access commands from the command interface, such that

a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common bank group, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups, and

a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups.

20. (New) The method of claim 19, wherein:

each bank includes a first sub-bank and a second sub-bank;

the first sub-bank is in a first bank group of the plurality of bank groups;

the second sub-bank is in a second bank group of the plurality of bank groups;

each sub-bank in the first bank group shares row decoder circuitry and column decoder circuitry with each other sub-bank in the first bank group; and

each sub-bank in the second bank group shares row decoder circuitry and column decoder circuitry with each other sub-bank in the second bank group.

21. (New) The method of claim 19, wherein:

the method further comprises transmitting bank address information as part of each command of the row activation commands and column access commands, to communicate selection of a bank group of the plurality of bank groups, and to communicate selection of a bank within the selected bank group.

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REMARKS

This preliminary amendment is submitted before the first office action on the merits, and is therefore believed to be made as a matter of right.

If it would be helpful for the Examiner to discuss any of the presented limitations, or if the Examiner has any questions or concerns, the Examiner is respectfully commanded to contact the undersigned using the contact information set forth below.

Respectfully submitted,
Attorney for Applicant

/Marc P. Schuyler/
Marc P. Schuyler, Reg. No. 35, 675
(408) 655-6375
marc@schuylerlawgroup.com

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Electronic Patent Application Fee Transmittal

Application Number:	15486068
Filing Date:	12-Apr-2017
Title of Invention:	Memory Controller For Micro-Threaded Memory Operations
First Named Inventor/Applicant Name:	Frederick A. Ware
Filer:	Marc Philip Schuyler
Attorney Docket Number:	2016091 / RA378C3C1C1US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	140	140
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1740**

Electronic Acknowledgement Receipt

EFS ID:	29612225
Application Number:	15486068
International Application Number:	
Confirmation Number:	2908
Title of Invention:	Memory Controller For Micro-Threaded Memory Operations
First Named Inventor/Applicant Name:	Frederick A. Ware
Customer Number:	78408
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	2016091 / RA378C3C1C1US
Receipt Date:	26-JUN-2017
Filing Date:	12-APR-2017
Time Stamp:	18:26:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1740
RAM confirmation Number	062717INTEFSW18273500
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Preliminary Amendment	00-RA378C3C1C1-PAM-2017-06-26.pdf	79309 96087a8d806518e8bbc3dbf2d3b2517b762c13ee	no	8
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	37163 f0e8476f28da648e6dae517eb18bceb1bc0f35fd	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	116472		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/486,068	04/12/2017	2827	1740	2016091 / RA378C3C1C1US	20	3

CONFIRMATION NO. 2908

UPDATED FILING RECEIPT

78408
MARC P. SCHUYLER / Rambus
P.O. BOX 2535
SARATOGA, CA 95070

OC000000092390543

Date Mailed: 06/28/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Frederick A. Ware, Los Altos Hills, CA;
Craig E. Hampel, Los Altos, CA;
Wayne S. Richardson, Saratoga, CA;
Chad A. Bellows, Birmingham, MI;
Lawrence Lai, San Jose, CA;

Applicant(s)

Rambus Inc., Sunnyvale, CA;

Power of Attorney: The patent practitioners associated with Customer Number 78408

Domestic Priority data as claimed by applicant

This application is a CON of 14/449,610 08/01/2014 PAT 9652176
which is a CON of 13/901,014 05/23/2013 PAT 9292223
which is a CON of 10/998,402 11/29/2004 PAT 8595459

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

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Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 04/20/2017

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/486,068**

Projected Publication Date: 10/05/2017

Non-Publication Request: No

Early Publication Request: No

Title

Memory Controller For Micro-Threaded Memory Operations

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/486,068

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 27

Complete if Known	
Application Number	15/486,068
Filing Date	12 Apr 2017
First Named Inventor	Ware, Frederick (Fred)
Art Unit	2827
Examiner Name	
Attorney Docket Number	RA378.C3C1C1.US

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- RE37409-E	10-16-2001	Richardson et al.	
	2	US- 4377855	03-22-1983	Lavi, Yoav	
	3	US- 4542483	09-17-1985	Procyk, Frank J.	
	4	US- 4569036	02-04-1986	Fujii, Syuso	
	5	US- 4633434	12-30-1986	Scheuneman, James	
	6	US- 4636982	01-13-1987	Takemae et al.	
	7	US- 4646268	02-24-1987	Kuno, Kazuo	
	8	US- 4654781	03-31-1987	Schwartz et al.	
	9	US- 4670745	06-02-1987	O'Malley et al.	
	10	US- 4698788	10-06-1987	Flannagan, Stephen T.	
	11	US- 4700328	10-13-1987	Burghard, Ronald A.	
	12	US- 4710902	12-01-1987	Pelley, III, Perry H.	
	13	US- 4740921	04-26-1988	Lewandowski, Alan	
	14	US- 4758993	07-19-1988	Takemae, Yoshihiro	
	15	US- 4766538	08-23-1988	Miyoshi, Akio	
	16	US- 4768157	08-30-1988	Chauvel et al.	
	17	US- 4787858	11-29-1988	Killian, Jr., John C.	
	18	US- 4796230	01-03-1989	Young, Ian A.	
	19	US- 4800525	01-24-1989	Shah, Ashwin H.	

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	1	CN-1214515-A	04-21-1999	Kazunari et al.		✓
	2	DE-102005021894-A1	01-12-2006	Lee et al.		✓
	3	EP-0339224A2	11-02-1989	Bowater et al.		
	4	EP-0887737-A2	12-30-1998	Fort, Philippe		
	5	EP-0910091-A2	04-21-1999	Reddy, Srinivas		
	6	EP-1248267-A2	10-09-2002	Uchida et al.		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 2 of 27

Complete if Known	
Application Number	15/486,068
Filing Date	12 Apr 2017
First Named Inventor	Ware, Frederick (Fred)
Art Unit	2827
Examiner Name	
Attorney Docket Number	RA378.C3C1C1.US

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	20	US- 4811302	03-07-1989	Koishi, Keiji	
	21	US- 4825413	04-25-1989	Tran, Hiep V.	
	22	US- 4837465	06-06-1989	Rubinstein, Jorge	
	23	US- 4837743	06-06-1989	Chiu, Edison H.	
	24	US- 4843264	06-27-1989	Galbraith, Douglas C.	
	25	US- 4862421	08-29-1989	Tran, Hiep V.	
	26	US- 4888732	12-19-1989	Inoue, Michihiro	
	27	US- 4903344	02-20-1990	Inoue, Hiroshi	
	28	US- 4961168	10-02-1990	Tran, Hiep V.	
	29	US- 4982370	01-01-1991	Matsumoto, Noriaki	
	30	US- 4984196	01-08-1991	Tran, Hiep V.	
	31	US- 4985867	01-15-1991	Ishii et al.	
	32	US- 4991141	02-05-1991	Tran, Hiep V.	
	33	US- 5046050	09-03-1991	Kertis, Robert A.	
	34	US- 5093806	03-03-1992	Tran, Hiep V.	
	35	US- 5111434	05-05-1992	Cho, Soon-In	
	36	US- 5119340	06-02-1992	Slemmer, William C.	
	37	US- 5121358	06-09-1992	Slemmer, William C.	
	38	US- 5124610	06-23-1992	Conley, Jerry J.	

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	7	GB-2367400-A	04-03-2002	So et al.		✓
	8	JP-05-290573-A	05-11-1993	Yasushi, Takahashi		✓
	9	JP-07-262767	10-13-1995	Makoto et al.		✓
	10	JP-10-172283	06-26-1998	Monma et al.		✓
	11	JP-2000-066950-A	03-03-2000	Shunichi, Ishiwatari		✓
	12	JP-2000-082287	03-21-2000	Shinya et al.		✓

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	39	US- 5124951	06-23-1992	Slemmer, William C.	
	40	US- 5128897	07-07-1992	McClure, David C.	
	41	US- 5132931	07-21-1992	Koker, Gregory T.	
	42	US- 5146592	09-08-1992	Pfeiffer et al.	
	43	US- 5150330	09-22-1992	Hag, Ejaz U.	
	44	US- 5181205	01-19-1993	Kertis, Robert	
	45	US- 5193072	03-09-1993	Frenkil, Gerald L.	
	46	US- 5193074	03-09-1993	Anami, Kenji	
	47	US- 5214610	05-25-1993	Houston, Theodore W.	
	48	US- 5222047	06-22-1993	Matsuda et al.	
	49	US- 5241503	08-31-1993	Cheng, Lik T.	
	50	US- 5249165	09-28-1993	Toda, Haruki	
	51	US- 5251178	10-05-1993	Childers, Jimmie D.	
	52	US- 5263002	11-16-1993	Suzuki, Youichi	
	53	US- 5267215	11-30-1993	Tsujimoto, Akira	
	54	US- 5274596	12-28-1993	Watanabe, Yohji	
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	13	JP-2002-251883-A	09-06-2002	Toshiya et al.		✓
	14	JP-2003-007052	01-10-2003	Wataru, Sakamoto		✓
	15	JP-2003-223785-A	08-08-2003	Nagashima et al.		✓
	16	JP-2003-317474-A	11-07-2003	Parris et al.		✓
	17	JP-2004-005856-A	01-08-2004	Hiroki, Fujisawa		✓
	18	JP-2004-139552-A2	05-13-2004	Matsui, Yoshinori		✓

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Sheet 4 of 27

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Application Number	15/486,068
Filing Date	12 Apr 2017
First Named Inventor	Ware, Frederick (Fred)
Art Unit	2827
Examiner Name	
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	59	US- 5321646	06-14-1994	Tomishima, Shigeki	
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	61	US- 5343438	08-30-1994	Choi, Yun-Ho	
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	63	US- 5390308	02-14-1995	Ware et al.	
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	66	US- 5414662	05-09-1995	Foss, Richard C.	
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	70	US- 5455802	10-03-1995	McClure, David C.	
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	72	US- 5485430	01-16-1996	McClure, David C.	
	73	US- 5517456	05-14-1996	Chishiki, Shigeo	
	74	US- 5530814	06-25-1996	Wong et al.	
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	19	JP-9-231760-A	09-05-1997	Shigeo, Oshima		✓
	20	JP-H09-231760-A	09-05-1997	Shigeo, Oshima		✓
	21	WO-1991-016680-A1	10-31-1991	Farmwald et al.		
	22	WO-2004-034401-A2	04-22-2004	Ware et al.		
	23	WO-2006-039106	04-13-2006	Ware et al.		
	24	WO-2009-089301	07-16-2009	Shaeffer, Ian		

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Sheet 5 of 27

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Art Unit	2827
Examiner Name	
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	78	US- 5614855	03-25-1997	Lee et al.	
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	82	US- 5675180	10-07-1997	Pedersen, David V.	
	83	US- 5689472	11-18-1997	Tanaka et al.	
	84	US- 5701270	12-23-1997	Rao, G.R. Mohan	
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	86	US- 5717901	02-10-1998	Sung et al.	
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	89	US- 5787267	07-28-1998	Leung et al.	
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	93	US- 5852725	12-22-1998	Yen, Juei-Hsiang	
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	97	US- 5881017	03-09-1999	Matsumoto et al.	
	98	US- 5892981	04-06-1999	Wiggers, Hans	
	99	US- 5893927	04-13-1999	Hovis, William	
	100	US- 5903509	05-11-1999	Ryan et al.	
	101	US- 5933387	08-03-1999	Worley, Eugene Robert	
	102	US- 5936885	08-10-1999	Morita, Tsuyoshi	
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	110	US- 6049855	04-11-2000	Jeddeloh, Joseph	
	111	US- 6050983	04-18-2000	Moore et al.	
	112	US- 6065092-A	05-16-2000	Roy, Richard Stephen	
	113	US- 6075728	06-13-2000	Inoue, Kazunari	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 7 of 27

Complete if Known	
Application Number	15/486,068
Filing Date	12 Apr 2017
First Named Inventor	Ware, Frederick (Fred)
Art Unit	2827
Examiner Name	
Attorney Docket Number	RA378.C3C1C1.US

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	115	US- 6138185	10-24-2000	Nelson et al.	
	116	US- 6141273	10-31-2000	Ku et al.	
	117	US- 6144220	11-07-2000	Young et al.	
	118	US- 6160750	12-12-2000	Shieh, Ming-Huei	
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	185	US- 2006-0039227	02-23-2006	Lai et al.	
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Sheet 11 of 27

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	192	US- 2009-0157994	06-18-2009	Hampel et al.	
	193	US- 2010-0211748	08-19-2010	Perego et al.	
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1	AIMOTO et al., "SP23.3 A 7168GIPS 3.84GB/s 1W Parallel Image-Processing RAM Integrating a 16Mb DRAM and 128 Processors," ISSCC, February 1996, pp. 372-373/476. 3 pages	
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	4	CN Board Opinion dated December 1, 2011 re CN Application No. 200580045523.7. 8 pages. (With Translation)	✓
	5	CN Office Action dated December 22, 2010 re Rejection Decision for CN Application No. 200580045523.7. 14 pages. (With Translation)	✓
	6	CN Office Action dated March 24, 2010 re CN Application No. 200580045523.7, Includes Text of the Second Office Action and Translation. 14 pages. (With Translation)	✓
	7	CN Response dated June 3, 2010 re CN Patent Application No. 200580045523.7. 11 pages. (With Translation)	✓
	8	CUPPU, V., et al. "A Performance Comparison of Contemporary DRAM Architectures", Proceedings of the 26th International Symposium on Computer Architecture, Atlanta, GA, May 2-4,1999; [International Symposium on Computer Architecture (ISCA)], Los Alamitos, CA; IEEE Comp. Soc, US, vol Conf. 26, 2 May 1999 (1999-05-02), pages 222-233, XP000887620, ISBN: 978-0-7695-0171-0. 12 pages	
	9	Elpida Memory Inc., "User's Manual: New Features of DDR3 SDRAM," Document E1503E10 (Ver.1.0), published March 2009. 18 pages	
	10	EP Communication pursuant to Article 94(3) EPC, dated July 30, 2010 in EP Application No. 05852108.8 - 2210. 6 pages	

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Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	11	EP Examination Report dated April 24, 2013 in EP Application No. 11184623.4. 7 pages	
	12	EP Examination Report dated July 29, 2013 re EP Application No. 11168736.4. 10 pages	
	13	EP Examination Report dated June 3, 2013 in EP Application No. 05852180.8. 8 pages	
	14	EP Extended European Search Report dated March 27, 2012 re EP Application No. 11168734.9. 9 pages	
	15	EP Extended European Search Report dated March 27, 2012 re EP Application No. 11168735.6. 9 pages	
	16	EP Extended European Search Report dated March 28, 2012 re EP Application No. 11168736.4. 11 pages	
	17	EP Extended Search Report dated December 30, 2011 re EP Application No. 11179126.5. 10 pages	
	18	EP Extended Search Report dated December 30, 2011 re EP Application No. 11184623.4. 9 pages	
	19	EP Extended Search Report dated January 2, 2012 re EP Application No. 11184627.5. 7 pages	
	20	EP Office Action dated April 24, 2013 in EP Application No. 11179126.5. 9 pages	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	14	of	27

Complete if Known	
Application Number	15/486,068
Filing Date	12 Apr 2017
First Named Inventor	Ware, Frederick (Fred)
Art Unit	2827
Examiner Name	
Attorney Docket Number	RA378.C3C1C1.US

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	22	EP Office Action dated March 23, 2012 re EP Application No. 05852180.8. 5 pages	
	23	EP Office Communication dated August 1, 2013 in EP Application 11168735.6. 23 pages	
	24	EP Office Communication dated August 1, 2013 re EP Application No. 11168734.9. 24 pages	
	25	EP Office Communication dated January 11, 2012 re EP Application No. 07782931.5. 7 pages	
	26	EP Office Communication dated November 24, 2010 re EP Application No. 09167223.8. 6 pages	
	27	EP Official Communication dated September 27, 2012 in EP Application No. 09167223.8-1233. 2 pages	
	28	EP Provision of a Copy of the Minutes in Accordance With Rule 124(4) EPC with mail date of 3/15/2016 re EP Appln. No. 05852180.8. 7 Pages.	
	29	EP Provision of a Copy of the Minutes Rule 124(4) EPC dated January 27, 2014 re EP Application No. 07782931.5. 12 pages	
	30	EP Reponse with EP Appln. No. 11168736.4 filed on 1/16/2016 in Response to the Summons to Attend Oral Proceedings of 8/17/2015. 31 Pages.	

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	31	EP Response dated 10/8/2013 in EP Application No. 05852180.8, Includes New Claims (Highlighted and Clear copies) and New Description pages 2, 2a, and 2b (Highlighted and Clear copies). 47 pages	
	32	EP Response dated April 15, 2010 to the Official Communication dated 5 October 2009 re EP Application No. 07783931.5-1233. 25 pages	
	33	EP Response dated April 4, 2011 to the Official Communication dated 24 November 2010 re EP Application No. 09167223.8, Includes New Claims (Highlighted & Clear Copy) and Cross-Reference of New Claims. 41 pages	
	34	EP Response dated August 29, 2012 to the Official Communication dated 27 March 2012, Application No. 11168735.6. 21 pages	
	35	EP Response dated December 10, 2013 in EP Application No. 07782931.5, Includes the Main Request and Auxiliary Requests I-IV (Clear and Highlighted Copies). 63 pages	
	36	EP Response dated February 3, 2011 to the Official Communication dated 30 July 2010 re EP Application No. 05852180.8. 33 pages	
	37	EP Response dated February 5, 2014 in EP Application No. 11168736.4, Includes New Claims (Clear and Highlighted Copies) and New Description pages (Clear and Highlighted Copies). 30 pages	
	38	EP Response dated February 6, 2014 in EP Application No. 11168734.9, Includes New Claims (Highlighted and Clear Copies) and New Description pages. 26 pages	
	39	EP Response dated February 6, 2014 in EP Application No. 11168735.6, Includes New Claims (Highlighted and Clear Copies) and New Description pages. 23 pages	
	40	EP Response dated July 20, 2012 to the Official Communication dated January 11, 2012 in EP Application No. 07782931.5-1233, Includes New Claims (Clear and Highlighted Copies). 23 pages	

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	41	EP Response dated July 22, 2015 in EP Application No. 11168735.6, Includes Summons to Attend Oral Proceedings. 10 pages	
	42	EP Response dated July 23, 2015 in EP Application No. 05852180.8, Includes Summons to Attend Oral Proceedings. 14 pages	
	43	EP Response dated July 30, 2012 In response to the Official Communication dated February 6, 2012 and to the Extended European Search Report dated December 30, 2012, in EP Application No. 11 184 623.4, Includes New Claims (Clear and Highlighted Copies). 29 pages	
	44	EP Response dated July 30, 2012 in Response to the Official Communication dated February 6, 2012 and to the Extended European Search Report dated December 30, 2012, in EP Application No. 11 184 627.5, Includes New Description pp. 2, 2a, and 22. 13 pages	
	45	EP Response dated July 30, 2012 to the Official Communication dated February 6, 2011 and the extended European Search Report dated December 30, 2011, in EP Application No. 11 179 126.5, Includes New Claims (Clear and Highlighted Copies). 26 pages	
	46	EP Response dated November 4, 2013 in EP Application No. 11179126.5, Includes New Claims (Clear and Highlighted copies). 19 pages	
	47	EP Response dated November 4, 2013 in EP Application No. 11184623.4, Includes New Claims (Clear and Highlighted copies). 20 pages	
	48	EP Response dated November 4, 2013 in EP Application No. 11184627.5, Includes New Claims (Clear and Highlighted versions). 17 pages	
	49	EP Response dated September 6, 2012 to the Official Communication dated 2 May 2012, Application No. 11168734.9. 22 pages	
	50	EP Response dated September 6, 2012 to the Official Communication dated 2 May 2012, Application No. 11168736.4. 27 pages	

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Sheet 17 of 27

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	52	EP Response to Official Communication dated August 29, 2012, in EP Application No. 11168735.6, Includes New Claims (Clear and Highlighted Copies). 19 pages	
	53	EP Response to the Decision to Refuse European Patent Application of November 14, 2012, dated March 22, 2013 in EP Application No. 09 167 223.8. 71 pages	
	54	EP Response to the Official Communication of January 31, 2012 and the telephone call with Mr. Wolff of September 21, 2012, dated September 24, 2012 in EP Application No. 09167223.8. 11 pages	
	55	EP Response with EP Appln. No. 05852180.8 filed on 1/15/2016 in Response to Summons to Attend Oral Proceedings of 8/20/2015. 78 Pages.	
	56	EP Submission dated 3 February 2012 in Response to the Official Communication dated 31 January 2012 re EP Application No. 09167223.8. 4 pages	
	57	EP Submission dated January 15, 2014 in EP Application No. 07782931.5, Includes Auxiliary Request V (Clear and Highlighted copies). 9 pages	
	58	EP Summons to Attend Oral Proceedings dated August 17, 2015 in EP Application No. 11168734.9. 8 pages	
	59	EP Summons to Attend Oral Proceedings dated August 17, 2015 in EP Application No. 11168736.4. 9 pages	
	60	EP Summons to Attend Oral Proceedings re EP Application No. 09167223.8 dated 31 January 2012. 8 pages	

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	61	Fairchild Semiconductor, "Design Optimization Techniques for Double Data Rate SDRAM Modules," July 2000. 6 pages	
	62	Final Office Action with mail date of July 7, 2010 re U.S. Application No. 12/392,071. 15 pages	
	63	First EP Examination Report with mail date of October 5, 2009, re EP Application No. 07 782 931.5-1233. 5 pages	
	64	Fujitsu Limited, "Memory CMOS 8 x 256K x 32 BIT DOUBLE DATA RATE FCRAM, MB81N643289-50/-60," pp. 1-56, Fujitsu Semiconductor Data Sheet, Advance Info., AEO.5E. 57 pages	
	65	GARRETT, Jr., Billy, U.S. Application No. 09/837,307 filed April 17, 2007, re Application and Figures As Filed. 54 pages	
	66	GIACALONE et al., "SP23.2: A 1MB, 100MHz Integrated L2 Cache Memory with 128b Interface and ECC Protection," IEEE ISSCC, February 1996, pp. 370-371/475. 3 pages	
	67	HAMPEL, Craig, U.S. Application No. 11/381,349 filed May 2, 2006, re Reply Brief in Response to Examiner's Answer mailed February 8, 2010. 6 pages	
	68	HAMPEL, Craig, U.S. Application No. 12/392,071 filed February 24, 2009, re Office Action with mail date of February 17, 2011. 19 pages	
	69	HIROSE et al., "A 20-ns 4-Mb CMOS SRAM with Hierarchical Word Decoding Architecture," IEEE, October 1990, pp. 1068-1072, Vol. 25, No. 5. 8 pages	
	70	International Preliminary Report on Patentability (Chapter 1) dated April 12, 2007, re International Application No PCT/US2005/032770. 6 pages	

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	72	International Preliminary Report on Patentability (Chapter II) with mailing date of April 9, 2010 re Int'l. Application No. PCT/US07/67814. 7 pages	
	73	International Preliminary Report on Patentability with mailing date of April 9, 2010 re Int'l. Application No. PCT/US07/67814. 7 pages	
	74	International Search Report and the Written Opinion for International Application No. PCT/US2007/067814, dated February 29, 2008. 18 pages	
	75	International Search Report and Written Opinion dated January 26, 2006 in International Application No. PCT/US2005/032770. 9 pages	
	76	International Search Report and Written Opinion dated January 4, 2006 in International Application No. PCT/US2005/028728. 5 pages	
	77	International Search Report and Written Opinion dated May 10, 2006 in International Application No. PCT/US2005/042722. 15 pages	
	78	International Search Report and Written Opinion in International Application No. PCT/US/2005/032770, dated January 26, 2006. 12 pages	
	79	Invitation to Pay Additional Fees from the International Searching Authority in International Application PCT/US2007/067814, dated December 17, 2007. 8 pages	
	80	JEDEC, "Minutes of Meeting No. 71, JC-42.3 Committee on RAM Memories," including Proposal to Add Number of Banks Option to the Mode Register for 64M SDRAM, Joint Electron Device Engineering Council (JEDEC), May 25, 1994, New York, pp. 1-14 plus Attachment T. 8 pages	

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	81	JP Office Action dated June 19, 2012 for JP Application No. 2009-510005. 6 Pages. (With Translation)	✓
	82	JP Office Action dated October 27, 2011 re JP Application No. 2007-543517. 18 pages. (With Translation)	✓
	83	JP Office Action for JP Appln. No. 2015-152586 with Mail Date of 9/2/2016. 7 Pages. (With Translation)	✓
	84	JP Response (Argument and Amendment) dated June 7, 2013 in JP Application No. 2007-543517, Includes English Translation. 28 pages	✓
	85	JP Response dated April 26, 2012, re Argument and Amendment to the Office Action dated October 27, 2011 in JP Application No. 2007-543517. 21 pages. (With Translation)	✓
	86	KIRIHATA et al., "A 390-mm2, 16-Bank, 1-Gb DDR SDRAM with Hybrid Bitline Architecture," IEEE Journal of Solid-State Circuits, Vol. 34, No. 11, November 1999, pp. 1580-1588. 10 pages	
	87	KOIKE et al., "SP23.1: A 60ns 1Mb Nonvolatile Ferroelectric Memory with Non-Driven Cell Plate Line Write/Read Scheme," ISSCC, February 10, 1996, pp. 368-379/475. 3 pages	
	88	Konishi et al., "Session XVIII: STATIC RAMs, FAM 18.6: A 64Kb CMOS RAM," IEEE International Solid State Circuits Conference, February 12, 1982, pp. 258-259. 3 pages	
	89	KR Office Action dated May 9, 2012 re KR Application No. 2007-7014584. 4 pages. (With Translation)	✓
	90	KR Response (Argument and Amendment) dated May 31, 2013 in KR Application No. 2007-7014584, Includes English Translation of Argument and Claims. 133 pages	✓

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Sheet 21 of 27

Complete if Known	
Application Number	15/486,068
Filing Date	12 Apr 2017
First Named Inventor	Ware, Frederick (Fred)
Art Unit	2827
Examiner Name	
Attorney Docket Number	RA378.C3C1C1.US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	91	KR Response (Argument/Amendment) dated June 18, 2012 in KR Application No. 10-2007-7014584. 123 pages	✓
	92	MALVIYA et al., "Module Threading Technique to Improve DRAM Power and Performance," D&R Industry Articles, dated March 11, 2011, Copyright 2009. 9 pages	
	93	MASUMOTO, Rodney T., "Configurable On-Chip RAM Incorporated Into High Speed Logic Array," Proceedings of the IEEE 1985 Custom Integrated Circuits Conference, May 20 - 23, 1985, pp. 240-243. 6 pages	
	94	Micron Technology, Inc., "256Mb: x32 GDDR3 DRAM, MT44H8M32 - 2 MEG x 32 x 4 Banks," GDDR3_1.fm - Rev A, June 2003. 68 pages	
	95	Micron Technology, Inc., "Designing for High-Density DDR2 Memory," Technical Note, TN-47-16, Rev. B., December 2009. 10 pages	
	96	Micron Technology, Inc., "DRAM DATA BOOK," Preliminary 1997. 71 pages	
	97	MICRON TECHNOLOGY, INC., "Graphics DDR3 DRAM," Advance, 256 Mb x 32 GDDR3 DRAM, © 2003, pp. 1-67. 67 pages	
	98	Micron Technology, Inc., "Micron Synchronous DRAM 128Mb: x32 SDRAM," pp. 1-52, Rev. 9/00. 52 pages	
	99	Micron Technology, Inc., "Synchronous DRAM," Rev. April 1996. 43 pages	
	100	Minutes of Meeting No. 70, JC-42.3 Committee on RAM Memories, March 9, 1994, Orlando, Florida. 41 pages	

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	101	NAKAMURA et al., "FA14.2: A 29ns 64Mb DRAM with Hierarchical Array Architecture," ISSCC, February 1995, pp. 246-247/373. 3 pages	
	102	NITTA et al., "SP23.5: A 1.6GB/s Data-Rate 1Gb Synchronous DRAM with Hierarchical Square-Shaped Memory Block & Distributed Bank Architecture," IEEE ISSCC Digest of Technical Papers, pp. 376-377, 477, February 10, 1996. 3 pages	
	103	Non-Final Office Action with mail date of March 1, 2010 re U.S. Application No. 12/392,071. 13 pages	
	104	Notice of Allowance and Fee(s) Due dated August 4, 2011 re U.S. Application No. 12/392,071. 22 pages	
	105	Nvidia Corporation, "GeForce3: Lightspeed Memory Architecture," Technical Brief, pp. 1-9. 11 pages	
	106	Office Action with mail date of 1/5/2016 re Japanese Application No. 2014-095678. 9 Pages. (With Translation)	
	107	Official Communication with Extended European Search Report for EP Application No. 09167223.8 - 1233, dated October 6, 2009. 8 pages	
	108	Rambus Inc., "Micro-Threading," dated April 3, 2011, found online at rambus.com/in/.../microthreading.html. 4 pages	
	109	Response dated January 7, 2011 to the Notice of Appeal filed October 7, 2010 re U.S. Application No. 12/392,071, Includes Request for Continued Examination. 15 pages	
	110	Response dated May 17, 2011 to the Office Action mailed February 17, 2011 re U.S. Application No. 12/392,071 26 pages	

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	111	Response to Office Action of May 5, 2009, dated October 5, 2009, re Serial No. 11/767,863 filed on June 25, 2007. 20 pages	
	112	Response to the Official Communication dated January 31, 2012 (Summons to Attend Oral Proceedings), dated August 28, 2012 in EP Application No. 09167223.8. 55 pages	
	113	SAEKI et al., "SP 23.4: A 2.5 ns Clock Access 250MHz 256Mb SDRAM with a Synchronous Mirror Delay," IEEE ISSCC Digest of Technical Papers, pp. 374-375, 476, February 10, 1996. 3 pages	
	114	SAKATA et al., "Two-Dimensional Power-Line Selection Scheme for Low Subthreshold-Current Multi-Gigabit DRAM's," IEEE Journal of Solid State Circuits, Vol. 29, No. 8, August 1994, pp. 887-893. 9 pages	
	115	Samsung Electronics, "SDRAM Device Operations," 1999. 42 pages	
	116	SATOH et al., "A 209K-Transistor ECL Gate Array with RAM," IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, October 1989, pp. 1275-1281. 7 pages	
	117	SCHUETTE, Michael, "Rambus/Kingston Threaded DDR3 Modules," dated October 8, 2009, last updated October 24, 2009. 8 pages	
	118	Standards Information Network, IEEE Press, "The Authoritative Dictionary of IEEE Standards Terms," Copyright 2000, IEEE 100, Seventh Edition, p. 252. 2 pages	
	119	SUGIBAYASHI et al., "A 30-ns 256-Mb DRAM with a Multidivided Array Structure," IEEE, November 1993, pp. 1092-1098, Vol. 28, No. 11. 8 pages	
	120	SUGIBAYASHI et al., "WP3.5: A 30ns 256Mb DRAM with Multi-Divided Array Structure," ISSCC February 1993, pp. 50-51/262. 3 pages	

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	121	TAKASE et al., "A 1.6-Gbyte/s DRAM with Flexible Mapping Redundancy Technique and Additional Refresh Scheme," IEEE Journal of Solid-State Circuits, Vol. 34, No. 11, November 1999, pp. 1600-1606. 7 pages	
	122	TAKASE et al., "WP 24.1 A 1.6GB/s DRAM with Flexible Mapping Redundancy Technique and Additional Refresh Scheme," ISSCC99/Session 24/Paper, Toshiba Corp., WP 24.1, February 17, 1999. 2 pages	
	123	TAKASE et al., "WP 24.1: A 1.6GB/s DRAM with Flexible Mapping Redundancy Technique and Additional Refresh Scheme," IEEE International Solid-State Circuits Conference, 1999. 8 pages	
	124	WARE et al., "Micro-threaded Row and Column Operations in a DRAM Core," Rambus White Paper, March 2005. 7 pages	
	125	WARE et al., U.S. Application No. 12/391,873 filed February 24, 2009, re Notice of Allowance and Fee(s) Due mailed August 31, 2010. 10 pages	
	126	WARE et al., U.S. Application No. 12/391,873 filed February 24, 2009, re Notice of Allowance and Fee(s) Due mailed November 3, 2010. 11 pages	
	127	WARE et al., U.S. Application No. 13/019,785 filed February 2, 2011, re Notice of Allowance and Fee(s) Due mailed June 29, 2011. 14 pages	
	128	WARE, Frederick A., "Direct RDRAM 256/288-Mbit (512Kx16/18x32s) Data Sheet," Preliminary Information, Rambus Inc., Document DL0060 Version 0.90, 1999, pp. 1-66. 66 pages	
	129	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Amendment mailed January 11, 2011. 10 pages	
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	132	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Corrected Response submitted February 22, 2012 to the Office Action of November 23, 2011. 17 pages	
	133	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Final Office Action mailed November 23, 2011. 33 pages	
	134	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Office Action mailed February 8, 2011. 3 pages	
	135	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Office Action mailed July 9, 2010. 17 pages	
	136	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Office Action mailed March 11, 2011. 37 pages	
	137	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Office Action mailed March 21, 2012. 36 pages	
	138	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Response submitted February 22, 2012 to the Office Action of November 23, 2011, Includes Request for Continued Examination. 21 pages	
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	143	WARE, Frederick, U.S. Application No. 11/767,863 filed June 25, 2007, re Office Action mailed March 10, 2011. 23 pages	
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	147	WARE, Frederick, U.S. Application No. 11/767,863 filed on June 25, 2007, re Response After Final Office Action mailed March 24, 2010. 15 pages	
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	149	WARE, Frederick, U.S. Application No. 13/239,846 filed September 22, 2011, re Corrected Notice of Allowability mailed January 17, 2012. 5 pages	
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	153	YOO et al., "A 150 MHZ 8-Banks 256M Synchronous DRAM with Wave Pipelining Methods," IEEE ISSCC, Digest of Technical Papers, pp. 250-251, 374, February 17, 1995. 3 pages	
	154	YOO et al., "SP23.6 A 32-Bank 1Gb DRAM with 1GB/s Bandwidth," ISSCC, February 1996, pp. 378-379/477. 3 pages	
	155	YOON et al., "A 2.5V 333Mb/pin 1Gb Double Data Rate SDRAM," ISSCC Digest of Technical Papers, February 17, 1999. 11 pages	
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	29860441
Application Number:	15486068
International Application Number:	
Confirmation Number:	2908
Title of Invention:	Memory Controller For Micro-Threaded Memory Operations
First Named Inventor/Applicant Name:	Frederick A. Ware
Customer Number:	78408
Filer:	Jose Gabriel Moniz/Ann Williams
Filer Authorized By:	Jose Gabriel Moniz
Attorney Docket Number:	2016091 / RA378C3C1C1US
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Time Stamp:	17:44:53
Application Type:	Utility under 35 USC 111(a)

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Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	RA378C3C1C1US_StatementA.pdf	37046 554894f9ff37df6f25b66afa2de83b97a4073a80	no	3

Warnings:

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	RA378_IDS.pdf	1085567 68a6f98358db8e2b978dbb9b657de6a0f479da3e	no	28
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
			Total Files Size (in bytes):	1122613	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor:	Ware, Frederick (Fred), et al.
Application No.:	15/486,068
Filing Date:	12 Apr 2017
Title:	MEMORY CONTROLLER FOR MICRO-THREADED MEMORY OPERATIONS
Examiner:	
Group Art Unit:	2827
Confirmation No.:	2908
In-House Docket No.:	RA378.C3C1C1.US
Attorney Docket No.:	2016091

INFORMATION DISCLOSURE STATEMENT A
Under 37 CFR §§ 1.56 and 1.97-98

Pursuant to the provisions of 37 C.F.R §§1.56 and 1.97-98, enclosed herewith is modified form PTO/SB/08A listing references for consideration by the Examiner.

The filing of this Information Disclosure Statement shall not be construed as a representation regarding the completeness of the list of references, or that inclusion of a reference in this list is an admission that it is prior art or is pertinent to this application, or that a search has been made, or as an admission that the information listed is, or may be considered to be, material to patentability, or that no other material information exists, and shall not be construed as an admission against interest in any manner.

This Information Disclosure Statement is being filed:

- [X] within three months of the filing date of the application, or date of entry into the national stage of an international application, or before the mailing date of a first office action on the merits, whichever event last occurred;
- [ ] before the mailing of a first official action after the filing of a request for continued examination (RCE) under 37 C.F.R. §1.114;
- [ ] after three months of the filing date of this national application or the date of entry of the national stage in an international application, or after the mailing date of the first official action on the merits, whichever event last

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occurred, but before the mailing date of the first to occur of either: (1) a final action under 37 C.F.R. §1.113; or (2) an action that otherwise closes prosecution in the application, and:

☐ Authorization is hereby given to Charge Deposit Account No. 505066 for the fee of $180.00 under 37 C.F.R. §1.17(p) for submission of this Information Disclosure Statement under 37 C.F.R. §1.97(c); OR

☐ Applicant certifies pursuant to 37 C.F.R. §1.97(e) that:

☐ each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Statement; OR

☐ no item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the person signing this certification after making reasonable inquiry, no item of information contained in this Statement was known to any individual designated under 37 C.F.R. §1.56(c) more than three months prior to the filing of this Statement;

☐ on or before the payment of the issue fee but after the mailing date of the first to occur of either: (1) a final action under 37 C.F.R. §1.113; (2) a notice of allowance under 37 C.F.R. §1.311; or (3) an action that otherwise closes prosecution in the application, and:

☐ Applicant certifies pursuant to 37 C.F.R.. §1.97(e) that:

☐ each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Statement; OR

☐ no item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the person signing this certification after making reasonable inquiry, no item of information contained in this Statement was known to any individual designated under 37 C.F.R. §1.56(c) more than three months prior to the filing of this Statement;

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AND

☐ attached hereto is the fee set forth under 37 C.F.R. §1.17(p) for submission of this Information Disclosure Statement under 37 C.F.R. .§1.97(d); OR

☐ after the payment of the issue fee. Applicant requests that the information contained in this Information Disclosure Statement be placed in the file according to 37 C.F.R. §1.97(i), although the information may not be considered by the USPTO.

☒ This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior application No. 14/449,610, filed on 1 AUGUST 2014, and the references cited therein are hereby referenced, but are not required to be provided in this application under 37 C.F.R. §1.98(d).

☒ In accordance with 37 C.F.R. §§1.97 and 1.98, and in compliance with the duty of disclosure set forth in 37 C.F.R. §1.56, applicant submits attached Form PTO/SB/08a (EFS-Web) for consideration and request the references cited therein be made of record by the U.S. Patent and Trademark Office in the above-captioned application. Consideration of the foregoing plus the prompt return of a copy of the enclosed Form SB/08A with the Examiner's initials in the left column in accordance with MPEP §609 are respectfully requested.

Respectfully submitted,

Dated 7/21/2017

/ Jose Moniz /

Jose G. Moniz, Reg. No.: 50192
Rambus Inc.
1050 Enterprise Way, Suite 700
Sunnyvale, CA 94089
Tel.: (408) 462-8000
Fax: (408) 462-8001

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UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/486,068	04/12/2017	Frederick A. Ware	2016091 / RA378C3C1C1US

CONFIRMATION NO. 2908

78408
MARC P. SCHUYLER / Rambus
P.O. BOX 2535
SARATOGA, CA 95070

PUBLICATION NOTICE



Title: Memory Controller For Micro-Threaded Memory Operations

Publication No.US-2017-0286017-A1
Publication Date:10/05/2017

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/486,068	04/12/2017	Frederick A. Ware	2016091 / RA378C3C1C1US	2908

78408 7590 06/29/2018

MARC P. SCHUYLER / Rambus
P.O. BOX 2535
SARATOGA, CALIFORNIA 95070
UNITED STATES OF AMERICA

EXAMINER	
CYGIEL, GARY W	

ART UNIT	PAPER NUMBER
2137	

MAIL DATE	DELIVERY MODE
06/29/2018	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 15/486,068	Applicant(s) Ware et al.	
	Examiner Gary W Cygiel	Art Unit 2137	AIA Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 6/26/2017.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 2-21 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 2-21 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 4/12/2017 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 102

2. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

3. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 2, 7, 9-11, 16, 18, 19, and 21 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Inoue et al. (US Patent No. 5,953,257).

Consider **Claim 2**,

A memory controller to control a memory device, the memory device having a plurality of bank groups, the memory controller comprising:

circuitry to provide a clock signal to the memory device, the clock signal having clock transitions (Inoue, e.g., Fig 7, clock signal);

a command interface to transmit, to the memory device, row activation commands to instruct row activations and column access commands to instruct column accesses (Inoue, e.g., Fig 1 (300,400,500), several interfaces for receiving/transmitting commands.); and

circuitry to schedule issuance of the row activation commands and the column access commands from the command interface (Inoue, e.g., Fig 7, shows scheduling; Col 11:37+, schedule to avoid interlock.), such that

a first interval, defined by a first number of clock transitions to transpire between back- to-back row activations to banks within a common bank group, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups (Inoue:Fig 7B/C, row activations within a common bank group can operate sequentially (i.e., wait one clock cycle); Col 11:42-55, activations to same bank group cause interlock while no restriction (i.e, 0 cycles < 1 cycle) exists between bank groups.), and

a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups (Inoue:Fig 7F/C, column-to-column to different sub-banks of a bank group occurs adjacent in time while column-to-column within the same sub-bank is illustrated to wait one extra cycle; Col 11:42-55, activations to same bank group cause interlock while no restriction (i.e., 0 cycles < 1 cycle) exists between bank groups.).

Consider **Claim 7**,

Inoue further teaches wherein the memory controller also comprises a data interface to exchange data with the memory device via links, using respective, mutually-exclusive subsets of the links to exchange data in association with the back-to-back column accesses to banks within different bank groups (Inoue, e.g., Fig 1, 2010n and 2020n shows mutually exclusive subsets of data links.).

Consider **Claim 9**,

Inoue further teaches wherein the memory controller further comprises a data interface to exchange each of data, and write mask values with the memory device, via respective link subsets (Inoue, e.g., Fig 1, shows data interface to exchange data (mask values are a subset of data).).

Consider **Claim 10**,

Inoue further teaches wherein the memory controller is to interleave row activation commands and is to interleave column access commands for back-to-back data accesses in different bank groups (Inoue, e.g., Fig 7, shows interleaved commands.), and is to transmit bank address information as part of each command of the row activation commands and column access commands, to select a bank group of the plurality of bank groups, and to select a bank within the selected bank group (Inoue, e.g., Fig 7, shows bank address being sent for each row and column access command.).

Consider **Claim 11**,

Inoue teaches a memory controller to control a memory device, the memory device having a plurality of bank groups, the memory controller comprising:

circuitry to provide a clock signal to the memory device, the clock signal having clock transitions (Inoue, e.g., Fig 7, clock signal);

a command interface to transmit row activation commands and column access commands to the memory device, via a command bus (Inoue, e.g., Fig 1 (300,400,500), several interfaces for receiving/transmitting commands.);

a data interface to exchange data with the memory device in association with each column access command (Inoue, e.g., Fig 1, shows plural data interfaces to exchange data.); and

circuitry coupled to the command interface to schedule issuance of the row activation commands and the column access commands to banks within the plurality of bank groups (Inoue, e.g., Fig 7, shows scheduling; Col 11:37+, schedule to avoid interlock.), such that

a first interval, defined by a first number of clock transitions to transpire between back- to-back row activations to banks within a common one of the bank groups, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different ones of the bank groups (Inoue:Fig 7B/C, row activations within a common bank group can operate sequentially (i.e., wait one clock cycle); Col 11:42-55, activations to same bank group cause interlock while no restriction (i.e, 0 cycles < 1 cycle) exists between bank groups.), and

a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common one of the bank groups, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different ones of the bank groups (Inoue:Fig 7F/C, column-to-column to different sub-banks of a bank group occurs adjacent in time while column-to-column within the same sub-bank is illustrated to wait one extra cycle; Col 11:42-55, activations to same bank group cause interlock while no restriction (i.e., 0 cycles < 1 cycle) exists between bank groups.);

wherein the memory controller is to transmit bank address information as part of each command of the row activation commands and column access commands, to communicate selection of a bank group of the plurality of bank groups, and to communicate selection of a bank within the selected bank group (Inoue, e.g., Fig 7, shows bank address being sent for each row and column access command.).

Consider **Claim 16**,

Inoue further teaches wherein the memory controller also comprises a data interface to exchange data with the memory device via links, using respective, mutually-exclusive subsets of the links to exchange data in association with the back-to-back column accesses to banks within different bank groups (Inoue, e.g., Fig 1, 2010n and 2020n shows mutually exclusive subsets of data links.).

Consider **Claim 18**,

Inoue further teaches wherein the memory controller further comprises a data interface to exchange each of data, and write mask values with the memory device, via respective link subsets (Inoue, e.g., Fig 1, shows data interface to exchange data (mask values are a subset of data).).

Consider **Claim 19**,

Inoue teaches a method of operation in a memory controller, the memory controller to control a memory device, the memory device having a plurality of bank groups, the method comprising:

providing a clock signal to the memory device, the clock signal having clock transitions (Inoue, e.g., Fig 7, clock signal);

transmitting to the memory device, via a command interface, row activation commands to instruct row activations and column access commands to instruct column accesses (Inoue, e.g., Fig 1 (300,400,500), several interfaces for receiving/transmitting commands.); and

scheduling issuance of the row activation commands and the column access commands from the command interface (Inoue, e.g., Fig 7, shows scheduling; Col 11:37+, schedule to avoid interlock.), such that

a first interval, defined by a first number of clock transitions to transpire between back- to-back row activations to banks within a common bank group, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups (Inoue:Fig 7B/C, row activations within a common bank group can operate sequentially (i.e., wait

one clock cycle); Col 11:42-55, activations to same bank group cause interlock while no restriction (i.e, 0 cycles < 1 cycle) exists between bank groups.), and

a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups (Inoue:Fig 7F/C, column-to-column to different sub-banks of a bank group occurs adjacent in time while column-to-column within the same sub-bank is illustrated to wait one extra cycle; Col 11:42-55, activations to same bank group cause interlock while no restriction (i.e., 0 cycles < 1 cycle) exists between bank groups.).

Consider **Claim 21**,

Inoue further teaches wherein the method further comprises transmitting bank address information as part of each command of the row activation commands and column access commands, to communicate selection of a bank group of the plurality of bank groups, and to communicate selection of a bank within the selected bank group (Inoue, e.g., Fig 7, shows bank address being sent for each row and column access command.).

Claim Rejections - 35 USC § 103

5. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of

rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

6. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 8 and 17 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (US Patent No. 5,953,257).

Consider **Claim 8**,

Inoue teaches the controller of Claim 1, further comprising wherein the memory controller further comprises a data interface to exchange data with the memory device via links, in association with each column access command (see, e.g., Inoue:Fig 1), but fails to expressly describe wherein the memory controller further comprises

serialization/deserialization circuitry to exchange serialized data with the memory device over each of the links in association with each column access command. However, there are only two ways to transmit data: serial and parallel. The benefits of serial over parallel transmission is that it is cheaper and easier to implement. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include serialization/deserialization circuitry to exchange serialized data with the memory device over each of the links in association with each column (memory) access command because it is one of only two possible options and, in view of the benefits listed above, would be a basic choice of design.

Consider **Claim 17**,

Inoue teaches the controller of Claim 11, above, further comprising wherein the memory controller further comprises a data interface to exchange data with the memory device via links, in association with each column access command (see, e.g., Inoue:Fig 1), but fails to expressly describe wherein the memory controller further comprises serialization/deserialization circuitry to exchange serialized data with the memory device over each of the links in association with each column access command. However, there are only two ways to transmit data: serial and parallel. The benefits of serial over parallel transmission is that it is cheaper and easier to implement. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include serialization/deserialization circuitry to exchange serialized data with the memory device over each of the links in association with each column (memory) access command

because it is one of only two possible options and, in view of the benefits listed above, would be a basic choice of design.

9. Claims 3-6, 12-15, and 20 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (US Patent No. 5,953,257) in view of Suh (US Patent No. 6,209,056).

Consider **Claim 3**,

Inoue additionally teaches the memory controller of claim 2, including two memory scopes (i.e., banks and bank groups), but fails to additionally describe wherein each bank includes a first sub-bank and a second sub-bank, the first sub-bank is in a first bank group of the plurality of bank groups, and the second sub-bank is in a second bank group of the plurality of bank groups.

Suh teaches systems and methods for optimizing a memory configuration and is considered analogous prior art. Suh describes partitioning banks into sub-banks and distributing them into a set of bank groups. Suh does describe wherein each bank includes a first sub-bank and a second sub-bank (Suh, e.g., Fig 2, bank 0 is divided into 8 sub-banks.), the first sub-bank is in a first bank group of the plurality of bank groups (Suh, e.g., Fig 2, first bank group (top-left grouping) includes a bank 0 sub-bank.), and the second sub-bank is in a second bank group of the plurality of bank groups (Suh, e.g., Fig 2, each non-first bank group includes a bank 0 sub-bank.). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the system of Inoue with the teachings of Suh because it provides a significant reduction in

chip area and allows a data bus to be minimized in length such that high-speed operation is possible (Suh:Col 2:1-6).

Consider **Claim 4**,

The combined system of Inoue and Suh further teaches wherein each sub-bank in the first bank group shares first row decoder circuitry and first column decoder circuitry with each other sub-bank in the first bank group (Suh, e.g., Fig 2, sub-banks of first bank group share decoder circuitry.); and each sub-bank in the second bank group shares second row decoder circuitry and second column decoder circuitry with each other sub-bank in the second bank group (Suh, e.g., Fig 2, sub-banks of a non-first bank group share decoder circuitry.).

Consider **Claim 5**,

The combined system of Inoue and Suh further teaches wherein the circuitry to schedule is to schedule at least one column access command for each row activation command, in order to access a column within a row activated by a corresponding row activation command (Inoue, e.g., Fig 7, shows at least one column access command for each row activation command), and wherein the command interface is to transmit bank address information to the memory device for each row activation command and for each column access command, in order to select a bank and in order to select one of the bank groups in the plurality of bank groups (Inoue, e.g., Fig 7, shows bank address for each row and column access command; In combination with Suh, the address would

be used in order to select a bank and in order to select one of the bank groups in the plurality of bank groups).

Consider **Claim 6**,

The combined system of Inoue and Suh further teaches wherein the circuitry to schedule is to schedule for a given row activation command, at least two column access commands, in order to access different columns within a row activated by the given row activation command (Inoue, e.g., Fig 7, shows two column access commands per row activation command.).

Consider **Claim 12**,

Inoue additionally teaches the memory controller of claim 11, including two memory scopes (i.e., banks and bank groups), but fails to additionally describe wherein each bank includes a first sub-bank and a second sub-bank, the first sub-bank is in a first bank group of the plurality of bank groups, and the second sub-bank is in a second bank group of the plurality of bank groups.

Suh teaches systems and methods for optimizing a memory configuration and is considered analogous prior art. Suh describes partitioning banks into sub-banks and distributing them into a set of bank groups. Suh does describe wherein each bank includes a first sub-bank and a second sub-bank (Suh, e.g., Fig 2, bank 0 is divided into 8 sub-banks.), the first sub-bank is in a first bank group of the plurality of bank groups (Suh, e.g., Fig 2, first bank group (top-left grouping) includes a bank 0 sub-bank.), and the second sub-bank is in a second bank group of the plurality of bank groups (Suh,

e.g., Fig 2, each non-first bank group includes a bank 0 sub-bank.). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the system of Inoue with the teachings of Suh because it provides a significant reduction in chip area and allows a data bus to be minimized in length such that high-speed operation is possible (Suh:Col 2:1-6).

Consider **Claim 13**,

The combined system of Inoue and Suh further teaches wherein each sub-bank in the first bank group shares first row decoder circuitry and first column decoder circuitry with each other sub-bank in the first bank group (Suh, e.g., Fig 2, sub-banks of first bank group share decoder circuitry.); and each sub-bank in the second bank group shares second row decoder circuitry and second column decoder circuitry with each other sub-bank in the second bank group (Suh, e.g., Fig 2, sub-banks of a non-first bank group share decoder circuitry.).

Consider **Claim 14**,

The combined system of Inoue and Suh further teaches wherein the circuitry to schedule is to schedule at least one column access command for each row activation command, in order to access a column within a row activated by a corresponding row activation command (Inoue, e.g., Fig 7, shows at least one column access command for each row activation command), and wherein the command interface is to transmit bank address information to the memory device for each row activation command and for each column access command, in order to select a bank and in order to select one of

the bank groups in the plurality of bank groups (Inoue, e.g., Fig 7, shows bank address for each row and column access command; In combination with Suh, the address would be used in order to select a bank and in order to select one of the bank groups in the plurality of bank groups).

Consider **Claim 15**,

The combined system of Inoue and Suh further teaches wherein the circuitry to schedule is to schedule for a given row activation command, at least two column access commands, in order to access different columns within a row activated by the given row activation command (Inoue, e.g., Fig 7, shows two column access commands per row activation command.).

Consider **Claim 20**,

Inoue additionally teaches the method of claim 19, including two memory scopes (i.e., banks and bank groups), but fails to additionally describe wherein each bank includes a first sub-bank and a second sub-bank, the first sub-bank is in a first bank group of the plurality of bank groups, and the second sub-bank is in a second bank group of the plurality of bank groups wherein each sub-bank in the first bank group shares first row decoder circuitry and first column decoder circuitry with each other sub-bank in the first bank group; and each sub-bank in the second bank group shares second row decoder circuitry and second column decoder circuitry with each other sub-bank in the second bank group.

Suh teaches systems and methods for optimizing a memory configuration and is considered analogous prior art. Suh describes partitioning banks into sub-banks and distributing them into a set of bank groups. Suh does describe wherein each bank includes a first sub-bank and a second sub-bank (Suh, e.g., Fig 2, bank 0 is divided into 8 sub-banks.), the first sub-bank is in a first bank group of the plurality of bank groups (Suh, e.g., Fig 2, first bank group (top-left grouping) includes a bank 0 sub-bank.), and the second sub-bank is in a second bank group of the plurality of bank groups (Suh, e.g., Fig 2, each non-first bank group includes a bank 0 sub-bank.), wherein each sub-bank in the first bank group shares first row decoder circuitry and first column decoder circuitry with each other sub-bank in the first bank group (Suh, e.g., Fig 2, sub-banks of first bank group share decoder circuitry.), and each sub-bank in the second bank group shares second row decoder circuitry and second column decoder circuitry with each other sub-bank in the second bank group (Suh, e.g., Fig 2, sub-banks of a non-first bank group share decoder circuitry.). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the system of Inoue with the teachings of Suh because it provides a significant reduction in chip area and allows a data bus to be minimized in length such that high-speed operation is possible (Suh:Col 2:1-6).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary W Cygiel whose telephone number is (571)270-1170. The examiner can normally be reached on Monday - Thursday 11am-3pm CST.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Adam Queler can be reached on (571) 272-4140. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Gary W. Cygiel/
Primary Examiner, Art Unit 2137

Notice of References Cited	Application/Control No. 15/486,068	Applicant(s)/Patent Under Reexamination Ware et al.	
	Examiner Gary W Cygiel	Art Unit 2137	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
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	N					
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NON-PATENT DOCUMENTS

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/486,068	Ware et al.
	Examiner	Art Unit
	Gary W Cygiel	2137

CPC - Searched*		
Symbol	Date	Examiner

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

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Search Notes		
Search Notes	Date	Examiner
EAST text search (incl. inventor name and assignee)	06/24/2018	GC

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

Silicon Motion Inc. Ex. 1002, Page 131
Silicon Motion Inc. v. K.Mizra LLC, IPR2024-01236

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Sheet 1 of 27

Complete if Known	
Application Number	15/486,068
Filing Date	12 Apr 2017
First Named Inventor	Ware, Frederick (Fred)
Art Unit	2827
Examiner Name	
Attorney Docket Number	RA378.C3C1C1.US

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	2	US- 4377855	03-22-1983	Lavi, Yoav	
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Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	1	CN-1214515-A	04-21-1999	Kazunari et al.		✓
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Examiner Signature	/Gary W. Cygiel/	Date Considered	06/24/2018

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Sheet 2 of 27

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First Named Inventor	Ware, Frederick (Fred)
Art Unit	2827
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	22	US- 4837465	06-06-1989	Rubinstein, Jorge	
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Examiner Signature	/Gary W. Cygiel/	Date Considered	06/24/2018

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Sheet 3 of 27

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First Named Inventor	Ware, Frederick (Fred)
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Examiner Name	
Attorney Docket Number	RA378.C3C1C1.US

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Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
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Examiner Signature	/Gary W. Cygiel/	Date Considered	06/24/2018

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Sheet 4 of 27

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Examiner Signature	/Gary W. Cygiel/	Date Considered	06/24/2018

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 5 of 27

Complete if Known	
Application Number	15/486,068
Filing Date	12 Apr 2017
First Named Inventor	Ware, Frederick (Fred)
Art Unit	2827
Examiner Name	
Attorney Docket Number	RA378.C3C1C1.US

U. S. PATENT DOCUMENTS

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Art Unit	2827
Examiner Name	
Attorney Docket Number	RA378.C3C1C1.US

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Art Unit	2827
Examiner Name	
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Art Unit	2827
Examiner Name	
Attorney Docket Number	RA378.C3C1C1.US

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	183	US- 2005-0182885-A1	08-18-2005	Matsui et al.	
	184	US- 2006-0004976	01-05-2006	Rader, Shiela	
	185	US- 2006-0039227	02-23-2006	Lai et al.	
	186	US- 2006-0047899	03-02-2006	Ilda et al.	
	187	US- 2006-0067146	03-30-2006	Woo et al.	
	188	US- 2006-0072366	04-06-2006	Ware et al.	
	189	US- 2007-0268765	11-22-2007	Woo et al.	
	190	US- 2008-0028135	01-31-2008	Rajan et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/Gary W. Cygiel/	Date Considered	06/24/2018

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Sheet 11 of 27

Complete if Known	
Application Number	15/486,068
Filing Date	12 Apr 2017
First Named Inventor	Ware, Frederick (Fred)
Art Unit	2827
Examiner Name	
Attorney Docket Number	RA378.C3C1C1.US

U. S. PATENT DOCUMENTS

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	191	US- 2008-0062807	03-13-2008	Ware et al.	
	192	US- 2009-0157994	06-18-2009	Hampel et al.	
	193	US- 2010-0211748	08-19-2010	Perego et al.	
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NON PATENT LITERATURE DOCUMENTS

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	1	AIMOTO et al., "SP23.3 A 7168GIPS 3.84GB/s 1W Parallel Image-Processing RAM Integrating a 16Mb DRAM and 128 Processors," ISSCC, February 1996, pp. 372-373/476. 3 pages	
	2	Amendment and Response dated April 20, 2010 re U.S. Application No. 12/392,071. 12 pages	
	3	CHANG, Kun-Yung, "Design of a CMOS Asymmetric Serial Link," A Dissertation Submitted to the Department of Electrical Engineering and the Committee on Graduate Studies of Stanford University, August 1999. 133 pages	
	4	CN Board Opinion dated December 1, 2011 re CN Application No. 200580045523.7. 8 pages. (With Translation)	✓
	5	CN Office Action dated December 22, 2010 re Rejection Decision for CN Application No. 200580045523.7. 14 pages. (With Translation)	✓
	6	CN Office Action dated March 24, 2010 re CN Application No. 200580045523.7, Includes Text of the Second Office Action and Translation. 14 pages. (With Translation)	✓
	7	CN Response dated June 3, 2010 re CN Patent Application No. 200580045523.7. 11 pages. (With Translation)	✓
	8	CUPPU, V., et al. "A Performance Comparison of Contemporary DRAM Architectures", Proceedings of the 26th International Symposium on Computer Architecture, Atlanta, GA, May 2-4,1999; [International Symposium on Computer Architecture (ISCA)], Los Alamitos, CA; IEEE Comp. Soc, US, vol Conf. 26, 2 May 1999 (1999-05-02), pages 222-233, XP000887620, ISBN: 978-0-7695-0171-0. 12 pages	
	9	Elpida Memory Inc., "User's Manual: New Features of DDR3 SDRAM," Document E1503E10 (Ver.1.0), published March 2009. 18 pages	
	10	EP Communication pursuant to Article 94(3) EPC, dated July 30, 2010 in EP Application No. 05852108.8 - 2210. 6 pages	

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	11	EP Examination Report dated April 24, 2013 in EP Application No. 11184623.4. 7 pages	
	12	EP Examination Report dated July 29, 2013 re EP Application No. 11168736.4. 10 pages	
	13	EP Examination Report dated June 3, 2013 in EP Application No. 05852180.8. 8 pages	
	14	EP Extended European Search Report dated March 27, 2012 re EP Application No. 11168734.9. 9 pages	
	15	EP Extended European Search Report dated March 27, 2012 re EP Application No. 11168735.6. 9 pages	
	16	EP Extended European Search Report dated March 28, 2012 re EP Application No. 11168736.4. 11 pages	
	17	EP Extended Search Report dated December 30, 2011 re EP Application No. 11179126.5. 10 pages	
	18	EP Extended Search Report dated December 30, 2011 re EP Application No. 11184623.4. 9 pages	
	19	EP Extended Search Report dated January 2, 2012 re EP Application No. 11184627.5. 7 pages	
	20	EP Office Action dated April 24, 2013 in EP Application No. 11179126.5. 9 pages	

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Filing Date	12 Apr 2017
First Named Inventor	Ware, Frederick (Fred)
Art Unit	2827
Examiner Name	
Attorney Docket Number	RA378.C3C1C1.US

Sheet 14 of 27

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	21	EP Office Action dated April 24, 2013 in EP Application No. 11184627.5. 7 pages	
	22	EP Office Action dated March 23, 2012 re EP Application No. 05852180.8. 5 pages	
	23	EP Office Communication dated August 1, 2013 in EP Application 11168735.6. 23 pages	
	24	EP Office Communication dated August 1, 2013 re EP Application No. 11168734.9. 24 pages	
	25	EP Office Communication dated January 11, 2012 re EP Application No. 07782931.5. 7 pages	
	26	EP Office Communication dated November 24, 2010 re EP Application No. 09167223.8. 6 pages	
	27	EP Official Communication dated September 27, 2012 in EP Application No. 09167223.8-1233. 2 pages	
	28	EP Provision of a Copy of the Minutes in Accordance With Rule 124(4) EPC with mail date of 3/15/2016 re EP Appln. No. 05852180.8. 7 Pages.	
	29	EP Provision of a Copy of the Minutes Rule 124(4) EPC dated January 27, 2014 re EP Application No. 07782931.5. 12 pages	
	30	EP Reponse with EP Appln. No. 11168736.4 filed on 1/16/2016 in Response to the Summons to Attend Oral Proceedings of 8/17/2015. 31 Pages.	

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	31	EP Response dated 10/8/2013 in EP Application No. 05852180.8, Includes New Claims (Highlighted and Clear copies) and New Description pages 2, 2a, and 2b (Highlighted and Clear copies). 47 pages	
	32	EP Response dated April 15, 2010 to the Official Communication dated 5 October 2009 re EP Application No. 07783931.5-1233. 25 pages	
	33	EP Response dated April 4, 2011 to the Official Communication dated 24 November 2010 re EP Application No. 09167223.8, Includes New Claims (Highlighted & Clear Copy) and Cross-Reference of New Claims. 41 pages	
	34	EP Response dated August 29, 2012 to the Official Communication dated 27 March 2012, Application No. 11168735.6. 21 pages	
	35	EP Response dated December 10, 2013 in EP Application No. 07782931.5, Includes the Main Request and Auxiliary Requests I-IV (Clear and Highlighted Copies). 63 pages	
	36	EP Response dated February 3, 2011 to the Official Communication dated 30 July 2010 re EP Application No. 05852180.8. 33 pages	
	37	EP Response dated February 5, 2014 in EP Application No. 11168736.4, Includes New Claims (Clear and Highlighted Copies) and New Description pages (Clear and Highlighted Copies). 30 pages	
	38	EP Response dated February 6, 2014 in EP Application No. 11168734.9, Includes New Claims (Highlighted and Clear Copies) and New Description pages. 26 pages	
	39	EP Response dated February 6, 2014 in EP Application No. 11168735.6, Includes New Claims (Highlighted and Clear Copies) and New Description pages. 23 pages	
	40	EP Response dated July 20, 2012 to the Official Communication dated January 11, 2012 in EP Application No. 07782931.5-1233, Includes New Claims (Clear and Highlighted Copies). 23 pages	

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	41	EP Response dated July 22, 2015 in EP Application No. 11168735.6, Includes Summons to Attend Oral Proceedings. 10 pages	
	42	EP Response dated July 23, 2015 in EP Application No. 05852180.8, Includes Summons to Attend Oral Proceedings. 14 pages	
	43	EP Response dated July 30, 2012 In response to the Official Communication dated February 6, 2012 and to the Extended European Search Report dated December 30, 2012, in EP Application No. 11 184 623.4, Includes New Claims (Clear and Highlighted Copies). 29 pages	
	44	EP Response dated July 30, 2012 in Response to the Official Communication dated February 6, 2012 and to the Extended European Search Report dated December 30, 2012, in EP Application No. 11 184 627.5, Includes New Description pp. 2, 2a, and 22. 13 pages	
	45	EP Response dated July 30, 2012 to the Official Communication dated February 6, 2011 and the extended European Search Report dated December 30, 2011, in EP Application No. 11 179 126.5, Includes New Claims (Clear and Highlighted Copies). 26 pages	
	46	EP Response dated November 4, 2013 in EP Application No. 11179126.5, Includes New Claims (Clear and Highlighted copies). 19 pages	
	47	EP Response dated November 4, 2013 in EP Application No. 11184623.4, Includes New Claims (Clear and Highlighted copies). 20 pages	
	48	EP Response dated November 4, 2013 in EP Application No. 11184627.5, Includes New Claims (Clear and Highlighted versions). 17 pages	
	49	EP Response dated September 6, 2012 to the Official Communication dated 2 May 2012, Application No. 11168734.9. 22 pages	
	50	EP Response dated September 6, 2012 to the Official Communication dated 2 May 2012, Application No. 11168736.4. 27 pages	

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	52	EP Response to Official Communication dated August 29, 2012, in EP Application No. 11168735.6, Includes New Claims (Clear and Highlighted Copies). 19 pages	
	53	EP Response to the Decision to Refuse European Patent Application of November 14, 2012, dated March 22, 2013 in EP Application No. 09 167 223.8. 71 pages	
	54	EP Response to the Official Communication of January 31, 2012 and the telephone call with Mr. Wolff of September 21, 2012, dated September 24, 2012 in EP Application No. 09167223.8. 11 pages	
	55	EP Response with EP Appln. No. 05852180.8 filed on 1/15/2016 in Response to Summons to Attend Oral Proceedings of 8/20/2015. 78 Pages.	
	56	EP Submission dated 3 February 2012 in Response to the Official Communication dated 31 January 2012 re EP Application No. 09167223.8. 4 pages	
	57	EP Submission dated January 15, 2014 in EP Application No. 07782931.5, Includes Auxiliary Request V (Clear and Highlighted copies). 9 pages	
	58	EP Summons to Attend Oral Proceedings dated August 17, 2015 in EP Application No. 11168734.9. 8 pages	
	59	EP Summons to Attend Oral Proceedings dated August 17, 2015 in EP Application No. 11168736.4. 9 pages	
	60	EP Summons to Attend Oral Proceedings re EP Application No. 09167223.8 dated 31 January 2012. 8 pages	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known	
Application Number	15/486,068
Filing Date	12 Apr 2017
First Named Inventor	Ware, Frederick (Fred)
Art Unit	2827
Examiner Name	
Attorney Docket Number	RA378.C3C1C1.US

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	61	Fairchild Semiconductor, "Design Optimization Techniques for Double Data Rate SDRAM Modules," July 2000. 6 pages	
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	63	First EP Examination Report with mail date of October 5, 2009, re EP Application No. 07 782 931.5-1233. 5 pages	
	64	Fujitsu Limited, "Memory CMOS 8 x 256K x 32 BIT DOUBLE DATA RATE FCRAM, MB81N643289-50/-60," pp. 1-56, Fujitsu Semiconductor Data Sheet, Advance Info., AEO.5E. 57 pages	
	65	GARRETT, Jr., Billy, U.S. Application No. 09/837,307 filed April 17, 2007, re Application and Figures As Filed. 54 pages	
	66	GIACALONE et al., "SP23.2: A 1MB, 100MHz Integrated L2 Cache Memory with 128b Interface and ECC Protection," IEEE ISSCC, February 1996, pp. 370-371/475. 3 pages	
	67	HAMPEL, Craig, U.S. Application No. 11/381,349 filed May 2, 2006, re Reply Brief in Response to Examiner's Answer mailed February 8, 2010. 6 pages	
	68	HAMPEL, Craig, U.S. Application No. 12/392,071 filed February 24, 2009, re Office Action with mail date of February 17, 2011. 19 pages	
	69	HIROSE et al., "A 20-ns 4-Mb CMOS SRAM with Hierarchical Word Decoding Architecture," IEEE, October 1990, pp. 1068-1072, Vol. 25, No. 5. 8 pages	
	70	International Preliminary Report on Patentability (Chapter 1) dated April 12, 2007, re International Application No PCT/US2005/032770. 6 pages	

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	72	International Preliminary Report on Patentability (Chapter II) with mailing date of April 9, 2010 re Int'l. Application No. PCT/US07/67814. 7 pages	
	73	International Preliminary Report on Patentability with mailing date of April 9, 2010 re Int'l. Application No. PCT/US07/67814. 7 pages	
	74	International Search Report and the Written Opinion for International Application No. PCT/US2007/067814, dated February 29, 2008. 18 pages	
	75	International Search Report and Written Opinion dated January 26, 2006 in International Application No. PCT/US2005/032770. 9 pages	
	76	International Search Report and Written Opinion dated January 4, 2006 in International Application No. PCT/US2005/028728. 5 pages	
	77	International Search Report and Written Opinion dated May 10, 2006 in International Application No. PCT/US2005/042722. 15 pages	
	78	International Search Report and Written Opinion in International Application No. PCT/US/2005/032770, dated January 26, 2006. 12 pages	
	79	Invitation to Pay Additional Fees from the International Searching Authority in International Application PCT/US2007/067814, dated December 17, 2007. 8 pages	
	80	JEDEC, "Minutes of Meeting No. 71, JC-42.3 Committee on RAM Memories," including Proposal to Add Number of Banks Option to the Mode Register for 64M SDRAM, Joint Electron Device Engineering Council (JEDEC), May 25, 1994, New York, pp. 1-14 plus Attachment T. 8 pages	

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	81	JP Office Action dated June 19, 2012 for JP Application No. 2009-510005. 6 Pages. (With Translation)	✓
	82	JP Office Action dated October 27, 2011 re JP Application No. 2007-543517. 18 pages. (With Translation)	✓
	83	JP Office Action for JP Appln. No. 2015-152586 with Mail Date of 9/2/2016. 7 Pages. (With Translation)	✓
	84	JP Response (Argument and Amendment) dated June 7, 2013 in JP Application No. 2007-543517, Includes English Translation. 28 pages	✓
	85	JP Response dated April 26, 2012, re Argument and Amendment to the Office Action dated October 27, 2011 in JP Application No. 2007-543517. 21 pages. (With Translation)	✓
	86	KIRIHATA et al., "A 390-mm2, 16-Bank, 1-Gb DDR SDRAM with Hybrid Bitline Architecture," IEEE Journal of Solid-State Circuits, Vol. 34, No. 11, November 1999, pp. 1580-1588. 10 pages	
	87	KOIKE et al., "SP23.1: A 60ns 1Mb Nonvolatile Ferroelectric Memory with Non-Driven Cell Plate Line Write/Read Scheme," ISSCC, February 10, 1996, pp. 368-379/475. 3 pages	
	88	Konishi et al., "Session XVIII: STATIC RAMs, FAM 18.6: A 64Kb CMOS RAM," IEEE International Solid State Circuits Conference, February 12, 1982, pp. 258-259. 3 pages	
	89	KR Office Action dated May 9, 2012 re KR Application No. 2007-7014584. 4 pages. (With Translation)	✓
	90	KR Response (Argument and Amendment) dated May 31, 2013 in KR Application No. 2007-7014584, Includes English Translation of Argument and Claims. 133 pages	✓

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	91	KR Response (Argument/Amendment) dated June 18, 2012 in KR Application No. 10-2007-7014584. 123 pages	✓
	92	MALVIYA et al., "Module Threading Technique to Improve DRAM Power and Performance," D&R Industry Articles, dated March 11, 2011, Copyright 2009. 9 pages	
	93	MASUMOTO, Rodney T., "Configurable On-Chip RAM Incorporated Into High Speed Logic Array," Proceedings of the IEEE 1985 Custom Integrated Circuits Conference, May 20 - 23, 1985, pp. 240-243. 6 pages	
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	97	MICRON TECHNOLOGY, INC., "Graphics DDR3 DRAM," Advance, 256 Mb x 32 GDDR3 DRAM, © 2003, pp. 1-67. 67 pages	
	98	Micron Technology, Inc., "Micron Synchronous DRAM 128Mb: x32 SDRAM," pp. 1-52, Rev. 9/00. 52 pages	
	99	Micron Technology, Inc., "Synchronous DRAM," Rev. April 1996. 43 pages	
	100	Minutes of Meeting No. 70, JC-42.3 Committee on RAM Memories, March 9, 1994, Orlando, Florida. 41 pages	

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	102	NITTA et al., "SP23.5: A 1.6GB/s Data-Rate 1Gb Synchronous DRAM with Hierarchical Square-Shaped Memory Block & Distributed Bank Architecture," IEEE ISSCC Digest of Technical Papers, pp. 376-377, 477, February 10, 1996. 3 pages	
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	104	Notice of Allowance and Fee(s) Due dated August 4, 2011 re U.S. Application No. 12/392,071. 22 pages	
	105	Nvidia Corporation, "GeForce3: Lightspeed Memory Architecture," Technical Brief, pp. 1-9. 11 pages	
	106	Office Action with mail date of 1/5/2016 re Japanese Application No. 2014-095678. 9 Pages. (With Translation)	
	107	Official Communication with Extended European Search Report for EP Application No. 09167223.8 - 1233, dated October 6, 2009. 8 pages	
	108	Rambus Inc., "Micro-Threading," dated April 3, 2011, found online at rambus.com/in/.../microthreading.html. 4 pages	
	109	Response dated January 7, 2011 to the Notice of Appeal filed October 7, 2010 re U.S. Application No. 12/392,071, Includes Request for Continued Examination. 15 pages	
	110	Response dated May 17, 2011 to the Office Action mailed February 17, 2011 re U.S. Application No. 12/392,071 26 pages	

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	111	Response to Office Action of May 5, 2009, dated October 5, 2009, re Serial No. 11/767,863 filed on June 25, 2007. 20 pages	
	112	Response to the Official Communication dated January 31, 2012 (Summons to Attend Oral Proceedings), dated August 28, 2012 in EP Application No. 09167223.8. 55 pages	
	113	SAEKI et al., "SP 23.4: A 2.5 ns Clock Access 250MHz 256Mb SDRAM with a Synchronous Mirror Delay," IEEE ISSCC Digest of Technical Papers, pp. 374-375, 476, February 10, 1996. 3 pages	
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	115	Samsung Electronics, "SDRAM Device Operations," 1999. 42 pages	
	116	SATOH et al., "A 209K-Transistor ECL Gate Array with RAM," IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, October 1989, pp. 1275-1281. 7 pages	
	117	SCHUETTE, Michael, "Rambus/Kingston Threaded DDR3 Modules," dated October 8, 2009, last updated October 24, 2009. 8 pages	
	118	Standards Information Network, IEEE Press, "The Authoritative Dictionary of IEEE Standards Terms," Copyright 2000, IEEE 100, Seventh Edition, p. 252. 2 pages	
	119	SUGIBAYASHI et al., "A 30-ns 256-Mb DRAM with a Multidivided Array Structure," IEEE, November 1993, pp. 1092-1098, Vol. 28, No. 11. 8 pages	
	120	SUGIBAYASHI et al., "WP3.5: A 30ns 256Mb DRAM with Multi-Divided Array Structure," ISSCC February 1993, pp. 50-51/262. 3 pages	

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	122	TAKASE et al., "WP 24.1 A 1.6GB/s DRAM with Flexible Mapping Redundancy Technique and Additional Refresh Scheme," ISSCC99/Session 24/Paper, Toshiba Corp., WP 24.1, February 17, 1999. 2 pages	
	123	TAKASE et al., "WP 24.1: A 1.6GB/s DRAM with Flexible Mapping Redundancy Technique and Additional Refresh Scheme," IEEE International Solid-State Circuits Conference, 1999. 8 pages	
	124	WARE et al., "Micro-threaded Row and Column Operations in a DRAM Core," Rambus White Paper, March 2005. 7 pages	
	125	WARE et al., U.S. Application No. 12/391,873 filed February 24, 2009, re Notice of Allowance and Fee(s) Due mailed August 31, 2010. 10 pages	
	126	WARE et al., U.S. Application No. 12/391,873 filed February 24, 2009, re Notice of Allowance and Fee(s) Due mailed November 3, 2010. 11 pages	
	127	WARE et al., U.S. Application No. 13/019,785 filed February 2, 2011, re Notice of Allowance and Fee(s) Due mailed June 29, 2011. 14 pages	
	128	WARE, Frederick A., "Direct RDRAM 256/288-Mbit (512Kx16/18x32s) Data Sheet," Preliminary Information, Rambus Inc., Document DL0060 Version 0.90, 1999, pp. 1-66. 66 pages	
	129	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Amendment mailed January 11, 2011. 10 pages	
	130	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Amendment/Response to Office Action submitted August 4, 2011. 12 pages	

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

	Complete if Known
Application Number	15/486,068
Filing Date	12 Apr 2017
First Named Inventor	Ware, Frederick (Fred)
Art Unit	2827
Examiner Name	
Attorney Docket Number	RA378.C3C1C1.US

Sheet 25 of 27

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	131	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Appeal Brief mailed April 6, 2010. 28 pages	
	132	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Corrected Response submitted February 22, 2012 to the Office Action of November 23, 2011. 17 pages	
	133	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Final Office Action mailed November 23, 2011. 33 pages	
	134	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Office Action mailed February 8, 2011. 3 pages	
	135	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Office Action mailed July 9, 2010. 17 pages	
	136	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Office Action mailed March 11, 2011. 37 pages	
	137	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Office Action mailed March 21, 2012. 36 pages	
	138	WARE, Frederick, U.S. Application No. 10/998,402 filed November 29, 2004, re Response submitted February 22, 2012 to the Office Action of November 23, 2011, Includes Request for Continued Examination. 21 pages	
	139	WARE, Frederick, U.S. Application No. 11/767,863 filed June 25, 2007, re Final Office Action mailed March 1, 2010. 17 pages	
	140	WARE, Frederick, U.S. Application No. 11/767,863 filed June 25, 2007, re Final Office Action mailed November 25, 2011. 30 pages	

Examiner Signature	/Gary W. Cygiel/	Date Considered	06/24/2018

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Sheet 26 of 27

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Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	141	WARE, Frederick, U.S. Application No. 11/767,863 filed June 25, 2007, re Notice of Appeal from the Examiner to The Board of Patent Appeals and Interferences dated July 30, 2010. 1 page	
	142	WARE, Frederick, U.S. Application No. 11/767,863 filed June 25, 2007, re Office Action mailed April 7, 2010. 3 pages	
	143	WARE, Frederick, U.S. Application No. 11/767,863 filed June 25, 2007, re Office Action mailed March 10, 2011. 23 pages	
	144	WARE, Frederick, U.S. Application No. 11/767,863 filed June 25, 2007, re Office Action mailed March 22, 2012. 34 pages	
	145	WARE, Frederick, U.S. Application No. 11/767,863 filed June 25, 2007, re Response to Notice of Appeal submitted December 24, 2010. 18 pages	
	146	WARE, Frederick, U.S. Application No. 11/767,863 filed June 25, 2007, re Response to Office Action mailed March 10, 2011. 15 pages	
	147	WARE, Frederick, U.S. Application No. 11/767,863 filed on June 25, 2007, re Response After Final Office Action mailed March 24, 2010. 15 pages	
	148	WARE, Frederick, U.S. Application No. 13/239,846 filed November 15, 2011, re Preliminary Amendment submitted November 16, 2011, Includes Terminal Disclaimer(s). 19 pages	
	149	WARE, Frederick, U.S. Application No. 13/239,846 filed September 22, 2011, re Corrected Notice of Allowability mailed January 17, 2012. 5 pages	
	150	WARE, Frederick, U.S. Application No. 13/239,846 filed September 22, 2011, re Notice of Allowance and Fee(s) Due mailed December 6, 2011. 47 pages	

Examiner Signature	/Gary W. Cygiel/	Date Considered	06/24/2018

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	151	YAMASHITA et al., "FA 15.2: A 3.84 GIPS Integrated Memory Array Processor LSI with 64 Processing Elements and 2-Mb SRAM," IEEE International Solid-State Circuit Conference, pp. 260-261, February 1994. 3 pages	
	152	YOO et al., "17.7: A 1.8V 700Mb/s/pin 512Mb DDR-II SDRAM with On-Die Termination and Off-Chip Driver Calibration", ISSCC, Feb. 2003, pp 312-313, 495, 250-251, 535. 6 pages	
	153	YOO et al., "A 150 MHZ 8-Banks 256M Synchronous DRAM with Wave Pipelining Methods," IEEE ISSCC, Digest of Technical Papers, pp. 250-251, 374, February 17, 1995. 3 pages	
	154	YOO et al., "SP23.6 A 32-Bank 1Gb DRAM with 1GB/s Bandwidth," ISSCC, February 1996, pp. 378-379/477. 3 pages	
	155	YOON et al., "A 2.5V 333Mb/pin 1Gb Double Data Rate SDRAM," ISSCC Digest of Technical Papers, February 17, 1999. 11 pages	
	156	ZHAO et al., "TA 11.6: An 18Mb, 12.3GB/s CMOS Pipeline-Burst Cache SRAM with 1.54Gb/pin," IEEE International Solid-State Circuits Conference, 1999. 10 pages	
	157	ZHENG et al., "Decoupled DIMM: Building High-Bandwidth Memory System Using Low-Speed DRAM Devices," ISCA '09, dated June 20-24, 2009. 12 pages	

Examiner Signature	/Gary W. Cygiel/	Date Considered	06/24/2018

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	14473	eDRAM or (embedded adj DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L2	1059	L1 and concurrent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L3	144	L2 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L4	14473	eDRAM or (embedded adj DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L5	1059	L4 and concurrent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L6	144	L5 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L7	86578	(column or row) near address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L8	7519	L7 and interleav$3	US-PGPUB;	OR	ON	2018/06/24

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			16:09
L9	66820	column near address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L10	684	L9 with interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L11	174	L10 with (row near address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L12	79629	column near2 address$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L13	11028	L12 with (multiple or plural$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L14	145	L13 with ((one or single) with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L15	185145	column with (access$3 or address$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L16	26929	L15 with (multiple or plural$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2018/06/24 16:09

			IBM_TDB			
L17	11037	L16 and (concurrent or simultaneous or ("same" near2 time))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L18	6497	711/157.ccls. 711/167.ccls. 711/168.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L19	198	L17 and L18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L20	32	("3643236" | "4875196" | "5276642" | "5367494" | "5864505" | "6157560" | "6377492").PN. OR ("6587917").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:09
L21	6497	711/157.ccls. 711/167.ccls. 711/168.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L22	42	L21 and multi$mode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L23	176803	(time near2 multiplex$3) or time$1multiplex$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L24	376	L23 with (memory near2 (bank or array or (sub$1bank or subbank)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L25	60	L24 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09

L26	1302	TDM with RAS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L27	270	TDM with CAS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L28	2	L26 and L27	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L29	0	L26 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L30	0	L27 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L31	304830	(memory near2 (bank or array or (sub$1bank or subbank)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L32	176	L31 with (time near3 (overlap$4 or over$1lap$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L33	5	L32 and 711/167-169.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L34	19	(memory near2 conflict) with (multiplex%3 or multi$1plex$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2018/06/24 16:09

			DERWENT; IBM_TDB			
L35	3045	(memory near2 interface) with (MUX or multiplex$3 or multi$1plex$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L36	139	inter$1threading	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L37	11	microthreading and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L38	31	micro$1threading and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L39	660	interleav$3 with SDRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L40	17	L39 and nibble	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L41	5	("6075728").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L42	20601	quadrant with (between or center or middle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L43	39	L42 with bank	US-PGPUB; USPAT; USOCR;	OR	OFF	2018/06/24 16:09

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L44	3	("20030052885").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L45	2	("6356975").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L46	8	link$1stagger$3 with data with transfer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L47	9	link$1stagger$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L48	36	"6591349"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L49	5	(("6591349") or ("20050015539")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L50	4	("5953252").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L51	41549	kazunari$.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L52	41	L51 and unidirectional	US-PGPUB;	OR	OFF	2018/06/24

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			16:09
L53	2407	(bank near2 switch$3) with (tim$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L54	255	L53 same (concurrent$2 or simultaneous$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L55	28	L53 same ((concurrent$2 or simultaneous$2) and sequential$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L56	6	(bank adj switching adj time)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L57	107	quadrant same time same interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L58	0	L57 and tcc	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L59	3	L57 and (bank with tim$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L60	4	L57 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2018/06/24 16:09

			IBM_TDB			
L61	12	"7290109"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L62	18	("5530828" | "5890192" | "6065092" | "6201735" | "6202138" | "6339817" | "6385688" | "6397314").PN. OR ("7290109").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:09
L63	5	("6065092").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L64	245	("4161040" | "4272832" | "4290120" | "4361869" | "4417302" | "4665483" | "4697112" | "4833648" | "4843264" | "4935868" | "5036231" | "5081575" | "5099452" | "5218690" | "5243703" | "5254883" | "5261064" | "5268639" | "5282174" | "5299156" | "5319755" | "5325053" | "5337285" | "5355391" | "5357195" | "5388237" | "5390308" | "5408129" | "5422529" | "5432823" | "5434818" | "5440523" | "5452436" | "5454082" | "5473575" | "5481496" | "5485490" | "5499385" | "5513327" | "5542067" | "5630163").PN. OR ("6065092").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:09
L65	4	("5995438").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L66	5	("6075728").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L67	1846	ware-fred$.in. or hampel-craig$.in. or richardson-wayne$.in. or bellows-chad$.in. or lai-lawrence$.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L68	1	L67 and (sequential$2 and bank and row and activate and (concurrent$2 or sequential$2) and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2018/06/24 16:09

			IBM_TDB			
L69	1	L67 and (sequential$2 and bank and row and activate and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L70	5	L67 and (bank and row and activate and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L71	1	("5870347").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:09
L72	191	("4096402" | "4404474" | "4638187" | "4789796" | "4958088" | "4984204" | "5122690" | "5128560" | "5128563" | "5134311" | "5150186" | "5165046" | "5179298" | "5194765" | "5220208" | "5239206" | "5254883" | "5274276" | "5276642" | "5278460" | "5281865" | "5311481" | "5321368" | "5347177" | "5347179" | "5361002" | "5390308" | "5400283" | "5438545" | "5440260" | "5457407" | "5473575" | "5497127" | "5498990" | "5506814" | "5508638" | "5515327" | "5568077" | "5574698" | "5576645" | "5578941" | "5581197" | "5590073" | "5619473" | "5621690" | "5627780" | "5627791" | "5631872" | "5636163" | "5636173" | "5636174" | "5638335" | "5650971" | "5668763" | "5694065").PN. OR ("5870347").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:09
L73	3	(sequential$2 and request and memory and synchronous and row and column and bank and array).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L74	1	("5701270").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:09
L75	69	("4570242" | "4608666" | "5117492" | "5159572" | "5161221" | "5200925" | "5245585" | "5265231" | "5278801" | "5287527" | "5329490" | "5353402" | "5377154" | "5383193" | "5388073" | "5426753" | "5452257" | "5469388" | "5477503" | "5491664").PN. OR ("5701270").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:09
L76	31689	(G06F3/0659 or G06F3/0613 or G06F3/0673 or G11C8/06 or G11C7/22 or G11C7/1042 or G11C11/4076 or G11C11/4097 or G11C7/1006).cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:09
L77	4394	(G06F3/0613).CPC.	US-PGPUB; USPAT;	OR	ON	2018/06/24 16:09

			USOCR			
L78	21	(G06F3/0613).CPC. and (G11C7/1042).CPC.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:09
L79	1	("5343438").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:09
L80	129	L67 and (time adj interval).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L81	81	L67 and (can).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L84	14473	eDRAM or (embedded adj DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L85	1059	L84 and concurrent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L86	144	L85 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L87	14473	eDRAM or (embedded adj DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L88	1059	L87 and concurrent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L89	144	L88 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2018/06/24 16:09

			EPO; JPO; DERWENT; IBM_TDB			
L90	86578	(column or row) near address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L91	7519	L90 and interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L92	66820	column near address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L93	684	L92 with interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L94	174	L93 with (row near address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L95	79629	column near2 address$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L96	11028	L95 with (multiple or plural$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L97	145	L96 with ((one or single) with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L98	185145	column with (access$3 or address$3)	US-PGPUB; USPAT;	OR	ON	2018/06/24 16:09

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L99	26929	L98 with (multiple or plural$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L100	11037	L99 and (concurrent or simultaneous or ("same" near2 time))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L101	6497	711/157.ccls. 711/167.ccls. 711/168.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L102	198	L100 and L101	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L103	32	("3643236" | "4875196" | "5276642" | "5367494" | "5864505" | "6157560" | "6377492").PN. OR ("6587917").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:09
L104	6497	711/157.ccls. 711/167.ccls. 711/168.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L105	42	L104 and multi$mode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L106	176803	(time near2 multiplex$3) or time$1multiplex$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L107	376	L106 with (memory near2 (bank or array or (sub$1bank or subbank)))	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2018/06/24 16:09

			EPO; JPO; DERWENT; IBM_TDB			
L108	60	L107 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L109	1302	TDM with RAS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L110	270	TDM with CAS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L111	2	L109 and L110	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L112	0	L109 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L113	0	L110 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L114	304830	(memory near2 (bank or array or (sub$1bank or subbank)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L115	176	L114 with (time near3 (overlap$4 or over$1lap$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L116	5	L115 and 711/167-169.ccls.	US-PGPUB; USPAT;	OR	ON	2018/06/24 16:09

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L117	19	(memory near2 conflict) with (multiplex%3 or multi$1plex$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L118	3045	(memory near2 interface) with (MUX or multiplex$3 or multi$1plex$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L119	139	inter$1threading	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L120	11	microthreading and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L121	31	micro$1threading and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L122	660	interleav$3 with SDRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L123	17	L122 and nibble	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L124	5	("6075728").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09

L125	20601	quadrant with (between or center or middle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L126	39	L125 with bank	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L127	3	("20030052885").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L128	2	("6356975").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L129	8	link$1stagger$3 with data with transfer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L130	9	link$1stagger$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L131	36	"6591349"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L132	5	(("6591349") or ("20050015539")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L133	4	("5953252").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2018/06/24 16:09

			DERWENT; IBM_TDB			
L134	41549	kazunari$.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L135	41	L134 and unidirectional	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L136	2407	(bank near2 switch$3) with (tim$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L137	255	L136 same (concurrent$2 or simultaneous$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L138	28	L136 same ((concurrent$2 or simultaneous$2) and sequential$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L139	6	(bank adj switching adj time)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L140	107	quadrant same time same interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L141	0	L140 and tcc	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L142	3	L140 and (bank with tim$3)	US-PGPUB; USPAT; USOCR;	OR	OFF	2018/06/24 16:09

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L143	4	L140 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L144	12	"7290109"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L145	18	("5530828" | "5890192" | "6065092" | "6201735" | "6202138" | "6339817" | "6385688" | "6397314").PN. OR ("7290109").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:09
L146	5	("6065092").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L147	245	("4161040" | "4272832" | "4290120" | "4361869" | "4417302" | "4665483" | "4697112" | "4833648" | "4843264" | "4935868" | "5036231" | "5081575" | "5099452" | "5218690" | "5243703" | "5254883" | "5261064" | "5268639" | "5282174" | "5299156" | "5319755" | "5325053" | "5337285" | "5355391" | "5357195" | "5388237" | "5390308" | "5408129" | "5422529" | "5432823" | "5434818" | "5440523" | "5452436" | "5454082" | "5473575" | "5481496" | "5485490" | "5499385" | "5513327" | "5542067" | "5630163").PN. OR ("6065092").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:09
L148	4	("5995438").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L149	5	("6075728").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L150	1846	ware-fred$.in. or hampel-craig$.in. or richardson-wayne$.in. or bellows-chad$.in. or lai-lawrence$.in.	US-PGPUB; USPAT; USOCR;	OR	OFF	2018/06/24 16:09

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L151	1	L150 and (sequential$2 and bank and row and activate and (concurrent$2 or sequential$2) and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L152	1	L150 and (sequential$2 and bank and row and activate and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L153	5	L150 and (bank and row and activate and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L154	1	("5870347").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:09
L155	191	("4096402" | "4404474" | "4638187" | "4789796" | "4958088" | "4984204" | "5122690" | "5128560" | "5128563" | "5134311" | "5150186" | "5165046" | "5179298" | "5194765" | "5220208" | "5239206" | "5254883" | "5274276" | "5276642" | "5278460" | "5281865" | "5311481" | "5321368" | "5347177" | "5347179" | "5361002" | "5390308" | "5400283" | "5438545" | "5440260" | "5457407" | "5473575" | "5497127" | "5498990" | "5506814" | "5508638" | "5515327" | "5568077" | "5574698" | "5576645" | "5578941" | "5581197" | "5590073" | "5619473" | "5621690" | "5627780" | "5627791" | "5631872" | "5636163" | "5636173" | "5636174" | "5638335" | "5650971" | "5668763" | "5694065").PN. OR ("5870347").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:09
L156	3	(sequential$2 and request and memory and synchronous and row and column and bank and array).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L157	1	("5701270").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:09
L158	69	("4570242" | "4608666" | "5117492" | "5159572" | "5161221" | "5200925" | "5245585" | "5265231" | "5278801" | "5287527" | "5329490" | "5353402" |	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:09

		"5377154" | "5383193" | "5388073" | "5426753" | "5452257" | "5469388" | "5477503" | "5491664").PN. OR ("5701270").URPN.				
L159	31689	(G06F3/0659 or G06F3/0613 or G06F3/0673 or G11C8/06 or G11C7/22 or G11C7/1042 or G11C11/4076 or G11C11/4097 or G11C7/1006).cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:09
L160	4394	(G06F3/0613).CPC.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:09
L161	21	(G06F3/0613).CPC. and (G11C7/1042).CPC.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:09
L162	1	("5343438").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:09
L163	129	L150 and (time adj interval).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L164	81	L150 and (can).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:09
L165	2	(("5313603") or ("5822772")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:09
L168	135	sub$1bank.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L169	15	L168 and (row near2 activat$3) and (column near2 activat$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L170	11	L168 and ((shar$3 or common) with row with decoder)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L171	1669	((shar$3 or common) with row with decoder) and ((shar$3 or common) with column with decoder)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2018/06/24 16:09

			DERWENT; IBM_TDB			
L172	452	L171 and bank	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:09
L173	184	L171 and bank.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L174	28	("5329488" | "5384743" | "5621690" | "5682350" | "5777922" | "5812452" | "5847994").PN. OR ("6026021").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:10
L175	20	("4630230" | "4635233" | "4731761" | "4845677" | "5150330" | "5297102" | "5327389" | "5369619" | "5463590" | "5568427" | "5604697" | "5712827" | "5831924").PN. OR ("6209056").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:10
L176	14473	eDRAM or (embedded adj DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L177	1059	L176 and concurrent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L178	144	L177 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L179	14473	eDRAM or (embedded adj DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L180	1059	L179 and concurrent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L181	144	L180 and "711".clas.	US-PGPUB;	OR	ON	2018/06/24

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			16:10
L182	86578	(column or row) near address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L183	7519	L182 and interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L184	66820	column near address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L185	684	L184 with interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L186	174	L185 with (row near address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L187	79629	column near2 address$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L188	11028	L187 with (multiple or plural$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L189	145	L188 with ((one or single) with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2018/06/24 16:10

			IBM_TDB			
L190	185145	column with (access$3 or address$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L191	26929	L190 with (multiple or plural$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L192	11037	L191 and (concurrent or simultaneous or ("same" near2 time))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L193	6497	711/157.ccls. 711/167.ccls. 711/168.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L194	198	L192 and L193	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L195	32	("3643236" | "4875196" | "5276642" | "5367494" | "5864505" | "6157560" | "6377492").PN. OR ("6587917").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:10
L196	6497	711/157.ccls. 711/167.ccls. 711/168.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L197	42	L196 and multi$mode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L198	176803	(time near2 multiplex$3) or time$1multiplex$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10

L199	376	L198 with (memory near2 (bank or array or (sub$1bank or subbank)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L200	60	L199 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L201	1302	TDM with RAS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L202	270	TDM with CAS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L203	2	L201 and L202	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L204	0	L201 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L205	0	L202 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L206	304830	(memory near2 (bank or array or (sub$1bank or subbank)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L207	176	L206 with (time near3 (overlap$4 or over$1lap$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2018/06/24 16:10

			DERWENT; IBM_TDB			
L208	5	L207 and 711/167-169.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L209	19	(memory near2 conflict) with (multiplex%3 or multi$1plex$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L210	3045	(memory near2 interface) with (MUX or multiplex$3 or multi$1plex$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L211	139	inter$1threading	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L212	11	microthreading and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L213	31	micro$1threading and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L214	660	interleav$3 with SDRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L215	17	L214 and nibble	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L216	5	("6075728").PN.	US-PGPUB; USPAT; USOCR;	OR	OFF	2018/06/24 16:10

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L217	20601	quadrant with (between or center or middle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L218	39	L217 with bank	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L219	3	("20030052885").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L220	2	("6356975").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L221	8	link$1stagger$3 with data with transfer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L222	9	link$1stagger$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L223	36	"6591349"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L224	5	(("6591349") or ("20050015539")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L225	4	("5953252").PN.	US-PGPUB;	OR	OFF	2018/06/24

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			16:10
L226	41549	kazunari$.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L227	41	L226 and unidirectional	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L228	2407	(bank near2 switch$3) with (tim$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L229	255	L228 same (concurrent$2 or simultaneous$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L230	28	L228 same ((concurrent$2 or simultaneous$2) and sequential$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L231	6	(bank adj switching adj time)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L232	107	quadrant same time same interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L233	0	L232 and tcc	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2018/06/24 16:10

			IBM_TDB			
L234	3	L232 and (bank with tim$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L235	4	L232 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L236	12	"7290109"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L237	18	("5530828" | "5890192" | "6065092" | "6201735" | "6202138" | "6339817" | "6385688" | "6397314").PN. OR ("7290109").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:10
L238	5	("6065092").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L239	245	("4161040" | "4272832" | "4290120" | "4361869" | "4417302" | "4665483" | "4697112" | "4833648" | "4843264" | "4935868" | "5036231" | "5081575" | "5099452" | "5218690" | "5243703" | "5254883" | "5261064" | "5268639" | "5282174" | "5299156" | "5319755" | "5325053" | "5337285" | "5355391" | "5357195" | "5388237" | "5390308" | "5408129" | "5422529" | "5432823" | "5434818" | "5440523" | "5452436" | "5454082" | "5473575" | "5481496" | "5485490" | "5499385" | "5513327" | "5542067" | "5630163").PN. OR ("6065092").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:10
L240	4	("5995438").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L241	5	("6075728").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2018/06/24 16:10

			IBM_TDB			
L242	1846	ware-fred$.in. or hampel-craig$.in. or richardson-wayne$.in. or bellows-chad$.in. or lai-lawrence$.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L243	1	L242 and (sequential$2 and bank and row and activate and (concurrent$2 or sequential$2) and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L244	1	L242 and (sequential$2 and bank and row and activate and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L245	5	L242 and (bank and row and activate and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L246	1	("5870347").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:10
L247	191	("4096402" | "4404474" | "4638187" | "4789796" | "4958088" | "4984204" | "5122690" | "5128560" | "5128563" | "5134311" | "5150186" | "5165046" | "5179298" | "5194765" | "5220208" | "5239206" | "5254883" | "5274276" | "5276642" | "5278460" | "5281865" | "5311481" | "5321368" | "5347177" | "5347179" | "5361002" | "5390308" | "5400283" | "5438545" | "5440260" | "5457407" | "5473575" | "5497127" | "5498990" | "5506814" | "5508638" | "5515327" | "5568077" | "5574698" | "5576645" | "5578941" | "5581197" | "5590073" | "5619473" | "5621690" | "5627780" | "5627791" | "5631872" | "5636163" | "5636173" | "5636174" | "5638335" | "5650971" | "5668763" | "5694065").PN. OR ("5870347").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:10
L248	3	(sequential$2 and request and memory and synchronous and row and column and bank and array).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L249	1	("5701270").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:10

L250	69	("4570242" | "4608666" | "5117492" | "5159572" | "5161221" | "5200925" | "5245585" | "5265231" | "5278801" | "5287527" | "5329490" | "5353402" | "5377154" | "5383193" | "5388073" | "5426753" | "5452257" | "5469388" | "5477503" | "5491664").PN. OR ("5701270").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:10
L251	31689	(G06F3/0659 or G06F3/0613 or G06F3/0673 or G11C8/06 or G11C7/22 or G11C7/1042 or G11C11/4076 or G11C11/4097 or G11C7/1006).cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:10
L252	4394	(G06F3/0613).CPC.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:10
L253	21	(G06F3/0613).CPC. and (G11C7/1042).CPC.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:10
L254	1	("5343438").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:10
L255	129	L242 and (time adj interval).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L256	81	L242 and (can).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L257	14473	eDRAM or (embedded adj DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L258	1059	L257 and concurrent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L259	144	L258 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L260	14473	eDRAM or (embedded adj DRAM)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2018/06/24 16:10

			EPO; JPO; DERWENT; IBM_TDB			
L261	1059	L260 and concurrent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L262	144	L261 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L263	86578	(column or row) near address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L264	7519	L263 and interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L265	66820	column near address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L266	684	L265 with interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L267	174	L266 with (row near address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L268	79629	column near2 address$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L269	11028	L268 with (multiple or plural$3)	US-PGPUB; USPAT;	OR	ON	2018/06/24 16:10

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L270	145	L269 with ((one or single) with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L271	185145	column with (access$3 or address$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L272	26929	L271 with (multiple or plural$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L273	11037	L272 and (concurrent or simultaneous or ("same" near2 time))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L274	6497	711/157.ccls. 711/167.ccls. 711/168.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L275	198	L273 and L274	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L276	32	("3643236" | "4875196" | "5276642" | "5367494" | "5864505" | "6157560" | "6377492").PN. OR ("6587917").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:10
L277	6497	711/157.ccls. 711/167.ccls. 711/168.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L278	42	L277 and multi$mode	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2018/06/24 16:10

			EPO; JPO; DERWENT; IBM_TDB			
L279	176803	(time near2 multiplex$3) or time$1multiplex$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L280	376	L279 with (memory near2 (bank or array or (sub$1bank or subbank)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L281	60	L280 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L282	1302	TDM with RAS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L283	270	TDM with CAS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L284	2	L282 and L283	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L285	0	L282 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L286	0	L283 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L287	304830	(memory near2 (bank or array or (sub$1bank or subbank)))	US-PGPUB; USPAT;	OR	ON	2018/06/24 16:10

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L288	176	L287 with (time near3 (overlap$4 or over$1lap$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L289	5	L288 and 711/167-169.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L290	19	(memory near2 conflict) with (multiplex%3 or multi$1plex$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L291	3045	(memory near2 interface) with (MUX or multiplex$3 or multi$1plex$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L292	139	inter$1threading	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L293	11	microthreading and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L294	31	micro$1threading and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L295	660	interleav$3 with SDRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10

L296	17	L295 and nibble	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L297	5	("6075728").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L298	20601	quadrant with (between or center or middle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L299	39	L298 with bank	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L300	3	("20030052885").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L301	2	("6356975").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L302	8	link$1stagger$3 with data with transfer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L303	9	link$1stagger$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L304	36	"6591349"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2018/06/24 16:10

			DERWENT; IBM_TDB			
L305	5	(("6591349") or ("20050015539")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L306	4	("5953252").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L307	41549	kazunari$.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L308	41	L307 and unidirectional	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L309	2407	(bank near2 switch$3) with (tim$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L310	255	L309 same (concurrent$2 or simultaneous$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L311	28	L309 same ((concurrent$2 or simultaneous$2) and sequential$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L312	6	(bank adj switching adj time)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L313	107	quadrant same time same interleav$3	US-PGPUB; USPAT; USOCR;	OR	OFF	2018/06/24 16:10

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L314	0	L313 and tcc	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L315	3	L313 and (bank with tim$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L316	4	L313 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L317	12	"7290109"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L318	18	("5530828" | "5890192" | "6065092" | "6201735" | "6202138" | "6339817" | "6385688" | "6397314").PN. OR ("7290109").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:10
L319	5	("6065092").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L320	245	("4161040" | "4272832" | "4290120" | "4361869" | "4417302" | "4665483" | "4697112" | "4833648" | "4843264" | "4935868" | "5036231" | "5081575" | "5099452" | "5218690" | "5243703" | "5254883" | "5261064" | "5268639" | "5282174" | "5299156" | "5319755" | "5325053" | "5337285" | "5355391" | "5357195" | "5388237" | "5390308" | "5408129" | "5422529" | "5432823" | "5434818" | "5440523" | "5452436" | "5454082" | "5473575" | "5481496" | "5485490" | "5499385" | "5513327" | "5542067" | "5630163").PN. OR ("6065092").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:10
L321	4	("5995438").PN.	US-PGPUB; USPAT; USOCR;	OR	OFF	2018/06/24 16:10

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L322	5	("6075728").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L323	1846	ware-fred$.in. or hampel-craig$.in. or richardson-wayne$.in. or bellows-chad$.in. or lai-lawrence$.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L324	1	L323 and (sequential$2 and bank and row and activate and (concurrent$2 or sequential$2) and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L325	1	L323 and (sequential$2 and bank and row and activate and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L326	5	L323 and (bank and row and activate and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:10
L327	1	("5870347").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:10
L328	191	("4096402" | "4404474" | "4638187" | "4789796" | "4958088" | "4984204" | "5122690" | "5128560" | "5128563" | "5134311" | "5150186" | "5165046" | "5179298" | "5194765" | "5220208" | "5239206" | "5254883" | "5274276" | "5276642" | "5278460" | "5281865" | "5311481" | "5321368" | "5347177" | "5347179" | "5361002" | "5390308" | "5400283" | "5438545" | "5440260" | "5457407" | "5473575" | "5497127" | "5498990" | "5506814" | "5508638" | "5515327" | "5568077" | "5574698" | "5576645" | "5578941" | "5581197" | "5590073" | "5619473" | "5621690" | "5627780" | "5627791" | "5631872" | "5636163" | "5636173" | "5636174" | "5638335" | "5650971" | "5668763" | "5694065").PN. OR ("5870347").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:10

L329	3	(sequential$2 and request and memory and synchronous and row and column and bank and array).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:10
L330	1	("5701270").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:10
L331	69	("4570242" | "4608666" | "5117492" | "5159572" | "5161221" | "5200925" | "5245585" | "5265231" | "5278801" | "5287527" | "5329490" | "5353402" | "5377154" | "5383193" | "5388073" | "5426753" | "5452257" | "5469388" | "5477503" | "5491664").PN. OR ("5701270").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:10
L332	31689	(G06F3/0659 or G06F3/0613 or G06F3/0673 or G11C8/06 or G11C7/22 or G11C7/1042 or G11C11/4076 or G11C11/4097 or G11C7/1006).cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:10
L333	4394	(G06F3/0613).CPC.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:10
L334	21	(G06F3/0613).CPC. and (G11C7/1042).CPC.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:10
L335	1	("5343438").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:11
L336	129	L323 and (time adj interval).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:11
L337	81	L323 and (can).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/06/24 16:11
L338	2	(("5313603") or ("5822772")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/06/24 16:11
L339	135	sub$1bank.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:11
L340	15	L339 and (row near2 activat$3) and (column near2 activat$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2018/06/24 16:11

			DERWENT; IBM_TDB			
L341	11	L339 and ((shar$3 or common) with row with decoder)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:11
L342	1669	((shar$3 or common) with row with decoder) and ((shar$3 or common) with column with decoder)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:11
L343	452	L342 and bank	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:11
L344	184	L342 and bank.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/24 16:11
L345	28	("5329488" | "5384743" | "5621690" | "5682350" | "5777922" | "5812452" | "5847994").PN. OR ("6026021").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:11
L346	20	("4630230" | "4635233" | "4731761" | "4845677" | "5150330" | "5297102" | "5327389" | "5369619" | "5463590" | "5568427" | "5604697" | "5712827" | "5831924").PN. OR ("6209056").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/06/24 16:11

6/24/2018 4:25:36 PM
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BIB DATA SHEET

CONFIRMATION NO. 2908

SERIAL NUMBER	FILING or 371(c) DATE / RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/486,068	04/12/2017	711	2137	2016091 / RA378C3C1C1US

APPLICANTS

Rambus Inc., Sunnyvale, CA;

INVENTORS

Frederick A. Ware, Los Altos Hills, CA;
Craig E. Hampel, Los Altos, CA;
Wayne S. Richardson, Saratoga, CA;
Chad A. Bellows, Birmingham, MI;
Lawrence Lai, San Jose, CA;

**** CONTINUING DATA ***************************

This application is a CON of 14/449,610 08/01/2014 PAT 9652176
which is a CON of 13/901,014 05/23/2013 PAT 9292223
which is a CON of 10/998,402 11/29/2004 PAT 8595459

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

04/20/2017

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /GARY W CYGIEL/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	25	20	3

ADDRESS

MARC P. SCHUYLER / Rambus
P.O. BOX 2535
SARATOGA, CA 95070
UNITED STATES

TITLE

Memory Controller For Micro-Threaded Memory Operations

FILING FEE RECEIVED		
1740	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/486,068	04/12/2017	Frederick A. Ware	2016091 / RA378C3C1C1US	2908

78408 7590 10/05/2018

MARC P. SCHUYLER / Rambus
P.O. BOX 2535
SARATOGA, CA 95070

EXAMINER	
CYGIEL, GARY W	

ART UNIT	PAPER NUMBER
2137	

MAIL DATE	DELIVERY MODE
10/05/2018	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Applicant-Initiated Interview Summary	Application No. 15/486,068	Applicant(s) Ware et al.		
	Examiner Gary W Cygiel	Art Unit 2137	AIA (First Inventor to File) Status No	Page 1 of 1

All participants (applicant, applicants representative, PTO personnel):

1. Gary W Cygiel (Primary Examiner); Telephonic
2. Marc Schuyler (Attorney of Record); Telephonic

Date of Interview: 03 October 2018

Claims Discussed: Claim 1

Prior Art Discussed: Inoue et al.

Issues Discussed:

Item(s) under 35 U.S.C. 102:
Discussed controller circuitry and time intervals. Primary discussion regarding time intervals and their manner of implementation. Examiner indicated that the presented arguments appeared to be reasonable and would review them fully upon a formal submission.

/Gary W. Cygiel/ Primary Examiner, Art Unit 2137	

Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04
Please further see:
MPEP 713.04
Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)
37 CFR § 1.2 Business to be transacted in writing

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/486,068	Filing Date 04/12/2017	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	10/19/2018	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 22	Minus	** 22	= 0	X $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
HALLEY MASSEY

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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Electronic Patent Application Fee Transmittal

Application Number:	15486068
Filing Date:	12-Apr-2017
Title of Invention:	Memory Controller For Micro-Threaded Memory Operations
First Named Inventor/Applicant Name:	Frederick A. Ware
Filer:	Marc Philip Schuyler
Attorney Docket Number:	2016091 / RA378C3C1C1US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	2	100	200
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Extension - 1 month with $0 paid	1251	1	200	200
Miscellaneous:				
		Total in USD ($)		**400**

Electronic Acknowledgement Receipt

EFS ID:	34066404
Application Number:	15486068
International Application Number:	
Confirmation Number:	2908
Title of Invention:	Memory Controller For Micro-Threaded Memory Operations
First Named Inventor/Applicant Name:	Frederick A. Ware
Customer Number:	78408
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	2016091 / RA378C3C1C1US
Receipt Date:	19-OCT-2018
Filing Date:	12-APR-2017
Time Stamp:	17:53:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$400
RAM confirmation Number	102218INTEFSW17551200
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	RA378C3C1C1-Resp2OA-2018-10-19.pdf	102152 0025c5258c2924ca603da2d4aa944f9a2642145c	no	10
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32307 b50fd270d7325c361431e9ef8ac598a8c44f71a1	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	134459		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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New International Application Filed with the USPTO as a Receiving Office

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Frederick A. Ware	Filed:	12 April 2017
Title:	Micro-Threaded Memory	Art Unit:	2827
Serial No.:	15/486068	Conf.:	2908
Publ. No.:	20170286017		
Docket:	2016091 / RA378C3C1C1	Examiner:	Cygiel, Gary B.

RESPONSE TO 06/29/2018 OFFICE ACTION

Please consider this amendment in response to the Office Action mailed 6/29/2018. A one month extension of time is also hereby requested, to extend the response date to 10/29/2018. Fees for two extra dependent claims and for the one month extension are being concurrently paid via the EFS.

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In The Claims.

Please amend the claims as set forth below. This listing replaces all prior listings of claims.

1. (Canceled)

2. (Previously Presented) A memory controller to control a memory device, the memory device having a plurality of bank groups, the memory controller comprising:

circuitry to provide a clock signal to the memory device, the clock signal having clock transitions;

a command interface to transmit, to the memory device, row activation commands to instruct row activations and column access commands to instruct column accesses; and

circuitry to schedule issuance of the row activation commands and the column access commands from the command interface, such that

a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common bank group, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups, and

a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups.

3. (Previously Presented) The memory controller of claim 2, wherein:

each bank includes a first sub-bank and a second sub-bank;

the first sub-bank is in a first bank group of the plurality of bank groups; and

the second sub-bank is in a second bank group of the plurality of bank groups.

4. (Previously Presented) The memory controller of claim 3, wherein:

each sub-bank in the first bank group shares first row decoder circuitry and first column decoder circuitry with each other sub-bank in the first bank group; and

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each sub-bank in the second bank group shares second row decoder circuitry and second column decoder circuitry with each other sub-bank in the second bank group.

5. (Previously Presented) The memory controller of claim 3, wherein the circuitry to schedule is to schedule at least one column access command for each row activation command, in order to access a column within a row activated by a corresponding row activation command, and wherein the command interface is to transmit bank address information to the memory device for each row activation command and for each column access command, in order to select a bank and in order to select one of the bank groups in the plurality of bank groups.

6. (Previously Presented) The memory controller of claim 3, wherein the circuitry to schedule is to schedule for a given row activation command, at least two column access commands, in order to access different columns within a row activated by the given row activation command.

7. (Previously Presented) The memory controller of claim 2, wherein the memory controller also comprises a data interface to exchange data with the memory device via links, using respective, mutually-exclusive subsets of the links to exchange data in association with the back-to-back column accesses to banks within different bank groups.

8. (Previously Presented) The memory controller of claim 2, wherein:

the memory controller further comprises a data interface to exchange data with the memory device via links, in association with each column access command; and

the memory controller further comprises serialization/deserialization circuitry to exchange serialized data with the memory device over each of the links in association with each column access command.

9. (Previously Presented) The memory controller of claim 2, wherein the memory controller further comprises a data interface to exchange each of data, and write mask values with the memory device, via respective link subsets.

10. (Previously Presented) The memory controller of claim 2, wherein the memory controller is to interleave row activation commands and is to interleave column access commands for back-to-back

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data accesses in different bank groups, and is to transmit bank address information as part of each command of the row activation commands and column access commands, to select a bank group of the plurality of bank groups, and to select a bank within the selected bank group.

11. (Previously Presented) A memory controller to control a memory device, the memory device having a plurality of bank groups, the memory controller comprising:

circuitry to provide a clock signal to the memory device, the clock signal having clock transitions;

a command interface to transmit row activation commands and column access commands to the memory device, via a command bus;

a data interface to exchange data with the memory device in association with each column access command; and

circuitry coupled to the command interface to schedule issuance of the row activation commands and the column access commands to banks within the plurality of bank groups, such that

a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common one of the bank groups, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different ones of the bank groups, and

a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common one of the bank groups, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different ones of the bank groups;

wherein the memory controller is to transmit bank address information as part of each command of the row activation commands and column access commands, to communicate selection of a bank group of the plurality of bank groups, and to communicate selection of a bank within the selected bank group.

12. (Previously Presented) The memory controller of claim 11, wherein:

each bank includes a first sub-bank and a second sub-bank;

the first sub-bank is in a first bank group of the plurality of bank groups; and

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the second sub-bank is in a second bank group of the plurality of bank groups.

13. (Previously Presented) The memory controller of claim 12, wherein:

each sub-bank in the first bank group shares first row decoder circuitry and first column decoder circuitry with each other sub-bank in the first bank group; and

each sub-bank in the second bank group shares second row decoder circuitry and second column decoder circuitry with each other sub-bank in the second bank group.

14. (Previously Presented) The memory controller of claim 12, wherein the circuitry to schedule is to schedule at least one column access command for each row activation command, in order to access a column within a row activated by a corresponding row activation command, and wherein the command interface is to transmit bank address information to the memory device for each row activation command and for each column access command, in order to select a bank and in order to select one of the bank groups in the plurality of bank groups.

15. (Previously Presented) The memory controller of claim 12, wherein the circuitry to schedule is to schedule for a given row activation command, at least two column access commands, in order to access different columns within a row activated by the given row activation command.

16. (Previously Presented) The memory controller of claim 11, wherein the memory controller also comprises a data interface to exchange data with the memory device via links, using respective, mutually-exclusive subsets of the links to exchange data in association with the back-to-back column accesses to banks within different bank groups.

17. (Previously Presented) The memory controller of claim 11, wherein:

the memory controller further comprises a data interface to exchange data with the memory device via links, in association with each column access command; and

the memory controller further comprises serialization/deserialization circuitry to exchange serialized data with the memory device over each of the links in association with each column access command.

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18. (Previously Presented) The memory controller of claim 11, wherein the memory controller further comprises a data interface to exchange each of data, and write mask values with the memory device, via respective link subsets.

19. (Previously Presented) A method of operation in a memory controller, the memory controller to control a memory device, the memory device having a plurality of bank groups, the method comprising:

providing a clock signal to the memory device, the clock signal having clock transitions;

transmitting to the memory device, via a command interface, row activation commands to instruct row activations and column access commands to instruct column accesses; and

scheduling issuance of the row activation commands and the column access commands from the command interface, such that

a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common bank group, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups, and

a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups.

20. (Previously Presented) The method of claim 19, wherein:

each bank includes a first sub-bank and a second sub-bank;

the first sub-bank is in a first bank group of the plurality of bank groups;

the second sub-bank is in a second bank group of the plurality of bank groups;

each sub-bank in the first bank group shares row decoder circuitry and column decoder circuitry with each other sub-bank in the first bank group; and

each sub-bank in the second bank group shares row decoder circuitry and column decoder circuitry with each other sub-bank in the second bank group.

21. (Previously Presented) The method of claim 19, wherein:

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the method further comprises transmitting bank address information as part of each command of the row activation commands and column access commands, to communicate selection of a bank group of the plurality of bank groups, and to communicate selection of a bank within the selected bank group.

22. (New) The memory controller of claim 2, wherein:

the first interval is longer than the third interval and the second interval is longer than the fourth interval.

23. (New) The memory controller of claim 2, wherein:

the memory controller is to establish command queues respective to each of the banks in the memory device;

the memory controller further comprises logic to time-multiplex commands from the command queues for the banks for transmission to the memory device via the command interface; and

said logic is to interleave commands from the command queues in a manner that observes the first time interval, the second time interval, the third time interval and the fourth time interval.

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REMARKS

Applicant thanks the Examiner for the interview held on October 3, 2018. This document memorializes the points which were presented to the Examiner in that interview.

In the Office Action, the Examiner rejected claims 2, 7, 9-11, 16, 18-19 and 21 under 35 USC §102(b) as allegedly anticipated over USPT 5953257 to Inoue, rejected claims 8 and 12 under 35 USC §103(a) as allegedly obvious over Inoue, and rejected claims 3-6, 12-15 and 20 under 35 USC §103(a) as allegedly obvious over Inoue combined with Suh (USPT 6209056). Reconsideration is respectfully requested.

As the Examiner is aware for a rejection under 35 USC §102 to be proper, a single prior art reference must show the same invention. Applicant does not see where Inoue shows a memory controller, as claimed, nor does Applicant see the respective memory controller circuitry, memory controller command interface, or four time periods, as claimed. After scrutinizing Inoue, the only reference Applicant can find to how control is performed in Inoue is at Inoue's column 4, lines 57-63:

> "The DRAM further includes a logic circuit 300 for the input/output of a data signal.... a control circuit 400 for controlling the above circuits, and an external pin 500."

First, it is not seen how or why this structure necessarily shows a memory controller or components of a memory controller as claimed. For example, it appears to Applicant that the Examiner's position is that a memory controller and associated circuitry must be "somewhere" in the embedded DRAM of Inoue, but Applicant does not agree. For example, Applicant's independent claims require that a memory controller have circuitry to "provide a clock signal to the memory device," "a command interface to transmit, to the memory device, row activation commands to instruct row activations and column access commands to instruct column accesses," and circuitry to schedule issuance of the commands such that four specific time intervals are observed. Applicant does not see where Inoue shows a memory controller having any of circuitry to provide a clock signal to a memory device, a command interface to transmit row and column commands, and circuitry to schedule issuance of these commands according to four (minimum) time intervals, as claimed.

Second, Applicant notes that its claims recite a memory controller having "circuitry to schedule issuance of the ... commands ... such that" four time intervals are necessarily observed; the Examiner's position appears to be that Inoue's FIG. 7 shows this. However, Inoue's figures appear to only show example timing seen purely internally to an embedded DRAM device, and neither Inoue description nor

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figures teach anything about *scheduling issuance* of commands to a memory device (which is the subject of Applicant's claims) so that four time periods are observed. For example, see column 10 of Inoue (i.e., which discusses Inoue's FIGS. 7A-I, and which simply narrates an example operation within Inoue's embedded DRAM) - no detail or discussion is provided which would suggest that a memory controller enforces time intervals through its scheduling of commands. It is noted that Applicant's claims require this, because Applicant's claims recite "circuitry to schedule issuance of ... commands .... *such that*" the specific relative time periods are observed. Because Inoue does not show this, here also Inoue cannot anticipate the claims at-issue.

Thirdly, the Examiner's position also appears to be that in operation, Inoue shows analogies to the four claimed time intervals. However, Applicant disagrees here also. Inoue shows four banks (#1-4), each having two subbanks (A/B) where each subbank has a *dedicated* row decoder (i.e., there are eight row decoders total as stated at Inoue's column 11, line 38), but where a column decoder is *shared* across each A/B pair of subbanks. The only timing discussed by Inoue presenting any restriction at all relates to "interlock," i.e., Inoue states at his column 11, lines 42-55 that accesses to different banks bear "no restriction," whereas because subbanks A and B can experience interlock because they share a common column decoder. Inoue does not relate or have any teachings relating to scheduling of commands, as discussed above, but Inoue also does not show four different timing requirements between columns and rows in a memory device, as the Examiner appears to think, i.e., Applicant sees no structure, implicitly or otherwise in Inoue, which restricts in any manner Inoue's row commands can be issued to banks within a common "bank group," or how row timing differs for respective row commands sent to banks in respective bank groups versus Inoue's subbanks. Applicant notes that its claims distinguish Inoue here also, because Applicant's claims require

> "a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations *to banks within a common bank group*, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups."

In other words, as claimed, a memory controller supporting DRAM must enforce a first time interval within a given bank group in scheduling row commands to respective banks in that group, which is longer than an interval before a different bank group can be the subject of a row command, but Inoue does not show this (either in terms of scheduling or in terms of memory device operation, implied or otherwise). Similarly, as claimed, a memory controller supporting DRAM must enforce a second time interval between back to back row accesses to banks in respective bank groups and a fourth time

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interval between bank to back column accesses to bank in respective bank groups, and Inoue provides no indication that his circuitry (or that any memory controller anywhere) enforces different respective minimum timing for these accesses.

Whether the grounds of rejection is 35 USC §102 (or is 35 USC §103), it is the Examiner's burden to prove that a reference teaches something, and Inoue does not have teachings relevant to the four different intervals which are claimed, much less that a memory controller must observe such time intervals in scheduling issuance of commands. Suh does not supply the missing teachings, and therefore the cited art does not show all of the limitations of the claims, and no claim of record can be considered unpatentable.

It is therefore submitted that the current record does not support rejection of any of the claims. Because the independent claims are clearly patentable based on the current record, the dependent claims are also, and it is unnecessary to reach the merits of the rejection of dependent claims.

It is noted that the newly added claims add detail as to how the claimed memory controller operates, and is supported by way of example, by Applicant's FIGS. 14 and 29, among others. There are two new dependencies, including one which additionally characterizes differences between the four claimed time intervals, and one which introduces queue architecture in the memory controller and specifies that time interval observance operates in conjunction with a multiplexing function that interleaves commands from the various queues in a manner that enforces the time intervals (i.e., as minimums); Inoue does not show any of these things.

If it would be helpful for the Examiner to discuss any of the presented limitations, or if the Examiner has any questions or concerns, the Examiner is respectfully commanded to contact the undersigned using the contact information set forth below.

Respectfully submitted,
Attorney for Applicant

/Marc P. Schuyler/
Marc P. Schuyler, Reg. No. 35, 675
(408) 655-6375
marc@schuylerlawgroup.com

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MARC P. SCHUYLER / Rambus
P.O. BOX 2535
SARATOGA, CA 95070

EXAMINER
CYGIEL, GARY W

ART UNIT	PAPER NUMBER
2137	

DATE MAILED: 02/19/2019

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/486,068	04/12/2017	Frederick A. Ware	2016091 / RA378C3C1C1US	2908

TITLE OF INVENTION: Memory Controller For Micro-Threaded Memory Operations

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	05/20/2019

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THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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(Typed or printed name)
(Signature)
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/486,068	04/12/2017	Frederick A. Ware	2016091 / RA378C3C1C1US	2908

TITLE OF INVENTION: Memory Controller For Micro-Threaded Memory Operations

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	05/20/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
CYGIEL, GARY W	2137	711-168000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

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5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

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NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Silicon Motion Inc. Ex. 1002, Page 268
Silicon Motion Inc. v. K.Mizra LLC, IPR2024-01236

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/486,068	04/12/2017	Frederick A. Ware	2016091 / RA378C3C1C1US	2908

78408 7590 02/19/2019

MARC P. SCHUYLER / Rambus
P.O. BOX 2535
SARATOGA, CA 95070

EXAMINER	
CYGIEL, GARY W	

ART UNIT	PAPER NUMBER
2137	

DATE MAILED: 02/19/2019

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Silicon Motion Inc. Ex. 1002, Page 269
Silicon Motion Inc. v. K.Mizra LLC, IPR2024-01236

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/486,068	Applicant(s) Ware et al.	
	Examiner Gary W Cygiel	Art Unit 2137	AIA Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to submission by applicant dated 19OCT2018.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are See Continuation Sheet . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/Gary W. Cygiel/
Primary Examiner, Art Unit 2137

Continuation of 3. The allowed claim(s) is/are: 2-23 (renumbered as 1-22)

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Allowable Subject Matter

2. Claims 2-23 (*renumbered as 1-22*) are allowed.

3. The following is an examiner's statement of reasons for allowance:

The applicant's arguments (REMARKS:P9) regarding timing constraints are persuasive.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary W Cygiel whose telephone number is (571)270-1170. The examiner can normally be reached on Monday - Thursday 11am-3pm CST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Adam Queler can be reached on (571) 272-4140. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Gary W. Cygiel/
Primary Examiner, Art Unit 2137

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/486,068	Ware et al.
	Examiner	**Art Unit**
	Gary W Cygiel	2137

CPC						
Symbol					**Type**	**Version**
G06F	/	3	/	0659	F	2013-01-01
G11C	/	7	/	1006	I	2013-01-01
G11C	/	7	/	1042	I	2013-01-01
G11C	/	7	/	22	I	2013-01-01
G11C	/	11	/	4076	I	2013-01-01
G11C	/	11	/	4097	I	2013-01-01
G11C	/	8	/	06	I	2013-01-01
G06F	/	3	/	0613	I	2013-01-01
G06F	/	3	/	0673	I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	22	
/Gary W. Cygiel/ Primary Examiner, Art Unit 2137	13 February 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	20	1

U.S. Patent and Trademark Office

Part of Paper No.: 20190213

Silicon Motion Inc. Ex. 1002, Page 275
Silicon Motion Inc. v. K.Mizra LLC, IPR2024-01236

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/486,068	Ware et al.
	Examiner	**Art Unit**
	Gary W Cygiel	2137

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G06F	/	3	/	06
G11C7/10	/	7	/	10
G11C7/22	/	7	/	22
G11C8/06	/	8	/	06
G11C11/4076	/	11	/	4076
G11C11/4097	/	11	/	4097
	/		/	

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	22	
/Gary W. Cygiel/ Primary Examiner, Art Unit 2137	13 February 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	20	1

U.S. Patent and Trademark Office — Part of Paper No.: 20190213

Silicon Motion Inc. Ex. 1002, Page 276
Silicon Motion Inc. v. K.Mizra LLC, IPR2024-01236

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/486,068	Ware et al.
	Examiner	**Art Unit**
	Gary W Cygiel	2137

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1	9	10	20	19										
1	2	12	11	21	20										
2	3	13	12	22	21										
3	4	14	13	10	22										
4	5	15	14	11	23										
5	6	16	15												
6	7	17	16												
7	8	18	17												
8	9	19	18												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	22	
/Gary W. Cygiel/ Primary Examiner, Art Unit 2137	13 February 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	20	1

U.S. Patent and Trademark Office

Part of Paper No.: 20190213

Silicon Motion Inc. Ex. 1002, Page 277
Silicon Motion Inc. v. K.Mizra LLC, IPR2024-01236

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/486,068	Ware et al.
	Examiner	Art Unit
	Gary W Cygiel	2137

CPC - Searched*		
Symbol	Date	Examiner
within G06F 3/0613,0659	02/13/2019	GC
within G11C 8/06; 7/22,1042,1006; 11/4076,4097	02/13/2019	GC

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST text search (incl. inventor name and assignee)	06/24/2018	GC
Updated EAST text search	02/13/2019	GC

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	see attached EAST text search	02/13/2019	GC

Silicon Motion Inc. Ex. 1002, Page 276
Silicon Motion Inc. v. K.Mizra LLC, IPR2024-01236

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BIB DATA SHEET

CONFIRMATION NO. 2908

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/486,068	04/12/2017	711	2137	2016091 / RA378C3C1C1US

APPLICANTS

Rambus Inc., Sunnyvale, CA;

INVENTORS

Frederick A. Ware, Los Altos Hills, CA;
Craig E. Hampel, Los Altos, CA;
Wayne S. Richardson, Saratoga, CA;
Chad A. Bellows, Birmingham, MI;
Lawrence Lai, San Jose, CA;

**** CONTINUING DATA ***************************

This application is a CON of 14/449,610 08/01/2014 PAT 9652176
which is a CON of 13/901,014 05/23/2013 PAT 9292223
which is a CON of 10/998,402 11/29/2004 PAT 8595459

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

04/20/2017

Foreign Priority claimed ❑ Yes ☑ No 35 USC 119(a-d) conditions met ❑ Yes ☑ No Verified and Acknowledged /GARY W CYGIEL/ Examiner's Signature	❑ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	25	~~20~~ 22	3

ADDRESS

MARC P. SCHUYLER / Rambus
P.O. BOX 2535
SARATOGA, CA 95070
UNITED STATES

/GWC/
02/13/2019

TITLE

Memory Controller For Micro-Threaded Memory Operations

FILING FEE RECEIVED		
1940	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other _____ ❑ Credit

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	15643	eDRAM or (embedded adj DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L4	1381	L3 and concurrent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L5	144	L4 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L6	15643	eDRAM or (embedded adj DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L7	1381	L6 and concurrent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L8	144	L7 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L9	89184	(column or row) near address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L10	7776	L9 and interleav$3	US-PGPUB;	OR	ON	2019/02/13

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:19
L11	68769	column near address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L12	690	L11 with interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L13	177	L12 with (row near address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L14	81979	column near2 address$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L15	11299	L14 with (multiple or plural$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L16	150	L15 with ((one or single) with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L17	192102	column with (access$3 or address$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L18	27916	L17 with (multiple or plural$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2019/02/13 11:19

			IBM_TDB			
L19	11340	L18 and (concurrent or simultaneous or ("same" near2 time))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L20	6709	711/157.ccls. 711/167.ccls. 711/168.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L21	198	L19 and L20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L22	33	("3643236" | "4875196" | "5276642" | "5367494" | "5864505" | "6157560" | "6377492").PN. OR ("6587917").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:19
L23	6709	711/157.ccls. 711/167.ccls. 711/168.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L24	42	L23 and multi$mode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L25	184096	(time near2 multiplex$3) or time$1multiplex$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L26	378	L25 with (memory near2 (bank or array or (sub$1bank or subbank)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L27	60	L26 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19

L28	1361	TDM with RAS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L29	288	TDM with CAS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L30	2	L28 and L29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L31	0	L28 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L32	0	L29 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L33	317717	(memory near2 (bank or array or (sub$1bank or subbank)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L34	180	L33 with (time near3 (overlap$4 or over$1lap$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L35	5	L34 and 711/167-169.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L36	21	(memory near2 conflict) with (multiplex%3 or multi$1plex$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/02/13 11:19

			DERWENT; IBM_TDB			
L37	3152	(memory near2 interface) with (MUX or multiplex$3 or multi$1plex$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L38	141	inter$1threading	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L39	11	microthreading and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L40	31	micro$1threading and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L41	666	interleav$3 with SDRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L42	17	L41 and nibble	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L43	5	("6075728").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L44	21308	quadrant with (between or center or middle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L45	40	L44 with bank	US-PGPUB; USPAT; USOCR;	OR	OFF	2019/02/13 11:19

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L46	3	("20030052885").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L47	4	("6356975").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L48	8	link$1stagger$3 with data with transfer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L49	9	link$1stagger$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L50	37	"6591349"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L51	5	(("6591349") or ("20050015539")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L52	4	("5953252").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L53	42573	kazunari$.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L54	42	L53 and unidirectional	US-PGPUB;	OR	OFF	2019/02/13

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:19
L55	2511	(bank near2 switch$3) with (tim$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L56	259	L55 same (concurrent$2 or simultaneous$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L57	28	L55 same ((concurrent$2 or simultaneous$2) and sequential$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L58	6	(bank adj switching adj time)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L59	108	quadrant same time same interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L60	0	L59 and tcc	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L61	3	L59 and (bank with tim$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L62	4	L59 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2019/02/13 11:19

			IBM_TDB			
L63	17	"7290109"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L64	23	("5530828" | "5890192" | "6065092" | "6201735" | "6202138" | "6339817" | "6385688" | "6397314").PN. OR ("7290109").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:19
L65	5	("6065092").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L66	247	("4161040" | "4272832" | "4290120" | "4361869" | "4417302" | "4665483" | "4697112" | "4833648" | "4843264" | "4935868" | "5036231" | "5081575" | "5099452" | "5218690" | "5243703" | "5254883" | "5261064" | "5268639" | "5282174" | "5299156" | "5319755" | "5325053" | "5337285" | "5355391" | "5357195" | "5388237" | "5390308" | "5408129" | "5422529" | "5432823" | "5434818" | "5440523" | "5452436" | "5454082" | "5473575" | "5481496" | "5485490" | "5499385" | "5513327" | "5542067" | "5630163").PN. OR ("6065092").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:19
L67	4	("5995438").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L68	5	("6075728").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L69	1896	ware-fred$.in. or hampel-craig$.in. or richardson-wayne$.in. or bellows-chad$.in. or lai-lawrence$.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L70	1	L69 and (sequential$2 and bank and row and activate and (concurrent$2 or sequential$2) and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2019/02/13 11:19

			IBM_TDB			
L71	1	L69 and (sequential$2 and bank and row and activate and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L72	5	L69 and (bank and row and activate and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L73	1	("5870347").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:19
L74	192	("4096402" | "4404474" | "4638187" | "4789796" | "4958088" | "4984204" | "5122690" | "5128560" | "5128563" | "5134311" | "5150186" | "5165046" | "5179298" | "5194765" | "5220208" | "5239206" | "5254883" | "5274276" | "5276642" | "5278460" | "5281865" | "5311481" | "5321368" | "5347177" | "5347179" | "5361002" | "5390308" | "5400283" | "5438545" | "5440260" | "5457407" | "5473575" | "5497127" | "5498990" | "5506814" | "5508638" | "5515327" | "5568077" | "5574698" | "5576645" | "5578941" | "5581197" | "5590073" | "5619473" | "5621690" | "5627780" | "5627791" | "5631872" | "5636163" | "5636173" | "5636174" | "5638335" | "5650971" | "5668763" | "5694065").PN. OR ("5870347").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:19
L75	3	(sequential$2 and request and memory and synchronous and row and column and bank and array).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L76	1	("5701270").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:19
L77	69	("4570242" | "4608666" | "5117492" | "5159572" | "5161221" | "5200925" | "5245585" | "5265231" | "5278801" | "5287527" | "5329490" | "5353402" | "5377154" | "5383193" | "5388073" | "5426753" | "5452257" | "5469388" | "5477503" | "5491664").PN. OR ("5701270").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:19
L78	34663	(G06F3/0659 or G06F3/0613 or G06F3/0673 or G11C8/06 or G11C7/22 or G11C7/1042 or G11C11/4076 or G11C11/4097 or G11C7/1006).cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:19
L79	4772	(G06F3/0613).CPC.	US-PGPUB; USPAT;	OR	ON	2019/02/13 11:19

			USOCR			
L80	24	(G06F3/0613).CPC. and (G11C7/1042).CPC.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:19
L81	1	("5343438").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:19
L82	138	L69 and (time adj interval).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L83	84	L69 and (can).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L86	15643	eDRAM or (embedded adj DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L87	1381	L86 and concurrent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L88	144	L87 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L89	15643	eDRAM or (embedded adj DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L90	1381	L89 and concurrent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L91	144	L90 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2019/02/13 11:19

			EPO; JPO; DERWENT; IBM_TDB			
L92	89184	(column or row) near address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L93	7776	L92 and interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L94	68769	column near address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L95	690	L94 with interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L96	177	L95 with (row near address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L97	81979	column near2 address$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L98	11299	L97 with (multiple or plural$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L99	150	L98 with ((one or single) with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L100	192102	column with (access$3 or address$3)	US-PGPUB; USPAT;	OR	ON	2019/02/13 11:19

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L101	27916	L100 with (multiple or plural$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L102	11340	L101 and (concurrent or simultaneous or ("same" near2 time))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L103	6709	711/157.ccls. 711/167.ccls. 711/168.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L104	198	L102 and L103	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L105	33	("3643236" | "4875196" | "5276642" | "5367494" | "5864505" | "6157560" | "6377492").PN. OR ("6587917").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:19
L106	6709	711/157.ccls. 711/167.ccls. 711/168.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L107	42	L106 and multi$mode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L108	184096	(time near2 multiplex$3) or time$1multiplex$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L109	378	L108 with (memory near2 (bank or array or (sub$1bank or subbank)))	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2019/02/13 11:19

			EPO; JPO; DERWENT; IBM_TDB			
L110	60	L109 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L111	1361	TDM with RAS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L112	288	TDM with CAS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L113	2	L111 and L112	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L114	0	L111 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L115	0	L112 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L116	317717	(memory near2 (bank or array or (sub$1bank or subbank)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L117	180	L116 with (time near3 (overlap$4 or over$1lap$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L118	5	L117 and 711/167-169.ccls.	US-PGPUB; USPAT;	OR	ON	2019/02/13 11:19

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L119	21	(memory near2 conflict) with (multiplex%3 or multi$1plex$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L120	3152	(memory near2 interface) with (MUX or multiplex$3 or multi$1plex$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L121	141	inter$1threading	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L122	11	microthreading and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L123	31	micro$1threading and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L124	666	interleav$3 with SDRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L125	17	L124 and nibble	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L126	5	("6075728").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19

L127	21308	quadrant with (between or center or middle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L128	40	L127 with bank	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L129	3	("20030052885").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L130	4	("6356975").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L131	8	link$1stagger$3 with data with transfer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L132	9	link$1stagger$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L133	37	"6591349"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L134	5	(("6591349") or ("20050015539")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L135	4	("5953252").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2019/02/13 11:19

			DERWENT; IBM_TDB			
L136	42573	kazunari$.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L137	42	L136 and unidirectional	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L138	2511	(bank near2 switch$3) with (tim$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L139	259	L138 same (concurrent$2 or simultaneous$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L140	28	L138 same ((concurrent$2 or simultaneous$2) and sequential$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L141	6	(bank adj switching adj time)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L142	108	quadrant same time same interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L143	0	L142 and tcc	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L144	3	L142 and (bank with tim$3)	US-PGPUB; USPAT; USOCR;	OR	OFF	2019/02/13 11:19

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L145	4	L142 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L146	17	"7290109"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L147	23	("5530828" | "5890192" | "6065092" | "6201735" | "6202138" | "6339817" | "6385688" | "6397314").PN. OR ("7290109").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:19
L148	5	("6065092").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L149	247	("4161040" | "4272832" | "4290120" | "4361869" | "4417302" | "4665483" | "4697112" | "4833648" | "4843264" | "4935868" | "5036231" | "5081575" | "5099452" | "5218690" | "5243703" | "5254883" | "5261064" | "5268639" | "5282174" | "5299156" | "5319755" | "5325053" | "5337285" | "5355391" | "5357195" | "5388237" | "5390308" | "5408129" | "5422529" | "5432823" | "5434818" | "5440523" | "5452436" | "5454082" | "5473575" | "5481496" | "5485490" | "5499385" | "5513327" | "5542067" | "5630163").PN. OR ("6065092").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:19
L150	4	("5995438").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L151	5	("6075728").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L152	1896	ware-fred$.in. or hampel-craig$.in. or richardson-wayne$.in. or bellows-chad$.in. or lai-lawrence$.in.	US-PGPUB; USPAT; USOCR;	OR	OFF	2019/02/13 11:19

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L153	1	L152 and (sequential$2 and bank and row and activate and (concurrent$2 or sequential$2) and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L154	1	L152 and (sequential$2 and bank and row and activate and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L155	5	L152 and (bank and row and activate and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L156	1	("5870347").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:19
L157	192	("4096402" | "4404474" | "4638187" | "4789796" | "4958088" | "4984204" | "5122690" | "5128560" | "5128563" | "5134311" | "5150186" | "5165046" | "5179298" | "5194765" | "5220208" | "5239206" | "5254883" | "5274276" | "5276642" | "5278460" | "5281865" | "5311481" | "5321368" | "5347177" | "5347179" | "5361002" | "5390308" | "5400283" | "5438545" | "5440260" | "5457407" | "5473575" | "5497127" | "5498990" | "5506814" | "5508638" | "5515327" | "5568077" | "5574698" | "5576645" | "5578941" | "5581197" | "5590073" | "5619473" | "5621690" | "5627780" | "5627791" | "5631872" | "5636163" | "5636173" | "5636174" | "5638335" | "5650971" | "5668763" | "5694065").PN. OR ("5870347").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:19
L158	3	(sequential$2 and request and memory and synchronous and row and column and bank and array).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L159	1	("5701270").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:19
L160	69	("4570242" | "4608666" | "5117492" | "5159572" | "5161221" | "5200925" | "5245585" | "5265231" | "5278801" | "5287527" | "5329490" | "5353402" |	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:19

		"5377154" | "5383193" | "5388073" | "5426753" | "5452257" | "5469388" | "5477503" | "5491664").PN. OR ("5701270").URPN.				
L161	34663	(G06F3/0659 or G06F3/0613 or G06F3/0673 or G11C8/06 or G11C7/22 or G11C7/1042 or G11C11/4076 or G11C11/4097 or G11C7/1006).cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:19
L162	4772	(G06F3/0613).CPC.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:19
L163	24	(G06F3/0613).CPC. and (G11C7/1042).CPC.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:19
L164	1	("5343438").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:19
L165	138	L152 and (time adj interval).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L166	84	L152 and (can).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:19
L167	2	(("5313603") or ("5822772")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:19
L170	140	sub$1bank.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:19
L171	15	L170 and (row near2 activat$3) and (column near2 activat$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L172	11	L170 and ((shar$3 or common) with row with decoder)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L173	1733	((shar$3 or common) with row with decoder) and ((shar$3 or common) with column with decoder)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/02/13 11:20

			DERWENT; IBM_TDB			
L174	461	L173 and bank	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L175	186	L173 and bank.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L176	29	("5329488" | "5384743" | "5621690" | "5682350" | "5777922" | "5812452" | "5847994").PN. OR ("6026021").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:20
L177	20	("4630230" | "4635233" | "4731761" | "4845677" | "5150330" | "5297102" | "5327389" | "5369619" | "5463590" | "5568427" | "5604697" | "5712827" | "5831924").PN. OR ("6209056").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:20
L178	15643	eDRAM or (embedded adj DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L179	1381	L178 and concurrent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L180	144	L179 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L181	15643	eDRAM or (embedded adj DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L182	1381	L181 and concurrent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L183	144	L182 and "711".clas.	US-PGPUB;	OR	ON	2019/02/13

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:20
L184	89184	(column or row) near address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L185	7776	L184 and interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L186	68769	column near address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L187	690	L186 with interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L188	177	L187 with (row near address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L189	81979	column near2 address$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L190	11299	L189 with (multiple or plural$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L191	150	L190 with ((one or single) with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2019/02/13 11:20

			IBM_TDB			
L192	192102	column with (access$3 or address$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L193	27916	L192 with (multiple or plural$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L194	11340	L193 and (concurrent or simultaneous or ("same" near2 time))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L195	6709	711/157.ccls. 711/167.ccls. 711/168.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L196	198	L194 and L195	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L197	33	("3643236" | "4875196" | "5276642" | "5367494" | "5864505" | "6157560" | "6377492").PN. OR ("6587917").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:20
L198	6709	711/157.ccls. 711/167.ccls. 711/168.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L199	42	L198 and multi$mode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L200	184096	(time near2 multiplex$3) or time$1multiplex$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20

L201	378	L200 with (memory near2 (bank or array or (sub$1bank or subbank)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L202	60	L201 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L203	1361	TDM with RAS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L204	288	TDM with CAS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L205	2	L203 and L204	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L206	0	L203 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L207	0	L204 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L208	317717	(memory near2 (bank or array or (sub$1bank or subbank)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L209	180	L208 with (time near3 (overlap$4 or over$1lap$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/02/13 11:20

			DERWENT; IBM_TDB			
L210	5	L209 and 711/167-169.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L211	21	(memory near2 conflict) with (multiplex%3 or multi$1plex$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L212	3152	(memory near2 interface) with (MUX or multiplex$3 or multi$1plex$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L213	141	inter$1threading	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L214	11	microthreading and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L215	31	micro$1threading and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L216	666	interleav$3 with SDRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L217	17	L216 and nibble	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L218	5	("6075728").PN.	US-PGPUB; USPAT; USOCR;	OR	OFF	2019/02/13 11:20

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L219	21308	quadrant with (between or center or middle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L220	40	L219 with bank	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L221	3	("20030052885").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L222	4	("6356975").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L223	8	link$1stagger$3 with data with transfer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L224	9	link$1stagger$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L225	37	"6591349"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L226	5	(("6591349") or ("20050015539")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L227	4	("5953252").PN.	US-PGPUB;	OR	OFF	2019/02/13

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:20
L228	42573	kazunari$.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L229	42	L228 and unidirectional	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L230	2511	(bank near2 switch$3) with (tim$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L231	259	L230 same (concurrent$2 or simultaneous$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L232	28	L230 same ((concurrent$2 or simultaneous$2) and sequential$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L233	6	(bank adj switching adj time)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L234	108	quadrant same time same interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L235	0	L234 and tcc	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2019/02/13 11:20

			IBM_TDB			
L236	3	L234 and (bank with tim$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L237	4	L234 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L238	17	"7290109"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L239	23	("5530828" | "5890192" | "6065092" | "6201735" | "6202138" | "6339817" | "6385688" | "6397314").PN. OR ("7290109").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:20
L240	5	("6065092").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L241	247	("4161040" | "4272832" | "4290120" | "4361869" | "4417302" | "4665483" | "4697112" | "4833648" | "4843264" | "4935868" | "5036231" | "5081575" | "5099452" | "5218690" | "5243703" | "5254883" | "5261064" | "5268639" | "5282174" | "5299156" | "5319755" | "5325053" | "5337285" | "5355391" | "5357195" | "5388237" | "5390308" | "5408129" | "5422529" | "5432823" | "5434818" | "5440523" | "5452436" | "5454082" | "5473575" | "5481496" | "5485490" | "5499385" | "5513327" | "5542067" | "5630163").PN. OR ("6065092").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:20
L242	4	("5995438").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L243	5	("6075728").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2019/02/13 11:20

			IBM_TDB			
L244	1896	ware-fred$.in. or hampel-craig$.in. or richardson-wayne$.in. or bellows-chad$.in. or lai-lawrence$.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L245	1	L244 and (sequential$2 and bank and row and activate and (concurrent$2 or sequential$2) and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L246	1	L244 and (sequential$2 and bank and row and activate and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L247	5	L244 and (bank and row and activate and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L248	1	("5870347").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:20
L249	192	("4096402" | "4404474" | "4638187" | "4789796" | "4958088" | "4984204" | "5122690" | "5128560" | "5128563" | "5134311" | "5150186" | "5165046" | "5179298" | "5194765" | "5220208" | "5239206" | "5254883" | "5274276" | "5276642" | "5278460" | "5281865" | "5311481" | "5321368" | "5347177" | "5347179" | "5361002" | "5390308" | "5400283" | "5438545" | "5440260" | "5457407" | "5473575" | "5497127" | "5498990" | "5506814" | "5508638" | "5515327" | "5568077" | "5574698" | "5576645" | "5578941" | "5581197" | "5590073" | "5619473" | "5621690" | "5627780" | "5627791" | "5631872" | "5636163" | "5636173" | "5636174" | "5638335" | "5650971" | "5668763" | "5694065").PN. OR ("5870347").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:20
L250	3	(sequential$2 and request and memory and synchronous and row and column and bank and array).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L251	1	("5701270").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:20

L252	69	("4570242" | "4608666" | "5117492" | "5159572" | "5161221" | "5200925" | "5245585" | "5265231" | "5278801" | "5287527" | "5329490" | "5353402" | "5377154" | "5383193" | "5388073" | "5426753" | "5452257" | "5469388" | "5477503" | "5491664").PN. OR ("5701270").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:20
L253	34663	(G06F3/0659 or G06F3/0613 or G06F3/0673 or G11C8/06 or G11C7/22 or G11C7/1042 or G11C11/4076 or G11C11/4097 or G11C7/1006).cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:20
L254	4772	(G06F3/0613).CPC.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:20
L255	24	(G06F3/0613).CPC. and (G11C7/1042).CPC.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:20
L256	1	("5343438").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:20
L257	138	L244 and (time adj interval).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L258	84	L244 and (can).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L259	15643	eDRAM or (embedded adj DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L260	1381	L259 and concurrent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L261	144	L260 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L262	15643	eDRAM or (embedded adj DRAM)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2019/02/13 11:20

			EPO; JPO; DERWENT; IBM_TDB			
L263	1381	L262 and concurrent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L264	144	L263 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L265	89184	(column or row) near address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L266	7776	L265 and interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L267	68769	column near address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L268	690	L267 with interleav$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L269	177	L268 with (row near address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L270	81979	column near2 address$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L271	11299	L270 with (multiple or plural$3)	US-PGPUB; USPAT;	OR	ON	2019/02/13 11:20

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L272	150	L271 with ((one or single) with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L273	192102	column with (access$3 or address$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L274	27916	L273 with (multiple or plural$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L275	11340	L274 and (concurrent or simultaneous or ("same" near2 time))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L276	6709	711/157.ccls. 711/167.ccls. 711/168.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L277	198	L275 and L276	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L278	33	("3643236" | "4875196" | "5276642" | "5367494" | "5864505" | "6157560" | "6377492").PN. OR ("6587917").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:20
L279	6709	711/157.ccls. 711/167.ccls. 711/168.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L280	42	L279 and multi$mode	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2019/02/13 11:20

			EPO; JPO; DERWENT; IBM_TDB			
L281	184096	(time near2 multiplex$3) or time$1multiplex$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L282	378	L281 with (memory near2 (bank or array or (sub$1bank or subbank)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L283	60	L282 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L284	1361	TDM with RAS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L285	288	TDM with CAS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L286	2	L284 and L285	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L287	0	L284 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L288	0	L285 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L289	317717	(memory near2 (bank or array or (sub$1bank or subbank)))	US-PGPUB; USPAT;	OR	ON	2019/02/13 11:20

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L290	180	L289 with (time near3 (overlap$4 or over$1lap$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L291	5	L290 and 711/167-169.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L292	21	(memory near2 conflict) with (multiplex%3 or multi$1plex$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L293	3152	(memory near2 interface) with (MUX or multiplex$3 or multi$1plex$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L294	141	inter$1threading	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L295	11	microthreading and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L296	31	micro$1threading and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L297	666	interleav$3 with SDRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20

L298	17	L297 and nibble	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:20
L299	5	("6075728").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L300	21308	quadrant with (between or center or middle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L301	40	L300 with bank	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L302	3	("20030052885").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L303	4	("6356975").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L304	8	link$1stagger$3 with data with transfer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L305	9	link$1stagger$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L306	37	"6591349"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2019/02/13 11:20

			DERWENT; IBM_TDB			
L307	5	(("6591349") or ("20050015539")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L308	4	("5953252").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L309	42573	kazunari$.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L310	42	L309 and unidirectional	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L311	2511	(bank near2 switch$3) with (tim$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:20
L312	259	L311 same (concurrent$2 or simultaneous$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:21
L313	28	L311 same ((concurrent$2 or simultaneous$2) and sequential$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:21
L314	6	(bank adj switching adj time)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:21
L315	108	quadrant same time same interleav$3	US-PGPUB; USPAT; USOCR;	OR	OFF	2019/02/13 11:21

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L316	0	L315 and tcc	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:21
L317	3	L315 and (bank with tim$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:21
L318	4	L315 and "711".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:21
L319	17	"7290109"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:21
L320	23	("5530828" | "5890192" | "6065092" | "6201735" | "6202138" | "6339817" | "6385688" | "6397314").PN. OR ("7290109").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:21
L321	5	("6065092").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:21
L322	247	("4161040" | "4272832" | "4290120" | "4361869" | "4417302" | "4665483" | "4697112" | "4833648" | "4843264" | "4935868" | "5036231" | "5081575" | "5099452" | "5218690" | "5243703" | "5254883" | "5261064" | "5268639" | "5282174" | "5299156" | "5319755" | "5325053" | "5337285" | "5355391" | "5357195" | "5388237" | "5390308" | "5408129" | "5422529" | "5432823" | "5434818" | "5440523" | "5452436" | "5454082" | "5473575" | "5481496" | "5485490" | "5499385" | "5513327" | "5542067" | "5630163").PN. OR ("6065092").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:21
L323	4	("5995438").PN.	US-PGPUB; USPAT; USOCR;	OR	OFF	2019/02/13 11:21

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L324	5	("6075728").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:21
L325	1896	ware-fred$.in. or hampel-craig$.in. or richardson-wayne$.in. or bellows-chad$.in. or lai-lawrence$.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:21
L326	1	L325 and (sequential$2 and bank and row and activate and (concurrent$2 or sequential$2) and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:21
L327	1	L325 and (sequential$2 and bank and row and activate and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:21
L328	5	L325 and (bank and row and activate and column and (active or open) and (two or plural)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:21
L329	1	("5870347").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:21
L330	192	("4096402" | "4404474" | "4638187" | "4789796" | "4958088" | "4984204" | "5122690" | "5128560" | "5128563" | "5134311" | "5150186" | "5165046" | "5179298" | "5194765" | "5220208" | "5239206" | "5254883" | "5274276" | "5276642" | "5278460" | "5281865" | "5311481" | "5321368" | "5347177" | "5347179" | "5361002" | "5390308" | "5400283" | "5438545" | "5440260" | "5457407" | "5473575" | "5497127" | "5498990" | "5506814" | "5508638" | "5515327" | "5568077" | "5574698" | "5576645" | "5578941" | "5581197" | "5590073" | "5619473" | "5621690" | "5627780" | "5627791" | "5631872" | "5636163" | "5636173" | "5636174" | "5638335" | "5650971" | "5668763" | "5694065").PN. OR ("5870347").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:21

L331	3	(sequential$2 and request and memory and synchronous and row and column and bank and array).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:21
L332	1	("5701270").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:21
L333	69	("4570242" | "4608666" | "5117492" | "5159572" | "5161221" | "5200925" | "5245585" | "5265231" | "5278801" | "5287527" | "5329490" | "5353402" | "5377154" | "5383193" | "5388073" | "5426753" | "5452257" | "5469388" | "5477503" | "5491664").PN. OR ("5701270").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:21
L334	34663	(G06F3/0659 or G06F3/0613 or G06F3/0673 or G11C8/06 or G11C7/22 or G11C7/1042 or G11C11/4076 or G11C11/4097 or G11C7/1006).cpc.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:21
L335	4772	(G06F3/0613).CPC.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:21
L336	24	(G06F3/0613).CPC. and (G11C7/1042).CPC.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:21
L337	1	("5343438").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:21
L338	138	L325 and (time adj interval).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:21
L339	84	L325 and (can).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/02/13 11:21
L340	2	(("5313603") or ("5822772")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/13 11:21
L341	140	sub$1bank.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:21
L342	15	L341 and (row near2 activat$3) and (column near2 activat$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/02/13 11:21

			DERWENT; IBM_TDB			
L343	11	L341 and ((shar$3 or common) with row with decoder)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:21
L344	1733	((shar$3 or common) with row with decoder) and ((shar$3 or common) with column with decoder)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:21
L345	461	L344 and bank	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:21
L346	186	L344 and bank.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/13 11:21
L347	29	("5329488" | "5384743" | "5621690" | "5682350" | "5777922" | "5812452" | "5847994").PN. OR ("6026021").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:21
L348	20	("4630230" | "4635233" | "4731761" | "4845677" | "5150330" | "5297102" | "5327389" | "5369619" | "5463590" | "5568427" | "5604697" | "5712827" | "5831924").PN. OR ("6209056").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2019/02/13 11:21

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L84	3	(sequential$2 and request and memory and synchronous and row and column and bank and array).clm.	USPAT	OR	ON	2019/02/13 11:19
L85	1	(memory and controller and read and clock and cycle and minimum and bank and array and activation).clm.	USPAT	OR	ON	2019/02/13 11:19
L168	3	(sequential$2 and request and memory and synchronous and row and column and bank and array).clm.	USPAT	OR	ON	2019/02/13 11:19
L169	1	(memory and controller and read and clock and cycle and minimum and bank and array and activation).clm.	USPAT	OR	ON	2019/02/13 11:19
L349	3	(sequential$2 and request and memory and synchronous and row and column and bank and array).clm.	USPAT	OR	ON	2019/02/13 11:21
L350	1	(memory and controller and read and clock	USPAT	OR	ON	2019/02/13

		and cycle and minimum and bank and array and activation).clm.				11:21
L351	3	(sequential$2 and request and memory and synchronous and row and column and bank and array).clm.	USPAT	OR	ON	2019/02/13 11:21
L352	1	(memory and controller and read and clock and cycle and minimum and bank and array and activation).clm.	USPAT	OR	ON	2019/02/13 11:21

2/13/2019 2:25:03 PM
C:\Users\gcygiel\Documents\Work\Patents\15xxxxxx\15486068\15486068.wsp

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/486068	04/12/2017	Frederick A. Ware	2016091 / RA378C3C1C1	2908

TITLE OF INVENTION:

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	1000	0	0	1000	5/20/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Rambus Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Sunnyvale, California (USA)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ■ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☑ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Marc P. Schuyler/ Date 07 May 2019

Typed or printed name Marc P. Schuyler, Reg. No. 35675 Registration No. 35675

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Silicon Motion Inc. Ex. 1002, Page 320
Silicon Motion Inc. v. K.Mizra LLC, IPR2024-01236

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	15486068
Filing Date:	12-Apr-2017
Title of Invention:	Memory Controller For Micro-Threaded Memory Operations
First Named Inventor/Applicant Name:	Frederick A. Ware
Filer:	Marc Philip Schuyler
Attorney Docket Number:	2016091 / RA378C3C1C1US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1000**

Electronic Acknowledgement Receipt

EFS ID:	35942558
Application Number:	15486068
International Application Number:	
Confirmation Number:	2908
Title of Invention:	Memory Controller For Micro-Threaded Memory Operations
First Named Inventor/Applicant Name:	Frederick A. Ware
Customer Number:	78408
Filer:	Marc Philip Schuyler
Filer Authorized By:	
Attorney Docket Number:	2016091 / RA378C3C1C1US
Receipt Date:	07-MAY-2019
Filing Date:	12-APR-2017
Time Stamp:	16:05:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	050819INTEFSW16065000
Deposit Account	
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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	000-ptol85b.pdf	72581 2c4b283e20552bab1f6084301fb2b8b72c4a27b7	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30241 02376528c523cb3fb11089120fb26a2bb61b6ae5	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	102822		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/486,068	06/25/2019	10331379	2016091 / RA378C3C1C1US	2908

78408 7590 06/05/2019

MARC P. SCHUYLER / Rambus
P.O. BOX 2535
SARATOGA, CA 95070

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Frederick A. Ware, Los Altos Hills, CA;
Rambus Inc., Sunnyvale, CA;
Craig E. Hampel, Los Altos, CA;
Wayne S. Richardson, Saratoga, CA;
Chad A. Bellows, Birmingham, MI;
Lawrence Lai, San Jose, CA;

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