UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SILICON MOTION INC.,

Petitioner

v.

K.MIZRA LLC,

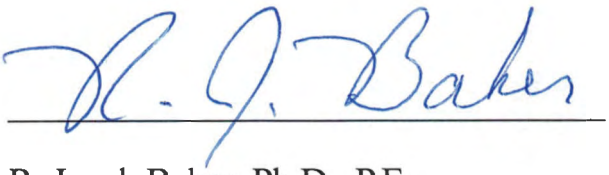
Patent Owner

U.S. PATENT NO. 10,331,379

DECLARATION OF R. JACOB BAKER, PH.D., P.E. IN SUPPORT OF SILICON MOTION'S PETITION FOR *INTER PARTES* REVIEW OF CLAIMS 1-22 OF U.S. PATENT NO. 10,331,379

Declaration of Dr. Baker

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the results of the proceedings.



Date: September 9, 2024

Las Vegas, NV

R. Jacob Baker, Ph.D., P.E.

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I, R. Jacob Baker, Ph.D., P.E., declare as follows:

1. I have been retained on behalf of Silicon Motion Inc. ("Petitioner") to provide expert opinions in connection with the *Inter Partes* Review ("IPR") of U.S. Patent 10,331,379 ("the '379 Patent").

2. I am being compensated for my time in connection with this IPR at my standard consulting rate for consulting services. My compensation is not affected by the outcome of this matter.

3. I have been asked to provide my opinions regarding whether Claims 1-22 of the '379 Patent (the "Challenged Claims") are invalid as anticipated by prior art or obvious to a person of ordinary skill in the art at the time of the alleged invention ("POSITA").

4. In preparing this declaration, I have reviewed the following materials. To the extent any materials are not listed below but are cited in this declaration, I have also reviewed those materials as well.

Exhibit No.	Description
1001	U.S. Patent No. 10,331,379
1002	File History of U.S. Patent No. 10,331,379
1004	U.S. Patent 6,185,149 ("Fujioka")
1005	U.S. Patent 6,209,056 ("Suh")
1006	U.S. Patent Application Publication 2005/0177690 ("LaBerge")
1007	European Patent Application Publication 0339224 ("Bowater")
1008	U.S. Patent No. 6,742,098 ("Halbert")

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Exhibit No.	Description
1009	U.S. Patent Application Publication 2003/0126485 ("Wilcox")
1010	U.S. Patent Application Publication 2004/0148482 ("Grundy")
1011	U.S. Patent 6,681,301 ("Mehta")
1012	U.S. Patent 5,822,772 ("Chan")
1013	U.S. Patent Application Publication 2002/0089879 ("Kobayashi")
1014	U.S. Patent 5,184,320 ("Dye")
1015	U.S. Patent 5,235,550 ("Zagar")
1016	U.S. Patent 4,707,809 ("Ando")

5. In forming the opinions expressed in this declaration, I relied upon my knowledge, skill, experience, training, and education in the relevant field of the art, and have considered the viewpoint of a POSITA as of November 29, 2004. My opinions are based on the following references in view of the knowledge of POSITA during this time.

I. Background Qualifications

6. My qualifications generally are set forth in my Curriculum Vitae, which is attached as **Appendix A**. Appendix A also includes a list of the publications I have authored and a list of the other cases in which I have testified during the last four years.

7. I have been working as an Engineer since 1985 and I have been teaching Electrical and Computer Engineering courses since 1991. I am currently a professor

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emeritus of electrical and computer engineering at the University of Nevada, Las Vegas ("UNLV").

8. I received B.S. and M.S. degrees in Electrical Engineering from UNLV in 1986 and 1988, respectively. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno, in 1993.

9. My doctoral research, culminating in the award of a Ph.D., investigated the use of power MOSFETs in the design of very high peak power, and high-speed, instrumentation. I developed techniques to reliably stack power MOSFETs to switch higher voltages, that is, greater than 1,000 V and 100 Amps of current with nanosecond switching times. This work was reported in the paper entitled "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices," published in the IEEE Transactions on Power Electronics. The paper received the Best Paper Award in 2000.

Industry Experience

10. I have done technical and expert witness consulting for over 200 companies and their subsidiaries since I started working as an engineer in 1985. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapon tests at the Nevada test site. During this time, I designed, and oversaw the fabrication of, over 30 electronic and electro-optic instruments,

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including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera sweep circuits, Pockel's cell drivers, micro-channel plate gating circuits, charging circuits for battery backup of equipment for recording test data, and analog oscilloscope electronics.

11. My work during this time, as one example, had a direct impact on my doctoral research work using power MOSFETs, subsequent publishing efforts, and industry designs. In addition to the 2000 Best Paper Award from the IEEE Power Electronics Society, I published several other papers in related areas while working in industry. I hold a patent, Patent No. 5,874,830, in the area of power supply design, titled, "Adaptively biased voltage regulator and operating method," which was issued on February 23, 1999. I have designed dozens of linear and switching power supplies for commercial products and scientific instrumentation.

12. I am a licensed Professional Engineer and have extensive industry experience in circuit design, fabrication, and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, Phase-Change Random Access Memory (PCRAM) chips, and CMOS Image Sensors (CISs) at Micron Technology, Inc. ("MTI") in Boise, Idaho. I spent considerable time working on the development of flash memory chips while at MTI. My efforts resulted in more than a dozen patents relating to flash memory. One of my projects at MTI included the development, design, and testing of circuit design techniques for a multi-level cell (MLC) flash

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memory using signal processing. This effort resulted in higher-density memories for use in solid-state drives and flash memory cards having an ATA interface that are ubiquitous in consumer electronics, including cameras and data storage systems. Further, the use of higher-density memory can result in fewer changes in the flash translation layer for logical-to-physical addressing, less need for garbage collection, and larger data segments that can improve a computing system's performance. Another project I worked on at MTI focused on the design of buffers for high-speed double-data rate DRAM, which resulted in around 10 U.S. patents in buffer design. Among many other experiences, I led the development of the delay locked loop (DLL) in the late 1990s so that MTI DRAM products could transition to the DDR memory protocol, used in mobile and non-mobile (server, desktop, cell phones, tablets, etc.) computing systems as main computer memory, for addressing and controlling accesses to memory via interprocess communications (IPC) with the memory controller (MC). I provided technical assistance with MTI's acquisition of Photobit during 2001 and 2002, including transitioning the manufacture of CIS products into MTI's process technology. Further, I did consulting work at Sun Microsystems and then Oracle on the design of memory modules during 2009 and 2010. This work entailed the design of low-power, high-speed, and wide interconnection methods with the goal of transmitting data to/from the memory module and the MC at higher speeds.

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13. I have extensive experience in the development of instrumentation and commercial products in a multitude of areas including: integrated electrical/biological circuits and systems, array (memory, imagers, and displays) circuit design, CMOS analog and digital circuit design, diagnostic electrical and electro-optic instrumentation for scientific research, CAD tool development and online tutorials, low-power interconnect and packaging techniques, design of communication/interface circuits (to meet commercial standards such as USB, firewire, DDR, PCIe, SPI, etc.), circuit design for the use and storage of renewable energy, and power electronics. For example, a part of my research at Boise State, for many years, focused on the use of Thru-Silicon-Vias (TSVs), aka Thru-Wafer Vias (TWVs), for high-density 3D packaging. These packaging techniques were utilized in the memory module development work I did with Sun Microsystems and Oracle. As another example, I designed circuitry for use in implementing Universal Serial Bus (USB) interface circuits while I did consulting at Tower Semiconductor. I designed PCI communication circuits for IPC between a Graphics Processor Unit (GPU) and memory while consulting for Rendition, Inc. From 1994 to 1996, I worked on the design of displays at Micron Display and Micron Technology, Inc. ("Micron") in Boise, Idaho. This work was at a time when cathode ray tubes (CRTs) were still the dominant type of display. Flat panel displays were being developed with the hope of replacing CRTs in the consumer market. I worked on flat panel

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displays which resulted in 5 patents: 5,598,156, 5,638,085, 5,818,365, 5,894,293, and 5,909,201. I worked on the design of the pixels, both active and passive, as well as the supporting electronics for processing video signals. I was involved with the evaluation of display technologies including liquid crystal displays (LCDs), light-emitting diodes, plasma displays, and organic light emitting diode (OLED) displays; the display technologies that were looking to displace CRTs in the consumer market. I was also involved with the packaging of the displays including the vacuum sealing and deposition of the phosphors for light wavelength conversion. I also taught display design as a topic in my courses and did display design consulting again in industry for Cirque in 2013.

14. My current research work is focused in part on the design of integrated circuits for wireless sensing using LIDAR (LIght Detection And Ranging). I have worked with several companies in the development of these circuits and systems including Freedom Photonics, Aerius Photonics, and FLIR. In the early 1990s, I worked on wireless systems for wideband impulse radar while at Lawrence Livermore Laboratory. Further, part of my research for several years focused on the digitization of IQ channels using delta-sigma modulation. The knowledge and experience gained from this effort are reflected in my textbook CMOS Mixed-Signal Circuit Design and a presentation, which I have presented at several universities and companies, http://cmosedu.com/jbaker/papers/talks/BP_DSM_talk.pdf.

Academic Experience

15. I was an adjunct faculty member in the Electrical Engineering departments of UNLV and UNR from 1991-1993. From 1993 to 2000, I served on the faculty at the University of Idaho as an Assistant Professor and then as a tenured Associate Professor of Electrical Engineering. In 2000, I joined a new Electrical and Computer Engineering program at Boise State University ("BSU"), where I served as department chair from 2004 to 2007. At BSU, I helped establish graduate programs in Electrical and Computer Engineering including, in 2006, the university's second Ph.D. degree. In 2012, I re-joined the faculty at UNLV. Over the course of my career as a professor, I have advised more than 100 masters and doctoral students.

16. I have been recognized for my contributions as an educator in the field. While at Boise State University, I received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001). In 2007, I received the Frederick Emmons Terman Award (the "Father of Silicon Valley"). The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession. In 2011, I received the IEEE Circuits and Systems Education Award. I received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor Award every year it was awarded while I was actively involved in teaching at UNLV.

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17. I have authored several books and papers in the electrical and computer engineering area. My published books include CMOS Circuit Design, Layout, and Simulation (Baker, R.J., Wiley-IEEE, ISBN: 9781119481515 (4th ed., 2019)) and CMOS Mixed-Signal Circuit Design (Baker, R.J., Wiley-IEEE, ISBN: 9780470290262 (2nd ed., 2009) and ISBN: 9780471227540 (1st ed., 2002)). I co-authored DRAM Circuit Design: Fundamental and High-Speed Topics (Keeth, B., Baker, R.J., Johnson, B., and Lin, F., Wiley-IEEE, ISBN: 9780470184752 (2008)), DRAM Circuit Design: A Tutorial (Keeth, B. and Baker, R.J., Wiley-IEEE, ISBN: 0-7803-6014-1 (2001)), and CMOS Circuit Design, Layout and Simulation (Baker, R.J., Li, H.W., and Boyce, D.E., Wiley - IEEE, ISBN: 9780780334168 (1998)). I contributed as an editor and co-author on several other electrical and computer engineering books.

Other Relevant Experience

18. I have given more than 50 invited talks at conferences, companies, and universities. Further, I am the author or co-author of more than 100 papers and presentations in the areas of electrical and computer engineering design, fabrication, and packaging.

19. I have served as a volunteer on the IEEE Press Editorial Board (1999-2004); as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018); as the Technical Program Chair of the 2015 IEEE 58th International Midwest

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Symposium on Circuits and Systems (MWSCAS 2015); on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016); as a Distinguished Lecturer for the SSCS (2012-2015); the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for IEEE Solid-State Circuits Magazine; IEEE Kirchhoff Award Committee (2020-2023); and advisor for the student branch of the IEEE at UNLV (2013-2024). These meetings, groups, and publications are intended to allow researchers to share and coordinate research. My active participation in these meetings, groups, and publications allowed me to see what other researchers in the field have been doing. In addition to the above, I am an IEEE Fellow for contributions to semiconductor memory design and a member of the honor societies Eta Kappa Nu and Tau Beta Pi.

II. Understanding of Patent Law

20. I am not an attorney, though I have been provided with an understanding of patent law sufficient to conduct the analysis given in this report. The following represents my understanding of these issues.

21. A patent or published patent application having a priority date or filing date before November 29, 2004, or a printed publication that was first published before November 29, 2004, is prior art against the ’379 patent.

22. A claim is invalid or unpatentable if that claim is either anticipated or obvious. In order to show anticipation of a claim, every element of a claim must be disclosed

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expressly or inherently in a single prior art reference. In order to show obviousness of a claim, the claim must be obvious from the perspective of a POSITA at the time the alleged invention was made. A claim may be obvious in view of a single reference or may be obvious from a combination of two or more prior art references.

23. An obviousness analysis requires an understanding of the scope and content of the prior art, any differences between the alleged invention and the prior art, and the level of ordinary skill in evaluating the pertinent art. In addition, certain factors may support or rebut the obviousness of a claim, such as secondary considerations. Secondary considerations can include things such as commercial success of the alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. Contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

24. A claim is invalid or unpatentable because it would have been obvious when it combines old elements with no change to a respective function, or alters prior art by mere substitution of one element for another known in the field, and that combination

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yields predictable results. Moreover, to facilitate a combination of prior art references, a reason to combine the prior art is helpful. However, common sense can be used as a guide; there is no rigid requirement to find an express teaching, suggestion, or motivation to combine. When a product is available, design incentives and other market forces can prompt variations of it, either in the same field or different one. If a person having ordinary skill in the relevant art can implement a predictable variation, a finding of obviousness would likely prohibit patentability of such variations. For the same reason, if a technique has been used to improve one device and a person having ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious. A claim may be obvious if common sense directs one to combine multiple prior art references or add missing features to reproduce the alleged invention recited in the claims.

III. Level of Ordinary Skill in the Pertinent Art

25. A POSITA for the ’379 Patent would have had a Bachelor’s degree in electrical or computer engineering or a related field, and two or more years of experience in computer memory design or equivalent work experience. Additional education might compensate for less experience, and vice-versa.

IV. Overview of the ’379 Patent

26. The ’379 patent is generally directed to a memory system. EX1001, 1:28-29. In part, claim 1 of the patent recites a “memory controller” comprising “circuitry to

schedule issuance" of "row activation commands" and "column access commands" such that certain "first," "second," and "third" intervals are present. *Id.*, claim 1. However, in my opinion, these aspects of claim 1, as well as the other recited aspects (and the other challenged claims), were well-known in the prior art before November 29, 2004. In my opinion, the grounds of the petition disclose or at least render obvious the challenged claims.

V. Claim Interpretation

27. I understand that claims terms are typically given their ordinary and customary meaning, as would have been understood by a POSITA, during the relevant time frame, which I was asked to assume was prior to November 29, 2004. In considering the meaning of the claims, I also understand that one must consider the claim language, specification, prosecution history, and the knowledge of a POSITA at the relevant time. I have followed these principles in my analysis. I believe all terms in the challenged claims should be given their ordinary and customary meaning, as would have been understood by a POSITA at the time of the purported invention.

28. I understand that certain terms in the Challenged Claims may be considered "means-plus-function" terms. If the following are treated as means-plus-function terms, I have identified their function and, as best understood, their corresponding structure below.

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A. "circuitry" terms (claims 1, 4, 5, 7, 12, 15, 16, 18)

29. I understand that Claims 1 and 12 recite (1) *circuitry to provide a clock signal* and (2) *circuitry* that is *to schedule issuance of the row activation commands and the column access commands*. Claims 4 and 15 recite that *circuitry to schedule is to schedule at least one column access command for each row activation command.* Claims 5 and 16 recite that *circuitry to schedule is to schedule for a given row activation command, at least two column access commands*. Claims 7 and 18 recite *serialization/deserialization circuitry to exchange serialized data with the memory device*.

30. If a means-plus-function interpretation applies, the respective functions are (1) *to provide a clock signal to the memory device*, (2) *to schedule issuance of the row activation commands and the column access commands from the command interface*, (3) *schedule at least one column access command for each row activation command*, (4) *schedule for a given row activation command, at least two column access commands*, and (5) *to exchange serialized data with the memory device*. As best understood, the structures for each is memory controller hardware and equivalents thereof. EX1001, 30:54-34:28, 31:41-32:9, Figs. 28, 29.

B. "interface" terms (claims 1, 4, 6-8, 12, 15, 17-19)

31. I understand that claims 1 and 12 recite (1) *a command interface to transmit* [] *row activation commands* [] *and column access commands*. Claims 4 and 15 recite

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(2) *the command interface is to transmit bank address information*. Claims 6, 7, 12, 17, and 18 recite (3) *a data interface to exchange data.* Claims 8 and 19 recite (4) *a data interface to exchange each of data, and write mask values*.

32. If a means-plus-function interpretation applies, the respective functions are (1) *to transmit* [] *row activation commands* [] *and column access commands ,* (2) *to transmit bank address information*, (3) *to exchange data*, and (4) *to exchange each of data, and write mask values with the memory device*. As best understood, the structures for each is memory controller hardware and equivalents thereof. EX1001, 30:54-34:28, 31:41-32:9, Fig. 29.

C. "logic" term (claim 11)

33. I understand that claim 11 recites *logic to time-multiplex commands from the command queues…* and *to interleave commands from the command queues*. If a means-plus-function interpretation applies, the function is *to time-multiplex commands from the command queues…* and *to interleave commands from the command queues*. As best understood, the structure is memory controller hardware and equivalents thereof. EX1001, 30:54-34:28, 31:41-32:9, Fig. 29.

VI. Overview of Challenge

A. Prior Art Printed Publications

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34. I understand the '379 Patent claims priority to November 29, 2004.[1] I understand Petitioner's challenge is based on the following prior art references:

U.S. Patent (USP)/U.S. Patent App. Pub. (USPAP)/European Patent Application (EP)	**Filing Date**	**Pub. Date**	**Prior Art Status**
USP 6,185,149 ("Fujioka") (EX1004)	June 28, 1999	February 6, 2001	§§102(a), (b), (e)
USP 6,209,056 ("Suh") (EX1005)	June 30, 1997	March 27, 2001	§§102(a), (b), (e)
USPAP 2005/0177690 ("LaBerge") (EX1006)	February 5, 2004	August 11, 2005	§102(e)
EP 0339224 ("Bowater") (EX1007)		November 2, 1989	§§102(a), (b)
USP 6,742,098 ("Halbert") (EX1008)	October 3, 2000	May 25, 2004	§§102(a), (e)
USPAP 2003/0126485 ("Wilcox") (EX1009)	January 2, 2002	July 3, 2003	§§102(a), (b), (e)

[1] I do not agree that the '379 patent is necessarily entitled to this priority date.

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USPAP 2004/0148482 ("Grundy") (EX1010)	January 13, 2004	July 29, 2004	§§102(a), (e)
USP 6,681,301 ("Mehta") (EX1011)	October 2, 2001	January 20, 2004	§§102(a), (e)
USP 5,822,772 ("Chan") (EX1012)	March 22, 1996	October 13, 1998	§§102(a), (b), (e)
USPAP 2002/0089879 ("Kobayashi") (EX1013)	July 25, 2001	July 11, 2002	§§102(a), (b), (e)

B. LaBerge

35. LaBerge is generally directed to a memory controller system. EX1006, Abstract. For example, LaBerge describes a memory controller 200 that is coupled to memory devices 80 and 86 of modules 310a-n, where memory controller 200 transmits command and address signals to the devices via memory bus 320. *Id.*, ¶0039, Fig. 6. Such command signals include "DRAM command signals" including RAS and CAS commands. *Id.*, ¶0034.

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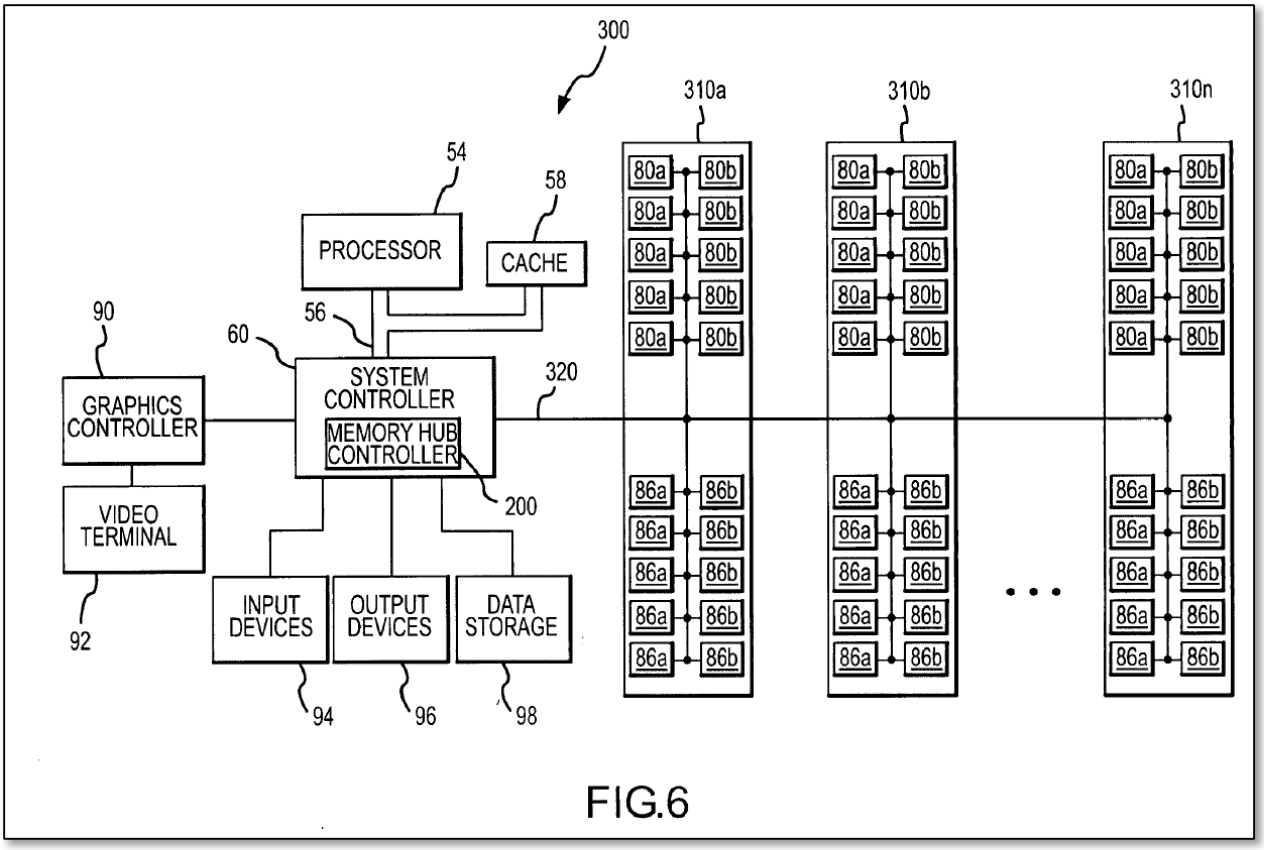
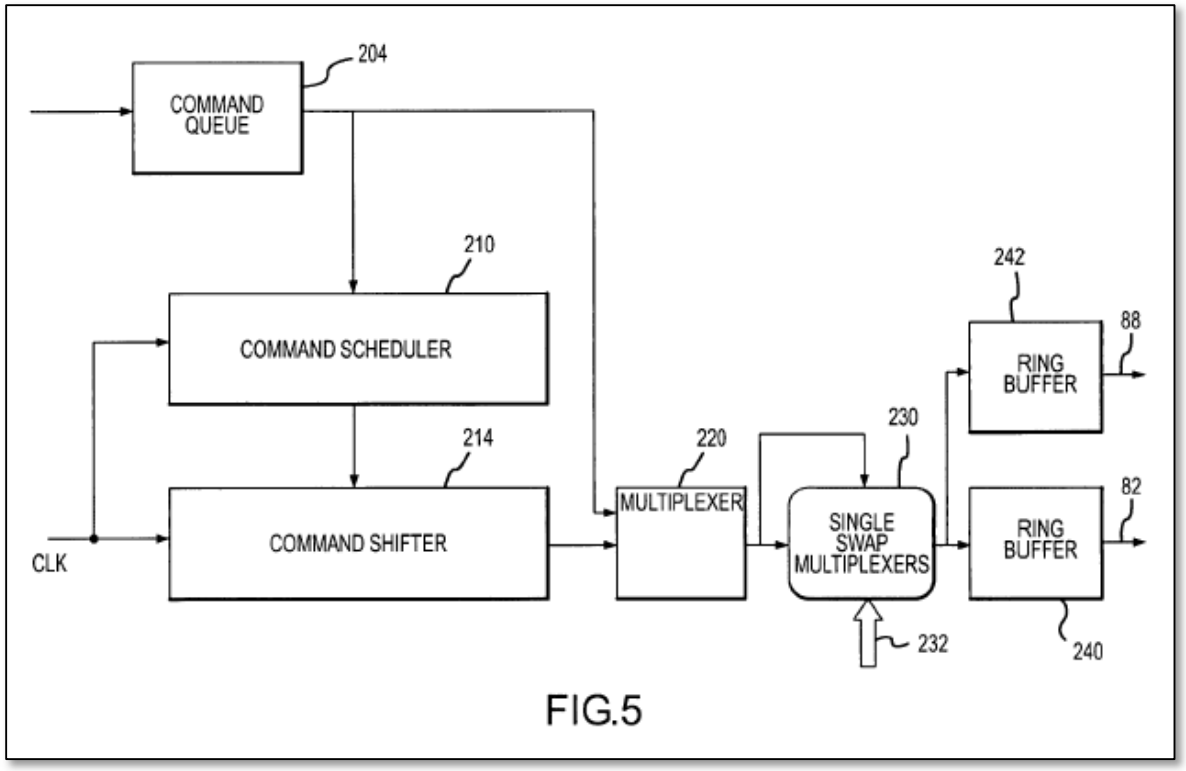


FIG.6

EX1006, Fig. 6

36. Figure 5 shows an example embodiment of memory controller 200. For example, memory controller 200 includes a command queue 204 that "places the command signals in a queue" and "outputs the commands in the proper order." EX1006, ¶0034. Memory controller 200 further includes a command scheduler 210. *Id.*, ¶0035 For example, command schedular "spaces the command and address signals apart from each other with the proper delay" and may, for example, schedule "CASZ to be output three clock periods after the RASZ" signal. *Id.*



EX1006, Fig. 5

C. Bowater

37. Bowater is generally directed to a dynamic memory controller that adjusts how memory banks are accessed. EX1007, Abstract. For example, Bowater's system includes a memory controller 110 that accesses memory banks 120-123. *Id.*, 4:40-43, Figs. 3, 4.

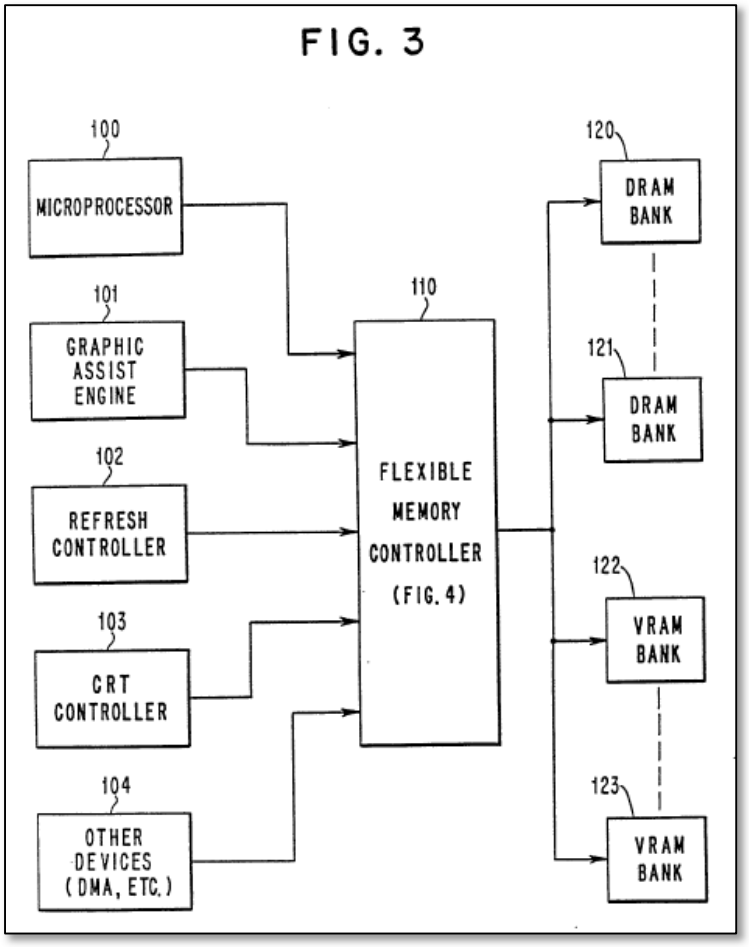
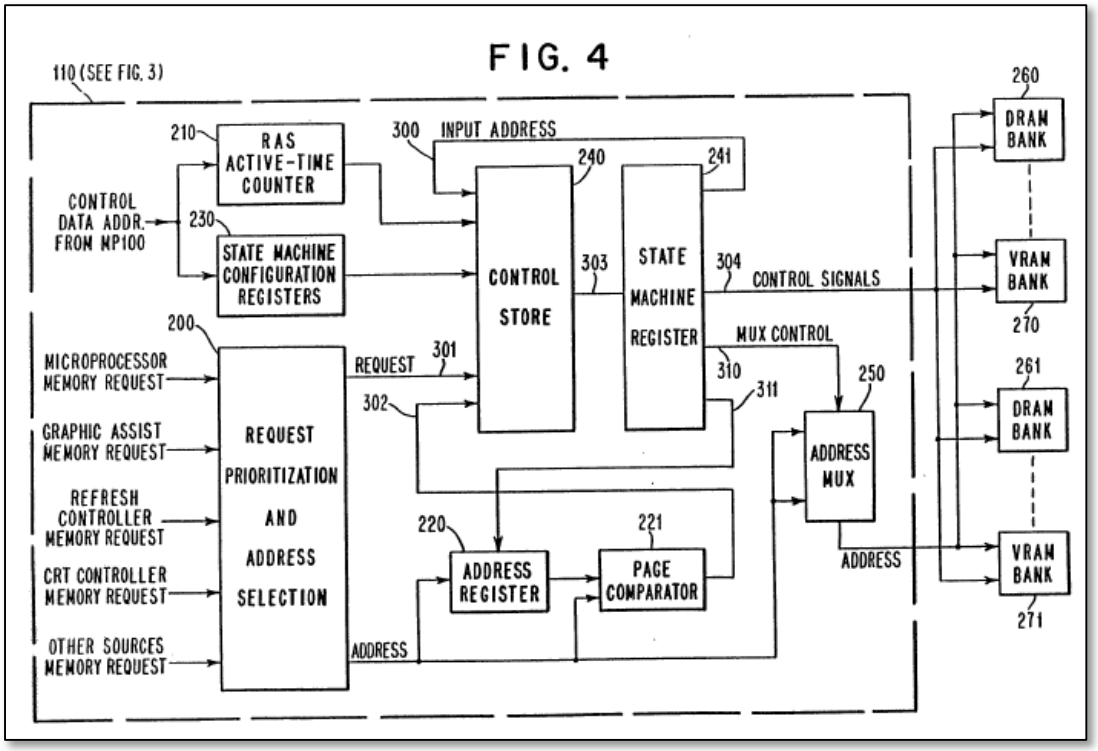


FIG. 3
100
MICROPROCESSOR
101
GRAPHIC ASSIST ENGINE
102
REFRESH CONTROLLER
103
CRT CONTROLLER
104
OTHER DEVICES (DMA, ETC.)
110
FLEXIBLE MEMORY CONTROLLER (FIG. 4)
120
DRAM BANK
121
DRAM BANK
122
VRAM BANK
123
VRAM BANK

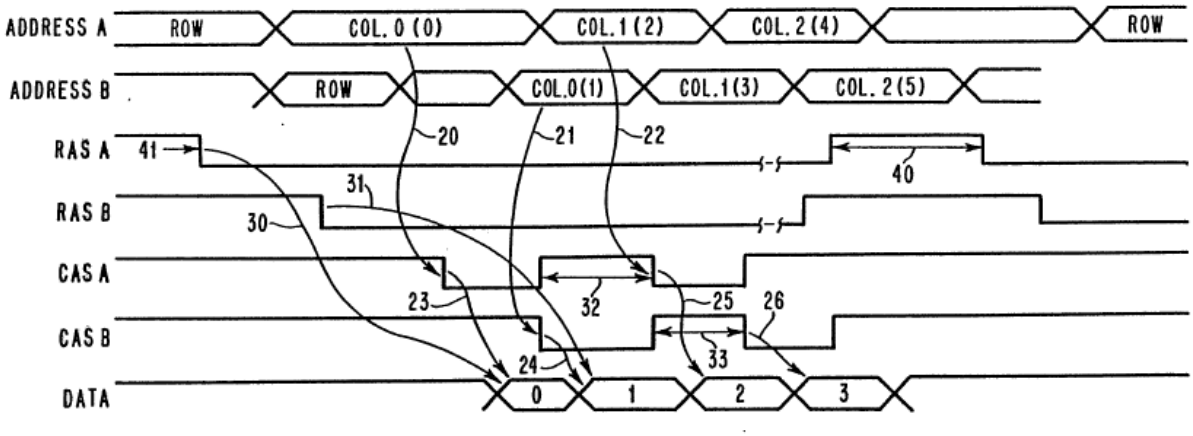
EX1007, Fig. 3



EX1007, Fig. 4

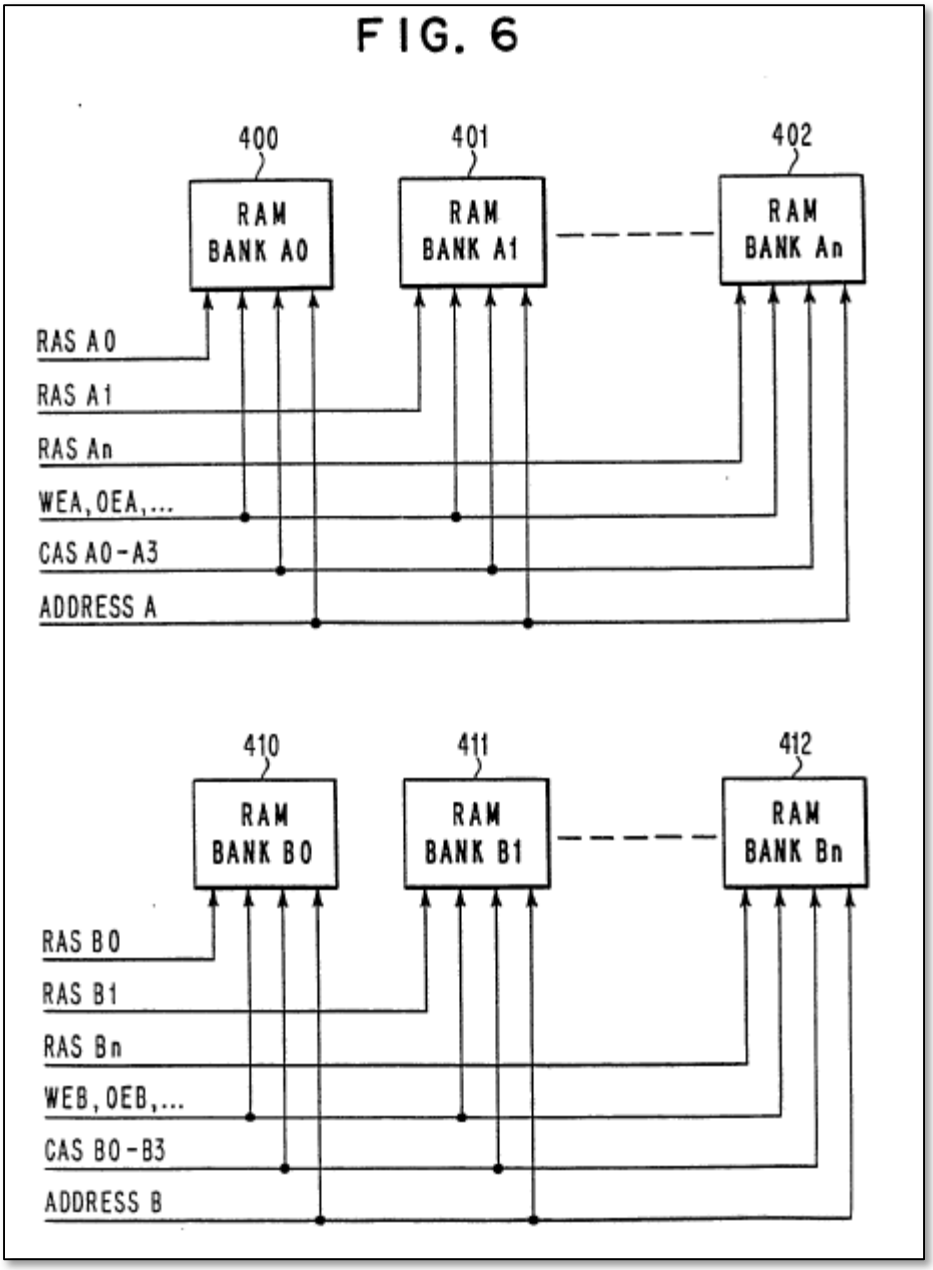
38. The memory controller generates control signals such as RAS and CAS signals and modifies the timing of these signals. EX1007, 4:19-40, Fig. 2. For example, Bowater's system provides for "dynamic delays" that are "determined by the memory controller in accordance with the type of memory being accessed at a given time, and the source of the request." *Id.*, 3:9-18. Indeed, Figure 2 provides an example of the timing of such control signals.

FIG. 2



EX1007, Fig. 2

39. Bowater teaches that memory banks can be accessed to allow DRAM interleaving. Such an example is shown in Figure 6, where RAS and CAS commands are sent to banks A0-An and B0-Bn of memory. EX1007, 7:1-13, Fig. 6.



EX1007, Fig. 6

D. Suh

40. Suh is generally directed to a memory having a "plurality of memory cell arrays with a plurality of bank sections." EX1005, Abstract.

41. Suh describes that each of bank 0, bank 1, bank 2, and bank 3 includes eight respective bank sections, each labeled as "bank 0," "bank 1," "bank 2," and "bank 3," distributed in the cell arrays of Figure 2. EX1005, 3:20-38, Fig. 2. Suh further describes "a column decoder is connected to each of the cell arrays, and a row decoder is positioned between the two cell arrays in each of the cell array blocks and connected in common to them." *Id.*, 3:28-31, Fig. 2.

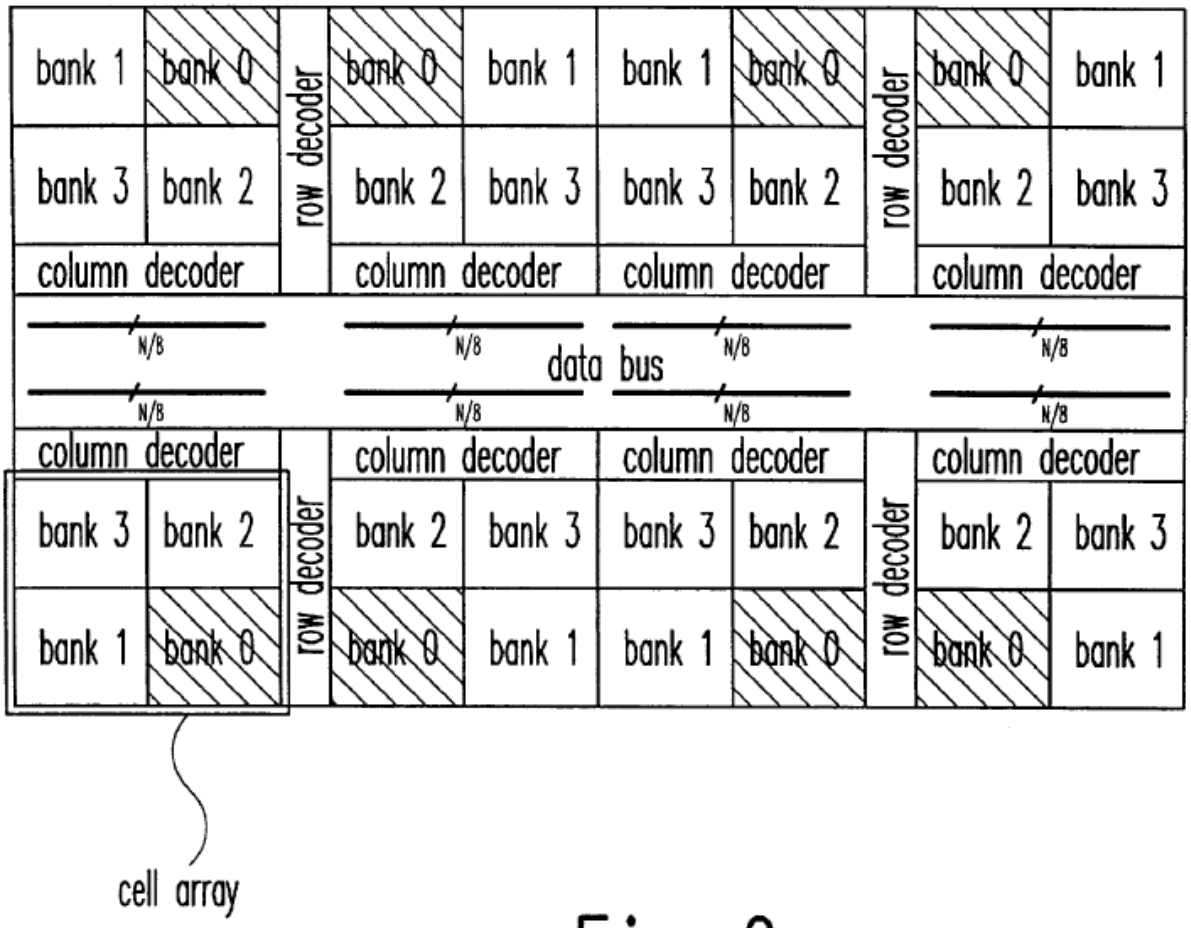


Fig. 2

EX1005, Fig. 2

E. Halbert

42. Halbert is generally directed to a memory system that accesses rows and columns of memory. EX1008, Abstract. For example, Halbert describes "two consecutive read operations (to the same ROW of the memory devices)," where a controller "latches an active command in RCMD," commanding a row activation, and a "READ command (to COL a) is clocked in, causing the controller to enter a read state," and "a second READ command (to COL b) is clocked in," providing two commands to access columns a and b, which are different columns within the same row of memory that has been activated by the active command. *Id.*, 5:58-6:6; *id.*, 2:36-50, Fig. 3 (a READ from "columns [] on the same ROW").

F. Grundy

43. Grundy is generally directed to a memory controller system. EX1010, Abstract. For example, Grundy describes a "memory controller 151" coupled to a collective memory device formed by memory devices 155sub1 through 155sub8, where the memory controller has inputs and outputs connecting it to memory devices 155sub1 and 155sub8 via "N multi-purpose lines 158" of "point-to-point signaling links 153" that allow for the sending and receiving of "N-bit wide data values" to and from the collective memory device, with one subset of links 153 used to send data values to memory device 155sub1 of the collective device and another subset

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of links 153 used to receive data values from memory device 155sub8 of the collective device, as shown in Figure 5A. EX1010, ¶¶0036, 0043-0044, Figs. 3, 5A.

44. Grundy further describes that memory controller 151 has a "serializer circuit" at its output "to serialize an N-bit transmission," thereby serializing data that is sent via the "N multi-purpose lines 158" of each of links 153 to the memory device formed devices 155sub1 through 155sub8, and has a "deserializer circuit" to "deserialize the N-bit transmission," thereby de-serializing data that is received via the "N multi-purpose lines 158" of each of the links 153 from the memory device formed by devices 155sub1 through 155sub8. EX1010, ¶¶0043-0044, 0051-0052, Fig. 5A.

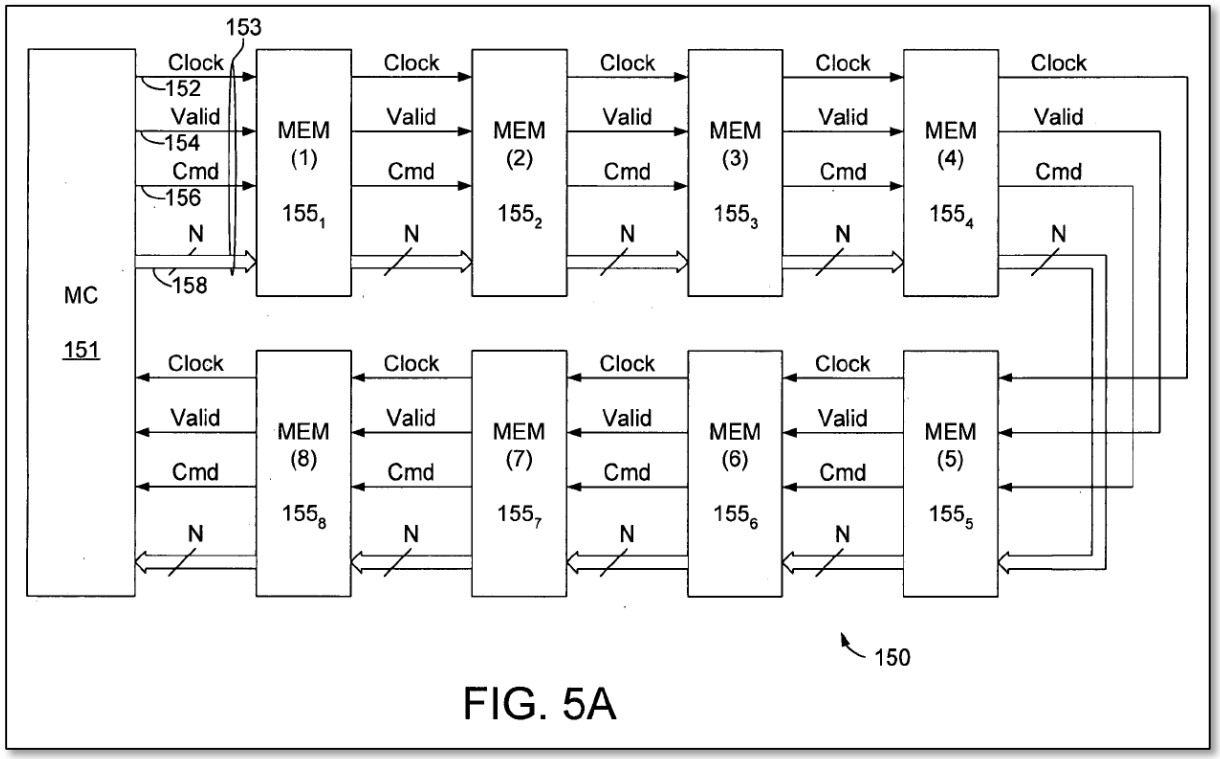

FIG. 5A

EX1010, Fig. 5A

G. Mehta

45. Mehta is generally directed to a memory controller system that controls data transfers with memory. EX1011, Abstract. For example, Mehta's "memory controller 210" includes "hybrid data read/write circuit 220" coupling the controller to memory 170 and 180, where circuit 220 includes "DIMM interface modules" 310-390 to "handle[] the necessary data, data strobe, and data mask signals for read and write commands" and "[d]ata, data strobes and data mask signals are likewise passed to and from the DIMMs" through interface modules 310-390. EX1011, 4:12-60, 5:6-40, 6:11-17, Figs. 1-3. The passing "to and from" of data and data mask values with Mehta's DIMM memory occurs over respective "sub-buses 241-250" of "bus 240." *Id.*, 5:15-40, Figs. 1-3.

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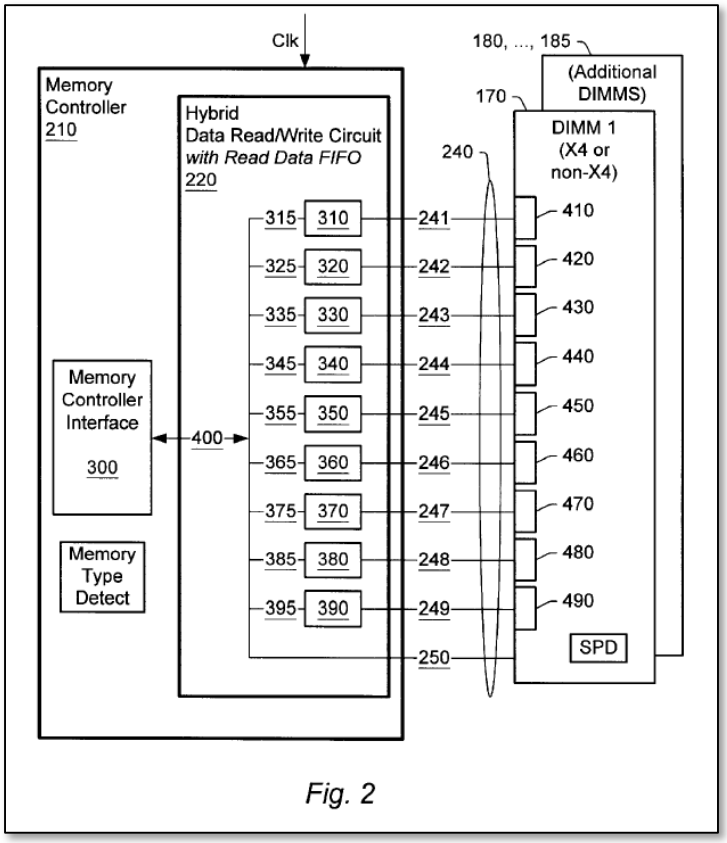

EX1011, Fig. 2

H. Chan

46. Chan is generally directed to a memory controller for accessing a computer memory. EX1012, Abstract. For example, Chan describes that its memory controller contains "memory command queues" 101 through 104 that each correspond to a bank of memory. EX1012, 5:29-6:31, Fig. 4.

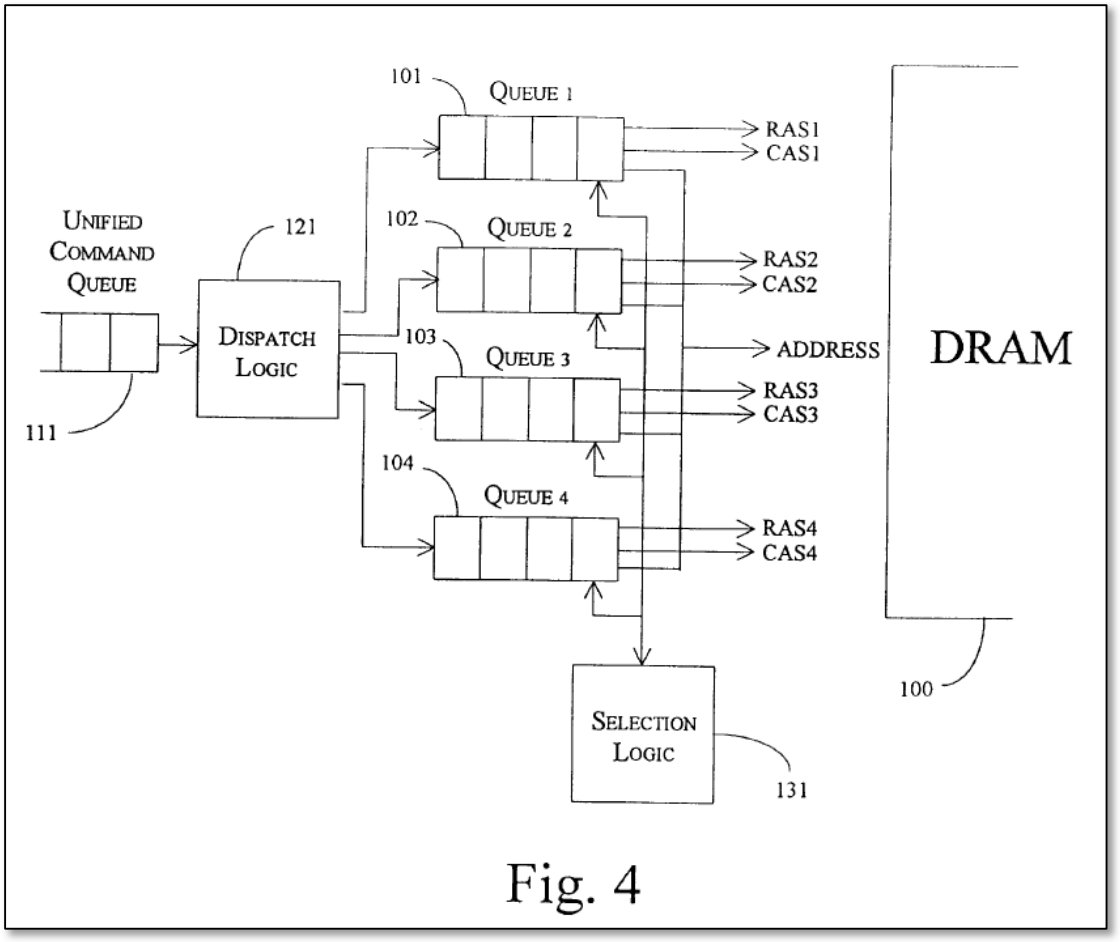

Fig. 4

EX1012, Fig. 4

I. Kobayashi

47. Kobayashi is generally directed to a memory device that allows time-multiplexing row selection and column access commands. EX1013, ¶0163

J. Wilcox

48. Wilcox is generally directed to a memory system that provides data signals from a memory controller interface to a memory. EX1009, Abstract. For example, a memory controller 18 includes a data interface 100 that includes "write path circuitry

120 for purposes of writing data to the system memory 22" and "circuitry associated with the read path of the data interface 100." *Id.*, ¶0028-0030, Fig. 3.

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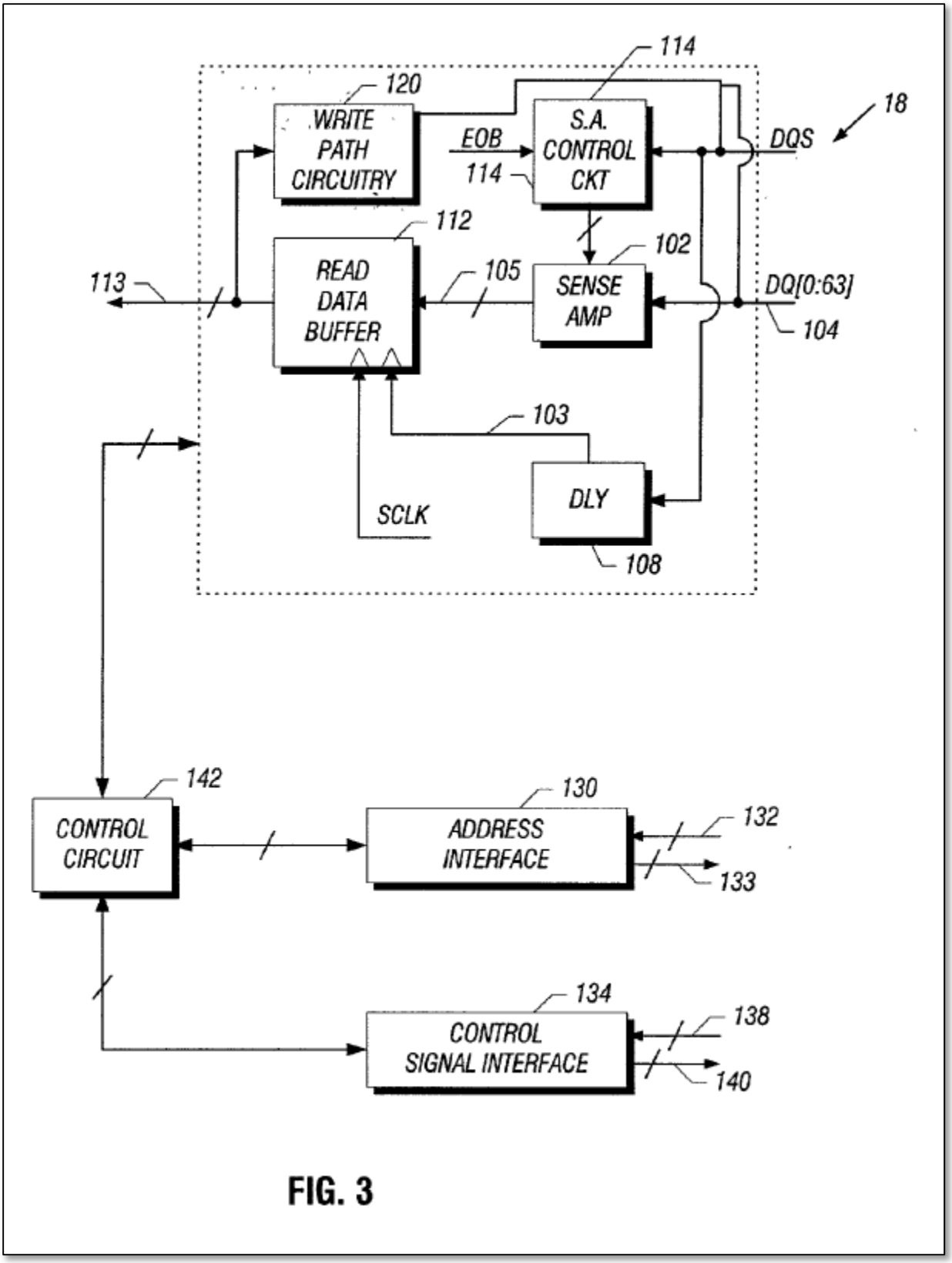
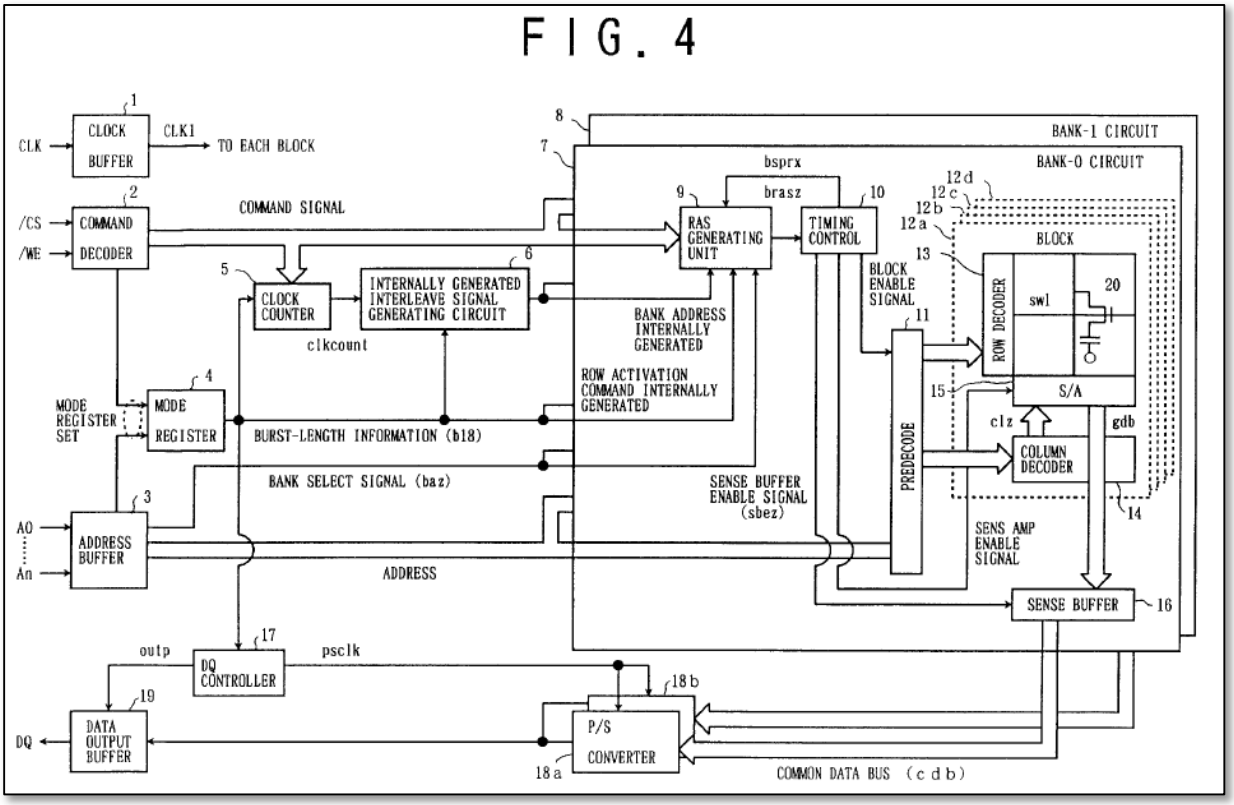


FIG. 3

EX1009, Fig. 3

K. Fujioka

49. Fujioka is generally directed to a memory device that selectively enables memory blocks based on burst length information. EX1004, Abstract. For example, Fujioka's system allows for control of memory cell blocks 12a-12d of bank-0 circuit 7 and bank-1 circuit 8 by "control[][ling] the row decoder 13 to generate a word line select signal swl at an appropriate timing" for a selected memory cell block and "control[ling] the column decoder 14 to generate a column line select signal clz at an appropriate timing" for a selected memory cell block. EX1004, 5:32-60, 6:21-42, 7:5-43, Fig. 4.



EX1004, Fig. 4

50. An example of the timing that results from such control, which schedules issuance of signals swl and cl, is shown in Figure 9. Here, signals swl and cl are controlled. Low to high changes of swl0z are the activations of word lines in blocks of memory cell blocks 12a-12d in the bank-0 circuit 7, and low to high, and low to high changes of the signal swl1z are activations of word lines in blocks of memory cell blocks 12a-12s in the bank-1 circuit 8. EX1004, 12:66-13:45, 13:59-14:37, 8:45-50. Low to high changes of the signal cl0z cause access of data in columns of blocks of memory cell blocks 12a-12d in the bank-0 circuit 7. *Id.*, 7:31-43, 12:67-13:45, 6:35-42. Low to high changes of the signal cl1z cause access of data in columns of blocks (*banks*) of memory cell blocks 12a-12d (*bank group*) in the bank-1 circuit 8. *Id.*, 7:31-43, 13:43-14:37, 6:35-42.

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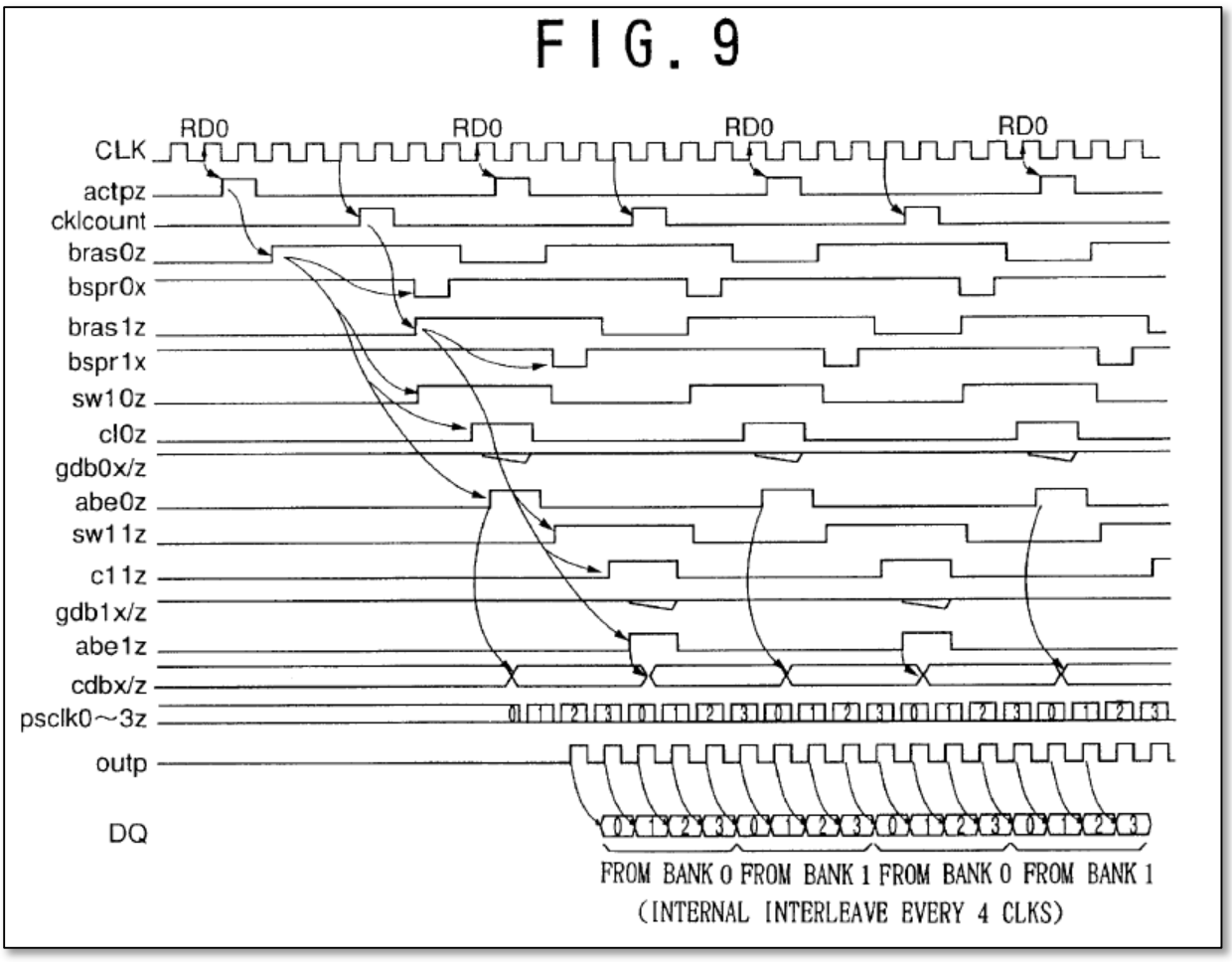

EX1004, Fig. 9

L. Grounds

51. I understand Petitioner's challenge is based on the following grounds:

Ground	Challenged Claims	Reference(s)	Basis
I	1, 2, 4, 9, 10, 20, 22	LaBerge, Bowater	§103(a)
II	3, 21	LaBerge, Bowater, Suh	
III	5	LaBerge, Bowater, Halbert	
IV	6, 7	LaBerge, Bowater, Grundy	
V	8	LaBerge, Bowater, Mehta	
VI	11	LaBerge, Bowater, Chan, Kobayashi	
VII	12, 13, 15	LaBerge, Bowater, Wilcox	
VIII	14	LaBerge, Bowater, Wilcox, Suh	
IX	16	LaBerge, Bowater, Wilcox, Halbert	
X	17, 18	LaBerge, Bowater, Wilcox, Grundy	
XI	19	LaBerge, Bowater, Wilcox, Mehta	
XII	1, 20	Fujioka	

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VII. FILE HISTORY

52. I understand that the U.S. Patent and Trademark Office issued a notice of allowance during prosecution of the '379 patent after a single office action and response. EX1002, 265, 273.

VIII. SPECIFIC GROUNDS FOR PETITION

A. Ground I: LaBerge and Bowater render claims 1, 2, 4, 9, 10, 20, and 22 obvious

1. Claim 1

a. [1a] "*A memory controller to control a memory device, the memory device having a plurality of bank groups*"

53. If limiting, LaBerge discloses or at least renders obvious this claim element. LaBerge describes a "memory hub controller 200" (*A memory controller*) that controls memory of memory modules 310a, 310b,…310n using "command and address signals" (*to control a memory device*). EX1006 (LaBerge), ¶0039, Fig. 6.

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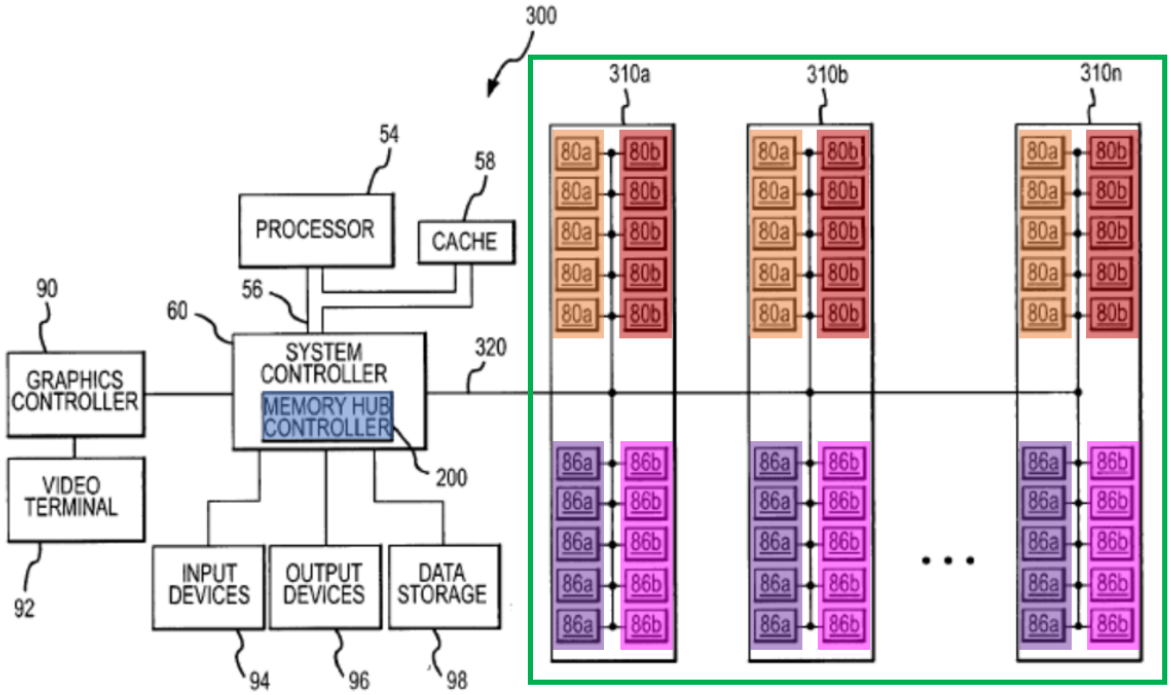

FIG.6

EX1006, Fig. 6 (annotated)

54. Within memory modules 310a, 310b,…310n (*the memory device*), each of memory modules 310a, 310b,…310n respectively includes a group of memory devices formed by devices 80a, 86a, 80b, and 86b, meaning memory modules 310a, 310b,…310n (*the memory device*) include a plurality of groups formed by devices 80a, 86a, 80b, and 86b (*having a plurality of bank groups*), as shown in annotated Figure 6. *Id.*

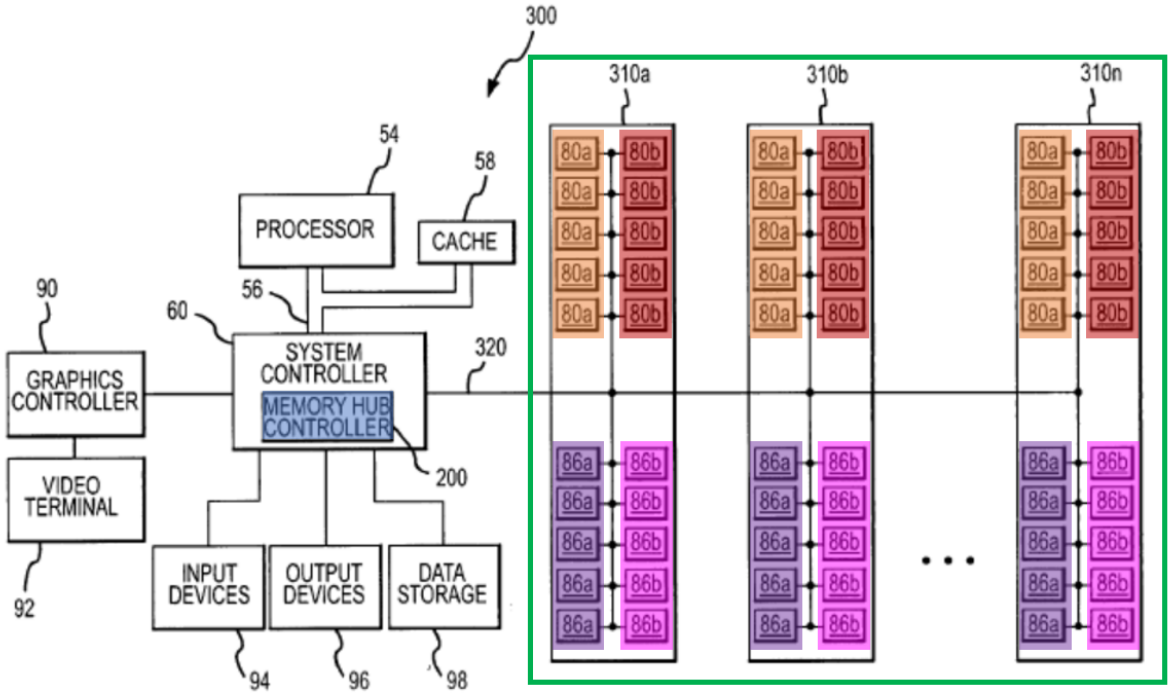

FIG.6

EX1006, Fig. 6 (annotated)

55. A POSITA would have understood or at least found obvious that memory devices 80a, 86a, 80b, and 86b each form a respective memory bank, and that the group of memory devices 80a, 86a, 80b, and 86b in each module 310 is therefore a *bank group*, with the plurality the groups of memory devices 80a, 86a, 80b, and 86b in each of modules 310a, 310b,…310n forming *a plurality of bank groups*. EX1006, ¶0039, Fig. 6. Memory banks are known as being groups of memory devices, just like the devices 80a, 86a, 80b, and 86b across modules 310. For example, Suh explains that memory cell arrays are "grouped into banks." EX1005, 1:8-27. I also note that LaBerge itself explicitly discloses bank addresses BA0, BA1, BA2, and

BA3; this further supports that a POSITA would have understood or at least found obvious that devices 80a, 86a, 80b, and 86b would each have been addressed as a bank. EX1006, ¶0029.

b. *[1b] "the memory controller comprising: circuitry to provide a clock signal to the memory device, the clock signal having clock transitions;"*

56. LaBerge discloses or at least renders obvious element [1b]. LaBerge describes memory hub controller 200 (*the memory controller*) includes "clock signals CLK0, CLK1, CLKZ0, and CLKZ1" (*a clock signal*) that drive ring buffers 240 and 242 and are also "applied to the memory devices 80, 86" of memory modules 310 (*provide a clock signal to the memory device*). EX1006, ¶¶0038-0039, Figs. 5 (clock signal "CLK" in memory hub controller 200), 6.

57. A POSITA would have understood or at least found obvious that memory hub controller 200 comprises circuitry that provides the clock signals to memory devices 80 and 86 of memory modules 310 (*memory controller comprising: circuitry to provide a clock signal to the memory device*). EX1006, ¶¶0038-0039, Figs. 5, 6. Such circuitry is needed to generate and/or receive such clock signals and "appl[][y]" them to memory devices 80 and 86 of memory modules 310. *Id.*

58. A POSITA would have further understood or at least found obvious that the clock signals CLK0, CLK1, CLKZ0, and CLKZ1 have clock transitions between low and high states (*the clock signal having clock transitions*) because this was the

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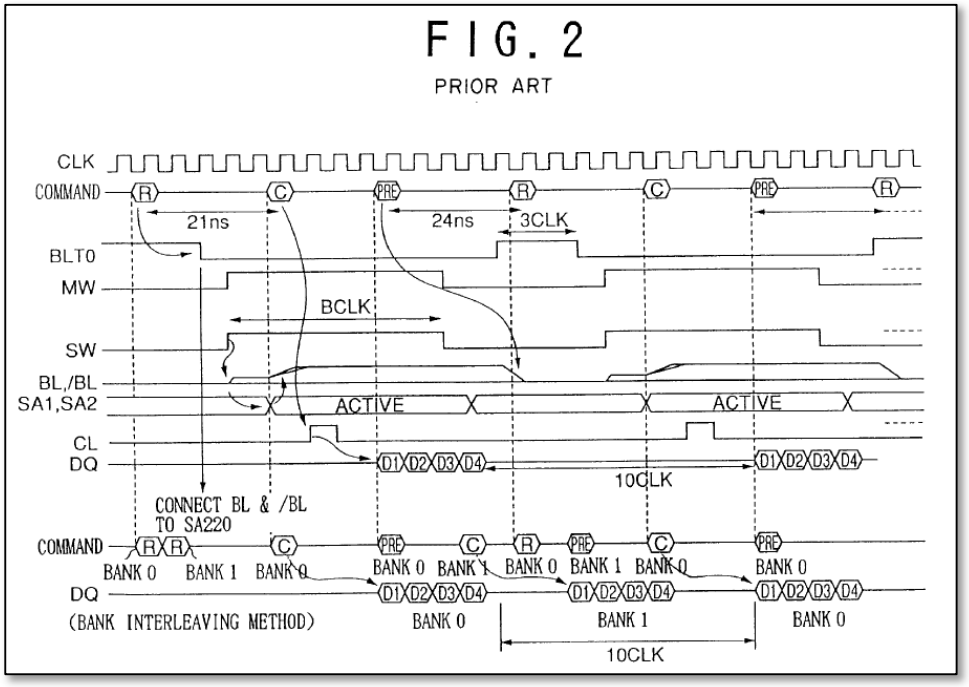
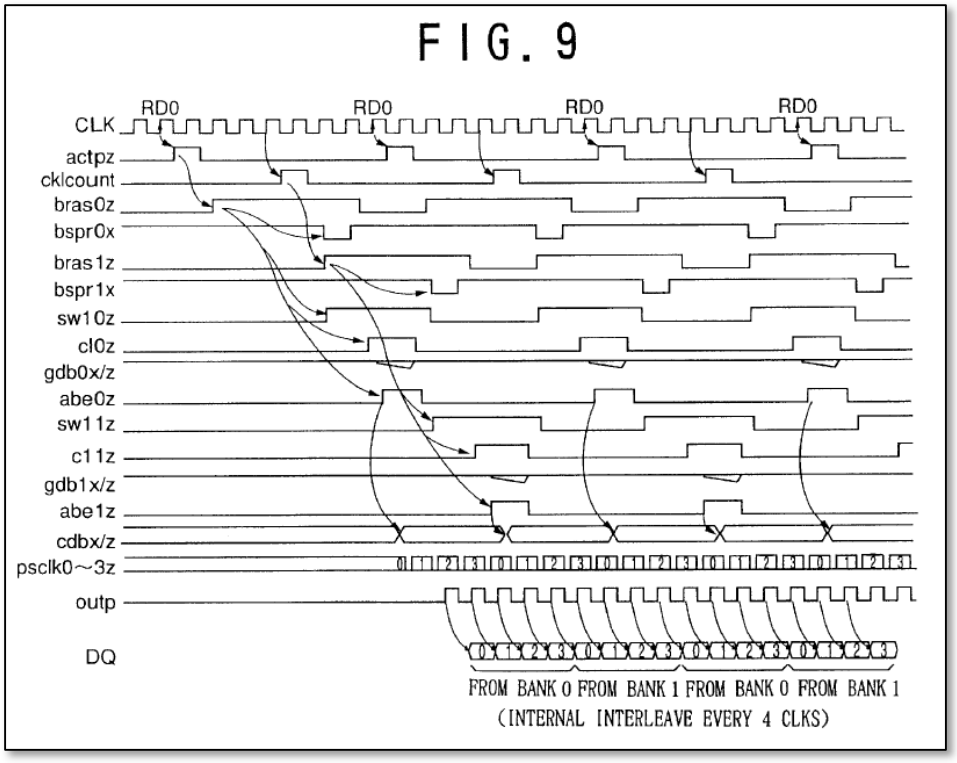
well-known way in which clock signals were implemented. EX1006, ¶¶0038-0039, Figs. 5, 6. For example, Fujioka shows that clock signals ("CLK") have clock transitions between low and high states. EX1004, Figs. 2, Fig. 9.



EX1004, Fig. 2



EX1004, Fig. 9

59. If *circuitry to provide a clock signal* is interpreted as a means-plus-function term, LaBerge discloses or at least renders obvious (1) the identified function for the reasons discussed above, and (2) the identified structure of memory controller hardware and equivalents thereof (Section V.A). This is because it describes memory controller hardware, i.e., circuitry of memory hub controller 200 that handles and provides clock signals to memory devices. Further, the circuitry of memory hub controller 200 is at least an equivalent to memory controller hardware because both perform the same functionality of *provid[ing] a clock signal to the memory device* in substantially the same way, i.e., by outputting a clock signal. A POSITA would

have further recognized the interchangeability of LaBerge's circuitry of memory hub controller 200 with the identified structure as both are used to provide a clock signal, and such interchangeability would have been routine and well-within the capabilities of a POSITA for the same reasons. I further note that LaBerge's circuitry of memory hub controller 200 is not excluded by any explicit definition in the '379 patent's specification for an equivalent to the identified structure.

c. ***[1c] "[the memory controller comprising:] a command interface to transmit, to the memory device, row activation commands to instruct row activations and column access commands to instruct column accesses; and"***

60. LaBerge discloses or at least renders obvious element [1c]. LaBerge describes memory controller 200 (*the memory controller*) includes command shifter 214, multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242, which collectively form a *command interface* as they provide an interface via which command and address signals are transmitted from memory controller 200 to memory devices 80 and 86 of memory modules 310a-310n. EX1006, ¶¶0034-0039, Figs. 5, 6.

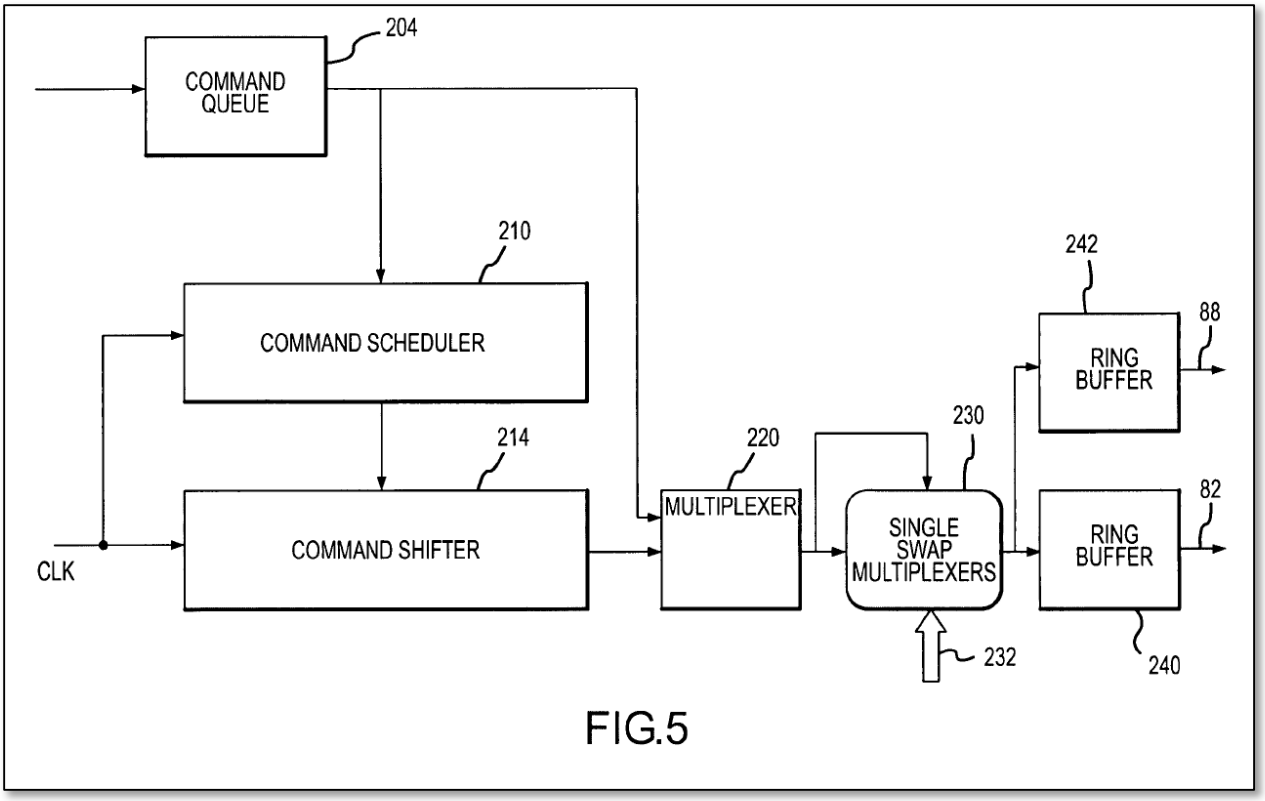


FIG.5

EX1006, Fig. 5

61. Multiplexor 220 receives at its input, from command shifter 214, "properly timed and ordered command and address signals," and also "receives the DRAM command and address signals at a second input directly from the Command Queue 204." EX1006, ¶0036, Fig. 5. These command and address signals are output by multiplexor 220 to single swap multiplexors 230, which routes them to ring buffers 240 and 242. *Id.*, ¶¶0037-0038, Fig. 5. Ring buffers then send the command and address signals to memory devices 80 and 86, via bus 320, depending on which memory device is being accessed and whether the memory device is operating in DDR2 or DDR3 mode. *Id.*, ¶¶0038-0039, Figs. 5, 6.

62. The command and address signals include "DRAM command signals" such as "RASZ," which is a "row address strobe" signal and known as being used to activate rows of memory, and "CASZ," which is a "column address strobe" signal and known as being used to access columns of memory. EX1006, ¶¶0029, 0034-0036; *id.*, ¶0003 (referring to RAS and CAS signals as "command" signals). For example, Dye explains that a DRAM can receive "inputs," including "Row Address Strobe" and "Column Address Strobe," and "controls the access to specified row and column addresses in the array." EX1014 (Dye), 2:41-54; *id.*, 3:39-46 (noting "control signals" include "e.g., CAS, RAS…").

63. Thus, LaBerge describes its command shifter 214, multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242 (*command interface*) transmit to memory devices 80 and 86 of memory modules 310a-310n (*transmit, to the memory device*) RASZ signals that instruct the memory devices to activate desired memory rows and CASZ signals that instruct the memory devices to allow access to desired memory columns (*row activation commands to instruct row activations and column access commands to instruct column accesses*). EX1006, ¶¶0034-0039, Figs. 5, 6.

64. If *a command interface to transmit…*is interpreted as a means-plus-function term, LaBerge discloses or at least renders obvious (1) the identified function for the same reasons discussed above and (2) the identified structure of memory controller

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hardware and equivalents thereof (Section V.B) because it describes memory controller hardware in the form of command shifter 214, multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242 as discussed above. Further, multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242 form at least an equivalent to memory controller hardware because both perform the same functionality of *transmit[ting], to the memory device, row activation commands…and column access commands* in substantially the same way, i.e., by transmitting row activation commands and column access commands to memory banks. A POSITA would have further recognized the interchangeability of LaBerge's multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242 with the identified structure. Both are used to transmit row activation commands and column access commands to memory banks, and such interchangeability would have been routine and well-within the capabilities of a POSITA for the same reasons. Moreover, LaBerge's multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242 are not excluded by any explicit definition in the '379 patent's specification for an equivalent to the identified structure.

d. *[1d] "[the memory controller comprising:] circuitry to schedule issuance of the row activation commands and the column access commands from the command interface, such that"*

65. LaBerge discloses or at least renders obvious element [1d]. LaBerge describes memory controller 200 (*the memory controller*) includes command scheduler 210

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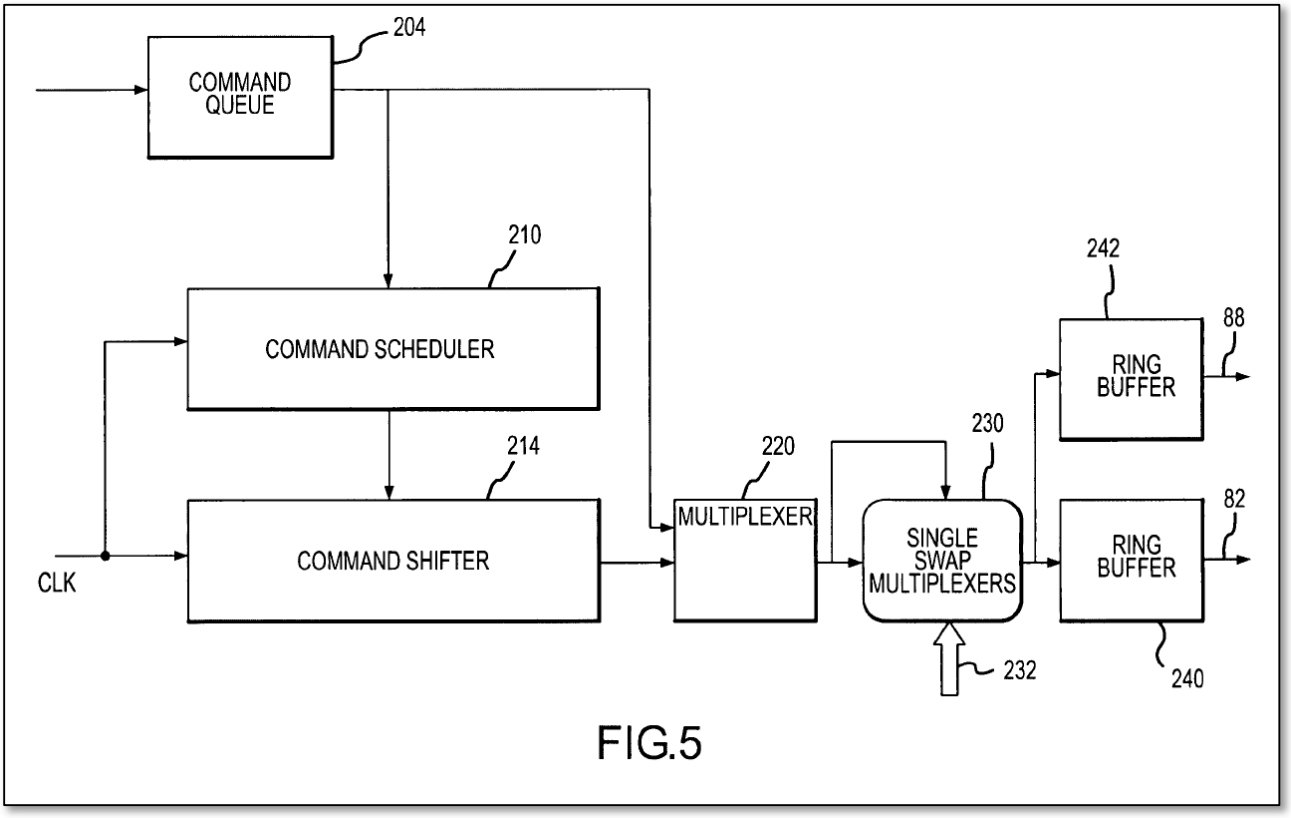
(*circuitry to schedule*), which "spaces the command and address signals apart from each other with the proper delay." EX1006, ¶0035, Figs. 5, 6; *id.*, ¶0034 ("memory controller 200…schedules the DRAM commands for outputting at the proper time").



EX1006, Fig. 5

66. LaBerge explains that "delay is measured in periods of the clock CLK signal" and that, in one example, "Command Scheduler 210 might schedule[] the CASZ to be output three clock periods after the RASZ signals [were] [] output from the Command Scheduler 210." EX1006, ¶¶0034-0035. Command scheduler 210 outputs the scheduled RASZ and CASZ commands to command shifter 214, which outputs them to multiplexor 220; the signals are then sent to single swap multiplexers 230

and then to buffers 240 and 242 for output to memory devices 80 and 86. *Id.*, ¶¶0034-0039, Figs. 5, 6. LaBerge therefore describes that command scheduler 210 schedules (*circuitry to schedule*) issuance of the RASZ and CASZ signals (*issuance of the row activation commands and the column access commands*) from command shifter 214, multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242 (*from the command interface*). *Id.*

67. If *circuitry to schedule issuance…*is interpreted as a means-plus-function term, LaBerge discloses or at least renders obvious (1) the identified function for the same reasons discussed above and (2) the identified structure of memory controller hardware and equivalents thereof (Section V.A) because it teaches memory controller hardware in the form of command scheduler 210 as discussed above. Moreover, command scheduler 210 is part of memory controller 200, and a POSITA would have understood or at least found obvious that it is formed by circuitry. Indeed, LaBerge explains memory controller 200 is implemented by "circuits" that perform the described functionality. LaBerge, ¶0041. Further, command scheduler 210 forms at least an equivalent to memory controller hardware because both perform the same functionality of *schedule[ing] issuance of the row activation commands and the column access commands from the command interface* in substantially the same way, i.e., by determining the appropriate timing by which commands are to be sent. A POSITA would have further recognized the

interchangeability of LaBerge's command scheduler 210 with the identified structure as both are used to schedule such commands, and such interchangeability would have been routine and well-within the capabilities of a POSITA for the same reasons. Moreover, LaBerge's command scheduler 210 is not excluded by any explicit definition in the '379 patent's specification for an equivalent to the identified structure.

e. ***[1e] "a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common bank group, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups, and"***

68. LaBerge and Bowater render obvious element [1e]. As noted for element [1d], LaBerge describes that command scheduler 210 (*circuitry to schedule*) "spaces the command and address signals apart from each other with the proper delay" and that scheduled CASZ commands, which are column accesses, and RASZ commands (*row activations*) are output to memory devices 80 and 86. EX1006, ¶¶0034-0039, Figs. 5, 6. LaBerge explains that "delay is measured in periods of the clock CLK signal" and that, in one example, "Command Scheduler 210 might schedule[] the CASZ to be output three clock periods after the RASZ signals [were] [] output from the Command Scheduler 210." *Id.*, ¶¶0034-0035.

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69. If LaBerge is found not to explicitly disclose that its command scheduler 210 schedules issuance of the RASZ and CASZ commands to meet element [1e], the combination of LaBerge and Bowater renders obvious element [1e]. Specifically, in the combination of LaBerge and Bowater, Bowater teaches a "memory controller" that controls "several different banks of memory," where "memory accesses are modified for each bank in order to maintain optimum performance." EX1007, 4:13-15, Fig. 2. Figure 2 shows a timing diagram of control signals issued by Bowater's memory controller; specifically, Figure 2 shows "address signals, RAS signals, CAS signals, and data signals," where "cycle time of these control signals are dynamically modified to change the RAS access time and precharge time, and the CAS access time and precharge time" by Bowater's system. *Id.*, 4:19-24, Fig. 2.

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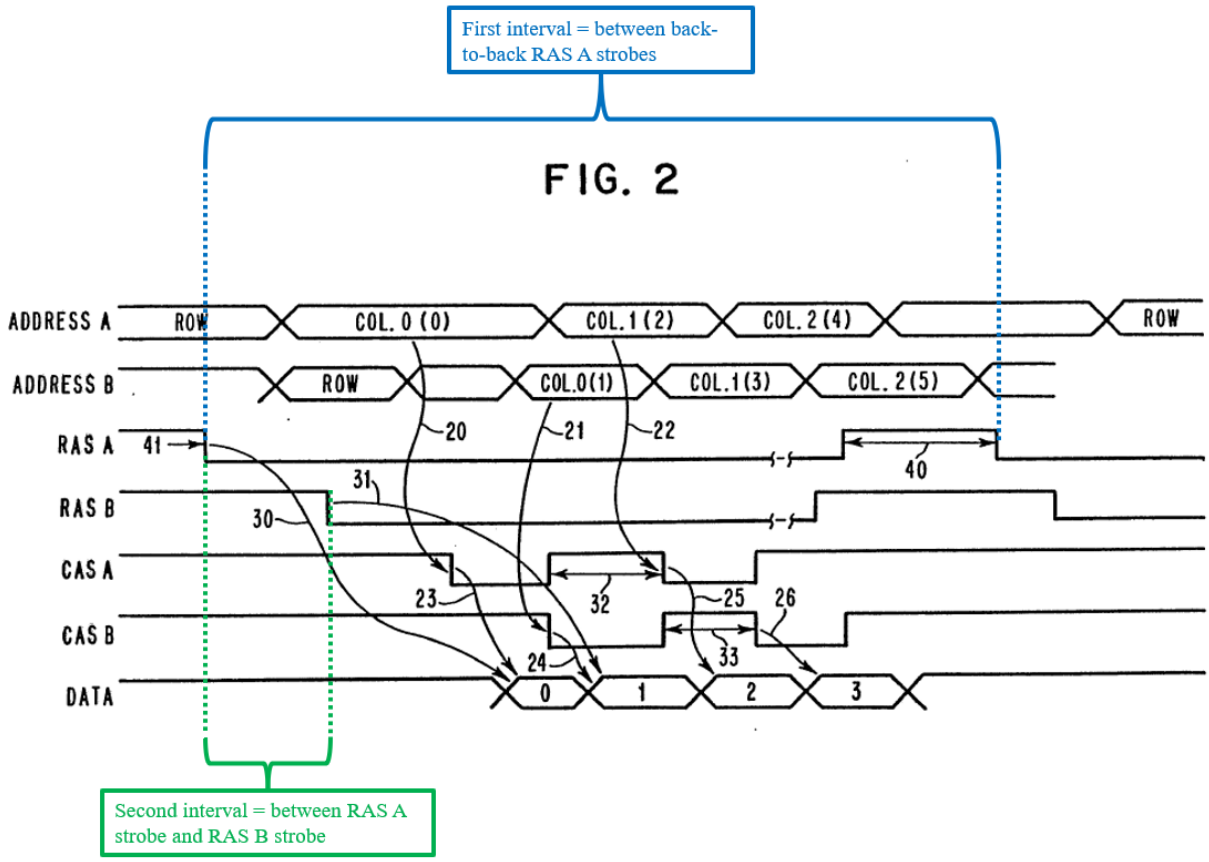
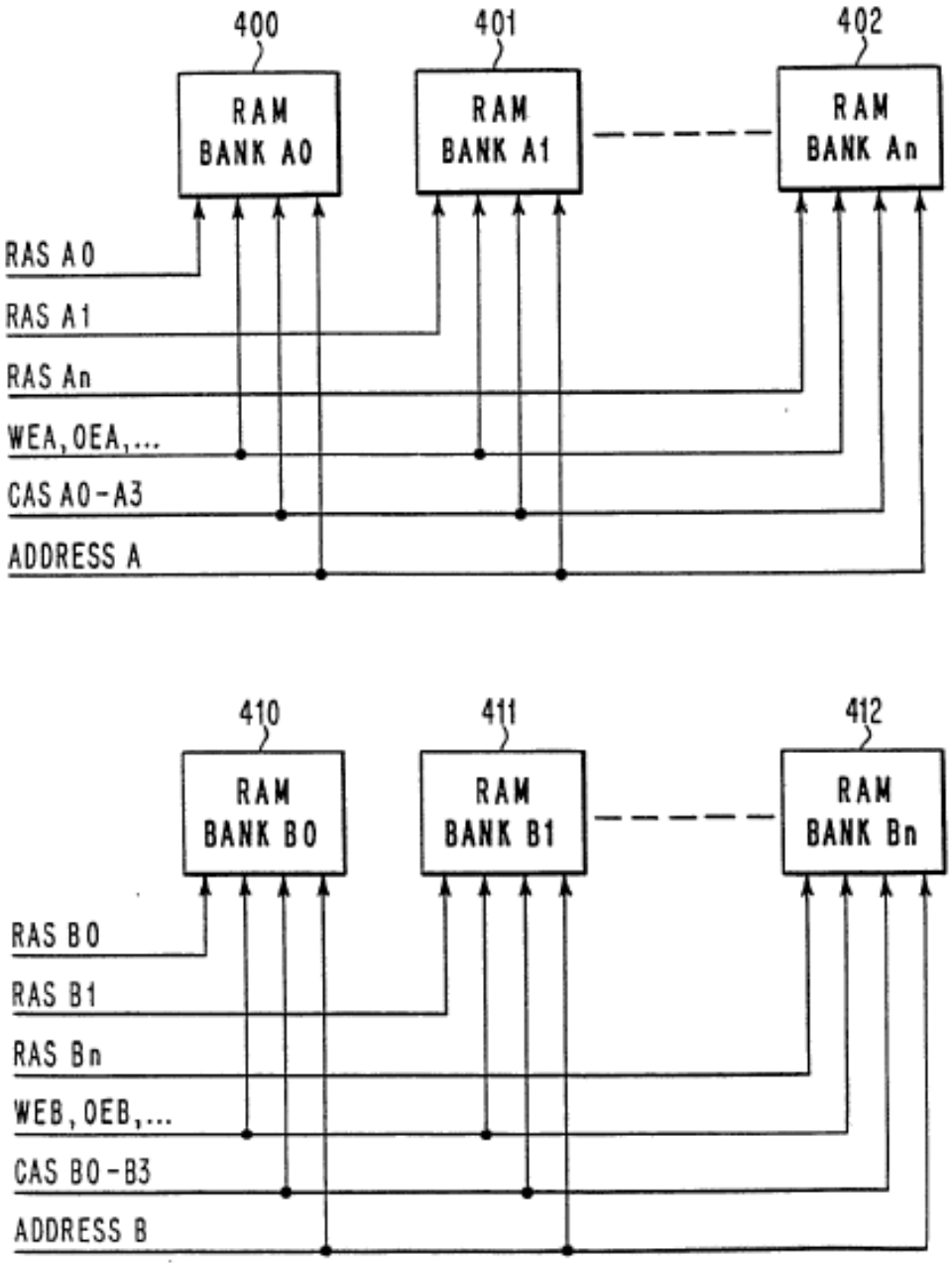


EX1007, Fig. 2 (annotated)

70. As shown by Figure 2, Bowater's memory controller issues back-to-back RAS A commands over an interval shown in annotated Figure 2 above. EX1007, 4:13-40, Fig. 2. As shown by Figure 6 below, these RAS A commands are row activations to rows within banks A0-An of the bank A group. *Id.*, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6; *id.*, 7:2-3 ("Fig. 6 shows how control signals connect to banks of memory for two-way interleaving. These control signals are illustrated in Fig. 2"). And Bowater's memory controller also issues RAS B commands which are row activations to rows within banks B0-Bn of the same bank B group. *Id.* Indeed,

Bowater's process is for "two memory banks being interleaved"—bank A and bank B—where RAS A are commands sent to bank A and RAS B are commands sent to bank B. *Id.*

FIG. 6



EX1007, Fig. 6

71. Thus, as combined with LaBerge such RAS A commands would have been applied to banks within a common bank group formed of memory devices 80a, 86a, 80b, and 86b in a **module 310a** (*bank group*) of LaBerge, while RAS B commands would have been applied to banks within another common bank group formed of memory devices 80a, 86a, 80b, and 86b in a **module 310b** (another *bank group*) of LaBerge. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6; VIII.A.1.a (element [1a]) (explaining each of devices 80a, 86a, 80b, and 86b is a *bank*, and the collection of devices 80a, 86a, 80b, and 86b in each module 310 is a *bank group*). Such commands would have been applied by LaBerge's memory controller 200 "to the signal lines of bus 320 depending on which memory devices 80a, 86a, 80b or 86b [banks] are being accessed." EX1006, ¶0039.

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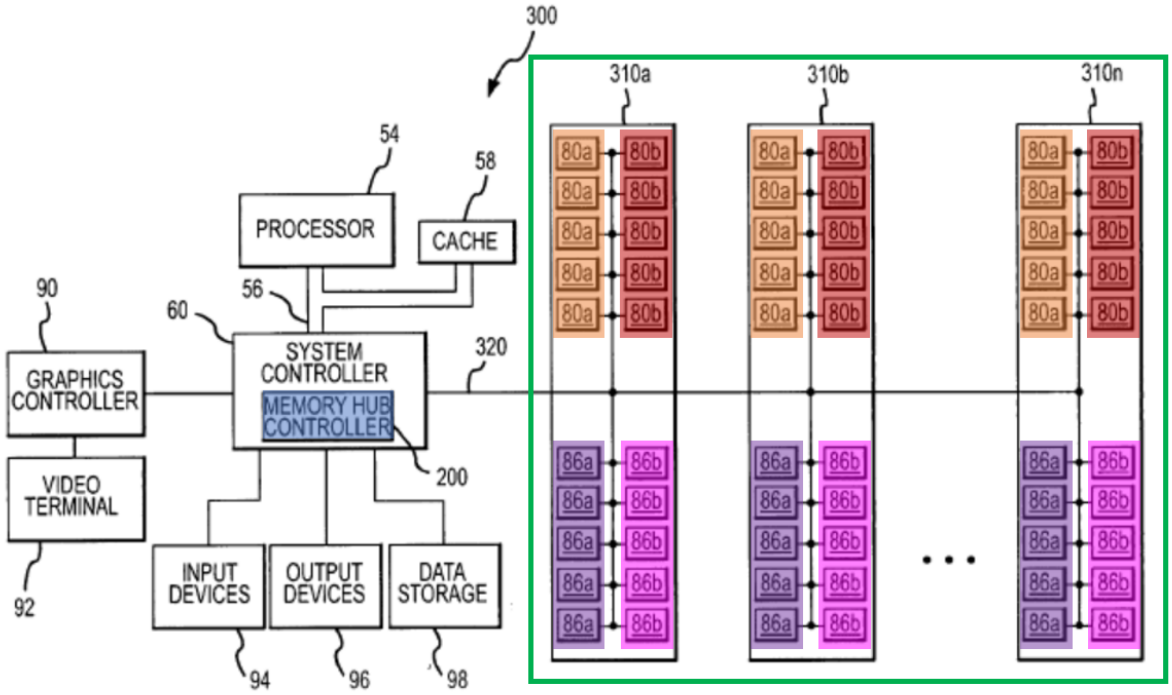
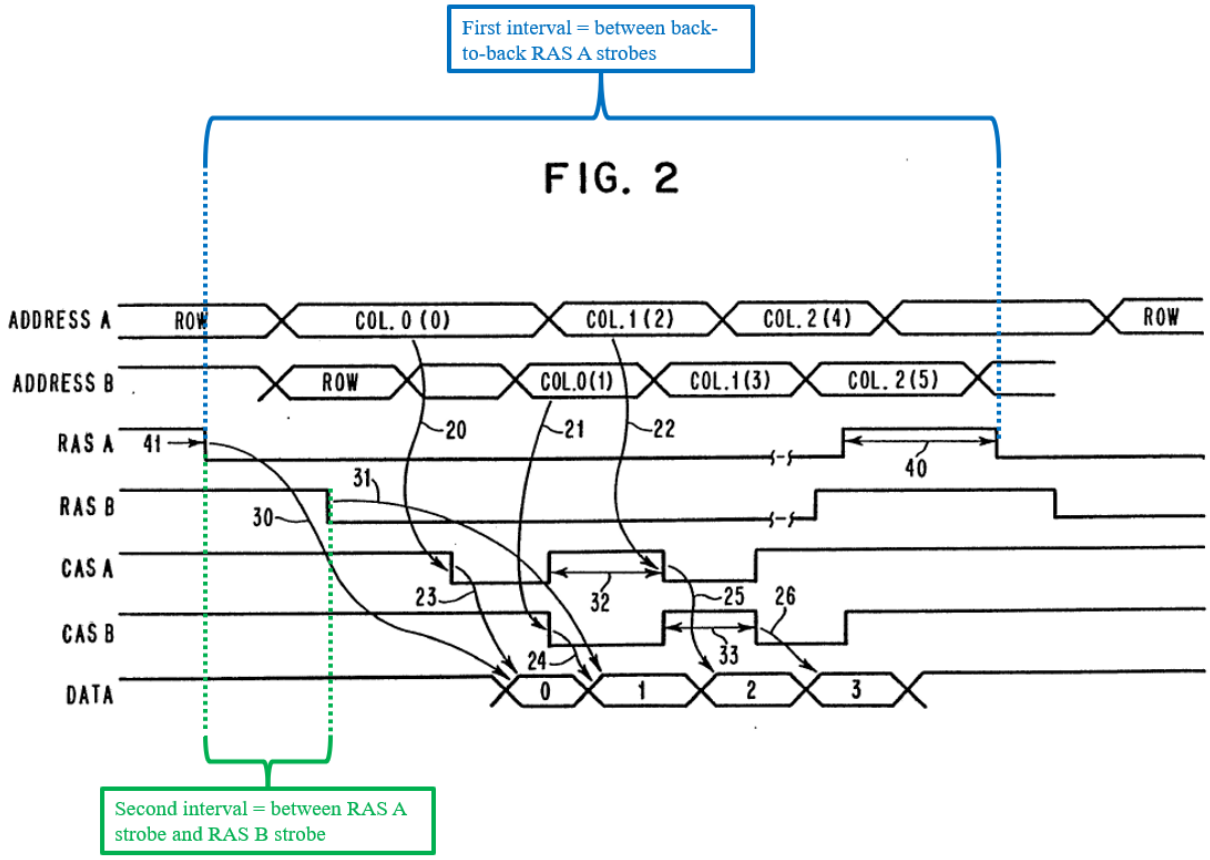


FIG.6

EX1006, Fig. 6 (annotated)

72. Thus, in the LaBerge-Bowater combined system, LaBerge's command scheduler 210 (*circuitry to schedule*) would have scheduled issuance of the RAS and CAS commands such that a first interval of clock transitions to transpire between back to back RAS A commands to banks within a common bank group formed of memory devices 80a, 86a, 80b, and 86b in **module 310a** is provided (*a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common bank group*) and a second interval of clock transitions to transpire between back to back row activations to banks within different bank groups—i.e., row activation using RAS A to memory devices 80a,

86a, 80b, and 86b in **module 310a** and a subsequent row activation using RAS B to memory devices 80a, 86a, 80b, and 86b in **module 310b**—is provided (*second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups*), as shown by Figure 2 below. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6.



EX1007, Fig. 2 (annotated)

73. As shown by Figure 2 above, the first interval is *longer* than the second interval. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 4:13-40, 6:32-50, 7:1-13, Figs.

2, 4, 6. Moreover, a POSITA would have understood or at least found obvious that the claimed intervals are defined by "*clock transitions*" as claimed because LaBerge explicitly explains that timing of its CAS and RAS signals are defined by "periods of the clock CLK signal" and that "clock periods" define intervals between signals. EX1006, ¶¶0034-0039, Figs. 5, 6. Moreover, defining intervals in such a manner was well-known in the art. For example, Fujioka shows that clock signals ("CLK") have clock transitions between low and high states, and Fujioka defines intervals between signals that are sent to banks, where transitions of CLK define intervals between when word line signal activations (signals "swl") are sent to banks, and also define intervals between when column activation signals (signals "cl") are sent to banks. EX1004, 6:35-42, 7:31-43, 8:45-50, 12:66-14:37, Fig. 9.

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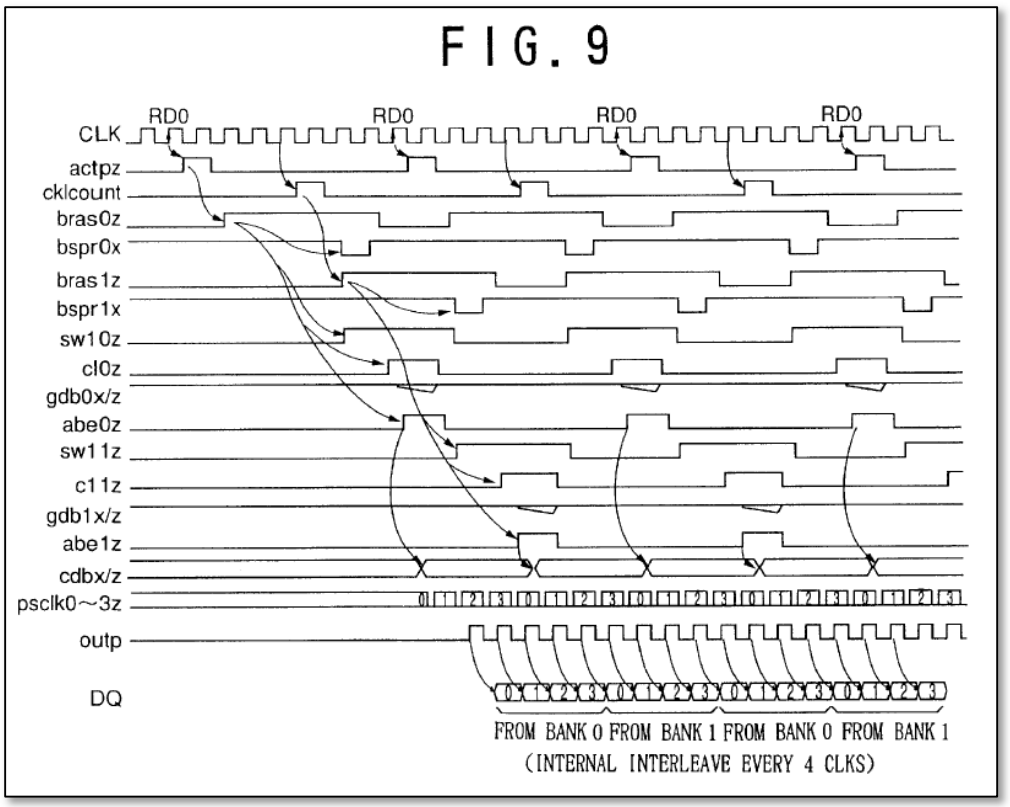
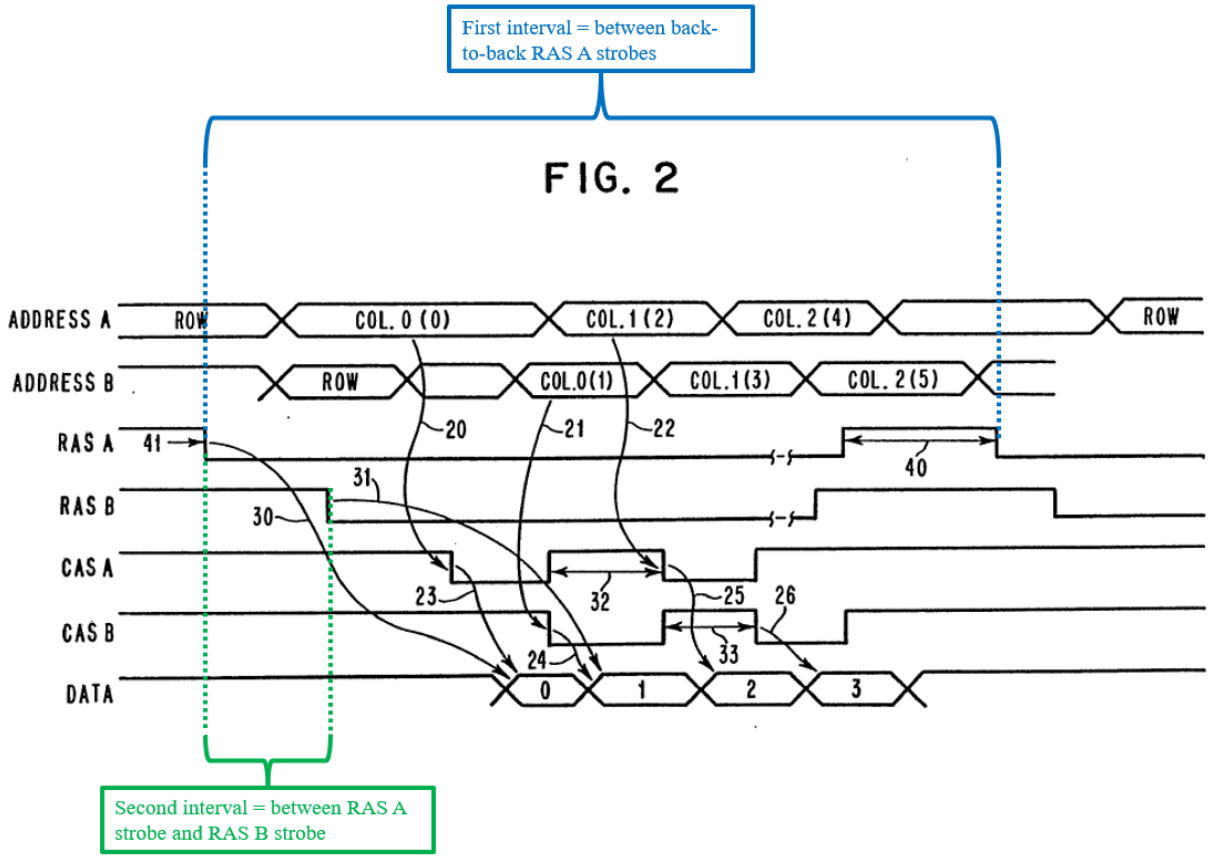


EX1004, Fig. 9

Motivation to Combine

74. A POSITA would have been motivated to combine LaBerge and Bowater such that LaBerge's command scheduler 210 schedules RAS and CAS commands as taught by Bowater. The combination would have enhanced LaBerge's system by providing increased flexibility and an additional technique by which RAS and CAS commands are scheduled and would have been nothing more than a design choice implemented by a POSITA. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6.

75. Combined, LaBerge's command scheduler 210 would have scheduled commands as taught by Bowater, including with the timing of Bowater's Figure 2, and would have transmitted commands, as taught by Bowater, via LaBerge's memory bus 320. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6. Such a combination would have been routine and straightforward to POSITAs. *Id.*



EX1007, Fig. 2 (annotated)

76. Indeed, LaBerge already describes that "memory controller 200 applies command and address signals…to the signal lines of the bus 320 depending on

which memory devices 80a, 86a, 80b or 86b are being accessed." EX1006, ¶0039. Each of memory devices 80a, 86a, 80b or 86b is a bank, and the collection of devices 80a, 86a, 80b, and 86b in each module 310 is a bank group. Section VIII.A.1.a. And LaBerge already describes that command scheduler 210 of memory controller 200 schedules RAS and CAS commands, such as where one is delayed by a number of clock cycles relative to the other. EX1006, ¶¶0034-0039, Figs. 5, 6.

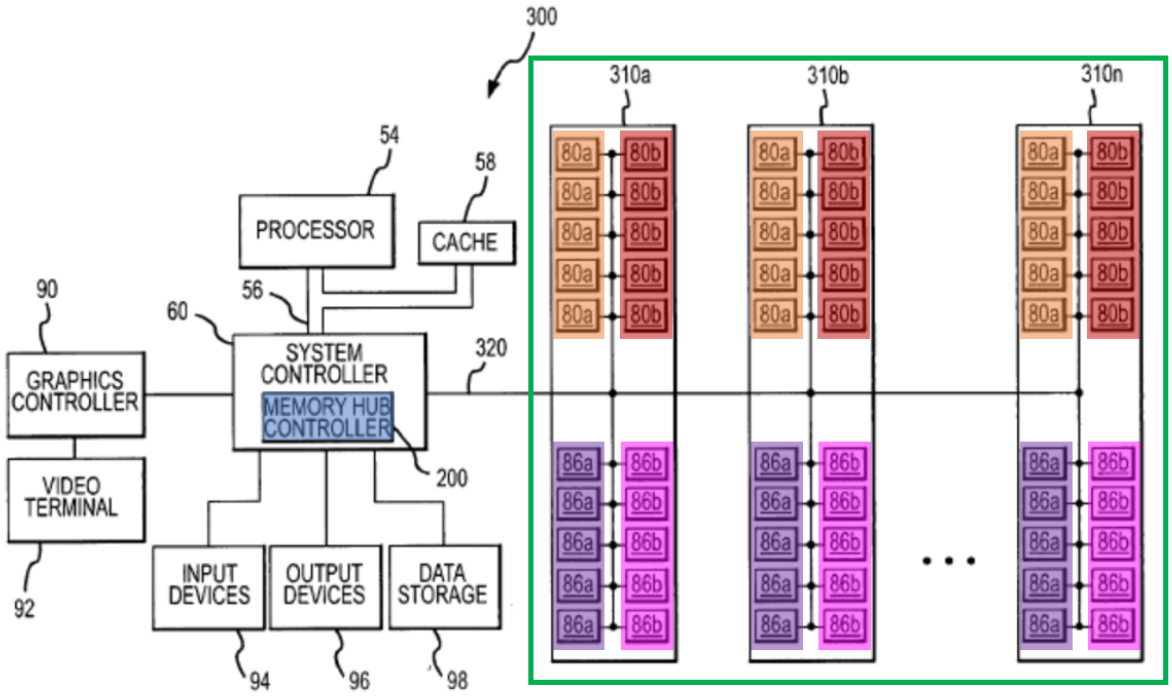


FIG.6

EX1006, Fig. 6 (annotated)

77. Bowater, applicable to LaBerge in that it similarly is directed to controlling memory using RAS and CAS commands, teaches that a memory controller may

dynamically access memory using RAS and CAS commands to banks in a particular group—banks A0 to An in a bank A group, and banks B0-Bn in a bank B group—via the technique of the timing diagram in Figure 2, where such commands are controlled to occur at certain times. EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6.

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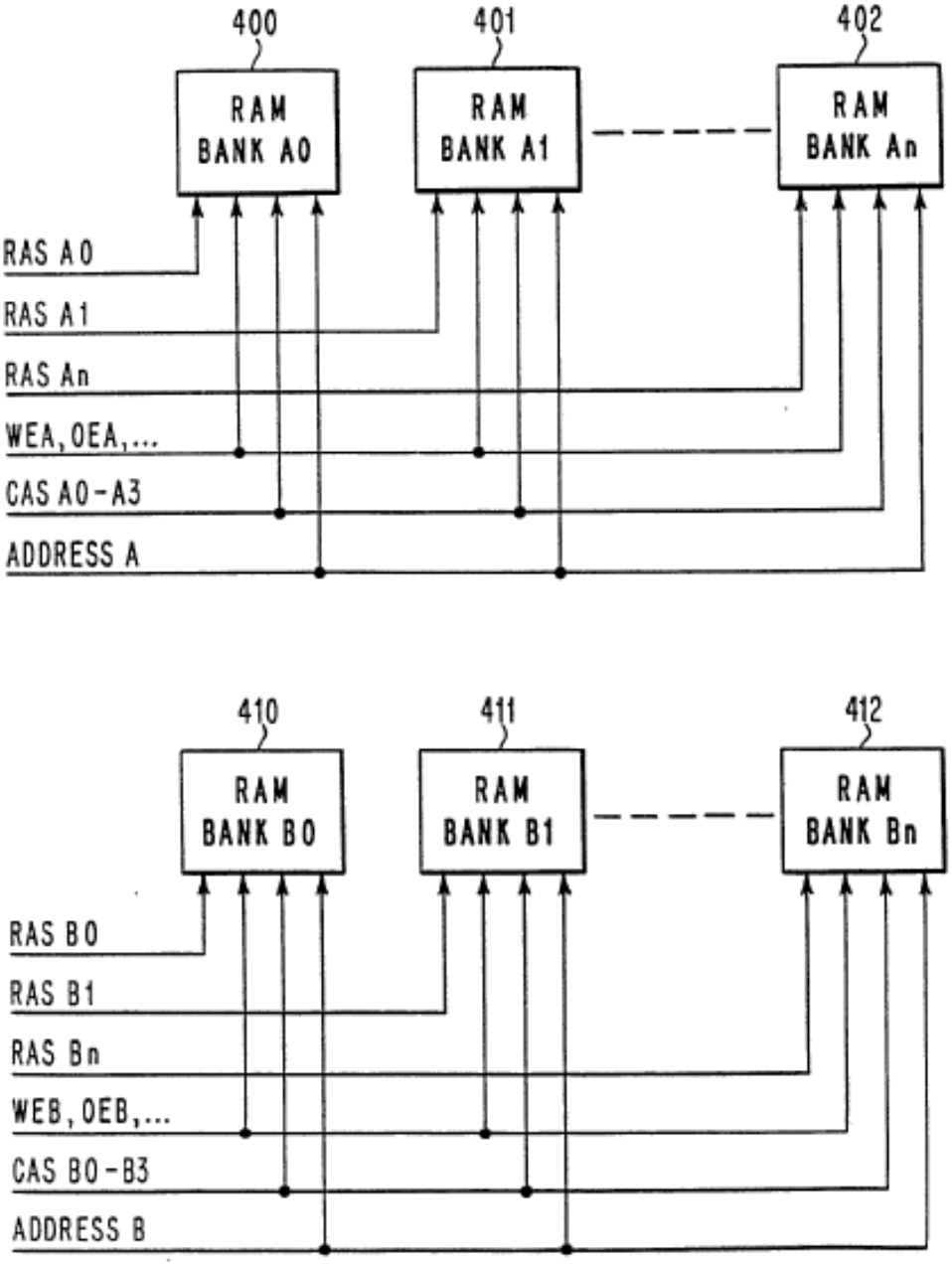
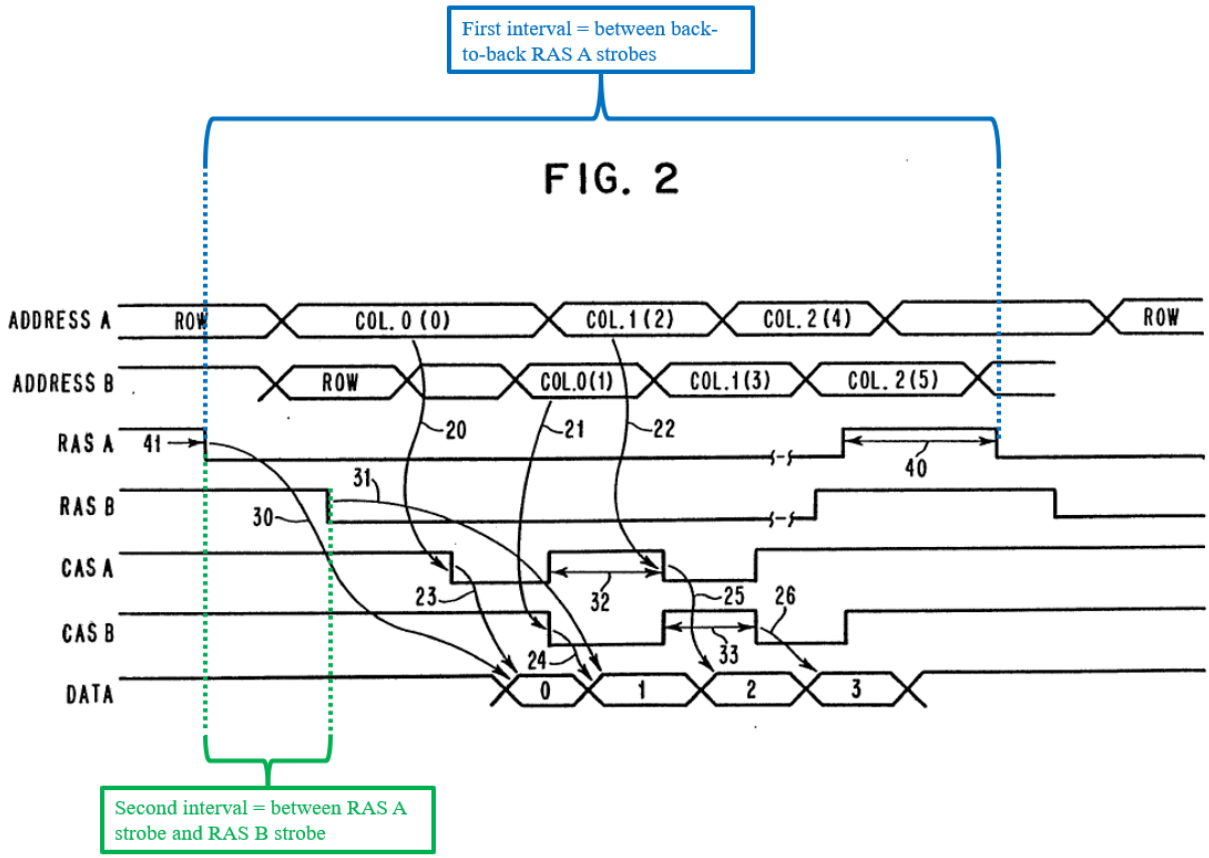
FIG. 6



EX1007, Fig. 6



EX1007, Fig. 2 (annotated)

78. Indeed, Bowater explains that its system provides "a dynamic memory controller to permit more flexibility than has been provided in available memory controllers," where "[m]emory attributes related to row address strobe (RAS) and column address strobe (CAS) have been made programmable" which "allows the speed of memory access to be altered." EX1007, 3:35-38; *id*, 3:5-18 ("The object of the invention is provide a flexible dynamic memory controller operable with dynamic RAMS having a wide range of operating characteristics is described,

including different operating speeds for various memory functions, and the usage of memories" and describing its system "allows extra delays on signals," where such delays are "dynamically determined by the memory controller"). Bowater is therefore explicitly directed to a memory controller that determines timing of its RAS and CAS signals and schedules them, i.e., by allowing extra delay, as needed. *Id.*; *id.*, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6.

79. Enhancing LaBerge with Bowater would have therefore been straightforward and well-within the capabilities of POSITAs, and provided a design choice as to how LaBerge's system, which schedules RAS and CAS signals, is implemented. Specifically, Bowater teaches a design choice as to how, within the context of signals transmitted to different banks within a bank group (e.g., signals to banks A0-An in a common bank group A; signals to banks B0-Bn in a common bank group B), CAS are scheduled relative to each other and RAS are scheduled relative to each other—again, a straightforward and routine matter for POSITAs due to the fact that LaBerge already discloses command scheduler 210 scheduling CAS and RAS commands and transmitting them to devices 80a, 86a, 80b, an 86b of modules 310 (i.e., 310a, 310b) via bus 320 "depending on which" device is being accessed. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6.

80. A POSITA would have combined LaBerge and Bowater as above using known hardware and software techniques associated with memory devices, and for the same

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reasons discussed above, a POSITA would have readily combined Bowater's teachings with LaBerge. And separate or combined, the LaBerge and Bowater systems would have both performed the same memory and data storage functionality. The combination would have further been predictable, straightforward, and routine for a POSITA, and a POSITA would have recognized as much. And a POSITA would have had a reasonable expectation of success in making this combination for the same reasons discussed above, and also due to the similarities of both references, where both references are at least directed to memory controllers that use RAS and CAS commands to access memory. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 3:35-46, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6.

81. Additionally, both LaBerge and Bowater are analogous art to the '379 patent, from the same field of endeavor as the patent (e.g., memory systems) and pertinent to the particular problem the patent was trying to solve (e.g., improving memory performance). EX1001, Abstract, 1:28-29, 4:1-20; EX1006, Abstract, ¶¶0001, 0013-0014; EX1007, Abstract, 2:1-2, 3:5-18, 9:53-10:8.

f. ***[1f] "a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups."***

82. LaBerge and Bowater render obvious element [1f]. LaBerge describes command scheduler 210 (*circuitry to schedule*) "spaces the command and address

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signals apart from each other with the proper delay" and that scheduled CASZ commands (*column accesses*) and RASZ commands are output to memory devices 80 and 86. EX1006, ¶¶0034-0039, Figs. 5, 6; Section VIII.A.1.d (element [1d]). LaBerge explains that "delay is measured in periods of the clock CLK signal" and that, in one example, "Command Scheduler 210 might schedule[] the CASZ to be output three clock periods after the RASZ signals [were] [] output from the Command Scheduler 210." EX1006, ¶¶0034-0035.

83. If LaBerge is found not to explicitly disclose that its command scheduler 210 schedules issuance of the RASZ and CASZ commands to meet element [1f], the combination of LaBerge and Bowater renders obvious element [1f]. Specifically, in the combination of LaBerge and Bowater, Bowater teaches a "memory controller" and Figure 2 shows a timing diagram of RAS and CAS controls signals issued by Bowater's memory controller as discussed in Section VIII.A.1.e (element [1e]).

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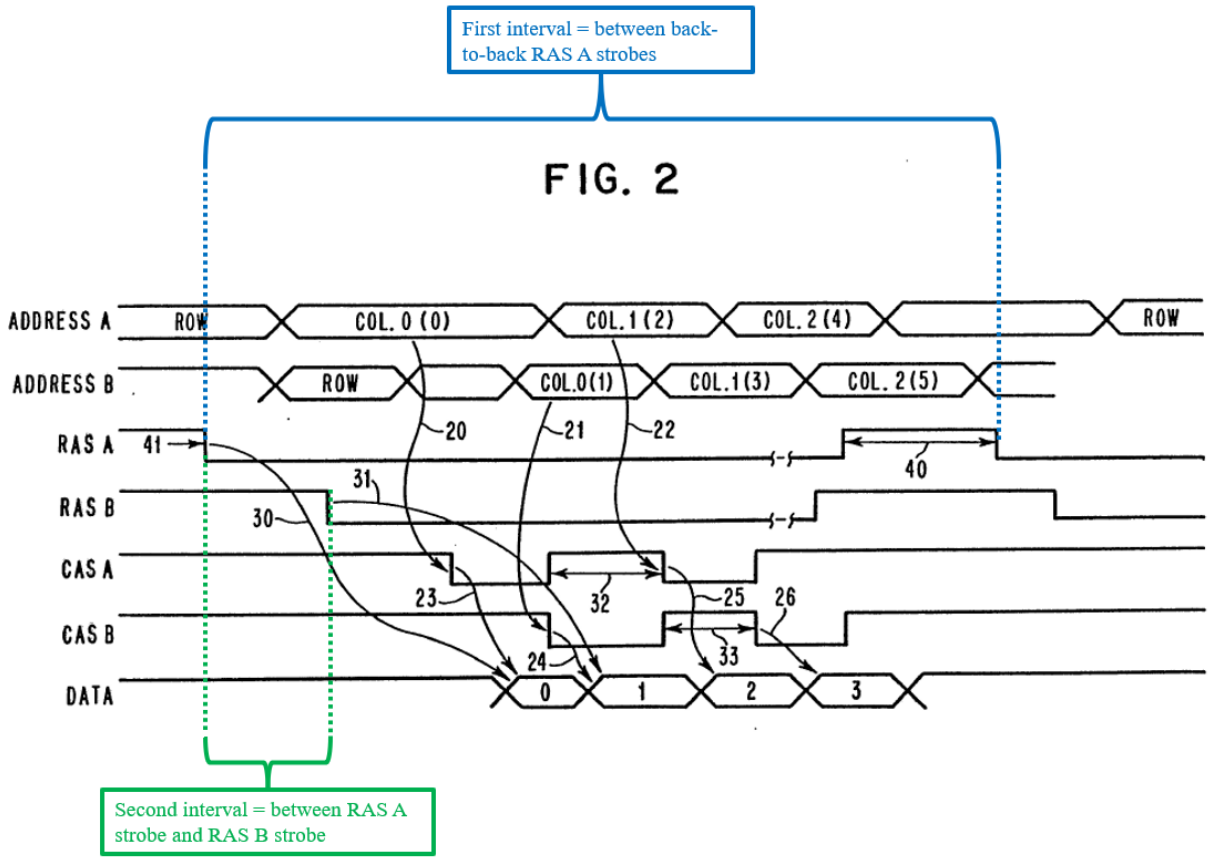
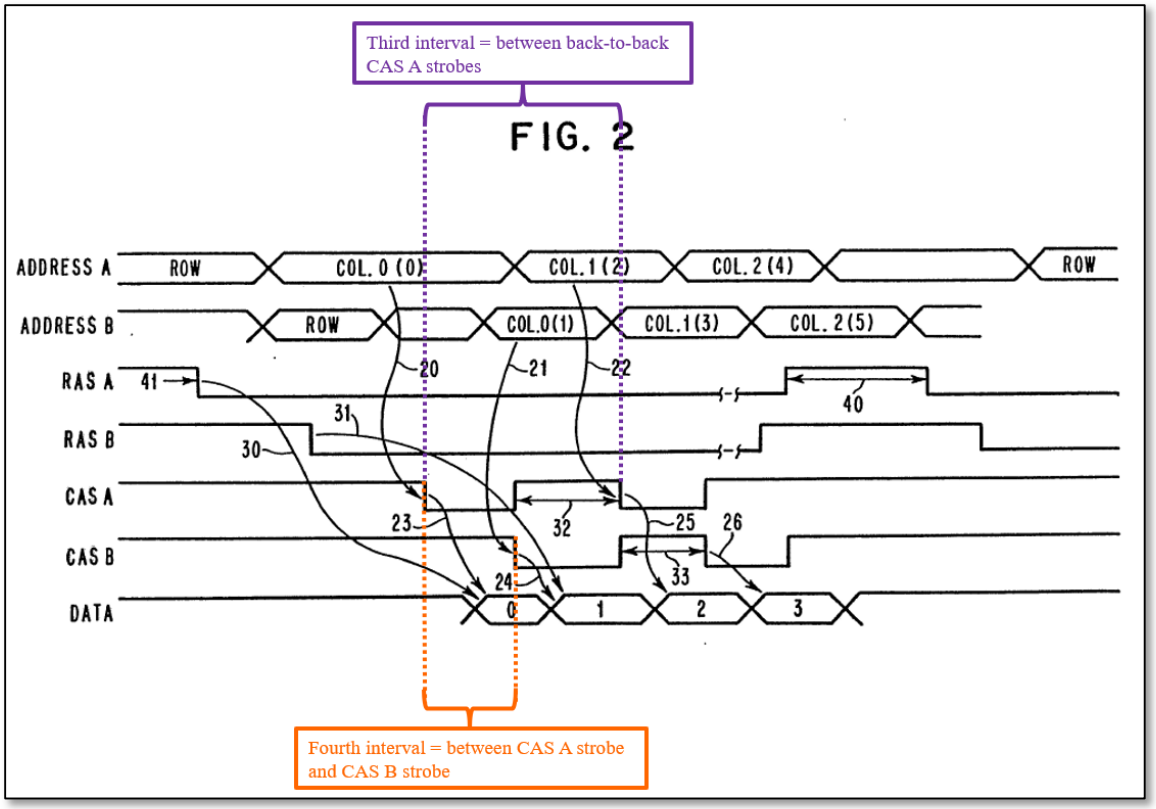


EX1007, Fig. 2 (annotated)

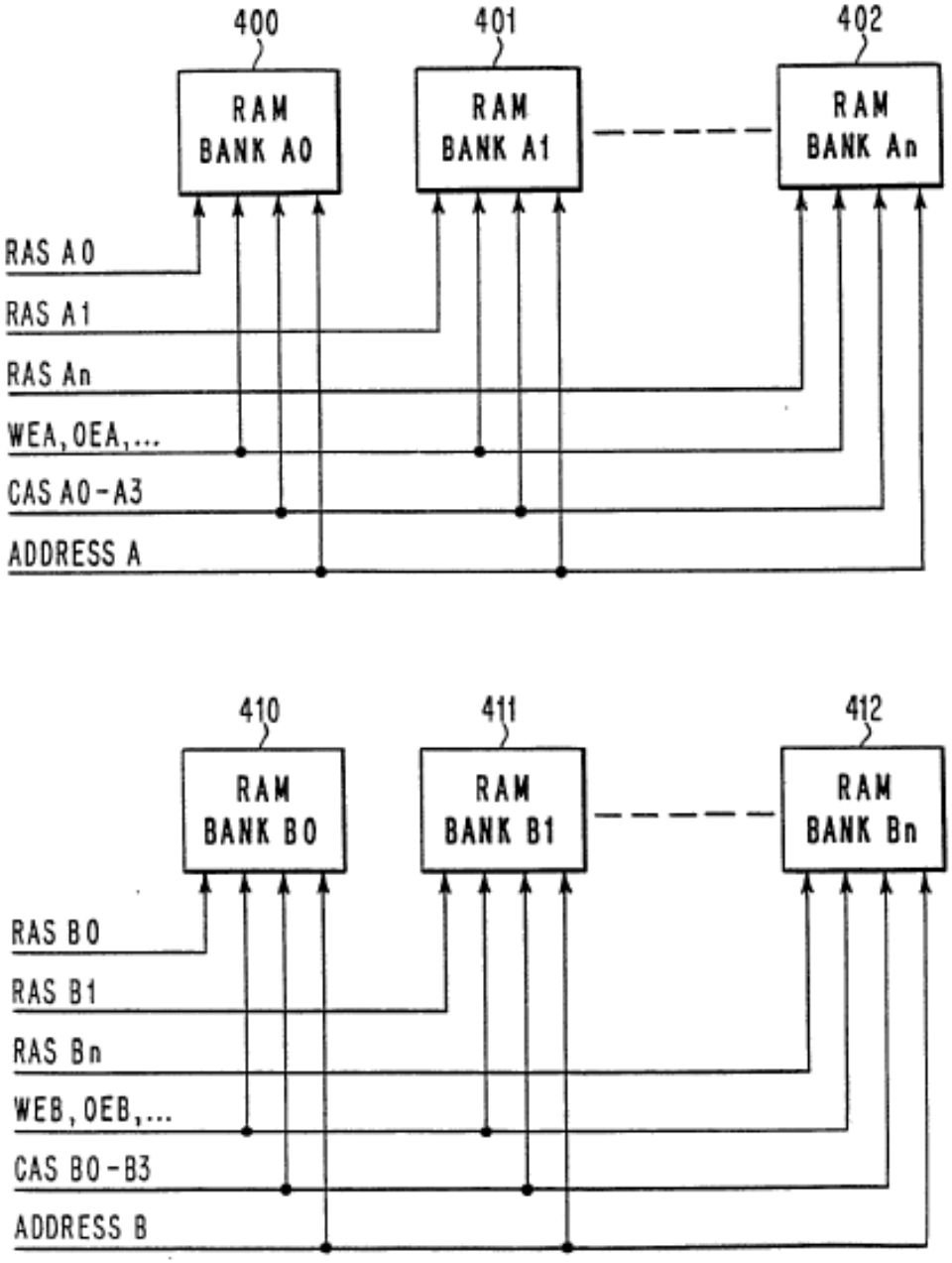
84. As shown by Figure 2, Bowater's memory controller issues back to back CAS A commands over an interval shown in annotated Figure 2 below. EX1007, 4:13-40, Fig. 2.



EX1007, Fig. 2 (annotated)

As shown by Figure 6 below, the CAS A commands are column accesses to columns within banks A0-An of the bank A group. EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6; *id.*, 7:2-3 ("Fig. 6 shows how control signals connect to banks of memory for two-way interleaving. These control signals are illustrated in Fig. 2"). Bowater's memory controller also issues CAS B commands which are columns accesses to columns within banks B0-Bn of the same bank B group. *Id.* Indeed, Bowater's process is for "two memory banks being interleaved"—bank A and bank B—where CAS A are commands sent to bank A and CAS B are commands sent to bank B. *Id.*

FIG. 6



EX1007, Fig. 6

85. Thus, as combined with LaBerge, such CAS A commands would have been applied to banks within a common bank group formed of memory devices 80a, 86a,

80b, and 86b in a **module 310a** (*bank group*) of LaBerge, while CAS B commands would have been applied to banks within another common bank group formed of memory devices 80a, 86a, 80b, and 86b in a **module 310b** (another *bank group*) of LaBerge. Section VIII.A.1.a (element [1a]) (explaining each of devices 80a, 86a, 80b, and 86b is a *bank*, and the collection of devices 80a, 86a, 80b, and 86b in each module 310 is a *bank group*); EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6. Such commands would have been applied by LaBerge's memory controller 200 "to the signal lines of bus 320 depending on which memory devices 80a, 86a, 80b or 86b [banks] are being accessed." EX1006, ¶0039.

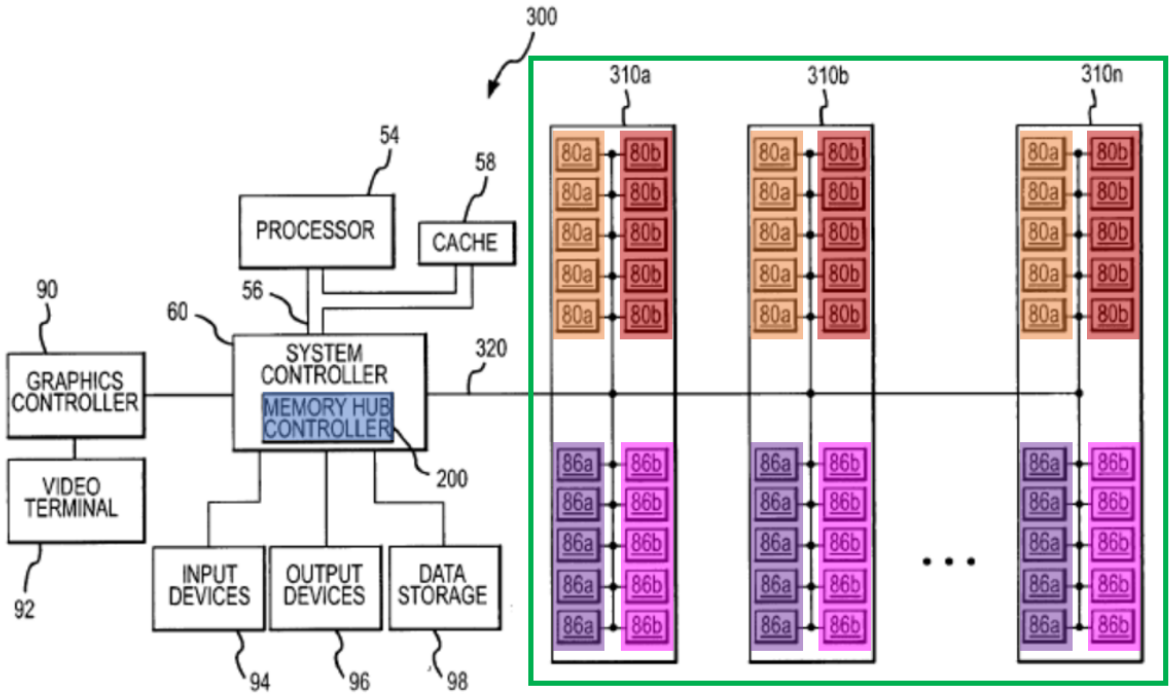


FIG.6

EX1006, Fig. 6 (annotated)

86. Thus, in the LaBerge-Bowater combined system, LaBerge's command scheduler 210 (*circuitry to schedule*) would have scheduled issuance of the RAS and CAS commands such that a third interval of clock transitions to transpire between back to back CAS A commands to banks within a common bank group formed of memory devices 80a, 86a, 80b, and 86b in **module 310a** is provided (*a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group*) and a fourth interval of clock transitions to transpire between back to back column activations to banks within different bank groups—i.e., column access using CAS A to memory devices 80a, 86a, 80b, and 86b in module 310a and a subsequent column access using CAS B to memory devices 80a, 86a, 80b, and 86b in **module 310b**—is provided (*a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups*) as shown by Figure 2 below. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6.

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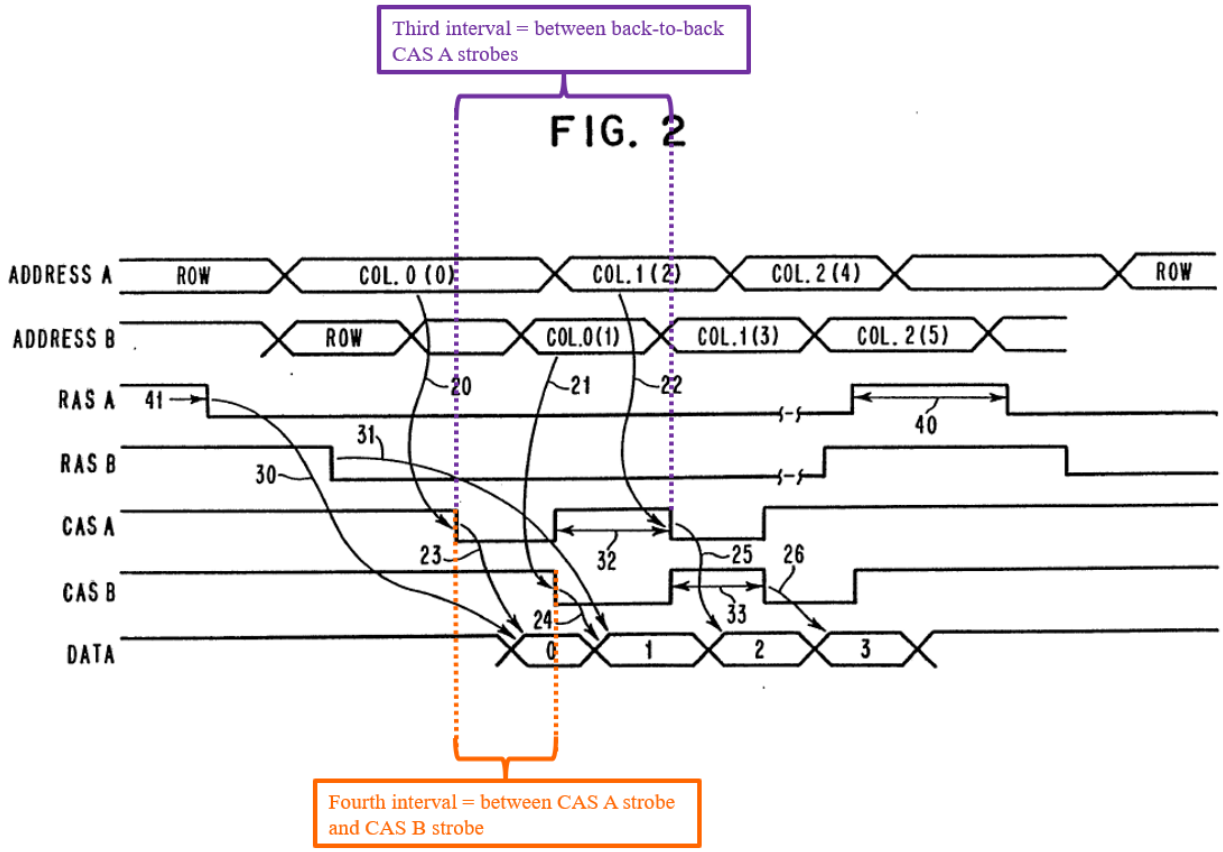
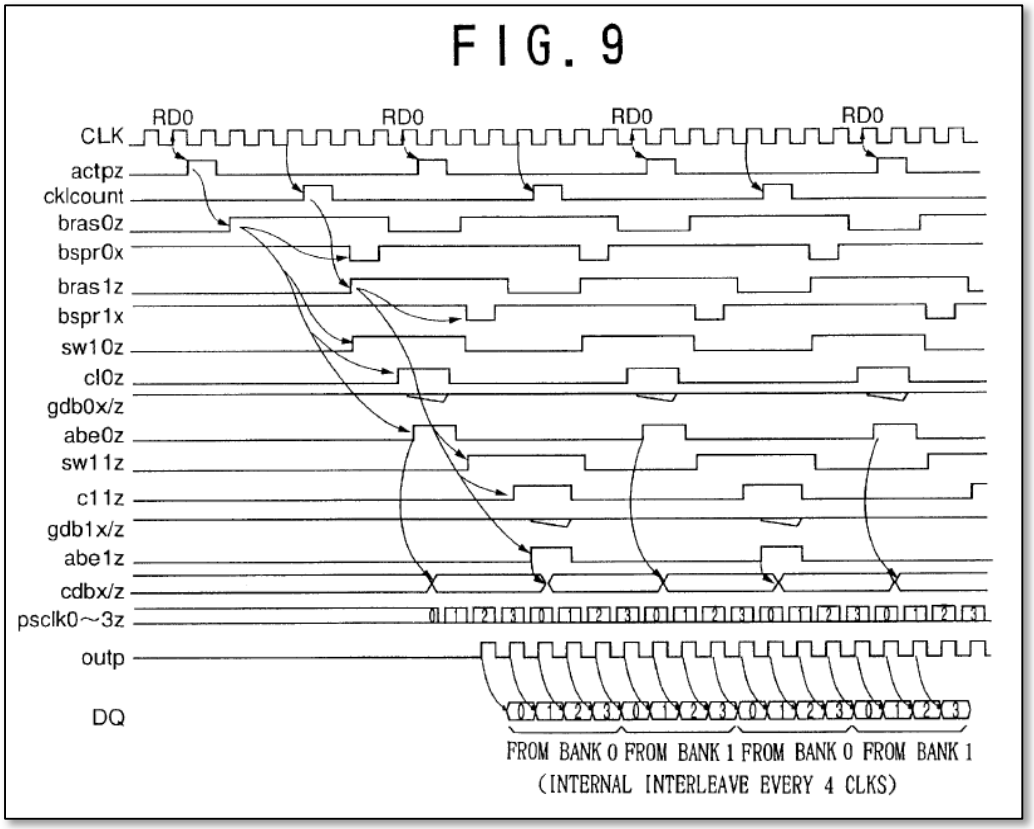


EX1007, Fig. 2 (annotated)

87. As shown by Figure 2, the third interval is *longer* than the fourth interval. *Id.* EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6. Moreover, a POSITA would have understood or at least found obvious that the claimed intervals are defined by "*clock transitions*" as claimed because LaBerge explicitly explains that timing of its CAS and RAS signals are defined by "periods of the clock CLK signal" and that "clock periods" define intervals between signals. EX1006, ¶¶0034-0039, Figs. 5, 6. Moreover, defining intervals in such a manner is well-known in the art. For example, Fujioka shows that clock signals ("CLK") have

clock transitions between low and high states, and Fujioka defines intervals between signals that are sent to banks, where transitions of CLK define intervals between when word line signal activations (signals "swl") are sent to banks, and also define intervals between when column activation signals (signals "cl") are sent to banks. EX1004, 6:35-42, 7:31-43, 8:45-50, 12:66-14:37, Fig. 9.



EX1004, Fig. 9

88. A POSITA would have been motivated to combine LaBerge and Bowater for the reasons discussed in Section VIII.A.1.e (element [1e]).

2. Claim 2: "*The memory controller of claim 1, wherein: each bank includes a first sub-bank and a second sub-bank; the first sub-bank is in a first bank group of the plurality of bank groups; and the second sub-bank is in a second bank group of the plurality of bank groups.*"

89. LaBerge and Bowater renders obvious claim 2. The group of memory devices 80a across the memory modules 310a, 310b…310n (*bank*) includes a first memory device 80a (*includes a first sub-bank*) located in memory module 310a and a second memory device 80a (*and a second sub-bank*) located in memory module 310b, as shown in annotated Figure 6 below. EX1006, ¶¶0034-0039, Fig. 6.

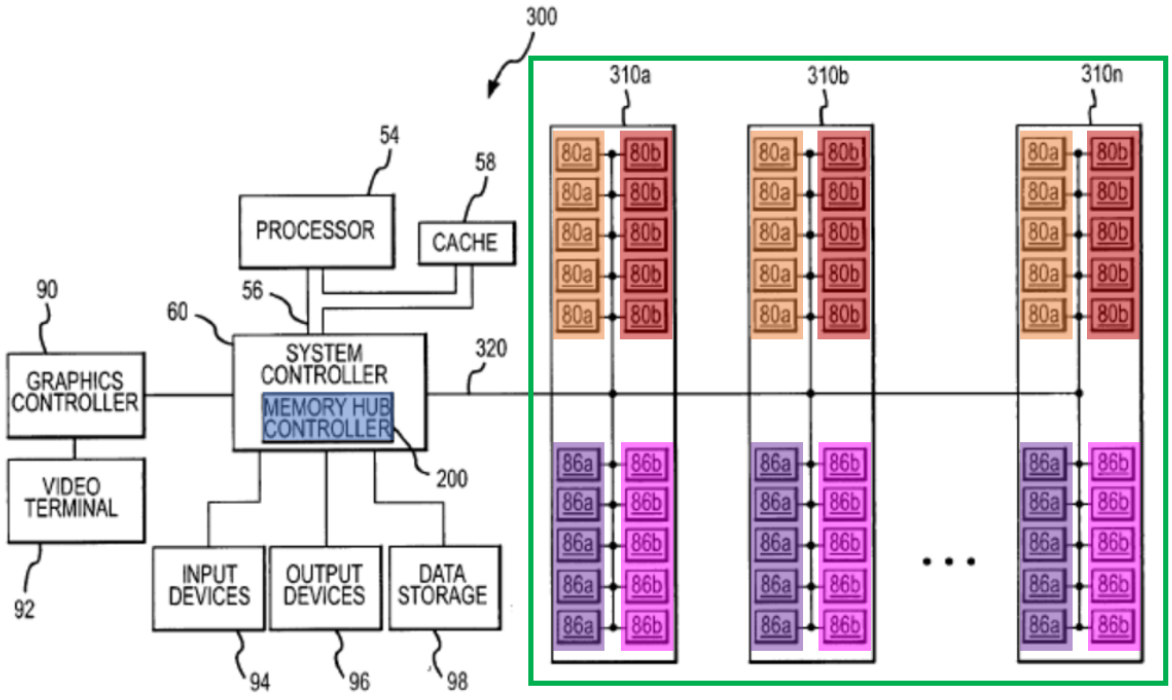


FIG.6

EX1006, Fig. 6 (annotated)

90. The same organization is true for each other group of memory devices 80b, 86a, and 86b, providing that *each bank includes a first sub-bank and a second sub-bank*. *Id.* Specifically, the group of memory devices 80b across the memory modules 310a, 310b…310n (*bank*) includes a first memory device 80b (*includes a first sub-bank*) located in memory module 310a and a second memory device 80b (*and a second sub-bank*) located in memory module 310b; the group of memory devices 86a across the memory modules 310a, 310b…310n (*bank*) includes a first memory device 86a (*includes a first sub-bank*) located in memory module 310a and a second memory device 86a (*and a second sub-bank*) located in memory module 310b; and the group of memory devices 86b across the memory modules 310a, 310b…310n (*bank*) includes a first memory device 86b (*includes a first sub-bank*) located in memory module 310a and a second memory device 86b (*and a second sub-bank*) located in memory module 310b. *Id.*

91. The first memory device 80a in memory module 310a (*first sub-bank*) is in a first group formed by memory devices 80a, 86a, 80b, and 86b in module 310a (*is in a first bank group*) out of the multiple groups formed by memory devices 80a, 86a, 80b, and 86b in modules 310a, 310b,…310n (*of the plurality of bank groups*), and the second memory device 80a in memory module 310b (*second sub-bank*) is in a second group formed by memory devices 80a, 86a, 80b, and 86b in module 310b (*is in a second bank group*) out of the multiple groups formed by memory devices 80a,

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86a, 80b, and 86b in modules 310a, 310b,…310n (*of the plurality of bank groups*), as shown in annotated Figure 6 below. EX1006, ¶¶0034-0039, Fig. 6.

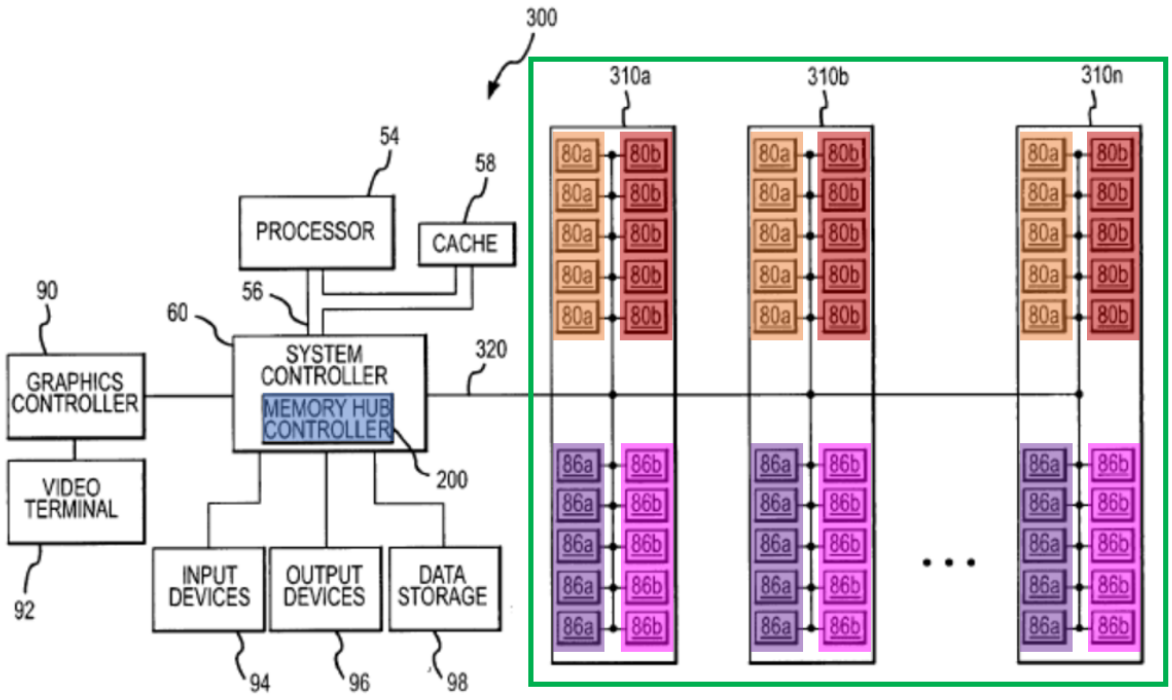

FIG.6

EX1006, Fig. 6 (annotated)

92. The same organization is true for each of memory devices 80b, 86a, and 86b. Thus, *the first sub-bank is in a first bank group of the plurality of bank groups; and the second sub-bank is in a second bank group of the plurality of bank groups*. *Id.*

3. Claim 4: "*The memory controller of claim 2, wherein the circuitry to schedule is to schedule at least one column access command for each row activation command, in order to access a column within a row activated by a corresponding row activation command, and wherein the command interface is to transmit bank address information to the memory device for*

> ***each row activation command and for each column access command, in order to select a bank and in order to select one of the bank groups in the plurality of bank groups.***"

93. LaBerge and Bowater render obvious claim 4. Command scheduler 210 (*circuitry to schedule*) schedules output of CASZ and RASZ DRAM commands. EX1006, ¶¶0034-0035, Figs. 5, 6. Table 1 of LaBerge shows that for memory devices 80a[2] and 86a, the signals sent by memory controller 200 and scheduled by command scheduler 210 include a CASZ signal, and respective RASZ signal. *Id.*, ¶¶0029-0030 (Table 1), 0034-0039, Figs. 5, 6.

TABLE 1

Hub Left Terminal Location	Hub Right Terminal Location	82a, 86a DDR2 CS_0	82b, 86b DDR2 CS_1	82a, 86a DDR3 CS_0	82b, 86b DDR3 CS_1
C_5	C_{27}	A_0	A_{10}	A_3	A_0
C_{11}	B_{21}	A_1	A_2	A_6	A_5
C_6	C_{26}	A_2	A_1	BA_3	BA_2
C_{12}	B_{20}	A_3	A_4	A_2	A_1
B_5	B_{27}	A_4	A_3	A_1	A_2
B_{11}	A_{21}	A_5	A_6	A_{12}	A_{13}
B_6	B_{26}	A_6	A_5	A_5	A_6
B_{12}	C_{19}	A_7	A_8	A_7	A_8
A_5	B_{29}	A_8	A_7	A_8	A_7
A_{13}	A_{19}	A_9	A_{11}	A_9	A_{11}
D_{12}	C_{21}	A_{10}	A_0	BA_2	BA_3
A_4	A_{29}	A_{11}	A_9	A_{11}	A_9
A_{12}	A_{20}	A_{12}	A_{13}	A_4	A_{14}
A_6	A_{27}	A_{13}	A_{12}	A_{13}	A_{12}
A_{11}	A_{22}	A_{14}	A_{15}	A_{15}	A_{15}

[2] I note that Table 1 lists a memory device "82"; this appears to be a typo and should apparently be "80" instead. Laberge elsewhere refers to 82 as a bus, and 80 as a memory device. EX1006, ¶¶0023-0030.

TABLE 1-continued

Hub Left Terminal Location	Hub Right Terminal Location	82a, 86a DDR2 CS_0	82b, 86b DDR2 CS_1	82a, 86a DDR3 CS_0	82b, 86b DDR3 CS_1
A_7	A_{28}	A_{15}	A_{14}	A_{14}	A_4
A_{10}	A_{23}	A_{16}	A_{16}	A_{16}	A_{16}
D_7	D_{27}	BA_0	BA_0	BA_1	BA_0
E_{13}	D_{20}	BA_1	CASZ	A_{10}	WEZ
E_7	E_{25}	BA_2	BA_2	CSZ_1	CSZ_1
F_{12}	F_{22}	BA_3	BA_3	ODT_1	ODT_1
D_8	D_{26}	CASZ	BA_1	CASZ	RASZ
D_6	D_{28}	CSZ_0	CSZ_0	WEZ	A_{10}
D_{11}	D_{21}	CSZ_1	CSZ_1	BA_0	BA_1
C_9	E_{28}	ODT_0	ODT_0	ODT_0	ODT_0
D_{13}	C_{20}	ODT_1	ODT_1	A_0	A_3
F_9	E_{22}	RASZ	WEZ	CSZ_0	CSZ_0
E_{10}	D_{22}	WEZ	RASZ	RASZ	CASZ

94. Thus, command scheduler 210 (*circuitry to schedule*) schedules output of a CASZ signal as well as output of an associated RASZ signal for the same memory devices (*is to schedule at least one column access command for each row activation command*). Moreover, a POSITA would have understood or at least found obvious that such an output of CASZ and RASZ signals is *in order to access a column within a row activated by a corresponding row activation command*. This is because the reason why a RASZ ("row address strobe") signal and CASZ ("column address strobe") signal are transmitted to a memory device is to access the information stored within the column, specified by the CASZ signal, of the row activated by the RASZ signal. EX1006, ¶¶0029, 0034-0036. For example, Dye explains that a DRAM can receive "inputs," including "Row Address Strobe" and "Column Address Strobe," and "controls the access to specified row and column addresses in the array." EX1014 (Dye), 2:41-54; *id.*, 3:39-46 (noting "control signals" include "e.g., CAS, RAS…").

95. Command shifter 214, multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242 (*the command interface*) transmits, using ring buffers 204 and 242, "command and address signals" that include bank addresses BA0-BA3 and chip select signals CSZ0 and CSZ1 that relate to associated CASZ column access strobe and RASZ row address strobe signals, to memory devices 80a, 86a, 80b, or 86b of memory modules 310 (*is to transmit bank address information to the memory device for each row activation command and for each column access command*). EX1006, ¶¶0034-0039, Figs. 5, 6; Section VIII.A.1.c (element [1c]). The bank addresses BA0-BA3 and chip select signals CSZ0 and CSZ1 are part of each command of the CASZ column access strobe and RASZ row address strobe signals because they inform the bank address and associated memory device (either an "a" device or "b" device) for each CASZ and RASZ command. *Id.*

96. The outputting of bank addresses BA0-BA3 is to select a bank since this value indicates the address for the bank that is subject to a read or write command (*in order to select a bank*) and the outputting of chip select signals CSZ0 and CSZ1 is to select either the group of devices 80a and 86a on the "first surface 100a" of a memory module or the group of devices 80b and 86b on the "second surface 100b" of a memory module (*and in order to select one of the bank groups in the plurality of bank groups*). EX1006, ¶¶0025-0026, 0029-0030, 0034-0039, Figs. 5, 6.

4. Claim 9: "*The memory controller of claim 1, wherein the memory controller is to interleave row activation commands*

> ***and is to interleave column access commands for back-to-back data accesses in different bank groups, and is to transmit bank address information as part of each command of the row activation commands and column access commands, to select a bank group of the plurality of bank groups, and to select a bank within the selected bank group.*"**

97. LaBerge and Bowater render obvious claim 9. Multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242 of memory controller 200 transmits, using ring buffers 240 and 242, "command and address signals" that include bank addresses BA0-BA3 and chip select signals CSZ0 and CSZ1 that relate to associated CASZ column access strobe and RASZ row address strobe signals, to memory devices 80a, 86a, 80b, or 86b of memory modules 310 (EX1006, ¶¶0034-0039, Figs. 5, 6; Section VIII.A.1.c (element [1c])), where the bank addresses BA0-BA3 and chip select signals CSZ0 and CSZ1 are part of each command of the CASZ column access strobe and RASZ row address strobe signals because they inform the bank address and associated memory device (either an "a" device or "b" device) for each CASZ and RASZ command (*the memory controller is to… transmit bank address information as part of each command of the row activation commands and column access commands*). *Id*. The outputting of chip select signals CSZ0 and CSZ1 is to select either the group of devices 80a and 86a on the "first surface 100a" of a memory module or the group of devices 80b and 86b on the "second surface 100b" of a memory module (*to select a bank group of the plurality of bank groups*) and the outputting of bank addresses BA0-BA3 is to select a bank since this value indicates

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the address for the bank that is subject to a read or write command (*and to select a bank within the selected bank group*). EX1006, ¶¶0025-0026, 0029-0030, 0034-0039, Figs. 5, 6.

98. In the LaBerge-Bowater combination, a POSITA would have understood or at least found obvious that LaBerge's memory controller 200 would have interleaved the RAS A commands and RAS B commands, and the CAS A commands and CAS B commands as taught by Bowater (*wherein the memory controller is to interleave row activation commands and is to interleave column access commands*) for back to back data accesses from rows in different bank groups—i.e., row activation using RAS A to memory devices 80a, 86a, 80b, and 86b in module 310a and a subsequent row activation using RAS B to memory devices 80a, 86a, 80b, and 86b in module 310b—and back to back data accesses from columns in different bank groups—i.e., column access using CAS A to memory devices 80a, 86a, 80b, and 86b in module 310a and a subsequent column access using CAS B to memory devices 80a, 86a, 80b, and 86b in module 310b (*for back-to-back data accesses in different bank groups*). Section VIII.A.1.e-f. This is at least because Bowater teaches, with reference to Figure 6, that "control signals" RAS A, RAS B, CAS A, and CAS B (shown in Figure 2) "connect to banks of memory for two-way interleaving." EX1007, 4:25-40, 6:47-50, 7:1-13, Figs. 2, 6.

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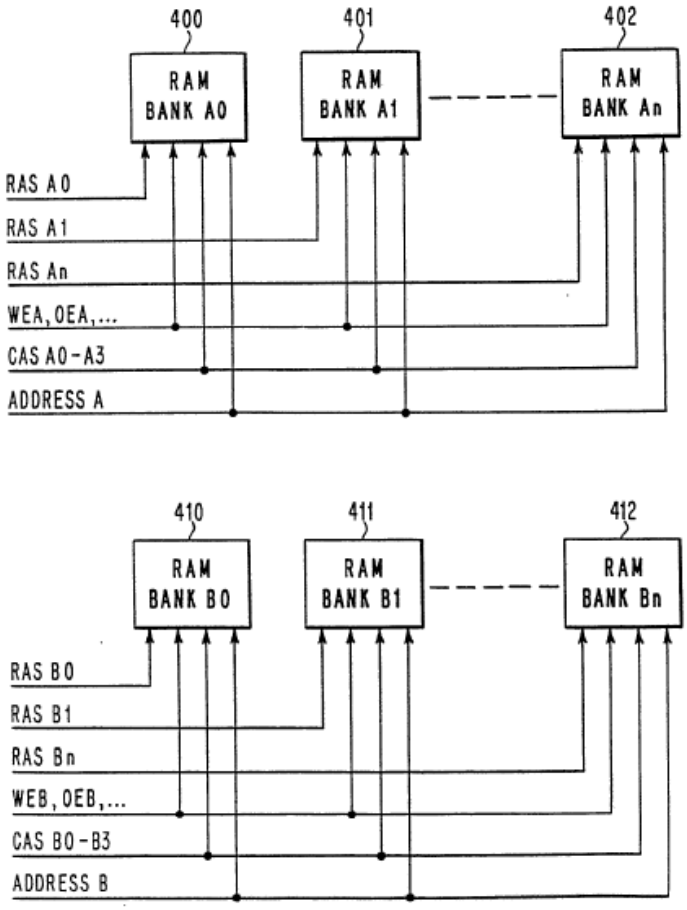
FIG. 6



Bowater, Fig. 6

99. A POSITA would have been motivated to combine LaBerge and Bowater in this manner for the reasons discussed in Section VIII.A.1.e. Indeed, the combination would have enhanced LaBerge's system by providing a technique by which RAS and CAS commands are handled and would have been nothing more than a design choice implemented by a POSITA. Such a combination would have been routine and straightforward to POSITAs and would have provided benefits including an increase in memory bandwidth and reduction of latency. Indeed, Bowater explains that such

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interleaving of RAS and CAS commands to memory banks provides "faster access to a contiguous chunk of memory because access to the banks can be overlapped" and that "page size is effectively doubled because there is an active row in both banks." EX1007, 6:47-50, 7:1-13. A POSITA would have further combined LaBerge and Bowater, and had a reasonable expectation of success in doing so, for the same reasons as discussed in Section VIII.A.1.e.

5. Claim 10: *"The memory controller of claim 1, wherein: the first interval is longer than the third interval and the second interval is longer than the fourth interval."*

100. LaBerge and Bowater renders obvious claim 10. LaBerge and Bowater describe the interval between back-to-back high to low changes of the signal "RAS A" (*first interval*) that is longer than the interval between back-to-back high to low changes of the signal "CAS A" (*is longer than the third interval*), and the interval between back-to-back low to high changes of the signal "RAS A" and the signal "RAS B" (*and the second interval*) that is longer than the interval between back-to-back low to high changes of the signal "CAS A" and the signal "CAS B" (*is longer than the fourth interval*). Sections VIII.A.1.e-f (elements [1e]-[1f]).

6. Claim 20

a. [20a] "*A method of operation in a memory controller, the memory controller to control a memory device, the memory device having a plurality of bank groups, the method comprising*"

101. *See* Section VIII.A.1.a.

b. [20b] "*providing a clock signal to the memory device, the clock signal having clock transitions;*"

102. *See* Section VIII.A.1.b.

c. [20c] "*transmitting to the memory device, via a command interface, row activation commands to instruct row activations and column access commands to instruct column accesses; and*"

103. *See* Section VIII.A.1.c.

d. [20d] "*scheduling issuance of the row activation commands and the column access commands from the command interface, such that*"

104. *See* Section VIII.A.1.d.

e. [20e] "*a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common bank group, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups, and*"

105. *See* Section VIII.A.1.e.

f. [20f] "*a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups*."

106. *See* Section VIII.A.1.f.

7. Claim 22: "*The method of claim 20, wherein: the method further comprises transmitting bank address information as*

part of each command of the row activation commands and column access commands, to communicate selection of a bank group of the plurality of bank groups, and to communicate selection of a bank within the selected bank group."

107. *See* Section VIII.A.3 (claim 4).

B. Ground II: LaBerge, Bowater, and Suh render claims 3 and 21 obvious

1. Claim 3: ""*The memory controller of claim 2, wherein: each sub-bank in the first bank group shares first row decoder circuitry and first column decoder circuitry with each other sub-bank in the first bank group; and each sub-bank in the second bank group shares second row decoder circuitry and second column decoder circuitry with each other sub-bank in the second bank group.*"

108. LaBerge, Bowater, and Suh render obvious claim 3. Suh describes that each of bank 0, bank 1, bank 2, and bank 3 (each a *bank*) includes eight respective bank sections (*sub-banks*), each labeled as "bank 0," "bank 1," "bank 2," and "bank 3," distributed in the cell arrays of Figure 2. EX1005, 3:20-38, Fig. 2; Suh also describes a first cell array (*first bank group*) and a second cell array (*second bank group*). *Id.*

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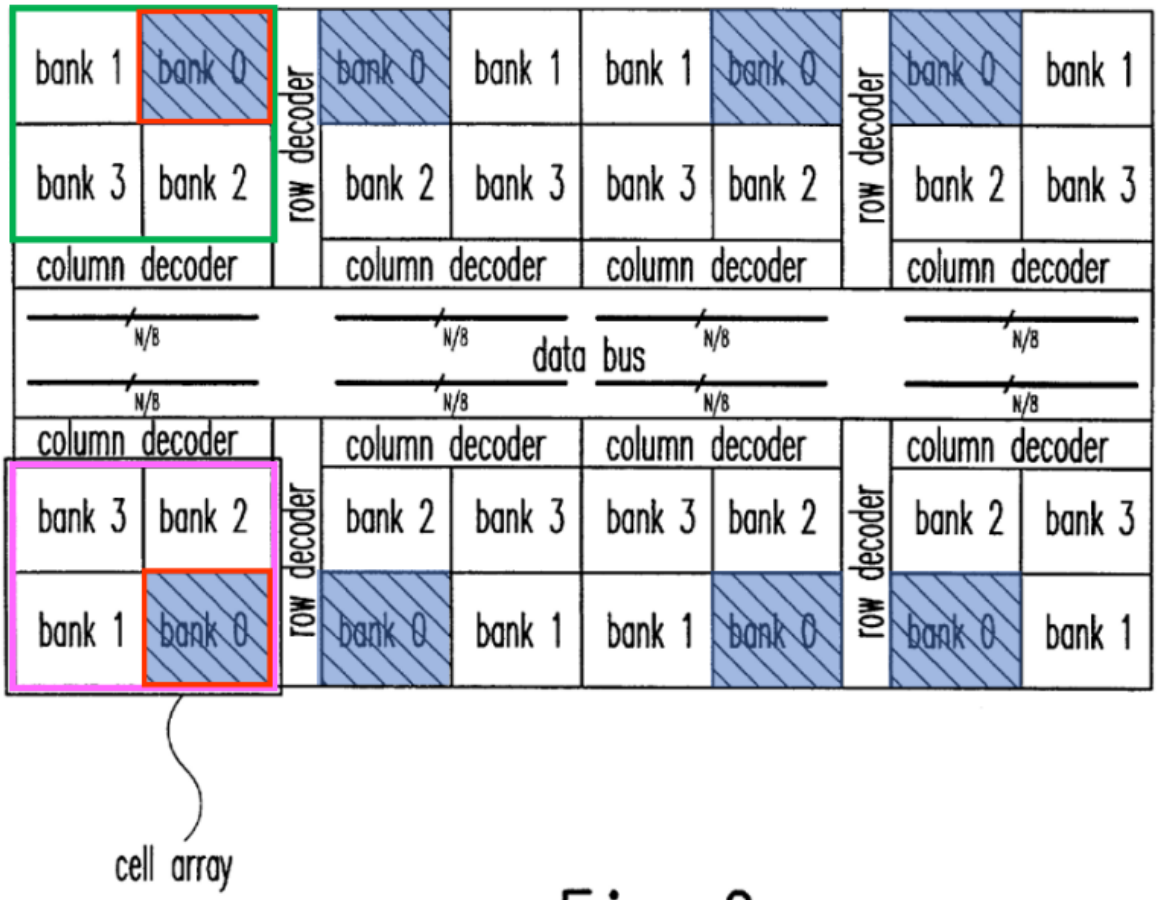

Fig. 2

Suh, Figure 2 (annotated)

109. Suh further describes "a column decoder is connected to each of the cell arrays, and a row decoder is positioned between the two cell arrays in each of the cell array blocks and connected in common to them." EX1005, 3:28-31, Fig. 2.

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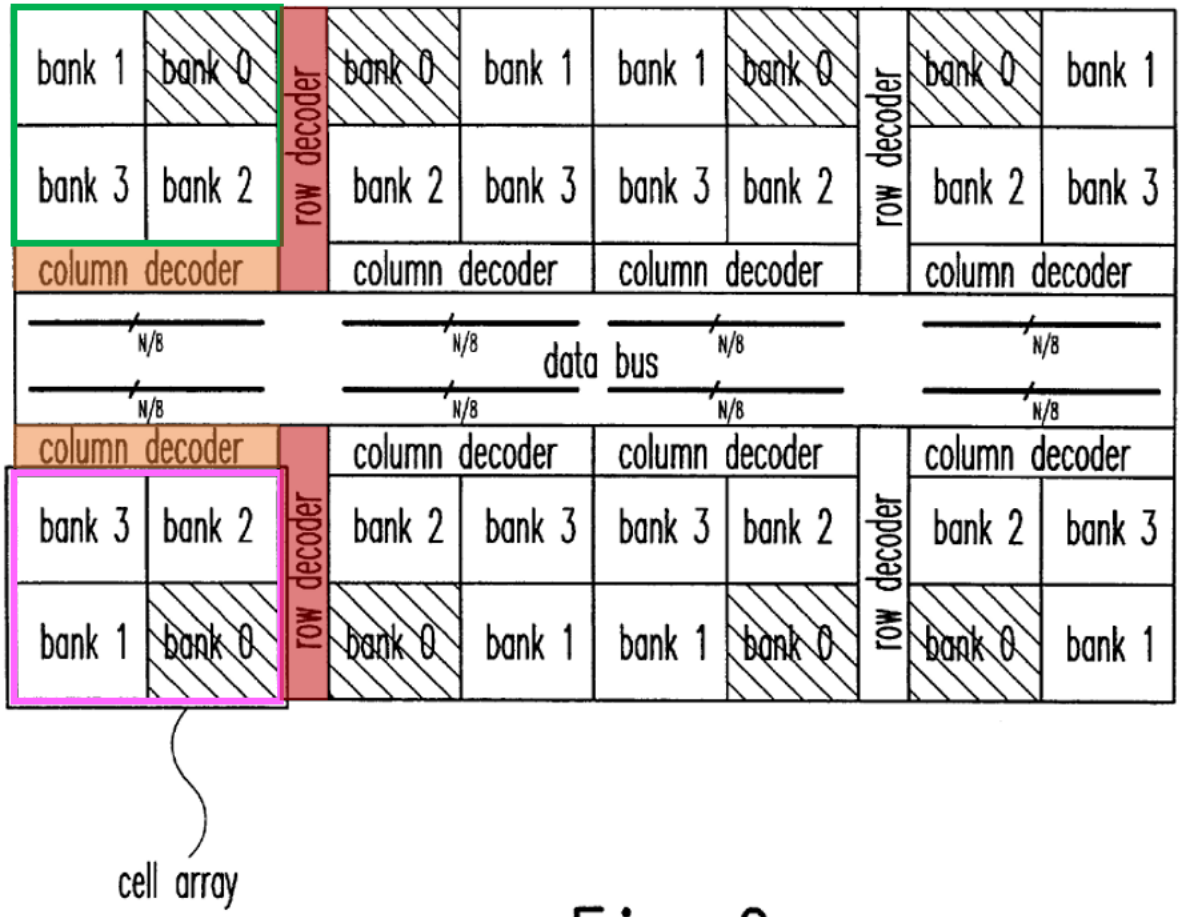

Fig. 2

Suh, Figure 2 (annotated)

110. As shown by Figure 2, each of Suh's bank sections (*each sub-bank*) in the first cell array (*in the first bank group*) shares a row decoder (*shares first row decoder circuitry*) and a column decoder with each other bank section in the first cell array (*and first column decoder circuitry with each other sub-bank in the first bank group*). EX1005, 3:28-31, Fig. 2. And each of Suh's bank sections (*each sub-bank*) in the second cell array (*in the second bank group*) shares a second row decoder (*shares second row decoder circuitry*) and a second column decoder with each other bank

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section in the second cell array (*and second column decoder circuitry with each other sub-bank in the second bank group*). *Id.*

Motivation to Combine

111. A POSITA would have been motivated to combine LaBerge and Bowater as discussed in Section VIII.A.1.e (element [e]). A POSITA would have been further motivated to combine the LaBerge-Bowater combined system with Suh such that LaBerge's memory devices 80a, 86a, 80b, and 86b that each form a respective memory bank (*bank*) would have been organized into cell arrays and bank sections and have bank sections that share a row decoder and column decoder, as taught by Suh. The combination would have enhanced the LaBerge-Bowater system, providing the more efficient grouping of memory cells, improved operation speed, and a reduction in chip area used by the memory. EX1005, 1:10-15, 1:28-30, 1:65-2:6, 5:41-48.

112. Combined, LaBerge's memory devices 80a, 86a, 80b, and 86b within the LaBerge-Bowater system would have taken advantage of Suh's cell array and bank section layout, with each bank section in a particular group sharing a row decoder and column decoder. LaBerge already describes that memory devices 80a, 86a, 80b, and 86b store data at locations indicated by row and column addresses. EX1006, ¶¶0034-0039, Figs. 5, 6. Suh, applicable to the LaBerge-Bowater system in that it is similarly directed to memory devices organizing data storage by row and column

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addresses, teaches the organization of such memory cells to improve access speed and chip layout. Suh, 1:10-15, 1:28-30, 1:65-2:6, 5:41-48. Enhancing the LaBerge-Bowater system with Suh would have improved the system, and furthered LaBerge's goals of addressing difficulties in prior systems such as, e.g., improperly using "area that could be used for the integrated circuit itself." EX1006, ¶0011.

113. A POSITA would have combined LaBerge-Bowater and Suh as above using known hardware and software techniques associated with memory devices, and for the same reasons discussed above, a POSITA would have combined Suh's teachings with the LaBerge-Bowater system. Separate or combined, the LaBerge-Bowater and Suh systems would have both performed the same memory and data storage functionality. The combination would have further been predictable, straightforward, and routine for a POSITA. A POSITA would have had a reasonable expectation of success in making this combination for the same reasons discussed above, and also due to the similarities of both references, where the references are at least directed to memory devices that aim to increase efficiencies. EX1006, ¶¶0011-0013; EX1005, 1:10-15, 1:28-30, 1:65-2:6, 5:41-48.

114. Additionally, Suh is analogous art to the '379 patent, from the same field of endeavor as the patent (e.g., memory systems) and pertinent to the particular problem the patent was trying to solve (e.g., how to improve memory performance). EX1001, Abstract, 1:28-29, 4:1-20; EX1005, Abstract, 1:8-16, 1:64-2:6.

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2. Claim 21: *"The method of claim 20, wherein: each bank includes a first sub-bank and a second sub-bank; the first sub-bank is in a first bank group of the plurality of bank groups; the second sub-bank is in a second bank group of the plurality of bank groups; each sub-bank in the first bank group shares row decoder circuitry and column decoder circuitry with each other sub-bank in the first bank group; and each sub-bank in the second bank group shares row decoder circuitry and column decoder circuitry with each other sub-bank in the second bank group."*

115. *See* Section VIII.A.2 (claim 2) and VIII.B.1 (claim 3).

C. Ground III: LaBerge, Bowater, and Halbert render claim 5 obvious

1. Claim 5: "*The memory controller of claim 2, wherein the circuitry to schedule is to schedule for a given row activation command, at least two column access commands, in order to access different columns within a row activated by the given row activation command*."

116. LaBerge's command scheduler 210 (*circuitry to schedule*) schedules issuance of the RASZ and CASZ signals, where for example, "Command Scheduler 210 might schedule[] the CASZ to be output three clock periods after the RASZ signals [were] [] output from the Command Scheduler 210" (*for a given row activation command, a column access command*). EX1006, ¶¶0034-0039, Figs. 5, 6. Halbert describes "two consecutive read operations (to the same ROW of the memory devices)," where a controller "latches an active command in RCMD," commanding a row activation, and a "READ command (to COL a) is clocked in, causing the controller to enter a read state," and "a second READ command (to COL b) is clocked in," providing two commands to access columns a and b, which are different

columns within the same row of memory that has been activated by the active command (*at least two column access commands, in order to access different columns within a row activated by the given row activation command*). EX1008 (Halbert), 5:58-6:6; *id.*, 2:36-50, Fig. 3 (a READ from "columns [] on the same ROW"). In the combination, LaBerge's command scheduler 210 would have scheduled its commands as taught by Halbert to access different columns within a row as claimed (*circuitry to schedule is to schedule for a given row activation command, at least two column access commands, in order to access different columns within a row activated by the given row activation command*.).

Motivation to Combine

117. A POSITA would have been motivated to combine LaBerge and Bowater for the reasons discussed in Section VIII.A.1.e (element [1e]). A POSITA would have been motivated to combine the LaBerge-Bowater combined system with Halbert such that LaBerge's command scheduler 210 would have scheduled its commands as taught by Halbert. The combination would have enhanced the LaBerge-Bowater combined system, providing more efficient accessing to data.

118. Combined, the LaBerge-Bowater combined system would have taken advantage of Halbert's data access techniques. The LaBerge-Bowater combined system already describes scheduling column access of an activated row using CAS and RAS commands. EX1006, ¶¶0034-0039, Figs. 5, 6. Halbert, applicable to the

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LaBerge-Bowater combined system in that it is similarly directed to DRAM memory devices, teaches accessing multiple columns of a row when the row is activated. EX1008, 2:36-50, 5:58-6:6, Fig. 3. Enhancing the LaBerge-Bowater combined system with Halbert would have provided that the LaBerge-Bowater combined system can schedule multiple column accesses for a given row activation. *Id.* This would have been straightforward and well within the capabilities of a POSITA as it would have been simply increasing the number of CAS commands in relation to a single RAS command. *Id.*

119. A POSITA would have combined the LaBerge-Bowater combined system with Halbert as above using known hardware and software techniques associated with memory devices, and for the same reasons discussed above, a POSITA would have combined the teachings. And separate or combined, the LaBerge-Bowater combined system and Halbert system would have both performed the same memory and data storage functionality. The combination would have further been predictable, straightforward, and routine for a POSITA. And a POSITA would have had a reasonable expectation of success in making this combination for the same reasons discussed above, and also due to the similarities of both references, where both references are at least directed to memory devices that operate using column access commands and row activation commands. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 3:35-46, 4:15-25, Fig. 2; EX1008, 5:58-6:6; 2:36-50, Fig. 3.

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120. Additionally, Halbert is analogous art to the '379 patent, from the same field of endeavor as the patent (e.g., memory systems) and pertinent to the particular problem the patent was trying to solve (e.g., how to improve memory performance). EX1001, Abstract, 1:28-29, 4:1-20; EX1008, 5:58-6:6; 2:36-50, Fig. 3.

D. Ground IV: LaBerge, Bowater, and Grundy render claims 6 and 7 obvious

1. Claim 6: "*The memory controller of claim 1, wherein the memory controller also comprises a data interface to exchange data with the memory device via links, using respective, mutually-exclusive subsets of the links to exchange data in association with the back-to-back column accesses to banks within different bank groups*."

121. The LaBerge-Bowater combination describes the claimed *memory controller*, *memory device*, and *column access commands* as explained for claim 1. Sections VIII.A.1.a-c (elements [1a]-[1c]). LaBerge also describes *the back-to-back column accesses to banks within different bank groups*. Section VIII.A.1.f (element [1f]).

122. Grundy describes a "memory controller 151" coupled to a collective memory device formed by memory devices 155sub1 through 155sub8; the memory controller has inputs and outputs connecting it to memory devices 155sub1 and 155sub8 via "N multi-purpose lines 158" of "point-to-point signaling links 153" that allow for the sending and receiving of "N-bit wide data values" to and from the collective memory device (*the memory controller also comprises a data interface to exchange data with the memory device via links*), with one subset of links 153 used to send

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data values to memory device 155sub1 of the collective device and another subset of links 153 used to receive data values from memory device 155sub8 of the collective device, as shown in Figure 5A (*using respective, mutually-exclusive subsets of the links to exchange data*). EX1010, ¶¶0043-0044, Fig. 5A; *id.*, ¶0036, Fig. 3 (memory controller having a "memory interface" connecting the controller to memory devices).

123. And the LaBerge-Bowater-Grundy combined system would have provided that such sending and receiving of data values (i.e., *exchange [of] data*) would have occurred "*in association with the back-to-back column accesses to banks within different bank groups*" because LaBerge's column access using CAS A to memory devices 80a, 86a, 80b, and 86b in module 310a and subsequent column access using CAS B to memory devices 80a, 86a, 80b, and 86b in module 310b are used when sending data to and receiving data from a memory device during write and read functions. EX1006, ¶¶0034-0039, Figs. 5, 6; Sections VIII.A.1.c, f (elements [1c], [1f]); EX1010, ¶¶0043-0044, Fig. 5A.

124. If *a data interface to exchange data…* is interpreted as a means-plus-function term, then LaBerge-Bowater-Grundy discloses or at least renders obvious (1) the identified function for the same reasons discussed, and (2) the identified structure (Section V.B, *supra*) as discussed above.

2. Claim 7: "*The memory controller of claim 1, wherein: the memory controller further comprises a data interface to*

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> ***exchange data with the memory device via links, in association with each column access command; and the memory controller further comprises serialization/deserialization circuitry to exchange serialized data with the memory device over each of the links in association with each column access command.*"**

125. The LaBerge-Bowater combination describes the claimed *memory controller*, *memory device*, and *column access commands*. Sections VIII.A.1.a-c (elements [1a]-[1c]). Multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242 transmit to memory devices 80 and 86 of memory modules 310a-310n (*transmit, to the memory device*) CASZ signals that instruct the memory devices to allow access to desired memory columns (*column access commands to instruct column accesses*). EX1006, ¶¶0003, 0029, 0034-0039, Figs. 5, 6; Section VIII.A.1.c (element [1c]).

126. Grundy describes a *memory controller further comprises a data interface to exchange data with the memory device via links.* Section VIII.D.1 (claim 6). The LaBerge-Bowater-Grundy combined system would have provided that such sending and receiving of data values (i.e., *exchange [of] data*) would have occurred "*in association with each column access command*" because LaBerge's CASZ signals that instruct the memory devices to allow access to desired memory columns are used when sending data to and receiving data from a memory device during write and read functions. EX1006, ¶¶0034-0039, Figs. 5, 6; Section VIII.A.1.c (element [1c]); EX1010*,* ¶¶0043-0044, Fig. 5A.

127. Grundy further describes a memory controller 151 (1) has a "serializer circuit" at its output "to serialize an N-bit transmission," thereby serializing data that is sent via the "N multi-purpose lines 158" of each of links 153 to the memory device formed devices 155sub1 through 155sub8, and (2) has a "deserializer circuit" to "deserialize the N-bit transmission," thereby de-serializing data that is received via the "N multi-purpose lines 158" of each of the links 153 from the memory device formed by devices 155sub1 through 155sub8 (*and the memory controller further comprises serialization/deserialization circuitry to exchange serialized data with the memory device over each of the links*). EX1010, ¶¶0043-0044, 0051-0052, Fig. 5A.

128. The LaBerge-Bowater-Grundy combined system would have provided that such sending and receiving of serialized data values (i.e., *exchange [of] serialized data*) would have occurred "*in association with each column access command*" because LaBerge's CASZ signals that instruct the memory devices to allow access to desired memory columns are used when sending data to and receiving data from a memory device during write and read functions. EX1006, ¶¶0034-0039, Figs. 5, 6; Section VIII.A.1.c (element [1c]); EX1010, ¶¶*00*43-0044, Fig. 5A.

129. If *data interface to exchange data with the memory device* is interpreted as a means-plus-function term, see analysis in Section VIII.D.1. If *serialization/deserialization circuitry to exchange serialized data* is interpreted as a means-plus-function term, LaBerge-Bowater-Grundy's discloses or at least renders

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obvious (1) the identified function for the same reasons discussed, and (2) the identified structure of memory controller hardware and equivalents thereof (Section V.A) for the reasons above.

3. Motivation to Combine

130. A POSITA would have been motivated to combine LaBerge and Bowater for the reasons discussed in Section VIII.A.1.e (element [1e]). A POSITA would have been motivated to combine the LaBerge-Bowater system with Grundy such that LaBerge's memory hub controller 200 (Section VIII.A.1.a-b) is enhanced by Grundy's teachings of (1) the inputs/outputs of memory controller 151 and connect to memory using N multi-purpose lines 158 of point-to-point signaling links 153 that allow for sending and receiving N-bit wide data values to and from the memory device, and (2) a serializer circuit and a deserializer circuit. Section VIII.D.1-2 (claims 6, 7). The combination would have merely provided techniques by which LaBerge's memory controller transmits data to and receives data from a memory device and processes data that is to be written to or read by a memory device, and would have been routine and simple to effectuate. Indeed, LaBerge already at least suggests transmitting data to and receiving data from a memory device, and enhancing the LaBerge-Bowater system with Grundy's specific teachings for how transmitting/receiving data and serialization/deserialization of such data is performed would have been appreciated and straightforward to POSITAs. EX1006,

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¶¶0034-0039, Figs. 5, 6; Section VIII.A.1.c, f (elements [1c], [1f]); EX1010, ¶¶0036, 0043-0044, Fig. 5A.

131. A POSITA would have combined the LaBerge-Bowater system and Grundy as above using known hardware and software techniques associated with memory devices, and for the same reasons discussed above, a POSITA would have combined the teachings with Grundy. And separate or combined, the LaBerge-Bowater and Grundy systems would have both performed the same memory and data storage functionality. The combination would have further been predictable, straightforward, and routine for a POSITA. And a POSITA would have had a reasonable expectation of success in making this combination for the same reasons discussed above, and also due to the similarities of the references, which are related to memory systems that provide improved performance. EX1006, Abstract, ¶¶0001, 0013-0014; EX1007, Abstract, 2:1-2, 3:5-18, 9:53-10:8; EX1010, Abstract, ¶¶0002, 0030.

132. Grundy is analogous art to the '379 patent, from the same field of endeavor as the patent (e.g., memory systems) and pertinent to the particular problem the patent was trying to solve (e.g., how to improve memory performance). EX1001, Abstract, 1:28-29, 4:1-20; EX1010, Abstract, ¶¶0002, 0030.

E. Ground V: LaBerge, Bowater, and Mehta render claim 8 obvious

1. Claim 8: "*The memory controller of claim 1, wherein the memory controller further comprises a data interface to*

exchange each of data, and write mask values with the memory device, via respective link subsets."

133. LaBerge, Bowater, and Mehta render claim 8 obvious. In the LaBerge, Bowater, and Mehta combination, Mehta's "memory controller 210" includes "hybrid data read/write circuit 220" (*wherein the memory controller further comprises a data interface*) coupling the controller to memory 170 and 180, where circuit 220 includes "DIMM interface modules" 310-390 to "handle[] the necessary data, data strobe, and data mask signals for read and write commands" and "[d]ata, data strobes and data mask signals are likewise passed to and from the DIMMs" through interface modules 310-390 (*to exchange each of data, and write mask values with the memory device*). EX1011, 4:12-60, 5:6-40, 6:11-17, Figs. 1-3. The passing "to and from" of data and data mask values with Mehta's DIMM memory occurs over respective "sub-buses 241-250" of "bus 240" (*exchange each of data, and write mask values with the memory device via respective link subsets*). *Id.*, 5:15-40, Figs. 1-3. "For a write operation to a DIMM, the…data mask signals…are passed from the memory controller …via bus 241 to the DIMM 170" (*id.*, 5:22-26) and a POSITA would have understood or at least found obvious that one or more sub-busses 242-250 would have been used to send data to and/or receive data from the DIMM in read and write operations as these links are used for reading and writing data. *Id.*, 4:12-60, 5:6-40, 6:11-17, Figs. 1-3. A POSITA would have further understood or at

least found obvious that one or multiple of sub-busses 241-250 form *respective link subsets* as they define the subsets of bus 240 over which data is read and written. *Id.*

134. If *a data interface to exchange…* is interpreted as a means-plus-function term, LaBerge-Bowater-Mehta discloses or at least renders obvious (1) the identified function for the same reasons discussed, and (2) the identified structure of memory controller hardware and equivalents thereof (Section V.B) for the same reasons discussed above.

2. Motivation to Combine

135. A POSITA would have been motivated to combine LaBerge and Bowater for the reasons discussed in Section VIII.A.1.e (element [1e]). A POSITA would have been motivated to combine the LaBerge-Bowater system with Mehta such that LaBerge's memory hub controller 200 (Section VIII.A.1.a, b) is enhanced by Mehta's teachings of hybrid data read/write circuit 220 that couples the controller to memory and allows for the passing to and from the memory of data and mask signals. Section VIII.E.1. The combination would have merely provided techniques by which LaBerge's memory controller transmits data to and receives data from a memory device and the ability to use mask values when writing to memory and would have been routine and simple to effectuate. Enhancing the LaBerge-Bowater system with Mehta's specific teachings for how transmitting/receiving data and uses mask values

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would have been appreciated and straightforward to POSITAs. Section VIII.A.1.b; EX1011, 4:12-60, 5:6-40, 6:11-17, Figs. 1-3.

136. A POSITA would have combined the LaBerge-Bowater system and Mehta as above using known hardware and software techniques associated with memory devices, and for the same reasons discussed above, a POSITA would have combined the teachings. And separate or combined, the LaBerge-Bowater and Mehta systems would have both performed the same memory and data storage functionality. The combination would have further been predictable, straightforward, and routine for a POSITA. And a POSITA would have had a reasonable expectation of success in making this combination for the same reasons discussed above, and also due to the similarities of the references, which are related to more flexible and efficient memory systems. EX1006, ¶¶0013-0014; EX1007, 3:35-38; *id*, 3:5-18; EX1011, 2:37-3:15.

137. Mehta is analogous art to the ’379 patent, from the same field of endeavor as the patent (e.g., memory systems) and pertinent to the particular problem the patent was trying to solve (e.g., how to improve memory performance and flexibility). EX1001, Abstract, 1:28-29, 4:1-20; EX1011, 2:37-3:15.

F. Ground VI: LaBerge, Bowater, Chan, and Kobayashi render claim 11 obvious

1. Claim 11: “*The memory controller of claim 1, wherein: the memory controller is to establish command queues respective*

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> ***to each of the banks in the memory device; the memory controller further comprises logic to time-multiplex commands from the command queues for the banks for transmission to the memory device via the command interface; and said logic is to interleave commands from the command queues in a manner that observes the first time interval, the second time interval, the third time interval and the fourth time interval.***"

138. LaBerge, Bowater, Chan, and Kobayashi render obvious claim 11. In the combination, LaBerge describes that memory controller 200 includes a "command queue 204" that "receives the high-level macro commands" and "translates the received macro commands to DRAM command signals, such as RASZ, CASZ, WESZ, etc., places the command signals in a queue in the order that their corresponding macro commands were received, and then outputs the commands in the proper order" (*the memory controller is to establish* a *command queue*). EX1006, ¶¶0034-0039, Fig. 5. LaBerge further describes that multiplexors 220 and 230 operate on the command signals to output the appropriate signal to the correct memory device 80 or 86 (*the memory controller further comprises logic to multiplex commands*). *Id.* Bowater describes a memory controller interleaving RAS and CAS commands (*and said logic is to interleave commands*) in that observe the claimed *first*, *second*, *third*, and *fourth* time intervals (*in a manner that observes the first time interval, the second time interval, the third time interval and the fourth time interval*). Sections VIII.A.1.e-f (elements [1e], [1f]), VIII.A.4 (claim 9).

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139. In the combination of LaBerge, Bowater, Chan, and Kobayashi, Chan teaches "memory command queues" 101 through 104 that each correspond to a bank of memory (*command queues respective to each of the banks in the memory device*). Chan (EX1012), 5:29-6:31, Fig. 4. Moreover, a POSITA would have understood or at least found obvious that in the LaBerge-Bowater-Chan-Kobayashi combination, Kobayashi teaches time-multiplexing commands, providing that in the combination the commands from queues 101 through 104 of Chan would have been time-multiplexed (*the memory controller further comprises logic to time-multiplex commands from the command queues*). Kobayashi (EX1013), 0163; EX1012, 5:29-6:31, Fig. 4. Moreover, in the combination, Bowater's CAS and RAS commands, located in command queues as taught by Chan, would have been interleaved (*and said logic is to interleave commands from the command queues*). EX1007, 4:25-40, 6:47-50, 7:1-13, Figs. 2, 6; VIII.A.1.e-f (elements [1e]-[1f]), VIII.A.4 (claim 9).

140. If *logic to…* is interpreted as a means-plus-function term, LaBerge-Bowater-Chan-Kobayashi discloses or at least renders obvious (1) the identified function for the same reasons discussed, and (2) the identified structure of memory controller hardware and equivalents thereof (Section V.C, *supra*) as discussed above.

Motivation to Combine

141. A POSITA would have been motivated to combine LaBerge and Bowater for the reasons discussed in Section VIII.A.1.e (element [e]). A POSITA would have

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been motivated to combine the LaBerge-Bowater system with Chan and Kobayashi such that LaBerge's memory hub controller 200 (Section VIII.A.1.a, b) is enhanced by Chan's and Kobayashi's Mehta's teachings, with LaBerge's RAS and CAS commands placed in queues corresponding to each bank of memory and being time-multiplexed and interleaved as taught. VIII.A.1.e-f (elements [1e]-[1f]), VIII.A.4 (claim 9). The combination would have merely provided techniques by which LaBerge's memory controller organizes and transmits RAS and CAS commands to memory and would have been routine and simple to effectuate, and appreciated and straightforward, to POSITAs. Indeed, LaBerge and Bowater already describe RAS and CAS commands that are sent to memory organized in banks, and Chan and Kobayashi teach techniques by which such commands are treated. EX1006, ¶¶0003, 0029, 0034-0036; EX1007, 4:25-40, 6:47-50, 7:1-13, Figs. 2, 6; EX1012, 5:29-6:31, Fig. 4; EX1013, 0163.

142. A POSITA would have combined the LaBerge-Bowater system and Chan and Kobayashi as above using known hardware and software techniques associated with memory devices. For the same reasons discussed above, a POSITA would have combined the teachings. And separate or combined, the LaBerge-Bowater and Chan and Kobayashi systems would have both performed the same memory and data storage functionality. The combination would have further been predictable, straightforward, and routine for a POSITA. A POSITA would have had a reasonable

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expectation of success in making this combination for the same reasons discussed above, and also due to the similarities of the references, which are related to more flexible and efficient memory systems. EX1006, ¶¶0013-0014; EX1007, 3:35-38; *id*, 3:5-18; EX1012, 1:8-15, 3:58-67; Fig. 4; EX1013, ¶¶0036-0045, 0163.

143. Chan and Kobayashi are analogous art to the '379 patent, from the same field of endeavor as the patent (e.g., memory systems) and pertinent to the particular problem the patent was trying to solve (e.g., how to improve memory performance and flexibility). EX1001, Abstract, 1:28-29, 4:1-20; EX1012, 1:8-15, 3:58-67; Fig. 4; EX1013, ¶¶0036-0045, 0163.

G. Ground VII: LaBerge, Bowater, and Wilcox render claims 12, 13, and 15 obvious

1. Claim 12

a. [12a] "*A memory controller to control a memory device, the memory device having a plurality of bank groups,*"

[12b] "*the memory controller comprising: circuitry to provide a clock signal to the memory device, the clock signal having clock transitions;*"

[12c] "*a command interface to transmit row activation commands and column access commands to the memory device, via a command bus;*"

144. *See* Sections VIII.A.1.a-c (elements [1a]-[1c]). Moreover, with respect to element [12c], LaBerge describes that its RASZ signals that instruct the memory devices to activate desired memory rows and CASZ signals that instruct the memory devices to allow access to desired memory columns (*row activation commands and column access commands*) are transmitted by command shifter 214, multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242 (*command interface*) via memory bus 320 (*via a command bus*). Section VIII.A.1.c (element [1c]); EX1006, ¶¶0034-0039, Figs. 5, 6. Since bus 320 carries such command signals, a POSITA would have understood or at least found obvious that it is a *command bus* as claimed. *Id.*

b. [12d] "*a data interface to exchange data with the memory device in association with each column access command; and*"

145. LaBerge, Bowater, and Wilcox renders obvious this element. In the combination, LaBerge teaches a "downstream bus 66" and "upstream bus 68" between a memory controller and memory modules, that "couple[s] data…away from or toward" the memory controller. EX1006, ¶0023, Fig. 4. The embodiment of Figure 6 utilizes a single bus 320 between memory controller 200 and memory modules 310, and a POSITA would have understood or at least found obvious that bus 320 operates in the same way as buses 66 and 68, because bus 320 similarly couples memory controller 200 to memory modules 310 and is similarly used to

access memory devices 80a, 86a, 80b, and 86b. *Id.*, ¶0039, Fig. 6; *id.*, ¶¶0034-0038, Fig. 5. Thus, a POSITA would have understood or at least found obvious that memory controller 200 uses bus 320 to couple data between the memory controller and memory modules 310, and controller 200 therefore includes an interface for coupling data using bus 320 between the controller and modules 310 *([memory controller comprising] a data interface to exchange data with the memory device*). *Id.* Moreover, a POSITA would have understood or at least found obvious that such coupling of data would have been associated with each CASZ signal that instructs the memory devices to allow access to desired memory columns when reading or writing (*in association with each column access command*) because the CASZ signal is a "column address strobe signal" and is known as being used to access a column of memory when reading from or writing to memory. EX1006, ¶¶0003 (referring to RAS and CAS signals as "command" signals), 0029, 0034-0036. For example, Dye explains that a DRAM can receive "inputs," including "Column Address Strobe," and "controls the access to specified…column address[] in the array." EX1014 (Dye), 2:41-54; *id.*, 3:39-46 (noting "control signals" include "e.g., CAS").

146. If the Board finds that LaBerge and Bowater do not explicitly teach the *memory controller* comprising a *data interface* as claimed, the combination of LaBerge, Bowater, and Wilcox teaches this. In the combination, Wilcox teaches LaBerge's memory controller 200 to be a "memory controller 18 [that] includes a

data interface 100" (*memory controller* comprising a *data interface*), where data interface 100 "includes write path circuitry 120 for purposes of writing data to the system memory 22" and "circuitry associated with the read path of the data interface 100" including "sense amplifiers 102 that are coupled to receive data bit line signals (called DQ[0:63], which represents sixty-four DQ data bit lines as an example) from respective data bit lines 104…." EX1009, ¶¶0028-0030, Fig. 3.

147. If *a data interface to exchange data…* is interpreted as a means-plus-function term, LaBerge, Bowater, and Wilcox render obvious (1) the identified function for the same reasons discussed above and the identified structure of memory controller hardware and equivalents thereof (Section V.B) for the same reasons discussed above. Further, LaBerge's memory controller, enhanced by the teachings of Wilcox's data interface 100, is at least an equivalent to memory controller hardware because both perform the same functionality of *exchanging data* as claimed in substantially the same way, i.e., by transmitting data when writing to memory and receiving data when reading memory. A POSITA would have further recognized the interchangeability of LaBerge's memory controller, enhanced by the teachings of Wilcox's data interface 100, with the identified structure as both are used to exchange data between a memory controller and memory, and such interchangeability would have been routine and well-within the capabilities of a POSITA for the same reasons.

Moreover, Wilcox's data interface 100 teachings are not excluded by any explicit definition in the '379 patent's specification for an equivalent to the identified structure.

Motivation to Combine

148. A POSITA would have been motivated to combine LaBerge and Bowater for the reasons discussed in Sections VIII.A.1.b (element [b]), VIII.A.1.e (element [e]). A POSITA would have been further motivated to combine the LaBerge-Bowater combined system with Wilcox such that LaBerge's memory controller 200 is enhanced by Wilcox's data interface 100 teachings. The combination would enhanced LaBerge's system by providing an additional technique by data is exchanged by LaBerge's memory controller with memory devices, and would have been nothing more than a design choice implemented by a POSITA.

149. Combined, LaBerge's memory controller 200 in the LaBerge-Bowater combination would have used an explicit data interface to exchange data. Such a combination would have been routine and straightforward to POSITAs. LaBerge already describes that its memory controller 200 sends and receives data from memory devices. EX1006, ¶¶0023, 0034-0039, Figs. 4-6. Wilcox, applicable to LaBerge and Bowater in that it similarly is directed to a memory controller that couples data, teaches that a memory controller that has specific read and write path circuitry. EX1009, ¶¶0028-0030, Fig. 3.

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150. Enhancing the LaBerge-Bowater system with Wilcox would have therefore been straightforward and well-within the capabilities of POSITAs, and provided a design choice as to how the LaBerge-Bowater system is implemented. Specifically, Wilcox teaches a design choice as to how data is coupled between a memory controller and memory—again, a straightforward and routine matter for POSITAs due to the fact that LaBerge already such coupling of data.

151. A POSITA would have combined the LaBerge-Bowater system with Wilcox as above using known hardware and software techniques associated with memory devices, and for the same reasons discussed above, a POSITA would have combined Wilcox's teachings with the LaBerge-Bowater system. And separate or combined, the LaBerge-Bowater and Wilcox systems would have both performed the same memory and data storage functionality. The combination would have been predictable, straightforward, and routine for a POSITA. And a POSITA would have had a reasonable expectation of success in making this combination for the same reasons discussed above, and also due to the similarities of both references, where both references are at least directed to memory controllers couple data to and from a memory device. EX1006, ¶¶0023, 0034-0039, Figs. 4-6; EX1009, ¶¶0028-0030, Fig. 3.

152. Wilcox is analogous art to the '379 patent, from the same field of endeavor as the patent (e.g., memory systems) and pertinent to the particular problem the patent

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was trying to solve (e.g., how to improve memory performance). EX1001, Abstract, 1:28-29, 4:1-20; EX1009, ¶¶0001-0007.

c. **[12e] "*circuitry coupled to the command interface to schedule issuance of the row activation commands and the column access commands to banks within the plurality of bank groups, such that*"**

[12f] "*a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common one of the bank groups, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different ones of the bank groups, and*"

[12g] "*a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common one of the bank groups, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different ones of the bank groups*;"

[12h] "*wherein the memory controller is to transmit bank address information as part of each command of the row activation commands and column access commands, to communicate selection of a bank group of the plurality of bank groups, and to communicate selection of a bank within the selected bank group*."

153. *See* VIII.A.1.d-f (elements [1d]-[1f]) and VIII.A.4 (claim 9). Moreover, with respect to element [12e], LaBerge describes that command scheduler 210 (*circuitry…to schedule issuance*) is connected to (*coupled to*) command shifter 214

(which forms part of the claimed *command interface*; VIII.A.1.c (element [1c]) as shown in Figure 5. EX1006, ¶¶0034-0039, Figs. 5, 6.

2. Claim 13: "*The memory controller of claim 12, wherein: each bank includes a first sub-bank and a second sub-bank; the first sub-bank is in a first bank group of the plurality of bank groups; and the second sub-bank is in a second bank group of the plurality of bank groups.*"

154. *See* Section VIII.A.2 (claim 2).

3. Claim 15: "*The memory controller of claim 13, wherein the circuitry to schedule is to schedule at least one column access command for each row activation command, in order to access a column within a row activated by a corresponding row activation command, and wherein the command interface is to transmit bank address information to the memory device for each row activation command and for each column access command, in order to select a bank and in order to select one of the bank groups in the plurality of bank groups.*"

155. *See* Section VIII.A.3 (claim 4).

H. Ground VIII: LaBerge, Bowater, Wilcox, and Suh render claim 14 obvious

1. Claim 14: "*The memory controller of claim 13, wherein: each sub-bank in the first bank group shares first row decoder circuitry and first column decoder circuitry with each other sub-bank in the first bank group; and each sub-bank in the second bank group shares second row decoder circuitry and second column decoder circuitry with each other sub-bank in the second bank group.*"

156. *See* Section VIII.B.1 (claim 3). A POSITA would have been motivated to combine LaBerge, Bowater, Wilcox, and Suh for the reasons in Section VIII.B.1.

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I. Ground IX: LaBerge, Bowater, Wilcox, and Halbert render claim 16 obvious

1. Claim 16: "*The memory controller of claim 13, wherein the circuitry to schedule is to schedule for a given row activation command, at least two column access commands, in order to access different columns within a row activated by the given row activation command.*"

157. *See* Section VIII.C.1 (claim 5). A POSITA would have been motivated to combine LaBerge, Bowater, Wilcox, and Halbert for the same reasons in Section VIII.C.1.

J. Ground X: LaBerge, Bowater, Wilcox, and Grundy render claims 17 and 18 obvious

1. Claim 17: "*The memory controller of claim 12, wherein the memory controller also comprises a data interface to exchange data with the memory device via links, using respective, mutually-exclusive subsets of the links to exchange data in association with the back-to-back column accesses to banks within different bank groups*."

Claim 18: "*The memory controller of claim 12, wherein: the memory controller further comprises a data interface to exchange data with the memory device via links, in association with each column access command; and the memory controller further comprises serialization/deserialization circuitry to exchange serialized data with the memory device over each of the links in association with each column access command*."

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158. *See* Section VIII.D.1 and D.2 (claims 6 and 7). A POSITA would have been motivated to combine LaBerge, Bowater, Wilcox, and Grundy for the same reasons in Section VIII.D.3.

K. Ground XI: LaBerge, Bowater, Wilcox, and Mehta render claim 19 obvious

1. Claim 19: "*The memory controller of claim 12, wherein the memory controller further comprises a data interface to exchange each of data, and write mask values with the memory device, via respective link subsets*."

159. *See* Section VIII.E.1 (claim 8). A POSITA would have been motivated to combine LaBerge, Bowater, Wilcox, and Mehta for the same reasons in Section VIII.E.2.

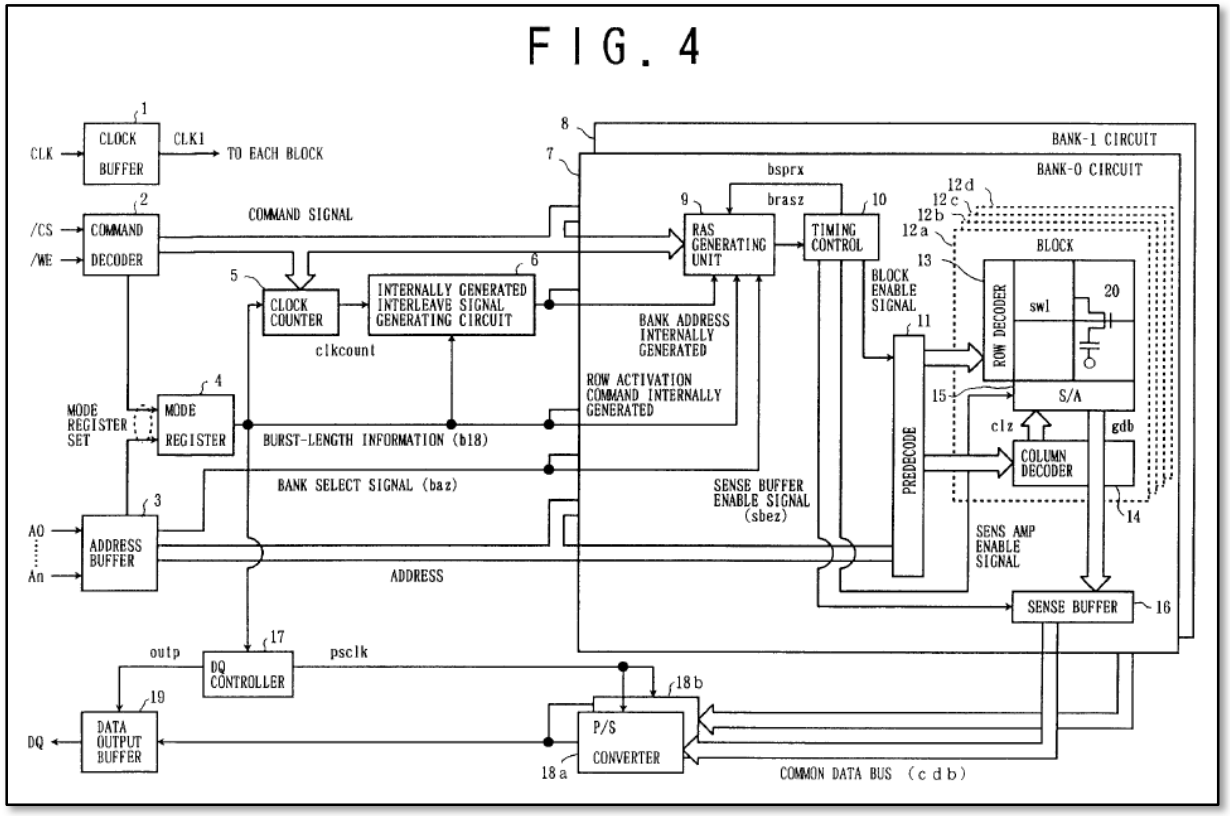
L. Ground XII: Fujioka renders claims 1 and 20 obvious

1. Claim 1

a. [1a] "*A memory controller to control a memory device, the memory device having a plurality of bank groups*"

160. If limiting, Fujioka discloses or at least renders obvious this claim element. Clock buffer 1 and predecoders 11 of bank-0 circuit 7 and bank-1 circuit 8 (collectively, a *memory controller*) control memory cell blocks 12a-12d of bank-0 circuit 7 and bank-1 circuit 8 by "control[][ling] the row decoder 13 to generate a word line select signal swl at an appropriate timing" for a selected memory cell block and "control[ling] the column decoder 14 to generate a column line select signal clz

at an appropriate timing" for a selected memory cell block (*to control a memory device*). EX1004 (Fujioka), 5:32-60, 6:21-42, 7:5-43, Fig. 4.



Fujioka, Fig. 4

161. Clock buffer 1 outputs an "internal clock signal CLK1" to predecoders 11 of bank-0 circuit 7 and bank-1 circuit 8. EX1004, 5:36-46, 6:51-62, Fig. 4 (CLK1 provided "TO EACH BLOCK," block 12a labeled a "BLOCK").

162. Fujioka's memory cell block is a "bank." EX1004, 5:32-60 9:18-20 ("bank (memory cell block) interleaving operation") (parentheses in original), Fig. 4. Bank-0 circuit 7 has a group of memory cell blocks/banks 12a-12d (first *bank group*) and bank-1 circuit 8 has another group of memory cell blocks/banks 12a-12d (second

bank group). *Id.* Memory cell blocks 12a-12d of bank-0 circuit 7 and memory cell blocks 12a-12d of bank-1 circuit 8 (*memory device*) has a plurality of groups of memory cell blocks 12a-12d (*having a plurality of bank groups*). *Id*.

b. [1b] *"the memory controller comprising: circuitry to provide a clock signal to the memory device, the clock signal having clock transitions;"*

163. Fujioka discloses or at least renders obvious element [1b]. Clock buffer 1 and predecoders 11 of bank-0 circuit 7 and bank-1 circuit 8 (collectively *the memory controller*) comprise clock buffer 1 that outputs an "internal clock signal CLK1" to memory cell blocks 12a-12d of each of bank-0 circuit 7 and bank-1 circuit 8 (*comprising: circuitry to provide a clock signal to the memory device*). EX1004, 5:36-46, 6:51-62, Fig. 4. A POSITA would have understood or at least found obvious that CLK1 (*the clock signal*) has clock transitions from a low state to a high state and a high state to low state (*having clock transitions*) because clock signals are well known in the art to have such transitions, and CLK1 is formed from input clock signal CLK which explicitly has such transitions. *Id.*; EX1004, Fig. 9.

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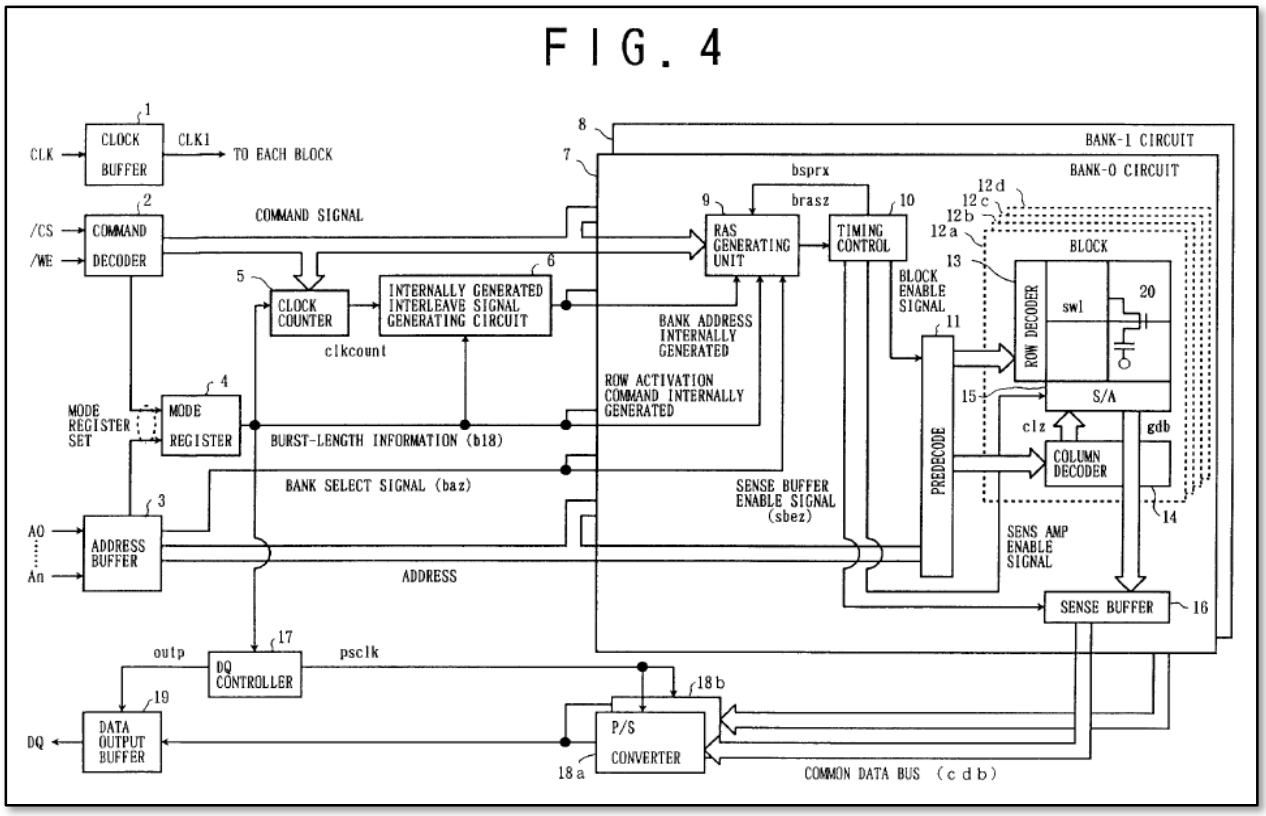

Fujioka, Fig. 4

164. If *circuitry to provide a clock signal* is interpreted under §112(6), Fujioka discloses or at least renders obvious (1) the identified function for the same reasons discussed above and (2) the identified structure and equivalents thereof (Section V.A, *supra*) because it teaches clock buffer 1. Clock buffer 1 is also at least an equivalent because both perform the same functionality of outputting an output clock signal to memory, and the components are therefore interchangeable. Moreover, clock buffer 1 is not excluded by any explicit definition in the ’379 patent's specification for an equivalent.

c. [1c] *“[the memory controller comprising:] a command interface to transmit, to the memory device, row*

activation commands to instruct row activations and column access commands to instruct column accesses; and"

165. Fujioka discloses or at least renders obvious element [1c]. Clock buffer 1 and predecoders 11 of bank-0 circuit 7 and bank-1 circuit 8 (collectively, *the memory controller*) comprise predecoders 11 of bank-0 circuit 7 and bank-1 circuit 8 (*a command interface*) that "control[] the row decoder 13 to generate a word line select signal swl at an appropriate timing" for selected memory cell blocks (*to transmit, to the memory device, row activation commands to instruct row activations*), where such control transmits the claimed commands by commanding row decoder 13 to activate a particular word line of a selected memory block 12a-12d using the word line select signal swl. EX1004, 5:32-60, 6:21-42, 7:5-43, 12:43-14:15, Fig. 4. Word lines were known in the art as rows of memory. *Id*. *See also* EX1015 (Zagar), 1:14-19 ("word line (generally referred to as a 'row' within the [DRAM] array"); EX1016 (Ando), 1:20-22 (referring to "word (row) lines").

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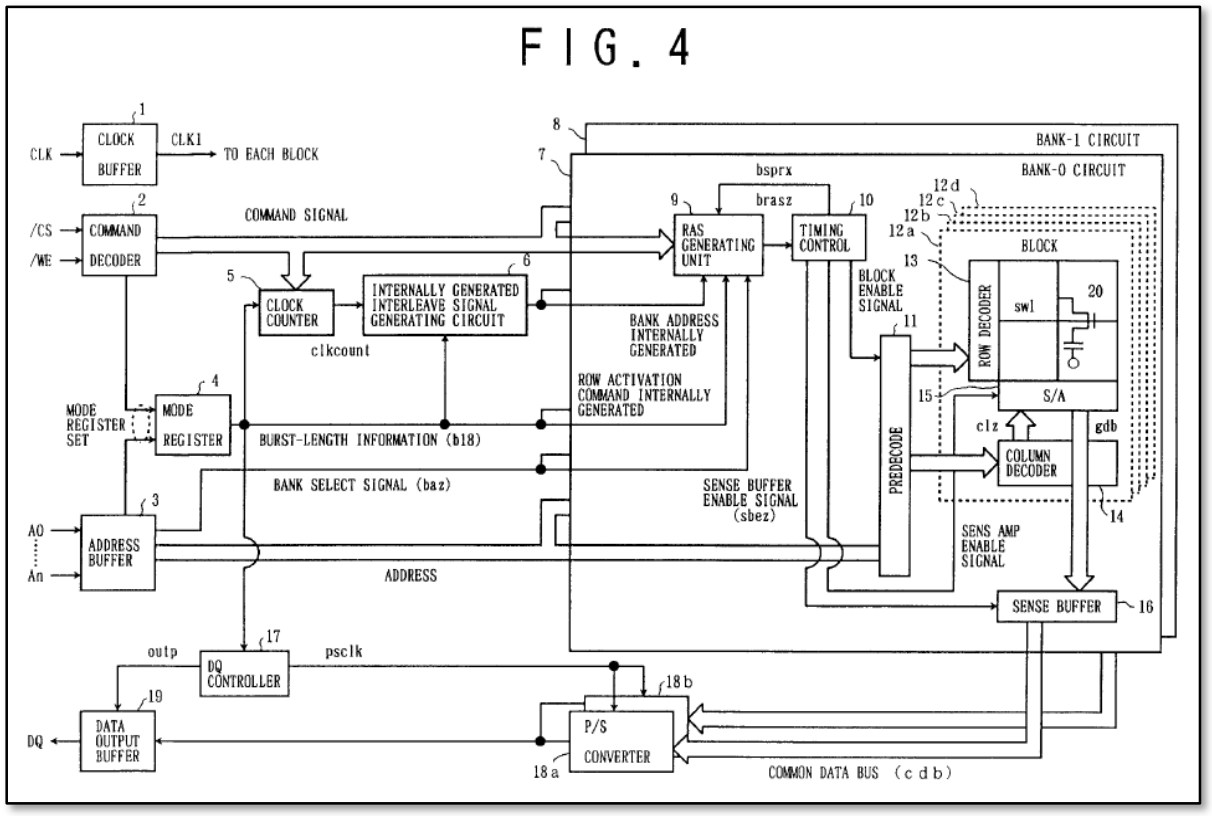

Fujioka, Fig. 4

166. Predecoders 11 of bank-0 circuit 7 and bank-1 circuit 8 (*command interface*) "control[] the column decoder 14 to generate a column line select signal clz at an appropriate timing" for selected memory cell blocks (*to transmit, to the memory device…column access commands to instruct column accesses*), where such control transmits the claimed commands by commanding column decoder 14 to access a particular column of a selected memory block 12a-12d using the column line select signal clz. Fujioka, 5:32-60, 6:21-42, 7:5-43, 12:43-14:15, Fig. 4.

167. If *a command interface to transmit…*is interpreted as a means-plus-function term, Fujioka discloses or at least renders obvious (1) the identified function for the

same reasons discussed above, and (2) the identified structure and equivalents thereof (Section V.B) because it describes predecoders 11 of bank-0 circuit 7 and bank-1 circuit 8. Further, the predecoders 11 form at least an equivalent because both perform the same functionality, i.e., transmitting row activation commands and column access commands to memory banks, and the components are therefore interchangeable. Moreover, predecoders 11 are not excluded by any explicit definition in the '379 patent's specification for an equivalent. *Id.*

d. [1d] *"[the memory controller comprising:] circuitry to schedule issuance of the row activation commands and the column access commands from the command interface, such that"*

168. Fujioka discloses or at least renders obvious element [1d]. Fujioka describes "internal interleave generating circuit 6" (*circuitry to schedule issuance…*) that "selects the bank to be activated on the basis of the burst information and the pulse signal generated by the clock counter 5." EX1004, 6:12-16, Fig. 4. Fujioka's internal interleave generating circuit 6 is *circuitry to schedule issuance of the row activation commands and the column access commands from the command interface* because it is used to schedule, based on a burst length:

- the enabling of the control (*row activation commands*) from (1) circuit 7's predecoder 11 (forming the *command interface*) to cause "row decoder 13 [of circuit 7] to change the word line select signal sw10z from the low level to the high level at an appropriate timing"

and (2) circuit 8's predecoder 11 (forming the *command interface*) to cause "row decoder 13 [of circuit 8] to change the word line select signal sw11z at an appropriate timing" (*Id.*, 8:17-50, 9:18-42, 9:51-61, Fig. 4, 12:43-13:27, 13:43-14:22, 14:38-49) and

- the enabling of control (*column access commands*) from (1) circuit 7's predecoder 11 (forming the *command interface*) to cause "column decoder 14 to change the column line select signal cl0z from the low level to the high level at an appropriate timing" and (2) circuit 8's predecoder 11 (forming the *command interface*) to cause "column decoder 14 to change the column line select signal cl1z from the low level to the high level at an appropriate timing." EX1004, 8:51-9:18, 9:51-61. 12:43-13:28, 13:43-14:22, 14:38-49.

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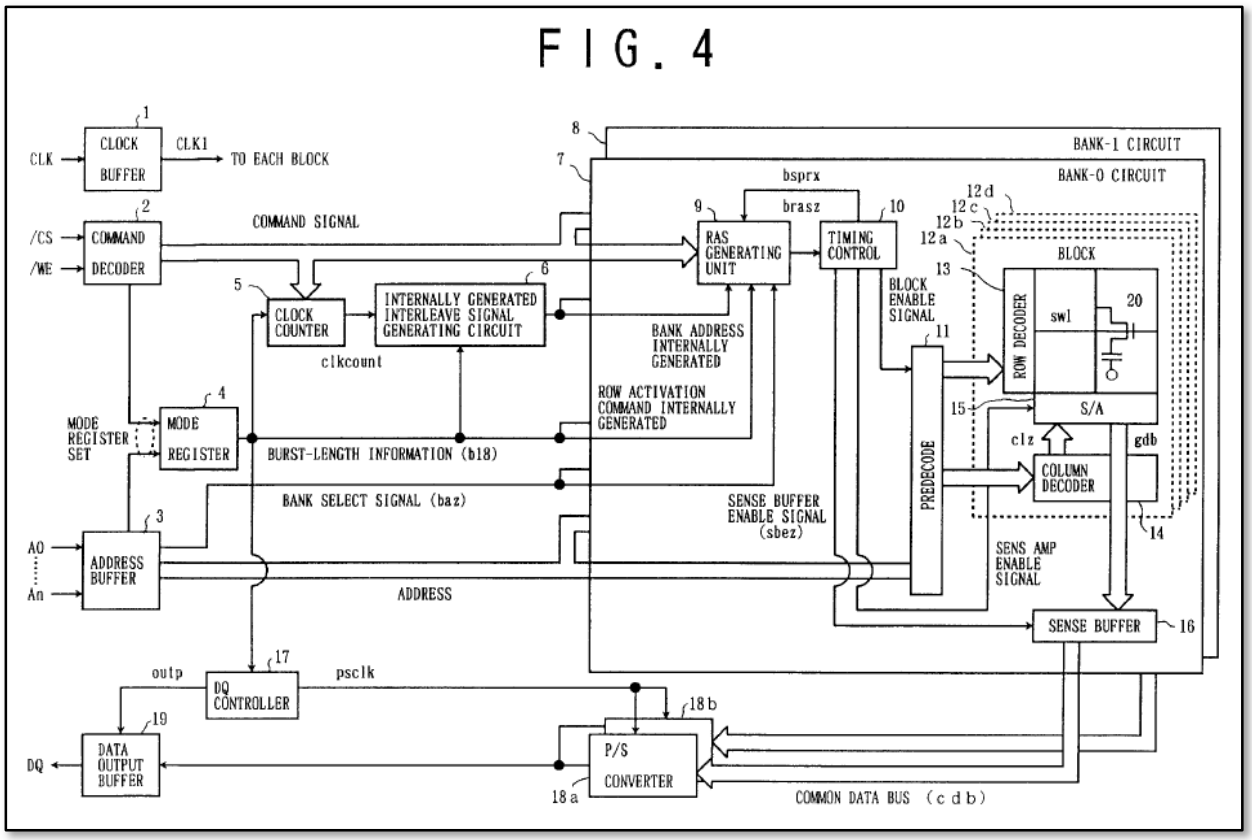


Fujioka, Fig. 4

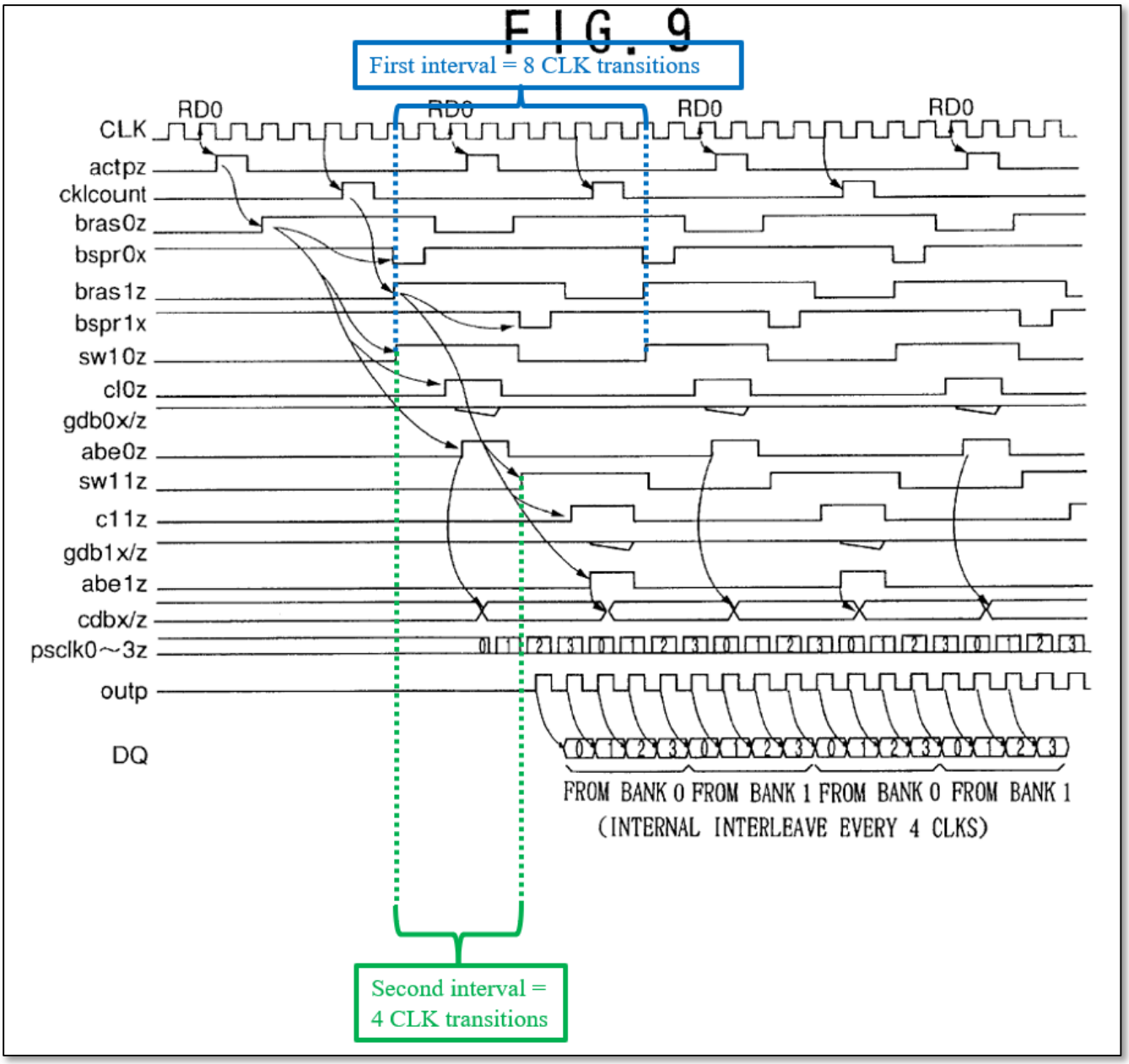
169. If *circuitry to schedule issuance…*is interpreted under §112(6), Fujioka discloses or at least renders obvious (1) the identified function for the same reasons discussed above for element [1d], and (2) the identified structure and equivalents thereof (Section V.A) because it teaches internal interleave generating circuit 6 as discussed above. Further, circuit 6 forms at least an equivalent to the structure because it performs the same functionality, i.e., by determining the appropriate timing by which commands are to be sent, and the components are therefore interchangeable. Moreover, circuit 6 is not excluded by any explicit definition in the '379 patent's specification for an equivalent.

e. [1e] *"a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common bank group, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups, and"*

170. Fujioka discloses or at least renders obvious element [1e]. Low to high changes of swl0z are *row activations to banks within a common bank group* because they are the activations of word lines in blocks (*banks*) of memory cell blocks 12a-12d (*common bank group*) in the bank-0 circuit 7. *Id.*, 12:66-13:45; *id.*, 8:45-50.

171. As discussed for element [1d], Fujioka's internal interleave generating circuit 6 (*circuitry to schedule issuance…*) schedules, based on a burst length, the enabling of control from (1) circuit 7's predecoder 11 and (2) circuit 8's predecoder 11 (*of the row activation commands and the column access commands from the command interface*). Section VIII.L.1.d (element [1d]). When the internal interleave generating circuit 6 utilizes a burst length of 8, this scheduling causes issuance of the signal "swl0z" as shown in Figure 9, such that an interval between back-to-back low to high changes of the signal "swl0z" is defined by **eight** low to high clock transitions of the signal CLK (*a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common bank group*). *Id.*; EX1004, Fig. 9. A POSITA would have further understood or at least found obvious that, since CLK forms the clock signal CLK1, clock signal

CLK1 would have also had a number of clock transitions corresponding to the eight low to high clock transitions of the signal CLK. Indeed, a POSITA would have understood that a clock signal necessarily has clock transitions as seen in the image pasted below. Section VIII.L.1.b (element [1b]).



EX1004, Figure 9 (annotated)

172. Fujioka also describes a signal "swl1z" that is a "word line select signal" that causes "the data stored in all the memory cells connected to the word line selected by the word line select signal swl1z are read by and held in the sense amplifier block 15." EX1004, 14:9-15. Low to high changes of the signal "swl1z" are activations of word lines in blocks (*banks*) of memory cell blocks 12a-12s (*bank group*) in the bank-1 circuit 8. *Id.*, 13:59-14:37.

173. The signals swl0z and swl1z therefore activate rows in banks of different bank groups, with swl0z activating rows in banks of memory cell blocks 12a-12d (*bank group*) in the bank-0 circuit 7, and swl1z activating rows banks of memory cell blocks 12a-12d (a different *bank group*) in the bank-1 circuit 8. Figure 9 shows an interval between back-to-back low to high changes of the signal swl0z and the signal swl1z. Fujioka, Fig. 9. As discussed for element [1d], Fujioka's internal interleave generating circuit 6 (*circuitry to schedule issuance…*) schedules, based on a burst length, the enabling of control from (1) circuit 7's predecoder 11 and (2) circuit 8's predecoder 11 (*of the row activation commands and the column access commands from the command interface*). Section VIII.L.1.d (element [1d]). When the internal interleave generating circuit 6 utilizes a burst length of 8, this scheduling causes issuance of the signal "swl1z" as shown in Figure 9, such that an interval between back-to-back low to high changes of the signal swl0z and the signal swl1z is defined

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by **four** low to high clock transitions of the signal CLK (*second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups*). EX1004, Fig. 9. A POSITA would have further understood or at least found obvious that, since CLK forms the clock signal CLK1, clock signal CLK1 would have also had a number of clock transitions corresponding to the four low to high clock transitions of the signal CLK. Section VIII.L.1.b (element [1b]).

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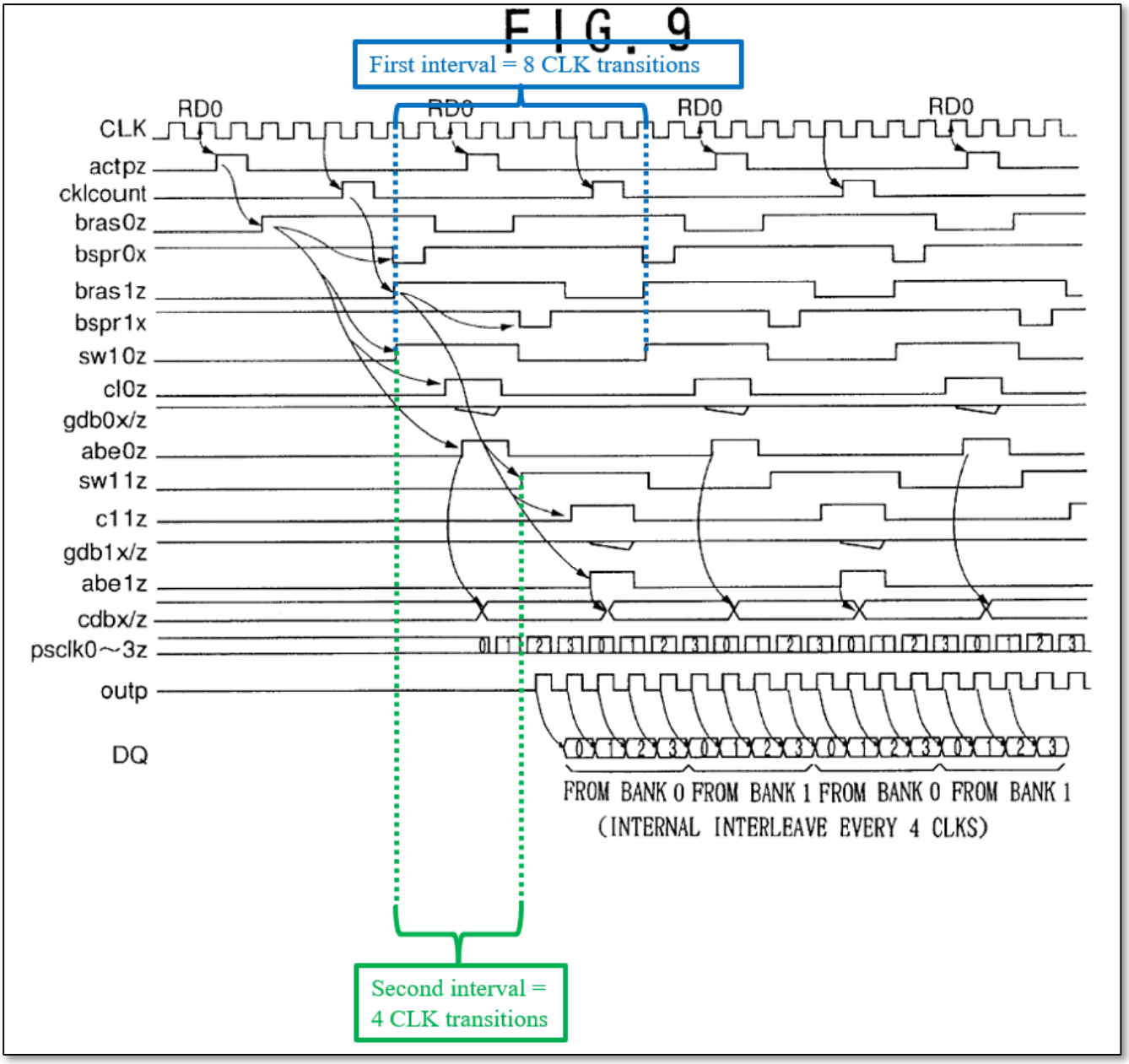

Figure 9 (annotated)

174. The interval defined by the **eight** low to high clock transitions of CLK between the back-to-back low to high changes of the signal "swl0z" (*first interval*) is longer than (*is longer than*) the interval defined by **four** low to high clock

transitions of CLK between the back-to-back low to high changes of the signal swl0z and the signal swl1z (*second interval*). EX1004, Fig. 9. And a POSITA would have understood or at least found obvious that the number of clock signal transitions of CLK1 equivalent to the eight transitions of CLK would have formed an interval longer than the interval formed by the number of clock signal transitions of CLK1 equivalent to the four transitions of CLK. A POSITA would have understood that a clock signal necessarily has clock transitions. Section VIII.L.1.b (element [1b]).

f. [1f] *"a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups."*

175. Fujioka discloses or at least renders obvious element [1f]. Fujioka describes a signal "cl0z" that is a "column line select signal" supplied to "columns specified" such that bits of data are "read from the sense amplifiers of the specified columns in parallel, and are supplied to the sense buffer 16." EX1004, 7:31-43, 12:67-13:45, 6:35-42. Low to high changes of the signal "cl0z" cause *column accesses to banks within a common bank group* because they access data in columns of blocks (*banks*) of memory cell blocks 12a-12d (*bank group*) in the bank-0 circuit 7. *Id*.

176. As discussed for element [1d], Fujioka's internal interleave generating circuit 6 (*circuitry to schedule issuance…*) schedules, based on a burst length, the enabling of control from (1) circuit 7's predecoder 11 and (2) circuit 8's predecoder 11 (*of the*

row activation commands and the column access commands from the command interface). Section VIII.L.1.d (element [1d]). When the internal interleave generating circuit 6 utilizes a burst length of 8, this scheduling causes issuance of the signal "cl0z" as shown in Figure 9, such than an interval between back-to-back low to high changes of the signal "cl0z" is defined by eight low to high clock transitions of the signal CLK (*a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group*). *Id.*; EX1004, Fig. 9. A POSITA would have further understood or at least found obvious that, since CLK forms the clock signal CLK1, clock signal CLK1 would have also had a number of clock transitions corresponding to the eight low to high clock transitions of the signal CLK. Section VIII.L.1.b (element [1b]).

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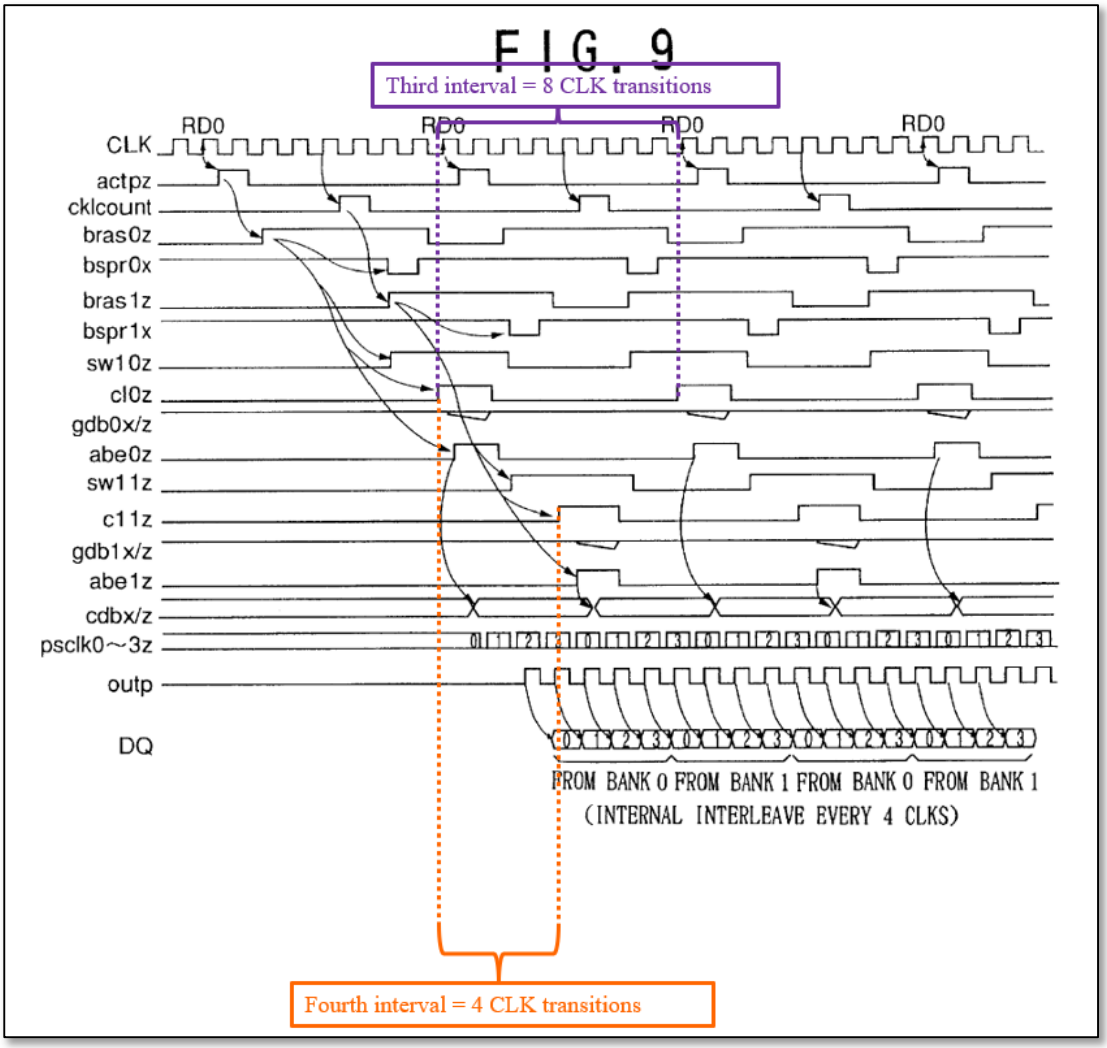

Figure 9 (annotated)

177. Fujioka also describes a signal "cl1z" that is a "column line select signal" supplied to "columns specified" such that bits of data are "read from the sense amplifiers of the specified columns in parallel, and are supplied to the sense buffer 16." EX1004, 7:31-43, 13:43-14:37, 6:35-42. Low to high changes of the signal "cl1z" access data in columns of blocks (*banks*) of memory cell blocks 12a-12d (*bank group*) in the bank-1 circuit 8. *Id.*

178. The signals cl0z and cl1z therefore access columns in banks of different bank groups, with cl0z accessing columns in banks of memory cell blocks 12a-12s (*bank group*) in the bank-0 circuit 7, and cl1z accessing columns in banks of memory cell blocks 12a-12s (a different *bank group*) in the bank-1 circuit 8. Figure 9 shows an interval between back-to-back low to high changes of the signal cl0z and the signal cl1z. EX1004, Fig. 9. As discussed for element [1d], Fujioka's internal interleave generating circuit 6 (*circuitry to schedule issuance…*) schedules, based on a burst length, the enabling of control from (1) circuit 7's predecoder 11 and (2) circuit 8's predecoder 11 (*of the row activation commands and the column access commands from the command interface*). Section VIII.L.1.d (element [1d]). When the internal interleave generating circuit 6 utilizes a burst length of 8, this scheduling causes issuance of the signal cl1z as shown in Figure 9, such that an interval between back-to-back low to high changes of the signal cl0z and the signal cl1z is defined by four low to high clock transitions of the signal CLK (*fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups*). EX1004, Fig. 9. A POSITA would have further understood or at least found obvious that, since CLK forms the clock signal CLK1, clock signal CLK1 would have also had a number of clock transitions corresponding to the four low to high clock transitions of the signal CLK. Section VIII.L.1.b (element [1b]).

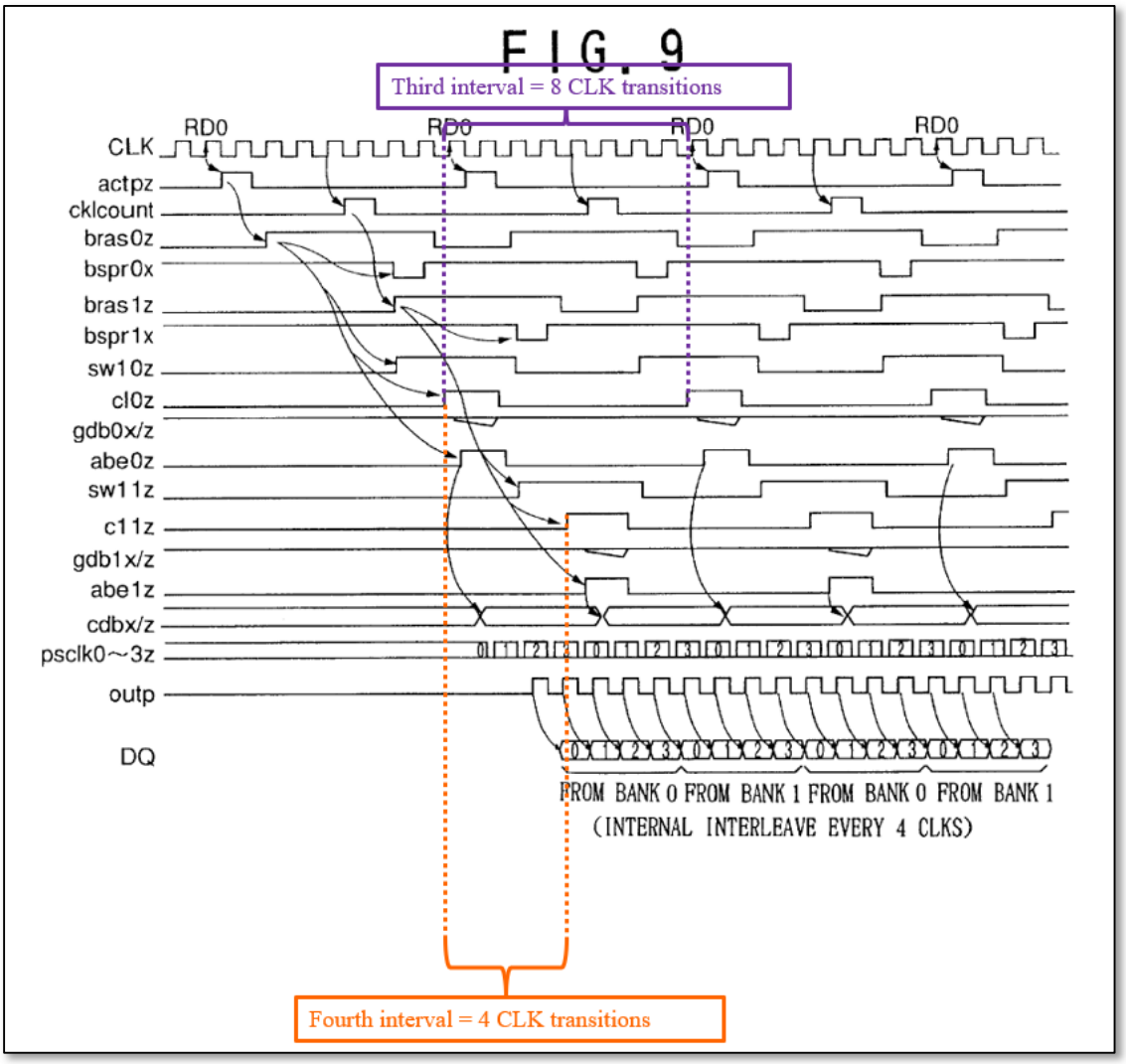

Figure 9 (annotated)

179. The interval that is defined by the **eight** low to high clock transitions of the signal CLK that occur between the back-to-back low to high changes of the signal "cl0z" (*third interval*) is longer than (*is longer than*) the interval that is defined by **four** low to high clock transitions of the signal CLK that occur between the back-to-back low to high changes of the signal cl0z and the signal cl1z (*fourth interval*).

EX1004, Fig. 9. And a POSITA would have understood or at least found obvious that, since CLK forms the clock signal CLK1, the number of clock signal transitions of CLK1 equivalent to the eight transitions of CLK would have formed an interval that is longer than the interval formed by the number of clock signal transitions of CLK1 equivalent to the four transitions of CLK. A POSITA would have understood that a clock signal necessarily has clock transitions. Section VIII.L.1.b (element [1b]).

2. Claim 20

a. [20a] "*A method of operation in a memory controller, the memory controller to control a memory device, the memory device having a plurality of bank groups, the method comprising*"

180. *See* Section VIII.L.1.a.

b. [20b] "*providing a clock signal to the memory device, the clock signal having clock transitions;*"

181. *See* Section VIII.L.1.b.

c. [20c] "*transmitting to the memory device, via a command interface, row activation commands to instruct row activations and column access commands to instruct column accesses; and*"

182. *See* Section VIII.L.1.c.

d. [20d] "*scheduling issuance of the row activation commands and the column access commands from the command interface, such that*"

183. *See* Section VIII.L.1.d.

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e. [20e] "*a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common bank group, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups, and*"

184. *See* Section VIII.L.1.e.

f. [20f] "*a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups*."

185. *See* Section VIII.L.1.f.

IX. CONCLUSION

186. For the reasons discussed herein, in my opinion, a person of ordinary skill in the art would have found the Challenged Claims of the '379 Patent rendered obvious by the prior art cited herein.

187. I understand that the Patent Owner has not asserted secondary considerations of non-obviousness. I reserve the right to respond to any such assertions.

188. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both,

under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the results of the proceedings.

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APPENDIX A

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PROFESSIONAL SUMMARY

Russel Jacob Baker (R. Jacob Baker), Ph.D., P.E. (IEEE Student Member 1983, Member 1988, Senior Member 1997, and Fellow 2013) was born in Ogden, Utah, on October 5, 1964. He received the B.S. and M.S. degrees in electrical engineering from the University of Nevada, Las Vegas (UNLV) in 1986 and 1988. He received the Ph.D. degree in electrical engineering from the University of Nevada, Reno (UNR) in 1993. His Google Scholar profile is here and his ResearchGate profile is here.

From 1981-1987 he served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division). From 1985-1993 he worked for E. G. & G. Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapons tests at the Nevada Test Site. During this time he designed, and oversaw the fabrication and the electrical/mechanical manufacture of, over 30 electronic and electro-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame- and bit-syncs for high-speed imaging, data converters, streak-camera sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics. From 1991-1993 he was an adjunct faculty member in the Departments of Electrical Engineering at UNLV and UNR. From 1993-2000 he served on the faculty in the Department of Electrical Engineering at the University of Idaho (UI), first as an untenured assistant professor and then from 1998 as a tenured associate professor. In 2000 he joined a new electrical and computer engineering (ECE) program at Boise State University (BSU) where he was promoted to professor in 2002. He then served as the ECE department chair from 2004-2007. At BSU he helped establish graduate programs in ECE including, in 2006, the university's second PhD degree. In 2012 he rejoined the faculty at UNLV as a tenured full professor of ECE. During his tenure at the UI, BSU, and UNLV he has been the major professor to more than 100 graduate students.

Dr. Baker has done consulting for over 200 companies. His research/development activities are in: photonics, circuit design for wireless and wired communications, analog-to-digital/digital-to-analog data conversion and transmission, optoelectronics (imagers, displays, LIDARs, APDs, SiPMs, and associated electronics), analog and digital integrated circuit design and fabrication, design of diagnostic electrical and electro-optic instrumentation for scientific research, integrated electrical/biological circuits and systems, array (memory, imagers, and displays) fabrication and design, design of digital processors for signal processing, CAD tool development and online tutorials, low-power interconnect and packaging (electrical and optical) techniques, design of wired/wireless communication and interface circuits, circuit design for the use and storage of renewable energy, power electronics and power supply design, and the delivery of online engineering education. As a result of this work, he is the named inventor on over 150 US patents and the author of over 100 publications.

He is a member of the honor societies Eta Kappa Nu and Tau Beta Pi, a licensed Professional Engineer, a popular lecturer that has delivered over 50 invited talks around the world, an IEEE Fellow, and the author of the books CMOS Circuit Design, Layout, and Simulation, CMOS Mixed-Signal Circuit Design, and a coauthor of DRAM Circuit Design: Fundamental and High-Speed Topics. He received the 2000 Best Paper Award from the IEEE Power Electronics Society,

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the 2007 Frederick Emmons Terman Award, the 2011 IEEE Circuits and Systems Education Award, and the 2021 Wiley-IEEE Press Textbook Award for the 4th Edition of his book CMOS Circuit Design, Layout, and Simulation.

His service activities include the IEEE Press Editorial Board (1999-2004), editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015), the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), Distinguished Lecturer for the SSCS (2012-2015), Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the IEEE Solid-State Circuits Magazine, IEEE Kirchhoff Award Committee (2020-2023), and advisor for the student branch of the IEEE at UNLV (2013-2024).

INDUSTRY EXPERIENCE

2008 - present: Expert witness in intellectual property disputes in electrical, electro-optic, and computer engineering matters for: 1) district court and ITC patent disputes, 2) inter partes reviews at the PTAB, and 3) arbitrations and mediations.

2013 - 2022: Worked with Freedom Photonics, Santa Barbara, CA, on the integration, fabrication and design, of optoelectronics with CMOS integrated circuits. Work includes the design of compact optical transceivers for range finding applications, high-efficiency integrated silicon avalanche photodetectors for quantum key receivers, Geiger mode SiGe receivers for long-range communications, cryptography, and the fabrication of near-infrared focal plane arrays. Packaging and testing of numerous chips fabricated in both CMOS and SiGe technologies using LEDs, ILDs, PIN, APDs, and ROICs.

2017 - 2019: Worked with Vorpal Research Systems, Las Vegas, NV on the design of integrated circuit electronics and optoelectronics for optical transceivers used in LIDARs/LADARs.

2016 - 2019: Worked with Attollo Engineering on the design of transient digitizers for the capture of high-speed signals for range finders using LEDs and lasers in compact optical transceivers.

2013 - 2018: Working with Mission Support and Test Services, LLC (MSTS, formerly National Security Technologies, LLC, [NSTec]) on the Design and Fabrication of Integrated electrical/photonic application specific integrated circuit (ASIC) design for use in the implementation of diagnostic instrumentation.

2013 - 2015: Consultant for OmniVision. Working on integrating CMOS image sensors (CIS) with memory for very high-speed consumer imager products. Design specialty DRAM, high-speed interfaces between CIS and DRAM, packaging techniques to pair the CIS with DRAM.

2010 - 2013: Worked with Arete' Associates on the design of high-speed compressive transimpedance amplifiers for LADAR projects and the design of ROIC unit cells. Work funded by the U. S. Air Force.

2013: Cirque, Inc. Consulting on the design of analog-to-digital interfaces for capacitive touch displays and pads.

2012: Consultant at Lockheed-Martin Santa Barbara Focal Plane Array. CMOS circuit design and fabrication for the development and manufacture of infrared components and imaging systems with an emphasis on highest sensitivity Indium Antimonide (InSb) focal plane arrays (FPAs) in linear through large staring formats. Product groups include FPAs, integrated dewar assemblies (IDCAs), camera heads, high-speed interfaces between image processors and imaging systems, and infrared imaging systems.

2010 - 2012: Working with Aerius Photonics (and then FLIR Inc. when Aerius was purchase by FLIR) on the design of Focal Plane Arrays funded (SBIRs and STTRs) by the U.S. Air Force, Navy, and Army. Experience with readout integrated circuits (ROICs) and the design/layout of photodetectors in standard CMOS.

2009 - 2010: Sun Microsystems, Inc. (and then Oracle) VLSI research group. Provided consulting on memory circuit design/fabrication and proximity connection (PxC) interfaces to DRAMs and SRAMs for lower power, 3D packaging, for memory modules and controllers implemented with FPGAs and custom ASICs.

2009 - 2010: Contour Semiconductor, Inc. Design of NMOS voltage and current references as well as the design of a charge pump for an NMOS memory chip.

1994 - 2008: Affiliate faculty (Senior Designer), Micron Technology. Designed CMOS circuits for DRAMs including DLLs, PLLs for embedded processors, voltage references and regulators, data converters, field-emitting display drivers, sensing for MRAM (using delta-sigma data conversion topologies), SRAMs, RFIDs, CMOS active pixel imagers and sensors, power supply design (linear and switching), input buffers, etc. Worked on a joint research project

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between Micron and HP labs in magnetic memory fabrication and design using the MTJ memory cell. Worked on numerous technologies ranging from LED lighting to medical imaging using CMOS image sensors (too many to list) resulting in numerous US patents (see following list). Considerable experience working with product engineering to ensure high-yield from the production line from fabrication to test. Co-authored a book on DRAM circuit design through the support of Micron. Gained knowledge in the entire memory design process from fabrication to packaging. Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing.

January 2008: Consultant for Nascentric located in Austin, TX. Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.

May 1997 - May 1999: Consultant for Tower Semiconductor, Haifa, Israel. Designed CMOS integrated circuit cells for various modem chips, interfaces, and serial buses including USB circuits, charging circuits based upon power up/down circuits using an MOS or bandgap reference, pre-amplifiers, comparators, etc.

Summer 1998: Consultant for Amkor Wafer Fabrication Services, Micron Technology, and Rendition, Inc., Design PLLs and DLLs for custom ASICs and processors.

Summers 1994 - 1995: Micron Display Inc. Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wrist watch size color television. Worked on the fabrication and design of video peripheral circuits for these displays.

September - October 1993: Lawrence Berkeley Laboratory. Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns rise-time and 8 ns fall-time for driving Helmholtz coils.

Summer 1993: Lawrence Livermore National Laboratory, Nova Laser Program. Researched picosecond instrumentation, including time-domain design for impulse radar and imaging.

December 1985 - June 1993: (from July 1992 to June 1993 employed as a consultant while finishing up my Ph.D.), E.G.&G. Energy Measurements Inc., Nevada, Senior Electronics Design Engineer. Responsible for the design and manufacturing of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Responsible for designing and fabricating over 30 electronic and electro-optic instruments including: CCD camera design, communication networks, fiber optic transmitters employing high speed laser drive electronics, receivers employing envelop tracking for DC voltage restoration and regeneration of received information, receiver low noise amplifier design, frame synchronizers for re-assembling transmitted images, high-speed SRAM memory system design with battery back-up, calibration equipment design such as a tunnel diode pulse generator for testing compensation of oscilloscopes and DAC design for calibrating CCD readout electronics, power supply and battery charger designs, sweep circuits for streak cameras, Pockel's cell drive electronics, vertical amplifier design using HBTs for analog oscilloscopes used at the Nevada Test Site, and 10 kV ramp designs using a planar triode to name some of the designs.

This position provided considerable fundamental grounding in EE with a broad exposure ranging from the design of PC boards to, for example, the design of cable equalizers. Summarizing, gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuit fabrication and design, GaAs (high speed logic and HBTs), Mach-Zehnder interferometers, Pockels cells, krytrons, power MOSFETs, microwave techniques, power supplies, fiber optic transmitters/receivers, etc.

Summer 1985: Reynolds Electrical Engineering Company, Las Vegas, Nevada. Gained hands on experience in primary and secondary power system design, installation and trouble-shooting electric motors on mining equipment.

ACADEMIC EXPERIENCE

January 1991 – present: Professor of Electrical and Computer Engineering at the **University of Nevada, Las Vegas** from August 2012 to present. From January 2000 to July 2012 held various positions at **Boise State University** including: Professor (2003 – 2012), Department Chair (2004 - 2007), and tenured Associate Professor (2000 - 2003). From August 1993 to January 2000 was a tenured/tenure track faculty member at the **University of Idaho**: Assistant Professor (1993 - 1998) and then tenured Associate Professor (1998 - 2000). Lastly, from January 1991 to May 1993 held adjunct faculty positions in the departments of Electrical Engineering at the University of Nevada, Las Vegas and Reno. Additional details:

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- Research is focused on analog and mixed-signal integrated circuit fabrication and design. Worked with multi-disciplinary teams (civil engineering, biology, materials science, etc.) on projects that have been funded by EPA, DARPA, NASA, Army, DMEA, Navy, and the AFRL.
- Current and past research and development interests are:
  - Design and packaging of electrical/optical systems (e.g., LiDARs/LADARs) using LEDs, semiconductor lasers, lens for focusing and directing light, integrated circuits, and associated control and communication systems/circuits.
  - Capacitive sensing techniques using delta-sigma modulation and interfacing to sensors
  - Design of high-voltage and energy switching circuits
  - Circuit design and fabrication for the control, use, and storage of renewable energy using thermoelectric generators
  - Design of electrical/biological/optical circuits and systems using electrowetting on dielectric for automating and controlling biological experiments
  - Design of readout integrated circuits (ROICs) for use with focal plane arrays (FPAs)
  - Heterogeneous integration of III-V photonic devices (e.g., FPAs and VCSELs) with CMOS
  - Methods (e.g., 3D packaging and capacitive interconnects) to reduce power consumption in semiconductor memories, memory modules, and digital systems using custom and non-custom (e.g., FPGAs) implementations
  - Analog and mixed-signal circuit fabrication and design for communication systems, synchronization, energy storage, data conversion, and interfaces
  - The design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g., magnetic, chalcogenide)
  - Reconfigurable electronics design and fabrication using nascent memory technologies such as the memristor to implement FPGAs
  - Finding an electronic, that is, no mechanical component, replacement for the hard disk drive using nascent fabrication technologies
  - Power electronics circuit design for consumers and consumer electronics including power management and adaptive control to reduce power consumption
  - Design of bandpass delta-sigma modulators for IQ demodulation in wireless communication systems in OFDM, WiFi, 802.11, Bluetooth, 3G, 4G, etc.
  - University prototyping, fabricating, and packaging of integrated circuits
- Led, as chair, the department in graduate curriculum (MS and PhD), program development, and ABET accreditation visits.
- Worked with established and start-up companies to provide technical expertise and identify employment opportunities for students.
- Held various leadership and service positions including: ECE chair, graduate coordinator, college curriculum committee (chair), promotion and tenure committee, scholarly activities committee, faculty search committee, university level search committees, etc. Collaborate with College of Engineering faculty on joint research projects.
- Taught courses in circuits, analog IC design, digital VLSI design and fabrication, fiber optics, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

EDUCATION

- Ph.D. in Electrical Engineering; December 1993; University of Nevada, Reno, GPA 4.0/4.0. Dissertation Title: *Applying power MOSFETs to the design of electronic and electro-optic instrumentation.*
- M.S. and B.S. in Electrical Engineering: May 1986 and May 1988; University of Nevada, Las Vegas. Thesis Title: *Three-dimensional simulation of a MOSFET including the effects of gate oxide charge*.

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MEMBERSHIPS IN PROFESSIONAL AND SCHOLARLY ORGANIZATIONS

IEEE (student, 1983; member, 1988; senior member, 1997; Fellow, 2013)
Member of the honor societies Eta Kappa Nu and Tau Beta Pi
Licensed Professional Engineer

HONORS AND AWARDS

- Consolidated Students of the University of Nevada, Las Vegas (CSUN) Faculty Award, 2017
- Tau Beta Pi UNLV Outstanding Professor of the Year in 2013, 2014, 2015 and 2016
- UNLV ECE Department Distinguished Professor of the Year in 2015
- IEEE Fellow for contributions to the design of memory circuits - 2013
- Distinguished Lecturer for the IEEE Solid-State Circuits Society, 2012 - 2015
- IEEE Circuits and Systems (CAS) Education Award - 2011
- Twice elected to the Administrative Committee of the Solid-State Circuits Society, 2011 - 2016
- Frederick Emmons Terman Award from the American Society of Engineering Education - 2007
- President's Research and Scholarship Award, Boise State University - 2005
- Honored Faculty Member - Boise State University Top Ten Scholar/Alumni Association 2003
- Outstanding Department of Electrical Engineering faculty, Boise State 2001
- Recipient of the IEEE Power Electronics Society's Best Paper Award in 2000
- University of Idaho, Department of Electrical Engineering outstanding researcher award, 1998-99
- University of Idaho, College of Engineering Outstanding Young Faculty award, 1996-97

SERVICE

Reviewer for IEEE transactions on solid-state circuits, circuits and devices magazine, education, instrumentation, nanotechnology, VLSI, etc. Reviewer for several American Institute of Physics journals as well (Review of Scientific Instruments, Applied Physics letters, etc.) Board member of the IEEE press (reviewed dozens of books and book proposals). Reviewer for the National Institutes of Health. Technology editor and then Editor-in-Chief for the Solid-State Circuits Magazine.

Led the Department on ABET visits, curriculum and policy development, and new program development including the PhD in electrical and computer engineering. Provided significant University and College service in infrastructure development, Dean searches, VP searches, and growth of academic programs. Provided university/industry interactions including starting the ECE department's advisory board. Held positions as the ECE department Master's graduate coordinator and coordinator for the Sophomore Outcomes Assessment Test (SOAT).

Also currently serves, or has served, on the IEEE Press Editorial Board (1999-2004), as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau, as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong University, as a Distinguished Lecturer for the SSCS (2012-2015), as the Technical Program Chair for the IEEE 58th 2015 International Midwest Symposium on Circuits and Systems, MWSCAS 2015, as advisor for the student branch of the IEEE at UNLV (2013-2023), and as the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the *IEEE Solid-State Circuits Magazine*, and IEEE Kirchhoff Award Committee (2020-2023).

ARMED FORCES

From 1981 to 1987 served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division), Honorable Discharge. Military Occupational Specialty (MOS) was Machine Gunner (MOS 0331)

TEXTBOOKS AUTHORED

Baker, R. J., "CMOS Circuit Design, Layout and Simulation, Fourth Edition" *Wiley-IEEE Press*, 1234 pages. ISBN 9781119481515 (2019) **Over 50,000 copies of this book in print.** (Third Edition published in 2010, Revised Second Edition published in 2008, and Second Edition Published in 2005)

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Baker, R. J., "CMOS Mixed-Signal Circuit Design," *Wiley-IEEE*, 329 pages. ISBN 978-0470290262 (second edition, 2009) and ISBN 9780471227540 (First Edition published in 2002)

Keeth, B., Baker, R. J., Johnson, B., and Lin, F., "DRAM Circuit Design: Fundamental and High-Speed Topics", *Wiley-IEEE*, 2008, 201 pages. ISBN: 9780470184752

Keeth, B. and Baker, R. J., "DRAM Circuit Design: A Tutorial", *Wiley-IEEE*, 2001, 201 pages. ISBN 0780360141

Baker, R. J., Li, H.W., and Boyce, D.E. "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1998, 904 pages. ISBN 9780780334168

BOOKS, OTHER (edited, chapters, etc.)

Saxena, V. and Baker, R. J., "Analog and Digital VLSI," chapter in the CRC Handbook on Industrial Electronics, edited by J. D. Irwin and B. D. Wilamowski, *CRC Press*, 2009 second edition.

Baker, R. J., "CMOS Analog Circuit Design," (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 2000. ISBN 0-7803-4822-2 (with textbook) and ISBN 0-7803-4823-0 (without textbook)

Baker, R. J., "CMOS Digital Circuit Design," (A self-study course with study guide, videos, and tests.) *IEEE Education Activity Department*, 2000. ISBN 0-7803-4812-5 (with textbook) and ISBN 0-7803-4813-3 (without textbook)

Li, H.W., Baker, R. J., and Thelen, D., "CMOS Amplifier Design," chapter 22 in the CRC VLSI Handbook, edited by Wai-kai Chen, *CRC Press*, 1999 (ISBN 0-8493-8593-8) and the second edition in 2007 (ISBN 978-0-8493-4199-1)

INVITED TALKS AND SEMINARS

Have given over 50 invited talks and seminars at the following locations: AMD (Fort Collins), AMI semiconductor, Arizona State University, Beijing Jiaotong University, Boise State University, Carleton University, Carnegie Mellon, Columbia University, Dublin City University (Ireland), E.G.&G. Energy Measurements, Foveon, the Franklin Institute, Georgia Tech, Gonzaga University, Hong Kong University of Science and Technology, ICSEng Keynote, ICySSS keynote, IEEE Computing and Communication Workshop (CCWC), IEEE Electron Devices Conference (NVMTS), IEEE Workshop on Microelectronics and Electron Devices (WMED), Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey (ITESM, Mexico), Iowa State University, Lawrence Livermore National Laboratory, Lehigh University, Lockheed-Martin, Micron Technology, Nascentric, National Semiconductor, Princeton University, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Temple University, Texas A&M University, Tower Semiconductor (Israel), University of Alabama (Tuscaloosa), University of Arkansas, University of Buenos Aires (Argentina), University of Houston, University of Idaho, University of Illinois (Urbana-Champaign), Université Laval (Québec City, Québec), University of Macau, University of Maryland, Université de Montréal (École Polytechnique de Montréal), Xilinx (Ireland), University of Nevada (Las Vegas), University of Nevada (Reno), University of Toronto, University of Utah, Utah State University, and Yonsei University (Seoul, South Korea).

RESEARCH FUNDING

In-kind, equipment, and other non-contract/grant funding [e.g., MOSIS support, money for travel for invited talks, etc.] not listed.

- Baker, R. J., (2023-2024) "Silicon Germanium (SiGe) Avalanche Photo Diode (APD) Chip," Department of Energy, Mission Support and Test Services (MSTS), LLC, $120,000
- Baker, R. Jacob, (2017-2023) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit," NASA, $29,999 (Phase I), $225,238 (Phase II), and $79,697 (Phase IIE)
- Goldman, J., Menezes, J., and Baker, R. J., (2021-2022) "Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling," UNLV Sports Research & Innovation Initiative. Proof of Concept Grant Program, $50,000
- Baker, R. Jacob, (2019-2021) "Dual-Mode, Extended Near-Infrared, Focal Plane Arrays Fabricated with CMOS Compatible GeSiSn Alloy Materials," DARPA, $149,998
- Baker, R. Jacob, (2018-2020) "Geiger Mode SiGe Receiver for Long-Range Optical Communications," NASA, $99,996

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- Baker, R. Jacob, (2019) "Improved Quantum Efficiency Photo-Detector," Navy, $29,999
- Baker, R. Jacob, (2018-2019) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit – Phase I," NASA, $29,999
- Baker, R. Jacob, (2017-2019) "Quantum Cryptography Detector Chip," Defense MicroElectronics Activity (DMEA), $266,029
- Baker, R. Jacob, (2017-2019) "Advanced Printed Circuit Board Design Methods for Compact Optical Transceiver," U.S. Army/DOD, $299,605
- Baker, R. Jacob, (2016-2018) "High-Sensitivity Monolithic Silicon APD and ROIC," U.S. Air Force/DOD, $299,665

DOCTORAL STUDENT SUPERVSION

10. Sachin Namboodiri – A Multi-channel MCP-PMT based Readout Integrated Circuit for LiDAR Applications (2020)
9. Wenlan Wu – High-Speed Radhard Mega-Pixel CIS Camera for High-Energy Physics (2019)
8. Kostas Moutafis – A Highly-Sensitive Global-Shutter CMOS Image Sensor with On-Chip Memory for Hundreds of kilo-frames per second Scientific Experiments (2019)
7. Yiyan Li – Portable High Throughput Digital Microfluidics and On-Chip Bacteria Cultures (2016)
6. Yacouba Moumouni – Designing, Building, and Testing a Solar Thermoelectric Generation, STEG, for Energy Delivery to Remote Residential Areas in Developing Regions (2015)
5. Qawi IbnZayd Harvard – Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design (2011)
4. Vishal Saxena – K-Delta-1-Sigma Modulators for Wideband Analog-to-Digital Conversion (2010)
3. Robert Russell Hay – Digitally-Tunable Surface Acoustic Wave Resonator (2009)
2. Xiangli Li (the first Boise State University College of Engineering PhD graduate) – MOSFET Modulated Dual Conversion Gain CMOS Image Sensors (2008)
1. Feng Lin, Research and Design of Low Jitter, Wide Locking-Range Phase-Locked and Delay-Locked Loops (2000)

MASTERS STUDENT SUPERVISION

91. Jazmine Boloor – Survey of how Irregular Pathways in the Electrical System of the Human Heart Link to Different Heart Arrhythmias (2023)
90. Abraham Lopez – An Avalanche-Transistor-Based Pulse Generator Design For Infrared Laser Applications (2023)
89. David Santiago – Development of an Automated GPIB System for Characterization of SiGe Avalanche Photodiodes (2023)
88. Minsung Cho – Studies of Forward Projection Algorithms and Implementation on PC and FPGA (2023)
87. Armani Alvarez – A Control Integrated Circuit for a Hysteretic Flyback Power Converter (2022)
86. Francisco Mata-carlos – A Wearable Electronic Monitoring Device for Low Pressure Garment Applications and Temperature Analysis for Prevention of Ulceration and Infection (2022)
85. Daniel Senda – Designs and Outcomes of Transcranial Magnetic Stimulation (TMS) and Repetitive Transcranial Magnetic Stimulation (rTMS) Circuits (2021)
84. James Skelly – Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling (2021)
83. Gonzalo Arteaga – Current-mode photon-counting circuit with SiGe BiCMOS input stage (2020)
82. Jason Silic – Design and Fabrication of a 6-bit Current-Mode ADC for Lidar and High-Speed Applications (2020)
81. Brandon Wade (2020)
80. Mario Valles Montenegro – Front-End CMOS Transimpedance Amplifiers on a Silicon Photomultiplier Resistant to Fast Neutron Fluence (2020)
79. Jonathan DeBoy (2018)
78. Dane Gentry – Design, Layout, and Testing of SiGe APDs Fabricated in a BiCMOS Process (2018)
77. James Mellot – Variable Transition Time Inverters in a Digital Delay Line with Analog Storage for Processing Fast Signals and Pulses (2018)
76. Eric Monahan – High Speed Fast Transient Digitizer Design and Simulation (2018)
75. Shada Sharif – Design and Analysis of First and Second Order K-Delta-1-Sigma Modulators in Multiple Fabrication Processes (2018)
74. Vikas Vinayaka – Analysis and Design of Analog Front-End Circuitry for Avalanche Photodiodes (APD) and Silicon Photo-Multipliers (SiPM) in Time-of-Flight Applications (2018)

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73. Claire Tsagkari – Design, Fabrication and Testing of a Capacitive Sensor Using Delta-Sigma Modulation (2017)
72. Kevin Buck – Fast Transient Digitizer and PCB Interface (2015)
71. Marzieh Sharbat Maleki (2015)
70. Angsuman Roy – Design, Fabrication and Testing of Monolithic Low-Power Passive Sigma-Delta Analog-to-Digital Converters (2015)
69. Daniel Anderson – Design and Implementation of an Instruction Set Architecture and Instruction Execution Unit for the RZ9 Coprocessor System (2014)
68. Jared Gordon – Design and Fabrication of an Infrared Optical Pyrometer ASIC (2013)
67. Justin Butterfield (2012)
66. Adam Johnson – Methods and Considerations for Testing Resistive Memories (2012)
65. Ben Millemon – CMOS Characterization, Modeling, and Circuit Design in the Presence of Random Local Variation (2012)
64. Justin Wood (2012)
63. Chamunda Ndinawe Chamunda (2011)
62. Gary VanAckern – Design Guide for CMOS Process On-Chip 3D Inductors using Thru-Wafer Vias (2011)
61. Lucien Jan Bissey – High-Voltage Programmable Delta-Sigma Modulation Voltage-Control Circuit (2010)
60. Kaijun Li (2010)
59. Yingting Li (co-supervised with Maria Mitkova) (2010)
58. Lael Matthews (co-supervised with Said Ahmed-Zaid) (2010)
57. Priyanka Mukeshbhai Parikh (2010)
56. Todd Plum (co-supervised with Jeff Jessing) – Design and Fabrication of a Chemicapacitive Sensor for the Detection of Volatile Organic Compounds (2010)
55. Rahul Srikonda (2010)
54. Avani Falgun Trivedi (2010)
53. Kuang Ming Yap – Gain and Offset Error Correction for CMOS Image Sensors using Delta-Sigma Modulation (2010)
52. Mahesh Balasubramanian – Phase Change Memory - Array Development and Sensing Circuits using Delta-Sigma Modulation (2009)
51. Lincoln Bollschweiler (2009)
50. Shantanu Gupta (2009)
49. Qawi Harvard – Wide I_O DRAM Architecture Utilizing Proximity Communication (2009)
48. Avinash Rajagiri (2009)
47. Ramya Ramarapu (2009)
46. Harikrishna Rapole (2009)
45. Aruna Vadla (2009)
44. Hemanth Ande (2008)
43. Curtis Cahoon – Low-Voltage CMOS Temperature Sensor Design using Schottky Diode-Based References (2008)
42. Prashanth Busa (2008)
41. John McCoy III (2008)
40. Dennis Montierth – Using Delta-Sigma-Modulation for Sensing in a CMOS Imager (2008)
39. Rudi Rashwand (2008)
38. Barsha Shrestha (co-supervised with Zhu Han) – Wireless Access in Vehicular Environments using Bit Torrent and Bargaining (2008)
37. Eric Becker – Design of an Integrated Half-Cycle Delay Line Duty Cycle Corrector Delay Locked Loop (2007)
36. Matthew Leslie – Noise-Shaping Sense Amplifier for Cross-Point Arrays (2007)
35. Jose Monje (2007)
34. Sanghyun Park (2007)
33. Vishal Saxena – Indirect Feedback Compensation Techniques for Multi-Stage Operational Amplifiers (2007)
32. Meshack Appikatla (2006)
31. Eric Booth – Wide Range, Low Jitter Delay-Locked Loop Using a Graduated Digital Delay Line and Phase Interpolator (2006)

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30. Sucheta Das (2006)
29. Krishna Duvvada – High Speed Digital CMOS Input Buffer Design (2006)
28. Krishnamraju Kurra (2006)
27. Soumya Narasimhan (2006)
26. Roger Porter (2006)
25. David Butler – Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes (2005)
24. Dragos Dimitriu (2005)
23. Surendranath Eruvuru – Sensing Circuit Design for an Ion Mobility Spectrometer (2005)
22. Sandhya Sandireddy (2005)
21. Harish Singidi (2005)
20. Indira Vemula – Delta-Sigma Modulator Used in CMOS Imagers (2005)
19. Bhavana Kollimarla – A 1-Bit Analog-to-Digital Converter Using Delta Sigma Modulation for Sensing in CMOS Imagers (2004)
18. Sandeep Pemmaraju – High Voltage Charge Pump Circuit for an Ion Mobility Spectrometer (2004)
17. Ravindra Puthumbaka – Circuit Design for an Ion Mobility Spectrometer (2004)
16. Brandon Roth – Comparison of Asynchronous vs. Synchronous Design Technologies using a 16-bit Binary Adder (2004)
15. Jennifer Taylor – Reading and Writing Flash Memory Using Delta-Sigma Modulation (2004)
14. Jing Plaisted – Methods for Memory Testing (2003)
13. Murugesh Subramaniam – Flash Memory Sensing Using Averaging (2003)
12. Brian Johnson – Application of an Asynchronous FIFO in a DRAM Data Path (2002)
11. Scott Ward – Electrostatic Discharge (ESD) Protection in CMOS (2002)
10. Tyler Gomm – Design of a Delay-Locked Loop with a DAC-Controlled Analog Delay Line (2001)
9. Gexin Huang (2001)
8. Chris Atkins (2000)
7. Thaddeus Black (2000)
6. Zuxu Qin (2000)
5. Hao Chen (1999)
4. Doug Hackler (co-supervised with Steve Parke) – TMOS: A Novel Design for MOSFET Technology (1999)
3. Song Liu – Design of a CMOS 6-bit Folding and Interpolating Analog-to-Digital Converter (1999)
2. Ben Ba (1997)
1. Brent Keeth – A Novel Architecture for Advanced High Density Dynamic Random Access Memories (1996)

GRANTED US PATENTS

152. Baker, R. J., “Quantizing circuits having improved sensing,” **10,658,018**, May 19, 2020.
151. Baker, R. J., “Quantizing circuits having improved sensing,” **10,403,339**, September 3, 2019.
150. Baker, R. J., “Digital Filters with Memory,” **10,366,744**, July 30, 2019.
149. Baker, R. J., “Quantizing circuits having improved sensing,” **10,127,954**, November 13, 2018.
148. Baker, R. J. and Parkinson, W., “NMOS regulated voltage reference,” **9,753,481**, September 5, 2017.
147. Baker, R. J., “Digital Filters with Memory,” **9,734,894**, August 15, 2017.
146. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **9,697,883**, July 7, 2017
145. Baker, R. J., “Comparators for delta-sigma modulators,” **9,641,193**, May 2, 2017.
144. Baker, R. J., “Quantizing circuits having improved sensing,” **9,449,664**, September 20, 2016.
143. Baker, R. J., “Error detection for multi-bit memory,” **9,336,084**, May 10, 2016.
142. Baker, R. J. and Keeth, B., “Optical interconnect in high-speed memory systems,” **9,299,423**, March 29, 2016.
141. Baker, R. J., “Methods for sensing memory elements in semiconductor devices,” **9,299,405**, March 29, 2016.
140. Baker, R. J., “Comparators for delta-sigma modulators,” **9,135,962**, September 15, 2015.
139. Baker, R. J., “Resistive memory element sensing using averaging,” **9,081,042**, July 14, 2015.
138. Baker, R. J., “Digital Filters with Memory,” **9,070,469**, June 30, 2015.
137. Baker, R. J., "Reference current sources,” **8,879,327**, November 4, 2014.
136. Baker, R. J. and Beigel, K. D., “Multi-resistive integrated circuit memory,” **8,878,274**, November 4, 2014.
135. Baker, R. J., “Methods for sensing memory elements in semiconductor devices,” **8,854,899**, October 7, 2014.

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134. Baker, R. J., "Quantizing circuits with variable parameters," **8,830,105**, September 9, 2014.
133. Baker, R. J., "Integrators for delta-sigma modulators," **8,754,795**, June 17, 2014.
132. Baker, R. J., "Methods of quantizing signals using variable reference signals," **8,717,220**, May 6, 2014.
131. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **8,712,249**, April 29, 2014.
130. Baker, R. J., "Resistive memory element sensing using averaging," **8,711,605**, April 29, 2014.
129. Baker, R. J., "Memory with correlated resistance," **8,681,557**, March 25, 2014.
128. Baker, R. J., "Reference current sources," **8,675,413**, March 18, 2014.
127. Baker, R. J., "Methods for sensing memory elements in semiconductor devices," **8,582,375**, November 12, 2013.
126. Linder, L. F., Renner, D., MacDougal, M., Geske, J., and Baker, R. J., "Dual well read-out integrated circuit (ROIC)," **8,581,168**, November 12, 2013.
125. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **8,516,292**, August 20, 2013.
124. Baker, R. Jacob, "Resistive memory element sensing using averaging," **8,441,834**, May 14, 2013.
123. Qawi, Q. I., Drost, R. J., and Baker, R. Jacob, "Increased DRAM-array throughput using inactive bitlines," **8,395,947**, March 12, 2013.
122. Baker, R. Jacob, "Memory with correlated resistance," **8,289,772**, October 16, 2012.
121. Lin, F. and Baker, R. Jacob, "Phase splitter using digital delay locked loops," **8,218,708**, July 10, 2012.
120. Baker, R. Jacob, "Subtraction circuits and digital-to-analog converters for semiconductor devices," **8,194,477**, June 5, 2012.
119. Baker, R. J., "Digital Filters for Semiconductor Devices," **8,149,646**, April 3, 2012.
118. Baker, R. J., "Error detection for multi-bit memory," **8,117,520**, February 14, 2012.
117. Baker, R. J., "Integrators for delta-sigma modulators," **8,102,295**, January 24, 2012.
116. Baker, R. J., "Devices including analog-to-digital converters for internal data storage locations," **8,098,180**, January 17, 2012.
115. Baker, R. J. and Beigel, K. D., "Multi-resistive integrated circuit memory," **8,093,643**, January 10, 2012.
114. Baker, R. J., "Quantizing circuits with variable parameters," **8,089,387**, January 3, 2012.
113. Baker, R. J., "Reference current sources," **8,068,367**, November 29, 2011.
112. Baker, R. J., "Methods of quantizing signals using variable reference signals," **8,068,046**, November 29, 2011.
111. Baker, R. J., "Systems and devices including memory with built-in self-test and methods of making using the same," **8,042,012**, October 18, 2011.
110. Baker, R. J., "Memory with correlated resistance," **7,969,783**, June 28, 2011.
109. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **7,941,056**, May 10, 2011.
108. Baker, R. J., "K-delta-1-sigma modulator," **7,916,054**, March 29, 2011.
107. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,877,623**, January 25, 2011.
106. Lin, F. and Baker, R. J., "Phase splitter using digital delay locked loops," **7,873,131**, January 18, 2011.
105. Hush, G. and Baker, R. J., "Complementary bit PCRAM sense amplifier and method of operation," **7,869,249**, January 11, 2011.
104. Baker, R. J., "Subtraction circuits and digital-to-analog converters for semiconductor devices," **7,839,703**, November 23, 2010.
103. Baker, R. J., "Digital Filters with Memory" **7,830,729**, November 9, 2010.
102. Baker, R. J., "Systems and devices including memory with built-in self test and methods of making using the same," **7,818,638**, October 19, 2010.
101. Baker, R. J., "Integrators for delta-sigma modulators," **7,817,073**, October 19, 2010.
100. Baker, R. J., "Digital filters for semiconductor devices," **7,768,868**, August 3, 2010.
99. Baker, R. J., "Quantizing circuits with variable reference signals," **7,733,262**, June 8, 2010.
98. Baker, R. J., "Quantizing circuits for semiconductor devices," **7,667,632**, February 23, 2010.
97. Baker, R. J., and Beigel, K. D., "Multi-resistive integrated circuit memory," **7,642,591**, January 5, 2010.
96. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,616,474**, November 10, 2009.
95. Baker, R. J., "Resistive memory element sensing using averaging," **7,577,044**, Aug. 18, 2009.

94. Baker, R. J., "Quantizing circuits with variable parameters," **7,538,702**, May 26, 2009.
93. Baker, R. J., "Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors," **7,528,877**, May 5, 2009.
92. Baker, R. J., "Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors," **7,515,188**, April 7, 2009.
91. Taylor, J. and Baker, R. J., "Method and apparatus for sensing flash memory using delta-sigma modulation," **7,495,964**, February 24, 2009.
90. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,489,575**, February 10, 2009.
89. Baker, R. J., "Per column one-bit ADC for image sensors," **7,456,885**, November 25, 2008.
88. Staples, T. and Baker, R. J., "Input buffer design using common-mode feedback," **7,449,953**, November 11, 2008.
87. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,421,607**, September 2, 2008.
86. Baker, R. J., "Methods for resistive memory element sensing using averaging," **7,372,717**, May 13, 2008.
85. Taylor, J. and Baker, R. J., "Method and apparatus for sensing flash memory using delta-sigma modulation," **7,366,021**, April 29, 2008.
84. Hush, G. and Baker, R. J., "Method of operating a complementary bit resistance memory sensor and method of operation," **7,366,003**, April 29, 2008.
83. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,330,390**, February 12, 2008.
82. Baker, R. J., "Input and output buffers having symmetrical operating characteristics and immunity from voltage variations," **7,319,620**, January 15, 2008.
81. Staples, T. and Baker, R. J., "Method and apparatus providing input buffer design using common-mode feedback," **7,310,018**, December 18, 2007.
80. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,286,428**, October 23, 2007.
79. Baker, R. J., and Cowles, T. B., "Method and apparatus for reducing duty cycle distortion of an output signal," **7,271,635**, September 18, 2007.
78. Baker, R. J., and Cowles, T. B., "Method and apparatus for reducing duty cycle distortion of an output signal," **7,268,603**, September 11, 2007.
77. Hush, G., Baker, R. J., and Moore, J., "Skewed sense AMP for variable resistance memory sensing," **7,251,177**, July 31, 2007.
76. Hush, G. and Baker, R. J., "Method of operating a complementary bit resistance memory sensor," **7,242,603**, July 10, 2007.
75. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,237,136**, June 26, 2007.
74. Moore, J. and Baker, R. J., "Rewrite prevention in a variable resistance memory," **7,224,632**, May 29, 2007.
73. Baker, R. J., "Integrated charge sensing scheme for resistive memories," **7,151,698**, December 19, 2006.
72. Baker, R. J., "Adjusting the frequency of an oscillator for use in a resistive sense amp," **7,151,689**, December 19, 2006.
71. Baker, R. J., "Resistive memory element sensing using averaging," **7,133,307**, Nov. 7, 2006.
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- Harvard, Q. I. and Baker, R. J., “Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design,” a presentation covering semiconductor packaging, DRAM architectures, and I/O circuits. The goal of this work is to investigate replacing the currently used dual in-line memory modules (DIMMs) with a smaller and a lower power memory module, a “Nano-Module.”
- Baker, R. J., and Campbell, K. A., “Reconfigurable Analog Electronics using the Memristor.”
- Baker, R. J., and Saxena, V., “A K-Delta 1-Sigma Modulator for Wideband Analog-to-Digital Conversion.”
- Li, K., Saxena, V., and Baker, R. J., "The Baker ADC: An Overview,"
- Saxena, V., and Baker, R. J., "High-Speed Op-Amp Design: Compensation and Topologies for Two and Three Stage Designs,"
- Baker, R. J., "Circuit Design for MLC Flash: Towards a Semiconductor Replacement for the Hard Disk Drive."
- Baker, R. J., Terman Award Acceptance Speech, given at the Frontiers in Education Conference (FIE 2007), Milwaukee, WI, October 11, 2007.
- Baker, R. J., "The One-Transistor, One-Capacitor (1T1C) Dynamic Random Access Memory (DRAM), and its Impact on Society," presented at the Franklin Institute, in the symposium honoring Dr. Robert H. Dennard and his receipt of the 2007 Benjamin Franklin Medal in Electrical Engineering, April 25, 2007.
- Baker, R. J. and Saxena, V., "Design of Bandpass Delta-Sigma Modulators: Avoiding Common Mistakes."
- Baker, R. J., "Sensing Circuits for Resistive Memory."
- Hadrick, M. and Baker, R. J., "Sensing in CMOS Imagers using Delta-Sigma Modulation."

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- Baker, R. J., "Design of High-Speed CMOS Op-Amps for Signal Processing," IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), April, 2005
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36. Saxena, V., and Baker, R. J., "Compensation of CMOS Op-Amps using Split-Length Transistors," *Proceedings of the IEEE 51st Midwest Symposium on Circuits and Systems*, pp. 109-112, August 10-13, 2008**.**
36. Saxena, V., and Baker, R. J., "Indirect Compensation Technique for Low-Voltage Op-Amps," *Proceedings of the* 3*rd Annual Austin Conference on Integrated Systems and Circuits (ACISC)*, May 7-9, 2008**.**
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23. Butler, D. L. and Baker, R. J., *Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes*, *Proceedings of the IEEE 48th International Midwest Symposium on Circuits and Systems*, Aug. 7-10, 2005.
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18. Stutzke, N., Cheek, B. J., Wiscombe, M., Lowman, T., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Effects of Circuit-Level Stress on Inverter Performance and MOSFET Characteristics*, 2003 IEEE International Integrated Reliability Workshop, Oct, 20-23.
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16. Baker, R. J., *Mixed-Signal Design in the Microelectronics Curriculum,* IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2.

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11. Cheek, B., Lawrence, C., Lawrence, T., Caldwell, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., Circuit level reliability of ultrathin gate oxides for SICBBs: Preliminary study concentrated on the effect of stress on the NMOSFET of an inverter, poster session at the IEEE International Integrated Reliability Workshop, October 21-24, 2002.
10. Baker, R. J., "Sensing Circuits for Resistive Memory," *IEEE Electron Devices Society* Meeting, Boise, Idaho October 25, 2002.
9. Rivera, B., Baker, R. J., Melngailis, J., "Design and Layout of Schottky Diodes in a Standard CMOS Process," 2001 International Semiconductor Device Research Symposium, Washington DC, Dec. 2001.
8. Hess, H. and Baker, R. J., "Easier Method to Simultaneously Trigger Series-Connected MOS Devices," *Power Systems World Conference* 2000, Boston, Massachusetts, September 2000.
7. Baker, R. J., and Hess, H., "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices." *International Electric Machines and Drives Conference,* Seattle, Washington, May 1999, pp. 673-676.
6. Baker, R. J., "A windows based integrated circuit design tool for distance education," *International Conference on Simulation and Multimedia in Engineering Education*."
5. Chen, H. and Baker, R. J., "A CMOS Standard-Cell Library for the PC-based LASI Layout System," *Proceedings of the 41st International Midwest Symposium on Circuits and Systems, August 9-12, 1998.*
4. Liu, S. and Baker, R. J., "Process and temperature performance of a CMOS beta-multiplier voltage reference," *Proceedings of the 41st International Midwest Symposium on Circuits and Systems, August 9-12, 1998.*
3. Boyce, D.E. and Baker, R. J., "A Complete Layout System for the PC," *IEEE 40th International Midwest Symposium on Circuits and Systems*, 1997.
2. Baker, R. J., and Blair, J. J., "Step response considerations and the design of a suitable step generator for high speed digitizer testing," *LLNL's Third Annual Workshop on High Speed Digitizers,* April 3-4, Las Vegas, Nevada, 1991.
1. Baker, R. J., "Step-recovery diodes sharpen pulses," *Engineering Design News Magazine*, pp. 154-156, May 10, 1990.

EXPERT WITNESS EXPERIENCE

The law firms and clients (underlined) whom I have provided expert witness services in electrical and computer engineering are listed below. I have been deposed 105 times, given expert testimony at 14 trials (7 USITC, 2 D. Del., 1 Arbitr., 1 S.D. Cal., 1 N.D. Ga., 1 D. Ore., and 1 E.D. Tex.), and participated in 1 mediation.

DLA Piper LLP (Palo Alto, CA and Austin, TX)

Case – *BOE Technology Group Co., Ltd.* v. Optronic Sciences LLC
Case Numbers – IPR2024-01130, IPR2024-01133, and IPR2024-01134. Petitions filed on July 5, 2024
Case Subject Matter – Imaging pixels, layout, and fabrication. Light emitting devices, including packaging, covers, and structures.
Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Dentons US LLP (Washington, DC)

Case – *Reolink Digital Technology Co., Ltd.* v. KT Imaging US, LLC

Case Numbers – IPR2024-01154 and IPR2024-01155. Petitions filed on July 3, 2024

Case Subject Matter – Image sensor structure and package with integrated lens module for digital image products such as digital cameras, camera phones, video phones, fingerprint readers and so on.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Paul Hastings LLP (Washington, DC)

Case – Ex Parte Reexaminations

Case Numbers – 90/019,560, 90/019,962, and 90/019,964. Requests filed on July 1, 2024

Case Numbers – 90/019,556, 90/019,557, and 90/019,558. Requests filed on June 28, 2024.

Case Subject Matter – Wireless charging systems, power sources, and inductive receivers for charging mobile devices.

Work Performed – Provided expert consulting services and wrote declarations for ex parte reviews.

Banner Witcoff (Chicago, IL and Washington, DC)

Case – *ZF Friedrichshafen AG, ZF Active Safety and Electronics US LLC, and Nissan Motor Company, Ltd.* v. Foras Technologies, Ltd.

Case Number – IPR2024-00969. Petition filed on June 24, 2024.

Case Subject Matter – Detecting loss of lockstep between pairs of processors and loss of lockstep recovery

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Fish & Richardson P.C. (San Diego, CA and Boston, MA)

Case – *Vicor Corporation* v. Delta Electronics, Inc.

Case Numbers – IPR2024-00704, IPR2024-00705, IPR2024-00706, and IPR2024-00715. Petitions filed on March 25, 2024.

Case Subject Matter – Power converters including design, packaging, heatsinking and manufacturing. Resonant converters with overcurrent protection.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Winston & Strawn LLP (Los Angeles, CA and Redwood City, CA)

Case – *Silicon Motion, Inc.* v. Unification Technologies LLC

Case Number – IPR2024-00199. Petition filed on December 18, 2023.

Case Subject Matter – Memory controller, solid-state drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Garlick & Markison, LLC (Austin, TX)

Case – *NXP USA, Inc.* v. Bell Semiconductor, LLC

Case Numbers – IPR2024-00167 and IPR2024-00168. Petitions filed on November 9, 2023.

Case Subject Matter – Semiconductor manufacturing processes, fabrication and packaging of integrated circuits, layout and routing of signal lines.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Unified Patents, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/019288. Request filed on October 20, 2023.

Case Subject Matter – Power conversion device to drive an alternating-current motor for an electric vehicle.

Work Performed – Provided expert consulting services and wrote declaration.

Haynes and Boone, LLP (Dallas, TX)

Case – *Western Digital Technologies, Inc.* v. Longitude Licensing LTD.

Case Number – IPR2023-01200. Petition filed on July 14, 2023.

Case Subject Matter – Communications between a memory controller and memory.

Work Performed – Provided expert consulting services, wrote declaration for inter partes review, and was deposed.

Paul Hastings LLP (Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. Mojo Mobility, Inc.

Case Numbers – IPR2023-01094, IPR2023-01095, IPR2023-01096, IPR2023-01097, IPR2023-01098, IPR2023-01099, IPR2023-01100, and IPR2023-01124. Petitions filed on June 30, 2023.

Case Numbers – IPR2023-01101 and IPR2023-01102. Petitions filed on June 29, 2023.

Case Numbers – IPR2023-01091, IPR2023-01092, and IPR2023-01093. Petitions filed on June 28, 2023.

Case Numbers – IPR2023-01086, IPR2023-01087, IPR2023-01088, IPR2023-01089, and IPR2023-01090. Petitions filed on June 27, 2023.

Case Subject Matter – Wireless charging systems, power sources, and inductive receivers for charging mobile devices.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Winston & Strawn LLP (Los Angeles, CA, Redwood City, CA, Chicago, IL, and Houston, TX)

Case – Unification Technologies LLC v. *Silicon Motion, Inc.*

Case Number – Texas, ED (Marshall) 2:23-cv-00267. Complaint filed June 2, 2023.

Case Subject Matter – Memory controller, solid-state drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services.

Norton Rose Fulbright LLP (Austin, TX and Dallas, TX)

Case – *Current Lighting Solutions, LLC d/b/a GE Current* v. Jiaxing Super Lighting Electric Appliance Co., Ltd.

Case Numbers – IPR2023-00979 and IPR2023-00980. Petitions filed on May 31, 2023.

Case Number – IPR2023-00270. Petition filed on December 19, 2022.

Case Number – IPR2023-00271. Petition filed on December 14, 2022.

Case Subject Matter – LED lighting, lamps, tube lamps, assembly, and associated circuits and electronics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes review.

Baker Botts LLP (Dallas, TX)

Case – *Lennox Industries Inc.* v. Rosen Technologies LLC

Case Numbers – IPR2023-00715, IPR2023-00716, IPR2023-00717, IPR2023-00718, and IPR2023-00719. Petitions filed on March 29, 2023.

Case Subject Matter – Thermostat system communications, programming, and displays.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Cooley LLP (Palo Alto, CA)

Case – *Nintendo Co., Ltd. and Nintendo of America Inc.* v. Polaris PowerLED Technologies, LLC

Case Number – IPR2023-00778. Petition filed on March 28, 2023.

Case Subject Matter – Visual displays, circuit design, and related technologies.

Work Performed – Provided expert consulting services, wrote declaration for inter partes review, and was deposed.

Bracewell LLP (New York, NY and Seattle, WA)

Case – *Kioxia America, Inc. and Kioxia Corporation* v. BiTMICRO LLC

Case Numbers – IPR2023-00741, IPR2023-00742, and IPR2023-00743. Petitions filed on March 23, 2023.

Case Subject Matter – Solid-state storage devices utilizing multi-profile memory controllers. Optimizing memory operations in a memory system suitable for use in an electronic storage device. Supplying energy to a cache memory using a super capacitor.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Bookoff McAndrews, PLLC (Washington, DC)

Case – *Lenovo Inc. and Motorola Mobility LLC* v. Theta IP, LLC

Case Numbers – IPR2023-00694, IPR2023-00697, and IPR2023-00698. Petitions filed on March 7, 2023.

Case Subject Matter – Power in wireless communication circuits.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA and San Diego, CA)

Case – Semiconductor Design Technologies LLC v. *Cadence Design Systems, Inc.*

Case Number – California, ND 3:23-cv-01001. Complaint filed March 6, 2023.

Case Subject Matter – Semiconductor design support device/method and manufacturing method for semiconductor integrated circuit.

Work Performed – Provided expert consulting services.

McDermott Will & Emery LLP (Chicago, IL and Austin, TX)

Case – *Xilinx, Inc.* v. Polaris Innovations Limited

Case Numbers – IPR2023-00513 and IPR2023-00514. Petitions filed on February 6, 2023.

Case Subject Matter – Methods for terminating a memory chip with various termination resistances and output drivers for integrated circuits.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed**.**

Willkie Farr & Gallagher LLP (San Franciso, CA)

Case –Bell Semiconductor, LLC. v. *Synopsys, Inc.*

Case Number – California, SD 3:22-cv-00594. Complaint filed on January 31, 2023.

Case Subject Matter – Integrated circuit design computer-aided design (CAD) tools for routing, design rule checking, layout versus schematic, electrical checking, dummy fill, reducing capacitance.

Work Performed – Provided expert consulting services and wrote expert reports.

Fish & Richardson P.C. (Washington, DC, Atlanta, GA, and Boston, MA)

Case – Element Capital Commercial Company PTE. LTD v. *BOE Technology Group Co. LTD and Motorola (Wuhan) Mobility*

Case Number – Texas, ED (Marshall) 2:22-cv-00118. Complaint filed January 11, 2023.

Case Subject Matter – Display technology, layout, circuit design, pixel design and fabrication.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Baker Botts LLP (San Franciso, CA and New York, NY) and O'Melveny & Myers LLP (Los Angeles, CA)

Case – Polaris PowerLED, LLC v. *Samsung Electronics and Samsung Display*

Case Number – Texas, ED (Marshall) 2:22-cv-00469. Complaint filed December 12, 2022.

Case Subject Matter – active matrix organic light-emitting diode (AMOLED) displays, controlling the intensity of light-emitting diodes in backlights of displays, control circuits for adjusting current delivery based upon temperature.

Work Performed – Provided expert consulting services including writing a declaration for claim construction.

Arnold & Porter (Los Angeles and Palo Alto, CA) and Willkie Farr & Gallagher LLP (San Franciso, CA)

Case – *Synopsys, Inc. and Cadence Design Systems, Inc.* v. Bell Semiconductor, LLC.

Case Number – Delaware, 1:22-cv-01512. Complaint filed on November 18, 2022.

Case Subject Matter – Integrated circuit design computer-aided design (CAD) tools for routing, design rule checking, layout versus schematic, electrical checking, dummy fill, reducing capacitance.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Paul Hastings LLP (Washington, DC)

Case – Ex Parte Reexaminations

Case Numbers – 90/015155 and 90/015156. Requests filed on November 7, 2022.

Case Number – 90/015134. Request filed on October 14, 2022.

Case Number – 90/015130. Request filed on September 30, 2022.

Case Subject Matter – Packaging and fabrication of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declaration.

Russ August & Kabat (Los Angeles, CA)

Case – *Resonant Systems, Inc.* v. Sony
Case Number – Texas, ED (Marshall) 2:22-cv-00424. Complaint filed on October 26, 2022.
Case Subject Matter – Linear vibration modules and linear-resonant vibration modules.
Work Performed – Provided expert consulting services and wrote claim construction disclosure.

Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA and San Diego, CA) and Willkie Farr & Gallagher LLP (San Francisco, CA)

Case – Bell Semiconductor, LLC v. *NXP*, SMC, Micron, Nvidia, *Advanced Micro Devices (AMD)*, *Acer*, Infineon, Qualcomm, Motorola Mobility, and Western Digital
Case Number – ITC Investigation No. 337-TA-1340. Complaint filed October 6, 2022.
Case Subject Matter – Electronic devices, semiconductor devices, and components.
Work Performed – Provided expert consulting services.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Daedalus Prime LLC v. *Samsung Electronics* and Qualcomm Inc.
Case Number – ITC Investigation No. 337-TA-1335. Complaint filed September 12, 2022.
Case Subject Matter – Semiconductor devices, mobile devices, and components.
Work Performed – Provided expert consulting services.

Fish & Richardson P.C. (Boston, MA, Houston, TX, and Washington, DC)

Case – Sonrai Memory LTD. v. *Micron Technology, Inc.*
Case Number – Texas, WD (Waco) 6:22-cv-00855 and Texas, WD (Waco) 1:23-cv-01407. Complaint filed August 16, 2022.
Case Subject Matter – Portable RAM drive and variable charge pump circuit with dynamic load.
Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Russ August & Kabat (Los Angeles, CA and New York, NY)

Case – *NextGen Innovations, LLC* v. Infinera, Fujitsu, AT&T, and Nokia
Case Number – Texas, ED (Marshall) 2:22-cv-00306, Texas, ED (Marshall) 2:22-cv-00307, Texas, ED (Marshall) 2:22-cv-00308, and Texas, ED (Marshall) 2:22-cv-00309. Complaints filed on August 9, 2022.
Case Subject Matter – optical transmission systems including optical components for encoding, transmission (fiber optic transmitters and receivers), and decoding of data and related standards and concepts.
Work Performed – Provided expert consulting services, wrote claim construction disclosure, wrote expert reports, and was deposed twice.

DLA Piper (Chicago, IL and Washington, DC)

Case – Ampt, LLC v. *SolarEdge Technologies, Inc.*
Case Number – ITC Investigation No. 337-TA-1327. Complaint filed July 28, 2022.
Case Subject Matter – Solar power optimizers, inverters, and components.
Work Performed – Provided expert consulting services including writing declarations for claim construction, expert reports, and was deposed.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)

Case – Signify North America Corporation v. *Shenzhen Intellirocks Tech Co.*
Case Number – Texas, WD (Waco) 6:22-cv-00760. Complaint filed on July 8, 2022.
Case Subject Matter – LED packaging, circuits, and systems.
Work Performed – Provided expert consulting services including writing declaration for claim construction. Was deposed.

Baker Botts LLP (Dallas, TX)

Case – Rosen Technologies LLC v. *Lennox Industries Inc.*
Case Number – Texas, ND (Dallas) 3:22-cv-00732. Complaint filed on June 7, 2022.
Case Subject Matter – Thermostat system communications, programming, and displays.
Work Performed – Provided expert consulting services.

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Paul Hastings LLP (Austin, TX and Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. Scramoge Technology Ltd.
Case Numbers – IPR2022-01052, IPR2022-01053, and IPR2022-01058. Petitions filed on May 26, 2022.
Case Numbers – IPR2022-01054, IPR2022-01055, IPR2022-01056, and IPR2022-01057. Petitions filed on May 24, 2022.
Case Number – IPR2022-00939. Petition filed on April 29, 2022.
Case Subject Matter – An antenna that supports wireless charging using switching power supplies such as flyback converters.
Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Ex Parte Reexaminations
Case Number – 90/015020. Request filed on May 2, 2022.
Case Number – 90/014906. Request filed on November 12, 2021.
Case Number – 90/014899. Request filed on November 10, 2021.
Case Number – 90/014888. Request filed on October 21, 2021.
Case Numbers – 90/014886 and 90/014887. Requests filed on October 20, 2021.
Case Number – 90/014885. Request filed on October 19, 2021.
Case Subject Matter – Universal Serial Bus (USB) for charging.
Work Performed – Provided expert consulting services and wrote declarations**.**

DLA Piper (Chicago, IL, Austin, TX, and Washington, DC)

Case – *SolarEdge Technologies, Inc.* v. Fronius International GMBH
Case Number – IPR2022-00849. Petition filed on April 14, 2022.
Case Subject Matter – Mechanical assembly and enclosure whereby an upper housing part is detached from a lower housing part using a "rotate-and-lift" feature.
Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Kirkland & Ellis LLP (New York, NY)

Case – *Samsung Electronics Co.* v. Sonrai Memory Ltd.
Case Numbers – IPR2022-00305 and IPR2022-00306. Petitions filed on December 10, 2021.
Case Subject Matter – USB devices and circuits for saving power.
Work Performed – Provided expert consulting services including writing declarations for inter partes reviews.

Haynes and Boone, LLP (Washington, DC)

Case – *Unified Patents, LLC* v. Arigna Technology Limited
Case Number – IPR2022-00285. Petition filed on December 9, 2021.
Case Subject Matter – High voltage driver circuit for driving power devices such as insulated gate bipolar transistors (IGBTs).
Work Performed – Provided expert consulting services, wrote declaration for inter partes review and was deposed.

Paul Hastings LLP (Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. Lynk Labs, Inc.
Case Numbers – IPR2022-00149 and IPR2022-00150. Petitions filed on November 12, 2021
Case Numbers – IPR2022-00100 and IPR2022-00101. Petitions filed on October 28, 2021.
Case Numbers – IPR2022-00051, IPR2022-00052, and IPR2022-00098. Petitions filed on October 27, 2021.
Case Numbers – IPR2021-01575 and IPR2021-01576. Petitions filed on October 1, 2021.
Case Numbers – IPR2021-01299, IPR2021-01300, IPR2021-01345, IPR2021-01346, and IPR2021-01347. Petitions filed on September 7, 2021.
Case Subject Matter – Circuit design, including switching power supply design (e.g., flyback), rectifiers, power factor correction, etc. for lighting and displays using light emitting diodes (LEDs).
Work Performed – Provided expert consulting services, wrote declarations, and was deposed ten times.

Haynes and Boone, LLP (Plano, TX)

Case – *Pure Storage, Inc.* v. Digital Cache, LLC

Case Number – IPR2022-00121. Petition filed on October 29, 2021.

Case Subject Matter – Non-volatile memory (NVM) devices capable of retaining stored data in case of a power failure.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Banner Witcoff (Washington, DC)

Case – *SolarEdge Technologies Ltd.* v. Koolbridge Solar, Inc.

Case Numbers – IPR2022-00007, IPR2022-00008, IPR2022-00009, IPR2022-00010, IPR2022-00011, and IPR2022-00012. Petitions filed on October 11, 2021.

Case Numbers – IPR2022-00013, IPR2022-00014, and IPR2022-00015. Petitions filed on October 8, 2021.

Case Subject Matter – DC-to-AC converters using full-bridges, multi-level conversion for power systems, and other electronics for harvesting solar energy.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. LED Wafer Solutions LLC

Case Number – IPR2021-01554. Petition filed on September 20, 2021.

Case Number – IPR2021-01526. Petition filed on September 10, 2021.

Case Number – IPR2021-01506. Petition filed on September 7, 2021.

Case Number – IPR2021-01491. Petition filed on September 3, 2021.

Case Subject Matter – Packaging of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declarations.

Paul Hastings, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/014,846. Request filed on August 30, 2021.

Case Subject Matter – Wireless power transmission and ways to wirelessly charge and/or discharge a battery.

Work Performed – Provided expert consulting services and wrote declaration.

Jones Day (San Diego, CA and Pittsburgh, PA)

Case – *SOLiD, Inc.* v. CommScope Technologies LLC

Case Numbers – IPR2021-01390, IPR2021-01391, IPR2021-01392, IPR2021-01393, and IPR2021-01394. Petitions filed on August 12, 2021.

Case Subject Matter – Digital antenna system that enables extension of radio frequency (RF) analog signals from base stations to areas (e.g., inside of buildings) where access to such signals is inhibited.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declaration.

Unified Patents, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/019,015. Request filed on July 20, 2021.

Case Subject Matter – Voltage-controlled oscillator (VCO) temperature compensation.

Work Performed – Provided expert consulting services and wrote declaration.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – *Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC* v. Unification Technologies LLC

Case Numbers – IPR2021-00940, IPR2021-00941, and IPR2021-00942. Petitions filed on June 4, 2021.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declarations.

Hill, Kertscher & Wharton, LLP (Atlanta, GA)

Case – Kaijet Technology v. *Sanho Corporation*

Case Number – IPR2021-00886. Petition filed on April 30, 2021.

Case Subject Matter – Port extension apparatus for headphone jack, USB (Universal Serial Bus or Type-C ports), and video ports such as VGA (Video Graphics Array), DVI (Digital Visual Interface), HDMI (High-Definition Multimedia Interface), DP (Display Port), and mini-DP.

Work Performed – Provided expert consulting services for inter partes review, wrote declaration, was deposed.

O'Melveny & Myers LLP (Los Angeles, CA and New York, NY)

Case – Solas OLED LTD. v. *Samsung Electronics Co. LTD.*

Case Number – Texas, ED (Marshall) 2:21-cv-00105. Complaint filed March 22, 2021.

Case Subject Matter – Touch-sensors for gesture recognition and signal processing for capacitive touch displays.

Work Performed – Provided expert consulting services including writing declaration for claim construction.

O'Melveny & Myers LLP (San Francisco, CA)

Case – Super Interconnect Technologies LLC v. *Google LLC*

Case Number – Texas, ED (Marshall) 2:18-cv-00463 (complaint filed November 2, 2018) and Texas, WD (Waco) 6:21-cv-00259 (complaint filed March 15, 2021).

Case Subject Matter – Transmission of data and clock signals. Serial signals such as transition minimized differential signaling. Communications between processors and non-volatile storage such as Universal Flash Storage (UFS) and embedded MultiMedia Controller (eMMC).

Work Performed – Provided expert consulting services and wrote expert reports.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)

Case – Fundamental Innovation Systems International LLC v. *Anker Innovations and Fantasia Trading LLC d/b/a Ankerdirect*

Case Number – Delaware, 1:21-cv-00339. Complaint filed on March 5, 2021.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – *TCT Mobile Inc. and TCL Communication, Inc.* v. Fundamental Innovation Systems International LLC

Case Numbers – IPR2021-00597, IPR2021-00598, and IPR2021-00599. Petitions filed on February 26, 2021.

Case Number – IPR2021-00428. Petition filed on January 13, 2021.

Case Number – IPR2021-00410. Petition filed on January 11, 2021.

Case Number – IPR2021-00395. Petition filed on December 31, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declarations for inter partes reviews. Was deposed twice.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – *Samsung, Inc.* v. Pictos Technologies, Inc.

Case Number – IPR2021-00557. Petition filed on February 18, 2021.

Case Number – IPR2021-00436. Petition filed on January 19, 2021.

Case Numbers – IPR2021-00437 and IPR2021-00438. Petitions filed on January 15, 2021.

Case Subject Matter – Solid-state imaging devices including red, green, and blue pixels, data conversion circuits, and interpolation circuits. CMOS imagers including fabrication and design, active pixels, and semiconductor physics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

O'Melveny & Myers LLP (San Francisco, CA) and DLA Piper (New York, NY)

Case – Solas OLED Ltd. v. *BOE Technology Group Co. Ltd. and Samsung Electronics*

Case Number – ITC Investigation No. 337-TA-1243. Complaint filed January 5, 2021.

Case Subject Matter – Active matrix OLED display devices and components

Work Performed – Provided expert consulting services, wrote expert reports, was deposed, and testified at trial.

Paul Hastings LLP (Washington, DC)

Case – *Samsung, Inc.* v. Garrity Power Services LLC

Case Number – IPR2021-00389. Petition filed on December 31, 2020.

Case Subject Matter – Power electronics including full-bridge PWM modules for wireless power transmission using magnetic coupling via antennas and transformers. Design of inductors and coils.

Work Performed – Provided expert consulting services and wrote declaration for inter partes reviews.

Morgan, Lewis & Bockius LLP (Palo Alto, CA and Shanghai, CN)

Case – Monolithic Power Systems, Inc. v. *Meraki Integrated Circuit Technology, Inc. and Promate Electronic Company, LTD.*

Case Number – Texas, WD (Waco) 6:20-cv-00876. Complaint filed on December 24, 2020.

Case Subject Matter – Design of switching power supplies including synchronous rectification.

Work Performed – Provided expert consulting services including declaration for claim construction, trade secret analysis and declaration, and Markman tutorial.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – *Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC; Dell Technologies Inc.; Dell Inc.; and HP Inc.* v. Unification Technologies LLC

Case Numbers – IPR2021-00343, IPR2021-00344, and IPR2021-00345. Petitions filed on December 22, 2020.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services for inter partes reviews, wrote declarations, and was deposed.

Jones Day (Chicago, IL and Dallas, TX)

Case – WSOU Investments, LLC d/b/a Brazos Licensing and Development v. *Xilinx, Inc.*

Case Numbers – Delaware, 1:20-cv-01231 and Delaware, 1:20-cv-01233. Complaints filed on November 23, 2020 and September 16, 2020.

Case Subject Matter – Controlling power cycles in communication devices and transferring multiple asynchronous clock signals.

Work Performed – Provided expert consulting services, wrote claim construction declaration, wrote expert reports, and was deposed.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Cosemi Technologies, Inc. v. EverPro Technologies, Fibbr Technologies, *Logitech, Inc.*, and Facebook Technologies

Case Number – ITC Investigation No. 337-TA-1233. Complaint filed October 28, 2020.

Case Subject Matter – Data cables, including HDMI, Display Port, and USB Type A, USB Type C and USB Type A/C data cables.

Work Performed – Provided expert consulting services.

Kirkland & Ellis LLP (Boston, MA and New York, NY)

Case – Pictos Technologies, Inc. v. *Samsung Electronics Co., LTD. and Samsung Semiconductor, Inc.*

Case Number – ITC Investigation No. 337-TA-1231. Complaint filed September 25, 2020.

Case Subject Matter – Solid-state imaging devices including red, green, and blue pixels, correction of bad pixels, data conversion circuits, and interpolation circuits. CMOS imagers including fabrication and design, active pixels, and semiconductor physics.

Work Performed – Provided expert consulting services and wrote expert report.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Fundamental Innovation Systems International LLC v. *TCT Mobile Inc. and TCL Communication, Inc.*

Case Number – Delaware, 1:20-cv-00552. Complaint filed on September 11, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declarations, expert report on invalidity, and was deposed.

Walters Wilson LLP (Redwood City, CA)

Case – *Western Digital Corporation and SanDisk, LLC* v. Martin Kuster

Case Numbers – IPR2020-01410 and IPR2020-01411. Petitions filed on August 3, 2020.

Case Subject Matter – Computer connectors such as universal serial bus (USB) that connect to peripheral devices such as mice, keyboards, displays, printers, external storage, etc.

Work Performed – Provided expert consulting services for inter partes review, wrote declarations and was deposed.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – *Advanced Micro Devices, Inc.* v. Monterey Research, LLC

Case Number – IPR2020-01315. Petition filed on July 16, 2020.

Case Number – IPR2020-00985. Petition filed on May 26, 2020.

Case Subject Matter – Reading and writing to semiconductor memory such as SRAM and double data rate (DDR) DRAM. Buffer circuits with variable current supplies for controlling the rise and fall times of output signals.

Work Performed – Provided expert consulting services for inter partes review, wrote declarations and was deposed twice.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – Unification Technologies LLC v. *Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC*

Case Number – Texas, WD (Waco) 6:20-cv-00500. Complaint filed June 5, 2020.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services, wrote declaration for claim construction, and was deposed.

Ari Law, P.C. (Palo Alto, CA) and Hill, Kertscher & Wharton, LLP (Atlanta, GA)

Case – *Sanho Corporation* v. Kaijet Technology, Magic Control Technology, and Star View Global

Case Numbers – Georgia, ND (Atlanta) 1:18-cv-05385 (third amended complaint filed November 14, 2019) and Georgia, ND (Atlanta) 1:20-cv-02150 (filed May 19, 2020).

Case Subject Matter – Port extension apparatus for headphone jack, USB (Universal Serial Bus or Type-C ports), and video ports such as VGA (Video Graphics Array), DVI (Digital Visual Interface), HDMI (High-Definition Multimedia Interface), DP (Display Port), and mini-DP.

Work Performed – Provided expert consulting services, wrote declaration for claim construction, and expert reports. Was deposed and testified at trial.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Fundamental Innovation Systems International LLC v. *Coolpad Group Limited, Coolpad Technologies, Inc., and Yulong Computer Telecommunication Scientific Co. Ltd.*

Case Number – Texas, ED (Marshall) 2:20-cv-00117. Complaint filed on April 23, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declaration for claim construction.

Pillsbury Winthrop Shaw Pittman LLP (San Francisco, CA and Shanghai, China)

Case – *SMIC, Americas* v. Innovative Foundry Technologies LLC

Case Numbers – IPR2020-00837 and IPR2020-00839. Petitions filed on April 14, 2020.

Case Subject Matter – Methods of manufacturing a semiconductor component, such as a short-channel MOS device, including forming graded-junctions using spacers along the sidewalls of a transistor's gate.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declarations.

Russ August & Kabat (Los Angeles, CA)

Case – *Oyster Optics, LLC* v. Ciena Corporation

Case Number – California, ND (Oakland) 3:20-cv-02354. Complaint filed on April 7, 2020.

Case Subject Matter – Fiber optic telecommunication systems.

Work Performed – Provided expert consulting services, wrote claim construction declaration, and was deposed.