UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SILICON MOTION INC.,

Petitioner

v.

K.MIZRA LLC,

Patent Owner

U.S. PATENT NO. 10,331,379

Case IPR2024-01236

PETITION FOR INTER *PARTES* REVIEW UNDER 35 U.S.C. §312 AND 37 C.F.R. §42.104

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Exhibit No.	Description
1001	U.S. Patent No. 10,331,379
1002	File History of U.S. Patent No. 10,331,379
1003	Declaration of Dr. Baker
1004	U.S. Patent 6,185,149 ("Fujioka")
1005	U.S. Patent 6,209,056 ("Suh")
1006	U.S. Patent Application Publication 2005/0177690 ("LaBerge")
1007	European Patent Application Publication 0339224 ("Bowater")
1008	U.S. Patent No. 6,742,098 ("Halbert")
1009	U.S. Patent Application Publication 2003/0126485 ("Wilcox")
1010	U.S. Patent Application Publication 2004/0148482 ("Grundy")
1011	U.S. Patent 6,681,301 ("Mehta")
1012	U.S. Patent 5,822,772 ("Chan")
1013	U.S. Patent Application Publication 2002/0089879 ("Kobayashi")
1014	U.S. Patent 5,184,320 ("Dye")
1015	U.S. Patent 5,235,550 ("Zagar")
1016	U.S. Patent 4,707,809 ("Ando")
1017	"Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation" (June 21, 2022)

Petitioner Silicon Motion Inc. requests *inter partes* review of claims 1-22 (the "Challenged Claims") of U.S. Patent No. 10,331,379 (EX1001).

I. MANDATORY NOTICES

A. Real Party-In-Interest

Silicon Motion Inc. ("Petitioner") is the real party in interest. In the litigation identified below, Patent Owner added infringement claims against Silicon Motion Technology Corporation on July 26, 2024. Patent Owner has further alleged that Silicon Motion, Inc. a California corporation ("SM-US"), is an agent or alter ego of Petitioner, which Petitioner disputes. Petitioner's immediate parent company is Silicon Motion Technology (Hong Kong) Limited ("SMHK"). Solely out of an abundance of caution, Petitioner identifies these three related entities as real parties-in-interest, but Petitioner maintains that these entities do not satisfy the legal criteria for being real parties-in-interest. Neither SM-US nor SMHK have been sued by Patent Owner.

B. Related Matters

The '379 Patent is the subject of the following active proceeding:

- *K.Mizra LLC v. Silicon Motion Inc*, Civil Action No. 2:24-cv-00101 in the Eastern District of Texas, filed February 15, 2024.

To the best of Petitioner's knowledge, the '379 patent has not been involved in any other proceedings.

C. Counsel Service Information

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D. 37 C.F.R. §42.8(b)(4): Service Information

Petitioner consents to electronic service directed to the following email address: DLSiliconIPR379@bakerbotts.com

A Power of Attorney is filed concurrently herewith under 37 C.F.R. § 42.10(b).

II. PAYMENT OF FEES UNDER 37 C.F.R. §42.103

The Office is authorized to charge the fee set forth in 37 C.F.R. § 42.15(a) to Deposit Account No. 02-0384 as well as any additional fees that might be due in connection with this Petition.

III. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies under Rule 42.104(a) that the '379 Patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the grounds identified in this Petition.

IV. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

A. Prior Art Printed Publications

The '379 Patent claims priority to November 29, 2004.[1] Petitioner's challenge is based on the following:

U.S. Patent (USP)/U.S. Patent App. Pub. (USPAP)/European Patent Application (EP)	**Filing Date**	**Pub. Date**	**Prior Art Status**
USP 6,185,149 ("Fujioka") (EX1004)	June 28, 1999	February 6, 2001	§102(b)
USP 6,209,056 ("Suh") (EX1005)	June 30, 1997	March 27, 2001	§102 (b)
USPAP 2005/0177690 ("LaBerge") (EX1006)	February 5, 2004	August 11, 2005	§102(e)

[1] Pre-America Invents Act (pre-AIA) statutory framework applies. The '379 patent is not necessarily entitled to this priority date.

EP 0339224 ("Bowater") (EX1007)		November 2, 1989	§102 (b)
USP 6,742,098 ("Halbert") (EX1008)	October 3, 2000	May 25, 2004	§§102(a), (e)
USPAP 2003/0126485 ("Wilcox") (EX1009)	January 2, 2002	July 3, 2003	§102(b)
USPAP 2004/0148482 ("Grundy") (EX1010)	January 13, 2004	July 29, 2004	§§102(a), (e)
USP 6,681,301 ("Mehta") (EX1011)	October 2, 2001	January 20, 2004	§§102(a), (e)
USP 5,822,772 ("Chan") (EX1012)	March 22, 1996	October 13, 1998	§102 (b)
USPAP 2002/0089879 ("Kobayashi") (EX1013)	July 25, 2001	July 11, 2002	§102 (b)

B. Relief Requested

The specific grounds are set forth below and supported by the declaration of Dr. Jacob Baker (EX1003).

Ground	Challenged Claims	Reference(s)	Basis
I	1, 2, 4, 9, 10, 20, 22	LaBerge, Bowater	§103(a)
II	3, 21	LaBerge, Bowater, Suh	
III	5	LaBerge, Bowater, Halbert	
IV	6, 7	LaBerge, Bowater, Grundy	
V	8	LaBerge, Bowater, Mehta	
VI	11	LaBerge, Bowater, Chan, Kobayashi	
VII	12, 13, 15	LaBerge, Bowater, Wilcox	
VIII	14	LaBerge, Bowater, Wilcox, Suh	
IX	16	LaBerge, Bowater, Wilcox, Halbert	
X	17, 18	LaBerge, Bowater, Wilcox, Grundy	
XI	19	LaBerge, Bowater, Wilcox, Mehta	
XII	1, 20	Fujioka	

V. PERSON OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art ("POSITA") for the '379 Patent would have had a Bachelor's degree in electrical or computer engineering or a related field, and two or more years of experience in computer memory design or equivalent work experience. EX1003, ¶25. Additional education might compensate for less experience, and vice-versa. *Id.*

VI. CLAIM CONSTRUCTION

Claims in an IPR are construed under *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). 37 C.F.R. §42.100(b). No claim term requires construction beyond its ordinary and customary meaning, and no constructions are necessary to resolve this proceeding. EX1003, ¶27.

A. Means-Plus-Function

If the following are treated as means-plus-function terms, Petitioner identifies their function and corresponding structure. 37 C.F.R. § 42.104(b)(3). Petitioner's identification is a separate inquiry from whether the identified structure is definite; Petitioner reserves the right to assert the claims are alternatively indefinite. *Zillow Grp., Inc. v. Int'l Bus. Machs. Corp.*, IPR2020-01656, Paper 8 at 11 (PTAB Mar. 15, 2021); *Target Corp. v. Proxicom Wireless, LLC*, IPR2020-00931, Paper 10 at 9 (PTAB Nov. 10, 2020); *Alcon Inc. v. AMO Dev., LLC*, IPR2021-00843, Paper 15 at 15-16 (PTAB Nov. 12, 2021).

1. "circuitry" terms (claims 1, 4, 5, 7, 12, 15, 16, 18)

Claims 1 and 12 recite (1) *circuitry to provide a clock signal* and (2) *circuitry* that is *to schedule issuance of the row activation commands and the column access commands*. Claims 4 and 15 recite that *circuitry to schedule is to schedule at least one column access command for each row activation command.* Claims 5 and 16 recite that *circuitry to schedule is to schedule for a given row activation command, at least two column access commands*. Claims 7 and 18 recite *serialization/deserialization circuitry to exchange serialized data with the memory device*.

If §112(¶6) applies, the respective functions are (1) *to provide a clock signal to the memory device*, (2) *to schedule issuance of the row activation commands and the column access commands from the command interface*, (3) *schedule at least one column access command for each row activation command*, (4) *schedule for a given row activation command, at least two column access commands*, and (5) *to exchange serialized data with the memory device*. EX1003, ¶30. As best understood, the structures for each are memory controller hardware and equivalents thereof. EX1001, 30:54-34:28, 31:41-32:9, Figs. 28, 29; EX1003, ¶30.

2. "interface" terms (claims 1, 4, 6-8, 12, 15, 17-19)

Claims 1 and 12 recite (1) *a command interface to transmit* [] *row activation commands* [] *and column access commands*. Claims 4 and 15 recite (2) *the command*

interface is to transmit bank address information. Claims 6, 7, 12, 17, and 18 recite (3) *a data interface to exchange data.* Claims 8 and 19 recite (4) *a data interface to exchange each of data, and write mask values*.

If §112(¶6) applies, the respective functions are (1) *to transmit* [] *row activation commands* [] *and column access commands ,* (2) *to transmit bank address information*, (3) *to exchange data*, and (4) *to exchange each of data, and write mask values with the memory device*. EX1003, ¶32. As best understood, the structures for each are memory controller hardware and equivalents thereof. EX1001, 30:54-34:28, 31:41-32:9, Fig. 29; EX1003, ¶32.

3. "logic" term (claim 11)

Claim 11 recites *logic to time-multiplex commands from the command queues…* and *to interleave commands from the command queues*. If §112(¶6) applies, the function is *to time-multiplex commands from the command queues…* and *to interleave commands from the command queues*. EX1003, ¶33. As best understood, the structure is memory controller hardware and equivalents thereof. EX1001, 30:54-34:28, 31:41-32:9, Fig. 29; EX1003, ¶33.

VII. FILE HISTORY

The '379 patent issued after a single office action and response. EX1002, 265, 273. Had the examiner had the benefit of the grounds herein, the patent would never have issued.

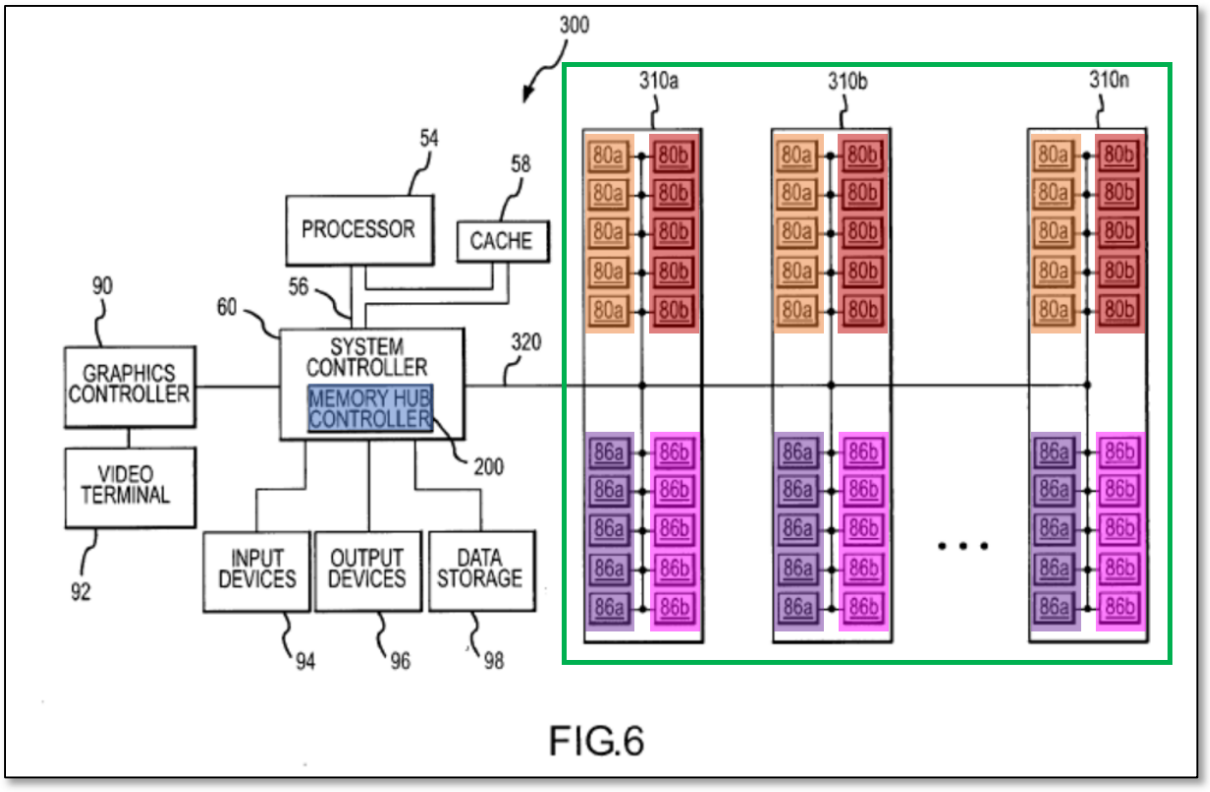
VIII. SPECIFIC GROUNDS FOR PETITION

A. Ground I: LaBerge and Bowater render claims 1, 2, 4, 9, 10, 20, and 22 obvious

1. Claim 1

a. [1a]

If the preamble is limiting, LaBerge discloses it or at least renders it obvious. LaBerge's memory hub controller 200 (*A memory controller*) controls memory of memory modules 310a, 310b,…310n using "command and address signals" (*to control a memory device*). EX1006 (LaBerge), ¶0039, Fig. 6.



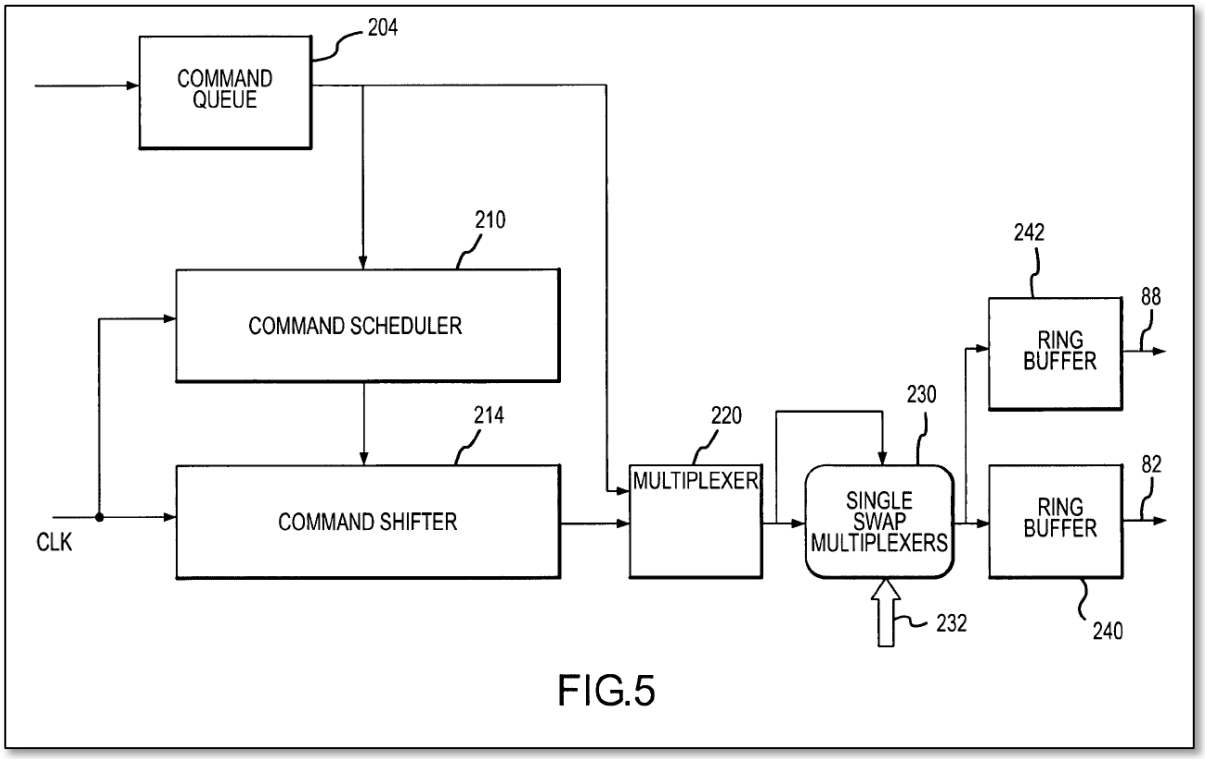
EX1006, Fig. 6 (annotated)

Within memory modules 310a, 310b,…310n (*the memory device*), each of memory modules 310a, 310b,…310n respectively includes a group of memory devices formed by devices 80a, 86a, 80b, and 86b, meaning memory modules 310a, 310b,…310n (*the memory device*) include a plurality of groups formed by devices 80a, 86a, 80b, and 86b (*having a plurality of bank groups*), as shown in annotated Figure 6. *Id.* A POSITA would have understood or at least found obvious that memory devices 80a, 86a, 80b, and 86b each form a respective memory bank, and that the group of memory devices 80a, 86a, 80b, and 86b in each module 310 is therefore a *bank group*, with the plurality the groups of memory devices 80a, 86a, 80b, and 86b in each of modules 310a, 310b,…310n forming *a plurality of bank groups*. *Id.*; EX1003, ¶55. This is because memory banks are known as being groups of memory devices, just like the devices 80a, 86a, 80b, and 86b across modules 310. EX1003, ¶55. LaBerge further discloses using bank addresses BA0, BA1, BA2, and BA3, showing that a POSITA would have understood or at least found obvious that devices 80a, 86a, 80b, and 86b are each addressed as a bank. EX1006, ¶0029; EX1003, ¶55.

b. [1b]

LaBerge's memory hub controller 200 (*the memory controller*) includes "clock signals CLK0, CLK1, CLKZ0, and CLKZ1" (*a clock signal*) that drive ring buffers 240 and 242 and are also "applied to the memory devices 80, 86" of memory

modules 310 (*provide a clock signal to the memory device*). EX1006, ¶¶0038-0039, Figs. 5 (clock signal "CLK" in memory hub controller 200), 6.



EX1006, Fig. 5

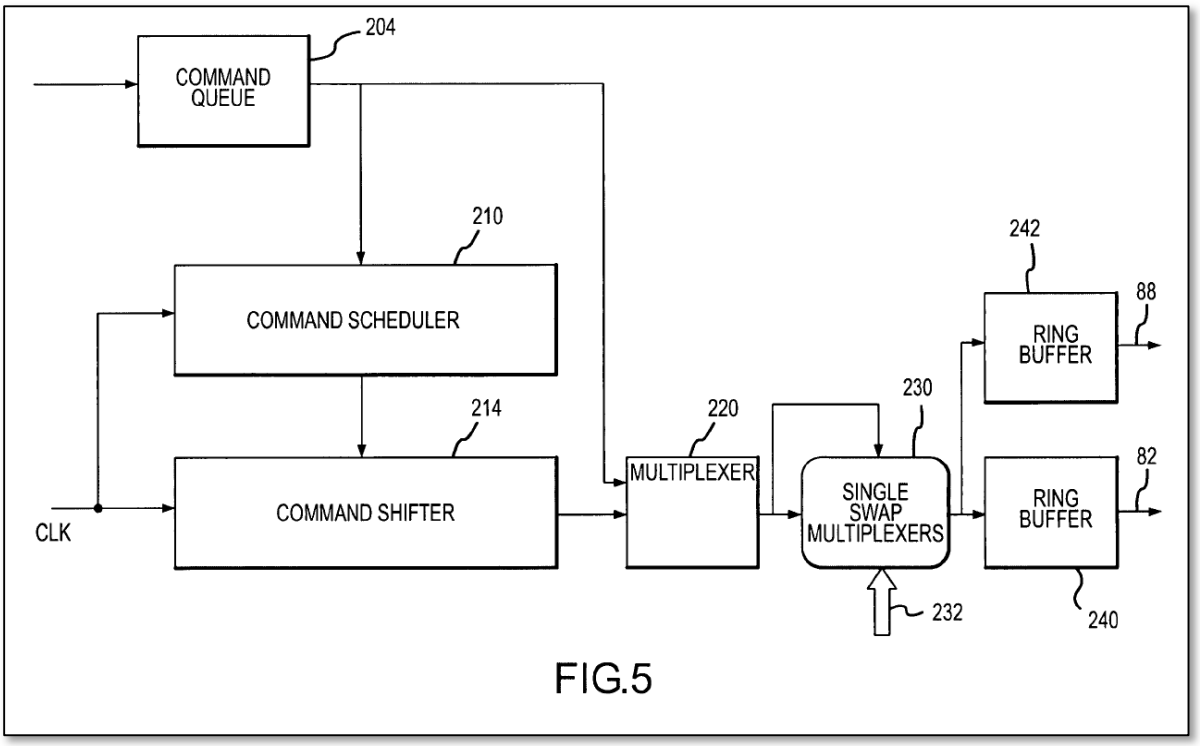
A POSITA would have understood or at least found obvious that memory hub controller 200 comprises circuitry that provides the clock signals to memory devices 80 and 86 of memory modules 310 (*memory controller comprising: circuitry to provide a clock signal to the memory device*) because such circuitry is needed to generate and/or receive such clock signals and provide them to memory devices 80 and 86 of memory modules 310. *Id.*; EX1003, ¶57. A POSITA would have further understood or at least found obvious that the clock signals CLK0, CLK1, CLKZ0, and CLKZ1 have clock transitions between low and high states (*the clock signal*

having clock transitions) because this was the well-known way in which clock signals were implemented. *Id.*; EX1003, ¶58.

If *circuitry to provide a clock signal* is interpreted under §112(¶6), LaBerge discloses or at least renders obvious (1) the identified function for the reasons discussed above, and (2) the identified structure of memory controller hardware and equivalents thereof (Section VI.A.1, *supra*) because it describes circuitry of memory hub controller 200 that handles and provides clock signals to memory devices. Further, the circuitry of memory hub controller 200 is at least an equivalent to memory controller hardware because both perform the same functionality of *provid[ing] a clock signal to the memory device* in substantially the same way, i.e., by outputting a clock signal. *Kemco Sales, Inc. v. Control Papers Co., Inc.*, 208 F.3d 1352, 1364 (Fed. Cir. 2000). A POSITA would have further recognized the interchangeability of LaBerge's circuitry of memory hub controller 200 with the identified structure as both are used to provide a clock signal, and such interchangeability would have been routine and well-within the capabilities of a POSITA for the same reasons. EX1003, ¶59. Moreover, LaBerge's circuitry of memory hub controller 200 is not excluded by any explicit definition in the '379 patent's specification for an equivalent to the identified structure. *Id.*

c. [1c]

LaBerge's memory controller 200 (*the memory controller*) includes command shifter 214, multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242, which collectively form a *command interface* as they provide an interface via which command and address signals are transmitted from memory controller 200 to memory devices 80 and 86 of memory modules 310a-310n. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1003, ¶60.



EX1006, Fig. 5

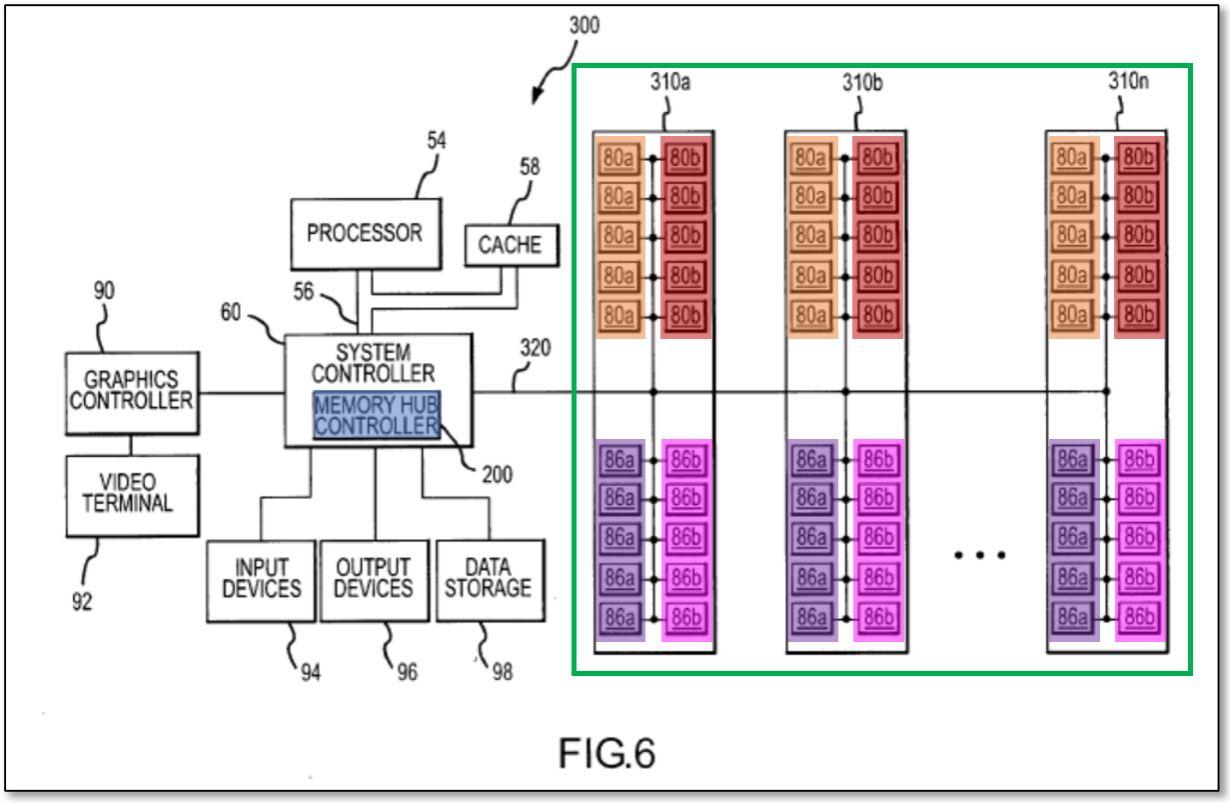


FIG.6

EX1006, Fig. 6 (annotated)

Specifically, multiplexor 220 receives at its input, from command shifter 214, "properly timed and ordered command and address signals," and also "receives the DRAM command and address signals at a second input directly from the Command Queue 204." *Id.*, ¶0036, Fig. 5. These command and address signals are output by multiplexor 220 to single swap multiplexors 230, which routes them to ring buffers 240 and 242. *Id.*, ¶¶0037-0038, Fig. 5. Ring buffers then send the command and address signals to memory devices 80 and 86, via bus 320, depending on which memory device is being accessed and whether the memory device is operating in DDR2 or DDR3 mode. *Id.*, ¶¶0038-0039, Figs. 5, 6.

The command and address signals include "DRAM command signals" such as "RASZ," which is a "row address strobe" signal and known as being used to activate rows of memory, and "CASZ," which is a "column address strobe" signal and known as being used to access columns of memory. EX1006, ¶¶0029, 0034-0036; *id.*, ¶0003 (referring to RAS and CAS signals as "command" signals); EX1003, ¶62. Thus, LaBerge describes its command shifter 214, multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242 (*command interface*) transmit to memory devices 80 and 86 of memory modules 310a-310n (*transmit, to the memory device*) RASZ signals that instruct the memory devices to activate desired memory rows and CASZ signals that instruct the memory devices to allow access to desired memory columns (*row activation commands to instruct row activations and column access commands to instruct column accesses*). EX1006, ¶¶0034-0039, Figs. 5, 6; EX1003, ¶63.

If *a command interface to transmit…*is interpreted under §112(¶6), LaBerge discloses or at least renders obvious (1) the identified function for the same reasons discussed above and (2) the identified structure of memory controller hardware and equivalents thereof (Section VI.A.2, *supra*) because it describes memory controller hardware in the form of shifter 214, multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242 as discussed above. Further, multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242 form at least an equivalent

because they perform the same functionality of *transmit[ting], to the memory device, row activation commands…and column access commands* in substantially the same way, i.e., by transmitting row activation commands and column access commands to memory banks. *Kemco Sales*, 208 F.3d at 1364. A POSITA would have further recognized the interchangeability of LaBerge's multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242 with the identified structure as both are simply used to transmit row activation commands and column access commands to memory banks, and such interchangeability would have been routine and well-within the capabilities of a POSITA for the same reasons. EX1003, ¶64. Moreover, these components are not excluded by any explicit definition in the '379 patent's specification for an equivalent to the identified structure. *Id.*

d. [1d]

LaBerge's memory controller 200 (*the memory controller*) includes command scheduler 210 (*circuitry to schedule*), which "spaces the command and address signals apart from each other with the proper delay." EX1006, ¶0035, Figs. 5, 6; *id.*, ¶0034 ("memory controller 200…schedules the DRAM commands").

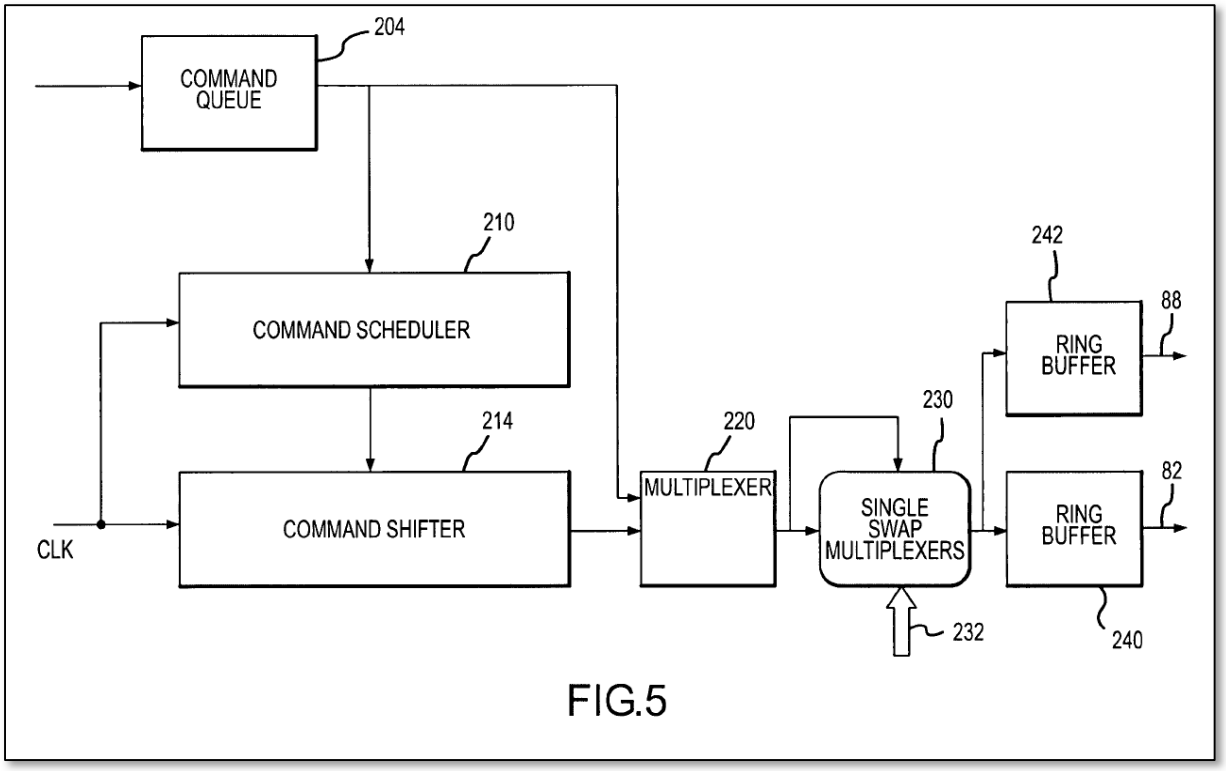


FIG.5

EX1006, Fig. 5

LaBerge explains that "delay is measured in periods of the clock CLK signal" and that, in one example, "Command Scheduler 210 might schedule[] the CASZ to be output three clock periods after the RASZ signals [were] [] output from the Command Scheduler 210." *Id.*, ¶¶0034-0035. Command scheduler 210 outputs the scheduled RASZ and CASZ commands to shifter 214, which outputs them to multiplexor 220; the signals are then sent to single swap multiplexers 230 and then to buffers 240 and 242 for output to memory devices 80 and 86. *Id.*, ¶¶0034-0039, Figs. 5, 6. LaBerge therefore describes that command scheduler 210 schedules (*circuitry to schedule*) issuance of the RASZ and CASZ signals (*issuance of the row activation commands and the column access commands*) from command shifter 214,

multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242 (*from the command interface*). *Id.*; EX1003, ¶66.

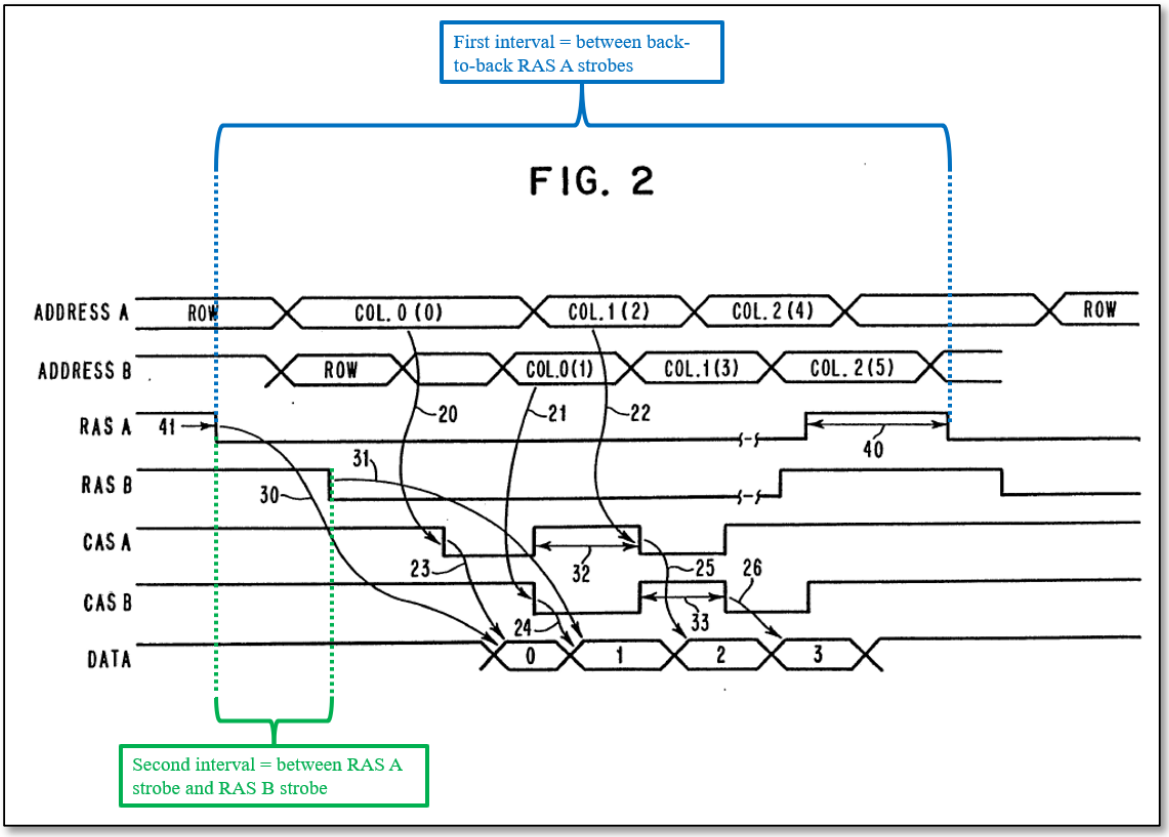
If *circuitry to schedule issuance…*is interpreted under §112(¶6), LaBerge discloses or at least renders obvious (1) the identified function for the same reasons discussed above and (2) the identified structure of memory controller hardware and equivalents thereof (Section VI.A.1, *supra*) because it teaches memory controller hardware in the form of command scheduler 210 as discussed above. EX1003, ¶67. Moreover, command scheduler 210 is part of memory controller 200, and a POSITA would have understood or at least found obvious that it is formed by circuitry. *Id*. Memory controller 200 is implemented by "circuits" that perform the described functionality. EX1006, ¶0041. Further, command scheduler 210 forms at least an equivalent because it performs the same functionality of *schedule[ing] issuance of the row activation commands and the column access commands from the command interface* in substantially the same way, i.e., by determining the appropriate timing by which commands are to be sent. *Kemco Sales*, 208 F.3d at 1364. A POSITA would have further recognized the interchangeability of LaBerge's command scheduler 210 with the identified structure as both are simply used to schedule such commands, and such interchangeability would have been routine and well-within the capabilities of a POSITA for the same reasons. EX1003, ¶67. Moreover,

LaBerge's command scheduler 210 is not excluded by any explicit definition in the '379 patent's specification for an equivalent to the identified structure. *Id.*

e. [1e]

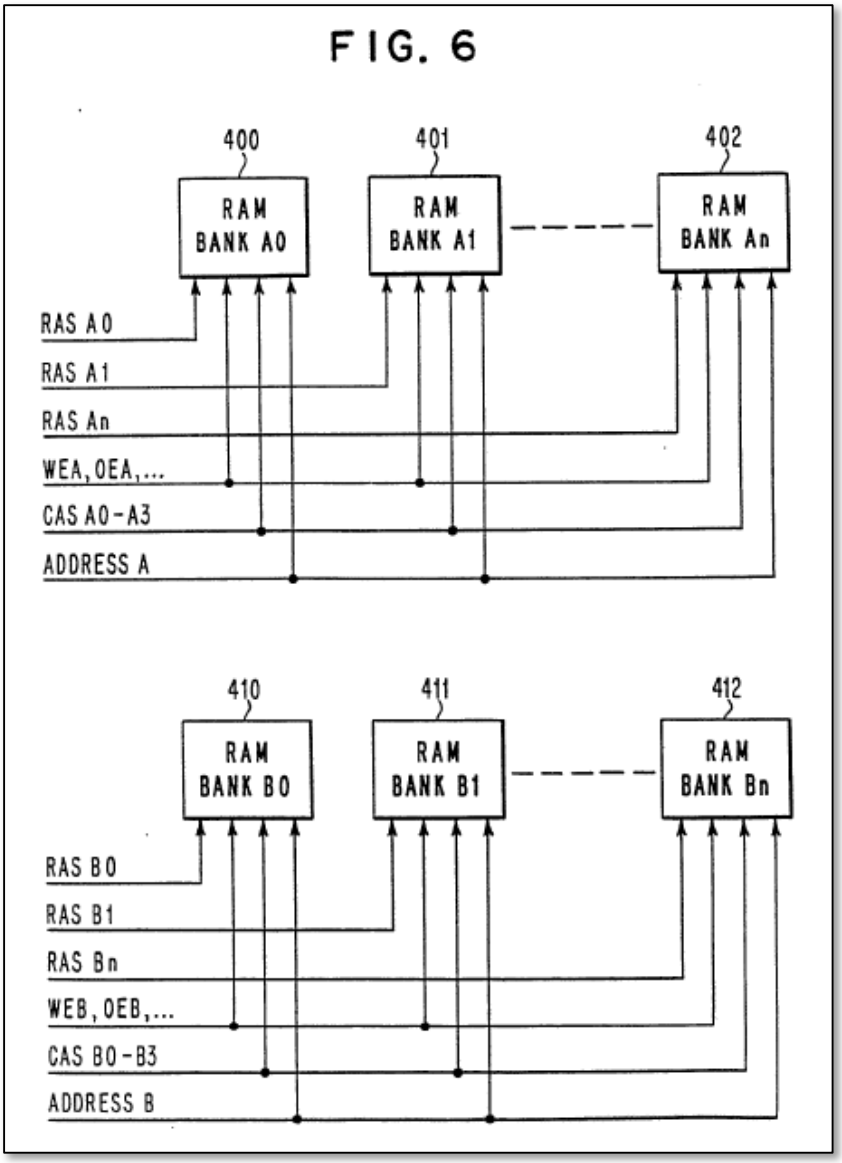
LaBerge's command scheduler 210 (*circuitry to schedule*) schedules CASZ commands, as well as RASZ commands (*row activations*) for output to memory devices 80 and 86. Sections VIII.A.1.c-d. EX1003, ¶¶68-69. Bowater teaches a "memory controller" that controls "several different banks of memory," where "memory accesses are modified for each bank in order to maintain optimum performance." *Id.*; EX1007, 4:13-15, Fig. 2. Figure 2 shows a timing diagram of control signals issued by Bowater's memory controller, including "address signals, RAS signals, CAS signals, and data signals," where "cycle time of these control signals are dynamically modified to change the RAS access time and precharge time, and the CAS access time and precharge time." *Id.*, 4:19-24, Fig. 2.

As shown by Figure 2, Bowater's memory controller issues back-to-back RAS A commands over an interval shown in annotated Figure 2 below. EX1007, 4:13-40, Fig. 2.



EX1007, Fig. 2 (annotated)

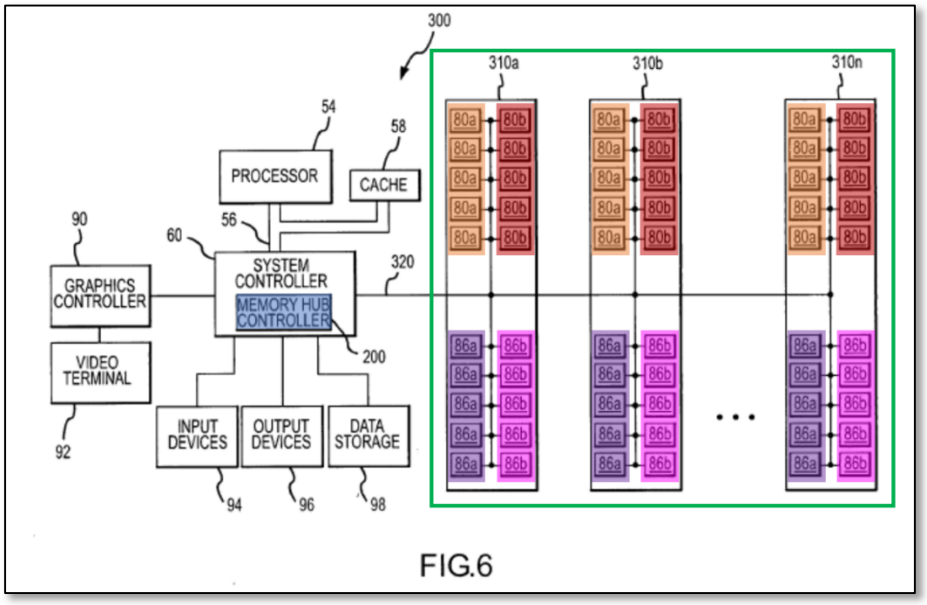
Figure 6 below shows that these RAS A commands are row activations to rows within banks A0-An of the bank A group. *Id.*, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6; *id.*, 7:2-3.



EX1007, Fig. 6

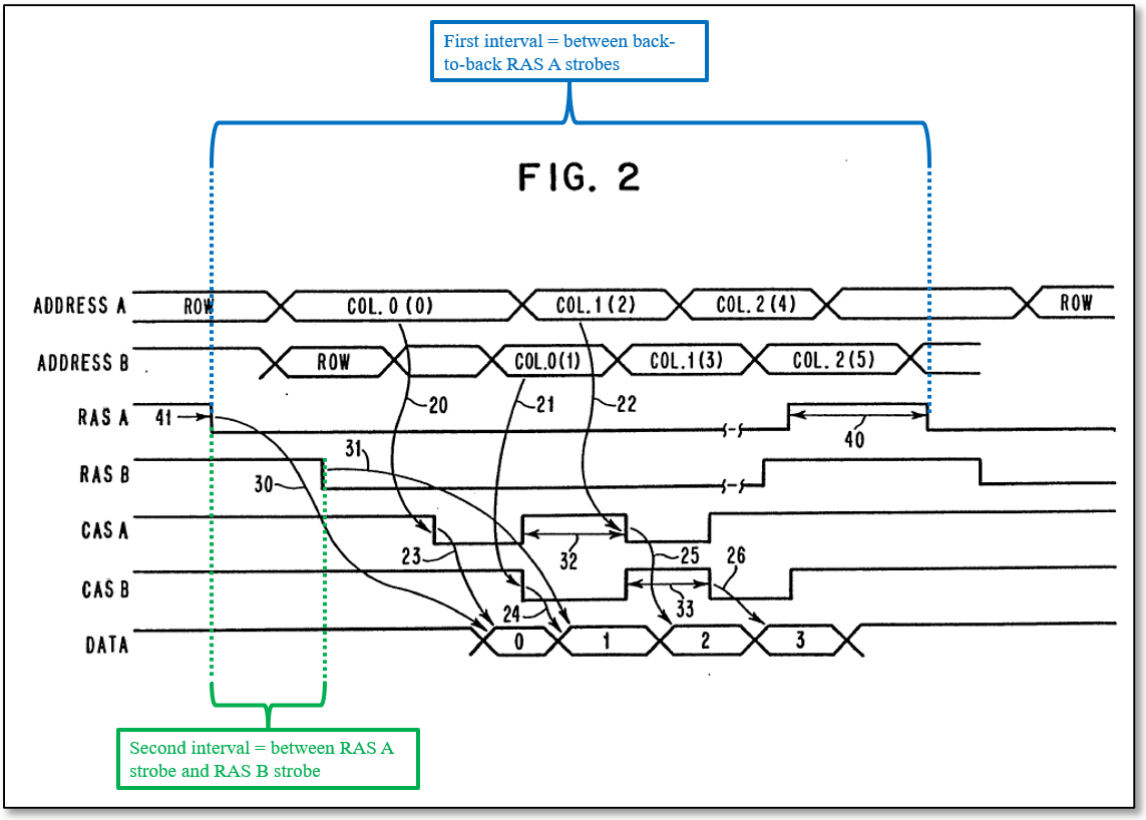
Bowater's memory controller also issues RAS B commands which are row activations to rows within banks B0-Bn of the bank B group. *Id.* Bowater's process is for "two memory banks being interleaved"—bank A and bank B. *Id.*; EX1003, ¶70.

Thus, as combined with LaBerge, Bowater's RAS A commands would have been applied to banks within a common bank group formed of memory devices 80a, 86a, 80b, and 86b in a module 310a (*bank group*) of LaBerge, while RAS B commands would have been applied to banks within another common bank group formed of memory devices 80a, 86a, 80b, and 86b in a module 310b (another *bank group*) of LaBerge. *See* Section VIII.A.1.a (each of LaBerge's devices 80a, 86a, 80b, and 86b is a *bank*, and the collection of devices 80a, 86a, 80b, and 86b in each module 310 is a *bank group*); EX1003, ¶¶70-71. Such commands would have been applied by LaBerge's memory controller 200 "to the signal lines of bus 320 depending on which memory devices 80a, 86a, 80b or 86b [banks] are being accessed." EX1006, ¶0039; EX1003, ¶71.



EX1006, Fig. 6 (annotated)

Thus, in the LaBerge-Bowater combined system, LaBerge's command scheduler 210 (*circuitry to schedule*) would have scheduled issuance of the RAS and CAS commands such that a first interval of clock transitions to transpire between back-to-back RAS A commands to banks within a common bank group formed of memory devices 80a, 86a, 80b, and 86b in **module 310a** is provided (*a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common bank group*) and a second interval of clock transitions to transpire between back-to-back row activations to banks within different bank groups—i.e, row activation using RAS A to memory devices 80a, 86a, 80b, and 86b in **module 310a** and a subsequent row activation using RAS B to memory devices 80a, 86a, 80b, and 86b in **module 310b**—is provided (*second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups*), as shown by Figure 2 below. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6; EX1003, ¶72.



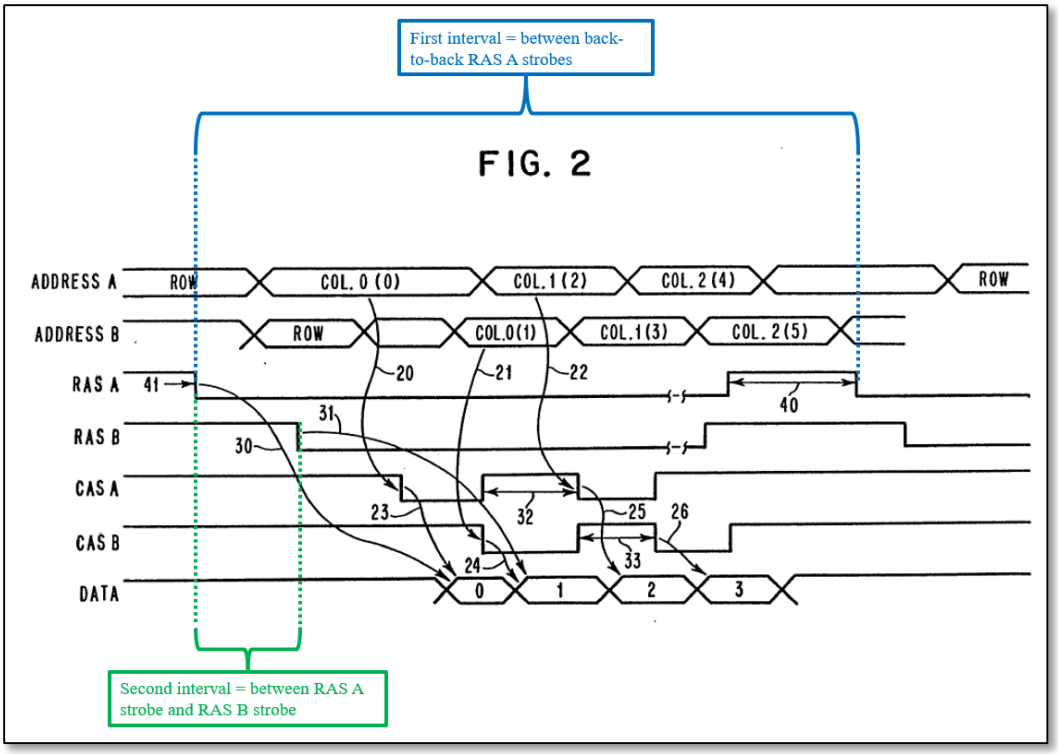
EX1007, Fig. 2 (annotated)

As shown by Figure 2, the first interval is *longer* than the second interval. *Id.* Moreover, a POSITA would have understood or at least found obvious that the claimed intervals are defined by "*clock transitions*" because LaBerge explicitly explains that timing of its CAS and RAS signals are defined by "periods of the clock CLK signal" and that "clock periods" define intervals between signals. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1003, ¶73. And defining intervals as clock transitions was well-known in the art. *Id.*

Motivation to Combine

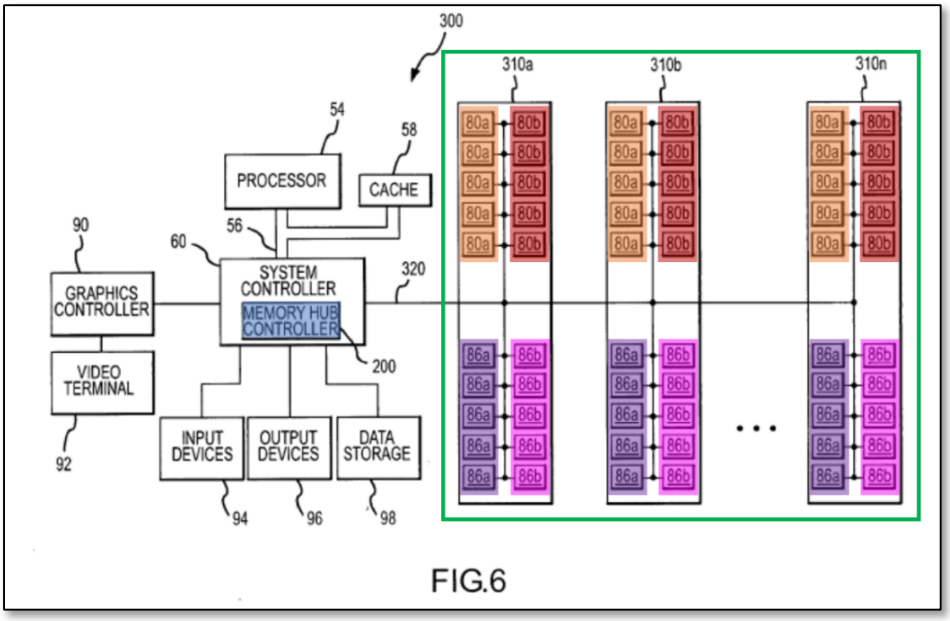
A POSITA would have been motivated to combine LaBerge and Bowater such that LaBerge's command scheduler 210 schedules RAS and CAS commands as taught by Bowater. EX1003, ¶74. The combination would have enhanced LaBerge's system by providing increased flexibility and an additional technique by which RAS and CAS commands are scheduled and would have been nothing more than a design choice implemented by a POSITA. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6; EX1003, ¶74.

Combined, LaBerge's command scheduler 210 would have scheduled commands as taught by Bowater, including with the timing of Bowater's Figure 2, and would have transmitted commands, as taught by Bowater, via LaBerge's memory bus 320. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6; EX1003, ¶75. Such a combination would have been routine and straightforward to POSITAs. *Id.*



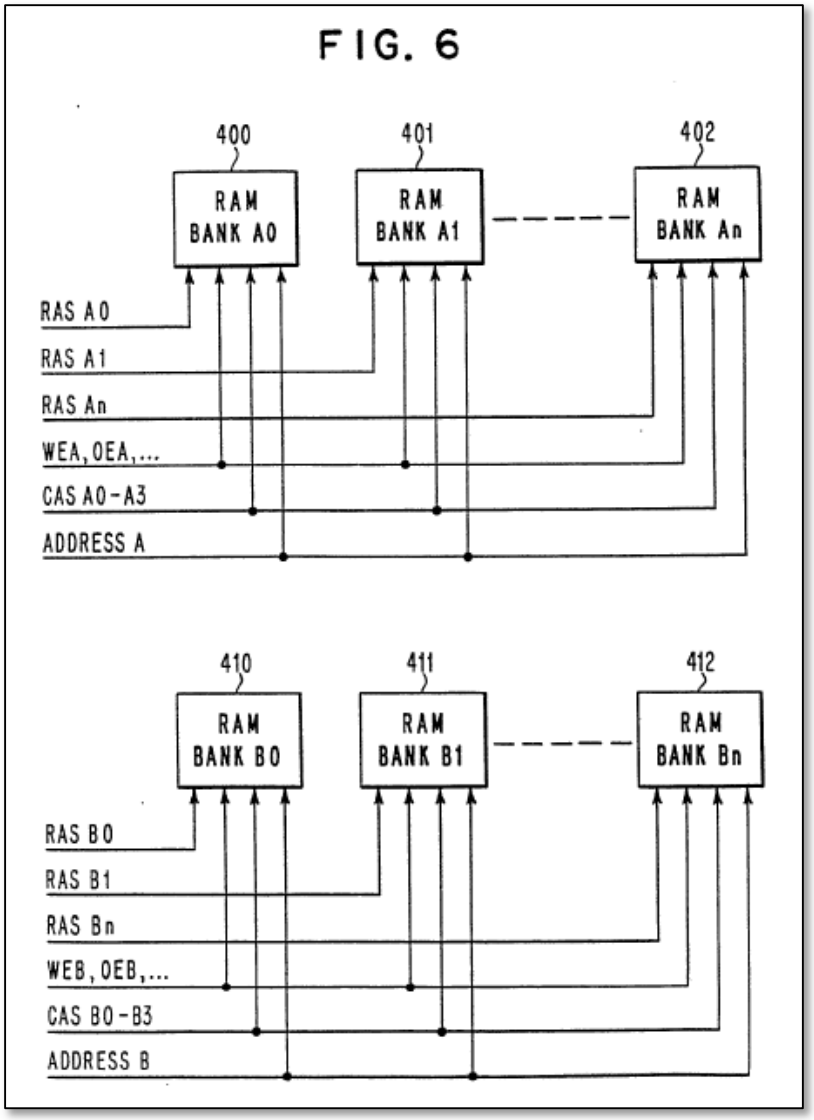
EX1007, Fig. 2 (annotated)

LaBerge already describes that "memory controller 200 applies command and address signals…to the signal lines of the bus 320 depending on which memory devices 80a, 86a, 80b or 86b are being accessed." EX1006, ¶0039. Each of memory devices 80a, 86a, 80b or 86b is a bank, and the collection of devices 80a, 86a, 80b, and 86b in each module 310 is a bank group. *See* Section VIII.A.1.a. LaBerge already describes that command scheduler 210 of memory controller 200 schedules RAS and CAS commands, such as where one is delayed by a number of clock cycles relative to the other. EX1006, ¶¶0034-0039, Figs. 5, 6.



EX1006, Fig. 6 (annotated)

Bowater, applicable to LaBerge as it similarly is directed to controlling memory using RAS and CAS commends, teaches that a memory controller may dynamically access memory using RAS and CAS commands to banks in a particular group—banks A0 to An in a bank A group, and banks B0-Bn in a bank B group—via the technique of the timing diagram in Figure 2, where such commands are controlled to occur at certain times. EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6; EX1003, ¶¶76-77.



EX1007, Fig. 6

Bowater explains that its system provides "a dynamic memory controller to permit more flexibility than has been provided in available memory controllers," where "[m]emory attributes related to row address strobe (RAS) and column address strobe (CAS) have been made programmable" which "allows the speed of memory access to be altered." EX1007, 3:35-38; *id*, 3:5-18 (describing a "flexible dynamic memory

controller" that "allows extra delays on signals" that are "dynamically determined by the memory controller"). Bowater is explicitly directed to a memory controller that determines timing of its RAS and CAS signals and schedules them, i.e., by allowing extra delay, as needed. *Id.*; *id.*, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6; EX1003, ¶78.

Enhancing LaBerge with Bowater would have therefore been straightforward and well-within the capabilities of POSITAs, and simply provided a design choice as to how LaBerge's system is implemented. EX1003, ¶79. Bowater teaches a design choice as to how, within the context of signals transmitted to different banks within a bank group (e.g., signals to banks A0-An in a common bank group A; signals to banks B0-Bn in a common bank group B), CAS are scheduled relative to each other and RAS are scheduled relative to each other—again, a straightforward and routine matter for POSITAs due to the fact that LaBerge already discloses command scheduler 210 scheduling CAS and RAS commands and transmitting them to devices 80a, 86a, 80b, an 86b of modules 310 (i.e., 310a, 310b) via bus 320 "depending on which" device is being accessed. *Id.*; EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6.

A POSITA would have combined LaBerge and Bowater as above using known hardware and software techniques associated with memory devices, and for the same reasons discussed above, a POSITA would have readily combined

Bowater's teachings with LaBerge. EX1003, ¶80. And separate or combined, the LaBerge and Bowater systems would have both performed the same memory and data storage functionality. *Id.*

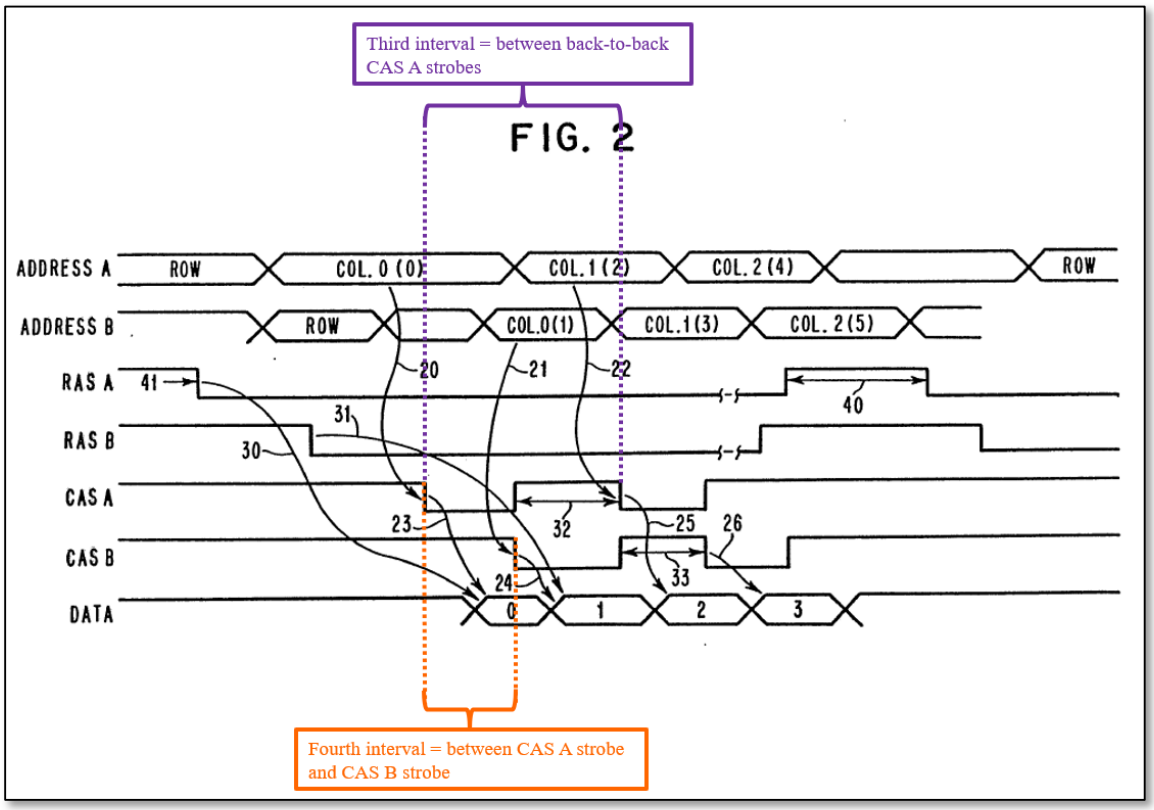
The combination would have further been predictable, straightforward, and routine for a POSITA, and a POSITA would have recognized as much. EX1003, ¶80. And a POSITA would have had a reasonable expectation of success in making this combination for the same reasons discussed above, and also due to the similarities of both references, where both references are at least directed to memory controllers that use RAS and CAS commands to access memory. *Id.*; EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 3:35-46, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6.

Additionally, both LaBerge and Bowater are analogous art to the '379 patent, from the same field of endeavor as the patent (e.g., memory systems) and reasonably pertinent to the particular problem the patent was trying to solve (e.g., improving memory performance). EX1001, Abstract, 1:28-29, 4:1-20; EX1006, Abstract, ¶¶0001, 0013-0014; EX1007, Abstract, 2:1-2, 3:5-18, 9:53-10:8; EX1003, ¶81.

f. [1f]

LaBerge's command scheduler 210 (*circuitry to schedule*) schedules CASZ commands (*column accesses*) and RASZ commands for output to memory devices 80 and 86. Sections VIII.A.1.c-d; EX1003, ¶¶82-83. Bowater teaches a "memory controller" and Figure 2 shows a timing diagram of controls signals issued by

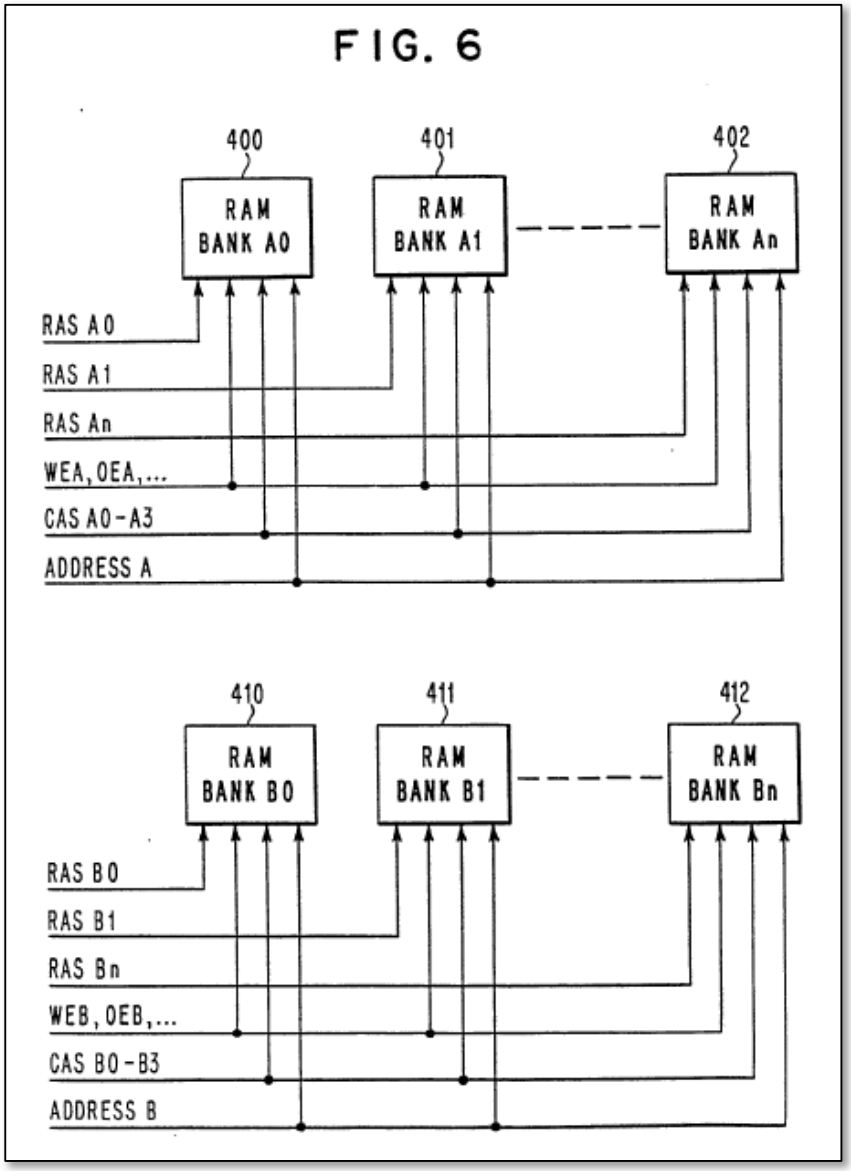
Bowater's memory controller as discussed in Section VIII.A.1.e. Bowater's memory controller issues back-to-back CAS A commands over an interval shown in annotated Figure 2 below. EX1007, 4:13-40, Fig. 2; Section VIII.A.1.e.



EX1007, Fig. 2 (annotated)

As shown by Figure 6 below, the CAS A commands are column accesses to columns within banks A0-An of the bank A group. EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6; *id.*, 7:2-3. Bowater's memory controller also issues CAS B commands which are columns accesses to columns within banks B0-Bn of the bank B group. *Id.*

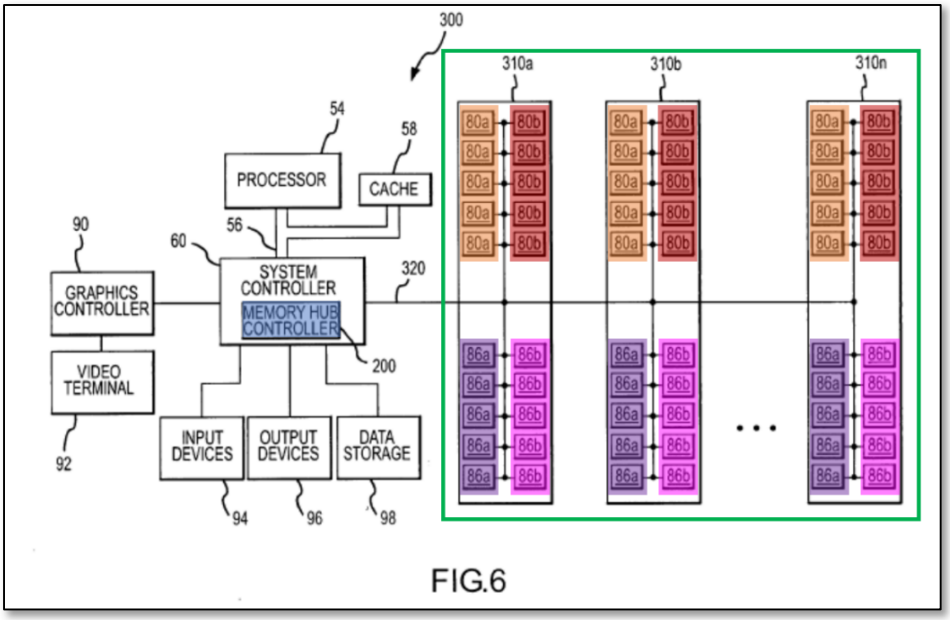
Bowater's process is for "two memory banks being interleaved"—bank A and bank B. *Id.*; EX1003, ¶84.



EX1007, Fig. 6

As combined with LaBerge, such CAS A commands would have been applied to banks within a common bank group formed of memory devices 80a, 86a, 80b, and

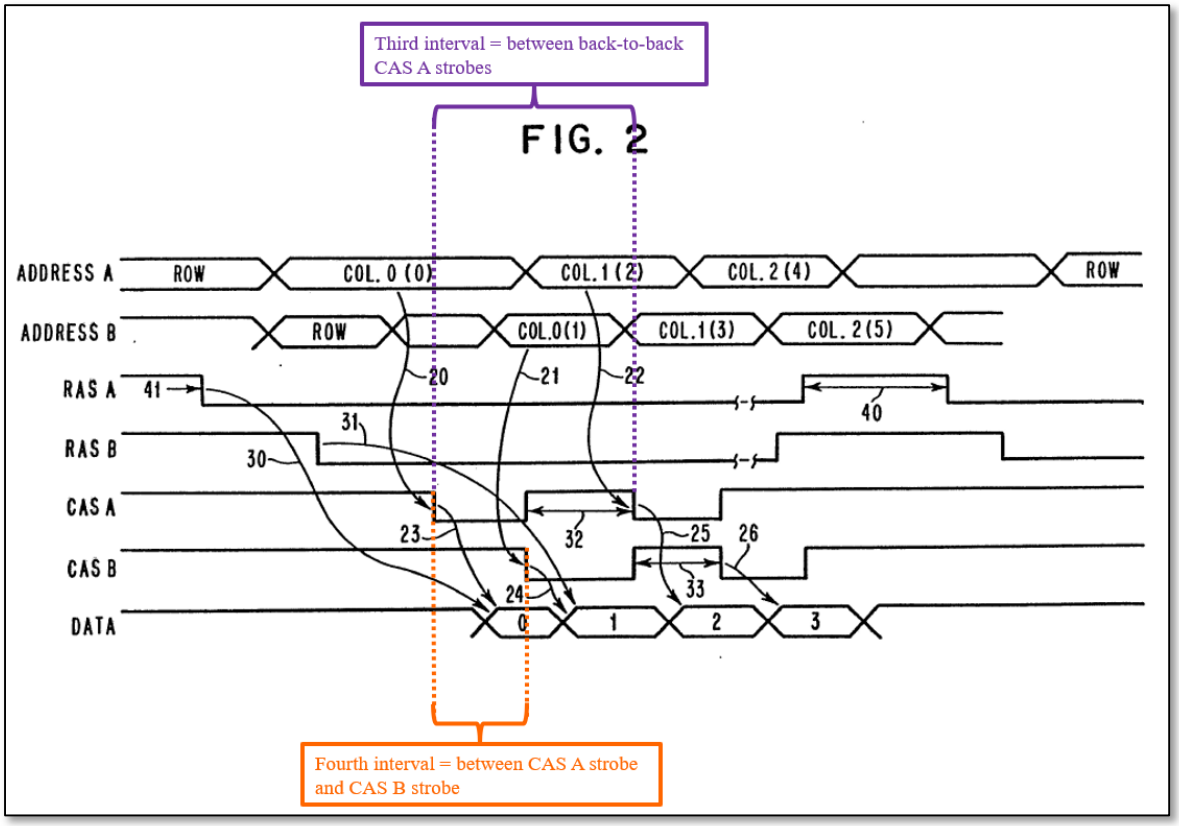
86b in a **module 310a** (*bank group*) of LaBerge, while CAS B commands would have been applied to banks within another common bank group formed of memory devices 80a, 86a, 80b, and 86b in a **module 310b** (another *bank group*) of LaBerge. Section VIII.A.1.a (each of devices 80a, 86a, 80b, and 86b is a *bank*, and the collection of devices 80a, 86a, 80b, and 86b in each module 310 is a *bank group*); EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6; EX1003, ¶85. Such commands would have been applied by LaBerge's memory controller 200 "to the signal lines of bus 320 depending on which memory devices 80a, 86a, 80b or 86b [banks] are being accessed." *Id.*; EX1006, ¶0039.



EX1006, Fig. 6 (annotated)

Thus, in the LaBerge-Bowater combined system, LaBerge's command scheduler 210 (*circuitry to schedule*) would have scheduled issuance of the RAS and

CAS commands such that a third interval of clock transitions to transpire between back-to-back CAS A commands to banks within a common bank group formed of memory devices 80a, 86a, 80b, and 86b in **module 310a** is provided (*a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group*) and a fourth interval of clock transitions to transpire between back-to-back column activations to banks within different bank groups—i.e, column access using CAS A to memory devices 80a, 86a, 80b, and 86b in **module 310a** and a subsequent column access using CAS B to memory devices 80a, 86a, 80b, and 86b in **module 310b**—is provided (*a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups*) as shown by Figure 2 below. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 4:13-40, 6:32-50, 7:1-13, Figs. 2, 4, 6; EX1003, ¶¶86-87.



EX1007, Fig. 2 (annotated)

As shown by Figure 2, the third interval is *longer* than the fourth interval. *Id.* Moreover, a POSITA would have understood or at least found obvious that the claimed intervals are defined by "*clock transitions*" because LaBerge explicitly explains that timing of its CAS and RAS signals are defined by "periods of the clock CLK signal" and that "clock periods" define intervals between signals. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1003, ¶87. Moreover, defining intervals in such a manner is well-known in the art. *Id.*

A POSITA would have been motivated to combine LaBerge and Bowater for the reasons discussed in Section VIII.A.1.e. EX1003, ¶88.

2. Claim 2

LaBerge's group of memory devices 80a across the memory modules 310a, 310b…310n (*bank*) includes a first memory device 80a (*includes a first sub-bank*) located in memory module 310a and a second memory device 80a (*and a second sub-bank*) located in memory module 310b, as shown in annotated Figure 6 below. EX1006, ¶¶0034-0039, Fig. 6; EX1003, ¶89.

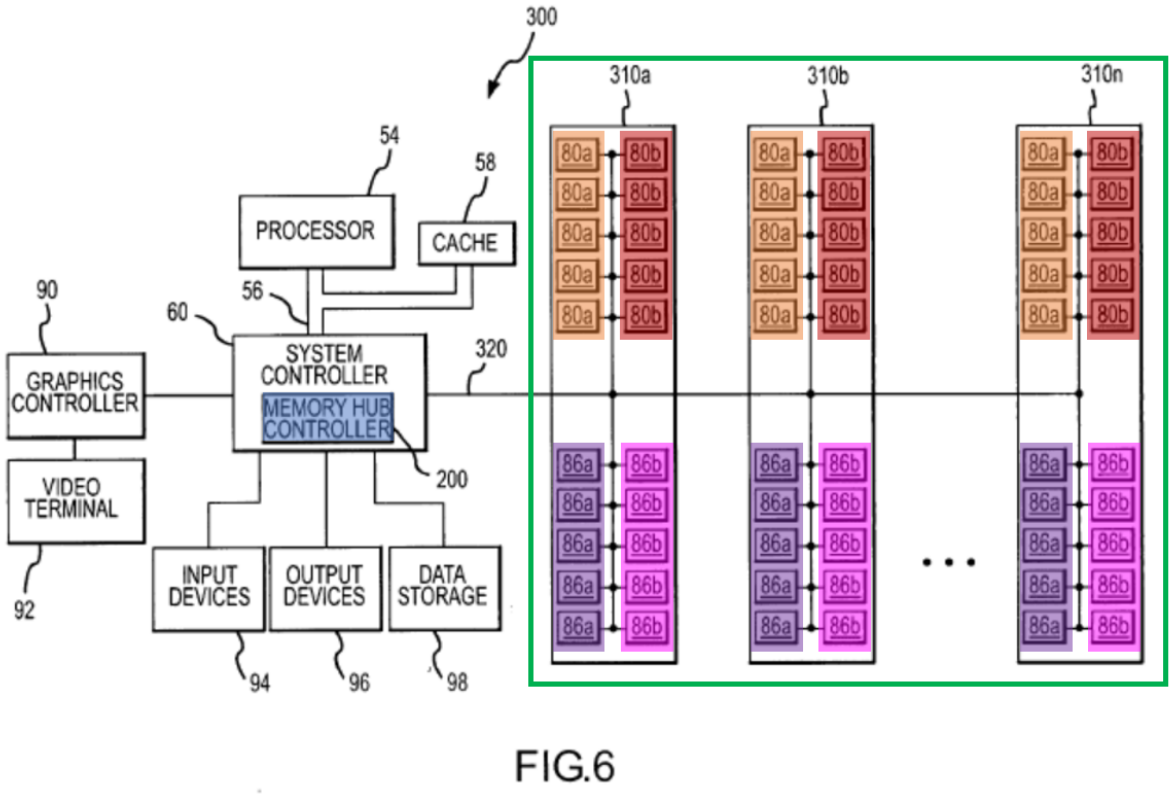


FIG.6

EX1006, Fig. 6 (annotated)

The same organization is true for each other group of memory devices 80b, 86a, and 86b, providing that *each bank includes a first sub-bank and a second sub-bank. Id.*; EX1003, ¶90.

The first memory device 80a in memory module 310a (*first sub-bank*) is in a first group formed by memory devices 80a, 86a, 80b, and 86b in module 310a (*is in a first bank group*) out of the multiple groups formed by memory devices 80a, 86a, 80b, and 86b in modules 310a, 310b,…310n (*of the plurality of bank groups*), and the second memory device 80a in memory module 310b (*second sub-bank*) is in a second group formed by memory devices 80a, 86a, 80b, and 86b in module 310b (*is in a second bank group*) out of the multiple groups formed by memory devices 80a, 86a, 80b, and 86b in modules 310a, 310b,…310n (*of the plurality of bank groups*), as shown in annotated Figure 6 below. EX1006, ¶¶0034-0039, Fig. 6; EX1003, ¶91.

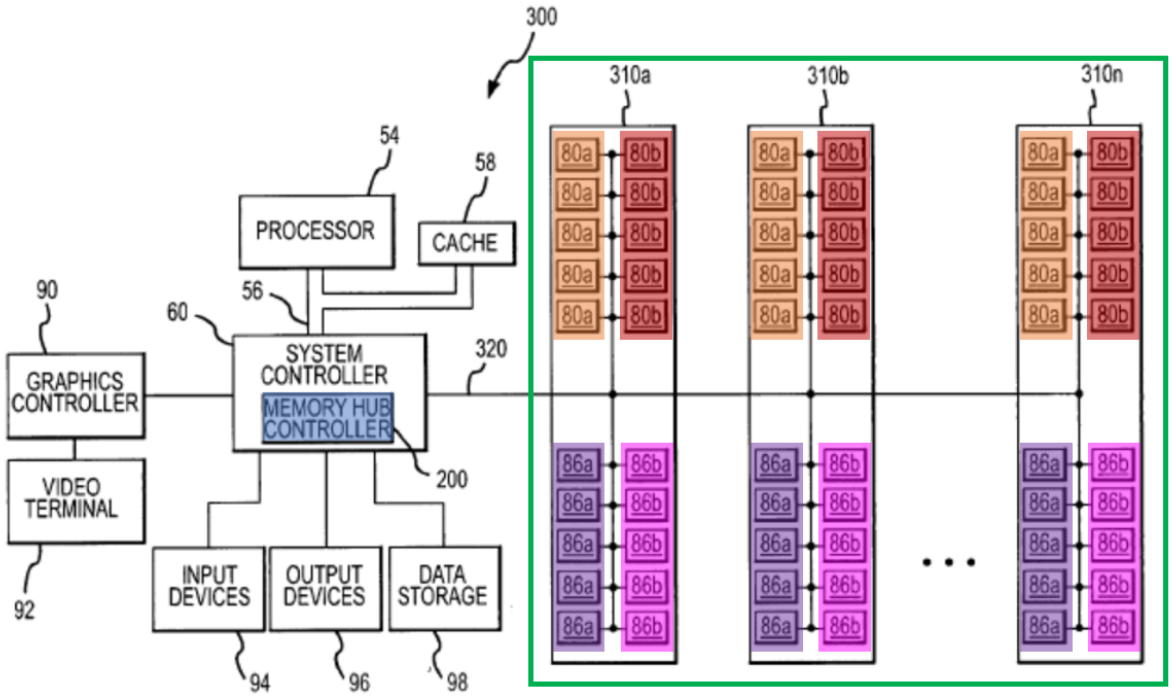


FIG.6

EX1006, Fig. 6 (annotated)

The same organization is true for each of memory devices 80b, 86a, and 86b, providing that *the first sub-bank is in a first bank group of the plurality of bank groups; and the second sub-bank is in a second bank group of the plurality of bank groups*. *Id.*; EX1003, ¶92.

3. Claim 4

LaBerge's command scheduler 210 (*circuitry to schedule*) schedules output of CASZ and RASZ DRAM commands. EX1006, ¶¶0034-0035, Figs. 5, 6. Table 1 of LaBerge shows that for memory devices 80a[2] and 86a, the signals sent by memory controller 200 and scheduled by command scheduler 210 include a CASZ signal, and respective RASZ signal. *Id.*, ¶¶0029-0030 (Table 1), 0034-0039, Figs. 5, 6.

TABLE 1

Hub Left Terminal Location	Hub Right Terminal Location	82a, 86a DDR2 CS_0	82b, 86b DDR2 CS_1	82a, 86a DDR3 CS_0	82b, 86b DDR3 CS_1
C_5	C_{27}	A_0	A_{10}	A_3	A_0
C_{11}	B_{21}	A_1	A_2	A_6	A_5
C_6	C_{26}	A_2	A_1	BA_3	BA_2
C_{12}	B_{20}	A_3	A_4	A_2	A_1
B_5	B_{27}	A_4	A_3	A_1	A_2
B_{11}	A_{21}	A_5	A_6	A_{12}	A_{13}
B_6	B_{26}	A_6	A_5	A_5	A_6
B_{12}	C_{19}	A_7	A_8	A_7	A_8
A_5	B_{29}	A_8	A_7	A_8	A_7
A_{13}	A_{19}	A_9	A_{11}	A_9	A_{11}
D_{12}	C_{21}	A_{10}	A_0	BA_2	BA_3
A_4	A_{29}	A_{11}	A_9	A_{11}	A_9
A_{12}	A_{20}	A_{12}	A_{13}	A_4	A_{14}
A_6	A_{27}	A_{13}	A_{12}	A_{13}	A_{12}
A_{11}	A_{22}	A_{14}	A_{15}	A_{15}	A_{15}

[2] Table 1 lists memory device "82" but should apparently be "80." Numeral 82 elsewhere refers to a bus, and 80 a memory device. EX1006, ¶¶0023-0030.

TABLE 1-continued

Hub Left Terminal Location	Hub Right Terminal Location	82a, 86a DDR2 CS_0	82b, 86b DDR2 CS_1	82a, 86a DDR3 CS_0	82b, 86b DDR3 CS_1
A_7	A_{28}	A_{15}	A_{14}	A_{14}	A_4
A_{10}	A_{23}	A_{16}	A_{16}	A_{16}	A_{16}
D_7	D_{27}	BA_0	BA_0	BA_1	BA_0
E_{13}	D_{20}	BA_1	CASZ	A_{10}	WEZ
E_7	E_{25}	BA_2	BA_2	CSZ_1	CSZ_1
F_{12}	F_{22}	BA_3	BA_3	ODT_1	ODT_1
D_8	D_{26}	CASZ	BA_1	CASZ	RASZ
D_6	D_{28}	CSZ_0	CSZ_0	WEZ	A_{10}
D_{11}	D_{21}	CSZ_1	CSZ_1	BA_0	BA_1
C_9	E_{28}	ODT_0	ODT_0	ODT_0	ODT_0
D_{13}	C_{20}	ODT_1	ODT_1	A_0	A_3
F_9	E_{22}	RASZ	WEZ	CSZ_0	CSZ_0
E_{10}	D_{22}	WEZ	RASZ	RASZ	CASZ

Thus, command scheduler 210 (*circuitry to schedule*) schedules output of a CASZ signal as well as output of an associated RASZ signal for the same memory devices (*is to schedule at least one column access command for each row activation command*). Moreover, a POSITA would have understood or at least found obvious such an output of CASZ and RASZ signals is *in order to access a column within a row activated by a corresponding row activation command*. EX1003, ¶94. This is because the reason why a RASZ ("row address strobe") signal and CASZ ("column address strobe") signal are transmitted to a memory device is to access the information stored within the column, specified by the CASZ signal, of the row activated by the RASZ signal. *Id.*; EX1006, ¶¶0029, 0034-0036; EX1003, ¶¶93-94.

Command shifter 214, multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242 (*the command interface*) transmits, using ring buffers 204 and 242, "command and address signals" that include bank addresses BA0-BA3 and chip select signals CSZ0 and CSZ1 that relate to associated CASZ column access

strobe and RASZ row address strobe signals, to memory devices 80a, 86a, 80b, or 86b of memory modules 310 (*is to transmit bank address information to the memory device for each row activation command and for each column access command*). EX1006, 0034-0039, Figs. 5, 6; Section VIII.A.1.c; EX1003, ¶95. The bank addresses BA0-BA3 and chip select signals CSZ0 and CSZ1 are part of each command of the CASZ column access strobe and RASZ row address strobe signals because they inform the bank address and associated memory device (either an "a" device or "b" device) for each CASZ and RASZ command. *Id.*; EX1003, ¶95.

The outputting of bank addresses BA0-BA3 is to select a bank since this value indicates the address for the bank subject to a read or write command (*in order to select a bank*) and the outputting of chip select signals CSZ0 and CSZ1 is to select either the group of devices 80a and 86a on the "first surface 100a" of a memory module or the group of devices 80b and 86b on the "second surface 100b" of a memory module (*and in order to select one of the bank groups in the plurality of bank groups*). EX1006, ¶¶0025-0026, 0029-0030, 0034-0039, Figs. 5, 6; EX1003, ¶96.

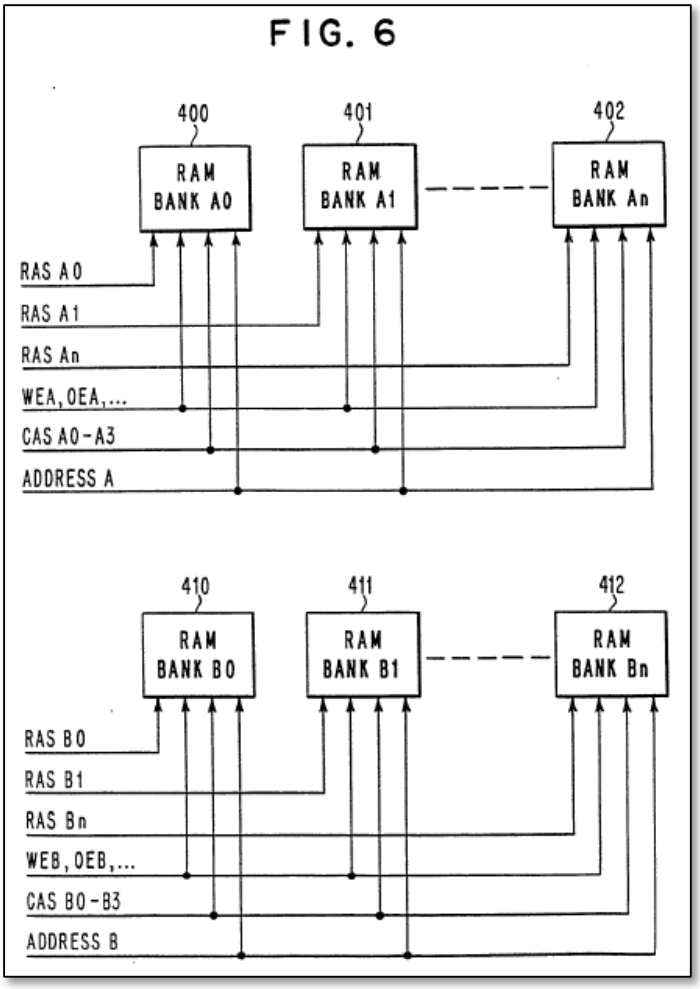
4. Claim 9

LaBerge's memory controller 200 transmits "command and address signals" that include bank addresses BA0-BA3 and chip select signals CSZ0 and CSZ1 that relate to associated CASZ column access strobe and RASZ row address strobe

signals, to memory devices 80a, 86a, 80b, or 86b of memory modules 310 (EX1006, ¶¶0034-0039, Figs. 5, 6; Section VIII.A.1.c; EX1003, ¶97), where the bank addresses BA0-BA3 and chip select signals CSZ0 and CSZ1 are part of each command of the CASZ column access strobe and RASZ row address strobe signals because they inform the bank address and associated memory device (either an "a" device or "b" device) for each CASZ and RASZ command (*the memory controller is to… transmit bank address information as part of each command of the row activation commands and column access commands*). *Id.*; EX1003, ¶97. The outputting of chip select signals CSZ0 and CSZ1 is to select either the group of devices 80a and 86a on the "first surface 100a" of a memory module or the group of devices 80b and 86b on the "second surface 100b" of a memory module (*to select a bank group of the plurality of bank groups*) and the outputting of bank addresses BA0-BA3 is to select a bank since this value indicates the address for the bank subject to a read or write command (*and to select a bank within the selected bank group*). EX1006, ¶¶0025-0030, 0034-0039, Figs. 5, 6; EX1003, ¶97.

In the LaBerge-Bowater combination, a POSITA would have understood or at least found obvious LaBerge's memory controller 200 would have interleaved the RAS A commands and RAS B commands, and the CAS A commands and CAS B commands as taught by Bowater (*wherein the memory controller is to interleave row activation commands and is to interleave column access commands*) for back-to-

back data accesses from rows in different bank groups—i.e, row activation using RAS A to memory devices 80a, 86a, 80b, and 86b in module 310a and a subsequent row activation using RAS B to memory devices 80a, 86a, 80b, and 86b in module 310b—and back-to-back data accesses from columns in different bank groups—i.e, column access using CAS A to memory devices 80a, 86a, 80b, and 86b in module 310a and a subsequent column access using CAS B to memory devices 80a, 86a, 80b, and 86b in module 310b (*for back-to-back data accesses in different bank groups*). Sections VIII.A.1.e-f; EX1003, ¶98. This is because Bowater teaches, with reference to Figure 6, "control signals" RAS A, RAS B, CAS A, and CAS B (shown in Figure 2) "connect to banks of memory for two-way interleaving." *Id.*; EX1007, 4:25-40, 6:47-50, 7:1-13, Figs. 2, 6.



Bowater, Fig. 6

A POSITA would have been motivated to combine LaBerge and Bowater in this manner. EX1003, ¶99. The combination would have enhanced LaBerge's system by providing how RAS and CAS commands are handled and would have been nothing more than a design choice implemented by a POSITA. *Id.* Such a combination would have been routine and straightforward to POSITAs, and would have provided benefits including increased memory bandwidth and reduced latency. *Id*. Bowater explains such interleaving of RAS and CAS commands to memory

banks provides "faster access to a contiguous chunk of memory because access to the banks can be overlapped" and that "page size is effectively doubled because there is an active row in both banks." EX1007, 6:47-50, 7:1-13. A POSITA would have further combined LaBerge and Bowater with a reasonable expectation of success for the same reasons as in Section VIII.A.1.e.

5. Claim 10

LaBerge and Bowater describe the interval between back-to-back high to low changes of the signal "RAS A" (*first interval*) is longer than the interval between back-to-back high to low changes of the signal "CAS A" (*is longer than the third interval*), and the interval between back-to-back low to high changes of the signal "RAS A" and the signal "RAS B" (*and the second interval*) is longer than the interval between back-to-back low to high changes of the signal "CAS A" and the signal "CAS B" (*is longer than the fourth interval*). Sections VIII.A.1.e-f.

6. Claim 20

See Section VIII.A.1.

7. Claim 22

See Section VIII.A.3.

B. Ground II: LaBerge, Bowater, and Suh render claims 3 and 21 obvious

1. Claim 3

Each of Suh's bank 0, bank 1, bank 2, and bank 3 (each a *bank*) includes eight respective bank sections (*sub-banks*), each labeled as "bank 0," "bank 1," "bank 2," and "bank 3," distributed in the cell arrays of Figure 2. EX1005, 3:20-38, Fig. 2. Suh describes a first cell array (*first bank group*) and a second cell array (*second bank group*). *Id.*

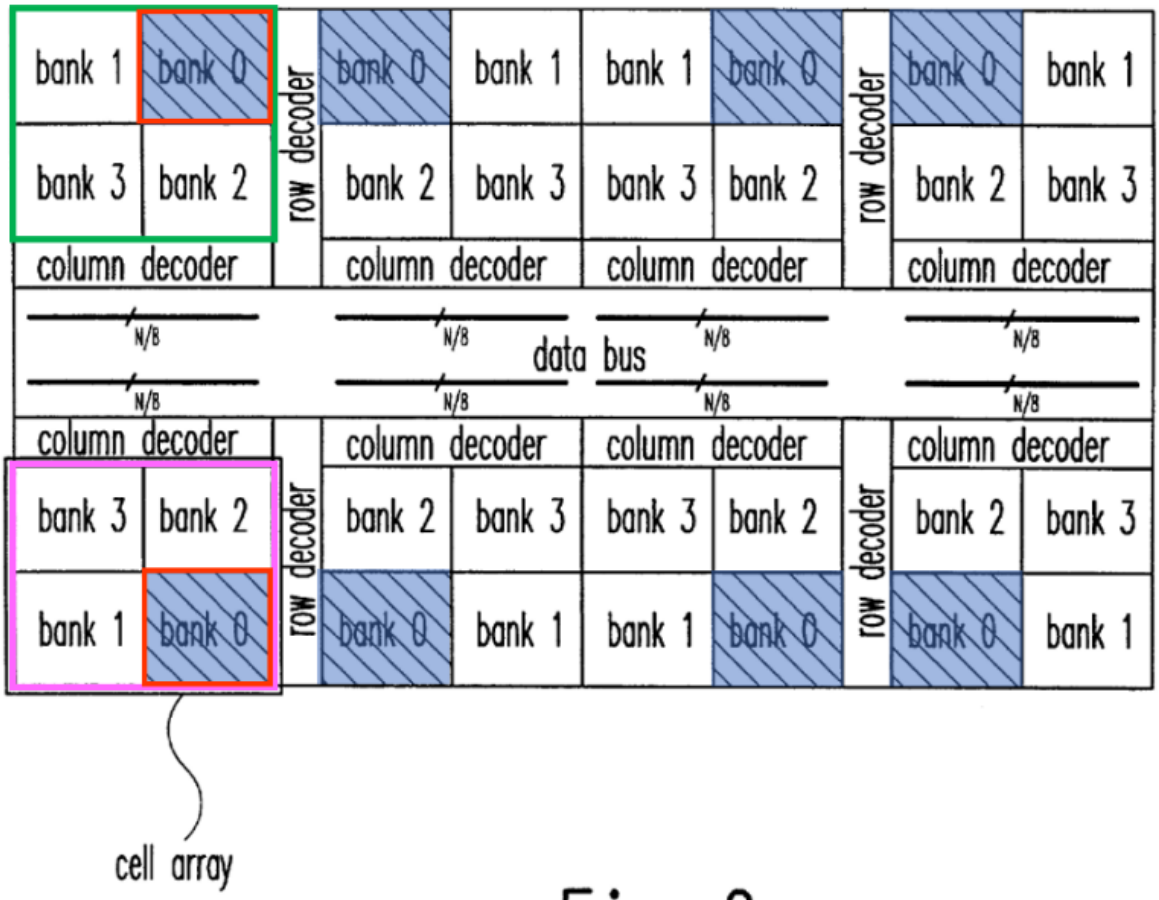


Fig. 2

Suh, Figure 2 (annotated)

In Suh, "a column decoder is connected to each of the cell arrays, and a row decoder is positioned between the two cell arrays in each of the cell array blocks and connected in common to them." EX1005, 3:28-31, Fig. 2.

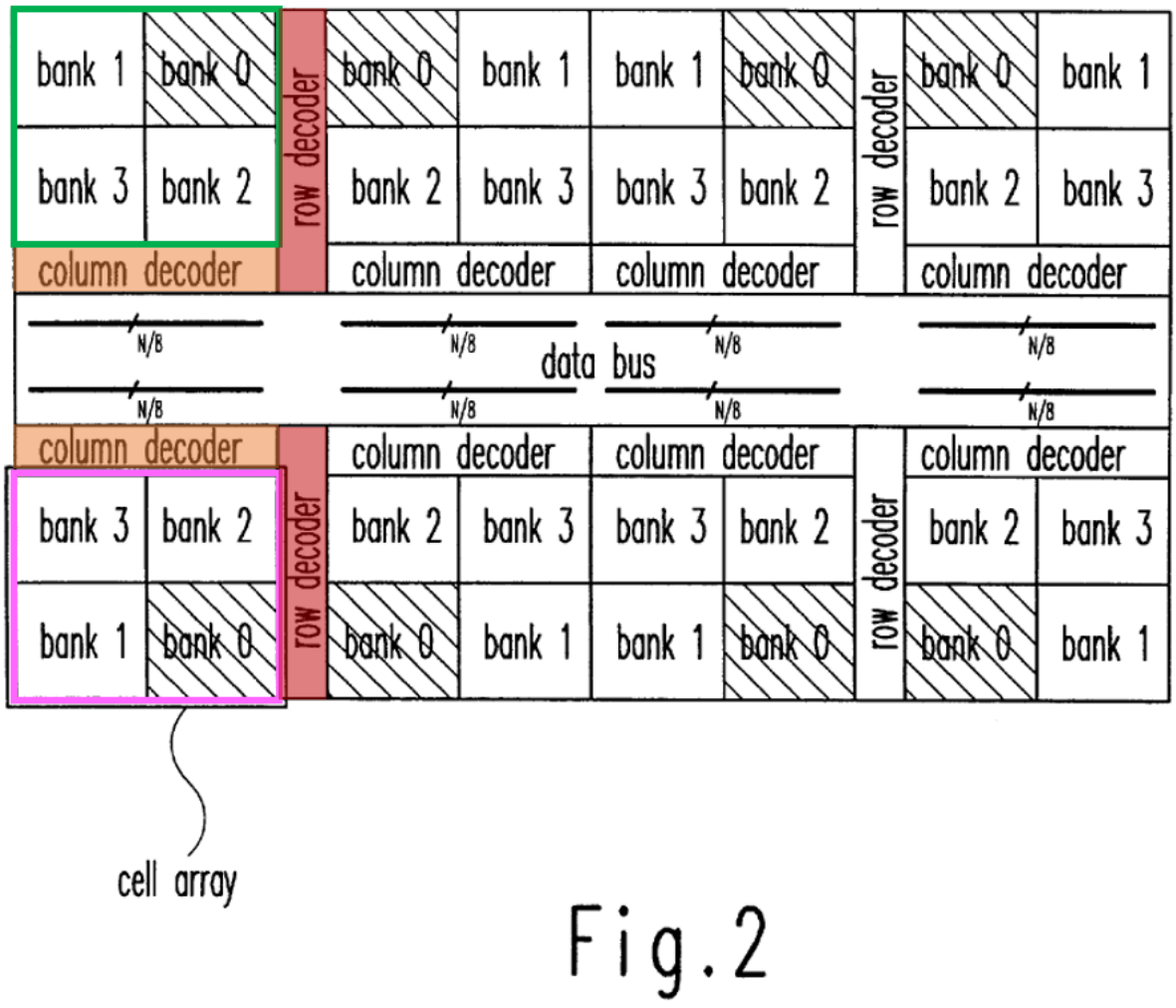


Fig. 2

Suh, Figure 2 (annotated)

As shown by Figure 2, each of Suh's bank sections (*each sub-bank*) in the first cell array (*in the first bank group*) shares a row decoder (*shares first row decoder circuitry*) and a column decoder with each other bank section in the first cell array (*and first column decoder circuitry with each other sub-bank in the first bank group*).

Id. And each of Suh's bank sections (*each sub-bank*) in the second cell array (*in the second bank group*) shares a second row decoder (*shares second row decoder circuitry*) and a second column decoder with each other bank section in the second cell array (*and second column decoder circuitry with each other sub-bank in the second bank group*). *Id.*; EX1003, ¶¶108-110.

Motivation to Combine

A POSITA would have been motivated to combine LaBerge and Bowater as of Section VIII.A.1.e. A POSITA would have been further motivated to combine the LaBerge-Bowater combined system with Suh such that LaBerge's memory devices 80a, 86a, 80b, and 86b that each form a respective memory bank (*bank*) would have been organized into cell arrays and bank sections, and have bank sections that share a row decoder and column decoder, as taught by Suh. EX1003, ¶111. The combination would have enhanced the LaBerge-Bowater system, providing the more efficient grouping of memory cells, improved operation speed, and a reduction in chip area used by the memory. *Id.*; EX1005, 1:10-15, 1:28-30, 1:65-2:6, 5:41-48.

Combined, LaBerge's memory devices 80a, 86a, 80b, and 86b within the LaBerge-Bowater system would have taken advantage of Suh's cell array and bank section layout, with each bank section in a particular group sharing a row decoder and column decoder. EX1003, ¶112. LaBerge already describes memory devices 80a, 86a, 80b, and 86b store data at locations indicated by row and column addresses.

EX1006, ¶¶0034-0039, Figs. 5, 6. Suh, applicable to the LaBerge-Bowater system as it is similarly directed to memory devices organizing data storage by row and column addresses, simply teaches the organization of such memory cells to improve access speed and chip layout. Suh, 1:10-15, 1:28-30, 1:65-2:6, 5:41-48; EX1003, ¶112. Enhancing the LaBerge-Bowater system with Suh would have improved the system, and furthered LaBerge's goals of addressing difficulties in prior systems such as, e.g., improperly using "area that could be used for the integrated circuit itself." EX1006, ¶0011; EX1003, ¶112.

A POSITA would have combined LaBerge-Bowater and Suh as above using known hardware and software techniques associated with memory devices, and for the same reasons discussed above, a POSITA would have readily combined Suh's teachings with the LaBerge-Bowater system. EX1003, ¶113. Separate or combined, the LaBerge-Bowater and Suh systems would have both performed the same memory and data storage functionality. *Id.* The combination would have further been predictable, straightforward, and routine for a POSITA. *Id*. And a POSITA would have had a reasonable expectation of success in making this combination for the same reasons discussed above, and also due to the similarities of both references, where the references are at least directed to memory devices that aim to increase efficiencies. *Id.*; EX1006, ¶¶0011-0013; EX1005, 1:10-15, 1:28-30, 1:65-2:6, 5:41-48.

Additionally, Suh is analogous art to the '379 patent, from the same field of endeavor as the patent (e.g., memory systems) and reasonably pertinent to the particular problem the patent was trying to solve (e.g., how to improve memory performance). EX1001, Abstract, 1:28-29, 4:1-20; EX1005, Abstract, 1:8-16, 1:64-2:6; EX1003, ¶114.

2. Claim 21

See Sections VIII.A.2, VIII.B.1.

C. Ground III: LaBerge, Bowater, and Halbert render claim 5 obvious

1. Claim 5

LaBerge's command scheduler 210 is *the circuitry to schedule* and schedules, for a RASZ command, a CASZ command (*for a given row activation command, a column access command*). Sections VIII.A.1.d-e. Halbert describes "two consecutive read operations (to the same ROW of the memory devices)," where a controller "latches an active command in RCMD," commanding a row activation, and a "READ command (to COL a) is clocked in, causing the controller to enter a read state," and "a second READ command (to COL b) is clocked in," providing two commands to access columns a and b, which are different columns within the same row of memory that has been activated by the active command (*at least two column access commands, in order to access different columns within a row activated by the given row activation command*). EX1008, 5:58-6:6, 2:36-50, Fig. 3

(a READ from "columns [] on the same ROW"). In the combination, LaBerge's command scheduler 210 would have scheduled its commands as taught by Halbert to access different columns within a row (*circuitry to schedule is to schedule for a given row activation command, at least two column access commands, in order to access different columns within a row activated by the given row activation command*.). EX1003, ¶116.

Motivation to Combine

A POSITA would have been motivated to combine LaBerge and Bowater for the reasons in Section VIII.A.1.e. A POSITA would have been motivated to combine the LaBerge-Bowater combined system with Halbert such that LaBerge's command scheduler 210 would have scheduled its commands as taught by Halbert. The combination would have enhanced the LaBerge-Bowater combined system, providing the more efficient accessing to data. EX1003, ¶¶117-118. Combined, the LaBerge-Bowater combined system would have taken advantage of Halbert's data access techniques; the LaBerge-Bowater combined system already describes scheduling column access of an activated row using CAS and RAS commands. *Id.*; EX1006, ¶¶0034-0039, Figs. 5, 6. Halbert, applicable to the LaBerge-Bowater combined system as it is similarly directed to DRAM memory devices, simply teaches accessing multiple columns of a row when the row is activated. EX1008, 2:36-50, 5:58-6:6, Fig. 3; EX1003, ¶118. Enhancing the LaBerge-Bowater

combined system with Halbert would have provided the system schedules multiple column accesses for a given row activation. *Id.* This would have been straightforward and well within the capabilities of a POSITA as it would have simply increased the number of CAS commands in relation to a single RAS command. *Id.*

A POSITA would have combined the LaBerge-Bowater combined system with Halbert as above using known hardware and software techniques associated with memory devices, and for the same reasons discussed above, a POSITA would have readily combined the teachings. EX1003, ¶119. And separate or combined, the LaBerge-Bowater combined system and Halbert system would have both performed the same memory and data storage functionality. *Id.* The combination would have further been predictable, straightforward, and routine for a POSITA. *Id*. And a POSITA would have had a reasonable expectation of success in making this combination for the same reasons discussed above, and also due to the similarities of both references, where both references are at least directed to memory devices that operate using column access commands and row activation commands. *Id.*; EX1006, ¶¶0034-0039, Figs. 5, 6; EX1007, 3:35-46, 4:15-25, Fig. 2; EX1008, 5:58-6:6; 2:36-50, Fig. 3.

Halbert is analogous art to the ’379 patent, from the same field of endeavor as the patent (e.g., memory systems) and reasonably pertinent to the particular problem

the patent was trying to solve (e.g., how to improve memory performance). EX1001, Abstract, 1:28-29, 4:1-20; EX1008, 5:58-6:6; 2:36-50, Fig. 3 ; EX1003, ¶120.

D. Ground IV: LaBerge, Bowater, and Grundy render claims 6 and 7 obvious

1. Claim 6

The LaBerge-Bowater combination describes the claimed *memory controller*, *memory device*, and *column access commands*, as well as *the back-to-back column accesses to banks within different bank groups*. Sections VIII.A.1.a-c, f.

Grundy describes a "memory controller 151" coupled to a collective memory device formed by memory devices 155sub1 through 155sub8; the memory controller has inputs and outputs connecting it to memory devices 155sub1 and 155sub8 via "N multi-purpose lines 158" of "point-to-point signaling links 153" that allow for the sending and receiving of "N-bit wide data values" to and from the collective memory device (*the memory controller also comprises a data interface to exchange data with the memory device via links*), with one subset of links 153 used to send data values to memory device 155sub1 of the collective device and another subset of links 153 used to receive data values from memory device 155sub8 of the collective device, as shown in Figure 5A (*using respective, mutually-exclusive subsets of the links to exchange data*). EX1010, ¶¶0043-0044, Fig. 5A; *id.*, ¶0036,

Fig. 3 (memory controller having a "memory interface" connecting the controller to memory devices).

And the LaBerge-Bowater-Grundy combined system would have provided such sending and receiving of data values (i.e., *exchange [of] data*) would have occurred "*in association with the back-to-back column accesses to banks within different bank groups*" because LaBerge's column access using CAS A to memory devices 80a, 86a, 80b, and 86b in module 310a and subsequent column access using CAS B to memory devices 80a, 86a, 80b, and 86b in module 310b are used when sending data to and receiving data from a memory device during write and read functions. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1003, ¶¶121-123; Sections VIII.A.1.c, f; EX1010, ¶¶0043-0044, Fig. 5A.

If *a data interface to exchange data…* is interpreted under §112(¶6), LaBerge-Bowater-Grundy discloses or at least renders obvious (1) the identified function and (2) the identified structure (Section VI.A.2) for the same reasons discussed above. EX1003, ¶124.

2. Claim 7

The LaBerge-Bowater combination describes the claimed *memory controller*, *memory device*, and *column access commands*. Sections VIII.A.1.a-c; EX1003, ¶125. Grundy describes a *memory controller further comprises a data interface to exchange data with the memory device via links.* Section VIII.D.1. The LaBerge-

Bowater-Grundy combined system would have provided such sending and receiving of data values (i.e., *exchange [of] data*) would have occurred "*in association with each column access command*" because LaBerge's CASZ signals that instruct the memory devices to allow access to desired memory columns are used when sending data to and receiving data from a memory device during write and read functions. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1003, ¶126; Section VIII.A.1.c; EX1010, ¶¶0043-0044, Fig. 5A.

In Grundy, memory controller 151 (1) has a "serializer circuit" at its output "to serialize an N-bit transmission," thereby serializing data sent via the "N multi-purpose lines 158" of each of links 153 to the memory device formed devices 155sub1 through 155sub8, and (2) has a "deserializer circuit" to "deserialize the N-bit transmission," thereby de-serializing data received via the "N multi-purpose lines 158" of each of the links 153 from the memory device formed by devices 155sub1 through 155sub8 (*and the memory controller further comprises serialization/deserialization circuitry to exchange serialized data with the memory device over each of the links*). EX1010, ¶¶0043-0044, 0051-0052, Fig. 5A; EX1003, ¶127.

The LaBerge-Bowater-Grundy combined system would have provided such sending and receiving of serialized data values (i.e., *exchange [of] serialized data*) would have occurred "*in association with each column access command*" because

LaBerge's CASZ signals that instruct the memory devices to allow access to desired memory columns are used when sending data to and receiving data from a memory device during write and read functions. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1003, ¶128; Section VIII.A.1.c; EX1010, ¶¶0043-0044, Fig. 5A.

If *data interface to exchange data with the memory device* is interpreted under §112(¶6), see analysis in Section VIII.D.1. If *serialization/deserialization circuitry to exchange serialized data* is interpreted under §112(¶6), LaBerge-Bowater-Grundy's discloses or at least renders obvious (1) the identified function and (2) the identified structure (Section VI.A.1) for the reasons discussed above. EX1003, ¶129.

3. Motivation to Combine

A POSITA would have been motivated to combine LaBerge and Bowater for the reasons of Section VIII.A.1.e. A POSITA would have been motivated to combine the LaBerge-Bowater system with Grundy such that LaBerge's memory hub controller 200 (Sections VIII.A.1.a-b) is enhanced by Grundy's teachings of (1) the inputs/outputs of memory controller 151 and connect to memory using N multi-purpose lines 158 of point-to-point signaling links 153 that allow for sending and receiving N-bit wide data values to and from the memory device, and (2) a serializer circuit and a deserializer circuit. Sections VIII.D.1-2. The combination would have merely provided techniques by which LaBerge's memory controller transmits data to and receives data from a memory device and processes data to be written to or

read by a memory device, and would have been routine and simple to effectuate. EX1003, ¶130. LaBerge already at least suggests transmitting data to and receiving data from a memory device, and enhancing the LaBerge-Bowater system with Grundy's specific teachings for how transmitting/receiving data and serialization/deserialization of such data is performed would have been appreciated and straightforward to POSITAs. *Id.*; EX1006, ¶¶0034-0039, Figs. 5, 6; Section VIII.A.1.c, f; EX1010, ¶¶0036, 0043-0044, Fig. 5A.

A POSITA would have combined the LaBerge-Bowater system and Grundy as above using known hardware and software techniques associated with memory devices, and for the same reasons discussed above, a POSITA would have readily combined the teachings with Grundy. EX1003, ¶131. And separate or combined, the LaBerge-Bowater and Grundy systems would have both performed the same memory and data storage functionality. *Id.* The combination would have further been predictable, straightforward, and routine for a POSITA. *Id.* And a POSITA would have had a reasonable expectation of success in making this combination for the same reasons discussed above, and also due to the similarities of the references, which are related to memory systems that provide improved performance. *Id.*; EX1006, Abstract, ¶¶0001, 0013-0014; EX1007, Abstract, 2:1-2, 3:5-18, 9:53-10:8; EX1010, Abstract, ¶¶0002, 0030.

Grundy is analogous art to the '379 patent, from the same field of endeavor as the patent (e.g., memory systems) and reasonably pertinent to the particular problem the patent was trying to solve (e.g., how to improve memory performance). EX1001, Abstract, 1:28-29, 4:1-20; EX1010, Abstract, ¶¶0002, 0030; EX1003, ¶132.

E. Ground V: LaBerge, Bowater, and Mehta render claim 8 obvious

1. Claim 8

In the LaBerge, Bowater, and Mehta combination, Mehta's "memory controller 210" includes "hybrid data read/write circuit 220" (*wherein the memory controller further comprises a data interface*) coupling the controller to memory 170 and 180, where circuit 220 includes "DIMM interface modules" 310-390 to "handle[] the necessary data, data strobe, and data mask signals for read and write commands" and "[d]ata, data strobes and data mask signals are likewise passed to and from the DIMMs" through interface modules 310-390 (*to exchange each of data, and write mask values with the memory device*). EX1011, 4:12-60, 5:6-40, 6:11-17, Figs. 1-3. The passing "to and from" of data and data mask values with Mehta's DIMM memory occurs over respective "sub-buses 241-250" of "bus 240" (*exchange each of data, and write mask values with the memory device via respective link subsets*). *Id.*, 5:15-40, Figs. 1-3. "For a write operation to a DIMM, the…data mask signals…are passed from the memory controller …via bus 241 to the DIMM

170" (*id.*, 5:22-26) and a POSITA would have understood or at least found obvious that one or more sub-busses 242-250 would have been used to send data to and/or receive data from the DIMM in read and write operations. *Id.*, 4:12-60, 5:6-40, 6:11-17, Figs. 1-3; EX1003, ¶133. A POSITA would have further understood or at least found obvious that one or multiple of sub-busses 241-250 form *respective link subsets* as they define the subsets of bus 240 over which data is read and written. *Id.*

If *a data interface to exchange…* is interpreted under §112(¶6), LaBerge-Bowater-Mehta discloses or at least renders obvious (1) the identified function and (2) the identified structure (Section VI.A.2) for the same reasons discussed above. EX1003, ¶134.

2. Motivation to Combine

A POSITA would have been motivated to combine LaBerge and Bowater for the reasons of Section VIII.A.1.e. A POSITA would have been motivated to combine the LaBerge-Bowater system with Mehta such that LaBerge's memory hub controller 200 (Sections VIII.A.1.a-b) is enhanced by Mehta's teachings of hybrid data read/write circuit 220 that couples the controller to memory and allows for the passing to and from the memory of data and mask signals. Section VIII.E.1. The combination would have merely provided techniques by which LaBerge's memory controller transmits data to and receives data from a memory device and the ability to use mask values when writing to memory and would have been routine and simple

to effectuate. EX1003, ¶135. Enhancing the LaBerge-Bowater system with Mehta's specific teachings for how transmitting/receiving data and uses mask values would have been appreciated and straightforward to POSITAs. *Id.*; Section VIII.A.1.b; EX1011, 4:12-60, 5:6-40, 6:11-17, Figs. 1-3.

A POSITA would have combined the LaBerge-Bowater system and Mehta as above using known hardware and software techniques associated with memory devices, and for the same reasons discussed above, a POSITA would have readily combined the teachings. EX1003, ¶136. And separate or combined, the LaBerge-Bowater and Mehta systems would have both performed the same memory and data storage functionality. *Id.* The combination would have further been predictable, straightforward, and routine for a POSITA. *Id*. And a POSITA would have had a reasonable expectation of success in making this combination for the same reasons discussed above, and also due to the similarities of the references, which are related to more flexible and efficient memory systems. *Id.*; EX1006, ¶¶0013-0014; EX1007, 3:35-38; *id*, 3:5-18; EX1011, 2:37-3:15.

Mehta is analogous art to the '379 patent, from the same field of endeavor as the patent (e.g., memory systems) and reasonably pertinent to the particular problem the patent was trying to solve (e.g., how to improve memory performance and flexibility). EX1001, Abstract, 1:28-29, 4:1-20; EX1011, 2:37-3:15; EX1003, ¶137.

F. Ground VI: LaBerge, Bowater, Chan, and Kobayashi render claim 11 obvious

1. Claim 11

LaBerge's memory controller 200 includes a "command queue 204" that places DRAM RASZ and CASZ command signals in a queue (*the memory controller is to establish* a *command queue*). EX1006, ¶¶0034-0039, Fig. 5. LaBerge's multiplexors 220 and 230 operate on the command signals to output the appropriate signal to the correct memory device 80 or 86 via elements 214, 220, 230, 240, and 242 (*the memory controller further comprises logic to [] multiplex commands* that is *for transmission to the memory device via the command interface*). *Id.*; Section VIII.A.1.c. Bowater teaches a memory controller interleaving RAS and CAS commands (*and said logic is to interleave commands*) that observe the claimed *first*, *second*, *third*, and *fourth* time intervals (*in a manner that observes the first time interval, the second time interval, the third time interval and the fourth time interval*). Sections VIII.A.1.e-f, VIII.A.4.

In the LaBerge, Bowater, Chan, and Kobayashi combination, Chan teaches "memory command queues" 101 through 104 each corresponding to a bank of memory (*command queues respective to each of the banks in the memory device*). Chan (EX1012), 5:29-6:31, Fig. 4. A POSITA would have understood or at least found obvious that in the LaBerge-Bowater-Chan-Kobayashi combination,

Kobayashi teaches time-multiplexing commands, providing that the commands from queues 101 through 104 of Chan would have been time-multiplexed (*the memory controller further comprises logic to time-multiplex commands from the command queues for the banks for transmission to the memory device via the command interface*). EX1013, ¶0163; EX1012, 5:29-6:31, Fig. 4; EX1003, ¶¶138-139. Moreover, in the combination, Bowater's CAS and RAS commands, located in command queues as taught by Chan, would have been interleaved (*and said logic is to interleave commands from the command queues*). EX1007, 4:25-40, 6:47-50, 7:1-13, Figs. 2, 6; EX1003, ¶¶138-139; VIII.A.1.e-f, VIII.A.4.

If *logic to…* is interpreted under §112(¶6), LaBerge-Bowater-Chan-Kobayashi discloses or at least renders obvious (1) the identified function and (2) the identified structure (Section VI.A.3) for the reasons discussed above. EX1003, ¶140.

Motivation to Combine

A POSITA would have been motivated to combine LaBerge and Bowater for the reasons of Section VIII.A.1.e. A POSITA would have been motivated to combine the LaBerge-Bowater system with Chan and Kobayashi such that LaBerge's memory hub controller 200 (Sections VIII.A.1.a-b) is enhanced by Chan's and Kobayashi's Mehta's teachings, with LaBerge's RAS and CAS commands placed in queues corresponding to each bank of memory and being time-multiplexed and

interleaved as taught. Sections VIII.A.1.e-f, VIII.A.4. EX1003, ¶141. The combination would have merely provided techniques by which LaBerge's memory controller organizes and transmits RAS and CAS commands to memory and would have been routine and simple to effectuate, and appreciated and straightforward, to POSITAs. *Id*. LaBerge and Bowater already describe RAS and CAS commands sent to memory organized in banks, and Chan and Kobayashi simply teach techniques by which such commands are treated. *Id.*; EX1006, ¶¶0003, 0029, 0034-0036; EX1007, 4:25-40, 6:47-50, 7:1-13, Figs. 2, 6; EX1012, 5:29-6:31, Fig. 4; EX1013, ¶0163.

A POSITA would have combined the LaBerge-Bowater system and Chan and Kobayashi as above using known hardware and software techniques associated with memory devices, and for the same reasons discussed above, a POSITA would have readily combined the teachings. EX1003, ¶142. And separate or combined, the LaBerge-Bowater and Chan and Kobayashi systems would have both performed the same memory and data storage functionality. *Id.* The combination would have further been predictable, straightforward, and routine for a POSITA. *Id*. And a POSITA would have had a reasonable expectation of success in making this combination for the same reasons discussed above, and also due to the similarities of the references, which are related to more flexible and efficient memory systems. *Id.*; EX1006, ¶¶0013-0014; EX1007, 3:35-38; *id*, 3:5-18; EX1012, 1:8-15, 3:58-67; Fig. 4; EX1013, ¶¶0036-0045, 0163.

Chan and Kobayashi are analogous art to the '379 patent, from the same field of endeavor as the patent (e.g., memory systems) and reasonably pertinent to the particular problem the patent was trying to solve (e.g., how to improve memory performance and flexibility). EX1001, Abstract, 1:28-29, 4:1-20; EX1012, 1:8-15, 3:58-67; Fig. 4; EX1013, ¶¶0036-0045, 0163; EX1003, ¶143.

G. Ground VII: LaBerge, Bowater, and Wilcox render claims 12, 13, and 15 obvious

1. Claim 12

a. [12a]-[12c]

See Sections VIII.A.1.a-c. Moreover, with respect to limitation [12c], LaBerge's RASZ signals instruct the memory devices to activate desired memory rows, and CASZ signals instruct the memory devices to allow access to desired memory columns (*row activation commands and column access commands*), and are transmitted by command shifter 214, multiplexer 220, single swap multiplexers 230, and ring buffers 240 and 242 (*command interface*) via memory bus 320 (*via a command bus*). Section VIII.A.1.c; EX1006, ¶¶0034-0039, Figs. 5, 6. Since bus 320 carries such command signals, a POSITA would have understood or at least found obvious it is a *command bus*. *Id.*; EX1003, ¶144.

b. [12d]

LaBerge, Bowater, and Wilcox renders obvious this limitation. In the combination, LaBerge teaches a "downstream bus 66" and "upstream bus 68"

between a memory controller and memory modules, that "couple[s] data…away from or toward" the memory controller. EX1006, ¶¶0023, Fig. 4. The embodiment of Figure 6 utilizes a single bus 320 between memory controller 200 and memory modules 310, and a POSITA would have understood or at least found obvious that bus 320 operates in the same way as buses 66 and 68, because bus 320 similarly couples memory controller 200 to memory modules 310 and is similarly used to access memory devices 80a, 86a, 80b, and 86b. *Id.*, ¶0039, Fig. 6; *id.*, ¶¶0034-0038, Fig. 5; EX1003, ¶145. Thus, a POSITA would have understood or at least found obvious that memory controller 200 uses bus 320 to couple data between the memory controller and memory modules 310, and controller 200 therefore includes an interface for coupling data using bus 320 between the controller and modules 310 *([memory controller comprising] a data interface to exchange data with the memory device*). *Id.* Moreover, a POSITA would have understood or at least found obvious that such coupling of data would have been associated with each CASZ signal that instructs the memory devices to allow access to desired memory columns when reading or writing (*in association with each column access command*) because the CASZ signal is a "column address strobe signal" and is known as being used to access a column of memory when reading from or writing to memory. EX1006, ¶¶0003 (referring to RAS and CAS signals as "command" signals), 0029, 0034-0036; EX1003, ¶145.

If the Board finds LaBerge and Bowater do not explicitly teach the *memory controller* comprising a *data interface*, the combination of LaBerge, Bowater, and Wilcox teaches this. In the combination, Wilcox teaches LaBerge's memory controller 200 is a "memory controller 18 [that] includes a data interface 100" (*memory controller* comprising a *data interface*), where data interface 100 "includes write path circuitry 120 for purposes of writing data to the system memory 22" and "circuitry associated with the read path of the data interface 100" including "sense amplifiers 102 that are coupled to receive data bit line signals (called DQ[0:63], which represents sixty-four DQ data bit lines as an example) from respective data bit lines 104…." EX1009, ¶¶0028-0030, Fig. 3; EX1003, ¶146.

If *a data interface to exchange data…* is interpreted under §112(¶6), LaBerge, Bowater, and Wilcox render obvious (1) the identified function for the same reasons discussed above and the identified structure (Section VI.A.2) for the same reasons discussed above. EX1003, ¶147. Further, LaBerge's memory controller, enhanced by the teachings of Wilcox's data interface 100, is at least an equivalent to memory controller hardware because both perform the same functionality of *exchanging data* in substantially the same way, i.e., by transmitting data when writing to memory and receiving data when reading memory. *Kemco Sales*, 208 F.3d at 1364. A POSITA would have further recognized the interchangeability of LaBerge's memory controller, enhanced by the teachings of Wilcox's data interface 100, with the identified structure

as both are simply used to exchange data between a memory controller and memory, and such interchangeability would have been routine and well-within the capabilities of a POSITA for the same reasons. EX1003, ¶147. Moreover, Wilcox's data interface 100 teachings are not excluded by any explicit definition in the '379 patent's specification for an equivalent to the identified structure.

Motivation to Combine

A POSITA would have been motivated to combine LaBerge and Bowater for the reasons discussed in Section VIII.A.1.e. A POSITA would have been further motivated to combine the LaBerge-Bowater combined system with Wilcox such that LaBerge's memory controller 200 is enhanced by Wilcox's data interface 100 teachings. EX1003, ¶148. The combination would enhanced LaBerge's system by simply providing an additional technique by data is exchanged by LaBerge's memory controller with memory devices, and would have been nothing more than a design choice implemented by a POSITA. *Id*.

Combined, LaBerge's memory controller 200 in the LaBerge-Bowater combination would have simply used an explicit data interface to exchange data. EX1003, ¶149. Such a combination would have been routine and straightforward to POSITAs. *Id* LaBerge already describes its memory controller 200 sends and receives data from memory devices. EX1006, ¶¶0023, 0034-0039, Figs. 4-6. Wilcox, applicable to LaBerge and Bowater as it similarly is directed to a memory controller

that couples data, teaches a memory controller that has specific read and write path circuitry. EX1009, ¶¶0028-0030, Fig. 3; EX1003, ¶149.

Enhancing LaBerge-Bowater system with Wilcox would have therefore been straightforward and well-within the capabilities of POSITAs, and simply provided a design choice as to how the LaBerge-Bowater system is implemented. EX1003, ¶¶150-151. Specifically, Wilcox teaches a design choice as to how data is coupled between a memory controller and memory—a straightforward and routine matter for POSITAs as LaBerge already describes such coupling of data. *Id.* A POSITA would have combined the LaBerge-Bowater system with Wilcox as above using known hardware and software techniques associated with memory devices, and for the same reasons discussed above, a POSITA would have readily combined Wilcox's teachings with the LaBerge-Bowater system. *Id*. And separate or combined, the LaBerge-Bowater and Wilcox systems would have both performed the same memory and data storage functionality. *Id.* The combination would have been predictable, straightforward, and routine for a POSITA. *Id*. And a POSITA would have had a reasonable expectation of success in making this combination for the same reasons discussed above, and also due to the similarities of both references, where both references are at least directed to memory controllers coupling data to and from a memory device. *Id.*; EX1006, ¶¶0023, 0034-0039, Figs. 4-6; EX1009, ¶0028-0030, Fig. 3.

Wilcox is analogous art to the '379 patent, from the same field of endeavor as the patent (e.g., memory systems) and reasonably pertinent to the particular problem the patent was trying to solve (e.g., how to improve memory performance). EX1001, Abstract, 1:28-29, 4:1-20; EX1009, ¶¶0001-0007; EX1003, ¶152.

c. [12e]-[12h]

See Sections VIII.A.1.d-f and VIII.A.4. Moreover, with respect to limitation [12e], LaBerge describes that command scheduler 210 (*circuitry…to schedule issuance*) is connected to (*coupled to*) shifter 214 (which forms part of the claimed *command interface*, see Section VIII.A.1.c) as shown in Figure 5. EX1006, ¶¶0034-0039, Figs. 5, 6; EX1003, ¶153.

2. Claim 13

See Section VIII.A.2.

3. Claim 15

See Section VIII.A.3.

H. Ground VIII: LaBerge, Bowater, Wilcox, and Suh render claim 14 obvious

1. Claim 14

See Section VIII.B.1. A POSITA would have been motivated to combine LaBerge, Bowater, Wilcox, and Suh for the reasons in Section VIII.B.1. EX1003, ¶156.

I. Ground IX: LaBerge, Bowater, Wilcox, and Halbert render claim 16 obvious

1. Claim 16

See Section VIII.C.1. A POSITA would have been motivated to combine LaBerge, Bowater, Wilcox, and Halbert for the same reasons in Section VIII.C.1. EX1003, ¶157.

J. Ground X: LaBerge, Bowater, Wilcox, and Grundy render claims 17 and 18 obvious

1. Claims 17 and 18

See Sections VIII.D.1 and D.2. A POSITA would have been motivated to combine LaBerge, Bowater, Wilcox, and Grundy for the same reasons in Section VIII.D.3. EX1003, ¶158.

K. Ground XI: LaBerge, Bowater, Wilcox, and Mehta render claim 19 obvious

1. Claim 19

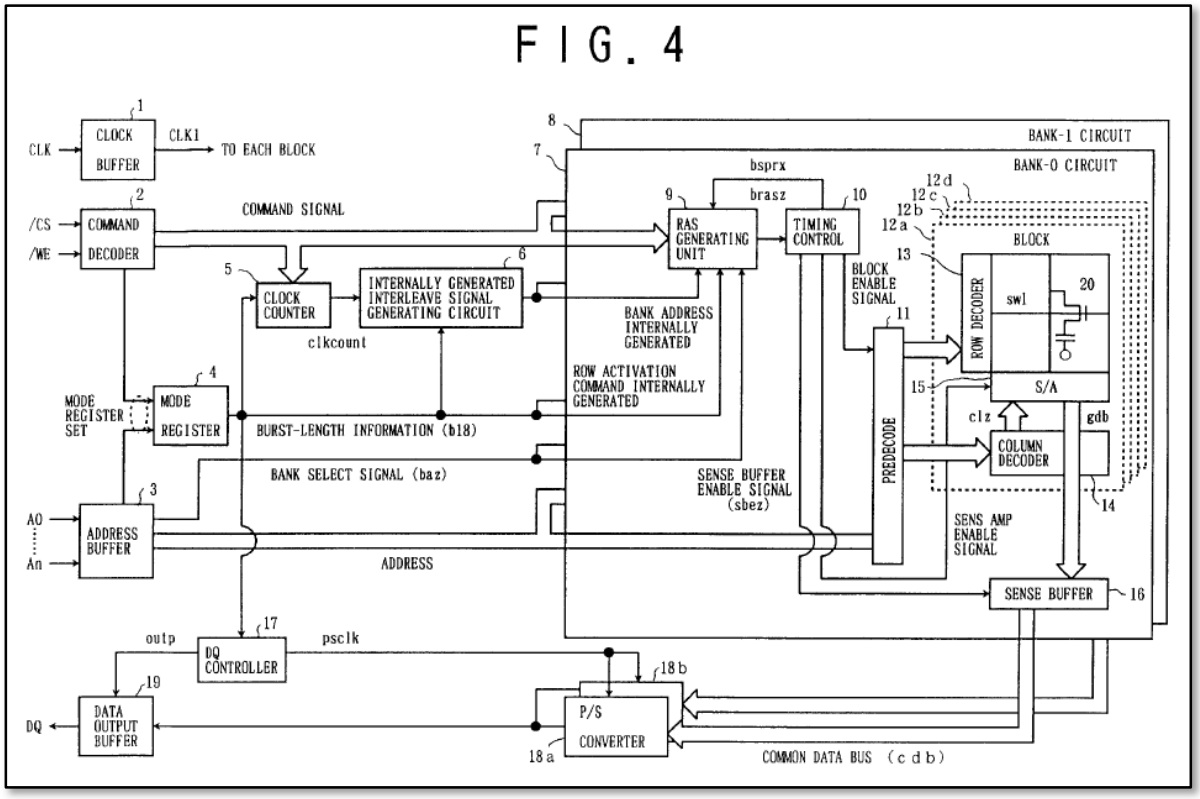
See Section VIII.E.1. A POSITA would have been motivated to combine LaBerge, Bowater, Wilcox, and Mehta for the same reasons in Section VIII.E.2. EX1003, ¶159.

L. Ground XII: Fujioka renders claims 1 and 20 obvious

1. Claim 1

a. [1a]

If the preamble is limiting, Fujioka discloses it or at least renders it obvious. Clock buffer 1 and predecoders 11 of bank-0 circuit 7 and bank-1 circuit 8 (collectively, a *memory controller*) control memory cell blocks 12a-12d of bank-0 circuit 7 and bank-1 circuit 8 by "control[][ling] the row decoder 13 to generate a word line select signal swl at an appropriate timing" for a selected memory cell block and "control[ling] the column decoder 14 to generate a column line select signal clz at an appropriate timing" for a selected memory cell block (*to control a memory device*). EX1004, 5:32-60, 6:21-42, 7:5-43, 12:43-14:15, Figs. 4, 9; EX1003, ¶160.



Fujioka, Fig. 4

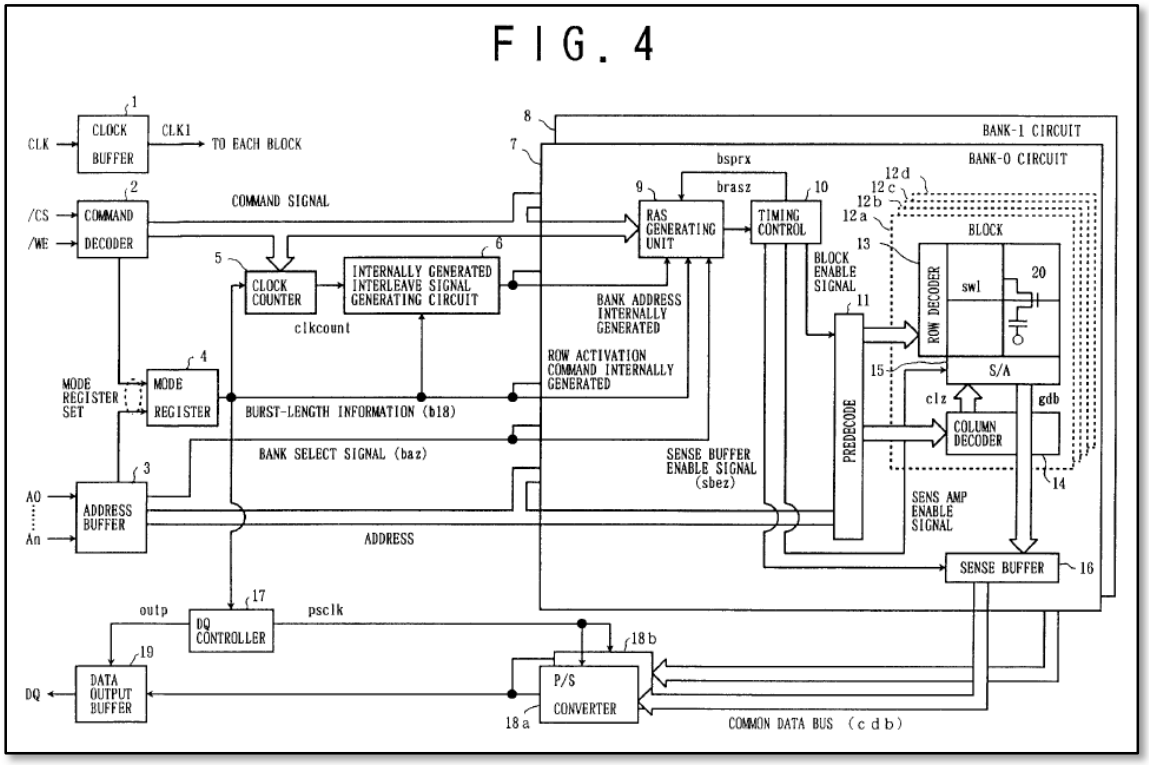
Clock buffer 1 outputs an "internal clock signal CLK1" to predecoders 11 of bank-0 circuit 7 and bank-1 circuit 8. EX1004, 5:36-46, 6:51-62, Fig. 4 (CLK1 provided "TO EACH BLOCK," block 12a labeled a "BLOCK"); EX1003, ¶161.

Fujioka's memory cell block is a "bank." EX1004, 5:32-60 9:18-20 ("bank (memory cell block) interleaving operation") (parentheses in original), Fig. 4; EX1003, ¶162. Bank-0 circuit 7 has a group of memory cell blocks/banks 12a-12d (first *bank group*) and bank-1 circuit 8 has another group of memory cell blocks/banks 12a-12d (second *bank group*). *Id.* Memory cell blocks 12a-12d of bank-0 circuit 7 and memory cell blocks 12a-12d of bank-1 circuit 8 (*memory device*) has a plurality of groups of memory cell blocks 12a-12d (*having a plurality of bank groups*). *Id*.

b. [1b]

Clock buffer 1 and predecoders 11 of bank-0 circuit 7 and bank-1 circuit 8 (collectively *the memory controller*) comprise clock buffer 1 that outputs an "internal clock signal CLK1" to memory cell blocks 12a-12d of each of bank-0 circuit 7 and bank-1 circuit 8 (*comprising: circuitry to provide a clock signal to the memory device*). EX1004, 5:36-46, 6:51-62, Fig. 4. A POSITA would have understood or at least found obvious that CLK1 (*the clock signal*) has clock transitions from a low state to a high state and a high state to low state (*having clock transitions*) because clock signals are well known in the art to have such transitions.

EX1003, ¶163. Moreover, CLK1 is formed from input clock signal CLK which has such transitions. *Id.*; EX1004, Fig. 9.

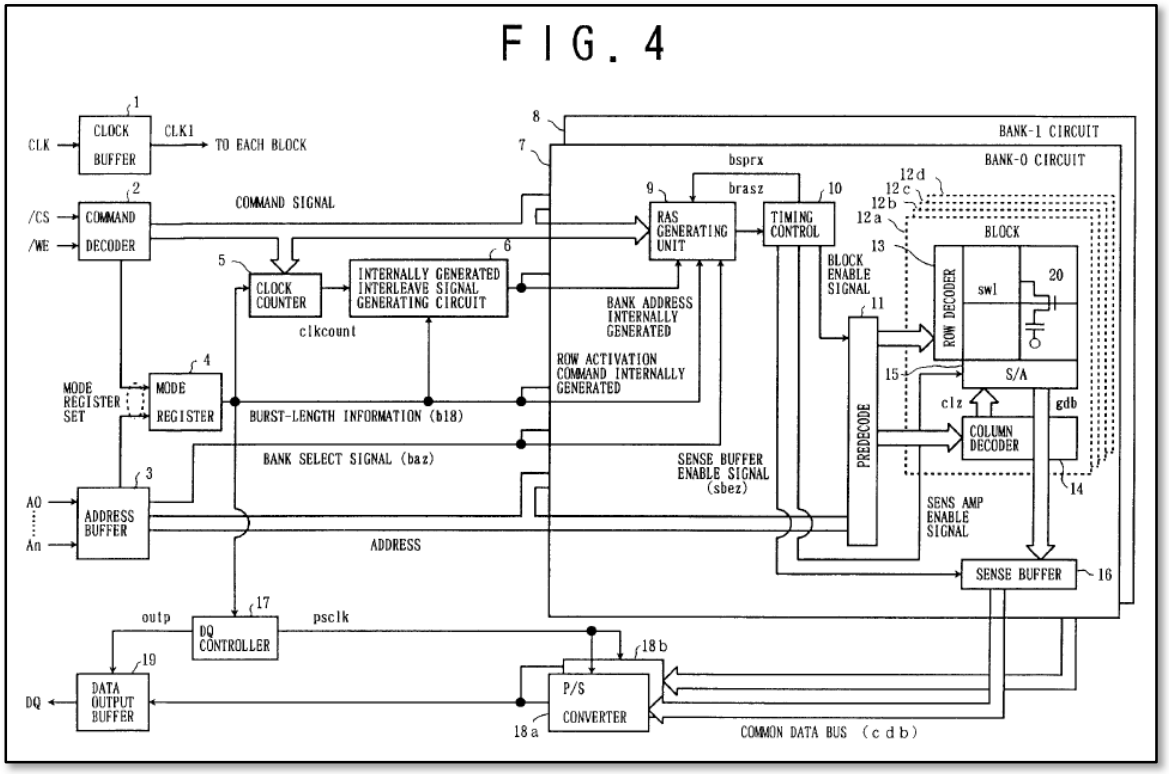


Fujioka, Fig. 4

If *circuitry to provide a clock signal* is interpreted under §112(6), Fujioka discloses or at least renders obvious (1) the identified function for the same reasons discussed above and (2) the identified structure and equivalents thereof (Section VI.A.1, *supra*) because it teaches clock buffer 1. Clock buffer 1 is also at least an equivalent because both perform the same functionality of outputting an output clock signal to memory, and the components are therefore interchangeable. *Kemco Sales,* F.3d at 1364; EX1003, ¶164. Clock buffer 1 is not excluded by any explicit definition in the ’379 patent's specification for an equivalent. *Id.*

c. [1c]

Clock buffer 1 and predecoders 11 of bank-0 circuit 7 and bank-1 circuit 8 (collectively, *the memory controller*) comprise predecoders 11 of bank-0 circuit 7 and bank-1 circuit 8 (*a command interface*) that "control[] the row decoder 13 to generate a word line select signal swl at an appropriate timing" for selected memory cell blocks (*to transmit, to the memory device, row activation commands to instruct row activations*), where such control transmits the claimed commands by commanding row decoder 13 to activate a particular word line of a selected memory block 12a-12d using the word line select signal swl. EX1004, 5:32-60, 6:21-42, 7:5-43, 12:43-14:15, Figs. 4, 9; EX1003, ¶165. Word lines were known in the art as rows of memory. *Id*.



Fujioka, Fig. 4

Predecoders 11 of bank-0 circuit 7 and bank-1 circuit 8 (*command interface*) "control[] the column decoder 14 to generate a column line select signal clz at an appropriate timing" for selected memory cell blocks (*to transmit, to the memory device…column access commands to instruct column accesses*), where such control transmits the claimed commands by commanding column decoder 14 to access a particular column of a selected memory block 12a-12d using the column line select signal clz. EX1004, 5:32-60, 6:21-42, 7:5-43, 12:43-14:15, Fig. 4; EX1003, ¶166.

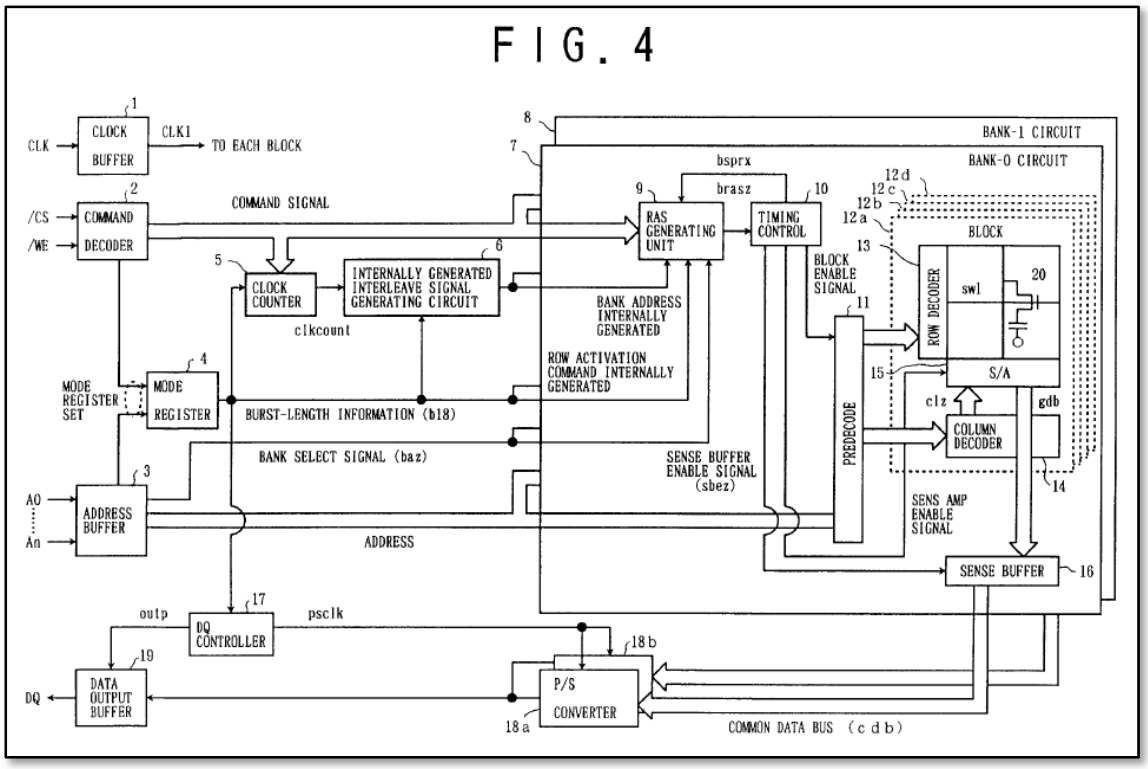
If *a command interface to transmit…*is interpreted under §112(6), Fujioka discloses or at least renders obvious (1) the identified function for the same reasons discussed above, and (2) the identified structure and equivalents thereof (Section VI.A.2) because it describes predecoders 11 of bank-0 circuit 7 and bank-1 circuit 8. Further, the predecoders 11 form at least an equivalent because both perform the same functionality, i.e., transmitting row activation commands and column access commands to memory banks, and the components are therefore interchangeable. *Kemco Sales*, 208 F.3d at 1364; EX1003, ¶167. Predecoders 11 are not excluded by any explicit definition in the '379 patent's specification for an equivalent. *Id.*

d. [1d]

Internal interleave generating circuit 6 "selects the bank to be activated on the basis of the burst information and the pulse signal generated by the clock counter 5."

EX1004, 6:12-16, Fig. 4. Internal interleave generating circuit 6 is *circuitry to schedule issuance of the row activation commands and the column access commands from the command interface* because it is used to schedule, based on a burst length:

- the enabling of the control (*row activation commands*) from (1) circuit 7's predecoder 11 (forming the *command interface*) to cause "row decoder 13 [of circuit 7] to change the word line select signal sw10z from the low level to the high level at an appropriate timing" and (2) circuit 8's predecoder 11 (forming the *command interface*) to cause "row decoder 13 [of circuit 8] to change the word line select signal sw11z at an appropriate timing" (*Id.*, 8:17-50, 9:18-42, 9:51-61, Fig. 4, 12:39-13:27, 13:43-14:22, 14:38-49; EX1003, ¶168) and
- the enabling of control (*column access commands*) from (1) circuit 7's predecoder 11 (forming the *command interface*) to cause "column decoder 14 to change the column line select signal cl0z from the low level to the high level at an appropriate timing" and (2) circuit 8's predecoder 11 (forming the *command interface*) to cause "column decoder 14 to change the column line select signal cl1z from the low level to the high level at an appropriate timing." EX1004, 8:51-9:18, 9:51-61. 12:39-13:28, 13:43-14:22, 14:38-49; EX1003, ¶168.



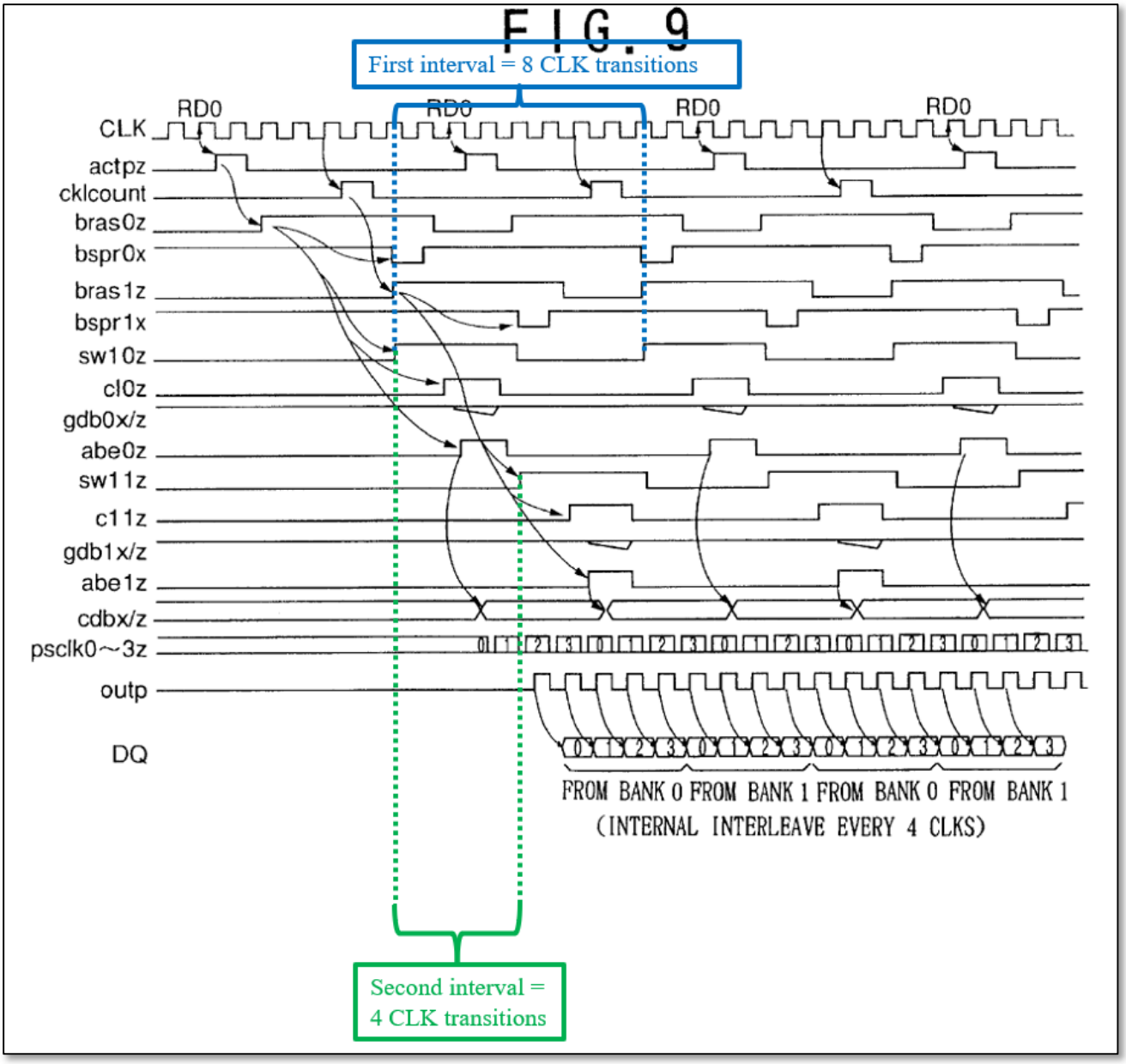
EX1004, Fig. 4

If *circuitry to schedule issuance…*is interpreted under §112(6), Fujioka discloses or at least renders obvious (1) the identified function for the same reasons discussed above for element [1d], and (2) the identified structure and equivalents thereof (Section VI.A.1) because it teaches internal interleave generating circuit 6 as discussed above. Further, circuit 6 forms at least an equivalent to the structure because it performs the same functionality, i.e., by determining the appropriate timing for sending commands, and the components are therefore interchangeable. *Kemco Sales*, 208 F.3d at 1364; EX1003, ¶169. Circuit 6 is not excluded by any explicit definition in the ’379 patent's specification for an equivalent.

e. [1e]

Low to high changes of swl0z are *row activations to banks within a common bank group* because they are the activations of word lines in blocks (*banks*) of memory cell blocks 12a-12d (*common bank group*) in the bank-0 circuit 7. EX1004, 12:66-13:45, Fig. 9; *id.*, 8:45-50; EX1003, ¶170.

As discussed for element [1d], internal interleave generating circuit 6 (*circuitry to schedule issuance…*) schedules, based on a burst length, the enabling of control from (1) circuit 7's predecoder 11 and (2) circuit 8's predecoder 11 (*of the row activation commands and the column access commands from the command interface*). Section VIII.L.1.d. When internal interleave generating circuit 6 utilizes a burst length of 8, this scheduling causes issuance of the signal "swl0z" as shown in Figure 9, such that an interval between back-to-back low to high changes of the signal "swl0z" is defined by **eight** low to high clock transitions of the signal CLK (*a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common bank group*). *Id.*; EX1004, Fig. 9. A POSITA would have further understood or at least found obvious that, since CLK forms the clock signal CLK1, clock signal CLK1 would have also had a number of clock transitions corresponding to the eight low to high clock transitions of the signal CLK. EX1003, ¶171; Section VIII.L.1.b.



EX1004, Figure 9 (annotated)

Fujioka's signal "swl1z" is a "word line select signal" that causes "the data stored in all the memory cells connected to the word line selected by the word line select signal swl1z are read by and held in the sense amplifier block 15." EX1004, 14:9-15. Low to high changes of the signal "swl1z" are activations of word lines in

blocks (*banks*) of memory cell blocks 12a-12s (*bank group*) in the bank-1 circuit 8. *Id.*, 13:59-14:37; EX1003, ¶172.

The signals swl0z and swl1z therefore activate rows in banks of different bank groups, with swl0z activating rows in banks of memory cell blocks 12a-12d (*bank group*) in the bank-0 circuit 7, and swl1z activating rows banks of memory cell blocks 12a-12d (a different *bank group*) in the bank-1 circuit 8. Figure 9 shows an interval between back-to-back low to high changes of the signal swl0z and the signal swl1z. EX1004, Fig. 9. As discussed for element [1d], Fujioka's internal interleave generating circuit 6 (*circuitry to schedule issuance…*) schedules, based on a burst length, the enabling of control from (1) circuit 7's predecoder 11 and (2) circuit 8's predecoder 11 (*of the row activation commands and the column access commands from the command interface*). Section VIII.L.1.d. When the internal interleave generating circuit 6 utilizes a burst length of 8, this scheduling causes issuance of the signal "swl1z" as shown in Figure 9, such that an interval between back-to-back low to high changes of the signal swl0z and the signal swl1z is defined by **four** low to high clock transitions of the signal CLK (*second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups*). EX1004, Fig. 9. A POSITA would have further understood or at least found obvious that, since CLK forms the clock signal CLK1, clock signal CLK1 would have also had a number of clock transitions corresponding

to the four low to high clock transitions of the signal CLK. EX1003, ¶173; Section VIII.L.1.b.

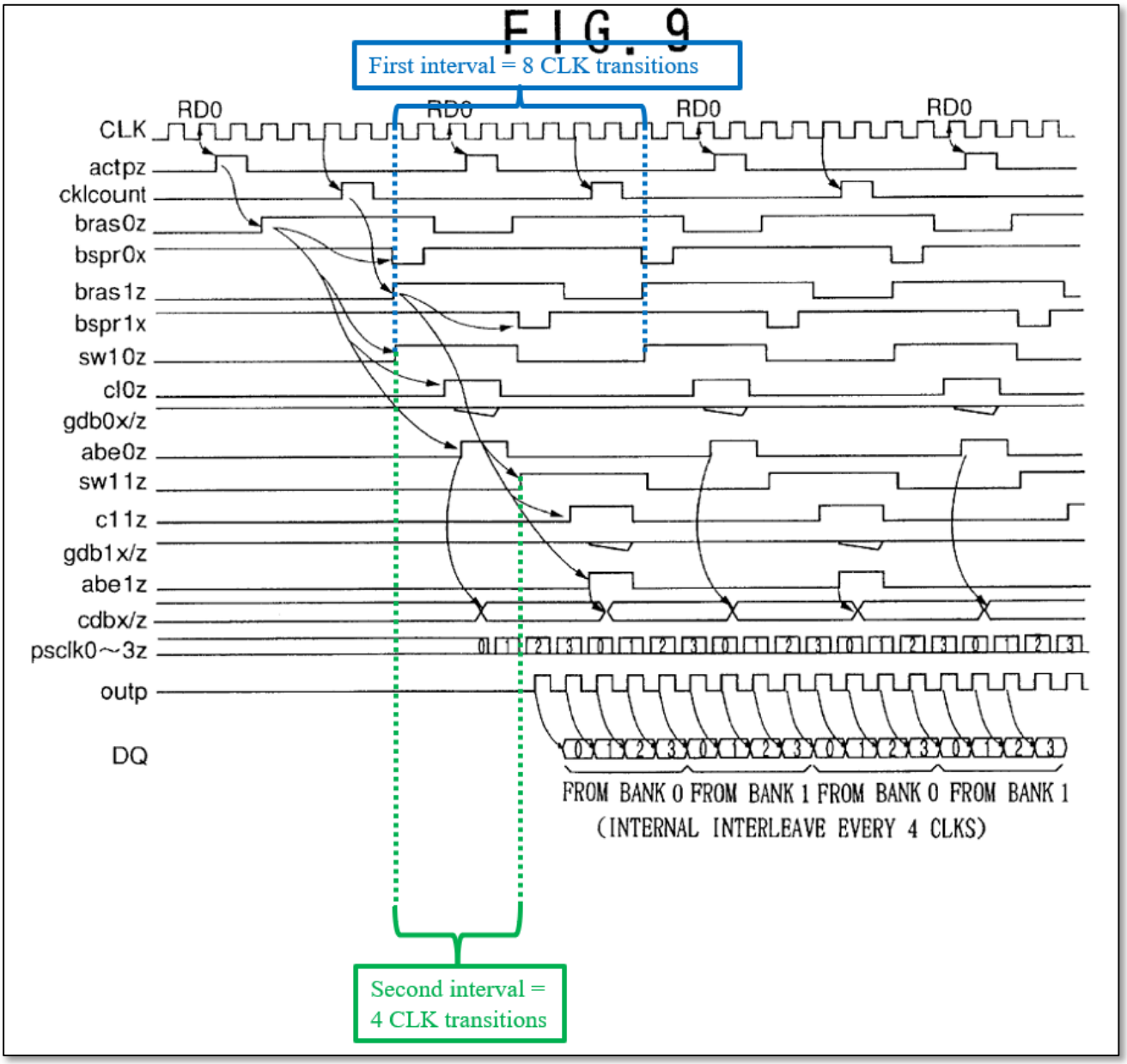


Figure 9 (annotated)

The interval defined by the **eight** low to high clock transitions of CLK between the back-to-back low to high changes of the signal "swl0z" (*first interval*) is longer than (*is longer than*) the interval defined by **four** low to high clock transitions of CLK between the back-to-back low to high changes of the signal swl0z and the signal swl1z (*second interval*). EX1004, Fig. 9; EX1003, ¶174. And a POSITA would have understood or at least found obvious that the number of clock signal transitions of CLK1 equivalent to the eight transitions of CLK would have formed an interval longer than the interval formed by the number of clock signal transitions of CLK1 equivalent to the four transitions of CLK. *Id.*; Section VIII.L.1.b.

f. [1f]

Fujioka's signal "cl0z" is a "column line select signal" supplied to "columns specified" such that bits of data are "read from the sense amplifiers of the specified columns in parallel, and are supplied to the sense buffer 16." EX1004, 7:31-43, 12:67-13:45, 6:35-42, Fig. 9. Low to high changes of the signal "cl0z" cause *column accesses to banks within a common bank group* because they access data in columns of blocks (*banks*) of memory cell blocks 12a-12d (*bank group*) in the bank-0 circuit 7. *Id.*; EX1003, ¶175.

As discussed for element [1d], Fujioka's internal interleave generating circuit 6 (*circuitry to schedule issuance…*) schedules, based on a burst length, the enabling

of control from (1) circuit 7's predecoder 11 and (2) circuit 8's predecoder 11 (*of the row activation commands and the column access commands from the command interface*). Section VIII.L.1.d. When the internal interleave generating circuit 6 utilizes a burst length of 8, this scheduling causes issuance of the signal "cl0z" as shown in Figure 9, such than an interval between back-to-back low to high changes of the signal "cl0z" is defined by eight low to high clock transitions of the signal CLK (*a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group*). *Id.*; EX1004, Fig. 9. A POSITA would have further understood or at least found obvious that, since CLK forms the clock signal CLK1, clock signal CLK1 would have also had a number of clock transitions corresponding to the eight low to high clock transitions of the signal CLK. EX1003, ¶176; Section VIII.L.1.b.

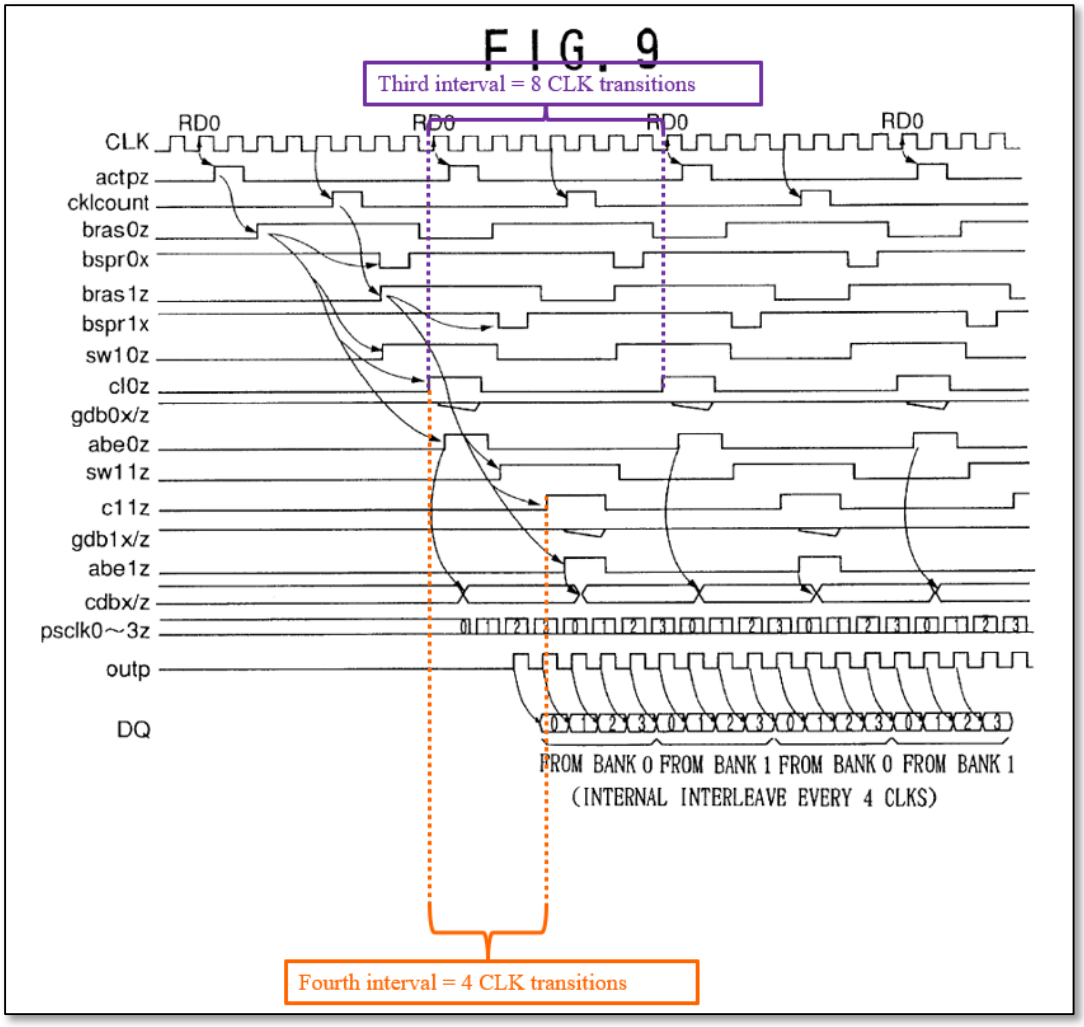


Figure 9 (annotated)

Fujioka's signal "cl1z" is a "column line select signal" supplied to "columns specified" such that bits of data are "read from the sense amplifiers of the specified columns in parallel, and are supplied to the sense buffer 16." EX1004, 7:31-43, 13:43-14:37, 6:35-42, Fig. 9. Low to high changes of the signal "cl1z" access data in columns of blocks (*banks*) of memory cell blocks 12a-12d (*bank group*) in the bank-1 circuit 8. *Id.*; EX1003, ¶177.

The signals cl0z and cl1z therefore access columns in banks of different bank groups, with cl0z accessing columns in banks of memory cell blocks 12a-12s (*bank group*) in the bank-0 circuit 7, and cl1z accessing columns in banks of memory cell blocks 12a-12s (a different *bank group*) in the bank-1 circuit 8. Figure 9 shows an interval between back-to-back low to high changes of the signal cl0z and the signal cl1z. EX1004, Fig. 9. As discussed for element [1d], Fujioka's internal interleave generating circuit 6 (*circuitry to schedule issuance…*) schedules, based on a burst length, the enabling of control from (1) circuit 7's predecoder 11 and (2) circuit 8's predecoder 11 (*of the row activation commands and the column access commands from the command interface*). Section VIII.L.1.d. When the internal interleave generating circuit 6 utilizes a burst length of 8, this scheduling causes issuance of the signal cl1z as shown in Figure 9, such that an interval between back-to-back low to high changes of the signal cl0z and the signal cl1z is defined by four low to high clock transitions of the signal CLK (*fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups*). EX1004, Fig. 9. A POSITA would have further understood or at least found obvious that, since CLK forms the clock signal CLK1, clock signal CLK1 would have also had a number of clock transitions corresponding to the four low to high clock transitions of the signal CLK. EX1003, ¶178; Section VIII.L.1.b.

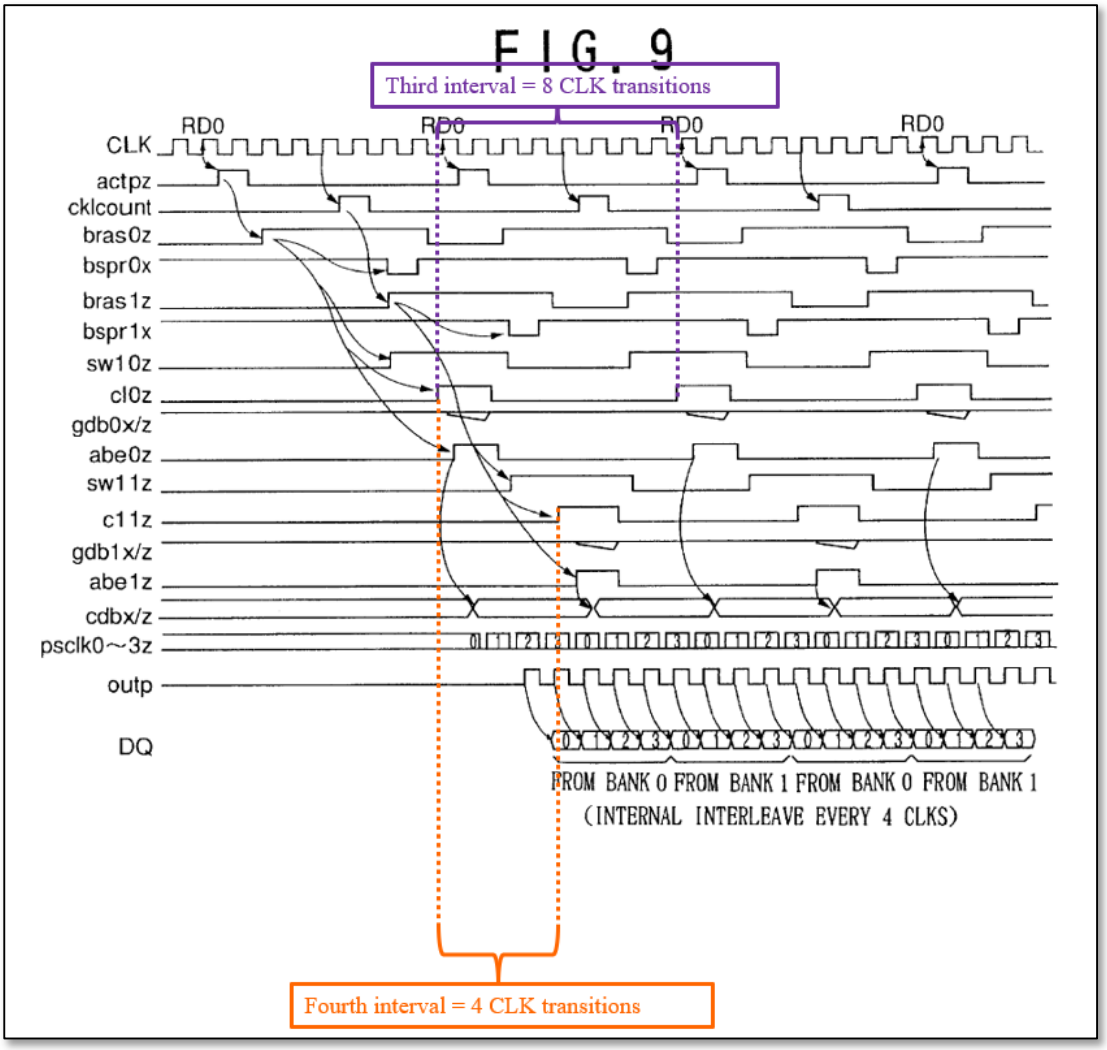


Figure 9 (annotated)

The interval defined by the **eight** low to high clock transitions of the signal CLK that occur between the back-to-back low to high changes of the signal "cl0z" (*third interval*) is longer than (*is longer than*) the interval defined by **four** low to high clock transitions of the signal CLK that occur between the back-to-back low to high changes of the signal cl0z and the signal cl1z (*fourth interval*). EX1004, Fig. 9; EX1003, ¶179. And a POSITA would have understood or at least found obvious

that, since CLK forms the clock signal CLK1, the number of clock signal transitions of CLK1 equivalent to the eight transitions of CLK would have formed an interval longer than the interval formed by the number of clock signal transitions of CLK1 equivalent to the four transitions of CLK. *Id.*; Section VIII.L.1.b.

2. Claim 20

See Section VIII.L.1.

IX. THE BOARD SHOULD INSTITUTE IPR

A. 35 U.S.C. § 314(a)

The merits are strong and present compelling evidence of unpatentability, which alone warrants institution. EX1017, 9. The *Fintiv* factors favor institution. Related litigation is at an early stage; no substantive landmarks have been reached or approach.

B. 35 U.S.C. § 325(d)

The Board should not deny institution under §325(d). Fujioka, Bowater, and Halbert were IDS-cited during prosecution, but never in a rejection or analyzed. EX1002, 128, 134-135. Suh was used to reject dependent claims but was not combined with any reference herein or argued against. *Id.*, 173, 264-266.

Dated: September 10, 2024

Respectfully submitted,

/Jeffrey Johnson/
Jeffrey Johnson
Reg. No. 53,078
Attorney for Petitioner

CLAIM APPENDIX

Claim 1	
[1a]	"*A memory controller to control a memory device, the memory device having a plurality of bank groups*"
[1b]	*"the memory controller comprising: circuitry to provide a clock signal to the memory device, the clock signal having clock transitions;"*
[1c]	*"[the memory controller comprising:] a command interface to transmit, to the memory device, row activation commands to instruct row activations and column access commands to instruct column accesses; and"*
[1d]	*"[the memory controller comprising:] circuitry to schedule issuance of the row activation commands and the column access commands from the command interface, such that"*
[1e]	*"a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common bank group, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups, and"*
[1f]	*"a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups."*
Claim 2	"*The memory controller of claim 1, wherein: each bank includes a first sub-bank and a second sub-bank; the first sub-bank is in a first bank group of the plurality of bank groups; and the second sub-bank is in a second bank group of the plurality of bank groups.*"
Claim 3	"*The memory controller of claim 2, wherein: each sub-bank in the first bank group shares first row decoder circuitry and first column decoder circuitry with each other sub-bank in the first bank group; and each sub-bank in the second bank group shares second row decoder circuitry and second column decoder circuitry with each other sub-bank in the second bank group.*"

Claim 4	"*The memory controller of claim 2, wherein the circuitry to schedule is to schedule at least one column access command for each row activation command, in order to access a column within a row activated by a corresponding row activation command, and wherein the command interface is to transmit bank address information to the memory device for each row activation command and for each column access command, in order to select a bank and in order to select one of the bank groups in the plurality of bank groups.*"
Claim 5	"*The memory controller of claim 2, wherein the circuitry to schedule is to schedule for a given row activation command, at least two column access commands, in order to access different columns within a row activated by the given row activation command*."
Claim 6	"*The memory controller of claim 1, wherein the memory controller also comprises a data interface to exchange data with the memory device via links, using respective, mutually-exclusive subsets of the links to exchange data in association with the back-to-back column accesses to banks within different bank groups*."
Claim 7	"*The memory controller of claim 1, wherein: the memory controller further comprises a data interface to exchange data with the memory device via links, in association with each column access command; and the memory controller further comprises serialization/deserialization circuitry to exchange serialized data with the memory device over each of the links in association with each column access command.*"
Claim 8	*"The memory controller of claim 1, wherein the memory controller further comprises a data interface to exchange each of data, and write mask values with the memory device, via respective link subsets."*
Claim 9	"*The memory controller of claim 1, wherein the memory controller is to interleave row activation commands and is to interleave column access commands for back-to-back data accesses in different bank groups, and is to transmit bank address information as part of each*

	command of the row activation commands and column access commands, to select a bank group of the plurality of bank groups, and to select a bank within the selected bank group."
Claim 10	*"The memory controller of claim 1, wherein: the first interval is longer than the third interval and the second interval is longer than the fourth interval."*
Claim 11	"*The memory controller of claim 1, wherein: the memory controller is to establish command queues respective to each of the banks in the memory device; the memory controller further comprises logic to time-multiplex commands from the command queues for the banks for transmission to the memory device via the command interface; and said logic is to interleave commands from the command queues in a manner that observes the first time interval, the second time interval, the third time interval and the fourth time interval*."
Claim 12	
[12a]	"*A memory controller to control a memory device, the memory device having a plurality of bank groups,*"
[12b]	"*the memory controller comprising: circuitry to provide a clock signal to the memory device, the clock signal having clock transitions;*"
[12c]	"*a command interface to transmit row activation commands and column access commands to the memory device, via a command bus;*"
[12d]	"*a data interface to exchange data with the memory device in association with each column access command; and*"
[12e]	"*circuitry coupled to the command interface to schedule issuance of the row activation commands and the column access commands to banks within the plurality of bank groups, such that*"
[12f]	"*a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common one of the bank groups, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different ones of the bank groups, and*"

[12g]	"*a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common one of the bank groups, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different ones of the bank groups*;"
[12h]	"*wherein the memory controller is to transmit bank address information as part of each command of the row activation commands and column access commands, to communicate selection of a bank group of the plurality of bank groups, and to communicate selection of a bank within the selected bank group*."
Claim 13	"*The memory controller of claim 12, wherein: each bank includes a first sub-bank and a second sub-bank; the first sub-bank is in a first bank group of the plurality of bank groups; and the second sub-bank is in a second bank group of the plurality of bank groups.*"
Claim 14	"*The memory controller of claim 13, wherein: each sub-bank in the first bank group shares first row decoder circuitry and first column decoder circuitry with each other sub-bank in the first bank group; and each sub-bank in the second bank group shares second row decoder circuitry and second column decoder circuitry with each other sub-bank in the second bank group*."
Claim 15	"*The memory controller of claim 13, wherein the circuitry to schedule is to schedule at least one column access command for each row activation command, in order to access a column within a row activated by a corresponding row activation command, and wherein the command interface is to transmit bank address information to the memory device for each row activation command and for each column access command, in order to select a bank and in order to select one of the bank groups in the plurality of bank groups.*"
Claim 16	"*The memory controller of claim 13, wherein the circuitry to schedule is to schedule for a given row activation command, at least two column access commands, in order to access different columns within a row activated by the given row activation command.*"

Claim 17	"*The memory controller of claim 12, wherein the memory controller also comprises a data interface to exchange data with the memory device via links, using respective, mutually-exclusive subsets of the links to exchange data in association with the back-to-back column accesses to banks within different bank groups*."
Claim 18	"*The memory controller of claim 12, wherein: the memory controller further comprises a data interface to exchange data with the memory device via links, in association with each column access command; and the memory controller further comprises serialization/deserialization circuitry to exchange serialized data with the memory device over each of the links in association with each column access command*."
Claim 19	"*The memory controller of claim 12, wherein the memory controller further comprises a data interface to exchange each of data, and write mask values with the memory device, via respective link subsets*."
Claim 20	
[20a]	"*A method of operation in a memory controller, the memory controller to control a memory device, the memory device having a plurality of bank groups, the method comprising*"
[20b]	"*providing a clock signal to the memory device, the clock signal having clock transitions;*"
[20c]	"*transmitting to the memory device, via a command interface, row activation commands to instruct row activations and column access commands to instruct column accesses; and*"
[20d]	"*scheduling issuance of the row activation commands and the column access commands from the command interface, such that*"
[20e]	"*a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common bank group, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups, and*"
[20f]	"*a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group, is longer than a fourth interval, defined by a*

	fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups."
Claim 21	*"The method of claim 20, wherein: each bank includes a first sub-bank and a second sub-bank; the first sub-bank is in a first bank group of the plurality of bank groups; the second sub-bank is in a second bank group of the plurality of bank groups; each sub-bank in the first bank group shares row decoder circuitry and column decoder circuitry with each other sub-bank in the first bank group; and each sub-bank in the second bank group shares row decoder circuitry and column decoder circuitry with each other sub-bank in the second bank group."*
Claim 22	"*The method of claim 20, wherein: the method further comprises transmitting bank address information as part of each command of the row activation commands and column access commands, to communicate selection of a bank group of the plurality of bank groups, and to communicate selection of a bank within the selected bank group*."

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,331,379 contains, as measured by the word-processing system used to prepare this paper, 13,919 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Dated: September 10, 2024

Respectfully submitted,

/Jeffrey Johnson/
Jeffrey Johnson
Reg. No. 53,078
Attorney for Petitioner

CERTIFICATE OF SERVICE UNDER 37 C.F.R. § 42.105

I hereby certify that on September 10, 2024, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,331,379 and supporting exhibits to be served via FedEx Express® or Express Mail on the Patent Owner at the following correspondence address of record as listed on the USPTO Patent Center:

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Respectfully submitted,

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