

Filed on behalf of: K.Mizra LLC

By: David T. DeZern
Registration No. 60,117
NELSON BUMGARDNER CONROY P.C.
2727 N. Harwood Street, Suite 250
Dallas, TX 75201
Telephone: (214) 446-4950
Email: david@nelbum.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SILICON MOTION INC.,
Petitioner

v.

K.MIZRA LLC,
Patent Owner

Case IPR2024-01236

U.S. Patent No. 10,331,379

PATENT OWNER'S PRELIMINARY RESPONSE

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	THE '379 PATENT AND THE CHALLENGED CLAIMS	2
	A. Overview of the '379 Patent.....	2
	B. Challenged Claims	6
	C. Prosecution History of the '379 Patent	10
III.	LEVEL OF ORDINARY SKILL	12
IV.	CLAIM CONSTRUCTION	13
V.	APPLICABLE LEGAL STANDARDS.....	13
	A. Obviousness.....	14
	i. Claims cannot be found obvious if an element is absent.	14
	ii. A petition must address the Graham factors.	15
	iii. A petition must provide articulated reasoning with rational underpinning to combine and/or modify references.	15
VI.	SUMMARY OF THE PRIOR ART REFERENCES.....	17
	A. Overview of LaBerge	17
	B. Overview of Bowater	20
	C. Overview of Fujioka.....	24
VII.	THE PETITION DOES NOT ESTABLISH A REASONABLE LIKELIHOOD OF SUCCESS	25
	A. The Petition Fails to Demonstrate Obviousness of Any Independent Claims.....	25
	i. Ground I: LaBerge & Bowater Fail to Render Independent Claims 1 and 20 Obvious.	26
	ii. Ground VII: LaBerge, Bowater, and Wilcox Fail to Render Independent Claim 12 Obvious.....	27
	iii. Ground XII: Fujioka Fails to Render Independent Claims 1 or 20 Obvious.	27

VIII. PATENT OWNER’S FINAL COMMENTS	28
IX. CONCLUSION.....	28

TABLE OF AUTHORITIES

Cases

<i>CFMT, Inc. v. YieldUp Int’l Corp.</i> , 349 F.3d 1333 (Fed. Cir. 2003)	14
<i>Eizo Corp. v. Barco N.V.</i> , Case No. IPR2014-00358, Paper 11 (PTAB July 23, 2014)	15
<i>Garmin Int’l, Inc. v. Patent of Cuozzo Speed Techs. LLC</i> , Case No. IPR2012-00001, Paper 15 (PTAB Jan. 9, 2013).....	14
<i>Graham v. John Deere Co.</i> , 383 U.S. 1 (1966).....	14, 15
<i>In re Kahn</i> , 441 F.3d 977 (Fed. Cir. 2006)	16
<i>In re Rijckaert</i> , 9 F.3d 1531 (Fed. Cir. 1993)	14
<i>In re Royka</i> , 490 F.2d 981 (C.C.P.A. 1974)	14
<i>InTouch Techs., Inc. v. VGo Comm’ns., Inc.</i> , 751 F.3d 1327 (Fed. Cir. 2014).....	15
<i>KSR Int’l Co. v. Teleflex Inc.</i> , 550 U.S. 398 (2007)	15
<i>LG Elecs., Inc. v. Cellular Commc’ns Equip. LLC</i> , Case No. IPR2016-00197, Paper 7 (PTAB April 29, 2016)	16
<i>N.V. v. Abbott Labs.</i> , 512 F.3d 1363 (Fed. Cir. 2008)	16
<i>Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.</i> ,	

200 F.3d 795 (Fed. Cir. 1999)	13
<i>Wellman, Inc. v. Eastman Chem. Co.</i> , 642 F.3d 1355 (Fed. Cir. 2011)	13
<u>Rules, Statutes, and Regulations</u>	
35 U.S.C. § 103	14
35 U.S.C. § 313	1
35 U.S.C. § 314 (a)	13, 25
37 C.F.R. § 42.107	1
37 C.F.R. § 42.108(c).....	13
<u>Other Authorities:</u>	
Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756 (Aug. 14, 2012)	13

I. INTRODUCTION

Pursuant to 35 U.S.C. § 313 and 37 C.F.R. § 42.107, K.Mizra LLC (“Patent Owner”) submits this Preliminary Response to Silicon Motion, Inc.’s (“Petitioner”) Petition for *Inter Partes* Review (“Petition,” Paper 1), challenging Claims 1-22 of U.S. Patent 10,331,379 (the “’379 Patent”) (Ex. 1001).

The ’379 Patent claims a memory controller (and method) for scheduling commands in a memory device with multiple bank groups. The claimed inventions address issues that arise when a memory device includes multiple storage arrays that share resources imposing timing constraints on access to the different parts of the memory device. The Petition attempts to combine elements from different references describing memory modules that neither disclose nor suggest the type of resource and timing constraints in a memory device that the ’379 Patent addresses. The Petition also fails to identify disclosure in any of the references of a memory controller that schedules commands such that the timing relationships are maintained to achieve the claimed inventions.

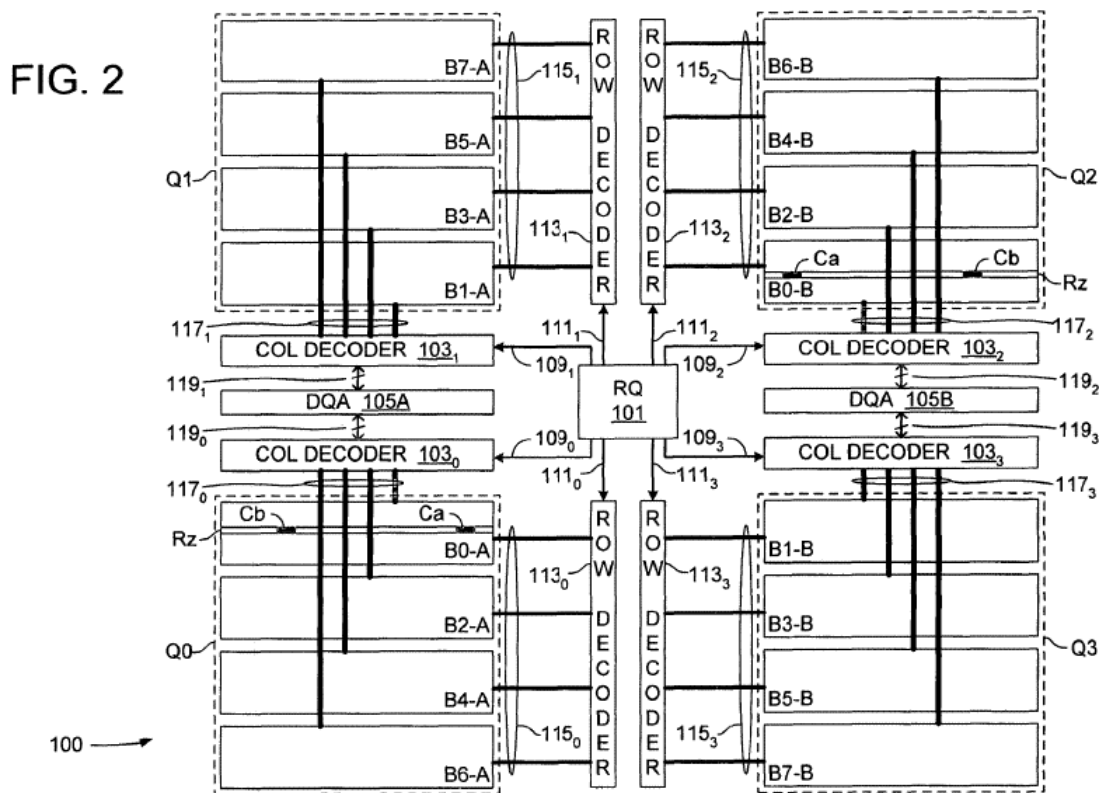
For at least the reasons detailed below, Petitioner cannot show that any of the challenged claims are reasonably likely to be found unpatentable, and the Board should not institute *inter partes* review.

II. THE '379 PATENT AND THE CHALLENGED CLAIMS

A. Overview of the '379 Patent

The '379 Patent is directed to a “[m]emory controller for micro-threaded memory operations.” Ex. 1001, *Title*. The problem it seeks to address is that “dynamic random access memory (DRAM)” “core access times have not scaled with memory bandwidth demand.” *Id.* at 1:33-37. That is, there are limitations regarding the speed with which a DRAM can be accessed, including for example “the minimum time between activation of different storage rows in the same storage bank,” “the minimum time between activation of rows in different banks of a multi-bank array,” and the “minimum time between column access operations (i.e., read or write operations at a specified column address) in the same row.” *Id.* at 1:37-47. Thus, while the systems using DRAM have increased their operating speeds and demands from memory, the DRAM core access times have remained “relatively constant” and are subject to limits imposed by the DRAM itself. *Id.* at 1:53-61. The '379 Patent addresses this problem and the limitations of prior solutions (*id.* at 1:48-2:2) teaching embodiments that “subdivide[] and allocate[] [the data transfer capacity of the DRAM] to multiple column access transactions, thereby reducing the amount of data transferred in any one transaction, yet maintaining the peak memory bandwidth of the DRAM device.” *Id.* at 4:1-7.

The '379 Patent illustrates a memory device on which the claimed invention can be implemented by a controller in Figure 2:

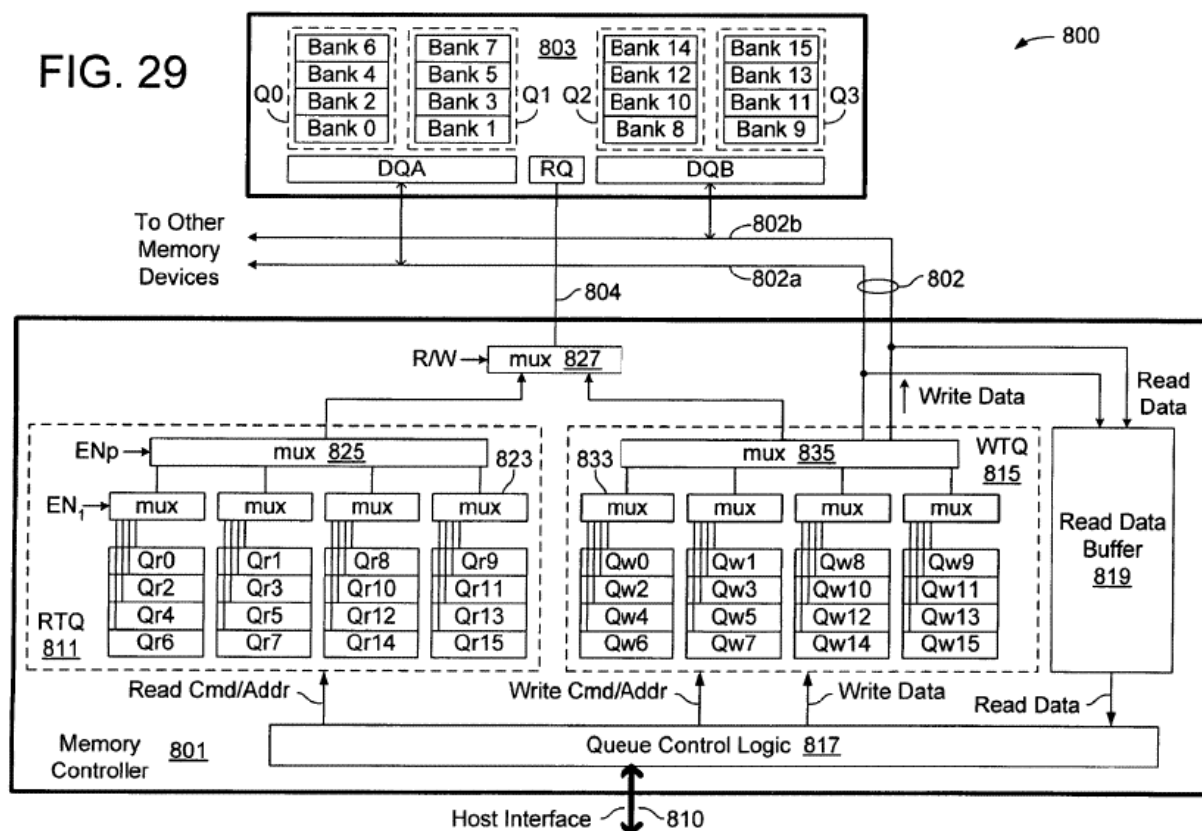


Ex. 1001, Fig. 2.

The memory device addressed by the '379 Patent is presumably a DRAM but includes “any type of memory device having multiple storage arrays that share addressing and/or data path resources in a manner that imposes timing constraints on sequential accesses directed to the different storage arrays.” *Id.* at 4:55-62. As shown in Figure 2, “the memory device 100 includes a request interface 101, column decoders 103₀-103₃, row decoders 113₀-113₃, data path interfaces 105A and 105B and eight storage banks, B0-B7.” *Id.* at 5:15-18. “Each storage bank, B0-

B7, is formed by a pair of A and B sub-banks (e.g., sub-banks B0-A and B0-B constitute bank B0, sub-banks B1-A and B1-B constitute bank B1, and so forth), with the sub-banks themselves being organized in four groups of four sub-banks each, referred to herein as quadrants.” *Id.* at 5:18-23.

In operation, a memory controller directs a stream of requests (or commands or instructions) at the request interface 101 of the memory device which “issues corresponding control and address signals to the row decoders 113 and column decoders 103 to carry out the requested operations.” *Id.* at 5:46-53. Figure 29 illustrates a memory system including a controller 801 and memory device 803:



Ex. 1001, Fig. 29

The '379 Patent teaches several embodiments for “micro-threaded memory transactions” that “subdivide[] and allocate[] [the data transfer capacity of the DRAM] to multiple column access transactions.” *Id.* at 4:1-7. For example, “[r]ather than allocating the full t_{CC} envelope to a single column access (i.e., as in the single-threaded mode described in reference to FIGS. 2-6) and redesigning the memory device 100 to include double-width internal data path widths, the t_{CC} envelope is subdivided into sub-envelopes that are allocated to alternating transactions in the odd and even bank sets.” *Id.* at 14:57-63. Because the timing restriction for row accesses in the memory device “is imposed primarily to avoid conflicting use of resources shared by banks in the same bank set, (e.g., row decoders shared by even banks and row decoders shared by odd banks),” “row activation operations directed alternately to the odd and even bank sets may be executed in sub-intervals” within the overall interval. *Id.* at 14:64-15:4. And “because distinct sets of column decoders and distinct data path resources are provided for the even and odd bank sets, micro-threaded column operations directed to the activated rows in alternate bank sets may be executed one after another within a single [time] interval.” *Id.* at 15:5-9. Thus, data throughput can be increased while reducing the column transaction granularity (*i.e.*, the amount of data transferred per column access (*see id.* at 1:58-60)). *Id.* at 15:16-24.

The '379 Patent describes several embodiments that make use of its micro-threaded approach to increase data throughput to/from a DRAM while reducing the column transaction granularity. *See, e.g., id.* at 14:50-23:65; 25:55-28:17; 29:15-31:40. The '379 Patent further claims a memory controller and method of operating the same in accordance with the micro-threaded approaches it teaches as further detailed in the next section.

B. Challenged Claims

The Petition challenges claims 1-22 of the '379 Patent. Claims 1, 12, and 20 are independent claims. Claims 2-11 depend from claim 1, claims 13-19 depend from claim 12, and claims 21-22 depend from claim 20. The Petition provides a listing of all the challenged claims in a Claim Appendix. Petition at 94-99 (of PDF).

Independent Claim 1 recites:

1. A memory controller to control a memory device, the memory device having a plurality of bank groups, the memory controller comprising:

 circuitry to provide a clock signal to the memory device, the clock signal having clock transitions;

 a command interface to transmit, to the memory device, row activation commands to instruct row activations and column access commands to instruct column accesses; and

circuitry to schedule issuance of the row activation commands and the column access commands from the command interface, such that

a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common bank group, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups, and

a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups.

Claim 1 is directed to a memory controller to control a memory device that has plurality of bank groups. The controller includes circuitry to schedule the row activation and column access commands such that the claimed first through fourth time intervals are necessarily observed. The first interval is the time between row activations to banks *within a common bank group*. The second interval is the time between row activations to banks *within different bank groups*. Similarly, the third interval is the time between column accesses to banks *within a common bank group*, and the fourth interval is the time between column accesses to banks *within different*

bank groups. The requirement to schedule these commands such that the claimed intervals are observed facilitates the '379 Patent's multi-threaded approach wherein a row activation in a different bank from the previous activation can occur sooner than in that same bank and subsequent column accesses.

Independent claims 12 and 20 similarly require a controller or method of operating the same that schedule row activation and column access commands in accordance with the claimed time intervals.

Claim 12 recites:

12. A memory controller to control a memory device, the memory device having a plurality of bank groups, the memory controller comprising:

circuitry to provide a clock signal to the memory device, the clock signal having clock transitions;

a command interface to transmit row activation commands and column access commands to the memory device, via a command bus;

a data interface to exchange data with the memory device in association with each column access command; and

circuitry coupled to the command interface to schedule issuance of the row activation commands and the column access commands to banks within the plurality of bank groups, such that

a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common one of the bank groups, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different ones of the bank groups, and

a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common one of the bank groups, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different ones of the bank groups;

wherein the memory controller is to transmit bank address information as part of each command of the row activation commands and column access commands, to communicate selection of a bank group of the plurality of bank groups, and to communicate selection of a bank within the selected bank group.

Claim 20 recites:

20. A method of operation in a memory controller, the memory controller to control a memory device, the memory device having a plurality of bank groups, the method comprising:

providing a clock signal to the memory device, the clock signal having clock transitions;

transmitting to the memory device, via a command interface, row activation commands to instruct row activations and column access commands to instruct column accesses; and

scheduling issuance of the row activation commands and the column access commands from the command interface, such that

a first interval, defined by a first number of clock transitions to transpire between back-to-back row activations to banks within a common bank group, is longer than a second interval, defined by a second number of clock transitions to transpire between back-to-back row activations to banks within different bank groups, and

a third interval, defined by a third number of clock transitions to transpire between back-to-back column accesses to banks within a common bank group, is longer than a fourth interval, defined by a fourth number of clock transitions to transpire between back-to-back column accesses to banks within different bank groups.

C. Prosecution History of the '379 Patent

The independent claims of the '379 Patent were added through Preliminary Amendment. Ex. 1002 at 111-18. Claim 2 during prosecution issued as independent claim 1 following the reordering after allowance. *See id.* at 277. During prosecution,

the Examiner issued one office action rejecting the pending claims over U.S. Pat. No. 5,953,257 to Inoue. *Id.* at 162-79. The Examiner and the Applicant's attorney participated in an interview (*id.* at 251), and Applicant subsequently submitted a response presenting two new dependent claims but without amending any of the previously presented claims. *Id.* at 257-63.

In the Remarks accompanying the response, the Applicant distinguished the asserted Inoue reference on several grounds. Among these, the Applicant noted that the claims "recite a memory controller having 'circuitry to schedule issuance of the . . . commands . . . such that' four time intervals are necessarily observed." *Id.* at 264. The Applicant observed however that the figures in Inoue "appear to only show example timing seen purely internally to an embedded DRAM device, and neither Inoue[']s] description nor figures teach anything about scheduling issuance of commands to a memory device (which is the subject of Applicant's claims) so that four time periods are observed." *Id.* at 264-65 (emphasis in original).

The Applicant also noted that the Inoue reference showed four banks, each with two subbanks "where each subbank has a dedicated row decoder (i.e., there are eight row decoders total as stated at Inoue's column 11, line 38), but where a column decoder is shared across each A/B pair of subbanks." *Id.* at 265 (emphasis in original). Accordingly, the Applicant explained that the reference "does not relate or have any teachings relating to scheduling of commands, as discussed above, but []

also does not show four different timing requirements between columns and rows in a memory device.” *Id.* That is, there was “no structure, implicitly or otherwise in Inoue, which restricts in any manner Inoue’s row commands can be issued to banks within a common ‘bank group,’ or how row timing differs for respective row commands sent to banks in respective bank groups versus Inoue’s subbanks.” *Id.* The Applicant highlighted the distinction in the claimed intervals between those activations “to banks within a common bank group” as opposed to different banks. *Id.* As the Applicant noted, the reference did not disclose a controller enforcing the claimed time intervals nor could it imply any such restriction between a common and different bank groups.

Following the Applicant’s Response, the Examiner issued a Notice of Allowance including the “examiner’s statement of reasons for allowance” that: “The applicant’s arguments (REMARKS:P9) regarding timing constraints are persuasive.” *Id.* at 267-73.

III. LEVEL OF ORDINARY SKILL

For the limited purpose of this Preliminary Response, Patent Owner does not contest Petitioner’s definition of a person of ordinary skill in the art, but it reserves the right to do so in the event that trial is instituted.

IV. CLAIM CONSTRUCTION

Patent Owner submits that the Board need not construe any claim term in a particular manner to arrive at the conclusion that the Petition is substantively deficient. *See Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“need only be construed ‘to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))). Patent Owner expressly reserves the right to address any and all claim constructions in the Petition whether explicit or implicit if trial were to be instituted or in any other or subsequent proceedings.

V. APPLICABLE LEGAL STANDARDS

The Board may only grant a petition for *inter partes* review where “the information presented in the petition ... shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); 37 C.F.R. § 42.108(c). Petitioner bears the burden of showing that this statutory threshold has been met. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756 (Aug. 14, 2012) (“The Board ... may institute a trial where the petitioner establishes that the standards for instituting the requested trial are met”).

A. Obviousness

Section 103 of the Patent Act provides that “[a] patent may not be obtained . . . if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a). The obviousness analysis requires several threshold inquiries: the level of ordinary skill in the art must be established; the scope and content of the prior art must be determined; and any differences between the prior art and the claims at issue must be ascertained. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

1. Claims cannot be found obvious if an element is absent.

If a single element of the claim is absent from the prior art, the claim cannot be considered obvious. *See CFMT, Inc. v. YieldUp Int’l Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003) (“Obviousness requires a suggestion of all limitations in a claim.”) (citing *In re Royka*, 490 F.2d 981, 985 (C.C.P.A. 1974)); *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversing obviousness rejection where prior art did not teach or suggest all claim limitations); *Garmin Int’l, Inc. v. Patent of Cuozzo Speed Techs. LLC*, IPR2012-00001, Paper 15 at 15 (PTAB Jan. 9, 2013) (refusing to institute an *inter partes* review under 35 U.S.C. § 103 where prior art did not disclose all claim limitations).

Additionally, it is improper to use the challenged claim as a roadmap to piece together disparate disclosure using hindsight bias. See *InTouch Techs., Inc. v. VGo Comm'ns., Inc.*, 751 F.3d 1327, 1351 (Fed. Cir. 2014) (reversing obviousness where “[i]t appears that [the expert] relied on the [] patent itself as her roadmap for putting what she referred to as pieces of a ‘jigsaw puzzle’ together.”); *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007) (“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning.”).

2. A petition must address the Graham factors.

Obviousness is resolved on a number of factual determinations “including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of ordinary skill in the art.” See *Graham*, 383 U.S. at 17-18. Petitions for *inter partes* reviews “must address the Graham factors.” *Eizo Corp. v. Barco N.V.*, IPR2014-00358, Paper 11 at 29-30 (PTAB July 23, 2014).

3. A petition must provide articulated reasoning with rational underpinning to combine and/or modify references.

The conclusion of obviousness based on a combination of references must also be supported with explicit analysis of a reason to combine those references. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). The Federal Circuit has stated that such reasons must be more than “mere conclusory statements; instead, there

must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006); *accord Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 (Fed. Cir. 2008) (agreeing with the district court’s reasoning that “some kind of motivation must be shown from some source, so that the jury can understand why a person of ordinary skill would have thought of either combining two or more references or modifying one to achieve the patented method”); *see also LG Elecs., Inc. v. Cellular Commc’ns Equip. LLC*, IPR2016-00197, Paper 7 at 7-11 (PTAB April 29, 2016) (faulting a petition’s obviousness analysis for lack of sufficient articulated reasons with rational underpinnings for modifying references to achieve particular elements required in the claims).

Furthermore, “[d]emonstrating that a reference is analogous art or relevant to the field of endeavor of the challenged patent is not sufficient to establish that one of ordinary skill would have had reason to combine its teachings with other prior art in the manner set forth in the claim.” *Johns Manville Corp. v. Knauf Insulation, Inc.*, IPR2018-00827, Paper 9 at 10 (PTAB Oct. 16, 2018) (citing *See Securus Techs., Inc. v. Global Tel*Link Corp.*, 701 F. App’x 971, 977 (Fed. Cir. 2017) (“a broad characterization of [prior art references] as both falling within the same alleged field . . . without more, is not enough for [Petitioner] to meet its burden of presenting a sufficient rationale to support an obviousness conclusion”)). “Mere compatibility of

the references is likewise not sufficient.” *Id.* (citing *Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993 (Fed. Cir. 2017) (it is not enough to show that “a skilled artisan, once presented with the two references, would have understood that they could be combined”).

VI. SUMMARY OF THE PRIOR ART REFERENCES

Petitioner relies on the LaBerge, Bowater, and Fujioka references in the proposed grounds addressed to the independent claims. Because the other references are only included in grounds addressed to dependent claims (Grounds 2-6, 8-9) or in the case of Wilcox is addressed to aspects of the independent claims not at issue in this Preliminary Response (Grounds 7-11), Patent Owner reserves the right to address these other references and any related arguments if *inter partes* review is instituted. A brief summary of the LaBerge, Bowater, and Fujioka references follows.

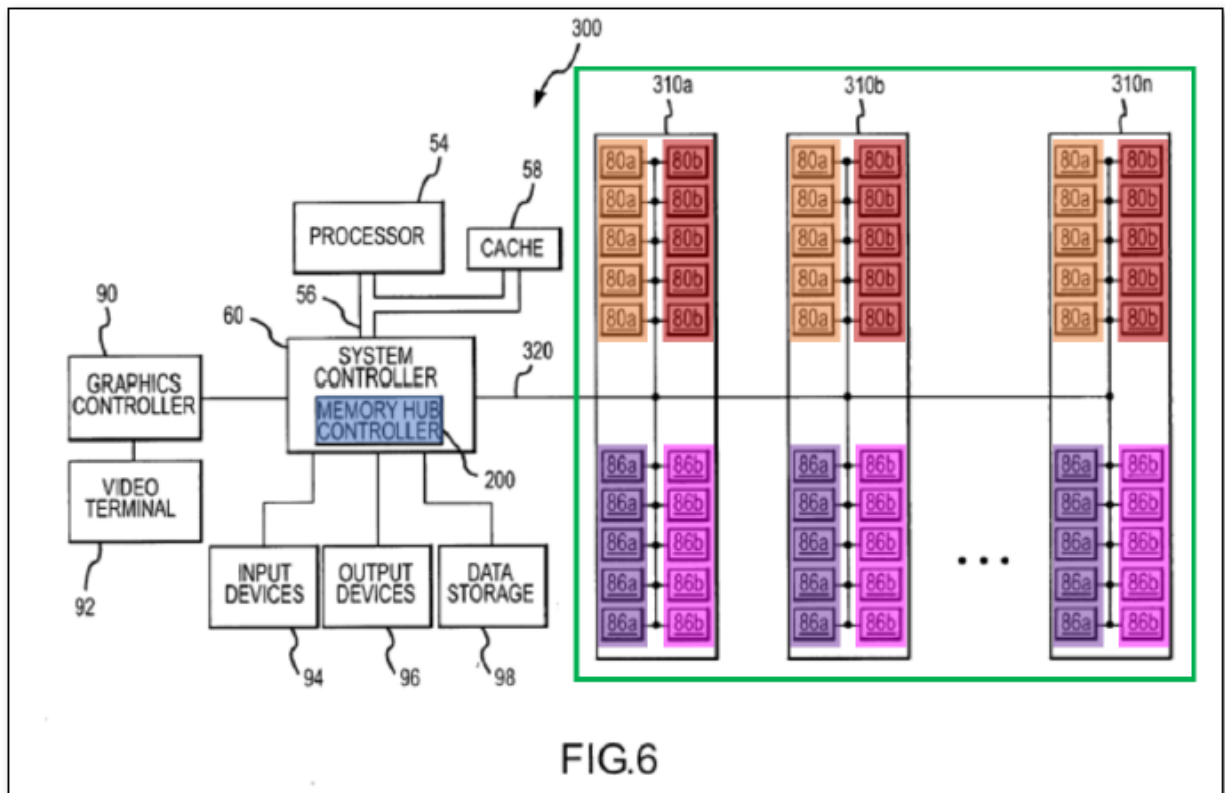
A. Overview of LaBerge

Petitioner relies on U.S. Patent Application Publication No. 2005/0177690 to LaBerge as a reference in each of Grounds 1 through 11. Petition at 5. LaBerge “relates to memory modules having memory devices mounted on opposite surfaces of a substrate.” Ex. 1006 at [0001]. LaBerge explains that “[m]emory modules are generally in the form of an insulative substrate, such as a printed circuit board,

having several memory devices mounted on one or both surfaces of the substrate.”

Id. at [0004].

The Petition relies on LaBerge, and in particular its Figure 6, for all the limitations of the independent claims except the claimed time intervals (*compare* e.g. Petition at 9-18 *with id.* at 19-35):



Ex. 1006, Fig. 6 (annotated by Petitioner; see Petition at 9).

LaBerge discloses that “memory devices 80 *a,b*” are “on one side of the memory module” and “memory devices 86 *a,b*” are “on the other side of the memory module” each with their own “command, address and data buses.” Ex. 1006 at [0023]; *see also id.* at [0039] (noting that “components [common to Figure 4] have

been provided with the same reference numerals” in Figure 6). In Figure 6, reference numerals 310a, 310b, etc. are the memory modules that incorporate memory devices 80 and 86. *Id.* at [0039].

Petitioner asserts that the memory modules 310a, 310b, etc. are the claimed “memory device” and that the memory devices of LaBerge each constitute a bank. *See* Petition at 10. Aside from arbitrarily substituting the language of the claims for the plain disclosure of LaBerge, the Petition overlooks the functional distinctions between the claimed memory devices and banks of the ’379 Patent and LaBerge’s modules and devices. As noted, each of LaBerge’s modules includes memory devices 80 *a,b* and 86 *a,b*. LaBerge’s devices themselves are a group of memory integrated circuits (ICs) which do not constitute a singular bank. Each of the memory ICs comprise ranks operating in parallel, i.e. simultaneously and identically, as opposed to independently as in the groups of banks in the ’379 Patent. More to the point, the Petition’s alleged “memory device” in LaBerge is not a “memory device having multiple storage arrays that share addressing and/or data path resources in a manner that imposes timing constraints on sequential accesses directed to the different storage arrays” as described in the ’379 Patent. Ex. 1001 at 4:55-62. Thus, LaBerge not only fails to disclose anything about “schedule[ing] issuance of the row activation commands and the column access commands from the command interface, such that” the four claimed time intervals are satisfied (and the Petition

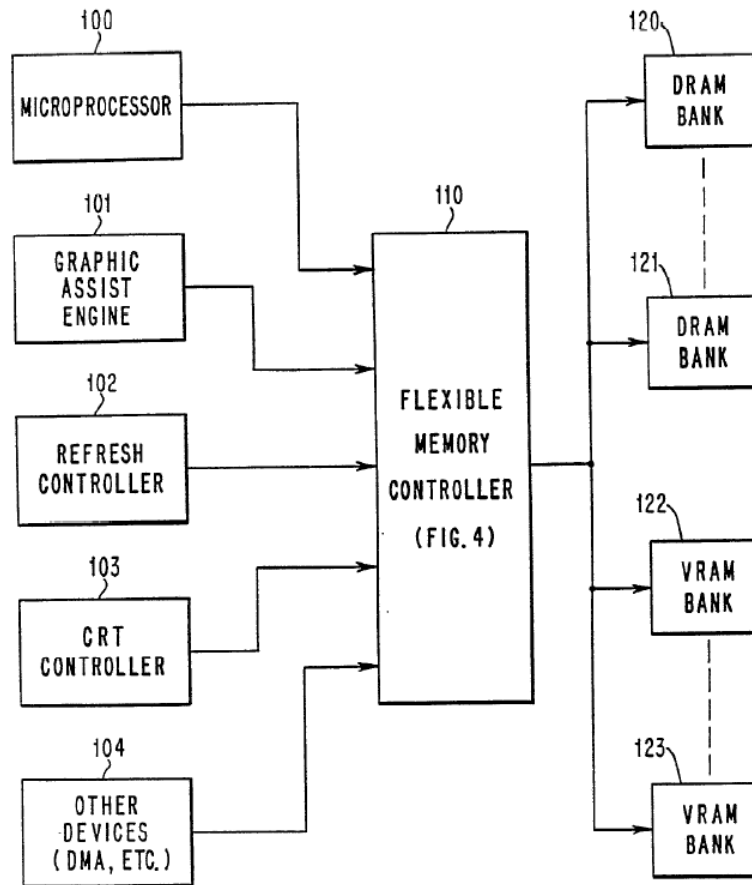
does not allege that it does, *see, e.g.*, Petition at 19-35), but the structure of LaBerge, like the Inoue reference distinguished during prosecution, has no structure, implicitly or otherwise restricting the issuance of commands to what Petition asserts is a bank group that would call for addition of the claimed time intervals.

B. Overview of Bowater

Petitioner relies on EP 0339224 to Bowater et al. as a reference in each of Grounds 1 through 11 in combination with LaBerge and other references. Petition at 5. Bowater was identified during prosecution and is cited on the face of the '379 Patent. *See* Ex. 1001 at 3; *see also* Petition at 86.

Bowater discloses that its objective “is to provide a flexible dynamic memory controller operable with dynamic RAMS having a wide range of operating characteristics is described, including different operating speeds for various memory functions, and the usage of memories.” Ex. 1007 at 3:5. Figure 3 of Bowater “is a block diagram of a memory controller according to the invention” (*id.* at 3:24):

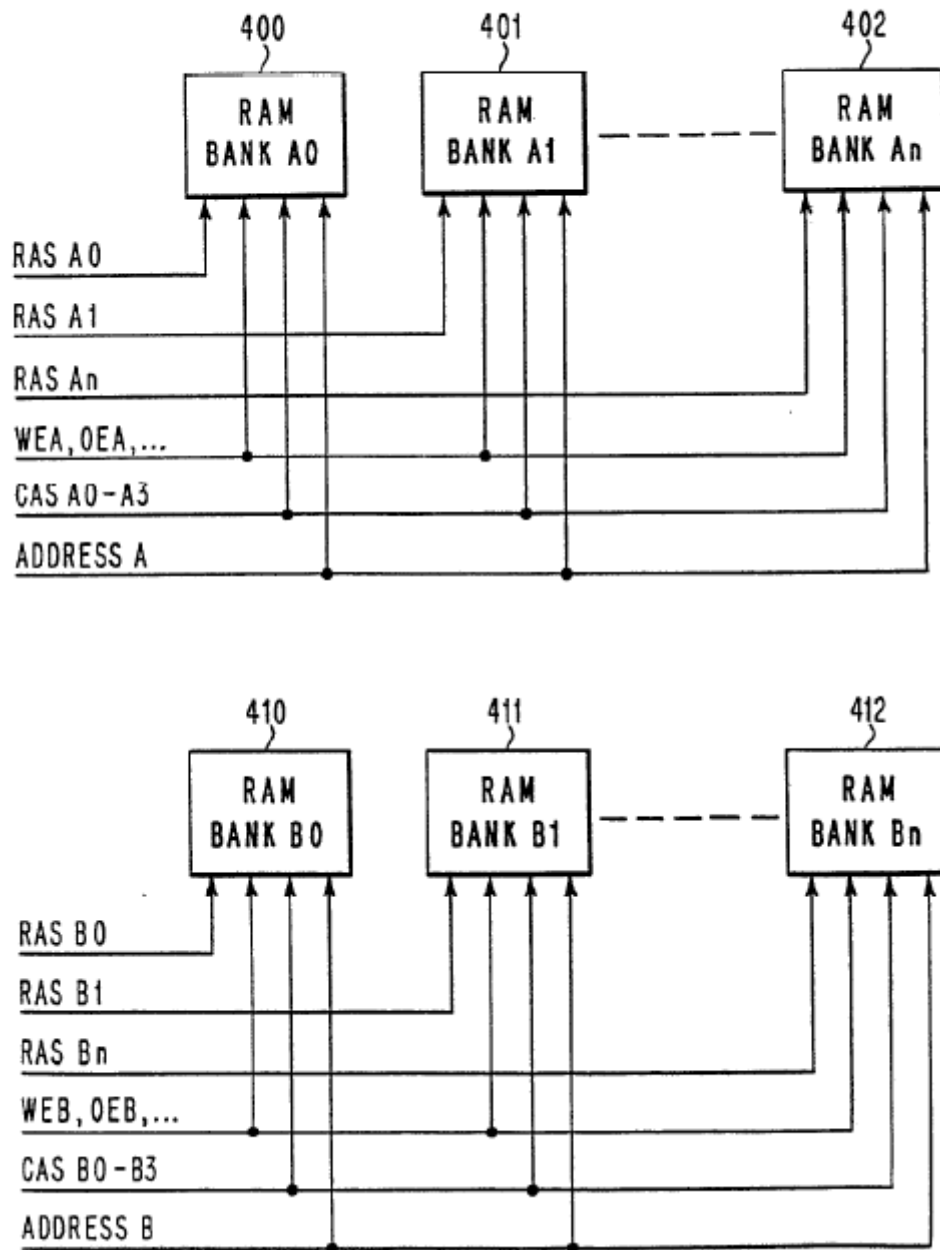
FIG. 3



Ex. 1007, Fig. 3.

Figure 3 includes a flexible memory controller and what it refers to as banks of memory 120-123. *Id.* at 4:41-43. Bowater also refers to these as “Memory modules 120-123” and states that they are “arranged in banks.” *Id.* at 5:4. “Each bank of memory contains several modules such that a bank is a complete word plus other bits optionally present for error detection and correction (EDC).” *Id.* at 5:4-5. As shown in Figure 6, Bowater’s “banks” are completely separate and share only a common data bus to the controller:

FIG. 6



Ex. 1007, Fig. 6.

Because the different “banks” are separate memory ICs, so long as there is no conflict on the data bus, the operation of them is completely independent. Once

again the structure of Bowater, like LaBerge and the Inoue reference addressed during prosecution, neither discloses nor implies anything about the bank-to-bank timing differences within a memory device as addressed in the '379 Patent.

Moreover, Bowater's objective is to disclose a flexible memory controller that can work with DRAMs with different operating characteristics. Ex. 1007 at 3:5. To that end, Bowater discloses a programmable state machine such that the controller can be "individually programmed" to work with different "banks" of memory "to maintain optimum performance." *Id.* at 4:11-15. There is no mention of managing performance of different banks within a single memory device or the timing constraints that requires. Bowater discloses a timing diagram in Figure 2 which the Petition relies on to show the claimed time intervals. But, there is no disclosure or suggestion in Bowater of scheduling the memory commands to achieve any particular timing relationship between the different banks as described and claimed in the '379 Patent. Again, like the Inoue reference addressed during prosecution, the Petition's assertion that the timing diagram discloses the claimed time intervals without any teaching or suggestion that such timing is and should be scheduled such that those timing relationships should occur does not render the '379 Patent's time interval limitations obvious. And it further does not teach or suggest somehow overlaying those timing relationships with fundamentally

different circuitry in LaBerge, or any other reference, that neither call for nor are compatible with the invention described in Bowater.

C. Overview of Fujioka

Petitioner relies on U.S. Patent No. 6,185,149 to Fujioka et al. as a reference in Ground 12 addressed to independent claims 1 and 20. Petition at 5. Fujioka was identified during prosecution and is cited on the face of the '379 Patent. *See* Ex. 1001 at 2; *see also* Petition at 86.

Fujioka discloses a memory device—not a controller. *See* Ex. 1004, *Title, generally*. The Petition alleges that a clock buffer and a predecoder 11 are a memory controller (*see, e.g.,* Petition at 70-76), but even as a collection these do not control nor do they schedule the issuance of commands to a memory device. For example, the Petition labels “Predecoders 11 of bank-0 circuit 7 and bank-1 circuit 8 (*command interface*),” i.e. asserting that it is the claimed “command interface.” Petition at 74 (*italics for claim language in original*). But the claim requires “a command interface to transmit, to the memory device, row activation commands to instruct row activations and column access commands to instruct column accesses.” Ex. 1001, Cl. 1. Fujioka explains however that “[t]he predecoder 11 latches and predecodes the address signal supplied.” Ex. 1004 at 6:29-31. That is, it predecodes addresses not commands.

Fujioka, much like the Inoue reference distinguished during prosecution, describes only timing seen internally to a DRAM and teaches nothing about scheduling issuance of commands to a memory device to obtain the claimed time intervals or address the problems the '379 Patent addresses.

VII. THE PETITION DOES NOT ESTABLISH A REASONABLE LIKELIHOOD OF SUCCESS

To justify the institution of an *inter partes* review, a petitioner must establish that there is a “reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). Petitioner has not met its burden of establishing a reasonable likelihood of success at least because the Petition fails to show that one of ordinary skill would have chosen to combine the cited elements to achieve the claimed inventions of the '379 Patent. Consequently, the Board should deny the Petition and decline to institute the *inter partes* review.

A. The Petition Fails to Demonstrate Obviousness of Any Independent Claims.

Petitioner has failed to demonstrate that any of independent claims 1, 12, or 20 is obvious over the cited combinations in Grounds 1, 7, or 12. Because the remaining challenged claims all depend from these independent claims, should the Board agree that trial should not be instituted on these independent claims, it necessarily follows that trial should not be instituted on the dependent claims in the

remaining grounds. Accordingly, Patent Owner focuses on at least some of the flaws in Grounds 1, 7, and 12 addressed to the independent claims.

1. Ground I: LaBerge & Bowater Fail to Render Independent Claims 1 or 20 Obvious.

Petitioner’s proposed combination of LaBerge and Bowater at least fails to teach or suggest the limitation of claim 1 requiring “circuitry to schedule issuance of the row activation commands and the column access commands . . . such that” the four claimed time intervals are satisfied. *See* Ex. 1001, Cl. 1; *supra* Section II.B. As set forth above, LaBerge does not disclose a memory controller for a memory device with a plurality of banks, but even under Petitioner’s application of the claim limitations to the structures in LaBerge, there is no disclosure or suggestion in LaBerge that it could or should be used with circuitry that schedules the claimed commands such that the four time intervals are preserved. *See supra* Section VI.A. And the Petition does not suggest that it does.

Bowater likewise fails to disclose or suggest the claimed circuitry to schedule issuance of commands to satisfy the four time intervals. *See supra* Section VI.B. The separate integrated circuits in Bowater are not part of a common memory device and operate independently such that there is not only no disclosure but also no suggestion that circuitry to schedule commands in accordance with the claimed time intervals would be necessary or desirable.

The Petition offers no additional argument for its combination for independent method claim 20, and accordingly the proposed combination fails to render it obvious for the same reasons. *See* Petition at 44.

2. Ground VII: LaBerge, Bowater, and Wilcox Fail to Render Independent Claim 12 Obvious.

The Petition asserts the combination of LaBerge and Bowater along with the Wilcox reference to address independent claim 12 and an additional limitation not present in claim 1 or 20. The Petition offers no additional argument or explanation with respect to the limitations [12e]-[12h] regarding the circuitry to schedule issuance of commands such that the four time intervals are observed. Petition at 68. Accordingly, the proposed combination fails to render claim 12 obvious for at least the same reasons identified in the previous section with respect to LaBerge and Bowater. *See supra* Section.V.A.1; *see also* Section VI.A and VI.B.

3. Ground XII: Fujioka Fails to Render Independent Claims 1 or 20 Obvious.

Petitioner’s proposed modification of Fujioka fails to teach or suggest at least the claimed “command interface . . .” and, like the above combinations, also fails to teach or suggest a memory controller with “circuitry to schedule issuance of the row activation commands and the column access commands . . . such that” the four claimed time intervals are satisfied. *See* Ex. 1001, Cl. 1; *supra* Section II.B. As set forth above, Fujioka does not even disclose a memory controller and the structures

the Petition relies on as the claimed “command interface” cannot provide the requisite functionality. *See supra* Section.VI.C. Moreover, Fujioka, much like the art that was distinguished during prosecution, discloses only internal DRAM signals and teaches nothing about scheduling issuance of commands to the device to obtain the claimed time intervals.

The Petition offers no additional argument for Fujioka for independent method claim 20, and accordingly the proposed combination/modification fails to render it obvious for the same reasons. *See* Petition at 86.

VIII. PATENT OWNER’S FINAL COMMENTS

Patent Owner does not concede the legitimacy of any arguments in the Petition that are not specifically addressed herein, and expressly reserves the right to rebut any such arguments in its Patent Owner Response if *inter partes* review is instituted. Similarly, Patent Owner also does not concede any underlying contentions in the Petition and reserves the right to rebut them later. Additionally, Patent Owner is not limited to the arguments presented here in this Preliminary Response, but expressly reserves the right to raise further arguments, including claim construction arguments, not presented in this Preliminary Response.

IX. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board decline to institute *inter partes* review of the ’379 patent.

Dated: December 23, 2024

By: /s/ David T. DeZern

David T. DeZern

Registration No. 60,117

NELSON BUMGARDNER

CONROY P.C.

2727 North Harwood Street, Ste. 250

Dallas, Texas 75201

Telephone: (214) 446-4950

Email: david@nelbum.com

Justin B. Kimble

Registration No. 58,591

NELSON BUMGARDNER

CONROY P.C.

2727 North Harwood Street, Ste. 250

Dallas, Texas 75201

Telephone: (214) 446-4950

Email: justin@nelbum.com

Attorneys for Patent Owner

CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that this Preliminary Response complies with the type-volume limits of 37 C.F.R. § 42.24(b)(1) because it contains 5,509 words, excluding the parts of this Patent Owner's Preliminary Response that are exempted by 37 C.F.R. § 42.24(a), according to the word processing system used to prepare this Patent Owner's Preliminary Response.

Dated: December 23, 2024

By: /s/ David T. DeZern

David T. DeZern

Registration No. 60,117

NELSON BUMGARDNER

CONROY P.C.

2727 North Harwood Street, Ste. 250

Dallas, Texas 75201

Telephone: (214) 446-4950

Email: david@nelbum.com

Justin B. Kimble

Registration No. 58,591

NELSON BUMGARDNER

CONROY P.C.

2727 North Harwood Street, Ste. 250

Dallas, Texas 75201

Telephone: (214) 446-4950

Email: justin@nelbum.com

Attorneys for Patent Owner

CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing Patent Owner's Preliminary Response was served on December 23, 2024, to Lead and Back-up Counsel for Petitioner at the service address provided in Petitioner's Mandatory Notices:

Email: Jeffrey.Johnson@bakerbotts.com

Ellyar.Barazesh@bakerbotts.com

Robert.Benson@bakerbotts.com

DLSiliconIPR379@bakerbotts.com

Dated: December 23, 2024

By: /s/ David T. DeZern

David T. DeZern

Registration No. 60,117

NELSON BUMGARDNER

CONROY P.C.

2727 North Harwood Street, Ste. 250

Dallas, Texas 75201

Telephone: (214) 446-4950

Email: david@nelbum.com

Justin B. Kimble

Registration No. 58,591

NELSON BUMGARDNER

CONROY P.C.

2727 North Harwood Street, Ste. 250

Dallas, Texas 75201

Telephone: (214) 446-4950

Email: justin@nelbum.com

Attorneys for Patent Owner