UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SILICON MOTION INC.

Petitioner

v.

K. MIZRA LLC

Patent Owner

Case No. IPR2024-01240

Patent No. 9,160,466

PETITION FOR *INTER PARTES* REVIEW OF CLAIMS 1-19 OF U.S. PATENT NO. 9,160,466

TABLE OF CONTENTS

Page

I. MANDATORY NOTICES 1

II. STANDING AND FEES 2

III. OVERVIEW OF THE '466 PATENT 3

A. Subject Matter of the '466 Patent 3

B. Prosecution History of the '466 Patent 6

C. Priority Date of the '466 Patent 7

IV. SUMMARY OF PRIOR ART 7

A. Meaney (Ex. 1004) 7

B. Nguyen (Ex. 1005) 8

C. Greeff (Ex. 1006) 9

D. Allee (Ex. 1007) 10

E. Summary of Grounds 11

V. INSTITUTION IS PROPER 12

VI. LEVEL OF ORDINARY SKILL IN THE ART 13

VII. CLAIM CONSTRUCTION 13

VIII. A REASONABLE LIKELIHOOD EXISTS THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE 14

A. Ground 1: Claims 1, 2, 6-12, 15, and 16 are obvious over Meaney in view of the knowledge of a POSITA 14

1. Claim 1 14

2. Claim 2 21

3. Claim 6 22

4. Claim 7 23

5. Claim 8 26

6. Claim 9 26

7. Claim 10 28

8. Claim 11 32

9. Claim 12 32

10. Claim 15 33

11. Claim 16 36

B. Ground 2: Claims 1, 2, 6-12, 15, and 16 are obvious over Meaney and Nguyen in view of the knowledge of a POSITA 37

1. One of skill in the art would have been motivated to combine *Meaney* with *Nguyen* 38

2. Claim 1 40

3. Claims 2, 6, 8, 9, 11, and 12 43

4. Claim 7 43

5. Claim 10 47

6. Claim 15 49

7. Claim 16 49

C. Ground 3: Claims 4, 5, 13, 14, and 17-19 are obvious over Meaney and Greeff in view of the knowledge of a POSITA 52

1. One of skill in the art would have been motivated to combine *Meaney* and *Greeff* 53

2. Claim 4 54

3. Claim 5 55

4. Claim 13 56

5. Claim 14 57

6. Claim 17 57

7. Claim 18 62

8. Claim 19 64

D. Ground 4: Claims 4, 5, 13, 14, and 17-19 are obvious over Meaney, Nguyen and Greeff in view of the knowledge of a POSITA 64

1. One of skill in the art would have been motivated to combine *Meaney*, *Nguyen*, and *Greeff* 65

2. Claims 4, 5, 13, and 14 65

3. Claim 17 65

4. Claims 18 and 19 67

E. Ground 5A: Claim 3 is obvious over Meaney and Allee in view of the knowledge of a POSITA 67

1. One of skill in the art would have been motivated to combine *Meaney* and *Allee* 67

2. Claim 3 68

F. Ground 5B: Claim 3 is obvious over Meaney and Nguyen and Allee in view of the knowledge of a POSITA 69

1. One of skill in the art would have been motivated to combine *Meaney*, *Nguyen,* and *Allee* 69

2. Claim 3 69

IX. CONCLUSION 69

TABLE OF AUTHORITIES

Page(s)

CASES

Apple, Inc. v. Fintiv, Inc,
IPR2020-00019, Paper 11 (PTAB March 20, 2020) 12

HP Inc. v. Slingshot Printing LLC,
IPR2020-01084, Paper 13 (PTAB Jan. 14, 2021) 12

KSR Int'l Co. v. Teleflex, Inc.,
127 S.Ct. 1727 (2007).....39, 54

Micron Tech., Inc. v. Godo Kaisha IPR Bridge 1,
IPR2020-01007, Paper 15 (PTAB Dec. 7, 2020) 12

Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.,
868 F.3d 1013 (Fed. Cir. 2017) 13

Phillips v. AWH Corp.,
415 F.3d 1303 (Fed. Cir. 2005) (en banc) 13

Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.,
200 F.3d 795 (Fed. Cir. 1999) 14

STATUTES

35 U.S.C. § 103.....11

35 U.S.C. § 318(b) 69

OTHER AUTHORITIES

37 C.F.R. § 42.10(b) 2

37 C.F.R. § 42.15(a).....3

37 C.F.R. § 42.100(b) 13

37 C.F.R. § 42.104(a).....2

37 C.F.R. § 42.104(b)(4)-(5).....14

LIST OF EXHIBITS

1001	U.S. Patent No. 9,160,466 by Hampel *et al.* entitled "Periodic calibration for communication channels by drift tracking" ("the '466 Patent").
1002	Declaration of R. Jacob Baker, Ph.D., P.E., Regarding U.S. Patent No. 9,160,466.
1003	File History for U.S. Patent No. 9,160,466.
1004	U.S. Patent Publication No. 2003/0070123, Meaney, et al., "Method and system for optimizing network data transmission using a configurable protocol stack," ("*Meaney*") filed on Sept. 21, 2001 and published on April 10, 2003.
1005	U.S. Patent Publication No. 2003/0151450, Nguyen, et al., "Signaling accommodation," ("*Nguyen*") filed on May 28, 2002 and published on August 14, 2003.
1006	U.S. Patent No. 6,356,106, Greeff, et al., "Active termination in a multidrop memory system," ("*Greeff*") filed on Sept. 12, 2000 and issued on March 12, 2002.
1007	U.S. Patent No. 6,255,979, Allee, et al., "CMOS flash analog to digital converter compensation," ("*Allee*") filed on February 24, 1999 and issued on July 3, 2001.
1008	Original Complaint in *K.Mizra LLC v. Silicon Motion Inc.*, No. 2:24-cv-101 (E.D. Tex.)
1009	Return of Service in *K.Mizra LLC v. Silicon Motion Inc.*, No. 2:24-cv-101 (E.D. Tex.)
1010	U.S. Patent Publication No. 2002/0066001, Olarig, et al., "Adaptive calibration technique for high speed memory devices," ("*Olarig*") filed on Nov. 30, 2000 and published on May 30, 2002.

I. MANDATORY NOTICES

Real Party in Interest: Silicon Motion Inc. ("Petitioner") is the real party in interest. In the litigation identified below, Patent Owner added infringement claims against Silicon Motion Technology Corporation on July 26, 2024. Patent Owner has further alleged that Silicon Motion, Inc. a California corporation ("SM-US"), is an agent or alter ego of Petitioner, which Petitioner disputes. Petitioner's immediate parent company is Silicon Motion Technology (Hong Kong) Limited ("SMHK"). Solely out of an abundance of caution, Petitioner identifies these three related entities as real parties-in-interest, but Petitioner maintains that these entities do not satisfy the legal criteria for being real parties-in-interest. Neither SM-US nor SMHK have been sued by Patent Owner.

Related Matters: Petitioner has, concurrently herewith, filed a Petition for IPR against one other patent that involves substantially similar subject matter: IPR2024-01241 against U.S. Patent No. 9,111,608.

U.S. Patent No. 9,160,466 (the "'466 Patent" or "Challenged Patent") is involved in a pending lawsuit entitled, *K.Mizra LLC v. Silicon Motion Inc.*, United States District Court for the Eastern District of Texas, Case No. 2:24-CV-00101 (the "District Court Litigation"). Ex. 1008. Patent Owner asserts the '466 Patent against Petitioner in the District Court Litigation. *Id.* Petitioner was served with the complaint in the District Court Litigation on February 27, 2024. Ex. 1009.

Lead Counsel and Request for Authorization: Petitioner designates lead and back-up counsel as noted below. A Power of Attorney is filed concurrently herewith under 37 C.F.R. § 42.10(b).

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Service Information: Petitioner consents to electronic service at DLSiliconIPR466@bakerbotts.com. A Power of Attorney is filed concurrently herewith under 37 C.F.R. § 42.10(b).

II. STANDING AND FEES

Standing: Petitioner certifies under 37 C.F.R. § 42.104(a) that the U.S. Patent No. 9,160,466 is eligible for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review on the grounds set forth herein.

Fees: The Office is authorized to charge the fee set forth in 37 C.F.R. § 42.15(a) to Deposit Account No. 02-0384 as well as any additional fees that might be due in connection with this Petition.

III. OVERVIEW OF THE '466 PATENT

Petitioner challenges claims 1-19 ("Challenged Claims") of the '466 Patent, titled "Periodic calibration for communication channels by drift tracking." *See* Ex. 1001.

A. *Subject Matter of the '466 Patent*

The '466 Patent teaches methods and systems for calibration of a communication channel in a system that includes a receive component with circuitry to receive a digital signal. Ex. 1001, Abstract, Fig. 1, Fig. 3. Figure 3, reproduced below, depicts a transmit component 100 including a transmitter circuit 103 driving a data signal over link 102 to a receive component 101 including a receiver circuit 104. *Id.*, 7:31-42.

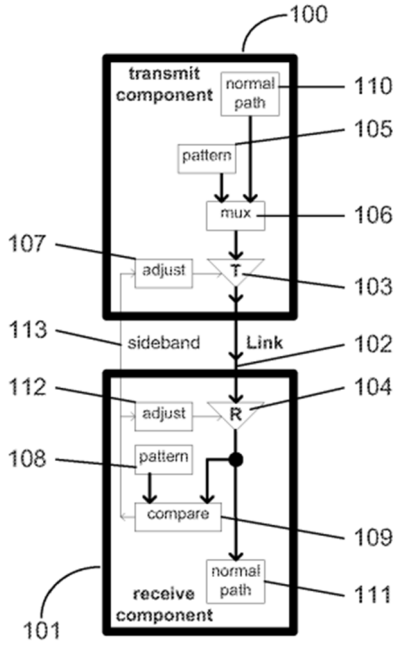


Fig. 3

The calibration methods of the ’466 Patent include a first calibration (e.g., during initialization) and a second calibration (e.g., during operation). *Id.*, Abstract. The ’466 Patent purports to have invented the use of a simplified second calibration to account for drift in timing, voltage or other parameters of a communication channel caused by changes in operation conditions, without repeating a more exhaustive initial calibration. *Id.*, 2:58-3:5.

The ’466 Patent explains that the first calibration identifies an initial value for a parameter of the communication channel, and that the first calibration may be exhaustive so that a suitable operation value can be determined for most conditions in which the system is designed to operate. *Id.*, 3:12-16, 3:33-38, 6:25-38. The ’466 Patent provides examples of the calibrated parameter as “timing parameters

specifying the drive times and sample times, voltage levels for drivers and comparators, resistance values such as link termination resistances, driver strength, adaptive equalization coefficients, noise cancellation coefficients, parameters that cause overshoot and undershoot of signals such as driver switching power or speed, and so on." *Id.*, 6:28-35.

The second calibration of the '466 Patent updates an existing value of the calibrated parameter to account for drift attributable to changes in operating conditions such as voltage or temperature. *Id.*, 2:31-3:11, 3:38-41. The second calibration of the '466 Patent is described as being performed periodically and as using less resources of the communication channel than the first calibration. *Id.*, 10:20-33.

The '466 Patent explains that these calibrations may be performed on the receive component of the communication system, which includes circuitry to receive data communicated across a channel by a transmit component. *Id.*, 7:31-42, 10:59-64. The '466 Patent explains that performing the second calibration may involve suspending operations of the receive component. *Id.*, 14:3-5.

The '466 Patent provides an example calibration technique of sending first and second data patterns from a transmit component to the receive component and comparing those data patterns to expected patterns. *Id.*, 9:22-43.

B. *Prosecution History of the '466 Patent*

The application that issued as the '466 Patent—U.S. Patent Application No. 14/535,006 ("'006 Application")—was filed Nov. 6, 2014. Ex. 1003 at 126. The '466 Patent is a continuation of co-pending U.S. Patent Application No. 14/145,966 ("'966 Application") that issued as U.S. Patent No. 8,929,424 (the "'424 Patent"), which is a continuation of U.S. Patent Application No. 13/452,543 ("'543 Application") that issued as U.S. Patent No. 8,644,419 (the "'419 Patent"), which is a continuation of U.S. Patent Application No. 12/173,530 ("'530 Application") that issued as U.S. Patent No. 8,165,187 (the "'187 Patent"), which is a continuation of U.S. Patent Application No. 11/754,107 ("'107 Application") that issued as U.S. Patent No. 7,400,671 (the "'671 Patent"), which is a continuation of U.S. Patent Application No. 10/766,761 ("'761 Application") that issued as U.S. Patent No. 7,400,670 (the "'670 Patent"). Ex. 1003 at 126.

After a preliminary amendment, the '006 application included 19 claims, of which claims 3, 12, and 19 were independent. *Id.* at 130-36.

In a first Non-Final Office Action dated February 26, 2015, the Examiner rejected claims 3-11 and 19-21 under 35 U.S.C. § 112 as lacking support in the specification for the limitation "a digital signal," as recited in claims 3 and 19. *Id.* at 69-76. The Examiner also rejected claims 12-18 on the ground of nonstatutory obviousness-type double patenting over U.S. Patent No. 8,929,424. *Id*. Applicant

filed a terminal disclaimer over U.S. Patent No. 8,929,424 and argued against the 35 U.S.C. § 112 rejection as inadequately supported and factually false, as the specification refers to transmission of bits and bytes and thus digital signals. *Id.* at 61-65. The Examiner approved the terminal disclaimer, withdrew the 35 U.S.C. 112 rejection, and allowed the application. *Id.* at 8-14.

C. *Priority Date of the '466 Patent*

The '466 Patent purports to claim priority to January 28, 2004. Petitioner relies on prior art that pre-dates January 28, 2004.

IV. SUMMARY OF PRIOR ART

Because the application that issued as the '466 Patent claims to have an effective filing date before March 16, 2013, it was examined under the pre-AIA first to invent provisions.

A. *Meaney* (Ex. 1004)

Meaney refers to U.S. Patent Publication No. 2003/0070123, which was filed on September 21, 2001 and published on April 10, 2003. Ex. 1004. *Meaney* is thus prior art to the '466 Patent under pre-AIA 35 U.S.C. §§ 102(a) and 102(e).

Meaney describes an apparatus and method for recalibrating a source-synchronous pipelined interface with minimal impact on a running system which allows a computer system to remain operational despite environmental drift or degradation. Ex. 1004, [0001].

Meaney explains that in symmetric multiprocessing (SMP) systems, managing latencies on cards, wires, or boards that exceed data cycle times is crucial, including source-synchronous pipelined interfaces that capture data within a precise timing window, which requires initial calibration with a known data pattern. Ex. 1004, [0003]-[0004]. *Meaney* further explains that over time, these interfaces can drift due to environmental changes (e.g., temperature), which can lead to system failures. Ex. 1004, [0005]-[0006].

Meaney states that it solves this problem by providing periodic recalibration with minimal disruption by putting the system into a wait state, performing fast initialization, and resuming operation. Ex. 1004, [0009]-[0012]. The recalibration is a simplified form of the initial calibration, using one less clock centering step and sipping a data deskew step. Ex. 1004, [0013]. The system assist processor ("SAP") controls the sequence, first ensuring the interface is idle before calibration by interacting directly with hardware registers and loading calibration patterns. Ex. 1004, [0036]-[0038]. The recalibration logic re-centers the clock efficiently, optimizing the timing window to adapt to environmental changes. Ex. 1004, [0040]. Upon completion, the system resumes normal operation, maintaining precise timing and continuous functionality. Ex. 1004, [0041].

B. *Nguyen* (Ex. 1005)

Nguyen refers to U.S. Patent Publication No. 2003/0151450, which was filed

on May 28, 2002 and published on August 14, 2003. Ex. 1005. *Nguyen* is thus prior art to the '466 Patent under pre-AIA 35 U.S.C. §§ 102(a) and 102(e).

Nguyen describes methods for applying offsets to existing values to determine a calibrated value. Ex. 1005, [0065]. This technique ensures that the reference voltage is accurately set to match the common mode voltage of received signals, thus maintaining signal integrity. *Id.*, [0004], [0059]-[0064].

Nguyen also discloses circuitry including components for receiving a digital signal and calibrating computer system parameters. *Id.*, [0083]-[0086]. A digital calibration component determines high and low compensated voltage failure points and calculates a midpoint value to set the reference voltage, ensuring it matches the common mode voltage of the received signal. *Id.*, [0083]-[0086].

Additionally, *Nguyen* details a parameters table for storing calibration data for different transmitting units. *Id.*, [0075]-[0078], [0098]-[0100]. This allows the system to dynamically adjust the reference voltage based on the specific characteristics of each unit and environmental conditions. *Id.*, [0100], [0147].

C. *Greeff* (Ex. 1006)

Greeff refers to U.S. Patent No. 6,356,106, which was filed on September 12, 2000 and issued on March 12, 2002. Ex. 1006. *Greeff* is thus prior art to the '466 Patent under pre-AIA 35 U.S.C. §§ 102(a), 102(b) and 102(e).

Greeff describes a system that addresses the issues of signal reflections and integrity in digital systems through an active termination scheme that integrates termination circuits within the devices connected to a multidrop bus rather than on the system's printed circuit board ("PCB"). Ex. 1006, Abstract, 1:5-20. *Greeff* states that this integration allows for selective enabling or disabling of termination based on the device location and communication traffic, thereby reducing cost and conserving PCB space. Ex. 1006, Abstract, 2:13-34.

A key aspect of *Greeff* is the calibration of termination resistance and driver strength to optimize signal integrity. Ex. 1006, 4:11-14, 6:3-6, 7:52-8:62. *Greeff* discloses adjusting the termination resistance during a calibration process that can be either static (performed after system configuration) or dynamic (adjusted during system operation) to account for variations in process, voltage, or temperature. Ex. 1006, 7:52-8:3.

D. *Allee* (Ex. 1007)

Allee refers to U.S. Patent No. 6,255,979, which was filed on February 24, 1999 and issued on July 3, 2001. Ex. 1007. *Allee* is thus prior art to the '466 Patent under pre-AIA 35 U.S.C. §§ 102(a), 102(b) and 102(e).

Allee provides a system including a plurality of comparators, each receiving differential input and reference signals to generate output signals. Ex. 1007, Abstract. A self-calibration circuit within the system adjusts these differential reference

signals to mitigate noise from digital switching, ensuring accurate signal processing by compensating for component mismatches and non-linearities. *Id.*, Abstract, 2:13-34. This design enhances the performance of the system in environments with significant digital switching noise. *Id*.

Each comparator in the system undergoes self-calibration to minimize input offset errors, where the reference voltage is adjusted until the comparator switches states accurately. Ex. 1007, 6:17-40. The calibration involves sequentially fine-tuning each comparator, starting from the lowest quantized level, to achieve accurate threshold points for reliable system performance. Ex. 1007, 6:17-40, 7:24-40.

E. *Summary of Grounds*

Petitioner requests cancellation of the claims on the following obviousness (35 U.S.C. § 103) grounds:

Ground	Claims	Prior Art
1	1, 2, 6-12, 15-16	*Meaney* in view of the knowledge of a POSITA
2	1, 2, 6-12, 15-16	*Meaney* and *Nguyen* in view of the knowledge of a POSITA
3	4-5, 13-14, 17-19	*Meaney* and *Greeff* in view of the knowledge of a POSITA
4	4-5, 13-14, 17-19	*Meaney*, *Nguyen* and *Greeff* in view of the knowledge of a POSITA
5A	3	*Meaney* and *Allee* in view of the knowledge of a POSITA
5B	3	*Meaney*, *Nguyen* and *Allee* in view of the

Ground	Claims	Prior Art
		knowledge of a POSITA

V. INSTITUTION IS PROPER

The factors described in *Apple, Inc. v. Fintiv, Inc*, IPR2020-00019, Paper 11 (PTAB March 20, 2020) (Precedential) ("*Fintiv-I*") favor institution.

As of this Petition, discovery has not commenced in the District Court Litigation and, although a stay motion has not yet been filed, Petitioner intends to promptly file a stay motion in the event of IPR institution. The Board has treated related factors as neutral after declining to speculate on the outcome of a stay motion. *See, e.g.*, *HP Inc. v. Slingshot Printing LLC*, IPR2020-01084, Paper 13 at 9 (PTAB Jan. 14, 2021) ("*HP*") (instituting IPR after declining to speculate on likelihood of a stay).

Institution is strongly favored where, as here, Petitioner has been "exceptionally diligent" in filing. *Micron Tech., Inc. v. Godo Kaisha IPR Bridge 1*, IPR2020-01007, Paper 15 at 15-16 (PTAB Dec. 7, 2020). The Board has made clear that "it is often reasonable for a Petitioner to wait to file its petition until it learns which claims are being asserted against it in the parallel proceeding," and here, Petitioner filed its Petition only 13 weeks after receiving infringement contentions. *Fintiv-I* at 11. In light of Petitioner's diligence, any argument comparing the timing of respective milestones between this proceeding and the District Court

Litigation would be premature.

If Patent Owner raises §314(a) arguments in a Preliminary Response, Petitioner respectfully requests the opportunity to reply prior to institution, in order to address expected schedules at that time and whether a stipulation limiting arguments to be made in the District Court Litigation would be appropriate.

VI. LEVEL OF ORDINARY SKILL IN THE ART

As of the time of the claimed invention, a POSITA would have had a bachelor's degree in Electrical Engineering, Computer Engineering, or a related field as well as at least two years of academic or industry experience in design and implementation of high-speed digital communication systems. An individual with an advanced degree in a relevant field, such as computer or electrical engineering, would require less experience in the design and implementation of high-speed digital communication systems, and vice versa.

VII. CLAIM CONSTRUCTION

Claim terms in IPRs are construed according to their "ordinary and customary meaning" to those of skill in the art. *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005) (en banc); 37 C.F.R. § 42.100(b). For the purposes of this proceeding and the grounds presented herein, Petitioner does not propose any constructions. Constructions are proposed "only to the extent necessary." *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co*., 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing

Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc., 200 F.3d 795, 803 (Fed. Cir. 1999) ("only those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy")).

VIII. A REASONABLE LIKELIHOOD EXISTS THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE

Pursuant to 37 C.F.R. § 42.104(b)(4)-(5), all of the Challenged Claims are unpatentable for the reasons set forth in detail below. Ex. 1002, ¶¶71-77. Petitioner is aware of no evidence of secondary considerations that would meaningfully rebut a finding of obviousness.

A. *Ground 1: Claims 1, 2, 6-12, 15, and 16 are obvious over Meaney in view of the knowledge of a POSITA*

Meaney teaches and/or suggests all limitations of claims 1, 2, 6-12, 15, and 16, and thus renders those claims obvious. Ex. 1002, ¶71, Appendix A ("Appx"), 1-53.

1. Claim 1

i. 1[pre] A method of operation in a system that includes a receive component having circuitry to receive a digital signal, the method comprising:

To the extent the preamble is limiting, *Meaney* discloses a "method of operation in a system that includes a receive component having circuitry to receive a digital signal." *Meaney* discloses "symmetrical computer systems, and particularly to an apparatus and method for recalibrating [a] source-synchronous pipelined interface with minimal impact to a running system." Ex. 1004, Abstract, [0001].

The computer systems and methods of *Meaney* include a "receiver" and "i logic 14" for capturing (i.e., receiving) transferred data from driver logic 11 through the interface bus 12. *Id.*, [0003]-[0004], [0023], Fig. 1 (annotated below). The receiver and/or receiver calibration logic of *Meaney* are "receive components."

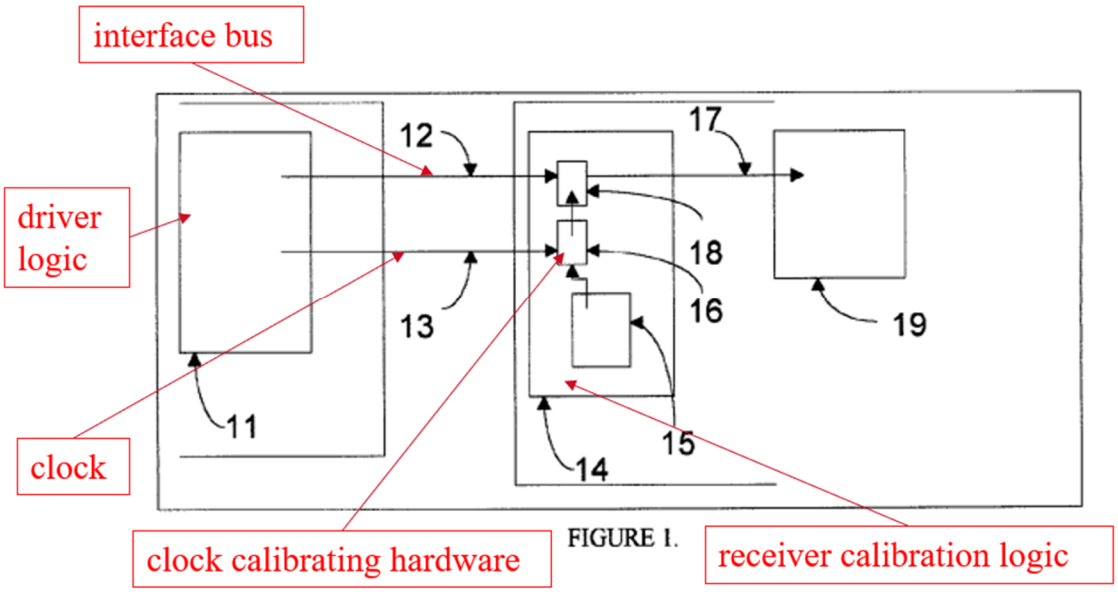


FIGURE 1.

Meaney further discusses the hardware and circuitry of its computer systems and the need to calibrate the receiver to compensate changes to the "circuit." *Id.*, [0007], [0015]-[0016], [0020]-[0021], claim 12. A POSITA would have understood that the receiver of *Meaney* would have circuitry to receive a digital signal. Ex. 1002, Appx, 1-5. Accordingly, a POSITA would have understood that *Meaney*, in view of the knowledge of a POSITA, renders obvious "[a] method of operation in a system that includes a receive component having circuitry to receive a digital signal." *Id.*

ii. 1[a] subjecting the receive component to a first calibration during initialization to identify an initial value

Meaney discloses an initial calibration of the receive component from a stopped position before the interface is in operation. Ex. 1004, [0006], [0021], [0024][1], Fig. 3; Ex. 1002, Appx, 6-8. One of the parameters calibrated to an initial value is clock delay. Ex. 1004, [0040]; Ex. 1002, Appx, 6-8. *Meaney* describes the receiver and the "receiver calibration logic" as performing calibration. Ex. 1004, [0004], [0038], Fig. 3. Specifically, *Meaney* describes the receive calibration logic of the receiver as including "clock calibrating hardware." *Id.* at [0023]. *Meaney* also discloses determining an initial value for clock delay during initialization by disclosing that future re-calibrations will be determined based on the original clock delay. *See, e.g.,* Ex. 1004, [0040] ("clock delays are reset as part of the final clock calibration sequence."); [0051] ("[f]or instance, if it is known that only the frequency changes, the change in frequency can be calculated by additional hardware and half the difference can be applied as a delay shift"); claim 12 ("recalibration []includes . . . ***re-applying the clock frequency calculation to the clock delay*** to re-center the clock") (emphasis added).

[1] While this is referred to in *Meaney* as prior art, *Meaney* states that the preferred method is "similar to the prior art calibration sequence" but includes "additional steps." Ex. 1004 at [0035]. Thus, *Meaney* is clear that the initial calibration of the clock would be part of the preferred method as well. Ex. 1002, Appx, 7.

iii. 1[b] for a parameter affecting proper reception by the circuitry of the receive component of data communicated across a channel as part of the digital signal;

Meaney discloses that the calibrated parameter (clock delay) affects proper reception by the circuitry of the receive component of data communicated across a channel as part of the digital signal. Ex. 1004, [0003], [0004], [0040]; Ex. 1002, Appx, 8-9. *Meaney* explains that in transferring data in its computer system, the data must be captured by the receiver within a small temporal window, or "eye." *Id.*; Ex. 1004, [0003]. *Meaney* further explains that the calibration of the clock delay calibration "is able to ***find the optimum data capture time for the interface***. Since the calibration is done periodically, ***this window gets reoptimized every time*** recalibration occurs." Ex. 1004, [0040] (emphasis added). *Meaney* states that this allows the receiver to recalibrate to new conditions such as changes to cycle time, voltage, or the computing environment. *Id.*

iv. 1[c] periodically subjecting the receive component to a second calibration to update an existing value of the parameter for drift attributable to change in at least one of operating voltage or temperature; and

Meaney discloses periodically subjecting the receive component to a second calibration in the form of a "recalibration." Ex. 1004, [0008] ("The invention allows for the re-calibration of the interface at periodic intervals."); [0009], [0038]. As discussed above, *Meaney* discloses identifying an initial value for clock delay,

which discloses the "existing value of the parameter." *Supra* Section VIII.A.1.ii. Alternatively, because *Meaney* discloses several periodic recalibrations, the output value from previous recalibrations would be the existing value for the next recalibration. Ex. 1004, [0008], [0016], [0040].

Meaney discloses that the recalibrations of the clock delay allow the receiver to compensate for "drift over time on the interface to compensate for temperature, voltage, cycle time, and end-of-life degradation." *Id.*, Abstract, [0015], [0016], [0040]; Ex. 1002, Appx, 9-10. Specifically, *Meaney* refers to recalibrating the receiver to update the clock delay to account for "cycle time, voltage, or other changes [] made to the environment for testing," and states that the recalibration allows the receiver to recalibrate to the new conditions. Ex. 1004, [0040]. A POSITA would have understood this as rendering obvious "subjecting the receive component to a second calibration to update an existing value of the parameter for drift attributable to change in at least one of operating voltage or temperature." Ex. 1002, Appx, 9-10.

v. 1[d] wherein the existing value is dependent on the initial value

Meaney discloses that the existing value of clock delay is dependent on the initial value identified by the first calibration. Ex. 1002, Appx, 10-13. As discussed above, *Meaney* discloses two alternative values that can be the claimed existing value: the initial value for clock delay or a clock delay value that was

determined from previous recalibrations. *See* Section VIII.A.1.iv. (citing Ex. 1004, [0008], [0016], [0040]).

A POSITA would have understood that either alternative of the "existing values" of *Meaney* are dependent on the initial value. Ex. 1002, Appx, 10-13. In the first instance, the initial value is copied or adopted as the existing value to be used as the starting point for the next calibration. *Id.*

In the second instance, the output of a previous recalibration depends on the initial value for clock delay because it is necessarily determined, directly, or indirectly, based on one or more recalibrations of the initial value for clock delay. *Id. Meaney* explains that recalibration reoptimizes the window for data capture by recalibrating the existing clock delay to account for changes in conditions, and discloses that this recalibration occurs without resetting the hardware. Ex. 1004, [0033], [0040], [0051]. A POSITA would have understood that these recalibrations would be performed based on the existing clock delay value. Ex. 1002, Appx, 11. For the first recalibration performed after the initial calibration, the initial value would be used as a starting point in the recalibration to generate a new clock delay, which was generated based on the initial clock delay value. *Id.* For the next recalibration, the starting point (the claimed "existing value") would be the new clock delay, which was generated from, and thus dependent on, the initial value. *Id*. For example, *Meaney* discloses that the clock can be recalibrated by "adding delay"

to the clock path or applying a delay shift to the existing clock delay. Ex. 1004, [0040], [0051]; Ex. 1002, Appx, 11.

To the extent Patent Owner argues that *Meaney* does not disclose the existing value being dependent on the initial value, in light of the disclosure of "adding delay" and "delay shifts" in *Meaney*, a POSITA would have found it obvious to modify *Meaney* to use the initial value as the starting point and apply the results of the calibration to that value to determine a calibrated value. Ex. 1002, Appx, 11. Moreover, *Meaney's* disclosure of "adding delay" necessarily requires an initial value to be present—otherwise there would nothing to which to add delay. *Id.*

vi. 1[e] and wherein the second calibration is constrained to occur during a time period that is shorter than a time period of the first calibration.

Meaney discloses that the recalibration is faster and has fewer steps than the initial calibration performed during the original initialization process. Ex. 1004, [0008], [0013], [0038]-[0039]. Specifically, *Meaney* discloses that recalibration is performed using a "fast initialization" process that can occur with minor disruption to the computer system by skipping certain steps (e.g., a data deskew and a clock centering step) that are performed during the original initialization process. Ex. 1004, [0008], [0013], [0038], Fig. 3. Moreover, the initial calibration of *Meaney* is performed from a stopped position, whereas the recalibration merely requires putting the system in a "wait" state for the duration of the recalibration. Ex. 1004, [0024],

[0035], [0039], [0041]. Accordingly, a POSITA would have understood that the recalibration of *Meaney* would occur during a time period that is shorter than the time period of *Meaney's* initial calibration. Ex. 1002, Appx, 13-14. Thus, a POSITA would have understood that *Meaney* discloses "the second calibration is constrained to occur during a time period that is shorter than a time period of the first calibration."

2. Claim 2

i. The method of claim 1, wherein periodically subjecting includes calculating an interval and repeatedly (a) performing the second calibration at each expiration of the interval and (b) resetting the interval.

Meaney discloses performing recalibration in "periodic intervals" and states that the recalibration method can be "triggered periodically." Ex. 1004, [0008], [0015], claim 5. Accordingly, a POSITA would have understood the disclosure of *Meaney* to disclose "calculating an interval and repeatedly (a) performing the second calibration at each expiration of the interval and (b) resetting the interval." Ex. 1002, Appx, 14-15. To be triggered in periodic intervals, *Meaney* necessarily must involve calculating the interval, repeating the recalibration when the interval is expired, and resetting the interval between recalibrations. *Id.*

To the extent Patent Owner argues this limitation is not taught by *Meaney*, it would have been obvious to a POSITA to modify *Meaney* to have the interval be calculated and repeatedly reset between recalibrations. Ex. 1002, Appx, 15. *Meaney*

discloses that periodic recalibration allows the system to ensure that changes to the circuitry or environmental characteristics do not adversely affect performance over time. Ex. 1004, [0016]. To achieve this objective, it would have been obvious to a POSITA to calculate an interval based on, for example, an expected time it would take an environmental characteristic (e.g., change in temperature) to affect performance, and then repeatedly recalibrate the system based on that calculated interval. Ex. 1002, Appx, 15. Periodic recalibration based on intervals using timers were well known at the time of the '466 Patent. Ex. 1002, Appx, 15; Ex. 1010, [0042].

3. Claim 6

i. The method of claim 1, wherein the second calibration uses less resources of the channel than the first calibration.

As discussed above in Section VIII.A.1.vi, *Meaney* discloses that a second calibration (*Meaney's* recalibration) is faster and has fewer steps than a first calibration, i.e., the initial calibration performed during the original initialization process. Ex. 1004, [0008], [0013], [0038]-[0039]. Specifically, *Meaney* discloses that recalibration is performed using a "fast initialization" process that can occur with minor disruption to the computer system by skipping certain steps (e.g., a data deskew and a clock centering step) that are performed during the original initialization process. Ex. 1004, [0008], [0013], [0038], Fig. 3.

Because the recalibration of *Meaney* is faster than the initial calibration, it occupies the data channel for less time. Ex. 1002, Appx, 16. Thus, a POSITA would have understood that *Meaney* discloses "second calibration uses less resources of the channel than the first calibration." *Id*.

4. Claim 7

i. 7[a] The method of claim 1, wherein subjecting the receive component to the first calibration comprises receiving a first set of operations at the circuitry to exhaustively determine the initial value of the parameter, and

As discussed above in Section VIII.A.1.ii, *Meaney* discloses subjecting the circuitry of the receive component to the first calibration by calibrating clock delay during initialization of the computer system. *Meaney* explains that the initial calibration is an exhaustive calibration, which involves sending a known data pattern across a data transfer interface to receive circuitry. Ex. 1004, [0004], [0024]-[0033], Fig. 3. This triggers the receiver circuitry to use exhaustive calibration techniques to determine an initial clock delay value that "compensates for the various package tolerances." *Id.* *Meaney* explains that a system assist processor (SAP) controls the calibration sequence and signals the receiver calibration logic to perform calibration. *Id.* at [0038]. Thus, the receiver of *Meaney* receiving the known data pattern and/or receiving signals from the SAP discloses "receiving a first set of operations at the circuitry." *Meaney* explains that this calibration technique

requires stopping the system and involves two separate clock calibrations and deskewing the data. *Id.* Accordingly, a POSITA would have understood that *Meaney* discloses "subjecting the receive component to the first calibration comprises receiving a first set of operations at the circuitry to exhaustively determine the initial value of the parameter." Ex. 1002, Appx, 17-19.

ii. 7[b] wherein periodically subjecting the receive component to the second calibration comprises receiving a second set of operations at the circuitry to update the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value.

As discussed above with respect to 1[d], *Meaney* discloses subjecting the receive component to a second calibration (*Meaney's* recalibration) to update an existing value of the parameter (clock delay) for drift. *Meaney* further discloses the receive component circuitry receiving a set of operations to perform the recalibration if a desired clock delay value has drifted from the existing value by more than a delta value. Ex. 1004, Abstract, [0001], [0005]. As explained above in 7[a], *Meaney* discloses a system assist processor (SAP) controlling the recalibration sequence and signaling the receiver calibration logic to perform recalibration. *Id.* at [0038]. Thus, the receiver receiving the known data pattern and/or receiving signals from the SAP discloses " receiving a second set of operations at the circuitry to update the existing value."

Meaney discloses that recalibration may be performed in response to a trigger event that suggests that the clock delay has drifted and the data capture time window has changed and is no longer accurate. Ex. 1004, [0017]. *Meaney* explains that this trigger event can be indicated when, for example, error correction (ECC) is performed on the data and a correctable error is found. *Id.* Errors in data caused by clock delay drift would indicate that the clock delay has drifted by more than a delta value, i.e., by more than the amount that the system could tolerate without introducing errors into the data. Ex. 1002, Appx, 20-21. Accordingly, a POSITA would have understood that *Meaney*, in view of the knowledge of a POSITA, renders obvious "wherein periodically subjecting the receive component to the second calibration comprises receiving a second set of operations at the circuitry to update the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value." *Id.*

To the extent Patent Owner argues that *Meaney* does not disclose recalibrating "a desired value of the parameter has drifted from the existing value by more than a delta value," it would have been obvious to a POSITA to modify *Meaney* to include this feature. *Id. Meaney* emphasizes the need to recalibrate clock delay to maintain accurate data capture despite drift to circuitry changes or changes in environmental conditions, and discloses recalibrating in response to a trigger event. Ex. 1004, Abstract, [0004]-[0005]. It would have been obvious to a POSITA to

trigger recalibration in response to clock delay, or other parameters indicative of clock delay, drifting from an existing value by an amount beyond the tolerance of the computer system (the claimed "delta value"). Ex. 1002, Appx, 20-21.

5. Claim 8

i. The method of claim 1, wherein periodically subjecting the receive component to the second calibration comprises suspending transmit and receive operations of the circuitry of the receive component.

As discussed above with respect to 1[c], *Meaney* discloses periodically recalibrating the receiver. *Meaney* further discloses that the first step of the recalibration process is putting the computer system or data transfer interface into a "wait state" to keep it from being used for anything other than recalibration. Ex. 1004, [0009]-[0015], [0041]-[0042], Fig. 3, claim 7. Additionally, *Meaney* discloses setting interface fences to block the interface from being used by any system operations other than recalibration. *Id.*, Abstract, [0037], [0044]. In this way, the system of *Meaney* suspends transit and receive operations of the receiver circuitry as part of the recalibration process. Ex. 1002, Appx, 22-24. Accordingly, *Meaney* discloses "wherein periodically subjecting the receive component to the second calibration comprises suspending transmit and receive operations of the circuitry of the receive component." *Id.*

6. Claim 9

i. 9[a] The method of claim 8, wherein subjecting the receive component to the first calibration comprises

receiving at the circuitry a first pattern transmitted by a transmit component and comparing, in the receive component, the first pattern with a first expected pattern, and

As discussed above with respect to 1[c], *Meaney* discloses an first calibration of the system clock during initialization to determine a clock delay. *Meaney* further discloses performing the initial calibration by sending a "known data pattern" across the interface to the receiver circuitry, which is used to calibrate the clock using calibration techniques. Ex. 1004, [0004], [0027]-[0031], Fig. 2. A POSITA would have understood that this discloses performing calibration by comparing, in the receive component, the received data pattern with the known data pattern to determine if they match, and if not, adjusting the clock delay. Ex. 1002, Appx, 25-26.

ii. 9[b] wherein periodically subjecting the receive component to the second calibration comprises receiving at the circuitry a second pattern transmitted by the transmit component and comparing in the receive component the second pattern with a second expected pattern.

As discussed above with respect to 1[c], *Meaney* discloses periodically recalibrating the receiver. As discussed above with respect to 9[a], *Meaney* discloses initially calibrating a clock by transmitting a known data pattern and comparing the data pattern received by the receiver component with the known data pattern. Ex. 1004, [0004], [0027]-[0031], Fig. 3; Ex. 1002, Appx, 27-28. *Meaney*

further discloses that the same "known data pattern" techniques are used for recalibration (the claimed "second calibration"). Ex. 1004, [0037]-[0038], [0042]-[0048]. *Meaney* explains that recalibration includes turning on a known "driver calibration pattern" (e.g., a repeating bit pattern), which is used to re-calibrate the clock. *Id.*; Ex. 1002, Appx, 27-28. A POSITA would have understood that the re-calibration would be performed by comparing, in the receiver and receiver calibration logic, the received data pattern with the known data pattern to determine if they match, and if not, to re-calibrate the clock. Ex. 1002, Appx, 27-28.

7. Claim 10

i. 10[pre] A system, comprising:

To the extent the preamble is limiting, *Meaney* discloses "[a]n SMP computer system has an apparatus and method for recalibrating a self-timed, source-synchronous, pipelined interface while the computer system is running." Ex. 1004, Abstract, [0001]; Ex. 1002, Appx, 28.

ii. 10[a] a receive component, the receive component having circuitry to receive data communicated across a channel by a transmit component;

As discussed above regarding claim 1[pre], *Meaney* discloses computer systems that include a receive component having circuitry to receive data. Ex. 1004, [0003]-[0004], [0007], [0015]-[0016], [0020]-[0021], [0023]. *Meaney* further discloses data communicated across a channel by a transmit component. Ex. 1002, Appx, 29-33. Specifically, the computer systems of *Meaney* include the

transfer of data across a source-synchronous pipelined interface, which a POSITA would have understood is a data channel. Ex. 1004, [0003]; Ex. 1002, Appx, 29-33. *Meaney* explains that data is communicated "across the interface." Ex. 1004, [0004]. Accordingly, a POSITA would have understood *Meaney* to disclose "a transmit component." Ex. 1002, Appx, 29-33.

iii. 10[b] the receive component to perform at system initialization a first calibration, the first calibration to identify an initial value for a parameter affecting proper reception by the circuitry of the data communicated across the channel, and

As discussed above regarding 1[a] and 1[b], *Meaney* discloses subjecting the receive component to a first calibration during initialization to identify an initial value for a parameter affecting proper reception by the circuitry of the receive component of data communicated across a channel as part of the digital signal. *Supra* Sections VIII.A.1.ii & iii. For the same reasons, *Meaney* discloses "the receive component to perform at system initialization a first calibration, the first calibration to identify an initial value for a parameter affecting proper reception by the circuitry of the data communicated across the channel." Ex. 1002, Appx, 34-35.

iv. 10[c] perform on a periodic basis a second calibration, the second calibration to update an existing value of the parameter for drift attributable to change in at least one of voltage or temperature,

As discussed above regarding 1[c], *Meaney* discloses periodically subjecting the receive component to a second calibration to update an existing value of the

parameter for drift attributable to change in at least one of operating voltage or temperature. *Supra* Section VIII.A.1.iv. For the same reasons, *Meaney*, in view of the knowledge of a POSITA, renders obvious "perform on a periodic basis a second calibration, the second calibration to update an existing value of the parameter for drift attributable to change in at least one of voltage or temperature." Ex. 1002, Appx, 36.

v. 10[d] wherein a time duration of the second calibration is constrained to be shorter than a time duration of the first calibration; and

As discussed above regarding 1[e], *Meaney* discloses wherein the second calibration is constrained to occur during a time period that is shorter than a time period of the first calibration. *Supra* Section VIII.A.1.vi. For the same reasons, *Meaney*, in view of the knowledge of a POSITA, renders obvious "wherein a time duration of the second calibration is constrained to be shorter than a time duration of the first calibration." Ex. 1002, Appx, 37.

vi. 10[e] circuitry to store the existing value of the parameter,

Meaney discloses that the computer system includes clock calibrating hardware. Ex. 1004, [0015]-[0016], [0020]-[0021], [0023]. *Meaney* further discloses a system assist processor (SAP) that uses a hardware interface protocol to read and write registers in the logic of the interface. Ex. 1004, [0037]. A POSITA would have understood that the clock calibrating hardware would include circuitry

and would at least temporarily store the existing value of the clock delay in order to perform the recalibration. Ex. 1002, Appx, 38. Additionally, a POSITA would have understood that the SAP would write the clock delay into a register in the interface logic. *Id.* Accordingly, *Meaney*, in view of the knowledge of a POSITA, renders obvious "circuitry to store the existing value of the parameter." *Id.*

Additionally, to the extent Patent Owner argues that *Meaney* does not disclose circuity to store the existing clock delay parameter, it would have been obvious to a POSITA to modify *Meaney* to do so. Ex. 1002, Appx, 38. *Meaney* has clock calibration hardware and discloses performing periodic recalibration of clock delay in a manner that depends on the existing clock delay. *Id.*; Ex. 1004, [0033], [0040], [0051]. A POSITA would have been motivated to store the existing clock delay locally in the computer system so that the existing clock delay would be readily accessible in performing the next clock recalibration. Ex. 1002, Appx, 38.

vii. 10[f] the existing value of the parameter dependent on the initial value and any updates from the second calibration.

As discussed above regarding 1[d], *Meaney* discloses the existing value of clock delay is dependent on the initial clock delay value. *Supra* Section VIII.A.1.v. For the same reasons, *Meaney*, in view of the knowledge of a POSITA, renders obvious "the existing value of the parameter dependent on the initial value." Ex.

1002, Appx, 39. And, as discussed above in 1[c], *Meaney* discloses updating the clock delay based on the recalibration.

8. Claim 11

i. The system of claim 10, wherein the second calibration is to be performed at expiration of an interval of time, at which time the circuitry is to suspend receive operations.

For the same reasons discussed above for claim 2, *Meaney*, in view of the knowledge of a POSITA, renders obvious "the second calibration is to be performed at expiration of an interval of time." *Supra* Section VIII.A.2; Ex. 1002, Appx, 41-43.

And for the same reasons discussed above for claim 8, *Meaney*, in view of the knowledge of a POSITA, renders obvious performing the second calibration at expiration of an interval of time, "at which time the circuitry is to suspend receive operations." *Supra* Section VIII.A.5.

9. Claim 12

i. The system of claim 11, wherein passage of the interval of time is to be tracked by the transmit component and the second calibration is to be initiated by the transmit component.

As discussed above for 10[a], *Meaney* discloses a transmit component. *Supra* Section VIII.A.7.ii. *Meaney* discloses performing recalibration in "periodic intervals" and states that the recalibration method can be "triggered periodically." Ex. 1004, [0008], *Meaney* further discloses that the passage of the interval of time is

tracked by the transmit component and the recalibration is initiated by the transmit component periodically. Specifically, the recalibration of *Meaney* is initiated by a driver side calibration flag signaling hardware to drive a repeating pattern across the interface to the receiver. Ex. 1004, [0037]. Accordingly, a POSITA would have understood that *Meaney* discloses the hardware of the transmit component tracking the periodic intervals and the second calibration being initiated by the transmit component. Ex. 1002, Appx, 44.

Additionally, to the extent Patent Owner argues that *Meaney* does not disclose the transmit component tracking the passage of the interval of time, it would have been obvious to a POSITA to modify *Meaney* to do so. *Id*. *Meaney* discloses that periodic recalibration allows the system to ensure that changes to the circuitry or environmental characteristics do not adversely affect performance over time, and discloses that the transmit component (the driver side hardware) initiates the recalibration. Ex. 1004, [0016], [0037]. A POSITA would have been motivated to have the transmit component track the periodic time intervals so it could initiate the recalibration directly without needing further instructions or signals (e.g., from the receiving component or other hardware). Ex. 1002, Appx, 44.

10. Claim 15

i. The system of claim 10, wherein the receive component is to perform, responsive to the second calibration, one of an increment operation or a decrement operation upon the existing value if a desired value of the

parameter has drifted from the existing value by more than a delta value.

As discussed above with respect to 1[d], *Meaney* discloses subjecting the receive component to a second calibration (*Meaney's* recalibration) to update an existing value of the parameter (clock delay) for drift. *Meaney* further discloses that the receive component performs, responsive to the second calibration, one of an increment operation or a decrement operation upon the existing clock delay if a desired value of the clock delay has drifted from the existing clock delay by more than a delta value. Ex. 1002, Appx, 46-47. *Meaney* discloses that recalibration may be performed, by the receiver and receiver calibration logic, in response to a trigger event that suggests that the clock delay has drifted and the data capture time window has changed and is no longer accurate. Ex. 1004, [0017]. *Meaney* explains that this trigger event can be indicated when, for example, error correction (ECC) is performed on the data and a correctable error is found. *Id.* Errors in data caused by clock delay drift would indicate that the clock delay has drifted by more than a delta value, i.e., by more than the amount that the system could tolerate without introducing errors into the data. Ex. 1002, Appx, 46-47. In response, *Meaney* discloses that the clock delay may be adjusted by a "delay shift" (i.e., an increment or decrement operation) calculated based on a recalibration and then applied to the existing clock delay value. Ex. 1004, [0051]; Ex. 1002, Appx, 46-47. Accordingly, a POSITA would have understood that *Meaney*, in view of the knowledge of a

POSITA, renders obvious "the receive component is to perform, responsive to the second calibration, one of an increment operation or a decrement operation upon the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value." Ex. 1002, Appx, 46-49.

To the extent Patent Owner argues that *Meaney* does not disclose "perform[ing], responsive to the second calibration, one of an increment operation or a decrement operation upon the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value," this would have been obvious to a POSITA. Ex. 1002, Appx, 47. *Meaney* emphasizes the need to recalibrate clock delay to maintain accurate data capture despite drift to circuitry changes or changes in environmental conditions, and discloses recalibrating in response to a trigger event. Ex. 1004, Abstract, [0004]-[0005]. *Meaney* also discloses changing the clock delay by performing a recalibration and then applying a "delay shift" to the existing clock delay based on the results of the recalibration. *Id.* at [0051]. It would have been obvious to a POSITA, in response to a recalibration, to perform an increment operation or a decrement operation on the existing clock delay value, to shift the value of the clock delay based on the results of the recalibration (e.g., based on the amount the received data pattern differs from the known data pattern). Ex. 1002, Appx, 46-49; Ex. 1004, [0004], [0037]-[0038], [0042]-[0048]. For example, a POSITA would be motivated to do so at least in view of *Meaney*

disclosure of recalibrating clock delay to account for drift due to changes in circuitry or environmental conditions, as well as *Meaney's* use of a "delay shift" to change the clock delay. Ex. 1002, Appx, 46-49.

11. Claim 16

i. 16[a] The system of claim 10, further comprising circuitry to store a first expected pattern and a second expected pattern, and

As discussed above with respect to claim elements 9[a] and 9[b], *Meaney* discloses that both the initial calibration and the recalibration may be performed by comparing, in the receive circuitry, the received data pattern with the known data pattern to determine if they match, and if not, adjusting the clock delay. *Supra* Section VIII.A.6. In order to carry out that comparison, the receiver circuity must, at least temporarily, store the respective known data patterns needed for each calibration or recalibration, and thus those data patterns must be stored in circuitry of the computer system. Ex. 1002, Appx, 49-51. Additionally, because claim 16[a] does not specify where the circuitry must be, storage of those known data patterns anywhere in the circuitry of *Meaney's* computer system is sufficient to meet this element. *Id.*

ii. 16[b] circuitry to compare the first expected pattern with a pattern received from the transmit component in association with the first calibration, and to compare the second expected pattern with a pattern received from the transmit component in association with the second calibration.

As discussed above with respect to claim elements 9[a] and 9[b], *Meaney* discloses that both the initial calibration and the recalibration may be performed by comparing, in the receive circuitry, the received data pattern with the known data pattern to determine if they match, and if not, adjusting the clock delay. *Supra* Section VIII.A.6. For the same reasons, *Meaney*, in view of the knowledge of a POSITA, renders obvious "circuitry to compare the first expected pattern with a pattern received from the transmit component in association with the first calibration, and to compare the second expected pattern with a pattern received from the transmit component in association with the second calibration." Ex. 1002, Appx, 52-53.

B. *Ground 2: Claims 1, 2, 6-12, 15, and 16 are obvious over Meaney and Nguyen in view of the knowledge of a POSITA*

The combination of *Meaney* and *Nguyen*, either alone or in combination, discloses and/or suggests all limitations of claims 1, 2, 6-12, 15, and 16, and thus renders those claims obvious. Ex. 1002, Appx, 54-81. Specifically, *Meaney* in combination with *Nguyen* discloses applying offsets to existing values to determine a calibrated value, and circuitry for receiving a digital signal, calibrating computer system parameters, and storing calibration data. *See, e.g.,* Ex. 1002, Appx, 54, 61-63, 75-77. All other elements of claims 1, 2, 6-12, 15, and 16 are disclosed or rendered obvious by *Meaney* as explained in Ground 1.

1. One of skill in the art would have been motivated to combine *Meaney* with *Nguyen*

Meaney discloses a system for calibrating communication system parameters. Ex. 1004, Abstract, [0008]-[0017], [0039]-[0040]. Similarly, *Nguyen* discloses techniques for applying offsets to existing values to determine calibrated values for a digital system, as well as specific circuitry for signal reception and parameter calibration. Ex. 1005, [0065], [0083-0085], [0099]. Accordingly, *Meaney* and *Nguyen* both relate to electronic systems and methods for calibration and adjustment of communication system parameters. Ex. 1002, Appx, 54.

Nguyen discloses applying offsets to existing values to derive calibrated values to ensure precise adjustments in system parameters. Ex. 1005, [0099]; Ex. 1002, Appx, 54. Combining this method with the system of *Meaney* would enhance the accuracy of *Meaney's* calibration process, improving overall system performance. Ex. 1002, Appx, 54. Thus, a POSITA would have been motivated to make this combination to enhance calibration accuracy. *Id.*

Due to similarities between the calibration techniques of *Meaney* and *Nguyen*, a POSITA would have had a reasonable expectation of success in making this modification. *Id*. For example, *Meaney* describes a concept similar to *Nguyen's* offsets: "adding delay" to the parameters or applying a shift to the existing parameters. Ex. 1004, [0040], [0051]; Ex. 1002, Appx, 54. Alternatively, a POSITA would have understood that the calibration systems of *Meaney* would be

enhanced with the offsets of *Nguyen* because this improvement represents the use of a known technique to predictably improve a similar system in the same way. Ex. 1002, Appx, 54; *see KSR Int'l Co. v. Teleflex, Inc.,* 127 S.Ct. 1727, 1740 (2007).

A POSITA would have also been motivated to integrate the circuitry of *Nguyen* into the system of *Meaney* to improve efficiency of the calibration. Ex. 1002, Appx, 54. *Nguyen* discloses a streamlined approach to system calibration with particular circuitry. Ex. 1005, [0065], [0083-0085], [0099]; Ex. 1002, Appx, 54. Because *Meaney* does not specify the particular circuitry that is employed, incorporating the circuitry of *Nguyen* into the system of *Meaney* would have been choosing from a finite number of identified, predictable solutions, and a simple substitution of one known element for another to yield predictable results. *Id.*, Appx, 54; *see KSR Int'l,* 127 S.Ct. at 1740 (2007).

A POSITA would have had a reasonable expectation of success in combining *Meaney* and *Nguyen*. Ex. 1002, Appx, 54. Both address common challenges in the field of electronic system calibration and optimization. Ex. 1004, Abstract, [0008]-[0017], [0039]-[0040]; Ex. 1005, [0065], [0083-0085], [0099]; Ex. 1002, Appx, 54. The integration of *Nguyen's* calibration techniques and circuitry into *Meaney's* system would have been straightforward and cost-effective. Ex. 1002, Appx, 54. The required modifications would have been minimal, and the results of the combination

would have been predictable, given the complementary nature of the technologies. Ex. 1005, 7:10-25; Ex. 1002, Appx, 54.

2. Claim 1

i. 1[pre] "a receive component having circuitry to receive a digital signal"

As discussed in Ground 1, *Meaney* discloses a method of operation in a system that includes a receive component having a receiver and a receiver calibration logic for capturing a digital signal. Ex. 1004, [0003]-[0004], [0023]; *supra* Section VIII.A.1.i. *Nguyen* also discloses a receive component having circuitry to receive a digital signal. Ex. 1002, Appx, 55-60. For example, *Nguyen* discloses a receiving unit 115 that receives a signal 110 from the transmitting unit 110. Ex. 1005, [0030] Fig. 1 (annotated below).

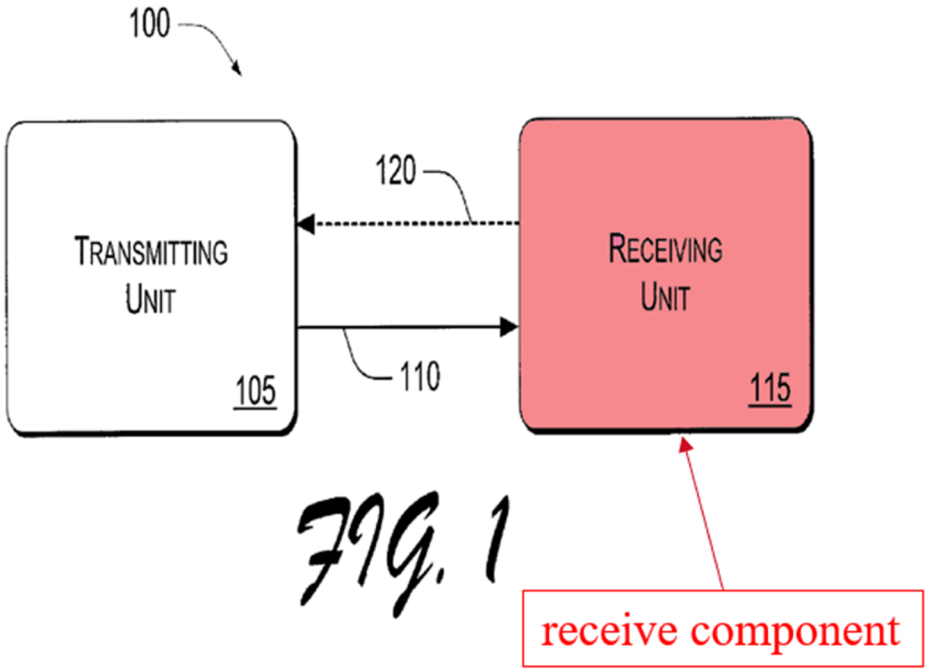


FIG. 1

Nguyen discloses, for example, that the receiving unit may be part of an integrated circuit or printed circuit board, and discloses that the transmitted signal 110 may be a digital signal. Ex. 1005, [0031], [0032], [0047]; Ex. 1002, Appx, 56. *Nguyen* also gives examples of specific circuitry that could be implemented in the receiving unit. Ex. 1005, Fig. 4A (annotated):

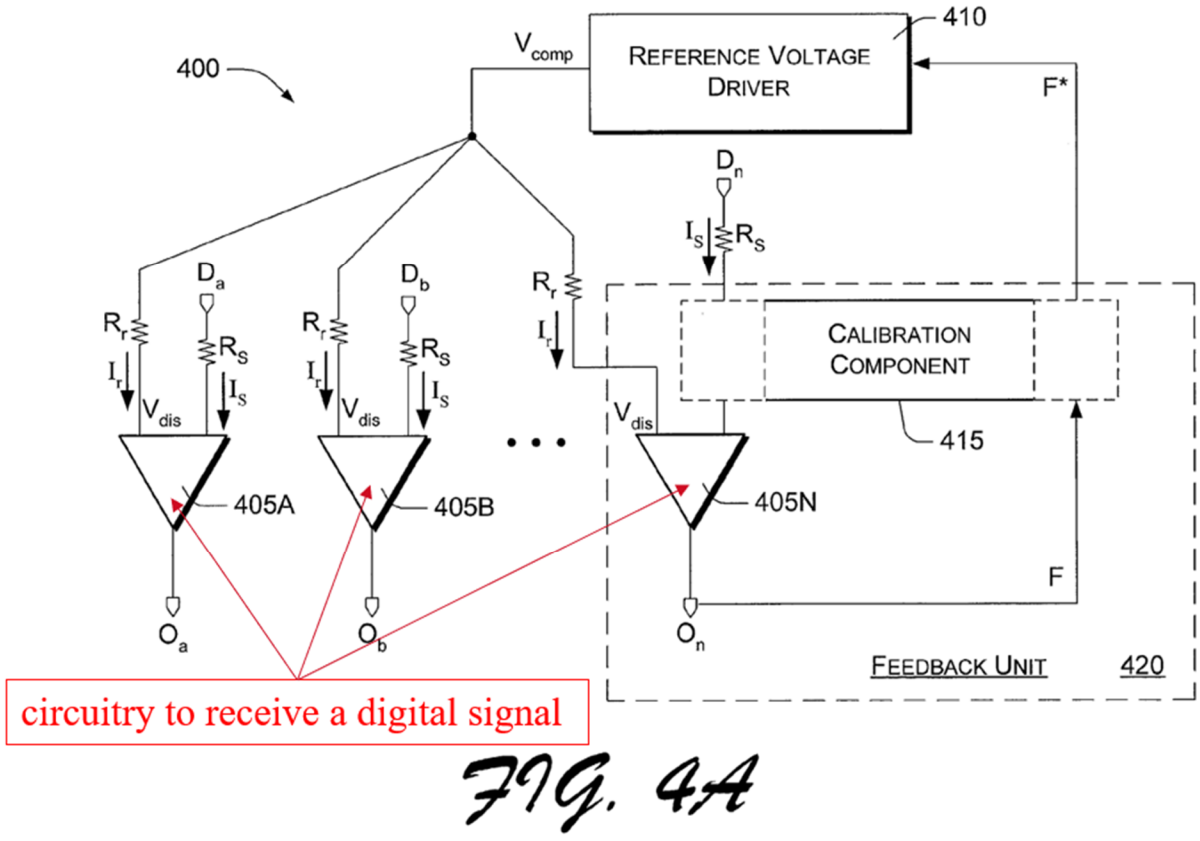


FIG. 4A

As discussed in Section VIII.B.1, it would have been obvious to a POSITA to enhance the computer system interface of *Meaney* with the receiver circuitry and digital signals of *Nguyen*. Ex. 1002, Appx, 56. Because *Meaney* does not specify the particular receiver circuitry that is employed in receiving the transmitted data, it would have been obvious to a POSITA to modify *Meaney* to include the digital

signal receiving unit of *Nguyen* to receive the digital signal of *Meaney*. Ex. 1002, Appx, 56-57.

ii. 1[d] wherein the existing value is dependent on the initial value

As discussed in Ground 1, *Meaney* discloses that an existing value for clock delay is dependent on an initial clock delay determined during initialization, either directly or indirectly. Ex. 1004, [0008], [0016], [0040]; *supra* Section VIII.A.1.v. *Nguyen* discloses adjusting a parameter of a digital signal receiver (compensated voltage) by applying an offset to a previously calibrated value. Ex. 1002, Appx, 61-63; Ex. 1005, [0099] ("This calibrated value may be read from the register 710 and an offset value may be added. The resultant summed value may then be programmed back into the register 710 and used during normal operation of the device"). Specifically, *Nguyen* discloses determining a calibrated value, then adding or subtracting an offset value. Ex. 1002, Appx, 61-63; Ex. 1005, [0099]. The offset value may be determined at design time or determined dynamically as part of an initialization or calibration procedure. Ex. 1002, Appx, 61-63; Ex. 1005, [0099].

As discussed in Section VIII.B.1, it would have been obvious to a POSITA to enhance the calibration techniques of *Meaney* with the offset values of *Nguyen*. Ex. 1002, Appx, 54. *Meaney* discloses recalibration techniques that include applying a delay shift to the existing clock delay. Ex. 1004, [0040], [0051]. A

POSITA would have understood this as a similar concept to the offsets of *Nguyen*. Ex. 1002, Appx, 61-62. In light of these similar disclosures, it would have been obvious to a POSITA to apply the offset values of *Nguyen* to the clock delay calibration of *Meaney.* Ex. 1002, Appx, 62. For example, a POSITA could implement a predetermined offset to the clock delay of *Meaney* to compensate for an environmental difference (e.g., temperature) between the calibration environment and operational environment of the computer system interface. *Id*.

3. Claims 2, 6, 8, 9, 11, and 12

As discussed above in Ground 1, each and every element of claims 2, 6, 8, 9, 11, and 12 are taught by *Meaney*. *Supra* Sections VIII.A.2-3, 5-6, & 8-9. The combination of *Meaney* and *Nguyen*, as described above, does not affect the disclosure of *Meaney* that render those claims obvious. Accordingly, the combination of *Meaney* and *Nguyen* render claims 2, 6, 8, 9, 11, and 12 obvious for the same reasons as discussed in Ground 1.

4. Claim 7

i. 7[a] The method of claim 1, wherein subjecting the receive component to the first calibration comprises receiving a first set of operations at the circuitry to exhaustively determine the initial value of the parameter, and

As discussed in Ground 1, *Meaney* discloses subjecting the circuitry of the receive component to a first calibration by calibrating clock delay during initialization of the computer system, which is triggered by sending a known data

pattern across a data transfer interface, to exhaustively determine the initial value of clock delay. *Supra* Section VIII.A.4.i. To the extent Patent Owner argues that *Meaney* does not disclose this element, *Nguyen* discloses the first calibration comprises receiving a first set of operations at the circuitry to exhaustively determine the initial value of the parameter. Ex. 1002, Appx, 65-70; Ex. 1005, [0071]-[0074], [0110], Fig. 4B.

As shown in Fig. 4B, reproduced below, *Nguyen* discloses steps taken during an initialization or calibration phase, including repeating many of the steps of the initialization or calibration process until the voltage parameter reaches a satisfactory level. Ex. 1005, [0071]-[0074], Fig. 4B (annotated):

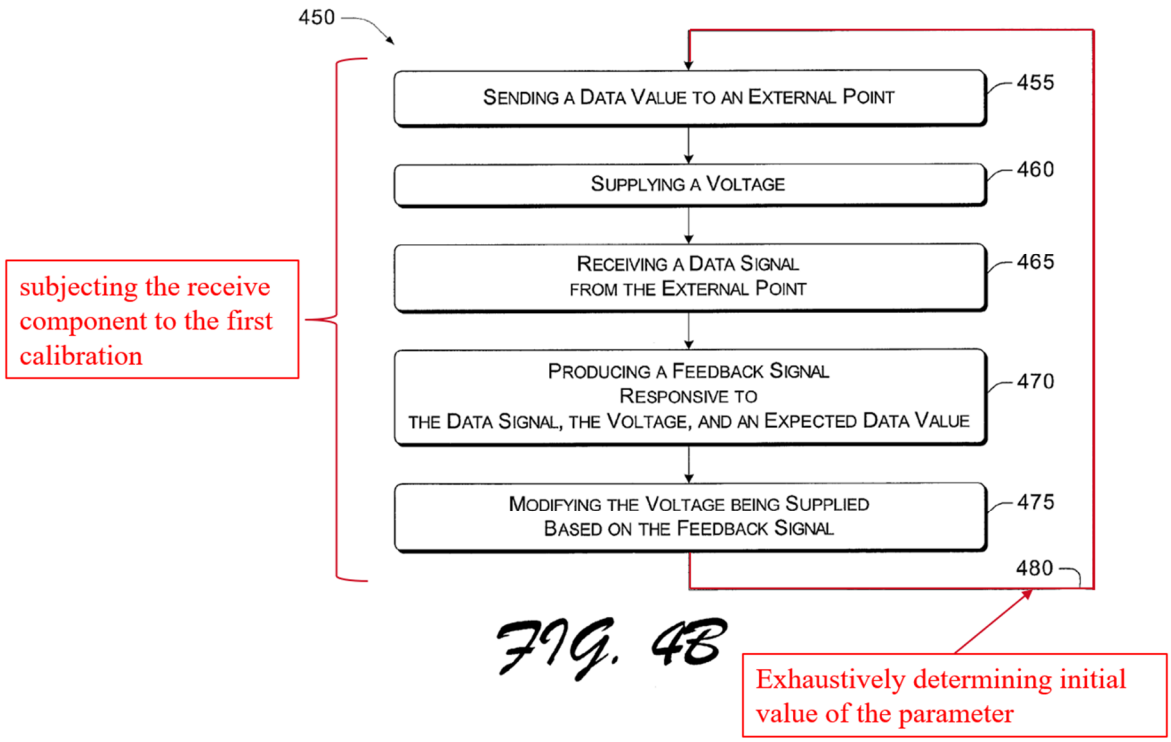


FIG. 4B

Similarly, as shown in Fig. 9B, reproduced below, *Nguyen* discloses steps taken during an initialization or calibration phase, including repeating many of the steps of the initialization or calibration process until the compensated voltage reaches a satisfactory level. Ex. 1005, [0107-0110], Fig. 9B (annotated):

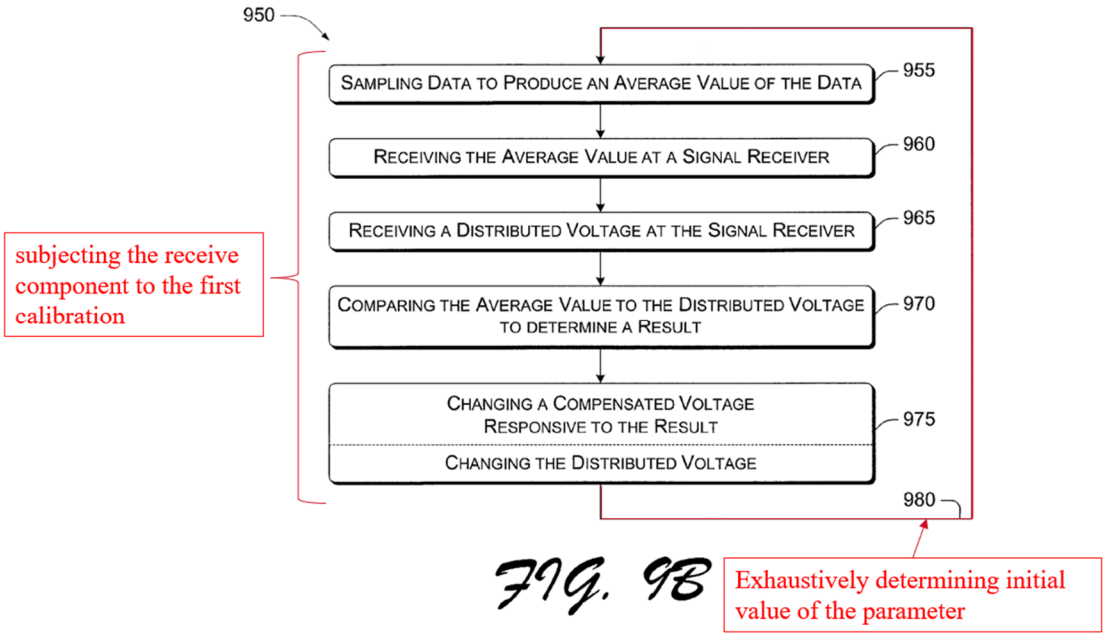


FIG. 9B

A POSITA would have understood this disclosure of *Nguyen* to disclose "exhaustively determining the initial value" of the calibrated parameter. Ex. 1002, Appx, 65-70.

As discussed in Section VIII.B.1, it would have been obvious to a POSITA to enhance the calibration techniques of *Meaney* with the exhaustive calibration techniques of *Nguyen*. Ex. 1002, Appx, 54. *Meaney* discloses initialization calibration techniques that involve repeating the clock calibration step twice. Ex. 1004, [0004], [0024]-[0033], Fig. 3. In combination with *Nguyen*, a POSITA

would have been motivated to repeat the clock calibration step of *Meaney*, as well as other initialization steps, until the clock delay recaches a satisfactory value. Ex. 1002, Appx, 65-70. For example, a POSITA would have been motivated to perform these steps periodically not just during initialization but periodically to account for shifts in temperature or power supply voltage. *Id.* at Appx, 67.

ii. 7[b] wherein periodically subjecting the receive component to the second calibration comprises receiving a second set of operations at the circuitry to update the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value.

As discussed in Ground 1, *Meaney* discloses receiving a second set of operations at the circuitry to update the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value. *Supra* Section VIII.A.4.ii. To the extent Patent Owner argues that *Meaney* does not disclose this limitation, *Nguyen* also discloses that calibration may be repeated to correct for drifts in the calibrated parameter, or in response to "a predetermined number of detected (e.g., bit or byte) errors." Ex. 1002, Appx, 71-72; Ex. 1005, [0094], [0147]. A POSITA would have understood a predetermined number of detected errors to represent a delta value (e.g., the delta between no errors and a certain number of errors) that represents a parameter drift. Ex. 1002, Appx, 71-72. Accordingly, a POSITA would have understood that *Nguyen* discloses recalibration

"if a desired value of the parameter has drifted from the existing value by more than a delta value." *Id*.

As discussed in Section VIII.B.1, it would have been obvious to a POSITA to enhance the recalibration triggers of *Meaney* with the predetermined number of errors of *Nguyen*. Ex. 1002, Appx, 54. *Meaney* also discloses triggering recalibration when correctable errors are found in the data. Ex. 1004, [0017]. Accordingly, it would have been obvious for a POSITA to modify *Meaney*'s error-triggered recalibrations to include the "predetermined number of detected errors" of *Nguyen* to allow the system of *Meaney* to react to a desired level of error tolerance for example, account for errors due to changes in voltage and temperature. Ex. 1002, Appx, 71-72.

5. Claim 10

As discussed in Ground 1, elements 10[pre], 10[b], 10[c], and 10[d] are taught by *Meaney. Supra* Sections VIII.A.7.i, iii-v.

i. 10[a] a receive component, the receive component having circuitry to receive data communicated across a channel by a transmit component;

As discussed in Ground 1, *Meaney* discloses a receive component having circuitry to receive data communicated across a channel by a transmit component. *Supra* Section VIII.A.7.ii. As discussed above in 1[pre], the combination of *Meaney* and *Nguyen*, in view of the knowledge of a POSITA, renders obvious "the receive

component having circuitry to receive data." *Supra* Section VIII.B.2.i; Ex. 1002, Appx, 73-74.

ii. 10[e] circuitry to store the existing value of the parameter,

As discussed in Ground 1, *Meaney* discloses that the computer system includes clock calibrating hardware including an SAP that uses a hardware interface protocol to read and write registers in the logic of the interface. Ex. 1004, [0015]-[0016], [0020]-[0021], [0023]. To the extent Patent Owner argues that *Meaney* does not disclose this limitation, *Nguyen* also discloses "circuitry to store the existing value of the parameter." Ex. 1002, Appx, 75-76. For example, *Nguyen* discloses the use of a "parameters table" and a parameters table bus during initialization/calibration to store calibrated parameter values. Ex. 1005, [0130-0133]. As discussed in Section VIII.B.1, it would have been obvious to a POSITA to enhance the computer system interface of *Meaney* with the calibration techniques and receiver circuitry of *Nguyen*. Ex. 1002, Appx, 54. Moreover, it would have been obvious for a POSITA to modify *Meaney*'s system to include the parameter table and parameter table bus of *Nguyen* to allow the system of *Meaney* to more easily and reliably store and retrieve clock delay values from calibrations and recalibrations. Ex. 1002, Appx, 75.

iii. 10[f] the existing value of the parameter dependent on the initial value and any updates from the second calibration.

As discussed in Ground 1, *Meaney* discloses "the existing value of the parameter dependent on . . . any updates from the second calibration" by updating clock delay based on a recalibration. *Supra* VIII.A.7.vii. As discussed above in this Ground 2, *Meaney* and *Nguyen*, in view of the knowledge of a POSITA, renders obvious "the existing value of the parameter dependent on the initial value." *Supra* Section VIII.B.2.ii; Ex. 1002, Appx, 77.

6. Claim 15

i. The system of claim 10, wherein the receive component is to perform, responsive to the second calibration, one of an increment operation or a decrement operation upon the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value.

As discussed in Ground 1, *Meaney* teaches recalibration may be performed in response to a trigger event that suggests that the clock delay has drifted and the data capture time window is no longer accurate. *Supra* VIII.A.10. As discussed in this Ground regarding 1[d] and 7[b], the combination of *Meaney* and *Nguyen* teaches applying an increment or decrement operation by adjusting the clock delay through by a predetermined offset in response to drift by more than a delta value (e.g., a predetermined number of detected errors). *Supra* Section VIII.B.2.ii, VIII.B.4.ii.; Ex. 1002, Appx, 78.

7. Claim 16

i. **16[a] The system of claim 10, further comprising circuitry to store a first expected pattern and a second expected pattern, and**

ii. **16[b] circuitry to compare the first expected pattern with a pattern received from the transmit component in association with the first calibration, and to compare the second expected pattern with a pattern received from the transmit component in association with the second calibration.**

As discussed in Ground 1, *Meaney* teaches circuitry to store a first expected pattern and a second expected pattern, as well as comparing first expected patterns and second expected patterns to data patterns received from a transmit component in association with first and second calibrations. *Supra* Section VIII.A.11.

To the extent Patent Owner argues that *Meaney* does not teach these limitations, *Nguyen* discloses first and second expected patterns and circuitry for receiving, storing, and providing the expected data, and circuitry for comparing the same. Ex. 1005, [0112], [0114], Fig. 10A. Specifically, as shown in annotated Fig. 10A below, *Nguyen* discloses a "digital calibration component 510" that has interfaces for "receiving and/or providing calibration data" including a "calibration data register 1005." Ex. 1005, [0112], [0114]. *Nguyen* explains that the calibration data includes "expected value[s] to be received from a transmitting unit" (i.e., "expected pattern[s]") which is compared against received data to determine if they are equal in the comparison unit 1010. *Id.*, [0114].

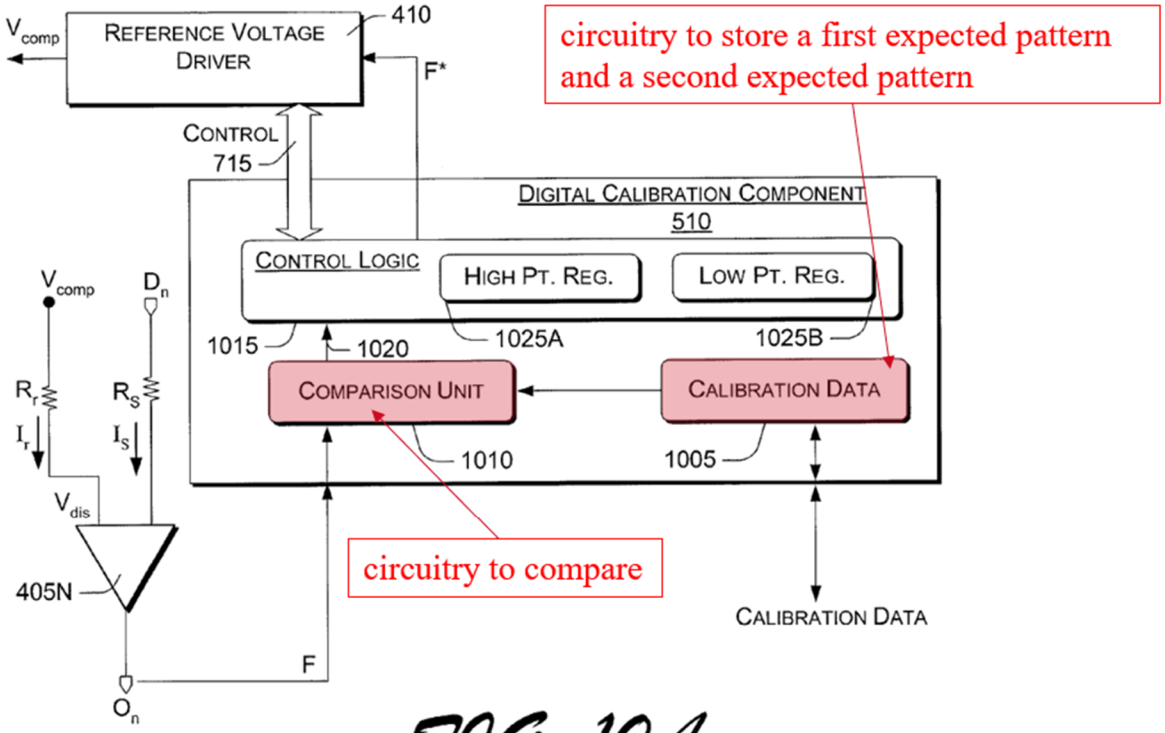


FIG. 10A

As discussed in Section VIII.B.1, it would have been obvious to a POSITA to enhance the computer system interface of *Meaney* with the calibration techniques and the storage and receiver circuitry of *Nguyen*. Ex. 1002, Appx, 79-81. For example, because *Meaney* does not specify the particular receiver circuitry that is employed in comparing the known data pattern with the received data pattern, it would have been obvious to look to *Nguyen* for the type of circuitry suitable for storage of the data pattern. *Id*. A POSITA would have been motivated to do because of the benefit of having local storage of the expected patterns for use during calibrations without needing to request the expected pattern from another location. Ex. 1002, Appx, 80. For example, a POSITA would find it obvious to include the

digital calibration component 510 of *Nguyen* to operate the receiver calibration logic 14 of *Meaney*, as shown below. *Id.*

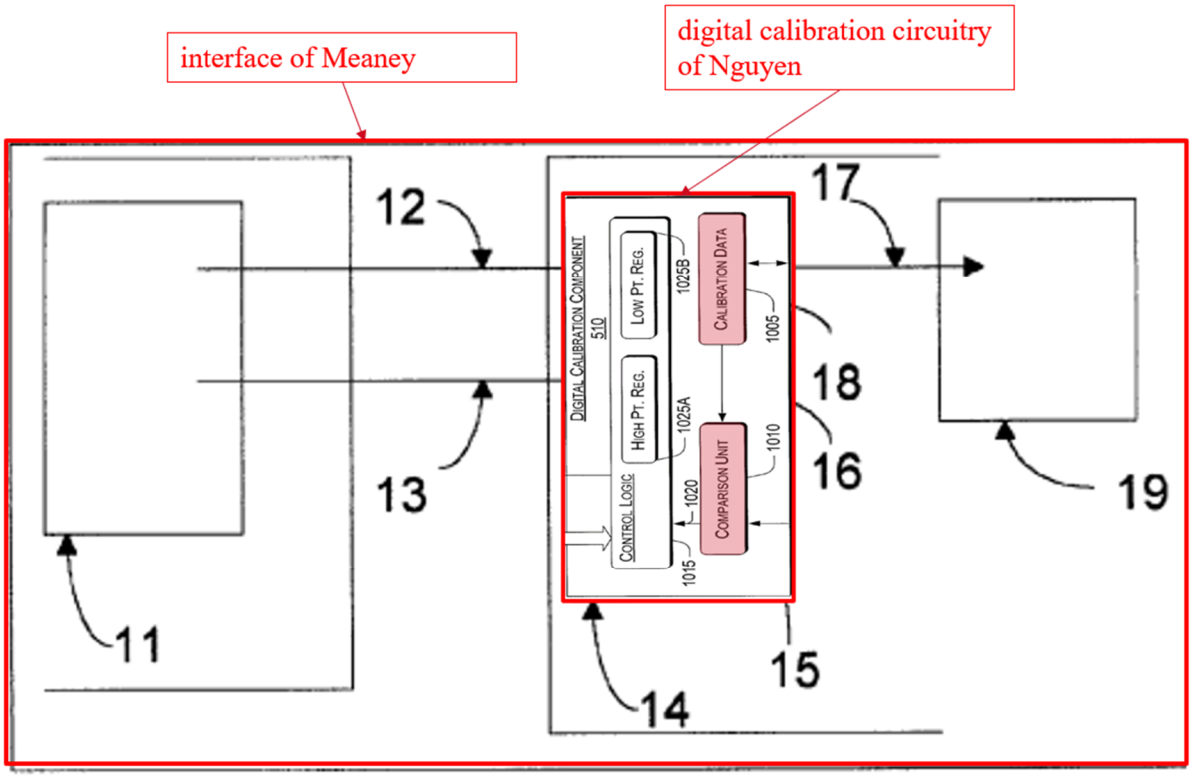


FIGURE 1.

C. *Ground 3: Claims 4, 5, 13, 14, and 17-19 are obvious over Meaney and Greeff in view of the knowledge of a POSITA*

The combination of *Meaney* and *Greeff* teaches and/or suggests all limitations of claims 4, 5, 13, 14, and 17-19, and thus renders those claims obvious. Ex. 1002, Appx, 82-123. Specifically, *Meaney* in combination with *Greeff* discloses or renders obvious "an existing value representative of at least one of a termination resistance and a driver strength" as required by independent claim 17. Ex. 1002,

Appx, 82. All other elements of claims 4, 5, 13, 14, and 17-19 are disclosed or at least rendered obvious by *Meaney* as described above in Ground 1.

1. One of skill in the art would have been motivated to combine *Meaney* and *Greeff*

Meaney and *Greeff* both pertain to electronic systems and methods for calibration and adjustment of system parameters. *Meaney* discloses a system for calibrating a parameter of an electronic system, while *Greeff* discloses termination circuitry that are integral to electronic system performance. Ex. 1004, Abstract, [0008]-[0017], [0039]-[0040]; Ex. 1006, 3:65-4:20, 4:11-20, 5:59-6:6, 7:52-8:56; Ex. 1002, Appx, 82. Both references emphasize the importance of calibrating variables both initially, prior to operation, and during operation. Ex. 1004, [0006], [0008], [0013], [0021], [0024], [0038]; Ex. 1006, 4:11-20, 7:52-8:56; Ex. 1002, Appx, 82.

A POSITA would have been motivated to incorporate the termination circuitry disclosed in *Greeff* with the system of *Meaney* to achieve enhanced system performance and reliability. Ex. 1002, Appx, 82. *Greeff's* termination circuitry ensures proper signal integrity and reduces reflections in high-speed data transmission systems. Ex. 1006, 1:28-31, 4:10-12, 8:3-5; Ex. 1002, Appx, 82. *Meaney's* calibration techniques, when applied to the termination resistance and transistor drive strength of *Greeff*, would ensure that these parameters remain optimal throughout system operation. Ex. 1002, Appx, 82.

Moreover, both *Meaney* and *Greeff* disclose methods for calibrating variables initially and during operation for recalibration. Ex. 1004, [0006], [0008], [0013], [0021], [0024], [0038]; Ex. 1006, 4:11-20, 7:52-8:56; Ex. 1002, Appx, 82. A POSITA would have found it obvious to apply *Meaney's* calibration process to *Greeff's* termination circuitry in order to optimize the termination resistance and drive strength of the termination circuitry. Ex. 1002, Appx, 82. This represents the use of a known technique to predictably improve a similar system in the same way. *KSR Int'l Co. v. Teleflex, Inc*., 127 S.Ct. 1727, 1740 (2007).

A POSITA would have had a reasonable expectation of success in combining *Meaney* and *Greeff*. Ex. 1002, Appx, 82. The integration of *Greeff's* termination circuitry into *Meaney's* system would have been straightforward and cost-effective. *Id.* The required modifications are minimal, and the results of the combination are predictable, given the complementary nature of the technologies. *Id*.

2. Claim 4

i. The method of claim 1, wherein the parameter is a link termination resistance.

As shown below in annotated Fig. 1, *Greeff* discloses a multidrop bus including circuitry capable of receiving a digital signal that includes termination circuitry 120 including a switch 122 connected between a "trimmable" termination resistor 124, having a trimmable termination resistance RTERM, and a reference voltage VTERM. Ex. 1006, 3:65-4:20, 5:59-6:6, 7:52-8:56, Fig. 1; Ex. 1002, Appx,

83. A POSITA would have understood *Greeff*'s termination resistance to be the claimed "link termination resistance." *Id.* *Greeff* explains that the termination resistance is modified during initial calibration and recalibration processes to provide a substantially optimal termination of the bus 102. Ex. 1006, 4:11-20, 7:52-8:56; Ex. 1002, Appx, 83.

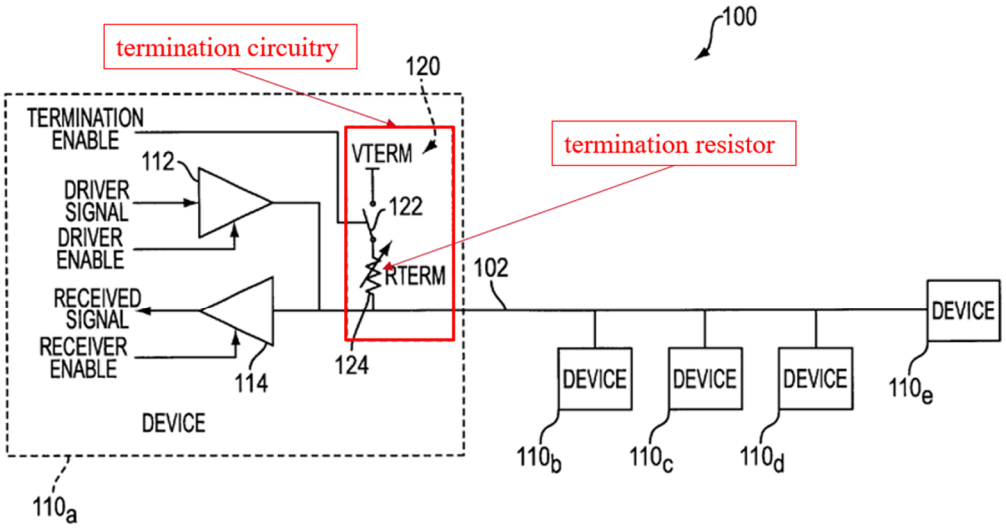


FIG. 1

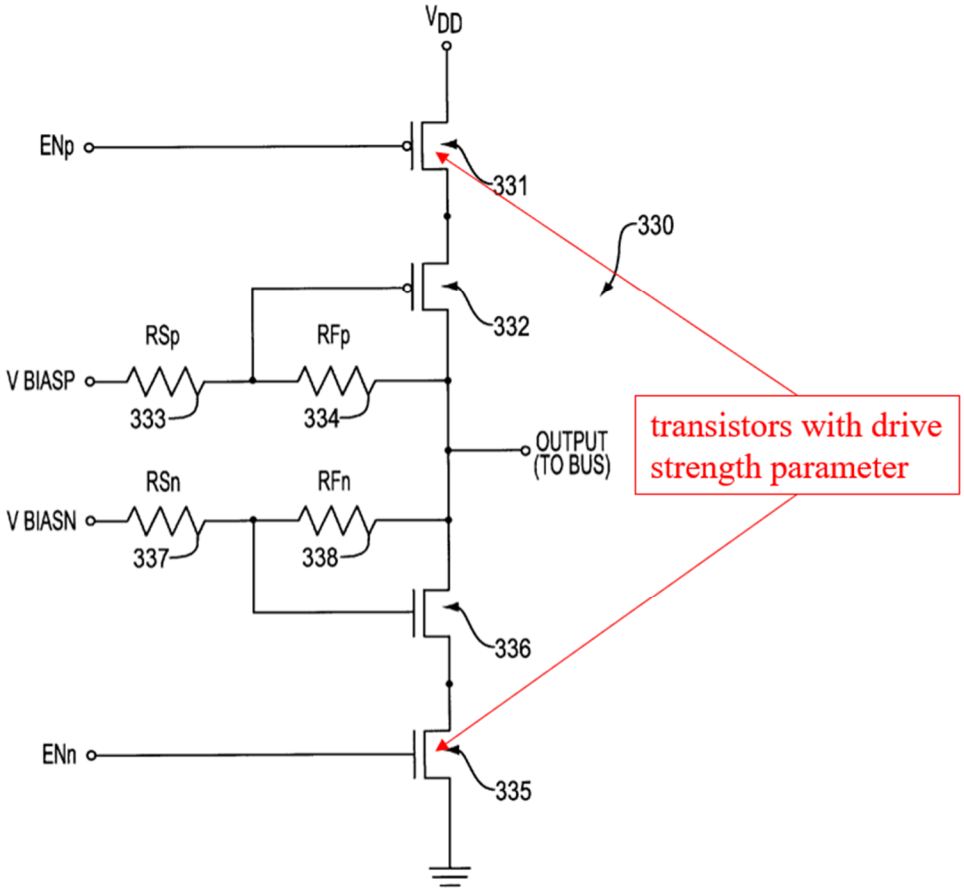
Thus, *Greeff* in combination with *Meaney* discloses claim 4. Ex. 1002, Appx, 83.

3. Claim 5

i. The method of claim 1, wherein the parameter is a driver strength.

As shown below in annotated Fig. 3, *Greeff* discloses an active termination circuit 330 including circuitry capable of receiving a digital signal that uses

transistors 331 and 335 as switches that enable or disable the active termination. Ex. 1006, 6:40-55, Fig. 3; Ex. 1002, Appx, 84-85. *Greeff* explains that the drive strength of the transistors can be calibrated. Ex. 1006, 8:3-5, claim 42; Ex. 1002, Appx, 84-85. A POSITA would have understood *Greeff*'s drive strength to be the claimed "driver strength." Ex. 1002, Appx, 84-85.



Thus, *Greeff* in combination with *Meaney* discloses claim 5. Ex. 1002, Appx, 84-85.

4. Claim 13

i. The system of claim 10, wherein the parameter is a link termination resistance.

Supra Section VIII.C.2.

5. Claim 14

i. The system of claim 10, wherein the parameter is a driver strength for a driver of the receive component.

See Section VIII.C.3.

6. Claim 17

i. 17[pre] A system, comprising:

To the extent the preamble is limiting, *Meaney* discloses a system. *Supra* Section VIII.A.7.i.

ii. 17[a] circuitry to store an existing value representative of at least one of a termination resistance and a driver strength to be applied in association with data communicated across a channel;

As discussed in Ground 1, *Meaney* discloses circuitry to store an existing value of a parameter. *Supra* Section VIII.A.7.vi. *Greeff* discloses that the existing value is representative of at least one of a termination resistance and a driver strength to be applied in association with data communicated across a channel. Ex. 1002, Appx, 86-89. As discussed above regarding claims 4 and 5, *Greeff* discloses calibration of both a termination resistance and a drive strength of transistors for active termination. *Supra* Sections VIII.C.2-3.

iii. 17[b] circuitry to perform a first calibration at system initialization, to identify a first value to be initially applied as the existing value,

As discussed in Ground 1, *Meaney* discloses circuitry to perform a first calibration at system initialization, to identify a first value to be initially applied as the existing value. *Supra* Section VIII.A.7.i-iii.

Greeff discloses calibrating parameters such as termination resistance prior to the first use of the system, which it refers to as "static calibration." Ex. 1006, 4:10-13, 7:52-61. As shown in Fig. 2 (annotated below), *Greeff* discloses active termination circuitry that would be used to calibrate the termination resistance ("RTERM"). Ex. 1006, 4:10-13, 7:52-61, Fig. 2; Ex. 1002, Appx, 89-90.

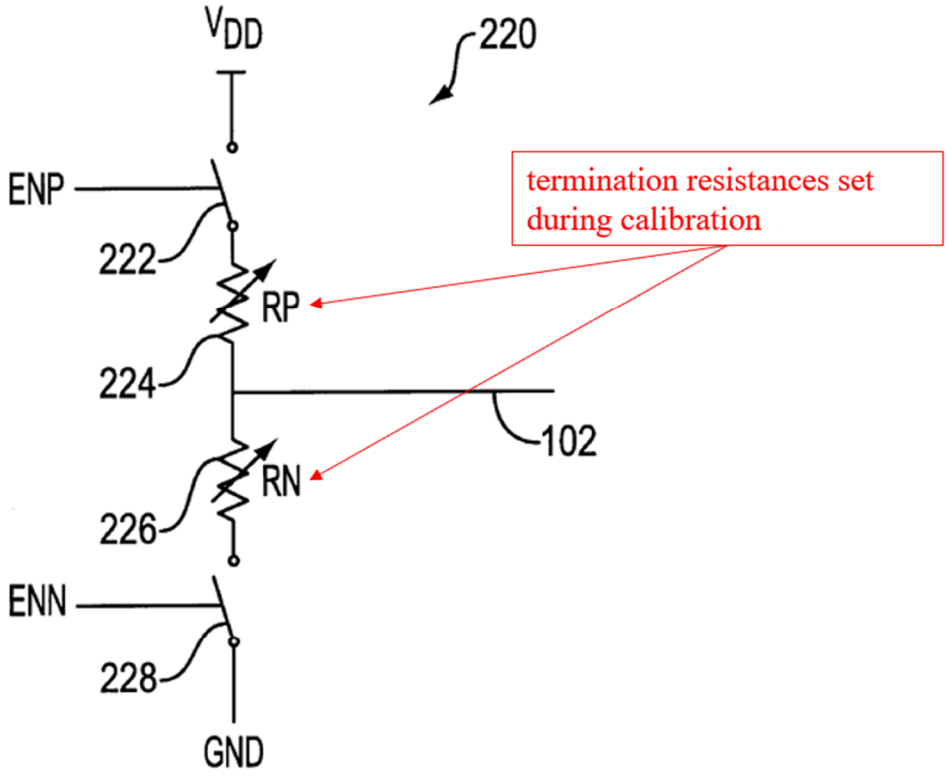


FIG. 2

For example, *Greeff* explains that the "two termination resistances RP, RN would be set during the calibration process to provide substantially optimal termination," and that the termination enable signals ENP and ENN would be generated during calibration as well. Ex. 1006, 6:3-5; Ex. 1002, Appx, 89-95.

iv. 17[c] the first calibration to be performed during a first calibration interval prior to normal system operation; and

As discussed in Ground 1, *Meaney* discloses the first calibration to be performed during initialization, prior to normal system operation. *Supra* Section

VIII.A.7.ii. *Greeff* discloses calibrating parameters such as termination resistance prior to the first use of the system, which it refers to as "static calibration." Ex. 1006, 7:52-61; Ex. 1002, Appx, 96-99. A POSITA would have understood calibration performed prior to first use to be calibration performed "during a first calibration interval prior to normal system operation." Ex. 1002, Appx, 96-99.

v. 17[d] circuitry to periodically perform a second calibration, to update the existing value;

As discussed in Ground 1, *Meaney* discloses periodically subjecting receiver circuitry to a second calibration in the form of a "recalibration" that updates an existing parameter value. *Supra* Sections VIII.A.7.ii, iv. As discussed above in 17[b], *Greeff* discloses circuitry for performing calibration of termination resistance. *Greeff* further discloses recalibrating termination resistance during operation of the system, for example when the value changes due to temperature or supply voltage changes, which *Greeff* refers to as "dynamic calibration." Ex. 1006, 7:52-65; Ex. 1002, Appx, 100-105. Thus, the combination of *Meaney* and *Greeff* discloses circuitry to periodically recalibrate an existing value of termination resistance. Ex. 1002, Appx, 100-105.

vi. 17[e] wherein the existing value is initially set and periodically updated responsive to the first calibration and the second calibration, respectively, and

As discussed in Ground 1, *Meaney* discloses determining an initial value for a parameter through an initial calibration and periodically performing a recalibration to update the parameter value. *Supra* Section VIII.A.1.ii, iii.

Greeff discloses calibration techniques including initially setting a termination resistance at a known value and then performing the calibration process to update the value. Ex. 1006, 8:27-33 ("Another calibration process may [ ] first set[] the resistance of the pull-up (or pull-down) resistor . . . against a known passive resistor, and then balance[e] the pull-down (or pull-up) resistor."); Ex. 1002, Appx, 106-111. *Greeff* also discloses an initial calibration to set a value (static calibration) and a second calibration (dynamic calibration) to adapt to changes in operating conditions. Ex. 1006, 4:10-13, 7:52-617:52-65; Ex. 1002, Appx, 106-111.

Thus, *Meaney* and *Greeff*, in view of the knowledge of a POSITA, render obvious "wherein the existing value is initially set and periodically updated responsive to the first calibration and the second calibration, respectively." Ex. 1002, Appx, 106-111.

vii. 17[f] wherein the second calibration is constrained to be performed during a time period that is shorter than a time period of the first calibration; and

As discussed in Ground 1, *Meaney* discloses "wherein the second calibration is constrained to be performed during a time period that is shorter than a time period of the first calibration." *Supra* VIII.A.1.vi; Ex. 1002, Appx, 112-113.

viii. 17[g] wherein the system further comprises a receive component, the at least one to be applied to permit proper reception of a digital signal to be communicated across a communications channel.

As discussed in Ground 1, *Meaney* discloses "a system further comprises a receive component" and at least one parameter "to be applied to permit proper reception of a digital signal to be communicated across a communications channel." *Supra* VIII.A.1.i & iii.

Greeff further discloses that the termination resistance and a driver strength are applied to permit proper reception of a digital signal to be communicated across a communications channel. Ex. 1002, Appx, 113-117. *Greeff* explains that termination resistance is calibrated to provide substantially optimal termination of the bus, and that drive strength is calibrated to improve achieve the desired active termination. Ex. 1006, 1:28-31, 4:10-12. Both of these calibrations are performed to improve the termination of the system, which improves digital signal integrity by minimizing transmission line reflections. Ex. 1006, 1:28-31, 4:10-12, 8:3-5; Ex. 1002, Appx, 113-17.

7. Claim 18

i. The system of claim 17, wherein the circuitry to perform the second calibration is, responsive to the second calibration, to perform one of an increment operation or a decrement operation upon the existing value if the desired value has drifted from the existing value by more than a delta value relative to an existing value.

As discussed in Ground 1, *Meaney* discloses this limitation either alone or in combination with the knowledge of a POSITA. *Supra* Section VIII.A.10. Specifically, *Meaney* discloses that the receive component performs, responsive to the second calibration, one of an increment operation or a decrement operation upon the existing value if a desired value of the parameter has drifted from the existing value by more than a delta value. *Id. Meaney* further discloses that recalibration may be performed in response to a trigger event that suggests that the parameter has drifted and the data capture time window has changed and is no longer accurate, which may be indicated, for example, by the detection of correctable errors. *Id.* Moreover, as explained in Ground 1, it would have been obvious to a POSITA, in response to a recalibration, to perform an increment operation or a decrement operation on the existing value, to shift the value of the based on the results of the recalibration. *Id.*

Greeff similarly discloses increasing and decreasing parameters used in the active termination circuit to account for variations in process, voltage, or temperature. *Greeff*, Ex. 1006, 7:66-8:5; Ex. 1002, Appx, 118-20. It would have been obvious to a POSITA to, in response to a recalibration, implement the increment or decrement operations of *Meaney* (and that were known in the art) when calibrating the termination resistance of *Greeff*. Ex. 1002, Appx, 118-20.

8. Claim 19

i. The system of claim 18, further comprising circuitry to store a first expected pattern and a second expected pattern, and circuitry to compare the first expected pattern with a pattern received from an external component in association with the first calibration, and to compare the second expected pattern with a pattern received from the external component in association with the second calibration.

As discussed in Ground 1, *Meaney* discloses circuitry to store a first expected pattern and a second expected pattern, and circuitry to compare the first expected pattern with a pattern received from an external component in association with the first calibration, and to compare the second expected pattern with a pattern received from the external component in association with the second calibration. *Supra* Sections VIII.A.6, 11; Ex. 1002, Appx, 121.

D. *Ground 4: Claims 4, 5, 13, 14, and 17-19 are obvious over Meaney, Nguyen and Greeff in view of the knowledge of a POSITA*

The combination of *Meaney*, *Nguyen* and *Greeff* discloses and/or suggests all limitations of claims 4, 5, 13, 14, and 17-19, and thus renders those claims obvious. Ex. 1002, Appx, 124-48. Specifically, as discussed above in Ground 2, *Meaney* in combination with *Nguyen* discloses applying offsets to existing values to determine a calibrated value, and circuitry for receiving a digital signal, calibrating computer system parameters, and storing calibration data. Ex. 1002, Appx, 54. Additionally, as discussed above in Ground 3, *Meaney* and *Greeff*, in view of the knowledge of a

POSITA, render obvious "an existing value representative of at least one of a termination resistance and a driver strength." *Id.*, Appx, 86-87. As discussed below, for the same reasons, the combination of *Meaney*, *Nguyen*, and *Greeff* discloses those same limitations. All other elements of claims 4, 5, 13, 14, and 17-19 are disclosed or rendered obvious by *Meaney* as explained in Ground 1.

1. One of skill in the art would have been motivated to combine *Meaney*, *Nguyen*, and *Greeff*

In addition to being motivated to combine *Meaney* and *Nguyen* as described in Section VIII.B.1 of Ground 2, a POSITA would have been motivated to further combine *Meaney* and *Nguyen* with *Greeff* with a reasonable expectation of success for the same reasons discussed above in Section VIII.C.1; Ex. 1002, Appx, 124.

2. Claims 4, 5, 13, and 14

As discussed above in Ground 3, each and every element of claims 4, 5, 13, and 14 are taught by *Greeff*. *Supra* Sections VIII.C.2-5. The combination of *Meaney*, *Nguyen*, and *Greeff* as described above, does not affect the disclosure of *Greeff* that render those claims obvious. Accordingly, the combination of *Meaney*, *Nguyen*, and *Greeff* render claims 4, 5, 13, and 14 obvious for the same reasons as discussed in Ground 3.

3. Claim 17

As discussed in Ground 3, elements 17[pre], 17[c], 17[e], 17[f], and 17[g] are taught by *Meaney* and *Greeff*. *Supra* Sections VIII.C.6.i, iv-vii.

i. 17[a] circuitry to store an existing value representative of at least one of a termination resistance and a driver strength to be applied in association with data communicated across a channel;

As discussed in Ground 2, *Meaney* and *Nguyen* disclose circuitry to store an existing value of a parameter. *Supra* Section VIII.B.5.ii. As discussed in Ground 3, *Meaney* and *Greeff* disclose termination resistance to be applied in association with data communicated across a channel. *Supra* Section VIII.C.6.ii; Ex. 1002, Appx, 125.

ii. 17[b] circuitry to perform a first calibration at system initialization, to identify a first value to be initially applied as the existing value,

As discussed in Ground 3, *Meaney* and *Greeff* disclose circuitry to perform a first calibration at system initialization, to identify a first value to be initially applied as the existing value. *Supra* Section VIII.C.6.ii. To the extent Patent Owner argues that *Meaney* and *Greeff* do not disclose circuitry to perform a first calibration, *Nguyen* discloses calibration circuitry. *Supra* Sections VIII.B.2.i, VIII.B.7; Ex. 1002, Appx, 125-33.

iii. 17[d] circuitry to periodically perform a second calibration, to update the existing value;

As discussed in Ground 3, *Meaney* and *Greeff* disclose circuitry to perform a second to update the existing value. *Supra* Section VIII.C.6.v; Ex. 1002, Appx, 134-41. To the extent Patent Owner argues that *Meaney* and *Greeff* do not disclose

circuitry to perform a second calibration, *Nguyen* discloses such calibration circuitry. *Supra* Sections VIII.B.2.ii, VIII.B.7; Ex. 1002, Appx, 134-41.

4. Claims 18 and 19

As discussed above in Ground 3, claim 18 is taught by the combination of *Meaney* and *Greeff*, and claim 19 is taught by *Meaney*. *See supra* Sections VIII.C.7-8; Ex. 1002, Appx, 143-48.

E. *Ground 5A: Claim 3 is obvious over Meaney and Allee in view of the knowledge of a POSITA*

1. One of skill in the art would have been motivated to combine *Meaney* and *Allee*

As described above, *Meaney* discloses calibration by comparing a known data pattern with a received data pattern. *Supra* Section VIII.A.6. *Allee* provides details of a comparator that is self-calibrating and allows expansion of the functionality of digital integrated circuits. Ex. 1007, 2:35-36, 3:9-19; Ex. 1002, Appx, 149. A POSITA would have been motivated to combine *Meaney* and *Allee* with a reasonable expectation of success to use the comparator of *Allee* to compare the data patterns of *Meaney* to achieve the stated benefits of self-calibration and expanded functionality of digital circuitry. Ex. 1002, Appx, 149. Accordingly, a POSITA would have been motivated to combine *Meaney* and *Allee* with a reasonable expectation of success, because the teaching, suggestion, and motivation in *Meaney* and in *Allee* would have led a POSITA to arrive at the claimed invention. *Id*.

2. Claim 3

i. The method of claim 1, wherein the parameter is a voltage level for a comparator.

Allee discloses computer systems including comparators that may be calibrated by a self-calibration circuit 116 to adjust the input voltage ("voltage level for a comparator"). Ex. 1007, 3:9-19,4:1-9, 6:17-39, Fig. 1; Ex. 1002, Appx, 149-151. As depicted in Fig. 1 below, *Allee* discloses comparators 102 that may be self-calibrated to compensate for an input offset by adjusting an input signal equal to a desired reference voltage. Ex. 1007, 3:9-19, Fig. 1 (annotated).

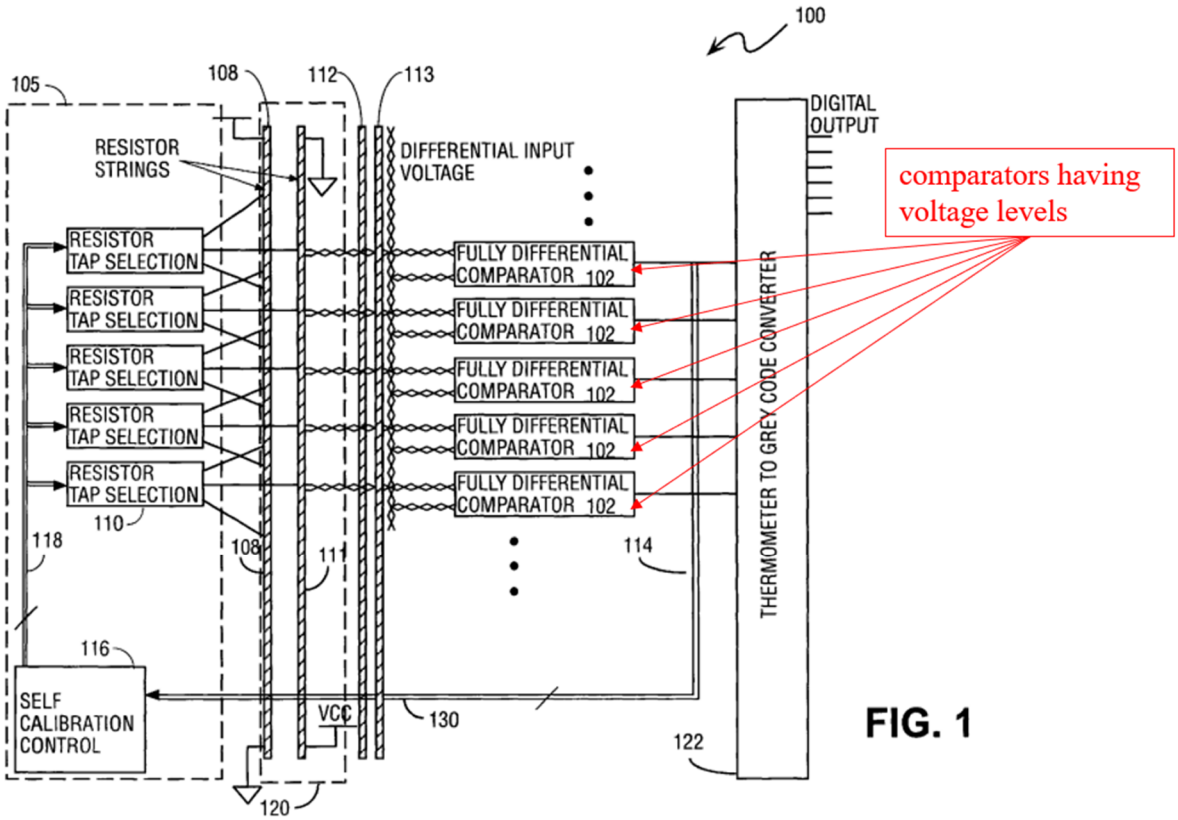


FIG. 1

Allee further discloses a self-calibration circuit 116 that calibrates the comparators 102 to adjust the voltage by adjusting the tap position of the reference voltage. Ex. 1007, 4:1-9; Ex. 1002, Appx, 149-150. *Allee* discloses both an initial calibration process (before operation), and self-calibration of the comparator during operation. Ex. 1007, 6:17-39; Ex. 1002, Appx, 149-151.

F. *Ground 5B: Claim 3 is obvious over Meaney and Nguyen and Allee in view of the knowledge of a POSITA*

1. One of skill in the art would have been motivated to combine *Meaney*, *Nguyen,* and *Allee*

In addition to being motivated to combine *Meaney* with *Nguyen* as explained in Section VIII.B.1, a POSITA would have been motivated to further combine *Meaney* and *Nguyen* with *Allee* with a reasonable expectation of success for the same reasons stated above in Section VIII.E.1. Ex. 1002, Appx, 152.

2. Claim 3

ii. The method of claim 1, wherein the parameter is a voltage level for a comparator.

Supra Section VIII.E.2.

IX. CONCLUSION

Petitioner respectfully requests that *inter partes* review of the ’466 Patent be instituted and that the Challenged Claims be cancelled as unpatentable under 35 U.S.C. § 318(b).

Respectfully submitted,

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Dated: August 13, 2024

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CERTIFICATE OF SERVICE

The undersigned hereby certifies on this 13th day of August 2024, that true and correct copies of the foregoing PETITION FOR *INTER PARTES* REVIEW OF CLAIMS 1-19 OF U.S. PATENT NO. 9,160,466 and Exhibits 1001-1010, and Petitioner's power of attorney were served in their entirety to Patent Owner via FedEx Express® or Express Mail:

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CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATION, TYPEFACE REQUIREMENTS, AND TYPE STYLE REQUIREMENTS

1. This Petition complies with the type-volume limitation of 14,000 words, comprising 13,664 words, excluding the parts exempted by 37 C.F.R. § 42.24(a).

2. This Petition complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word in 14-point Times New Roman.

Respectfully submitted,

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