

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SILICON MOTION INC.,
Petitioner,

v.

K.MIZRA LLC.,
Patent Owner.

IPR2024-01240
Patent 9,160,466 B2

Before MITCHELL G. WEATHERLY, MICHELLE N. WORMMEESTER,
and AARON W. MOORE, *Administrative Patent Judges*.

WORMMEESTER, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Silicon Motion Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1–19 of U.S. Patent No. 9,160,466 B2 (Ex. 1001, “the ’466 patent”). K.Mizra LLC (“Patent Owner”) filed a Preliminary Response (Paper 6, “Prelim. Resp.”).

We have authority under 35 U.S.C. § 314 and 37 C.F.R. § 42.4(a). Pursuant to 35 U.S.C. § 314(a), an *inter partes* review may not be instituted “unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” For the reasons that follow, we institute an *inter partes* review as to all the challenged claims of the ’466 patent based on all the challenges presented.

II. BACKGROUND

A. *Related Proceedings*

The parties identify one federal district court case involving the ’466 patent. Pet. 1; Paper 3, 2–3 (Patent Owner’s Mandatory Notices). Petitioner also identifies a petition for *inter partes* review of a related patent. Pet. 1.

B. *The ’466 Patent*

The ’466 patent relates to calibration of communication channel parameters in systems where components communicate via interconnection links. Ex. 1001, 1:26–31. To illustrate an exemplary system, Figure 1 of the ’466 patent is reproduced below.

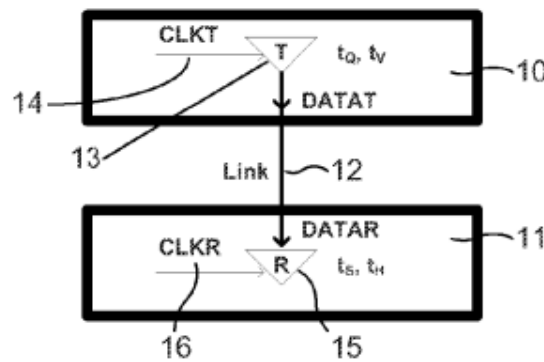


Fig. 1

Figure 1 shows a system with components 10 and 11 connected via link 12. *Id.* at 5:24–25, 6:13–14. Component 10 includes transmitter circuit 13, which drives bits on link 12. *Id.* at 6:14–17. These bits form signal DATAT. *Id.* at 6:17. Component 11 includes receiver circuit 15, which samples bits on link 12. *Id.* at 6:18–20. These bits form signal DATAR, which is an attenuated, time-delayed copy of DATAT. *Id.* at 6:21–23.

Together, transmitter 13, link 12, and receiver 15 comprise a communication channel characterized by various parameters. Ex. 1001, 6:25–28. These parameters may include, for example, drive times, sample times, link termination resistances, and driver strength. *Id.* at 6:28–35. An initial calibration sequence is used to determine the optimal operation value of a parameter, where the operation value refers to the value of the parameter that is used during normal operation of the communication channel. *Id.* at 3:8–11, 3:16–28; *see also id.* at 3:1–5.

Yet during normal operation, system conditions may change; that is, they may drift from their initial operation values. Ex. 1001, 2:31–35. These conditions may include, for example, ambient temperature, component temperature, supply voltages, and reference voltages. *Id.* at 2:33–35. As conditions drift, the optimal timing points of the transmitter and receiver as well as other parameters may change. *Id.* at 2:36–38.

A calibration sequence that is simpler than the initial calibration sequence is applied to track drift of a particular parameter during operation. Ex. 1001, 2:66–3:5. The system uses changes in the parameter to adjust the operation value that was created using the initial calibration sequence. *Id.* at 3:5–8. According to the '466 patent, the simpler calibration sequence occupies link 12, transmitter 13, and receiver 15 for less time than the initial calibration sequence. *Id.* at 3:1–5. In other words, the simpler calibration uses fewer of the communication channel's resources. *Id.*

Thus, the '466 patent “provides a system and method for calibrating an operation value for a parameter of a communication channel, which allows for optimizing the operation value of the parameter, while efficiently accounting for drift of properties of the channel.” Ex. 1001, 3:12–16.

C. Illustrative Claim

Petitioner challenges claims 1–19 of the '466 patent. Claims 1, 10, and 17 are the independent challenged claims. Claim 1 is illustrative and is reproduced below.

1. A method of operation in a system that includes a receive component having circuitry to receive a digital signal, the method comprising:
 - subjecting the receive component to a first calibration during initialization to identify an initial value for a parameter affecting proper reception by the circuitry of the receive component of data communicated across a channel as part of the digital signal;
 - periodically subjecting the receive component to a second calibration to update an existing value of the parameter for drift attributable to change in at least one of operating voltage or temperature; and

wherein the existing value is dependent on the initial value
and wherein the second calibration is constrained to occur
during a time period that is shorter than a time period of
the first calibration.

D. Asserted Challenges to Patentability

Petitioner asserts six challenges against various subsets of
claims 1–19 of the ’466 patent as follows.¹ Pet. 11–12, 14–69.

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 6–12, 15, 16	103(a) ²	Meaney ³
1, 2, 6–12, 15, 16	103(a)	Meaney, Nguyen ⁴
4, 5, 13, 14, 17–19	103(a)	Meaney, Greeff ⁵
4, 5, 13, 14, 17–19	103(a)	Meaney, Nguyen, Greeff
3	103(a)	Meaney, Allee ⁶
3	103(a)	Meaney, Nguyen, Allee

In support of its challenges, Petitioner relies on a Declaration of R.
Jacob Baker, Ph.D., P.E. (Ex. 1002).

¹ For each asserted challenge, Petitioner also lists the knowledge of a person of ordinary skill in the art (POSITA). Pet. 11–12. We note “the knowledge of such an artisan is part of the store of public knowledge that must be consulted when considering whether a claimed invention would have been obvious.” *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2013). Accordingly, we consider the knowledge of a POSITA as part of our obviousness analysis.

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284 (2011), amended 35 U.S.C. § 103, effective March 16, 2013. Because the application from which the ’466 patent issued claims priority to an application filed before this date, the pre-AIA version of § 103 applies.

³ U.S. Publ’n No. 2003/0070123 A1, published Apr. 10, 2003 (Ex. 1004).

⁴ U.S. Publ’n No. 2003/0151450 A1, published Aug. 14, 2003 (Ex. 1005).

⁵ U.S. Patent No. 6,356,106 B1, issued Mar. 12, 2002 (Ex. 1006).

⁶ U.S. Patent No. 6,255,979 B1, issued July 3, 2001 (Ex. 1007).

III. DISCUSSION

A. Level of Ordinary Skill in the Art

Petitioner asserts that “a POSITA would have had a bachelor’s degree in Electrical Engineering, Computer Engineering, or a related field as well as at least two years of academic or industry experience in design and implementation of high-speed digital communication systems.” Pet. 13. Petitioner further asserts that “[a]n individual with an advanced degree in a relevant field, such as computer or electrical engineering, would require less experience in the design and implementation of high-speed digital communication systems, and vice versa.” *Id.* Patent Owner “does not contest Petitioner’s definition of a person of ordinary skill in the art, but it reserves the right to do so if trial is instituted.” Prelim. Resp. 7. There being no present dispute, we adopt Petitioner’s formulation for purposes of this Decision.

B. Claim Construction

In an *inter partes* review proceeding, we construe a claim of a patent “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” *See* 37 C.F.R. § 42.100(b). That standard involves construing claims in accordance with the ordinary and customary meaning of such claims as would have been understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. *See id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005) (en banc).

Petitioner asserts that it “does not propose any constructions.” Pet. 13. Patent Owner does not respond other than to say, “Should the Board

institute trial, Patent Owner reserves the right to present claim construction positions.” Prelim. Resp. 7.

For purposes of this Decision, we determine that no claim term requires express interpretation to resolve any controversy in this proceeding. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (noting that “we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

C. Alleged Obviousness Over Meaney

Petitioner asserts that claims 1, 2, 6–12, 15, and 16 of the ’466 patent would have been obvious over Meaney. Pet. 14–37. Patent Owner challenges certain aspects of Petitioner’s analysis for claim 1. Prelim. Resp. 9–13. For the reasons explained below, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing on its asserted challenge.

Before addressing the parties’ arguments, we provide an overview of Meaney.

1. Overview of Meaney

Meaney describes a “method for recalibrating a[] source-synchronous pipelined interface with minimal impact to a running system, allowing for the system to remain operational, even in the midst of environmental drift or degradation.” Ex. 1004 ¶ 1. Meaney’s recalibration is applicable in prior art symmetric multiprocessing (SMP) computer systems. *Id.* ¶¶ 3, 8.

Meaney explains that “[i]n an SMP . . . computer system with high-level packaging, it is often necessary to allow latencies on cards, wires, or boards that exceed the cycle times of the transferred data.” Ex. 1004 ¶ 3. To capture the data, the system applies an initial calibration where “[a] known data pattern is sent across the interface and the receiver compensates for the various package tolerances using calibration techniques.” *Id.* ¶ 4; *see also id.* ¶ 23, Fig. 1 (prior art interface). The initial calibration sequence includes several steps:

1. Setting interface fences (block interface from being used by system operations)
2. Resetting interface state machine
3. Turning on the driver calibration pattern
4. Calibrating clock
5. Deskewing the data, one bit at a time
6. Recalibrating clock
7. Turning off driver calibration pattern
8. Resetting interface fences.

Ex. 1004 ¶¶ 24–32.

Over time, the interface may drift due to changes in the environment, such as voltage, temperature, and end-of-life degradation. Ex. 1004 ¶ 5. Cumulative degradations may cause a system failure. *Id.* ¶ 6. According to Meaney, prior art machines could only handle the initial calibration; they could not recalibrate an interface once it was in operation. *Id.* In other words, the interface could not be recalibrated without resetting the state machine and starting the entire calibration sequence over. *Id.* ¶ 33.

Meaney further explains that in a test environment, users “often want to run a hardware/architecture exerciser . . . under several environments,” where the interface may fail without a recalibration. Ex. 1004 ¶ 7. If the

system cannot be recalibrated under the new environment, the system must be restarted for every test, thereby jeopardizing the test time. *Id.*

To “allow[] for the re-calibration of the interface at periodic intervals with minor disruption,” Meaney introduces a recalibration sequence that involves “[p]utting the system of the interface into a wait state,” then “[p]erforming a fast initialization process for calibration,” and then “[t]aking the system of the interface out of a wait state.” Ex. 1004 ¶¶ 8–12. Meaney explains that “[t]he fast initialization process . . . is similar to the prior art [initial calibration], except that there is only one clock centering step, instead of two,” and “the data deskew step is skipped since that step has already been performed as part of the original initialization process [(i.e., initial calibration)].” *Id.* ¶ 13. Thus, Meaney’s recalibration sequence includes the following steps:

1. Putting the interface or system into a wait state,
2. Setting interface fences (block interface from being used by system operations)
3. Resetting interface state machine
4. Turning on the driver calibration pattern
5. Calibrating clock
6. Turning off driver calibration pattern
7. Resetting interface fences
8. Taking the interface or system out of a wait state.

Id. ¶¶ 42–50. According to Meaney, its recalibration sequence is “fast enough to avoid the system hangs that the full calibration would cause.” *Id.* ¶ 51.

2. Analysis

We turn now to the claims, starting with independent claim 1.

a. Independent Claim 1

Claim 1 is directed to a method and recites various limitations that Petitioner designates as limitations 1a through 1e. Patent Owner disputes limitation 1e in particular. Prelim. Resp. 9–16. We address the preamble of claim 1 as well as each limitation in turn.

i. Preamble

The preamble of claim 1 recites “[a] method of operation in a system that includes a receive component having circuitry to receive a digital signal.” For the preamble, Petitioner provides an annotated version of Figure 1 of Meaney, which is reproduced below. Pet. 15.

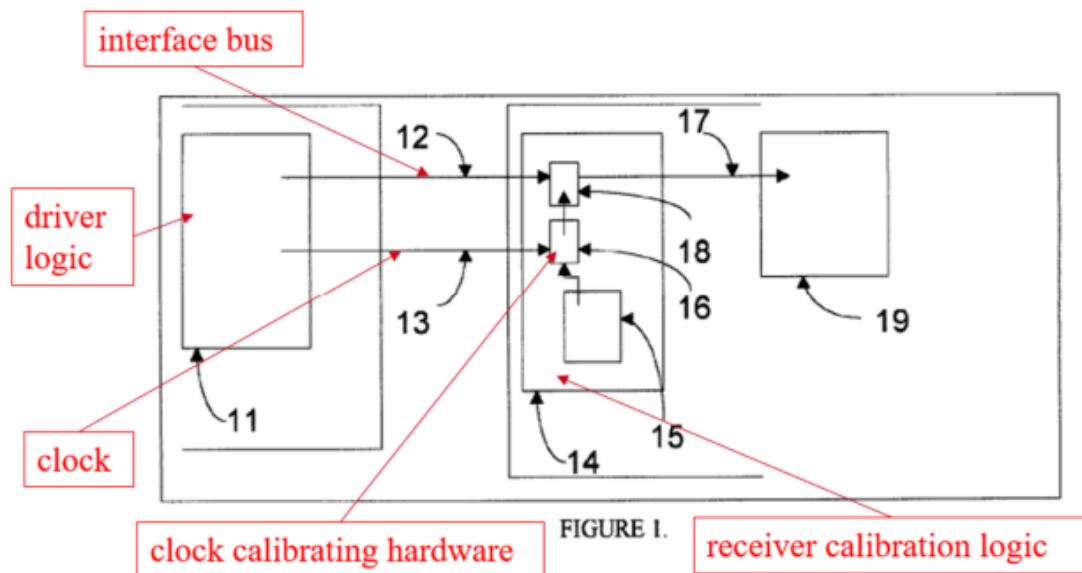


Figure 1 of Meaney, as annotated by Petitioner, shows what Meaney describes as a prior art source-synchronous pipelined interface. *See* Ex. 1004 ¶ 19. The interface includes driver logic 11, interface bus 12, and receiver calibration logic 14. *Id.* ¶ 23. Petitioner identifies receiver calibration logic 14 as a “receive component.” Pet. 15. As support, Petitioner asserts that “[t]he computer systems . . . of *Meaney* include a

‘receiver’ and ‘[receiver calibration] logic 14’ for capturing (i.e., receiving) transferred data from driver logic 11 through the interface bus 12.” *Id.* (citing Ex. 1004 ¶¶ 3, 4, 23). Petitioner also asserts that “*Meaney* further discusses the hardware and circuitry of its computer systems and the need to calibrate the receiver to compensate changes to the ‘circuit.’” *Id.* (citing Ex. 1004 ¶¶ 7, 15, 16, 20, 21, claim 12). According to Petitioner, “[a] POSITA would have understood that the receiver of *Meaney* would have circuitry to receive a digital signal.” *Id.* (citing Ex. 1002, app. A at 1–5).

Patent Owner does not dispute Petitioner’s analysis for the preamble of claim 1. *See* Prelim. Resp. Based on Petitioner’s argument and evidence, we are persuaded that Petitioner has shown sufficiently for purposes of this Decision that *Meaney* teaches the recited subject matter of the preamble. As such, we need not and do not determine whether the preamble is limiting.

ii. Limitation 1a: “subjecting the receive component to a first calibration”

Claim 1 recites “subjecting the receive component to a first calibration during initialization to identify an initial value.” For this limitation, which Petitioner designates as limitation 1a, Petitioner asserts that “*Meaney* discloses an initial calibration of the receive component from a stopped position before the interface is in operation.” Pet. 16 (citing Ex. 1004 ¶¶ 6, 21, 24, Fig. 3; Ex. 1002, app. A at 6–8). As support, Petitioner points to where *Meaney* says that prior art machines could only provide for calibration “from a stopped position” and had “no way to re-calibrate an interface once it was up and running,” whereas *Meaney*’s system provides for both “the initial calibration as well as the recalibration of the hardware.” Ex. 1004 ¶¶ 6, 21, 24 (cited by Pet. 16). Petitioner also points to where

Meaney teaches that the receiver calibration logic performs calibrations. Pet. 16 (citing Ex. 1004 ¶¶ 4, 38, Fig. 3).

Petitioner further asserts that “[o]ne of the parameters calibrated to an initial value is clock delay.” Pet. 16 (citing Ex. 1004 ¶ 40; Ex. 1002, app. A at 6–8). Petitioner points us to where Meaney teaches that the receiver calibration logic includes clock calibrating hardware. *Id.* (citing Ex. 1004 ¶ 23). Petitioner adds that Meaney “discloses determining an initial value for clock delay during initialization by disclosing that future re-calibrations will be determined based on the original clock delay.” *Id.* (citing Ex. 1004 ¶¶ 40, 51, claim 12).

Patent Owner does not dispute Petitioner’s analysis for this limitation. *See* Prelim. Resp. Based on Petitioner’s argument and evidence, we are persuaded that Petitioner has shown sufficiently for purposes of this Decision that Meaney teaches or suggests the recited “subjecting” step of limitation 1a.

iii. Limitation 1b: “parameter affecting proper reception”

In connection with limitation 1a, claim 1 further recites that the “initial value” is “for a parameter affecting proper reception by the circuitry of the receive component of data communicated across a channel as part of the digital signal.” For this limitation, which Petitioner designates as limitation 1b, Petitioner asserts that Meaney’s “calibrated parameter (clock delay) affects proper reception by the circuitry of the receive component of data communicated across a channel as part of the digital signal.” Pet. 17 (citing Ex. 1002 ¶¶ 3–4, 40; Ex. 1002, app. A at 8–9). As support, Petitioner asserts that “*Meaney* explains that in transferring data in its computer

system, the data must be captured by the receiver within a small temporal window, or ‘eye.’” *Id.* (citing Ex. 1004 ¶ 3). Petitioner also asserts that “*Meaney* further explains that the calibration of the clock delay . . . ‘is able to **find the optimum data capture time for the interface,**’” and “[s]ince the calibration is done periodically, **this window gets reoptimized every time** recalibration occurs.” *Id.* (quoting Ex. 1004 ¶ 40). Petitioner further notes that “*Meaney* states that this allows the receiver to recalibrate to new conditions such as changes to cycle time, voltage, or the computing environment.” *Id.* (citing Ex. 1004 ¶ 40).

Patent Owner does not dispute Petitioner’s analysis for this limitation. *See* Prelim. Resp. Based on Petitioner’s argument and evidence, we are persuaded that Petitioner has shown sufficiently for purposes of this Decision that *Meaney* teaches or suggests the recited “parameter” of limitation 1b.

iv. Limitation 1c: “periodically subjecting the receive component to a second calibration”

Claim 1 further recites “periodically subjecting the receive component to a second calibration to update an existing value of the parameter for drift attributable to change in at least one of operating voltage or temperature.” For this limitation, which Petitioner designates as limitation 1c, Petitioner asserts that “*Meaney* discloses periodically subjecting the receive component to a second calibration in the form of a ‘recalibration.’” Pet. 17 (citing Ex. 1004 ¶¶ 8–9, 38). Petitioner also asserts that *Meaney*’s “initial value for clock delay . . . discloses the ‘existing value of the parameter,’” or, alternatively, “because *Meaney* discloses several periodic recalibrations, the

output value from previous recalibrations would be the existing value for the next recalibration.” *Id.* at 17–18 (citing Ex. 1004 ¶¶ 8, 16, 40). Petitioner adds that “*Meaney* discloses that the recalibrations of the clock delay allow the receiver to compensate for ‘drift over time on the interface to compensate for temperature, voltage, cycle time, and end-of-life degradation.’” *Id.* at 18 (quoting Ex. 1004, code (57)); *see also id.* (citing Ex. 1004 ¶¶ 15–16, 40; Ex. 1002, app. A at 9–10). According to Petitioner, “[a] POSITA would have understood this as rendering obvious [the subject matter of limitation 1c].”

Patent Owner does not dispute Petitioner’s analysis for this limitation. *See* Prelim. Resp. Based on Petitioner’s argument and evidence, we are persuaded that Petitioner has shown sufficiently for purposes of this Decision that *Meaney* teaches or suggests the recited “periodically subjecting” step of limitation 1c.

v. Limitation 1d: “existing value”

Claim 1 further recites “wherein the existing value is dependent on the initial value.” Petitioner designates this limitation as limitation 1d. As discussed above with respect to limitation 1c, Petitioner identifies either “the initial value for clock delay or a clock delay value that was determined from previous recalibrations” as the “existing value.” Pet. 18–19. Petitioner contends that “[a] POSITA would have understood that either alternative of the ‘existing values’ of *Meaney* are dependent on the initial value.” *Id.* at 19 (citing Ex. 1002, app. A at 10–13).

With respect to Petitioner’s first theory, where *Meaney*’s initial value for clock delay is the “existing value,” Petitioner asserts that “the initial

value is copied or adopted as the existing value to be used as the starting point for the next calibration.” Pet. 19 (citing Ex. 1002, app. A at 10–13).

As to Petitioner’s second theory, where Meaney’s clock delay value that was determined from a previous recalibration is the “existing value,” Petitioner asserts that “the output of a previous recalibration . . . is necessarily determined, directly, or indirectly, based on one or more recalibrations of the initial value for clock delay.” Pet. 19 (citing Ex. 1002, app. A at 10–13). Petitioner asserts that “*Meaney* explains that recalibration reoptimizes the window for data capture by recalibrating the existing clock delay to account for changes in conditions, and discloses that this recalibration occurs without resetting the hardware.” *Id.* (citing Ex. 1004 ¶¶ 33, 40, 51). According to Petitioner, “[a] POSITA would have understood that these recalibrations would be performed based on the existing clock delay value.” *Id.* (citing Ex. 1002, app. A at 11). To illustrate, Petitioner asserts,

For the first recalibration performed after the initial calibration, the initial value would be used as a starting point in the recalibration to generate a new clock delay, which was generated based on the initial clock delay value. . . . For the next recalibration, the starting point (the claimed “existing value”) would be the new clock delay, which was generated from, and thus dependent on, the initial value.

Id. (citing Ex. 1002, app. A at 11). Petitioner also asserts that “*Meaney* discloses that the clock can be recalibrated by ‘adding delay’ to the clock path or applying a delay shift to the existing clock delay.” *Id.* at 19–20 (citing Ex. 1004 ¶¶ 40, 51; Ex. 1002, app. A at 11).

Patent Owner does not dispute Petitioner’s analysis for this limitation. *See* Prelim. Resp. Based on Petitioner’s argument and evidence,

we are persuaded that Petitioner has shown sufficiently for purposes of this Decision that Meaney teaches or suggests the recited “existing value” of limitation 1d.

vi. Limitation 1e: “second calibration”

Lastly, claim 1 recites “wherein the second calibration is constrained to occur during a time period that is shorter than a time period of the first calibration.” For this limitation, which Petitioner designates as limitation 1e, Petitioner asserts that “*Meaney* discloses that the recalibration is faster and has fewer steps than the initial calibration performed during the original initialization process.” Pet. 20 (citing Ex. 1004 ¶¶ 8, 13, 38–39). As support, Petitioner asserts that Meaney specifically “discloses that recalibration is performed using a ‘fast initialization’ process that can occur with minor disruption to the computer system by skipping certain steps (e.g., a data deskew and a clock centering step) that are performed during the original initialization process.” *Id.* (citing Ex. 1004 ¶¶ 8, 13, 38, Fig. 3). Petitioner also asserts that “the initial calibration of *Meaney* is performed from a stopped position, whereas the recalibration merely requires putting the system in a ‘wait’ state for the duration of the recalibration.” *Id.* at 20–21 (citing Ex. 1004 ¶¶ 24, 35, 39, 41). According to Petitioner, “a POSITA would have understood that the recalibration of *Meaney* would occur during a time period that is shorter than the time period of *Meaney*’s initial calibration.” *Id.* at 21 (citing Ex. 1002, app. A at 13–14).

Patent Owner responds that “*Meaney* does not disclose or render obvious the limitation recit[ing] that ‘second calibration is constrained to occur during a time period that is shorter than a time period of the first

calibration.” Prelim. Resp. 10. Patent Owner argues that “Petitioner relies on conclusory statements.” Prelim. Resp. 10. In particular, Patent Owner characterizes Petitioner’s statement that “a POSITA would have understood that the recalibration of *Meaney* would occur during a time period that is shorter than the time period of *Meaney*’s initial calibration” as a “conclusory statement that is insufficient to meet this limitation.” *Id.* (citing Pet. 21).

We disagree with Patent Owner. Patent Owner makes arguments that are not supported by citations to evidence; that is attorney argument. Petitioner’s statement, on the other hand, is based on cited teachings in *Meaney*. For example, Petitioner points to where *Meaney* teaches that “[t]he fast initialization process in the preferred embodiment is similar to the prior art, except that there is only one clock centering step, instead of two,” and “the data deskew step is skipped since that step has already been performed as part of the original initialization process.” Ex. 1004 ¶ 13 (cited by Pet. 20). Petitioner further points to where *Meaney* calls the data deskew step “lengthy.” *Id.* ¶ 38 (cited by Pet. 20). Petitioner also draws attention to *Meaney*’s reference to the recalibration as a “‘fast initialization’ process.” Pet. 20. We are persuaded on this record that *Meaney*’s teachings together indicate that its recalibration not only has fewer steps than the initial calibration but also is *fast* relative to the initial calibration. *See* Ex. 1004 ¶ 13 (comparing “fast initialization process” with “original initialization process”). Accordingly, contrary to Patent Owner’s position, Petitioner’s statement that “a POSITA would have understood that the recalibration of *Meaney* would occur during a time period that is shorter than the time period of *Meaney*’s initial calibration” is not conclusory; rather, it is supported by cited teachings in *Meaney*.

Patent Owner further argues that “[n]othing in *Meaney* suggests that the recalibration period is constrained to be shorter than the initial calibration.” Prelim. Resp. 10. Patent Owner acknowledges the initial calibration in *Meaney* includes step 34 (initial clock calibration sequence), step 35 (data deskew sequence), and step 36 (final clock calibration sequence), whereas *Meaney*’s recalibration includes “a new wait state, 41, . . . which allows the calibration logic to proceed directly to the final clock calibration sequence, 36.” *Id.* (citing Ex. 1004 ¶ 39). Patent Owner asserts “[t]his purportedly allows *Meaney* to skip steps 34 . . . and 35 . . . from the initial calibration sequence,” but “Petitioner incorrectly assumes that steps 34, 35, and 36 in the initial calibration necessarily take longer than performing a new step 36 and new wait state 41 during recalibration.” *Id.* at 10–11; *see also id.* at 11–12 (arguing “the final clock calibration sequence (36) in the recalibration may in some instances take much longer to run than the final clock calibration sequence (36) that occurred during the initial calibration”); *id.* at 12 (arguing “*Meaney* does not disclose that the new wait state is constrained in time such that its running would not, at least in some instances, cause the run time of the recalibration sequence to exceed the run time of the initial calibration sequence”).

We disagree with Patent Owner. Patent Owner’s positions appear to be speculation that is not supported by citations to evidence or testimony. Moreover, as discussed above, we are persuaded on this record that the cited teachings in *Meaney* indicate that its recalibration not only has fewer steps than the initial calibration but also is *fast* relative to the initial calibration. Ex. 1004 ¶¶ 13, 38 (cited by Pet. 20). In other words, the recalibration time period is shorter than the initial calibration time period.

This reading of Meaney is supported by other cited portions of Meaney. For example, in describing shortcomings in the prior art, Meaney explains that in a test environment, users “often want to run a hardware/architecture exerciser . . . under several environments,” where the interface may fail without a recalibration. Ex. 1004 ¶ 7 (cited by Pet. 15). Meaney further explains that if the system cannot be recalibrated under the new environment, the system must be restarted for every test, which means “[the] *test time is jeopardized*.” *Id.* (emphasis added). In describing its own invention, Meaney notes that its recalibration is “*fast enough* to avoid the system hangs that the full calibration would cause.” *Id.* ¶ 51 (emphasis added) (cited by Pet. 19–20). Thus, Meaney identifies a prior art problem of “lengthy,” time-jeopardizing calibrations and addresses that problem with its “fast” or “fast enough” recalibrations. *See id.* ¶ 7 (“[I]f . . . the system must be restarted for every test. . . . our test time is jeopardized.”); *id.* ¶ 38 (“[I]t is not necessary to perform this lengthy [data deskew] step during recalibration.”); *id.* ¶ 13 (describing “[t]he fast initialization process in the preferred embodiment”); ¶ 51 (“[T]he preferred embodiment was fast enough to avoid the system hangs that the full calibration would cause.”). In light of the cited teachings in Meaney, we are persuaded that the recalibration period is constrained to be shorter than the initial calibration period.

Patent Owner argues that “being described as ‘fast’ does not mean that the ‘second calibration is constrained to occur during a time period that is shorter than a time period of the first calibration.’” Prelim. Resp. 13. As discussed above, however, Meaney’s recalibration is “fast” relative to the initial calibration. *See* Ex. 1004 ¶ 13 (comparing “fast initialization process”

with “original initialization process”). We are persuaded on this record that Meaney’s reference to a “fast” recalibration, relative to an initial calibration, indicates that the recalibration time period is constrained to be shorter than the initial calibration time period.

Lastly, Patent Owner points to Petitioner’s assertion that “the initial calibration of *Meaney* is performed from a stopped position, whereas the recalibration merely requires putting the system in a ‘wait’ state for the duration of the recalibration.” Prelim. Resp. 13 (quoting Pet. 20). Patent Owner argues that “the wait state adds time to the recalibration procedure, requiring time for the processors [to] reach an idle state.” *Id.*; *see also id.* at 12 (same argument). According to Patent Owner, “[i]t is not, as Petitioner argues, a time-saving feature over the initial calibration procedure in the purported invention of *Meaney* to the extent that ‘the second calibration is constrained to occur during a time period that is shorter than a time period of the first calibration.’” *Id.* at 13.

We disagree with Patent Owner. As discussed above, Meaney identifies a prior art problem of “lengthy,” time-jeopardizing calibrations and offers a solution to that problem with its “fast” or “fast enough” recalibrations. *See* Ex. 1004 ¶¶ 7, 13, 38, 51. These teachings in Meaney indicate that Meaney’s recalibration is indeed “a time-saving feature over the initial calibration,” contrary to Patent Owner’s position. *See* Prelim. Resp. 13.

On the record before us, Patent Owner’s arguments do not undermine Petitioner’s showing for limitation 1e. Based on Petitioner’s arguments and evidence, and for the reasons given above, we are persuaded that Petitioner has shown sufficiently for purposes of this Decision that Meaney teaches or

suggests “the second calibration is constrained to occur during a time period that is shorter than a time period of the first calibration.”

b. Independent Claim 10

Claim 10 recites similar limitations as claim 1, including “wherein a time duration of the second calibration is constrained to be shorter than a time duration of the first calibration.” For claim 10, the parties rely primarily on their arguments for claim 1. Pet. 28–32; Prelim. Resp. 13–14. Based on the record before us, and for the reasons given above regarding claim 1, we are persuaded that Petitioner’s showing for claim 10 is sufficient for purposes of this Decision.

c. Dependent Claims 2, 6–9, 11, 12, 15, and 16

Claims 2, 6–9, 11, 12, 15, and 16 depend from claims 1 or 10. Patent Owner does not separately dispute Petitioner’s analysis for these claims. Prelim. Resp. 13–14. Having reviewed Petitioner’s arguments and evidence for claims 2, 6–9, 11, 12, 15, and 16, we are persuaded that Petitioner’s showing for these claims is sufficient for purposes of this Decision. *See* Pet. 21–37.

3. Summary

In view of the foregoing, we determine that Petitioner has demonstrated a reasonable likelihood of showing that claims 1, 2, 6–12, 15, and 16 would have been obvious over Meaney.

D. Alleged Obviousness Over Meaney and Greeff

Petitioner asserts that claims 4, 5, 13, 14, and 17–19 of the '466 patent would have been obvious over Meaney and Greeff. Pet. 52–64. Patent Owner disputes certain aspects of Petitioner's analysis for claim 17. Prelim. Resp. 14–15. For the reasons explained below, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing on its asserted challenge.

We have already provided an overview of Meaney. *See supra* Part III.C.1. Before addressing the parties' arguments, we also provide an overview of Greeff.

1. Overview of Greeff

Greeff discloses a multidrop system with an active termination circuit. Ex. 1006, 1:5–8, Fig. 1. As background, Greeff explains that “[a]s signals propagate down [an electronic] system's transmission lines, e.g., traces on a printed circuit board (PCB), unwanted signal reflections may occur on the lines.” *Id.* at 1:13–16. Greeff further explains that “[t]he reflections are a result of mismatched impedances between the driver impedance, receiver impedances, and interconnecting transmission lines,” which could ultimately cause “the receiving device to respond incorrectly and possibly generate an erroneous result.” *Id.* at 1:16–27. According to Greeff, “[t]ermination is used in high-speed signaling systems to improve signal integrity and operating bandwidth by minimizing transmission line reflections.” *Id.* at 1:29–31.

To illustrate an exemplary embodiment of Greeff's system, Figure 1 of Greeff is reproduced below.

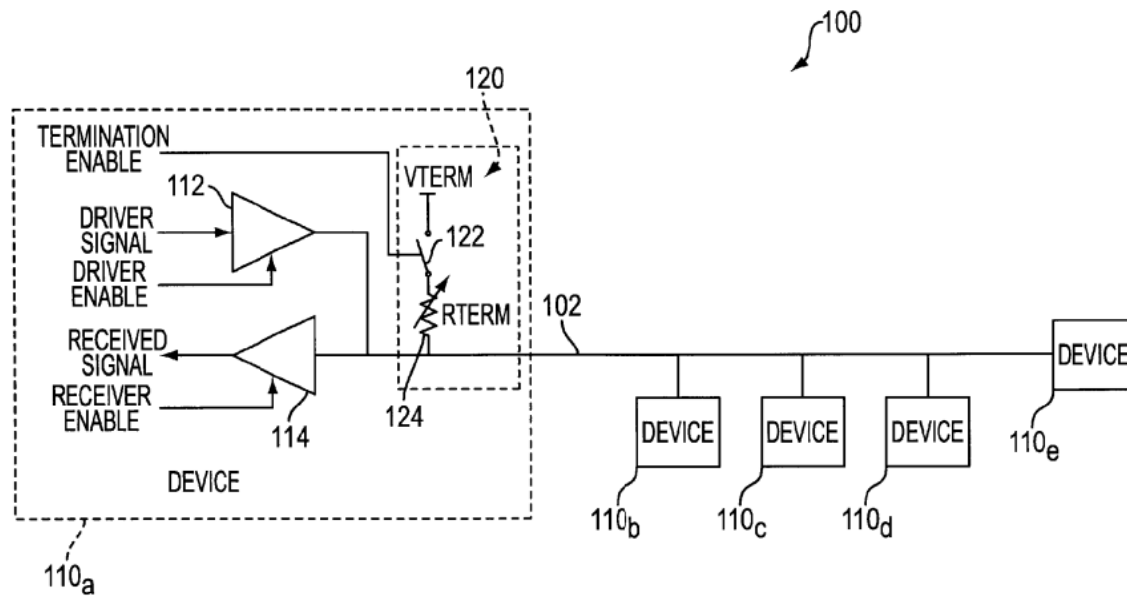


FIG. 1

Figure 1 of Greeff shows multidrop system 100 with devices 110a through 110e. Ex. 1006, 3:24–27. Each device includes transmitting driver 112 for driving a driver signal on bus 102. *Id.* at 3:48–49. Each device also includes receiving driver 114 for receiving a received signal from bus 102. *Id.* at 3:56–58. Additionally, each device includes active termination circuit 120, which “includes a switch 122 connected between a ‘trimmable’ termination resistor 124, having a trimmable termination resistance R_{TERM} , and reference voltage V_{TERM} .” *Id.* at 3:65–4:3.

The values of the termination resistance and reference voltage are selected to provide substantially optimal termination of bus 102. Ex. 1006, 7:54–58. These values can be selected during a calibration after system 100 has been configured and before its first use. *Id.* at 7:58–60. These values also can be adjusted while system 100 is operating. *Id.* at 7:61–64. For example, the termination resistance value can be calibrated for process, voltage, or temperature variations. *Id.* at 7:66–8:3.

2. Analysis

Turning now to the claims, we start with independent claim 17.

a. Independent Claim 17

Claim 17 is directed to a system and recites various limitations that Petitioner designates as limitations 17a through 17g. We address these limitations in turn.

i. Limitation 17a: “circuitry to store an existing value”

Claim 17 recites “circuitry to store an existing value representative of at least one of a termination resistance and a driver strength to be applied in association with data communicated across a channel.” Petitioner designates this limitation as limitation 17a.

For the first part of limitation 17a (which recites “circuitry to store an existing value”), Petitioner cross-references its discussion of claim 10 for the challenge based on *Meaney*. *See* Pet. 57 (citing Pet. 30–31).⁷ In that discussion, Petitioner asserts that “*Meaney* discloses that the computer system includes clock calibrating hardware,” and that “a system assist processor (SAP) . . . uses a hardware interface protocol to read and write registers in the logic of the interface.” *Id.* at 30 (citing Ex. 1004 ¶¶ 15, 16, 20, 21, 23, 37). Petitioner contends that “[a] POSITA would have understood that the clock calibrating hardware would include circuitry and would at least temporarily store the existing value of the clock delay in order to perform the recalibration.” *Id.* at 30–31 (citing Ex. 1002, app. A at 38).

⁷ Petitioner cites section VIII.A.7.vi of the Petition, which corresponds to pages 30 through 31 of the Petition.

Petitioner also contends that “a POSITA would have understood that the SAP would write the clock delay into a register in the interface logic.” *Id.* at 31 (citing Ex. 1002, app. A at 38).

For the second part of limitation 17a (which requires the “existing value” to be “representative of at least one of a termination resistance and a driver strength to be applied in association with data communicated across a channel”), Petitioner cross-references its discussion of claims 4 and 5 for the challenge based on Meaney and Greeff. Pet. 57 (citing Pet. 54–56).⁸ In its discussion of claim 4, Petitioner provides an annotated version of Figure 1 of Greeff, reproduced below. Pet. 55.

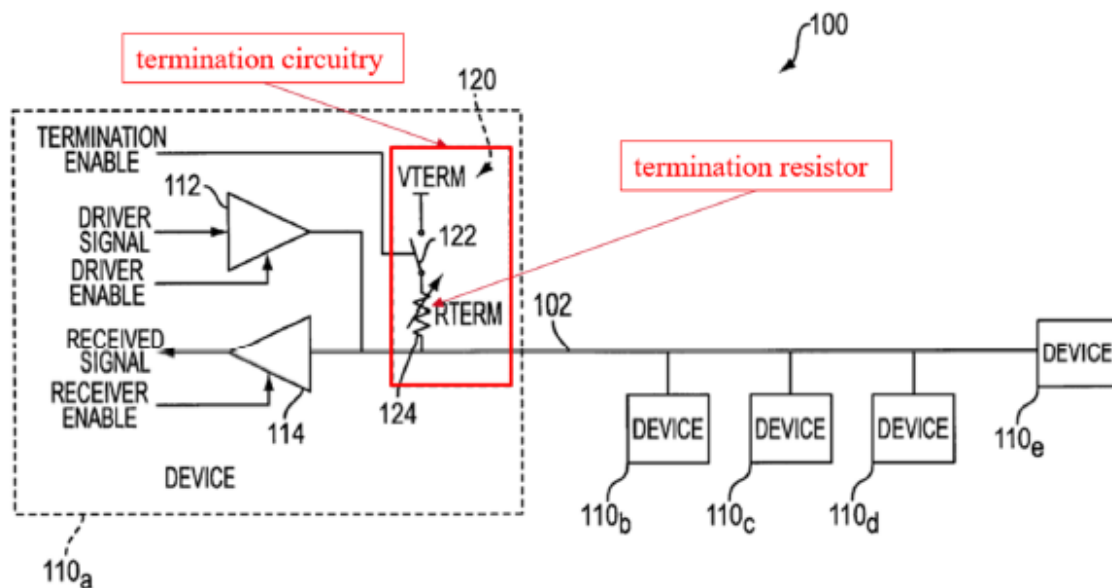


FIG. 1

Figure 1 of Greeff, as annotated by Petitioner, shows multidrop system 100 with devices 110a through 110e. *See* Ex. 1006, 3:24–27. Referring to the annotated figure, Petitioner asserts that “*Greeff* discloses a multidrop bus

⁸ Petitioner cites sections VIII.C.2 through VIII.C.3 of the Petition, which correspond to pages 54 through 56 of the Petition.

including circuitry capable of receiving a digital signal that includes termination circuitry 120 including a switch 122 connected between a ‘trimmable’ termination resistor 124, having a trimmable termination resistance R_{TERM} , and a reference voltage V_{TERM} .” Pet. 54 (citing Ex. 1006, 3:65–4:20, 5:59–6:6, 7:52–8:56, Fig. 1; Ex. 1002, app. A at 83). Petitioner adds, “*Greeff* explains that the termination resistance is modified during initial calibration and recalibration processes to provide a substantially optimal termination of the bus 102.” *Id.* at 55 (citing Ex. 1006, 4:11–20, 7:52–8:56; Ex. 1002, app. A at 83).

In its discussion of claim 5, Petitioner asserts that “*Greeff* discloses an active termination circuit 330 including circuitry capable of receiving a digital signal that uses transistors 331 and 335 as switches that enable or disable the active termination,” where “the drive strength of the transistors can be calibrated.” Pet. 55–56 (citing Ex. 1006, 6:40–55, 8:3–5, Fig. 3, claim 42; Ex. 1002, app. A at 84–85).

Petitioner contends that “[a] POSITA would have been motivated to incorporate the termination circuitry disclosed in *Greeff* with the system of *Meaney* to achieve enhanced system performance and reliability.” Pet. 53 (citing Ex. 1002, app. A at 82). As support, Petitioner asserts that “*Greeff*’s termination circuitry ensures proper signal integrity and reduces reflections in high-speed data transmission systems.” *Id.* (citing Ex. 1006, 1:28–31, 4:10–12, 8:3–5; Ex. 1002, app. A at 82). Petitioner further asserts that “*Meaney*’s calibration techniques, when applied to the termination resistance and transistor drive strength of *Greeff*, would ensure that these parameters remain optimal throughout system operation.” *Id.* (citing Ex. 1002, app. A at 82); *see also id.* at 54 (“A POSITA would have found it obvious to apply

Meaney's calibration process to *Greeff*'s termination circuitry in order to optimize the termination resistance and drive strength of the termination circuitry.”). Petitioner adds that “[a] POSITA would have had a reasonable expectation of success in combining *Meaney* and *Greeff*.” *Id.* at 54.

According to Petitioner, “[t]he integration of *Greeff*'s termination circuitry into *Meaney*'s system would have been straightforward and cost-effective,” any “required modifications are minimal, and the results of the combination are predictable, given the complementary nature of the technologies.” *Id.* (citing Ex. 1002, app. A at 82).

Patent Owner does not dispute Petitioner's analysis for this limitation. *See* Prelim. Resp. Based on Petitioner's argument and evidence, we are persuaded that Petitioner has shown sufficiently for purposes of this Decision that its proposed combination of *Meaney* and *Greeff* teaches or suggests the recited “circuitry” of limitation 17a. We also are persuaded that Petitioner's proffered reasoning for modifying *Meaney*'s system to include *Greeff*'s termination circuitry, namely, to ensure proper signal integrity and reduce reflections, is sufficient to support institution. *See In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (“[T]here must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.”).

ii. Limitations 17b through 17g

The rest of claim 17 recites similar limitations as claims 1 and 10, including “wherein the second calibration is constrained to be performed during a time period that is shorter than a time period of the first calibration.” For these similarly recited limitations, the parties rely

primarily on their discussion of claims 1 and 10 for the challenge based on Meaney. Pet. 58–62; Prelim. Resp. 14–15; *see also* Pet. 58–62 (also relying on Greeff). We disagree with Patent Owner’s arguments for the reasons explained above. *See supra* Part III.C.2.a.vi. On the record before us, and for the reasons given above regarding claims 1 and 10, as well as limitation 17a of claim 17, we are persuaded that Petitioner’s showing for limitations 17b through 17g is sufficient for purposes of this Decision.

b. Dependent Claims 4, 5, 13, 14, 18, and 19

Claims 4, 5, 13, 14, 18, and 19 depend from claims 1, 10, or 17. Patent Owner does not separately dispute Petitioner’s analysis for these dependent claims. Having reviewed Petitioner’s arguments and evidence for these claims, we are persuaded that Petitioner’s showing for claims 4, 5, 13, 14, 18, and 19 is sufficient for purposes of this Decision. *See* Pet. 54–57, 62–64.

3. Summary

In view of the foregoing, we determine that Petitioner has demonstrated a reasonable likelihood of showing that claims 4, 5, 13, 14, and 17–19 would have been obvious over Meaney and Greeff.

E. Remaining Challenges

Petitioner asserts four additional challenges. Specifically, Petitioner asserts that claims 1, 2, 6–12, 15, and 16 would have been obvious over Meaney and Nguyen. Pet. 37–52. Petitioner asserts that claims 4, 5, 13, 14, and 17–19 would have been obvious over Meaney, Nguyen, and Greeff. *Id.*

at 52–64. Petitioner asserts that claim 3 would have been obvious over Meaney and Allee. *Id.* at 67–69. Lastly, Petitioner asserts that claim 3 also would have been obvious over Meaney, Nguyen, and Allee. *Id.* at 69.

As discussed above, Petitioner has already demonstrated a reasonable likelihood that it will prevail on its asserted challenge based on Meaney as well as its asserted challenge based on Meaney and Greeff. *See supra* Parts III.C, III.D. Accordingly, we do not address Petitioner’s four additional asserted challenges based on various combinations of Meaney, Nguyen, Greeff, and Allee. *See SAS Inst. Inc. v. Iancu*, 584 U.S. 357, 359 (2018) (“The agency cannot curate the claims at issue but must decide them all.”); 37 C.F.R. § 42.108(a) (“When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.”). We note that Patent Owner does not present arguments directed to any claim or challenge that this Decision does not address.

IV. CONCLUSION

For the foregoing reasons, we institute *inter partes* review of all challenged claims based on all asserted challenges in the Petition. *See SAS*, 584 U.S. at 359; 37 C.F.R. § 42.108(a). At this stage of the proceeding, we have not made a final determination with respect to the patentability of any of the challenged claims or the construction of any claim term.

V. ORDER

For the reasons given, it is

ORDERED that *inter partes* review is instituted as to all challenged claims of the '466 patent, namely, claims 1–19, based on all challenges presented in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this Decision.

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