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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/230,558	03/31/2014	Scott C. Best	

44429
Peninsula Patent Group (Rambus)
203 Woodrow Ave.
Santa Cruz, CA 95060

CONFIRMATION NO. 9057
POWER OF ATTORNEY NOTICE



Date Mailed: 07/21/2016

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/15/2016.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/rmtturner myles/



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/230,558	03/31/2014	Scott C. Best	

69090
RAMBUS INC.
C/O Ann Williams
1050 Enterprise Way, Suite 700
Sunnyvale, CA 94089

CONFIRMATION NO. 9057
POA ACCEPTANCE LETTER



Date Mailed: 07/21/2016

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/15/2016.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/rmtturner myles/

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number

Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)



I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

69090

OR



I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:



The address associated with the above-mentioned Customer Number

OR



The address associated with Customer Number:

OR

Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Rambus Inc.



Inventor or Joint Inventor (title not required below)



Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)



Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)



Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

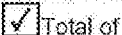
Name

Christopher P. Kosh

Title

Associate General Counsel for IP, Rambus Inc.

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.



Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office; U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: Scott C. BestApplication No./Patent No.: 9,111,608Filed/Issue Date: August 18, 2015Titled: STROBE-OFFSET CONTROL CIRCUITRambus Inc., a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 015725, Frame 0507, or for which a copy thereof is attached.
- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:
1. From: _____ To: _____
- The document was recorded in the United States Patent and Trademark Office at
- Reel _____, Frame _____, or for which a copy thereof is attached.
2. From: _____ To: _____
- The document was recorded in the United States Patent and Trademark Office at
- Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.☐ Additional documents in the chain of title are listed on a supplemental sheet(s).☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Lance M. Kreisman/

Signature

Lance M. Kreisman

Printed or Typed Name

July 15, 2016

Date

39,256

Title or Registration Number

[Page 2 of 2]

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**CHANGE OF
CORRESPONDENCE ADDRESS
Patent**Address to:
Mail Stop Post Issue
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Patent Number	9,111,608
Issue Date	August 18, 2015
Application Number	14/230,558
Filing Date	March 31, 2014
First Named Inventor	Scott C. Best
Attorney Docket Number	RBS2.P005C5

Please change the Correspondence Address for the above-identified patent to:



The address associated with Customer Number:

69090

OR**Firm or
Individual Name****Address****City****State****ZIP****Country****Telephone****Email**

This form cannot be used to change the data associated with a Customer Number. To change the data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB/124).

This form will not affect any "fee address" provided for the above-identified patent. To change a "fee address" use the "Fee Address Indication Form" (PTO/SB/47).

I am the:



Patentee.



If the Patentee was not the applicant for patent (37 CFR 1.42), then a Statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is enclosed or was filed on _____. See 37 CFR 3.71.

Attorney or agent of record. Registration Number 39,256.Patent practitioner acting in a representative capacity whose correspondence address is the correspondence address of record. Notice has been given to the patentee or owner. Registration Number 39,256.

Signature /Lance M. Kreisman/

Typed or
Printed Name Lance M. Kreisman

Date July 15, 2016

Telephone 650-468-9654

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.



*Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Post Issue, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	26368948
Application Number:	14230558
International Application Number:	
Confirmation Number:	9057
Title of Invention:	STROBE-OFFSET CONTROL CIRCUIT
First Named Inventor/Applicant Name:	Scott C. Best
Customer Number:	44429
Filer:	Lance Martel Kreisman
Filer Authorized By:	
Attorney Docket Number:	RBS2.P005C5 (RA356.C1C1C1
Receipt Date:	15-JUL-2016
Filing Date:	31-MAR-2014
Time Stamp:	19:36:38
Application Type:	Utility under 35 USC 111(a)

Payment information:					
Submitted with Payment			no		
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	POA_69090_CK.PDF	395518	no	1
			0d6571c9b4b50351d653ea8d7ee96b802167d7fd		
Warnings:			Silicon Motion Inc. Ex. 1002, Page 9 Silicon Motion Inc. v. K.Mizra LLC, IPR2024-01241		

Information:					
2	Assignee showing of ownership per 37 CFR 3.73	RA356_RBS2_P005C5_373_CC A.pdf	118073	no	3
			7b261d155299d4317e45972f9863c369452 268cf		
Warnings:					
Information:					
3	Change of Address	RBS2_P005c5_sb0123_AIA.pdf	236142	no	2
			efa1e47dbac22eb9f1202ab18b57136c0fe7 4944		
Warnings:					
Information:					
Total Files Size (in bytes):			749733		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/230,558	08/18/2015	9111608	RBS2.P005C5 (RA356.C1C1C1	9057

44429 7590 07/29/2015
Lance M. Kreisman
Peninsula Patent Group (Rambus)
606 Lincoln Ave.
Los Altos, CA 94022

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Scott C. Best, Palo Alto, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

44429 7590 04/16/2015
Lance M. Kreisman
Peninsula Patent Group (Rambus)
606 Lincoln Ave.
Los Altos, CA 94022

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
Filed via EFS-Web (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/230,558	03/31/2014	Scott C. Best	RBS2.P005C5 (RA356.C1C1C1)	9057

TITLE OF INVENTION: STROBE-OFFSET CONTROL CIRCUIT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	07/16/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
BARBEE, MANUEL L	2864	702-106000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Lance Kreisman
2 Peninsula Patent
3 Group

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Rambus Inc.

Sunnyvale, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☒ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Lance M. Kreisman/

Date July 10, 2015

Typed or printed name Lance M. Kreisman

Registration No. 39,256

Electronic Patent Application Fee Transmittal				
Application Number:		14230558		
Filing Date:		31-Mar-2014		
Title of Invention:		STROBE-OFFSET CONTROL CIRCUIT		
First Named Inventor/Applicant Name:		Scott C. Best		
Filer:		Lance Martel Kreisman		
Attorney Docket Number:		RBS2.P005C5 (RA356.C1C1C1		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt

EFS ID:	22887510
Application Number:	14230558
International Application Number:	
Confirmation Number:	9057
Title of Invention:	STROBE-OFFSET CONTROL CIRCUIT
First Named Inventor/Applicant Name:	Scott C. Best
Customer Number:	44429
Filer:	Lance Martel Kreisman
Filer Authorized By:	
Attorney Docket Number:	RBS2.P005C5 (RA356.C1C1C1
Receipt Date:	10-JUL-2015
Filing Date:	31-MAR-2014
Time Stamp:	16:48:56
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$960
RAM confirmation Number	3455
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	RBS2_P005C5_Iss_Fee_Xmtl.pdf	187792	no	1
			1b67d0fb7d4a98bff29c07f97cf02d29419d0843		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30418	no	2
			79aa7f2350de2b4992130c6418c0d2e8924a2c09		
Warnings:					
Information:					
Total Files Size (in bytes):			218210		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

44429 7590 04/16/2015
Lance M. Kreisman
Peninsula Patent Group (Rambus)
606 Lincoln Ave.
Los Altos, CA 94022

EXAMINER

BARBEE, MANUEL L

ART UNIT

PAPER NUMBER

2864

DATE MAILED: 04/16/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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14/230,558

03/31/2014

Scott C. Best

RBS2.P005C5
(RA356.C1C1C1)

9057

TITLE OF INVENTION: STROBE-OFFSET CONTROL CIRCUIT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	07/16/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

44429 7590 04/16/2015
Lance M. Kreisman
Peninsula Patent Group (Rambus)
606 Lincoln Ave.
Los Altos, CA 94022

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/230,558	03/31/2014	Scott C. Best	RBS2.P005C5 (RA356.C1C1C1)	9057

TITLE OF INVENTION: STROBE-OFFSET CONTROL CIRCUIT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	07/16/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
BARBEE, MANUEL L	2864	702-106000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/230,558	03/31/2014	Scott C. Best	RBS2.P005C5 (RA356.C1C1C1)	9057
44429	7590	04/16/2015	EXAMINER BARBEE, MANUEL L	
Lance M. Kreisman Peninsula Patent Group (Rambus) 606 Lincoln Ave. Los Altos, CA 94022			ART UNIT 2864	PAPER NUMBER

DATE MAILED: 04/16/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/230,558	Applicant(s) BEST, SCOTT C.	
	Examiner MANUEL L. BARBEE	Art Unit 2864	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to papers filed May 7, 2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. ☒ Notice of References Cited (PTO-892) | 5. ☐ Examiner's Amendment/Comment |
| 2. ☒ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date <u>5/7/14</u> | 6. ☒ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other _____. |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. | |

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Allowable Subject Matter

2. Claims 1-20 are allowed.
3. The following is an examiner's statement of reasons for allowance: The primary reason for the allowance of claims 1-15 is because the cited prior art does not teach an integrated circuit (IC) memory controller or method of operation in an IC controller that includes receiving a first and second data signal at a first and second data pin and a first and second adjustable delay element to delay the first and second delayed data signal. The primary reason for the allowance of claims 16-20 is because the cited prior art does not teach a Field Programmable Gate Array device that includes calibration circuitry to determine delay values corresponding to delays to impart for each data pin a received data signal to align the data signals with a strobe signal for data sampling operations, each pin associated with a given delay value.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent No. 6,707,723 to Jeong teaches data input circuits that include a delay element for the data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MANUEL L. BARBEE whose telephone number is (571)272-2212. The examiner can normally be reached on Monday-Friday from 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Breene can be reached on 571-272-4107. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MANUEL L. BARBEE/
Primary Examiner, Art Unit 2864
April 5, 2015

Notice of References Cited	Application/Control No. 14/230,558		Applicant(s)/Patent Under Reexamination BEST, SCOTT C.	
	Examiner MANUEL L. BARBEE		Art Unit 2864	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,707,723 B2	03-2004	Jeong, Woo-Seop	365/189.05
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Issue Classification 	Application/Control No. 14230558	Applicant(s)/Patent Under Reexamination BEST, SCOTT C.
	Examiner MANUEL L BARBEE	Art Unit 2864

CPC						
Symbol					Type	Version
G11C		7		222	F	2013-01-01
G06F		13		1689	I	2013-01-01
						
						
						
						
						
						
						
						
						
						
						
						
						

CPC Combination Sets						
Symbol			Type	Set	Ranking	Version
						
						

NONE		Total Claims Allowed: 20	
(Assistant Examiner)	(Date)	O.G. Print Claim(s)	O.G. Print Figure
/MANUEL L BARBEE/ Primary Examiner.Art Unit 2864	4/5/15	1	1
(Primary Examiner)	(Date)		

Issue Classification 	Application/Control No. 14230558	Applicant(s)/Patent Under Reexamination BEST, SCOTT C.
	Examiner MANUEL L BARBEE	Art Unit 2864

☐ Claims renumbered in the same order as presented by applicant															
☐ CPA															
☐ T.D.															
☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17												
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15	15														
16	16														

NONE	Total Claims Allowed: 20	
(Assistant Examiner)	(Date)	
/MANUEL L BARBEE/ Primary Examiner.Art Unit 2864	4/5/15	O.G. Print Claim(s) 1
(Primary Examiner)	(Date)	O.G. Print Figure 1

<i>Index of Claims</i> 	Application/Control No. 14230558	Applicant(s)/Patent Under Reexamination BEST, SCOTT C.
	Examiner MANUEL L BARBEE	Art Unit 2864

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant											☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE														
Final	Original	04/05/2015														
1	1	=														
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3	3	=														
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BIB DATA SHEET

CONFIRMATION NO. 9057

SERIAL NUMBER 14/230,558	FILING or 371(c) DATE 03/31/2014 RULE	CLASS 702	GROUP ART UNIT 2864	ATTORNEY DOCKET NO. RBS2.P005C5 (RA356.C1C1C1)		
APPLICANTS INVENTORS Scott C. Best, Palo Alto, CA; ** CONTINUING DATA ***** This application is a CON of 13/656,238 10/19/2012 PAT 8688399 which is a CON of 13/276,708 10/19/2011 PAT 8311761 which is a CON of 12/694,251 01/26/2010 PAT 8135555 which is a CON of 11/621,491 01/09/2007 PAT 7668679 which is a CON of 10/923,421 08/20/2004 PAT 7171321 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 04/21/2014						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/MANUEL L BARBEE/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 13	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS Lance M. Kreisman Peninsula Patent Group (Rambus) 606 Lincoln Ave. Los Altos, CA 94022 UNITED STATES						
TITLE STROBE-OFFSET CONTROL CIRCUIT						
FILING FEE RECEIVED 1740	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	7189	G11C7/222.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 07:33
L2	3459	G11C7/10.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 07:55
L3	13890	G11C7/22.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 08:03
L4	2670	G11C7/22.cpc. and delay and strobe	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 08:03
L5	3278	G11C7/106.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 08:13
L6	4965	G11C7/1066.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 08:26
L8	287	G11C11/407.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 08:38
L9	6632	G11C11/4076.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 08:39
L10	731	G11C11/409.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 08:54
L11	2460	G11C11/4093.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 08:56

L12	2582	G06F13/1689.qpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 09:04
L13	5188	H03L7/0814.qpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 09:14
S6	1172	(702/71,72,79).CCLS.	US-PGPUB; USPAT	OR	OFF	2015/04/05 02:35
S7	1961	(702/85,89).CCLS.	US-PGPUB; USPAT	OR	OFF	2015/04/05 02:35
S8	961	(702/106,107).CCLS.	US-PGPUB; USPAT	OR	OFF	2015/04/05 02:35
S9	275	365/189.07 and (calibration calibrate calibrating calibrated)	US-PGPUB; USPAT	OR	ON	2015/04/05 02:35
S10	1796	(365/193).CCLS.	US-PGPUB; USPAT	OR	OFF	2015/04/05 02:35
S11	317	365/194.ccls. and (calibration calibrate calibrating calibrated)	US-PGPUB; USPAT	OR	ON	2015/04/05 02:35
S12	1659	365/194.ccls. and synchroniz\$5 with (strobe sample clock data delay phase)	US-PGPUB; USPAT	OR	ON	2015/04/05 02:35
S13	203	711/105.ccls. and (calibration calibrate calibrating calibrated)	US-PGPUB; USPAT	OR	ON	2015/04/05 02:35
S14	892	711/105.ccls. and synchroniz\$5	US-PGPUB; USPAT	OR	ON	2015/04/05 02:35
S15	134	711/105.ccls. and (offset delay phase) near control	US-PGPUB; USPAT	OR	ON	2015/04/05 02:35
S16	2831	(713/400).CCLS.	US-PGPUB; USPAT	OR	OFF	2015/04/05 02:35
S17	1263	(713/401).CCLS.	US-PGPUB; USPAT	OR	OFF	2015/04/05 02:35
S18	2913	(327/158).CCLS.	US-PGPUB; USPAT	OR	OFF	2015/04/05 02:35
S19	1347	(327/161).CCLS.	US-PGPUB; USPAT	OR	OFF	2015/04/05 02:35
S20	1101	(calibrat\$3 adjust\$3 synchroniz\$3) with (sample strobe clock) with (delay phase offset) and DQ and DQS and receiver	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 02:35
S21	1281	(calibrat\$3 adjust\$3) with (sample strobe clock) with (delay phase offset) and DQ and DQS and double adj data adj rate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 02:35
S22	692	(calibrat\$3 adjust\$3 synchroniz\$3) with (sample strobe clock) with (delay phase offset) and multiplexer with (strobe sample) with input	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 02:35
S23	95	memory adj controller and receiver with rising adj edge and receiver	US-PGPUB; USPAT; USOCR;	OR	ON	2015/04/05 02:35

		with falling adj edge	FPRS; EPO; JPO; DERWENT; IBM_TDB			
S24	185	double adj data adj rate and receiver with rising adj edge and receiver with falling adj edge	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 02:35
S25	109	phase adj difference with (sample strobe) adj signal with data adj signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 02:35
S26	841	(delay offset) with (sample strobe) adj signal with data adj signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/05 02:35

EAST Search History (I nterference)

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<div>Substitute for form 1449/PTO</div> <div>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</div> <div>(Use as many sheets as necessary)</div>		Complete if Known	
		Application Number	14/230,558
		Filing Date	31 March 2014
		First Named Inventor	Scott C. Best
		Art Unit	2827
		Examiner Name	
Sheet 1 of 6	Attorney Docket Number	RA356.C1C1C1C1C1.US (RBS2.P005C5)	

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	1	US- 4410916	10-18-1983	Pratt et al.	Entire Document
	2	US- 4687954	08-18-1987	Yasuda et al.	Entire Document
	3	US- 4926447	05-15-1990	Corsetto et al.	Entire Document
	4	US- 5060239	10-22-1991	Briscoe et al.	Entire Document
	5	US- 5334883	08-02-1994	Rosenthal, Bruce D.	Entire Document
	6	US- 5341371	08-23-1994	Simpson, Robert J.	Entire Document
	7	US- 5655105	08-05-1997	McLaury, Loren L.	Entire Document
	8	US- 5805619	09-08-1998	Gardner et al.	Entire Document
	9	US- 5832303	11-03-1998	Murase et al.	Entire Document
	10	US- 5935257	08-10-1999	Nishimura, Koichi	Entire Document
	11	US- 5948083	09-07-1999	Gervasi, William M.	Entire Document
	12	US- 5978281	11-02-1999	Anand et al.	Entire Document
	13	US- 6023174	02-08-2000	Kirsch, Howard Clayton	Entire Document
	14	US- 6028816	02-22-2000	Takemae et al.	Entire Document
	15	US- 6055587	04-25-2000	Asami et al.	Entire Document
	16	US- 6279073-B1	08-21-2001	McCracken et al.	Entire Document
	17	US- 6316980-B1	11-13-2001	Vogt et al.	Entire Document
	18	US- 6396887	05-28-2002	Ware et al.	Entire Document
	19	US- 6498766	12-24-2002	Lee et al.	Entire Document

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		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
	1	DE-19920335-C1	09-07-2000	Hofmann et al.	Entire Document	✓
	2	WO-98/44674-A1	10-08-1998	Stallmann et al.	Entire Document	
	3	WO-99/17183-A1	04-08-1999	Gervasi, Williams S.	Entire Document	

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		Examiner Name	
Sheet 2 of 6	Attorney Docket Number	RA356.C1C1C1C1C1.US (RBS2.P005C5)	

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	20	US- 6512704	01-28-2003	Wu et al.	Entire Document
	21	US- 6570800	05-27-2003	Tanaka et al.	Entire Document
	22	US- 6570944	05-27-2003	Best et al.	Entire Document
	23	US- 6643787-B1	11-04-2003	Zerbe et al.	Entire Document
	24	US- 6646929-B1	11-11-2003	Moss et al.	Entire Document
	25	US- 6646953-B1	11-11-2003	Stark, Donald C.	Entire Document
	26	US- 6675272-B2	01-06-2004	Ware et al.	Entire Document
	27	US- 6691214	02-10-2004	Li et al.	Entire Document
	28	US- 6707723	03-16-2004	Jeong, Woo-Seop	Entire Document
	29	US- 6735709-B1	05-11-2004	Lee et al.	Entire Document
	30	US- 6759881	07-06-2004	Kizer et al.	Entire Document
	31	US- 6782459	08-24-2004	Ware, Frederick A.	Entire Document
	32	US- 6819157	11-16-2004	Cao et al.	Entire Document
	33	US- 6836503	12-28-2004	Best et al.	Entire Document
	34	US- 6836521	12-28-2004	Ware et al.	Entire Document
	35	US- 6889334	05-03-2005	Magro et al.	Entire Document
	36	US- 6898682	05-24-2005	Wekler et al.	Entire Document
	37	US- 6930932	08-16-2005	Rentschler, Eric McCutcheon	Entire Document
	38	US- 6940760	09-06-2005	Borkenhagen et al.	Entire Document

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		First Named Inventor	Scott C. Best
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Sheet 3 of 6	Attorney Docket Number	RA356.C1C1C1C1C1.US (RBS2.P005C5)	

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	39	US- 6940768	09-06-2005	Dahlberg et al.	Entire Document
	40	US- 6941433	09-06-2005	Libby et al.	Entire Document
	41	US- 7031205	04-18-2006	Han et al.	Entire Document
	42	US- 7107424	09-12-2006	Avakian et al.	Entire Document
	43	US- 7259606	08-21-2007	Ku et al.	Entire Document
	44	US- 6466491-B2	10-15-2002	Yanagawa, Miki	Entire Document
	45	US- 2001-0020278	09-06-2001	Saito, Tatsuya	Entire Document
	46	US- 2001-0032067	10-18-2001	Nemani et al.	Entire Document
	47	US- 2002-0009004-A1	01-24-2002	Hamada et al.	Entire Document
	48	US- 2002-0021616	02-21-2002	Keeth et al.	Entire Document
	49	US- 2002-0149397-A1	10-17-2002	Dally et al.	Entire Document
	50	US- 2002-0196883	12-26-2002	Best et al.	Entire Document
	51	US- 2003-0065465-A1	04-03-2003	Johnson et al.	Entire Document
	52	US- 2003-0081707	05-01-2003	Takeuchi et al.	Entire Document
	53	US- 2003-0091136-A1	05-15-2003	Sugita, Natsuki	Entire Document
	54	US- 2003-0179611	09-25-2003	Liou, Ming-Shi	Entire Document
	55	US- 2003-0218504	11-27-2003	Nguyen et al.	Entire Document
	56	US- 2003-0221050	11-27-2003	Hong et al.	Entire Document
	57	US- 2004-0044919	03-04-2004	Dabral, Sanjay	Entire Document

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STATEMENT BY APPLICANT

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Sheet 4 of 6

Complete if Known

Application Number

14/230,558

Filing Date

31 March 2014

First Named Inventor

Scott C. Best

Art Unit

2827

Examiner Name

Attorney Docket Number

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	58	US- 2004-0068682	04-08-2004	Takei et al.	Entire Document
	59	US- 2004-0084537	05-06-2004	Best, Scott C.	Entire Document
	60	US- 2004-0213067	10-28-2004	Best et al.	Entire Document
	61	US- 2004-0230715	11-18-2004	Huang, Hsilin	Entire Document
	62	US- 2005-0005056	01-06-2005	Ware, Frederick A.	Entire Document
	63	US- 2005-0071707	03-31-2005	Hampel, Craig E.	Entire Document
	64	US- 2005-0110544-A1	05-26-2005	Suda et al.	Entire Document
	65	US- 2005-0141294	06-30-2005	Bonelli, Andrea	Entire Document
	66	US- 2005-0163203	07-28-2005	Ware et al.	Entire Document
	67	US- 2012-0170389-A1	07-05-2012	Kizer et al.	Entire Document
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known			
		Application Number	14/230,558		
		Filing Date	31 March 2014		
		First Named Inventor	Scott C. Best		
		Art Unit	2827		
		Examiner Name			
Sheet	5	of	6	Attorney Docket Number	RA356.C1C1C1C1C1.US (RBS2.P005C5)

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	1	Integrated Device Technology, Inc., "CMOS Parallel-to-Serial FIFO: 256x16, 512x16, 1024x16," December 1999, Retrieved from http://www.digchip.com/datasheets/parts/datasheet/222/IDT72105.php . 10 pages	
	2	FIND, "DDR-SDRAM-2: Detailed Specifications," November 1998, FIND, Vol. 16, No. 4. 14 pages	
	3	FIND, "DDR-SDRAM-4: DLL Circuit Technology," November 1998, FIND, Vol. 16, No. 4. 4 pages	
	4	Texas Instruments, "SN74ALVC7804 512x18 First-In, First-Out Memory," SCAS432-January 1995, Retrieved from http://focus.ti.com/lit/ds/symlink/sn74alvc7804.pdf . 13 pages	
	5	Dallas Semiconductor, "Tech Brief 31: Using Delay Lines to Generate Multi-Phased Clocks," December 11, 2001, Retrieved from http://www.maximic.com/appnotes.cfm/appnote_number/880 . 1 page	
	6	CHAKRABORTY, Ajanta, "Efficient Self-Timed Interfaces for Crossing Clock Domains," August 2003, Thesis Submitted to the Department of Computer Science, University of British Columbia. 74 pages	
	7	Altera Corporation, "Using Source-Synchronous Signaling with DPA in Stratix GX Devices," Application Note 236, January 2003, Ver. 1.1, Retrieved from http://www.altera.com/literature/an/an236.pdf . 18 pages	
	8	COLLINS et al., "DDR-SDRAM, High-Speed, Source-Synchronous Interfaces Create Design Challenges," September 2, 1999, EDN Access, Retrieved from http://www.ednmag/reg/1999/090299/18ms544.htm . 15 pages	
	9	HOROWITZ, Hill, "The Art of Electronics" Second Edition, 1989, Cambridge, pp. 231-232. 2 pages	
	10	IBM Corporation, "PowerPC Embedded Processors: PowerPC 440GP - DDR SDRAM Controller Initialization," Application Note, March 20, 2002. 8 pages	

Examiner Signature		Date Considered	
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		Examiner Name			
Sheet	6	of	6	Attorney Docket Number	RA356.C1C1C1C1C1.US (RBS2.P005C5)

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	11	International Preliminary Report on Patentability dated March 1, 2007 in International Application No. PCT/US2005/028709. 13 pages	
	12	International Search Report and Written Opinion dated January 19, 2006 in International Application No. PCT/US2005/028709. 19 pages	
	13	International Search Report and Written Opinion dated July 7, 2006 in International Application No. PCT/US2006/008610. 12 pages	
	14	International Search Report and Written Opinion dated December 5, 2007 in International Application No. PCT/US2007/063780. 14 pages	
	15	MUTTERSBACH et al., "Practical Design of Globally-Asynchronous Locally-Synchronous Systems," Sixth International Symposium on Advanced Research in Asynchronous Circuits and Systems, 2000. 8 pages	
	16	KHATIB, Jamil, "FIFO, First-In First-Out Memory," March 28, 1999, Retrieved from http://www.geocities.com/Silicon Valley/Pines/6639/ip/fifo.html . 6 pages	
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	18	RYAN, Kevin, "DDR SDRAM Functionality and Controller Read Data Capture," 1999, Micron Technology, Inc., DesignLine Vol. 8, Issue 3. 24 pages	
	19	SCHUMANN et al., "An Asynchronous up/down Counter for Control of a Self-timed, Wave-pipelined Array Multiplier," ACiD-WL Workshop, Groningen, the Netherlands, September 1996, Retrieved from http://mikro.ee.tuberlin.de/forschung/sgemos/abstractACiD.ps.gz . 1 page	
	20	XILINX, "Using the XC9500 Timing Model," Application Note, XAPP071, January 1997, Version 1.0, pp. 2-9 to 2-12, Retrieved from http://direct.xilinx.com/bvdocs/appnotes/xapp071.pdf . 4 pages	

Examiner Signature	/Manuel L. Barbee/	Date Considered	04/05/2015
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
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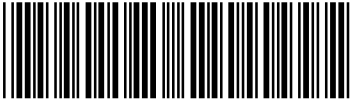
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Search Notes 	Application/Control No. 14230558	Applicant(s)/Patent Under Reexamination BEST, SCOTT C.
	Examiner MANUEL L BARBEE	Art Unit 2864

CPC- SEARCHED		
Symbol	Date	Examiner
G11C 7/222, 10, 106, 1066	4/5/15	mlb
G11C 11/407, 4076k, 409, 4093	4/5/15	mlb
G06F 13/1689	4/5/15	mlb
H03L 7/0814	4/5/15	mlb

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
EAST text search	4/5/15	mlb

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	Text search only. See search history.	4/5/15	mlb

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/230,558	03/31/2014	Scott C. Best	RBS2.P005C5 (RA356.C1C1C1)

CONFIRMATION NO. 9057

PUBLICATION NOTICE



OC000000070185266

44429
Lance M. Kreisman
Peninsula Patent Group (Rambus)
606 Lincoln Ave.
Los Altos, CA 94022

Title:STROBE-OFFSET CONTROL CIRCUIT

Publication No.US-2014-0226420-A1

Publication Date:08/14/2014

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 14/230,558	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(j))	20	minus 20 = *			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	1600
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	OR	x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	OR	x =
	Application Size Fee (37 CFR 1.16(s))					OR	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					OR	
				TOTAL ADD'L FEE		TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	OR	x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	OR	x =
	Application Size Fee (37 CFR 1.16(s))					OR	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					OR	
				TOTAL ADD'L FEE		TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
14/230,558	03/31/2014	2827	1740	RBS2.P005C5 (RA356.C1C1C1	20	3

CONFIRMATION NO. 9057

UPDATED FILING RECEIPT



44429

Lance M. Kreisman
Peninsula Patent Group (Rambus)
606 Lincoln Ave.
Los Altos, CA 94022

Date Mailed: 05/07/2014

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Inventor(s)

Scott C. Best, Palo Alto, CA;

Applicant(s)

Scott C. Best, Palo Alto, CA;

Assignment For Published Patent Application

Rambus Inc., Sunnyvale, CA

Power of Attorney: The patent practitioners associated with Customer Number 44429

Domestic Priority data as claimed by applicant

This application is a CON of 13/656,238 10/19/2012 PAT 8688399
which is a CON of 13/276,708 10/19/2011 PAT 8311761
which is a CON of 12/694,251 01/26/2010 PAT 8135555
which is a CON of 11/621,491 01/09/2007 PAT 7668679
which is a CON of 10/923,421 08/20/2004 PAT 7171321

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Projected Publication Date: 08/14/2014

Non-Publication Request: No

Early Publication Request: No
Title

STROBE-OFFSET CONTROL CIRCUIT

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1

of 6

Complete if Known

Application Number	14/230,558
Filing Date	31 March 2014
First Named Inventor	Scott C. Best
Art Unit	2827
Examiner Name	
Attorney Docket Number	RA356.C1C1C1C1C1.US (RBS2.P005C5)

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	1	US- 4410916	10-18-1983	Pratt et al.	Entire Document
	2	US- 4687954	08-18-1987	Yasuda et al.	Entire Document
	3	US- 4926447	05-15-1990	Corsetto et al.	Entire Document
	4	US- 5060239	10-22-1991	Briscoe et al.	Entire Document
	5	US- 5334883	08-02-1994	Rosenthal, Bruce D.	Entire Document
	6	US- 5341371	08-23-1994	Simpson, Robert J.	Entire Document
	7	US- 5655105	08-05-1997	McLaury, Loren L.	Entire Document
	8	US- 5805619	09-08-1998	Gardner et al.	Entire Document
	9	US- 5832303	11-03-1998	Murase et al.	Entire Document
	10	US- 5935257	08-10-1999	Nishimura, Koichi	Entire Document
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		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
	1	DE-19920335-C1	09-07-2000	Hofmann et al.	Entire Document	✓
	2	WO-98/44674-A1	10-08-1998	Stallmann et al.	Entire Document	
	3	WO-99/17183-A1	04-08-1999	Gervasi, Williams S.	Entire Document	

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Sheet **2**of **6****Complete if Known**

Application Number	14/230,558
Filing Date	31 March 2014
First Named Inventor	Scott C. Best
Art Unit	2827
Examiner Name	
Attorney Docket Number	RA356.C1C1C1C1C1.US (RBS2.P005C5)

U. S. PATENT DOCUMENTS

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	20	US- 6512704	01-28-2003	Wu et al.	Entire Document
	21	US- 6570800	05-27-2003	Tanaka et al.	Entire Document
	22	US- 6570944	05-27-2003	Best et al.	Entire Document
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**INFORMATION DISCLOSURE
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Sheet **3**of **6****Complete if Known**

Application Number	14/230,558
Filing Date	31 March 2014
First Named Inventor	Scott C. Best
Art Unit	2827
Examiner Name	
Attorney Docket Number	RA356.C1C1C1C1C1.US (RBS2.P005C5)

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	39	US- 6940768	09-06-2005	Dahlberg et al.	Entire Document
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Sheet 4

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Application Number	14/230,558
Filing Date	31 March 2014
First Named Inventor	Scott C. Best
Art Unit	2827
Examiner Name	
Attorney Docket Number	RA356.C1C1C1C1C1.US (RBS2.P005C5)

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Attorney Docket Number	RA356.C1C1C1C1C1.US (RBS2.P005C5)

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6

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	1	Integrated Device Technology, Inc., "CMOS Parallel-to-Serial FIFO: 256x16, 512x16, 1024x16," December 1999, Retrieved from http://www.digchip.com/datasheets/parts/datasheet/222/IDT72105.php . 10 pages	
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		Application Number	14/230,558		
		Filing Date	31 March 2014		
		First Named Inventor	Scott C. Best		
		Art Unit	2827		
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	11	International Preliminary Report on Patentability dated March 1, 2007 in International Application No. PCT/US2005/028709. 13 pages	
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EFS ID:	18964441
Application Number:	14230558
International Application Number:	
Confirmation Number:	9057
Title of Invention:	STROBE-OFFSET CONTROL CIRCUIT
First Named Inventor/Applicant Name:	Scott C. Best
Customer Number:	44429
Filer:	Jose Gabriel Moniz/Dorothy Levin
Filer Authorized By:	Jose Gabriel Moniz
Attorney Docket Number:	RBS2.P005C5 (RA356.C1C1C1
Receipt Date:	07-MAY-2014
Filing Date:	31-MAR-2014
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Application Type:	Utility under 35 USC 111(a)

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	RA356Transmittal.pdf	61660 18b95ad05d81cc7f8ee10cb470ea2e324e1e7b3a	no	3

Warnings:

Information:

2	Information Disclosure Statement (IDS) Form (SB08)	RA356IDS.pdf	1149320 4ecec84a14e95a8a2aa073f8f96fb5b2180b1fc	no	7
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
Total Files Size (in bytes):				1210980	
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor:	Scott C. Best
Application No.:	14/230,558
Filing Date:	31 March 2014
Title:	STROBE-OFFSET CONTROL CIRCUIT
Examiner:	Unknown
Group Art Unit:	2827
Confirmation No.:	9057
In-House Docket No.:	RA356.C1C1C1C1C1.US
Attorney Docket No.:	RBS2.P005C5

INFORMATION DISCLOSURE STATEMENT A
Under 37 CFR §§ 1.56 and 1.97-98

Pursuant to the provisions of 37 C.F.R. §§ 1.56 and 1.97-98, enclosed herewith is modified form PTO/SB/08A listing references for consideration by the Examiner.

The filing of this Information Disclosure Statement shall not be construed as a representation regarding the completeness of the list of references, or that inclusion of a reference in this list is an admission that it is prior art or is pertinent to this application, or that a search has been made, or as an admission that the information listed is, or may be considered to be, material to patentability, or that no other material information exists, and shall not be construed as an admission against interest in any manner.

This Information Disclosure Statement is being filed:

- ☒ within three months of the filing date of the application, or date of entry into the national stage of an international application, or before the mailing date of a first office action on the merits, whichever event last occurred;
- ☐ before the mailing of a first official action after the filing of a request for continued examination (RCE) under 37 C.F.R. § 1.114;
- ☐ after three months of the filing date of this national application or the date of entry of the national stage in an international application, or after the mailing date of the first official action on the merits, whichever event last

occurred, but before the mailing date of the first to occur of either: (1) a final action under 37 C.F.R. §1.113; or (2) an action that otherwise closes prosecution in the application, and:

- ☐ Authorization is hereby given to Charge Deposit Account No. 505066 for the fee of \$180.00 under 37 C.F.R. §1.17(p) for submission of this Information Disclosure Statement under 37 C.F.R. §1.97(c); OR
- ☐ Applicant certifies pursuant to 37 C.F.R. §1.97(e) that:
 - ☐ each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Statement; OR
 - ☐ no item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the person signing this certification after making reasonable inquiry, no item of information contained in this Statement was known to any individual designated under 37 C.F.R. §1.56(c) more than three months prior to the filing of this Statement;

- ☐ on or before the payment of the issue fee but after the mailing date of the first to occur of either: (1) a final action under 37 C.F.R. §1.113; (2) a notice of allowance under 37 C.F.R. §1.311; or (3) an action that otherwise closes prosecution in the application, and:

- ☐ Applicant certifies pursuant to 37 C.F.R. §1.97(e) that:
 - ☐ each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Statement; OR
 - ☐ no item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the person signing this certification after making reasonable inquiry, no item of information contained in this Statement was known to any individual

designated under 37 C.F.R. §1.56(c) more than three months prior to the filing of this Statement; AND

☐ attached hereto is the fee set forth under 37 C.F.R. §1.17(p) for submission of this Information Disclosure Statement under 37

C.F.R. §1.97(d); OR

☐ after the payment of the issue fee. Applicant requests that the information contained in this Information Disclosure Statement be placed in the file according to 37 C.F.R. §1.97(i), although the information may not be considered by the USPTO.

☒ This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior application No. 13/656,238, filed on 19 October 2012, and the references cited therein are hereby referenced, but are not required to be provided in this application under 37 C.F.R. §1.98(d).

☒ In accordance with 37 C.F.R. §§1.97 and 1.98, and in compliance with the duty of disclosure set forth in 37 C.F.R. §1.56, applicant submits attached Form PTO/SB/08a (EFS-Web) for consideration and request the references cited therein be made of record by the U.S. Patent and Trademark Office in the above-captioned application.

Consideration of the foregoing plus the prompt return of a copy of the enclosed Form SB/08A with the Examiner's initials in the left column in accordance with MPEP §609 are respectfully requested.

Respectfully submitted,

Dated 5/5/2014

/Jose G. Moniz/
Jose Gabriel Moniz, Reg. No.: 50,192
Rambus Inc.
1050 Enterprise Way, Suite 700
Sunnyvale, CA 94089
Tel.: (408) 462-8000
Fax: (408) 462-8001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of	)	Art Unit :	2827
	)		
Inventor: Scott C. Best	)	Examiner:	NOT ASSIGNED
	)		
Application No.: 14/230,558	)	Conf. No.:	9057
	)		
Filed: March 31, 2014	)		
	)	Filed via EFS	
For: STROBE-OFFSET CONTROL CIRCUIT	)		

Mail Stop Amendment
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Dear Sir/Madam:

Prior to examination, Applicants respectfully set forth amendments to the claims as shown below.

Amendment to the Claims: Begins on page 2 of this paper.

Remarks: Begin on page 7 of this paper.

In The Claims

Please amend the claims as set forth below.

1. (Currently Amended) An integrated circuit (IC) memory controller comprising:

~~a first interface circuit corresponding to a first input/output (I/O) pin, the first I/O pin to receive a first data signal accompanied by a strobe signal;~~

~~a first alignment circuit to impart a delay to at least one of the first data signal and the strobe signal, the first alignment circuit including a first data adjustable delay circuit element to delay the received first data signal by a first delay corresponding to a first predetermined delay value and generate a first delayed data signal;~~

~~a second interface circuit corresponding to a second input/output (I/O) pin, the second I/O pin to receive a second data signal accompanied by the strobe signal;~~

~~a second alignment circuit to impart a delay to at least one of the second data signal and the strobe signal, the second alignment circuit including a second data adjustable delay circuit element to delay the received second data signal by a second delay corresponding to a second predetermined delay value that is independent of the first predetermined delay value and generate a second delayed data signal;~~

~~a pin to receive a strobe signal;~~

~~a first sampling circuit to sample the first delayed data signal based on the strobe signal; and~~

~~a second sampling circuit to sample the second delayed data signal based on the received strobe signal.~~

2. (Currently Amended) The IC memory controller according to claim 1, further comprising storage to store each of the first and second predetermined delay values corresponding to the delays imparted to the first and second data signals.

3. (Original) The IC memory controller according to claim 1, embodied as a field programmable gate array (FPGA) device.

4. (Currently Amended) The IC memory controller according to claim 1, further comprising ~~a strobe I/O pin to receive the strobe signal wherein the first and second data signals are delayed to compensate for timing offset between the received first and second data signals.~~

5. (Currently Amended) The IC memory controller according to claim 1, wherein:
each of the first and second ~~data delay circuits elements~~ comprise locked-loop circuits having plural serially connected delay elements.

6. (Currently Amended) The IC memory controller according to claim 1, further comprising a calibration strobe delay ~~circuit element~~ to impart a calibrated delay to the strobe signal.

7. (Currently Amended) The IC memory controller according to claim 5, wherein the first ~~delay value is used to select delay elements of the first delay circuit and the second predetermined delay values is used to select~~ correspond to respective selected delay elements of the first and second data delay circuits to impart the respective delays to the first and second data signals.

8. (Currently Amended) The IC memory controller according to claim ~~14~~, further comprising:
a first timing signal delay ~~circuit element~~ associated with the first ~~I/O circuit pin~~;
and
a second timing signal delay ~~circuit element~~ associated with the second ~~I/O circuit pin~~;
wherein each of the first and second timing signal delay ~~circuits elements~~ impart independently-determined first and second timing signal delays to the strobe signal.

9. (Currently Amended) The IC memory controller according to claim 1, further comprising a calibration circuit to, in a calibration mode, determine the first and second ~~predetermined delay values.~~

10. (Currently Amended) A method of operation in an IC memory controller, the method comprising:

~~in a receiving mode;~~

receiving first and second data signals from a memory device at respective first and second I/O pins; ~~the first and second data signals accompanied by a strobe signal;~~

aligning the received first and second data signals with ~~the a~~ strobe signal, the aligning comprising

imparting a first delay to ~~at least one of the first data signal and the strobe~~ signal, the first delay corresponding to a first ~~predetermined~~ delay value,

imparting a second delay to ~~at least one of the second data signal and the strobe~~ signal, the second delay corresponding to a second ~~predetermined~~ delay value that is independent of the first ~~predetermined~~ delay value.

11. (Currently Amended) The method according to claim 10, further comprising:

in a calibration mode,

determining the first and second ~~predetermined~~ delay values; and

storing the first and second ~~predetermined~~ delay values.

12. (Currently Amended) The method according to claim 11, wherein:

during the receiving mode,

the imparting the first and second delays includes retrieving the stored first and second ~~predetermined~~ delay values.

13. (Currently Amended) The method according to claim 12, wherein:

the first and second data signals are delayed by the first and second ~~predetermined~~ delay values.

14. (Original) The method according to claim 11, further comprising:

during the calibration mode,

calibrating a timing signal delay value corresponding to a delay for application to the strobe signal.

15. (Original) The method according to claim 14, further comprising:

during the calibration mode,

storing the calibrated timing delay value.

16. (Currently Amended) A Field Programmable Gate Array (FPGA) device comprising:

a memory controller interface, the memory controller interface including data I/O pins and at least one strobe pin, the data I/O pins to receive respective data signals, ~~the at least one strobe pin to receive at least one strobe signal that accompanies the data signals;~~

calibration circuitry to, in a calibration mode, determine delay values corresponding to delays to impart to, for each I/O pin, ~~at least one of a received data signal and the strobe signal to align the data signals with and a strobe signals for data sampling operations,~~ each I/O pin associated with a given delay value, ~~wherein each of the delay values are determined independently of each other;~~

alignment circuits corresponding to each data I/O pin, each alignment circuit including delay circuitry responsive to a given determined delay value;

storage to store the determined delay values;

~~wherein during a receiving mode, the memory controller interface retrieves the stored determined delay values for each alignment circuit.~~

17. (Currently Amended) The FPGA according to claim 16, wherein the calibration circuitry determines a timing signal delay to impart to the ~~at least one strobe signal.~~

18. (Currently Amended) The FPGA according to claim 17, wherein each alignment circuit includes a timing signal delay ~~circuit element~~ responsive to the determined timing signal delay.

19. (Original) The FPGA according to claim 16, wherein the alignment circuits include respective locked-loop circuits responsive to different ones of the determined delay values.

20. (Currently Amended) The FPGA according to claim ~~19~~16, wherein the calibration circuitry includes a calibration strobe delay ~~circuit element~~ to impart a calibrated delay to the strobe signal.

Remarks

Claims 1-20 remain pending in the instant application, with claims 1, 2, 4-13, 16-18 and 20 being amended prior to examination. No new subject matter has been added.

Conclusion

In view of the foregoing, Applicant believes all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If there are any additional charges due in connection with this submission, including extension of time fees, please charge them to Deposit Account Number 506388.

Respectfully submitted,
Peninsula Patent Group

Date May 1, 2014

/Lance M. Kreisman/
Lance M. Kreisman, Reg. No. 39,256
Peninsula Patent Group
606 Lincoln Avenue
Los Altos, CA 94022
Tel. 650-468-9654

IN THE UNITED STATES PATENT OFFICE

In Re Patent Application of

Inventors: Scott C. Best

Application No.: 14/230,558

Filed: March 31, 2014

For: STROBE-OFFSET CONTROL CIRCUIT

Examiner: Unknown

Art Unit: 2827

Confirmation No.: 9057

Filed via EFS

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE TO FILE MISSING PARTS

This is in response to a Notice to File Missing Parts of Application under 37 CFR 1.53(b) dated April 23, 2014. Enclosed is a copy of the Notice, a requisite inventor Oath, and the following fees to complete the filing requirements of the above-identified application.

- (X) Total amount submitted herewith is **\$140.00**
- () Statutory basic filing fee, search fee and examination fee **\$1600.00**
- () Applicant Claims Small Entity status
- () Additional claim fees of **\$0.00**
- (X) Missing Parts Surcharge = **\$140.00**

Respectfully submitted,

MAHAMEDI PARADICE KREISMAN LLP

Date: May 1, 2014

/Lance M. Kreisman/
Lance M. Kreisman, Reg. No. 39,256
Peninsula Patent Group
606 Lincoln Avenue
Los Altos, CA 94022
Tel. 650-468-9654



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/230,558	03/31/2014	Scott C. Best	RBS2.P005C5

CONFIRMATION NO. 9057

FORMALITIES LETTER



44429

Lance M. Kreisman
Peninsula Patent Group (Rambus)
606 Lincoln Ave.
Los Altos, CA 94022

Date Mailed: 04/23/2014

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing.

Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.

The surcharge is due for any one of:

- late submission of the basic filing fee, search fee, or examination fee,
- late submission of inventor's oath or declaration,
- filing an application that does not contain at least one claim on filing, or
- submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- \$ 140 surcharge.
- \$(.00) previous unapplied payment amount.
- \$ 140 TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
Scott C. Best

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice".
<https://portal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/sareebuddin/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

**DECLARATION (37 CFR 1.63) FOR PROVISIONAL, UTILITY, DESIGN, OR NATIONAL
STAGE OF PCT APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention: **STROBE-OFFSET CONTROL CIRCUIT**

As a below named inventor, I hereby declare that:

This declaration is directed to:

- _____ The attached application, or
- _____ United States Provisional Application Number [Enter App #] filed on [Enter Date], or
- X United States Application Number **14/230,558**, filed on **March 31, 2014**.

The above-identified application was made or authorized to be made by me.

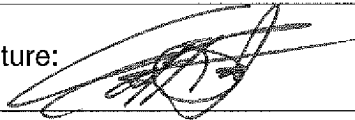
I have authorized and/or hereby do authorize my assignee to file patent applications claiming priority from the application referenced above, including provisional, non-provisional, design, divisional, continuation, continued prosecution, continuation-in-part, substitute, supplemental examination application, and other applications related to the subject matter of the application referenced above. I have authorized and/or hereby do authorize my assignee to make changes to the application for matters of formality.

I believe I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under Section 1001 of Title 18 of the United States Code by fine or imprisonment of not more than five (5) years, or both.

Warning: Declarant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent.

Legal Name of Inventor:

Inventor: Scott C. Best	Date: <i>7 Apr 14</i>
Signature: 	

Electronic Patent Application Fee Transmittal				
Application Number:	14230558			
Filing Date:	31-Mar-2014			
Title of Invention:	STROBE-OFFSET CONTROL CIRCUIT			
First Named Inventor/Applicant Name:	Scott C. Best			
Filer:	Lance Martel Kreisman			
Attorney Docket Number:	RBS2.P005C5			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Late Filing Fee for Oath or Declaration	1051	1	140	140
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				140

Electronic Acknowledgement Receipt	
EFS ID:	18922763
Application Number:	14230558
International Application Number:	
Confirmation Number:	9057
Title of Invention:	STROBE-OFFSET CONTROL CIRCUIT
First Named Inventor/Applicant Name:	Scott C. Best
Customer Number:	44429
Filer:	Lance Martel Kreisman
Filer Authorized By:	
Attorney Docket Number:	RBS2.P005C5
Receipt Date:	01-MAY-2014
Filing Date:	31-MAR-2014
Time Stamp:	21:16:51
Application Type:	Utility under 35 USC 111(a)

Payment information:	
Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 140
RAM confirmation Number	5194
Deposit Account	
Authorized User	

File Listing:				
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part / zip (if appl.) Pages

1	Preliminary Amendment	RA356_RBS2_P005C5_Prelim.pdf	39275 09d6486da31e990071896baa50fc1dc2aec5c089	no	7
Warnings:					
Information:					
2	Applicant Response to Pre-Exam Formalities Notice	RA356_RBS2_P005C5_RMP_AF.pdf	266571 58c8eab96d8c13ffad979ca1ff1da7fa5329485	no	3
Warnings:					
Information:					
3	Oath or Declaration filed	RA356_RBS2_P005_Declaration.pdf	33432 52ff8120e845b1c3ebdf16b3b528099f100d9afc	no	1
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	29654 114ab9399a304f8dc537c6c877b35587579eb318	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			368932		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/230,558	Filing Date 03/31/2014	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO**APPLICATION AS FILED – PART I**

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA		RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED – PART II

(Column 1)

(Column 2)

(Column 3)

	05/01/2014	CLAIMS REMAINING AFTER AMENDMENT	Minus	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x \$80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0		x \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

(Column 1)

(Column 2)

(Column 3)

		CLAIMS REMAINING AFTER AMENDMENT	Minus	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=		X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LDRC
/PAMELA ROGERS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY,DOCKET,NO	TOT CLAIMS	IND CLAIMS
14/230,558	03/31/2014	2827	1600	RBS2.P005C5	20	3

CONFIRMATION NO. 9057

44429

Lance M. Kreisman
Peninsula Patent Group (Rambus)
606 Lincoln Ave.
Los Altos, CA 94022

FILING RECEIPT



OC000000067937067

Date Mailed: 04/23/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Scott C. Best, Palo Alto, CA;

Applicant(s)

Scott C. Best, Palo Alto, CA;

Assignment For Published Patent Application

Rambus Inc., Sunnyvale, CA

Power of Attorney: The patent practitioners associated with Customer Number 44429

Domestic Priority data as claimed by applicant

This application is a CON of 13/656,238 10/19/2012 PAT 8688399
which is a CON of 13/276,708 10/19/2011 PAT 8311761
which is a CON of 12/694,251 01/26/2010 PAT 8135555
which is a CON of 11/621,491 01/09/2007 PAT 7668679
which is a CON of 10/923,421 08/20/2004 PAT 7171321

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 04/21/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/230,558**

Projected Publication Date: 07/31/2014

Non-Publication Request: No

Early Publication Request: No
Title

STROBE-OFFSET CONTROL CIRCUIT

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 14/230,558				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE <small>(37 CFR 1.16(a), (b), or (c))</small>	N/A	N/A	N/A			N/A	280			
SEARCH FEE <small>(37 CFR 1.16(k), (l), or (m))</small>	N/A	N/A	N/A			N/A	600			
EXAMINATION FEE <small>(37 CFR 1.16(o), (p), or (q))</small>	N/A	N/A	N/A			N/A	720			
TOTAL CLAIMS <small>(37 CFR 1.16(j))</small>	20	minus 20 = *			OR	x 80 =	0.00			
INDEPENDENT CLAIMS <small>(37 CFR 1.16(h))</small>	3	minus 3 = *				x 420 =	0.00			
APPLICATION SIZE FEE <small>(37 CFR 1.16(s))</small>	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT <small>(37 CFR 1.16(j))</small>							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	1600			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total <small>(37 CFR 1.16(i))</small>	*	Minus	**	=	x	=	OR	x	=
	Independent <small>(37 CFR 1.16(h))</small>	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee <small>(37 CFR 1.16(s))</small>							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <small>(37 CFR 1.16(j))</small>							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total <small>(37 CFR 1.16(i))</small>	*	Minus	**	=	x	=	OR	x	=
	Independent <small>(37 CFR 1.16(h))</small>	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee <small>(37 CFR 1.16(s))</small>							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <small>(37 CFR 1.16(j))</small>							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/230,558	03/31/2014	Scott C. Best	RBS2.P005C5

CONFIRMATION NO. 9057

FORMALITIES LETTER



OC000000067937068

44429
Lance M. Kreisman
Peninsula Patent Group (Rambus)
606 Lincoln Ave.
Los Altos, CA 94022

Date Mailed: 04/23/2014

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing.

Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.

The surcharge is due for any one of:

- late submission of the basic filing fee, search fee, or examination fee,
- late submission of inventor's oath or declaration,
- filing an application that does not contain at least one claim on filing, or
- submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- \$ 140 surcharge.
- \$(.00) previous unapplied payment amount.
- \$ 140 TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
Scott C. Best

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice".
<https://portal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/sareebuddin/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

UTILITY PATENT APPLICATION TRANSMITTAL <small>(Only for new nonprovisional applications under 37 CFR 1.53(b))</small>		Attorney Docket No.	RBS2.P005C5																
		First Named Inventor	Scott C. Best																
		Title	Strobe-Offset Control Circuit																
		Express Mail Label No.	filed via EFS-web																
APPLICATION ELEMENTS <small>See MPEP chapter 600 concerning utility patent application contents.</small>		Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450																	
<div style="display: flex; justify-content: space-between;"><div style="width: 48%;"><p>1. ☐ Fee Transmittal Form (PTO/SB/17 or equivalent)</p><p>2. ☐ Applicant asserts small entity status. See 37 CFR 1.27</p><p>3. ☐ Applicant certifies micro entity status. See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.</p><p>4. ☒ Specification [Total Pages <u>34</u>] Both the claims and abstract must start on a new page. (See MPEP § 608.01(a) for information on the preferred arrangement)</p><p>5. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets <u>13</u>]</p><p>6. Inventor's Oath or Declaration [Total Pages _____] (including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))</p><p style="margin-left: 20px;">a. ☐ Newly executed (original or copy)</p><p style="margin-left: 20px;">b. ☐ A copy from a prior application (37 CFR 1.63(d))</p><p>7. ☒ Application Data Sheet * See note below. See 37 CFR 1.76 (PTO/AIA/14 or equivalent)</p><p>8. CD-ROM or CD-R in duplicate, large table, or Computer Program (Appendix)</p><p style="margin-left: 20px;">☐ Landscape Table on CD</p><p>9. Nucleotide and/or Amino Acid Sequence Submission (if applicable, items a. – c. are required)</p><p style="margin-left: 20px;">a. ☐ Computer Readable Form (CRF)</p><p style="margin-left: 20px;">b. ☐ Specification Sequence Listing on:</p><p style="margin-left: 40px;">i. ☐ CD-ROM or CD-R (2 copies); or</p><p style="margin-left: 40px;">ii. ☐ Paper</p><p style="margin-left: 20px;">c. ☐ Statements verifying identity of above copies</p></div><div style="width: 48%;">ACCOMPANYING APPLICATION PAPERS<p>10. ☐ Assignment Papers (cover sheet & document(s)) Name of Assignee _____</p><p>11. ☒ 37 CFR 3.73(c) Statement ☒ Power of Attorney (when there is an assignee)</p><p>12. ☐ English Translation Document (if applicable)</p><p>13. ☐ Information Disclosure Statement (PTO/SB/08 or PTO-1449) ☐ Copies of citations attached</p><p>14. ☐ Preliminary Amendment</p><p>15. ☐ Return Receipt Postcard (MPEP § 503) (Should be specifically itemized)</p><p>16. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)</p><p>17. ☐ Nonpublication Request Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.</p><p>18. ☐ Other: _____ _____ _____ _____</p></div></div>																			
		*Note: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 must be included in an Application Data Sheet (ADS). (2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).																	
19. CORRESPONDENCE ADDRESS																			
☒ The address associated with Customer Number: <u>44429</u> OR ☐ Correspondence address below																			
<table border="1" style="width: 100%; border-collapse: collapse;"><tr><td style="width: 20%;">Name</td><td colspan="3"></td></tr><tr><td>Address</td><td colspan="3"></td></tr><tr><td>City</td><td style="width: 20%;">State</td><td style="width: 20%;">Zip Code</td><td></td></tr><tr><td>Country</td><td>Telephone</td><td>Email</td><td></td></tr></table>				Name				Address				City	State	Zip Code		Country	Telephone	Email	
Name																			
Address																			
City	State	Zip Code																	
Country	Telephone	Email																	
Signature		Date																	
/Lance M. Kreisman/		March 31, 2014																	
Name (Print/Type)		Registration No. (Attorney/Agent)																	
Lance M. Kreisman		39256																	

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	RBS2.P005C5
		Application Number	
Title of Invention	STROBE-OFFSET CONTROL CIRCUIT		
<p>The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.</p> <p>This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.</p>			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1					Remove	
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117		☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Scott	C.	Best			
Residence Information (Select One)		☒ US Residency ☐ Non US Residency ☐ Active US Military Service				
City	Palo Alto	State/Province	CA	Country of Residence ⁱ	US	
Citizenship under 37 CFR 1.41(b) ⁱ		US				
Mailing Address of Applicant:						
Address 1		1050 Enterprise Way, Suite 700				
Address 2						
City	Sunnyvale	State/Province	CA			
Postal Code	94089	Country ⁱ	US			
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add						

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence Information of this application.			
Customer Number	44429		
Email Address	uspto@peninsulaiplaw.com	Add Email	Remove Email

Application Information:

Title of the Invention	STROBE-OFFSET CONTROL CIRCUIT		
Attorney Docket Number	RBS2.P005C5	Small Entity Status Claimed ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)	702	Sub Class (if any)	106
Suggested Technology Center (if any)	2800		
Total Number of Drawing Sheets (if any)	13	Suggested Figure for Publication (if any)	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	RBS2.P005C5
		Application Number	
Title of Invention	STROBE-OFFSET CONTROL CIRCUIT		

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	44429		

Domestic Benefit/National Stage Information:

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Prior Application Status	Pending		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
Unassigned	Continuation of	13656238	2012-10-19		
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13656238	Continuation of	13276708	2011-10-19	8311761	2012-11-13
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13276708	Continuation of	12694251	2010-01-26	8135555	2012-03-13
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12694251	Continuation of	11621491	2007-01-09	7668679	2010-02-23
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11621491	Continuation of	10923421	2004-08-20	7171321	2007-01-30

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	RBS2.P005C5
		Application Number	
Title of Invention	STROBE-OFFSET CONTROL CIRCUIT		

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Organization Name Rambus Inc.

Mailing Address Information:

Address 1	1050 Enterprise Way, Suite 700		
Address 2			
City	Sunnyvale	State/Province	CA
Country ⁱ	US	Postal Code	94089
Phone Number	408-462-8000	Fax Number	
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		Application Number	
Title of Invention	STROBE-OFFSET CONTROL CIRCUIT		

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Strobe-Offset Control Circuit

Inventor:

Scott C. Best

[0001] Related Applications

[0002] This application is a Continuation of U.S. Patent Application Serial No. 13/656,238, filed October 19, 2012, which is a Continuation of U.S. Patent Application Serial No. 13/276,708, filed October 19, 2011, which is a Continuation of U.S. Patent Application Serial No. 12/694,251, filed January 26, 2010, now U.S. Patent No. 8,135,555, which is a Continuation of U.S. Patent Application Serial No. 11/621,491, filed January 9, 2007, now U.S. Patent No. 7,668,679, which is a Continuation of U.S. Patent Application Serial No. 10/923,421, filed August 20, 2004, now U.S. Patent No. 7,171,321, each of which is hereby incorporated by reference in its entirety.

[0003] Technical Field

[0004] The disclosure herein relates generally to memory systems and methods. In particular, this disclosure relates to systems and methods for transferring information among memory devices and a memory controller.

[0005] Background

[0006] High-speed processor-based electronic systems have become all-pervasive in computing, communications, and consumer electronic applications to name a few. The pervasiveness of these systems, many of which are based on multi-gigahertz processors,

has led in turn to an increased demand for the systems to host a larger number of applications having a higher level of complexity than those applications hosted on electronic systems of previous generations. The transfer of information and signals required among the components of these high-speed systems in support of these applications has led to increasing demands for interfaces to support the efficient high-speed transfer of information. Examples of such interfaces include the interfaces between processors and memory devices of high-speed systems.

[0007] One memory type typically used in high-speed processing systems is double-data rate dynamic random access memory (DRAM). The double-data rate DRAM is typically twice as fast as a single data rate DRAM running at the same clock speed because a double-data rate DRAM transfers data on both the rising and falling edge of the clock.

[0008] While the use of double-data rate memory systems leads to increases in data transfer speeds, issues arise regarding the timing of the data transfer, particularly where a memory controller receives data sent by a double data rate DRAM attached thereto using a strobe-based method. Using this strobe-based method, a strobe signal (also referred to as the DQS signal) is edge-aligned to and accompanies a data signal (also referred to as the DQ signal) sent by the DRAM. This DQS is used by the controller to capture the data signal sent by the DRAM. The DQS signal and the data are received and the DQS signal is delayed by some fixed amount, usually one-fourth of the memory system clock period. This delayed DQS signal, which is approximately in quadrature with the received data, is then used as a common sample clock for each of the DQ input receivers in typically a byte or 8 bits of data sent in parallel. Due to system offsets and

pin-to-pin offsets in the DRAM (commonly referred to on DRAM datasheets as “tDQSQ”), however, one strobe-delay value for the whole byte cannot be the ideal amount of strobe-delay for every pin. Furthermore, while manual adjustment of per-bit offsets can yield higher performing memory systems, requiring manual adjustments of these offsets in a production memory system tends to be expensive.

[0009] In some memory systems, calibration is performed by affecting the read and write timing positions of the memory controller based on pattern comparisons. For example, to calibrate the read timing of a system, a DRAM can be instructed to provide a known pattern to the controller. The controller then adjusts its read-clock timing position to determine the pass-fail regions (e.g., when a comparison between the received data and the expected data fails, the controller determines that phase position to be in a fail region). Once the pass-fail regions for the entire data-eye are known, the controller chooses an optimal read-clock position centered within the known passing region. A strobe-delay value can be subsequently determined for this optimal read-clock position.

[0010] Timing-calibrated memory systems which eliminate pin-to-pin timing variation can give better performance than strobe-based memory systems which use per-byte strobes, but they are substantially more complex. Consequently, there is a need in high-speed, strobe-based memory systems, for per-pin (data bit) strobe-offset control and timing calibration to minimize DQS-to-DQ timing offsets for each DQ pin individually, yielding more robust, higher-speed systems.

[0011] Brief Description of the Drawings

[0012] In the drawings, the same reference numbers identify identical or substantially similar elements or acts. To easily identify the discussion of any particular element or act, the most significant digit or digits in a reference number refer to the Figure number in which that element is first introduced (e.g., element 120 is first introduced and discussed with respect to Figure 1).

[0013] **Figure 1** is a block diagram of a strobe-based memory system including a strobe-offset control system for individual data line strobe-offset control, under an embodiment.

[0014] **Figure 2** is a flow diagram for individual data line strobe-offset calibration in a calibration mode, under an embodiment.

[0015] **Figure 3** is a flow diagram for receiving data signals of an individual data line using an optimized sample signal, under an embodiment.

[0016] **Figure 4** is a block diagram of a strobe-based memory system including a strobe-offset control system in the calibration mode, under an embodiment.

[0017] **Figure 5** is a timing diagram showing the determination/application of the optimal per-bit variable delay to a strobe signal to generate per-bit strobe signals during calibration mode, under an embodiment.

[0018] **Figure 6** is a block diagram of a strobe-based memory system including a strobe-offset control system in the receiver mode, under an embodiment.

[0019] **Figure 7** is a timing diagram showing adjustment of strobe signal timing using an optimal per-bit offset (calibration mode) along with a fixed delay (receiver

mode) to generate a per-bit strobe signal with optimal alignment for sampling a corresponding data signal, under an embodiment.

[0020] **Figure 8** is a block diagram of a strobe-based memory system including a strobe-offset control system for individual data line strobe-offset control, under an embodiment.

[0021] **Figure 9** is a block diagram of a delay element control circuit for use in strobe-based memory controllers, under an embodiment.

[0022] **Figure 10** is a block diagram of a strobe-offset control system for individual data line strobe-offset control in strobe-based DDR memory systems, under an alternative embodiment of Figure 1.

[0023] **Figure 11** is a block diagram of a control system for individual data line rising and falling edge strobe-offset control in strobe-based DDR memory controllers, under an alternative embodiment of Figure 10.

[0024] **Figure 12** is a block diagram of a calibration control circuit, under an embodiment.

[0025] **Figure 13** shows a charge pump that can replace the N-bit counter of a calibration control circuit, under an embodiment.

Detailed Description

[0026] Systems and methods for strobe signal timing calibration and control in strobe-based memory systems are provided below. These systems and methods, also referred to herein as strobe-offset control systems and methods, receive a strobe signal from a memory device and in turn generate separate per-bit strobe signals for use in receiving data on an external data line or signal line of a memory system. The systems/methods generate the optimal per-bit strobe signals by automatically calibrating per-bit offset timing between data signals $DQ\langle X \rangle$ of individual data lines (where $DQ\langle X \rangle$ represents any one of a number of data lines $DQ\langle N:0 \rangle$, where X is any of data lines 0, 1, 2 ... N) and corresponding strobe signals DQS . The strobe signals DQS are also referred to as strobes and data strobes. The strobe-offset control system is for use in strobe-based memory systems which include, for example, double data rate (DDR) systems like DDR SDRAM as well as DDR2 SDRAM and other DDR SDRAM variants, such as reduced latency DRAM (RLDRAM), RLDRAM2, Graphics DDR (GDDR) and GDDR2, GDDR3, but is not limited to these memory systems.

[0027] The strobe-offset control system generally includes a calibration control circuit coupled to a variable delay element, both of which couple to a receiver. When operating in a calibration mode, the receiver functions as a phase detector and the combination of the receiver, calibration control circuit and variable delay element can effectively form a delay-locked loop (DLL) circuit. This DLL circuit, in response to phase information of the data signals and corresponding strobe signals, adjusts the phase relationship between the strobe signals and the data signals for each received data bit by adjusting an offset or delay value applied to the strobe signal. The delay value is

adjusted, for example, to optimally edge-align the data signal DQ<X> and corresponding strobe signal DQS, but is not so limited. The optimal edge-alignment can be with respect to the rising edge or falling edge of the data DQ<X> and strobe DQS signals. The optimal delay value, once determined, is maintained and the system is subsequently placed in a receiver mode.

[0028] In the receiver mode, the receiver now functions as an input sampler or data signal sampler. The delay value determined during the calibration mode is applied to the strobe signals DQS received from the memory devices to generate a per-bit quadrature (i.e., approximately 90 degree phase offset) sample signal DQS' (also referred to as per-bit strobe signal DQS'); the per-bit strobe DQS' is output for use by the input sampler in receiving data of a corresponding data signal DQ<X>. Use of the delay value effectively removes the detected phase difference between the data signal DQ<X> and the strobe signal DQS, thereby optimizing the overall timing margin for that specific data bit DQ<X> during data transfer operations.

[0029] In the following description, numerous specific details are introduced to provide a thorough understanding of, and enabling description for, embodiments of the strobe-offset control system. One skilled in the relevant art, however, will recognize that these embodiments can be practiced without one or more of the specific details, or with other components, systems, etc. In other instances, well-known structures or operations are not shown, or are not described in detail, to avoid obscuring aspects of the disclosed embodiments. As an example, the strobe-offset control embodiments described herein are presented in the context of transferring individual data bits DQ<X>

with the understanding that the disclosed concepts apply to all data transferred during memory system operations.

[0030] **Figure 1** is a block diagram of a strobe-based memory system 199 including a strobe-offset control system 100 for individual data line strobe-offset control, under an embodiment. The strobe-based memory system 199 is a component of and/or coupled to a host system or device (not shown) as appropriate to the host system/device. A strobe-offset control system 100 is coupled to receive data of each data line of the memory system 199, and can include and/or couple with additional components as appropriate to the memory system 199 or host electronic system. The strobe-offset control system 100 includes a receiver 102 with a data input coupled to a data signal DQ<X> via a data line 104 through at least one data delay element 150. The data signal DQ<X> includes information of one data bit of an N-bit wide data byte transferred to the receiver 102 from one or more memory devices 190 via one or more signal lines or buses 170. The receiver 102 samples the data signal DQ<X> in response to the sample signal DQS' 106 as described below and outputs data signal 112 that includes data <0:N>.

[0031] The strobe-offset control system 100 also includes a multiplexer 140 that receives a delayed strobe signal at a first input 142 and a strobe signal DQS at a second input 144. The delayed strobe signal is generated from the strobe signal DQS by a strobe delay element 160. The multiplexer 140, under control of a memory controller or other device (not shown) via a calibrate-enable signal 122, provides one of the delayed strobe signal or the strobe signal DQS to an input 132 of a variable delay element 130 as appropriate to operating modes of the strobe-offset control system 100 described below.

[0032] The variable delay element 130 receives the output signal of the multiplexer 140 and generates sample signals DQS' 106 by applying a delay to the signals received at the input 132. The variable delay element 130 of an embodiment supports delays approximately in the range of one-sixth (i.e., 60 degrees) to one-third (i.e., 120 degrees) of the memory system clock period, and alternative embodiments support other delay periods as appropriate to the receiver and the desired tuning range of the control system 100. The variable delay element 130 outputs the sample signal DQS' via line 106 to the receiver 102.

[0033] The strobe-offset control system 100 also includes a calibration control circuit 120 which can alternatively be referred to as a calibration controller 120. The calibration control circuit 120, under control of a memory controller or other device (not shown) of the memory system 199 via a calibrate-enable signal 122, operates in a calibration mode to adjust an amount of the delay or offset applied by the variable delay element 130 to versions of the strobe signal.

[0034] The calibration control circuit 120 of an embodiment uses information of one or more signals received from the receiver 102 in performing adjustments of the variable delay value of delay element 130. One signal received from the receiver 102 is an adjustment control signal 114 that affects the amount of offset applied by the variable delay element 130 as described below. Further, the calibration control circuit 120 receives an optional adjustment valid signal 116 from the receiver 102 that indicates when information of the adjustment control signal 114 is valid, as described below.

[0035] As described above, the strobe signal DQS is coupled to a first input of the multiplexer 140 using at least one strobe delay element 160. The strobe delay element

160 applies pre-specified delay or offset to the received strobe signal DQS. The strobe delay element 160 of an embodiment delays the strobe signal DQS by a period of time that is one-fourth of the memory system clock period (i.e., 90 degrees), but alternative embodiments will use delay values appropriate to the receiver type. While the strobe delay element 160 is shown and described as dedicated to each byte, alternative embodiments may use one strobe delay element 160 per bit.

[0036] Likewise, the data signal DQ<X> of an embodiment couples to the receiver 102 through at least one data delay element 150. The data signal DQ<X> is transmitted from the memory devices 190 in a read operation, for example. In a strobe-based system, the transmitted data signal DQ<X> is edge-aligned to the transmitted strobe signal DQS. The data delay element 150 applies pre-specified delay to the received data signal DQ<X>, and couples a delayed version of the data signal DQ<X>' (referred to as the delayed data signal) to the receiver 102. The data delay element 150 delays the data signal DQ<X> by an amount that is approximately equal to the median delay of the variable delay element 130, such as one-fourth of the memory system clock period (i.e., 90 degrees), but alternative embodiments will use other delay values. The delayed data signal DQ<X>' is then used as a data input to the receiver 102.

[0037] The memory system 199 including the strobe-offset control system 100 operates in a number of modes including calibration and receiver modes. In the calibration mode the receiver 102 generally operates as a phase detector and determines any phase difference between a delayed data signal DQ<X>' and the strobe signal DQS'. When operating as a phase detector the receiver will generally be referred to herein as a receiver/phase detector 102. The receiver/phase detector 102 compares the phase

relationship between the strobe signal DQS' and the delayed data signals DQ<X>' for each received data bit, and provides those comparison results to the calibration control circuit 120 via the adjustment control signal 114. In response to the adjustment control signal 114, and optionally in additional response to the adjustment valid signal 116, the calibration control circuit 120 will adjust the delay control signal 124 which affects the delay value applied to the strobe signal DQS via the variable delay circuit 130. In this embodiment, the receiver/phase-detector 102 in combination with the calibration control circuit 120 and the variable delay circuit 130 acts very much like a delay-locked loop circuit (DLL). Once this DLL-like circuit is "locked", the adjusted delay of the variable delay circuit 130, when applied to the strobe signal DQS, results in a per-bit sample signal DQS' that is approximately edge-aligned to the delayed data signal DQ<X>'. Alternatively, at least one of the delay elements 130 or 150 is variable, while at most one of them is fixed, where the relative delay between delays provided by delay elements 130 and 150 are controlled by the calibration control circuit 120. Furthermore, if both delay elements 130 and 150 are variable delay elements, calibration control circuit 120 can additionally control the absolute delay of the delay elements 130 and 150 in addition to their relative values.

[0038] In addition to generating information representative of the offset between data and data strobe signals, the calibration control circuit 120 can also store the information for subsequent use and/or processing. As such, the information can be used to characterize the corresponding data paths of the memory system. For example, the data of this characterization can be used to generate offsets for use by the memory

controller in memory write operations. This data also has uses in generating predicted offset values for use by the variable delay element 130 during calibration.

[0039] **Figure 2** is a flow diagram 200 for individual data line strobe-offset calibration in a calibration mode, under an embodiment. Taking one data line as an example, a state of a calibrate-enable signal places one or more components of the strobe-offset control system in a calibration mode, at block 202. In the calibration mode, a multiplexer is configured to provide the received strobe signal (DQS) to the input of a delay circuit, at block 204. Additionally, the receiver is configured to compare timing of the edge-positions of the delayed sample signal (DQS') and the delayed data signals of the data line, at block 206. A dummy read of the memory devices is initiated, at block 208. A dummy read is generally defined to include a process in which a controller interface circuit makes a read request from the DRAM, independent of any data needs of the central processor or other higher layer machine-readable code; these reads are performed at power-up, or other intervals in which the DRAM was otherwise not being utilized.

[0040] In response to the dummy read, data and DQS signals are transmitted from the DRAM, received at the controller, and any phase difference between the delayed sample signal DQS' and the delayed data signal is detected, at block 210. Control signals are generated in response to detected phase differences, and the control signals are used to adjust the amount of variable delay which is applied to either the sample signal or the data signal, at block 212. The variable delay value for each data line, when applied to a per-bit sample signal, optimally edge-aligns the per-bit sample signal to the data signal of that data line, but is not so limited. A lock signal is output in response to

determination of the optimal offset, at block 214, but generation of a lock signal is optional as alternative embodiments can determine completion of calibration using any number of other methods.

[0041] Following determination and adjustment of the optimal variable delay value the memory system is placed in a receiver mode in which the receiver functions as an input sampler. When operating as an input sampler the receiver will generally be referred to herein as a receiver/input sampler 102. The variable delay value determined/adjusted during the calibration mode is subsequently used in generating a per-bit sample signal for use by the input sampler in receiving data of a corresponding data signal. Use of the variable delay value effectively removes any unwanted offsets between the data signal and the strobe signal, thereby optimizing the overall timing margin between the data signal and the per-bit sample signal during data transfer operations.

[0042] **Figure 3** is a flow diagram 300 for receiving data signals of an individual data line using an optimized sample signal, under an embodiment. Following calibration of the offset, as described above, a state of the calibrate-enable signal places the strobe-offset control system in a receiver mode, at block 302. In the receiver mode, a multiplexer is configured to provide a delayed version of the received strobe signal (DQS) as the input to a second delay circuit, at block 304. The delayed strobe signal is delayed by a period that is approximately one-fourth of the memory system clock period (i.e., 90 degrees). The output of this second delay circuit is provided as a sample signal for sampling data signals of the data line, at block 306. The second delay circuit applies an amount of delay (determined during calibration mode) to the delayed strobe signal, at

block 308 (the strobe signal, therefore, is delayed by a total period of approximately one-fourth of the memory system clock period plus the period of the calibrated delay). The twice delayed signal (delayed strobe signal with calibrated applied) is subsequently output as the sample signal for sampling the individual data line, at block 310.

[0043] As a further example of the operating modes described above, **Figure 4** is a block diagram of a strobe-based memory system 199 including a strobe-offset control system 100 in the calibration mode, under an embodiment. The strobe-offset control system 100 and memory system 199 are as described above with reference to Figure 1. Regarding the calibration mode, a memory controller or other component of the memory system 199 activates the calibrate-enable signals 122 to the strobe-offset control system 100 in response to, for example, initialization or re-initialization of a host system. The active state of the calibrate-enable signal 122 places the calibration control circuit 120 in a calibration mode, and selects the strobe signal DQS (input 144) as the output 132 of the multiplexer 140 and consequently the input of the variable delay element 130. The output of the variable delay element 130 is a delayed version of the input signal, as described below, and is used as a sample signal DQS' 106 input to the receiver.

[0044] A dummy read of the memory devices 190 is then initiated by the memory controller (not shown) during which the delayed data signal DQ<X>' is compared with DQS' by the receiver/phase detector 102. In the calibration mode the receiver/phase detector 102 acts as a phase detector (PD) 102 which compares the phase difference between the delayed data signal DQ<X>' and the sample signal DQS'. In response to detected phase differences the receiver/phase detector 102 generates an adjustment control signal 114, and an optional adjustment-valid signal 116. The receiver/phase

detector 102 outputs the adjustment control signal 114, and optionally the adjustment-valid signal 116, to the calibration control circuit 120.

[0045] The adjustment control signal 114 is an embodiment of a delay-lock loop's (DLL's) up/down signal that the calibration controller 120 uses to affect adjustments to the delay value. The calibration control circuit 120 adjusts the delay applied by the variable delay element 130 via signal lines 124 in response to the adjustment-control and optional adjustment-valid signals 114 and 116. Repeated adjustments of the variable delay value, in a closed-loop manner, results in signal DQS' 106 being optimally aligned (approximately edge-aligned) to the delayed data signal DQ<X>'.

[0046] Consequently, the combination of the receiver/phase detector 102, calibration control circuit 120 and variable delay element 130 effectively form a DLL circuit. This DLL circuit, in response to phase information of the delayed data signal DQ<X>' and corresponding delayed strobe signal DQS', adjusts the phase relationship between these signals for each received data bit DQ<X> (where "X" is 0...N, where "N" is the number of bits associated with a given DQS signal) by adjusting a delay applied to the strobe signal DQS. The adjusted delay when applied to the strobe signal DQS results in a per-bit sample signal DQS' that is approximately edge-aligned to the delayed data signal DQ<0>'. An optional lock signal 126 is subsequently output (to the memory controller or other circuitry of the memory system 199) by the calibration control circuit 120 in response to determination of the edge-alignment, but alternative embodiments may not output a lock signal.

[0047] In addition to the adjustment control signal 114 described above, the receiver/phase detector 102 of an embodiment outputs a valid signal 116 to the

calibration control circuit 120 of an embodiment. The valid signal 116, which is output by the receiver/phase detector 102 to indicate when the adjustment control signal 114 is valid, is used in systems in which the data pattern of the dummy read contains an unequal number of transitions between the data DQ<X> and strobe DQS signals. That is, while DQS is defined to transition once for every bit transmitted, the DQ<X> signal may not transition every bit (e.g., if two or more logic-high or logic-low states are transmitted in a row). In such systems, the valid signal 116 indicates that the DQ<X> to DQS comparison result (i.e., adjustment control signal 114) is valid only when DQ<X> is detected to have transitioned for purposes of the comparison. Thus, the valid signal 116 may not be used in systems in which the data pattern of the dummy read results in an equal number of transitions between the data DQ<X> and strobe DQS signals. Furthermore, in some embodiments the adjustment control signal 114 is the same electrical signal as the output of the input sampler when it is used in input-sampler mode, i.e. data<X> signal 112.

[0048] **Figure 5** is a timing diagram 500 showing the determination/application of the optimal per-bit variable delay to a strobe signal DQS to generate per-bit strobe signals DQS' during calibration mode, under an embodiment. Two data lines DQ<0> and DQ<3> are shown as examples only, as the methods described herein are similarly applied to all lines DQ<X>. Looking first at delayed data signal DQ<0>', the rising/falling edges of this data signal DQ<0>' during an example dummy read (calibration mode) are offset from the corresponding rising/falling edges of the strobe signal DQS by a first phase difference 502. This phase-difference will, if uncompensated for, limit the maximum bandwidth achievable by the memory system.

The receiver/phase detector in combination with the calibration control circuit and variable delay element (collectively the DLL) detects the phase difference 502, adjusts a variable delay 504 to compensate for the phase difference, and applies the adjusted delay 504 to the strobe signal DQS. The result of applying the adjusted delay 504 to the strobe signal DQS for this data line is a per-bit sample signal DQS<0>' that is approximately edge-aligned to the delayed data signal DQ<0>'.

[0049] Turning to a second delayed data signal DQ<3>', the rising/falling edges of this data signal DQ<3>' during the example dummy read (calibration mode) are offset from the rising/falling edges of the strobe signal DQS by a second phase difference 512. The DLL (receiver (phase detector), calibration control circuit, variable delay element) detects the phase difference 512, adjusts a variable delay 514 to compensate for the phase difference, and applies the adjusted delay 514 to the strobe signal DQS. The result of applying the adjusted delay 514 to the strobe signal DQS for this data line is a per-bit sample signal DQS<3>' that is approximately edge-aligned to the delayed data signal DQ<3>'.

[0050] Subsequent to or simultaneous with determining an optimal amount of variable delay in the calibration mode, the memory system begins operations in the receiver mode. **Figure 6** is a block diagram of a strobe-based memory system 199 including a strobe-offset control system 100 in the receiver mode, under an embodiment. The strobe-offset control system 100 and memory system 199 are as described above with reference to Figure 1. A memory controller or other component of the memory system 199 places the system in the receiver mode by deactivating the calibrate-enable signal.

[0051] The receiver/input sampler 102 operates as an input sampler in the receiver mode and, as such, receives a sample signal DQS' from the variable delay element. The sample signal is generated by the variable delay element by applying the offset determined during the calibration mode to the delayed strobe signal. The variable delay element outputs a per-bit sample signal DQS' to the receiver/input sampler 102 for use in sampling/receiving data of the corresponding delayed data signal DQ<X>'. The receiver/input sampler 102 outputs the sampled/received data on the data lines 112.

[0052] **Figure 7** is a timing diagram 700 showing adjustment of strobe signal timing using an optimal per-bit variable delay along with a fixed delay to generate a per-bit strobe signal with optimal alignment for sampling a corresponding data signal, under an embodiment. One data signal DQ<0> is shown as an example only, as the methods described herein are similarly applied to all data lines DQ<X>. As described above, the strobe-offset control system receives the strobe signal DQS from the memory devices along with the data signal DQ<0>. Due to system offsets and pin-to-pin offsets in the memory devices there is an edge-alignment offset 702 between the strobe signal DQS and the received data signal DQ<0>.

[0053] Applying a fixed delay 704 of approximately 90 degrees to the received data signal DQ<0> as described above produces delayed data signal DQ<0>'. During the calibration mode, as described above, the delayed data signal DQ<0>' is compared to the received strobe signal DQS and information of phase/timing differences detected during this process result in adjustment and subsequent application of a variable delay 706 to the received strobe signal DQS. Application of the variable delay 706 to the strobe signal DQS results in per-bit sample signal DQS<0>' (without a fixed delay).

The variable delay 706 is approximately equal to the edge-alignment offset 702 plus the fixed delay 704 applied to the data signal DQ<0>. This results in a sample signal DQS<0>' (without a fixed delay) that is approximately edge-aligned with the delayed data signal DQ<0>'.

[0054] Following adjustment of the variable delay 706 during calibration mode, a fixed delay 708 of approximately 90 degrees is applied to the strobe signal DQS along with the variable delay 706 to generate the optimal per-bit sample signal DQS<0>' for use by the receiver during normal receive operations. The per-bit sample signal DQS<0>' is optimally positioned relative to the data signal so as to maximize the probability of accurately sampling the delayed data signal DQ<0>'. The amount of per-pin offset that is correctable using the systems and methods herein is the maximum delay difference between the delay available from the variable delay element 130 and the data delay element 150 (Figure 1). The optimal alignment provided by the systems/methods herein, therefore, overcomes some if not all effects due to system/pin-to-pin offsets.

[0055] As described above with reference to **Figure 1**, the strobe-offset control system 100 includes data delay elements and strobe delay elements for applying fixed delays to the received data signals and strobe signals, respectively. The strobe-offset control system 100 of another embodiment therefore includes one or more delay element control circuits or controllers for use in controlling tolerances of the delays provided by the strobe and data delay elements.

[0056] **Figure 8** is a block diagram of a strobe-based memory system 199 including a strobe-offset control system 800 for individual data line strobe-offset control, under an

embodiment. The delay element control circuit 880 generates control signals 882 for use in controlling nominal values of the strobe delay element 160, and /or the data delay element 150, and/or the variable delay element 130. While a single delay element control circuit 880 is described below as controlling both the strobe 160 and data 150 delay elements, alternative embodiments can use separate delay element control circuit for each delay element, each type of delay element or for different combinations of delay elements.

[0057] **Figure 9** is a block diagram of a delay element control circuit 880 for use in strobe-based memory controllers, under an embodiment. The delay element control circuit 880 controls the respective delays or offsets within a pre-specified range in response to variations in operating or environmental parameters of the host system, memory controller, and/or strobe-offset control system. The operating parameters include, for example, the speed of operation, but can include numerous other parameters as appropriate. The environmental parameters include, for example temperature and/or power supply voltage, but can include numerous other parameters as appropriate.

[0058] The delay element control circuit 880 of an embodiment includes a delay line 902, a phase detector 904, and a delay line controller 906. The delay line 902 includes four unit delay elements DE1, DE2, DE3, and DE4 coupled in series and receiving the memory system clock signal 910 as an input; alternative embodiments can include any number of unit delay elements. The delay line 902 provides a total delay that is approximately one period of the memory system clock. Therefore, each of the four unit delay elements DE1-DE4 delays the input clock signal 910 by an amount that is one-fourth of the memory system clock period.

[0059] The delay line output couples to the phase detector 904 along with the memory system clock signal 910. The phase detector 904 determines any phase difference between these two input signals and outputs control signals 914 to the delay line controller 906 that include information of the detected phase difference. The delay line controller 906 in turn outputs control signals 882 for use in controlling timing offsets of one or more of the unit delay elements DE1-DE4 in response to the information from the phase detector 904. The delay line controller output signals 882 are also used as control signals for use in setting the nominal delay value of delay elements like the strobe delay element 106, the data delay element 150, and the variable delay element 130. The delay line controller output signals 882 can be any of a variety of signal types known in the art, such as voltage bias signals, current bias signals, or digital delay-control signals. The offsets of the delay elements are controlled within a pre-specified range in response to variations in operating parameters described above.

[0060] The strobe-offset control systems described above can be used in numerous memory system types/configurations. As an alternative example, **Figure 10** is a block diagram of a strobe-offset control system 1000 for individual data line strobe-offset control in strobe-based DDR memory systems 1099, under an alternative embodiment of Figure 1. As described above, the DDR memory system 1099 transfers data from the memory devices 190 on both the rising and falling edge of the strobe signal DQS. Consequently, the DDR memory system 1099 is similar to the strobe-based memory system 199 described above with reference to **Figure 1** except for an additional receiver/input sampler 102F that samples/receives data on the falling edge of the sample signal DQS'. Likewise, the strobe-offset control system 1000 is similar to the strobe-

offset control system 100 described above with reference to **Figure 1** except for an additional coupling of the variable delay element output signal DQS' to the falling-edge receiver/input sampler 102F.

[0061] The strobe-based DDR memory system 1099 includes a rising-edge receiver/input sampler 102R and a falling-edge receiver/input sampler 102F both having data inputs coupled to receive a delay data signal DQ<X>' that has been delayed by a data delay element 150. The data signal DQ includes information of one data bit of a data byte transferred between the receivers/input samplers 102R/102F and one or more memory devices 190 via one or more buses 170. The rising-edge receiver/input sampler 102R and falling-edge receiver/input sampler 102F both receive sample signal DQS' from the variable delay element 130. The rising-edge receiver/input sampler 102R samples the data signal DQ<X> in response to the sample signal DQS' 106 as described above and outputs data signal 112R that includes data DATAR<0:N>. The falling-edge receiver/input sampler 102F samples the data signal DQ<X> in response to the sample signal DQS' 106 as described above and outputs data signal 112F that includes data DATAF<0:N>.

[0062] Components of the strobe-offset control system 1000 include a calibration control circuit 120, a variable delay element 130, and a multiplexer 140, but can include and/or couple with additional components as appropriate to the memory system 1099 or host electronic system. The strobe-offset control system 1000 and its various components operate during data transfer operations as described above with reference to **Figures 1-7**.

[0063] Another alternative example of a strobe-offset control system provides separate strobe-offset control for rising and falling edges of the strobe signal DQS.

Figure 11 is a block diagram of a control system 1100 for individual data line rising and falling edge strobe-offset control in strobe-based DDR memory controllers 1199, under an alternative embodiment of Figure 10. As described previously, the DDR memory system 1199 transfers data from the memory devices on both the rising and falling edge of the strobe signal DQS. Consequently, the DDR memory system 1199 is similar to the strobe-based memory system 199 described above with reference to **Figure 1** except for an additional receiver. The strobe-based DDR memory system 1199 thus includes a rising-edge receiver/input sampler 102R and a falling-edge receiver/input sampler 102F both having data inputs coupled to receive a data signal DQ<X>' that has been delayed by a data delay element 150. The rising-edge receiver/input sampler 102R samples data on the rising edge of a sample signal DQS(R)' while the falling-edge receiver/input sampler 102F samples data on the falling edge of a sample signal DQS(F)'. The data signal DQ includes information of one bit of a data byte transferred between each of receiver/input sampler 102R/102F and one or more memory devices (not shown). The rising-edge receiver/input sampler 102R samples the data signal DQ<X> in response to the sample signal DQS(R)' as described above and outputs data signal 112R that includes data DATAR<0:N>. The falling-edge receiver/input sampler 102F samples the data signal DQ<X> in response to the sample signal DQS(F)' as described above and outputs data signal 112F that includes data DATAF<0:N>.

[0064] The strobe-offset control system 1100 is similar to the strobe-offset control system 100 described above with reference to **Figure 1** except that it includes additional

components that provide separate strobe-offset control for the rising and falling edges of the strobe signal DQS. The rising-edge strobe-offset control components (generally indicated with suffix “R”) include a calibration or offset controller 120R, a variable delay element 130R, and a multiplexer 140R along with corresponding signals 132R, 124R, and 112R, as described above with reference to Figure 1. Likewise, the falling-edge strobe-offset control components (generally indicated with suffix “F”) include a calibration or offset controller 120F, a variable delay element 130F, and a multiplexer 140F along with corresponding signals 132F, 124F, and 112F, as described above with reference to Figure 1. The strobe-offset control system 1100 can include and/or couple with additional components as appropriate to the memory system 1199 or host electronic system. The strobe-offset control system 1100 operates during data transfer operations as described above with reference to **Figures 1-7**.

[0065] As described above with reference to **Figure 1** for example, the calibration control circuit 120 of an embodiment uses information of one or more signals received from the receiver 102 in performing adjustments of the variable delay value of delay element 130. **Figure 12** is a block diagram of a calibration control circuit 120, under an embodiment. The calibration control circuit 120 receives an up/down adjustment control signal 114 that is a digital representation of the difference in phase between the strobe signal and the data signal as detected by the receiver. A flip-flop 1204 couples the control signal to an N-bit counter 1202, but the embodiment is not so limited. The calibration control circuit 120 can also receive an optional adjustment valid signal 116 from the receiver that indicates when the adjustment control signal 114 is valid. The

adjustment valid signal, when included, is coupled to the N-bit counter 1202 via flip-flop 1206 in an embodiment.

[0066] In response to phase difference information of the adjustment control signal 114 the N-bit counter 1202 accumulates the up/down adjustment and generates the delay control signal 124 as appropriate to the detected phase difference. The delay control signal 124 couples to adjust the variable delay value of delay element 130 up or down as appropriate to the detected phase difference.

[0067] The calibration control circuit 120 also includes optional circuitry 1210 for detecting a dither condition between the phase of the strobe signal and the data signal as detected by the receiver when the phase of the strobe signal is approximately the same as the phase of the data signal. In response to detecting the dither condition, the circuitry 1210 enables the optional lock signal 126. The lock signal 126 is subsequently output (to the memory controller or other circuitry of the memory system 199) by the calibration control circuit 120 to indicate detected phase alignment of the strobe and data signals.

[0068] The N-bit counter 1202 can be replaced by a charge pump in an alternative embodiment of the calibration control circuit 120. As one example, **Figure 13** shows a charge pump 1300 that can replace the N-bit counter 1202, under an embodiment. This charge pump 1300 includes current sources I1 and I2 selectively switched to a capacitor C via one of a control (up) signal/transistor Tu or a control (down) signal/transistor Td. Alternative charge pump circuits can be used.

[0069] In operation, the calibration control circuit 120 receives an up/down adjustment control signal 114 that represents the difference in phase between the strobe

signal and the data signal as detected by the receiver. Information of the adjustment control signal 114 is used to provide the control (up) signal to the gate of transistor Tu and to provide the control (down) signal to the gate of transistor Td.

[0070] In operation, when the control (up) signal is enabled (and the control (down) signal is disabled), transistor Tu causes a first current source I1 to deliver charge onto capacitor C. In contrast, when the control (down) signal is enabled (and the control (up) signal is disabled), transistor Td causes a second current source I2 to sink current with a subsequent decrease in charge on capacitor C. In this manner the charge stored on the capacitor C is representative of the up or down adjustment applied to the variable delay value in response to the detected phase difference between the strobe and data signals. The charge pump 1300 outputs an analog control voltage V_{out} for use in generating the delay control signal 124 (**Figure 1**) as appropriate to the detected phase difference. The delay control signal 124 couples to adjust the variable delay value (delay element 130) up or down as appropriate to the detected phase difference, as described above.

[0071] The components of the memory systems described above include any collection of computing components and devices operating together. The components of the memory systems can also be components or subsystems within a larger computer system or network. The memory system components can also be coupled among any number of components (not shown), for example other buses, controllers, memory devices, and data input/output (I/O) devices, in any number of combinations. Many of these system components may be soldered to a common printed circuit board (for example, a graphics card or game console device), or may be integrated in a system that includes several printed circuit boards that are coupled together in a system, for example,

using connector and socket interfaces such as those employed by personal computer motherboards and dual inline memory modules (“DIMM”). In other examples, complete systems may be integrated in a single package housing using a system in package (“SIP”) type of approach. Integrated circuit devices may be stacked on top of one another and utilize wire bond connections to effectuate communication between chips or may be integrated on a single planar substrate within the package housing.

[0072] Further, functions of the memory system components can be distributed among any number/combination of other processor-based components. The memory systems described above include, for example, various dynamic random access memory (DRAM) systems. As examples, the DRAM memory systems can include double data rate (“DDR”) systems like DDR SDRAM as well as DDR2 SDRAM and other DDR SDRAM variants, such as Graphics DDR (“GDDR”) and further generations of these memory technologies, i.e., GDDR2, and GDDR3, but is not limited to these memory systems.

[0073] Aspects of the system for per-bit offset control and calibration described herein may be implemented as functionality programmed into any of a variety of circuitry, including programmable logic devices (PLDs), such as field programmable gate arrays (FPGAs), programmable array logic (PAL) devices, electrically programmable logic and memory devices and standard cell-based devices, as well as application specific integrated circuits (ASICs). Some other possibilities for implementing aspects of the per-bit offset control and calibration system include: microcontrollers with memory (such as electronically erasable programmable read only memory (EEPROM)), embedded microprocessors, firmware, software, etc. Furthermore,

aspects of the per-bit offset control and calibration system may be embodied in microprocessors having software-based circuit emulation, discrete logic (sequential and combinatorial), custom devices, fuzzy (neural) logic, quantum devices, and hybrids of any of the above device types. Of course the underlying device technologies may be provided in a variety of component types, e.g., metal-oxide semiconductor field-effect transistor (MOSFET) technologies like complementary metal-oxide semiconductor (CMOS), bipolar technologies like emitter-coupled logic (ECL), polymer technologies (e.g., silicon-conjugated polymer and metal-conjugated polymer-metal structures), mixed analog and digital, etc.

[0074] Unless the context clearly requires otherwise, throughout the description and the claims, the words “comprise,” “comprising,” and the like are to be construed in an inclusive sense as opposed to an exclusive or exhaustive sense; that is to say, in a sense of “including, but not limited to.” Words using the singular or plural number also include the plural or singular number respectively. Additionally, the words “herein,” “hereunder,” “above,” “below,” and words of similar import refer to this application as a whole and not to any particular portions of this application. When the word “or” is used in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list and any combination of the items in the list.

[0075] The above description of illustrated embodiments of the system for per-bit offset control and calibration is not intended to be exhaustive or to limit the system to the precise form disclosed. While specific embodiments of, and examples for, the system for per-bit offset control and calibration are described herein for illustrative

purposes, various equivalent modifications are possible within the scope of the system, as those skilled in the relevant art will recognize. The teachings of the system for per-bit offset control and calibration provided herein can be applied to other processing systems, not only for the systems described above.

[0076] The elements and acts of the various embodiments described above can be combined to provide further embodiments. These and other changes can be made to the system for per-bit offset control and calibration in light of the above detailed description.

[0077] In general, in the following claims, the terms used should not be construed to limit the system for per-bit offset control and calibration to the specific embodiments disclosed in the specification and the claims, but should be construed to include all processing systems that operate under the claims to provide per-bit offset control and calibration. Accordingly, the system for per-bit offset control and calibration is not limited by the disclosure, but instead the scope of the system is to be determined entirely by the claims.

[0078] While certain aspects of the system for per-bit offset control and calibration are presented below in certain claim forms, the inventor contemplates the various aspects of the system in any number of claim forms. For example, while only one aspect of the system is recited as embodied in computer-readable medium, other aspects may likewise be embodied in computer-readable medium. Accordingly, the inventor reserves the right to add additional claims after filing the application to pursue such additional claim forms for other aspects of the system for per-bit offset control and calibration.

Claims

What is claimed is:

1. An integrated circuit (IC) memory controller comprising:
 - a first interface circuit corresponding to a first input/output (I/O) pin, the first I/O pin to receive a first data signal accompanied by a strobe signal;
 - a first alignment circuit to impart a delay to at least one of the first data signal and the strobe signal, the first alignment circuit including a first data delay circuit to delay the first data signal by a first delay corresponding to a first predetermined delay value;
 - a second interface circuit corresponding to a second input/output (I/O) pin, the second I/O pin to receive a second data signal accompanied by the strobe signal;
 - a second alignment circuit to impart a delay to at least one of the second data signal and the strobe signal, the second alignment circuit including a second data delay circuit to delay the second data signal by a second delay corresponding to a second predetermined delay value that is independent of the first predetermined delay value.
2. The IC memory controller according to claim 1, further comprising storage to store each of the first and second predetermined delay values.
3. The IC memory controller according to claim 1, embodied as a field programmable gate array (FPGA) device.
4. The IC memory controller according to claim 1, further comprising a strobe I/O pin to receive the strobe signal.
5. The IC memory controller according to claim 1, wherein:
 - each of the first and second data delay circuits comprise locked-loop circuits having plural serially connected delay elements.

6. The IC memory controller according to claim 1, further comprising a calibration strobe delay circuit to impart a calibrated delay to the strobe signal.
7. The IC memory controller according to claim 5, wherein the first and second predetermined delay values correspond to respective selected delay elements of the first and second data delay circuits to impart the respective delays to the first and second data signals.
8. The IC memory controller according to claim 1, further comprising:
 - a first timing signal delay circuit associated with the first I/O circuit; and
 - a second timing signal delay circuit associated with the second I/O circuit;wherein each of the first and second timing signal delay circuits impart independently determined first and second timing signal delays to the strobe signal.
9. The IC memory controller according to claim 1, further comprising a calibration circuit to, in a calibration mode, determine the first and second predetermined delay values.
10. A method of operation in an IC memory controller, the method comprising:
 - in a receiving mode,
 - receiving first and second data signals from a memory device at respective first and second I/O pins, the first and second data signals accompanied by a strobe signal;
 - aligning the received first and second data signals with the strobe signal, the aligning comprising
 - imparting a first delay to at least one of the first data signal and the strobe signal, the first delay corresponding to a first predetermined delay value,
 - imparting a second delay to at least one of the second data signal and the strobe signal, the second delay corresponding to a second predetermined delay value that is independent of the first predetermined delay value.

11. The method according to claim 10, further comprising:
 - in a calibration mode,
 - determining the first and second predetermined delay values; and
 - storing the first and second predetermined delay values.
12. The method according to claim 11, wherein:
 - during the receiving mode,
 - the imparting the first and second delays includes retrieving the stored first and second predetermined delay values.
13. The method according to claim 12, wherein:
 - the first and second data signals are delayed by the first and second predetermined delay values.
14. The method according to claim 11, further comprising:
 - during the calibration mode,
 - calibrating a timing signal delay value corresponding to a delay for application to the strobe signal.
15. The method according to claim 14, further comprising:
 - during the calibration mode,
 - storing the calibrated timing delay value.
16. A Field Programmable Gate Array (FPGA) device comprising:
 - a memory controller interface, the memory controller interface including data I/O pins and at least one strobe pin, the data I/O pins to receive respective data signals, the at least one strobe pin to receive at least one strobe signal that accompanies the data signals;
 - calibration circuitry to, in a calibration mode, determine delay values corresponding to delays to impart to, for each I/O pin, at least one of a received data signal and the strobe signal to align the data and strobe signals for data sampling

operations, each I/O pin associated with a given delay value, wherein each of the delay values are determined independently of each other;

alignment circuits corresponding to each data I/O pin, each alignment circuit including delay circuitry responsive to a given determined delay value;

storage to store the determined delay values;

wherein during a receiving mode, the memory controller interface retrieves the stored determined delay values for each alignment circuit.

17. The FPGA according to claim 16, wherein the calibration circuitry determines a timing signal delay to impart to the at least one strobe signal.

18. The FPGA according to claim 17, wherein each alignment circuit includes a timing signal delay circuit responsive to the determined timing signal delay.

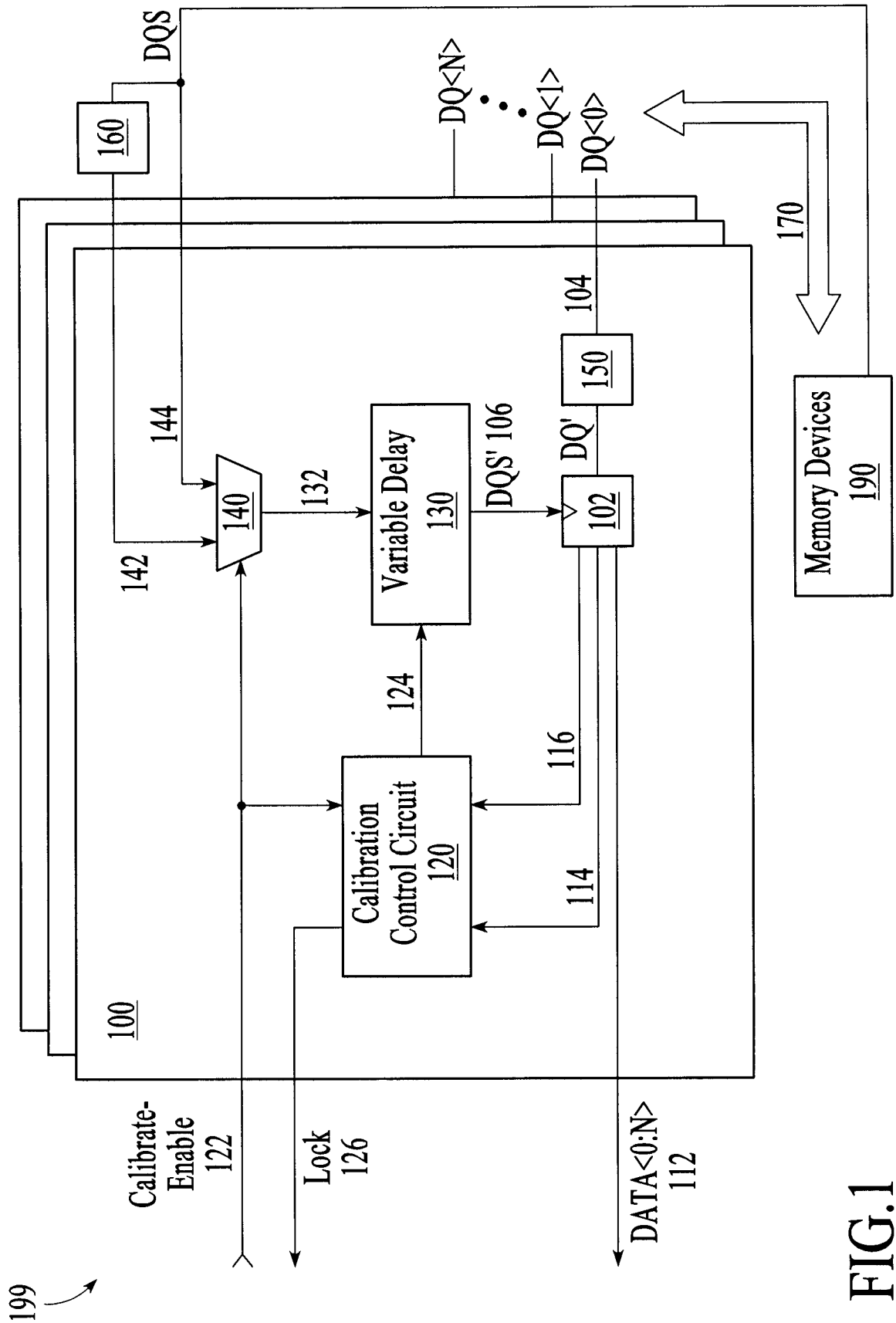
19. The FPGA according to claim 16, wherein the alignment circuits include respective locked-loop circuits responsive to different ones of the determined delay values.

20. The FPGA according to claim 19, wherein the calibration circuitry includes a calibration strobe delay circuit to impart a calibrated delay to the strobe signal.

Strobe-Offset Control Circuit

ABSTRACT

A method of operation in a memory controller is disclosed. The method includes receiving a strobe signal having a first phase relationship with respect to first data propagating on a first data line, and a second phase relationship with respect to second data propagating on a second data line. A first sample signal is generated based on the first phase relationship and a second sample signal is generated based on the second phase relationship. The first data signal is received using a first receiver clocked by the first sample signal. The second data signal is received using a second receiver clocked by the second sample signal.



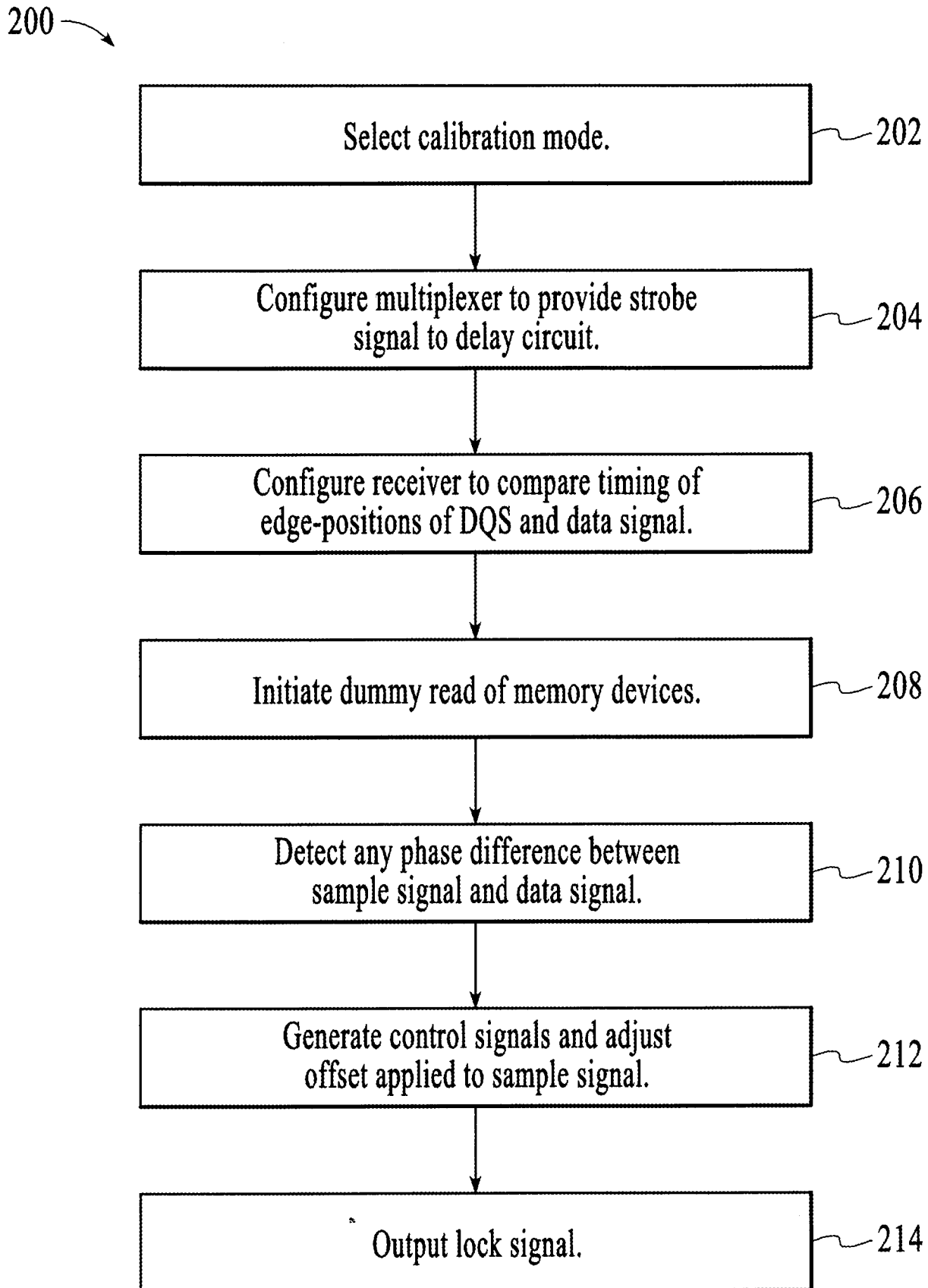


FIG.2

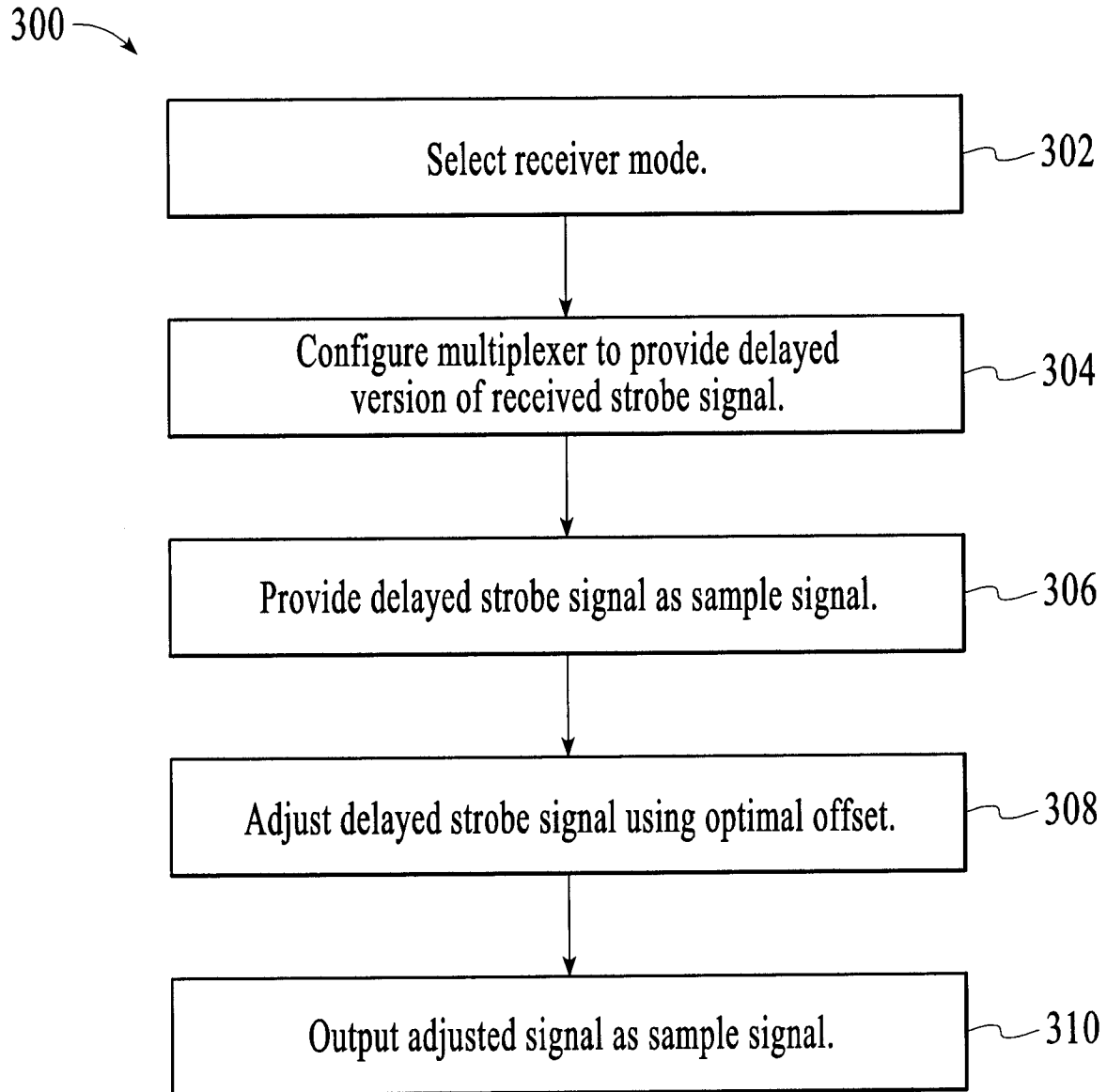


FIG.3

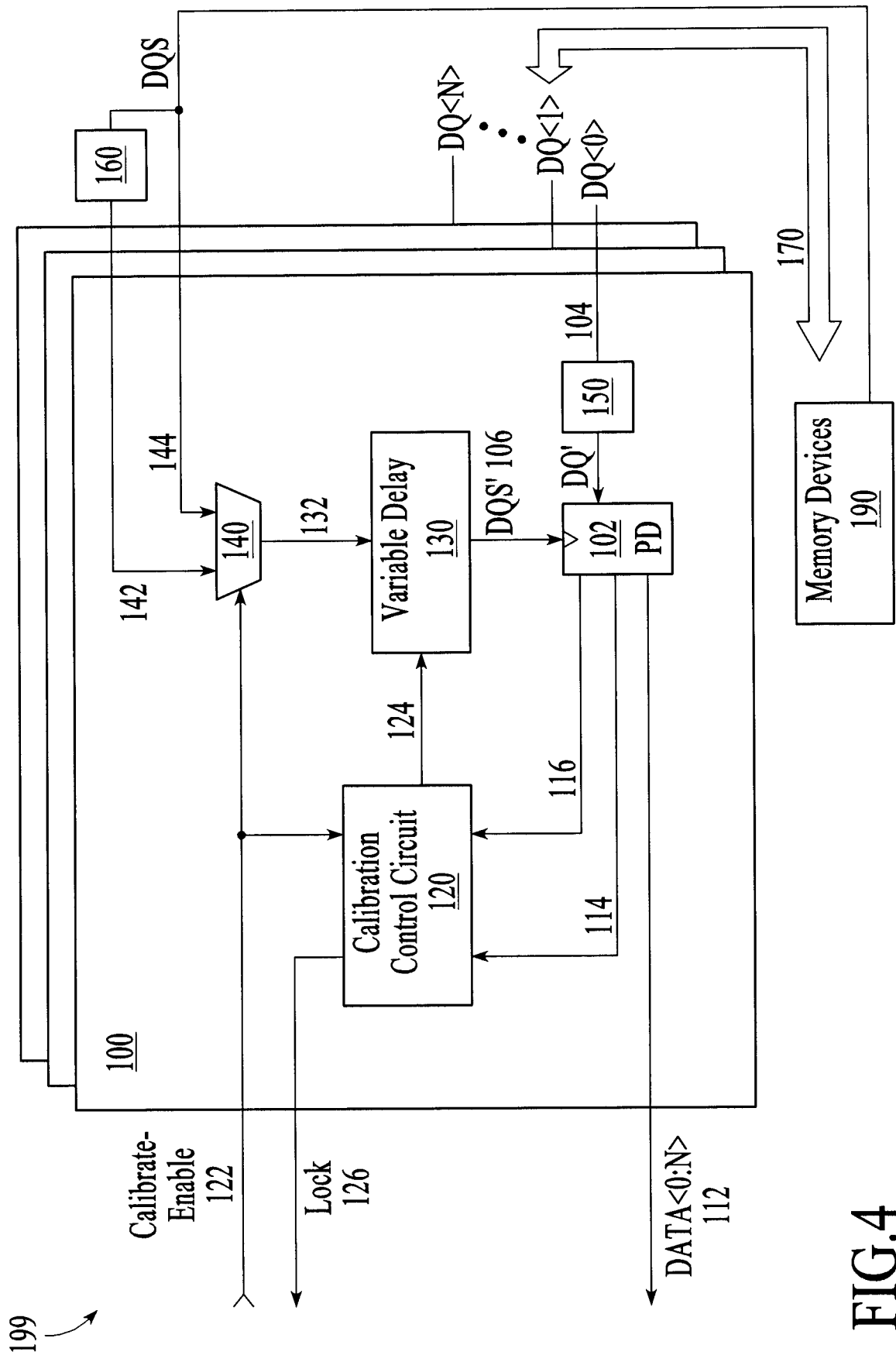


FIG. 4

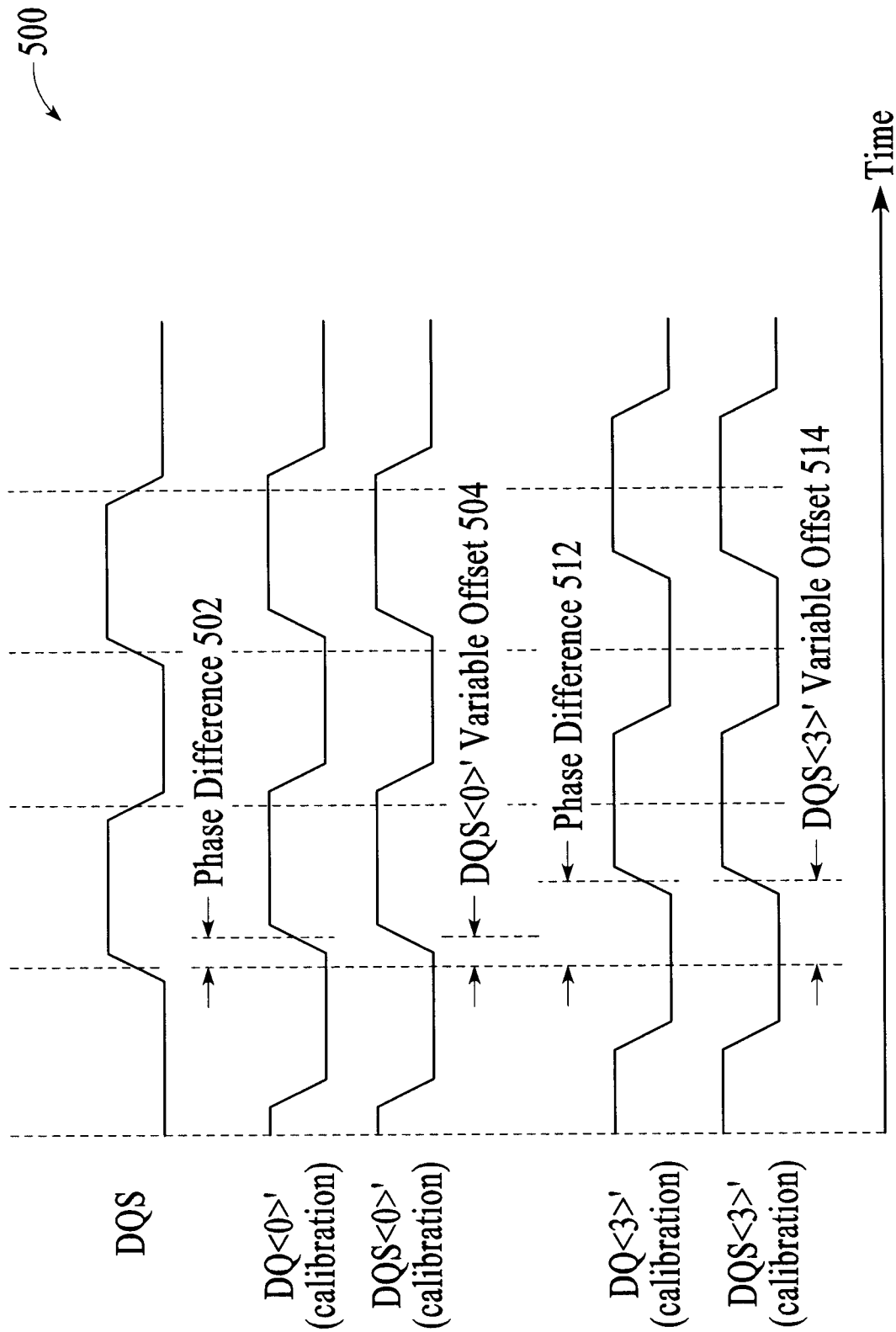


FIG.5

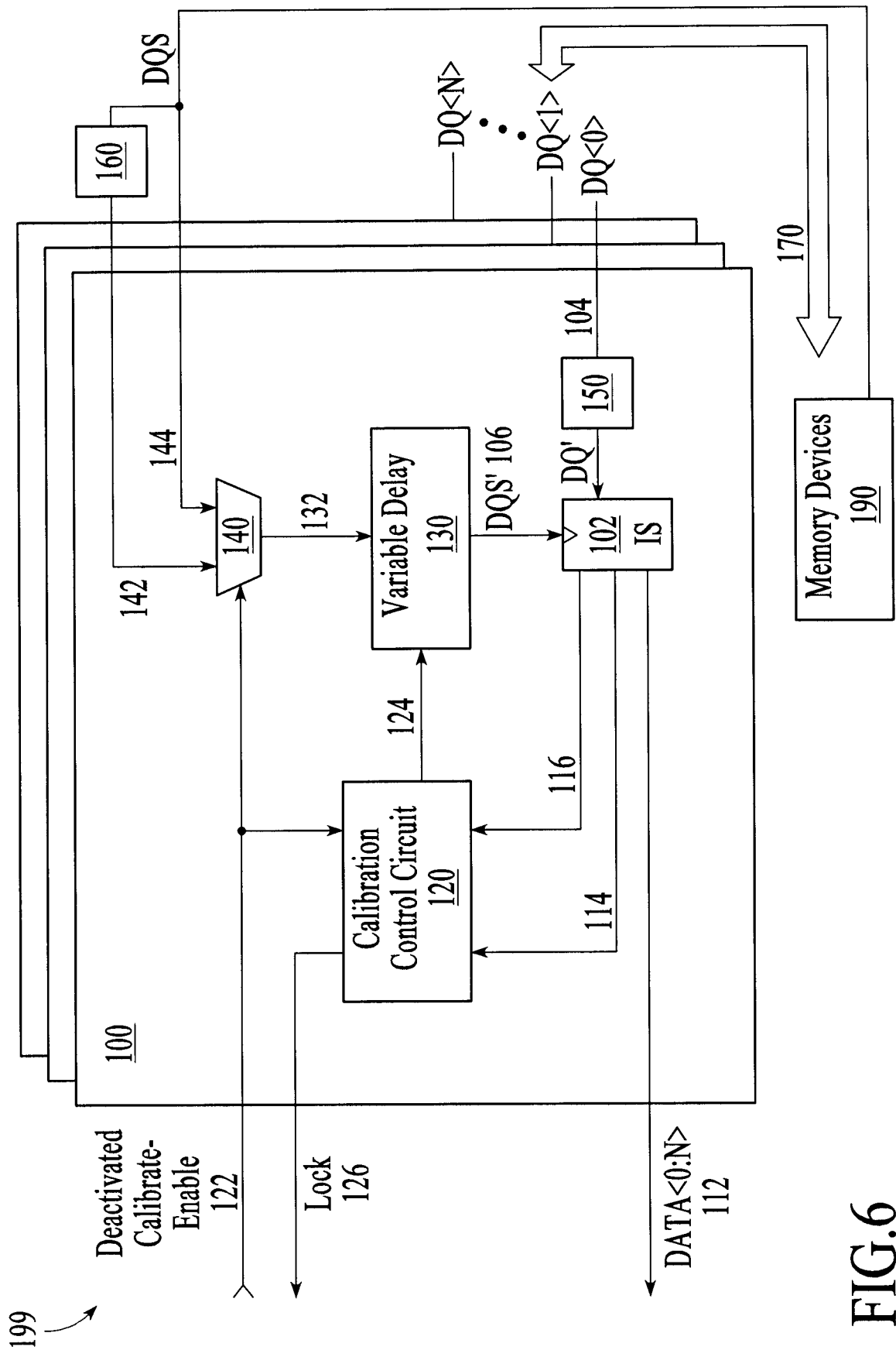


FIG. 6

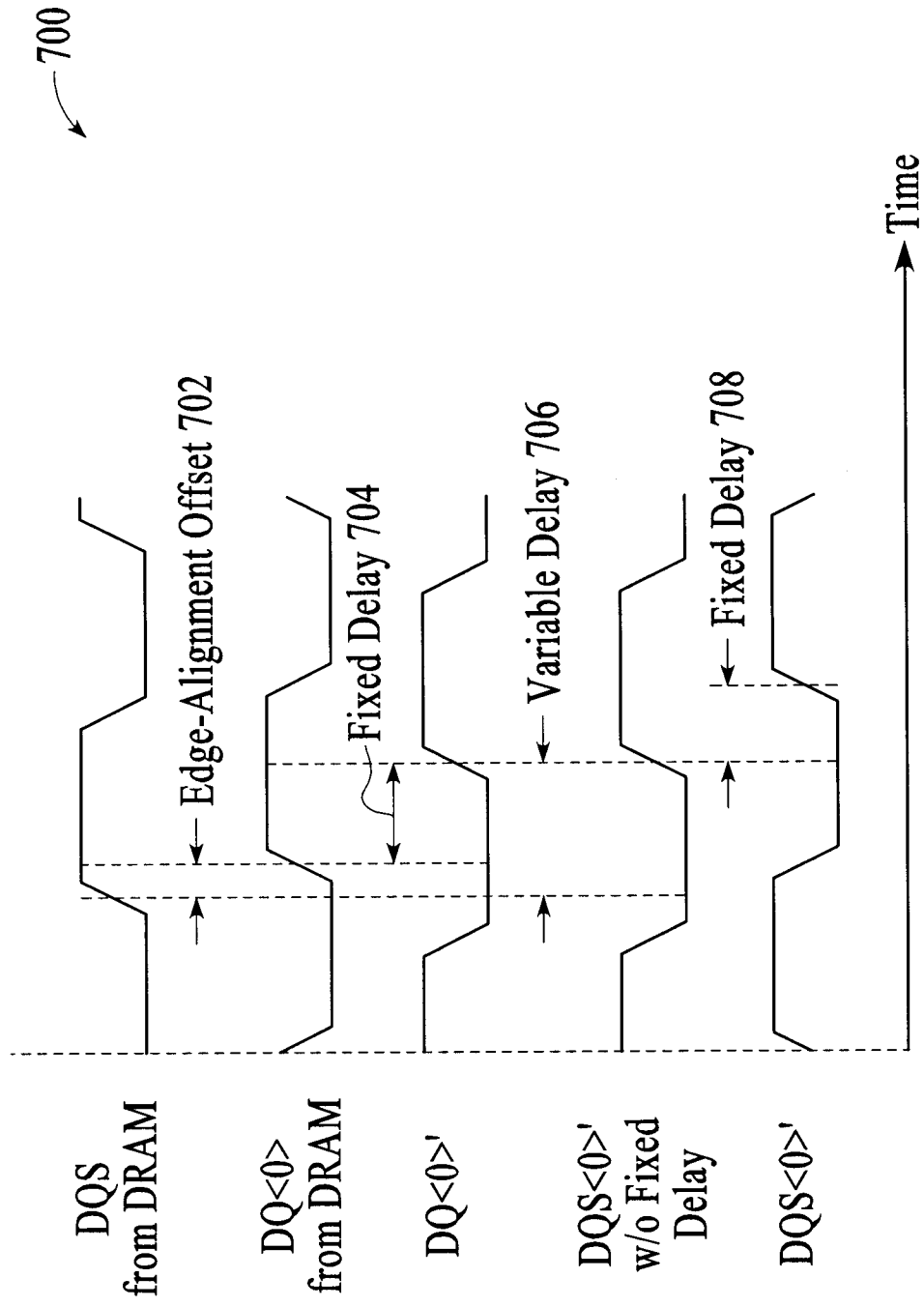


FIG.7

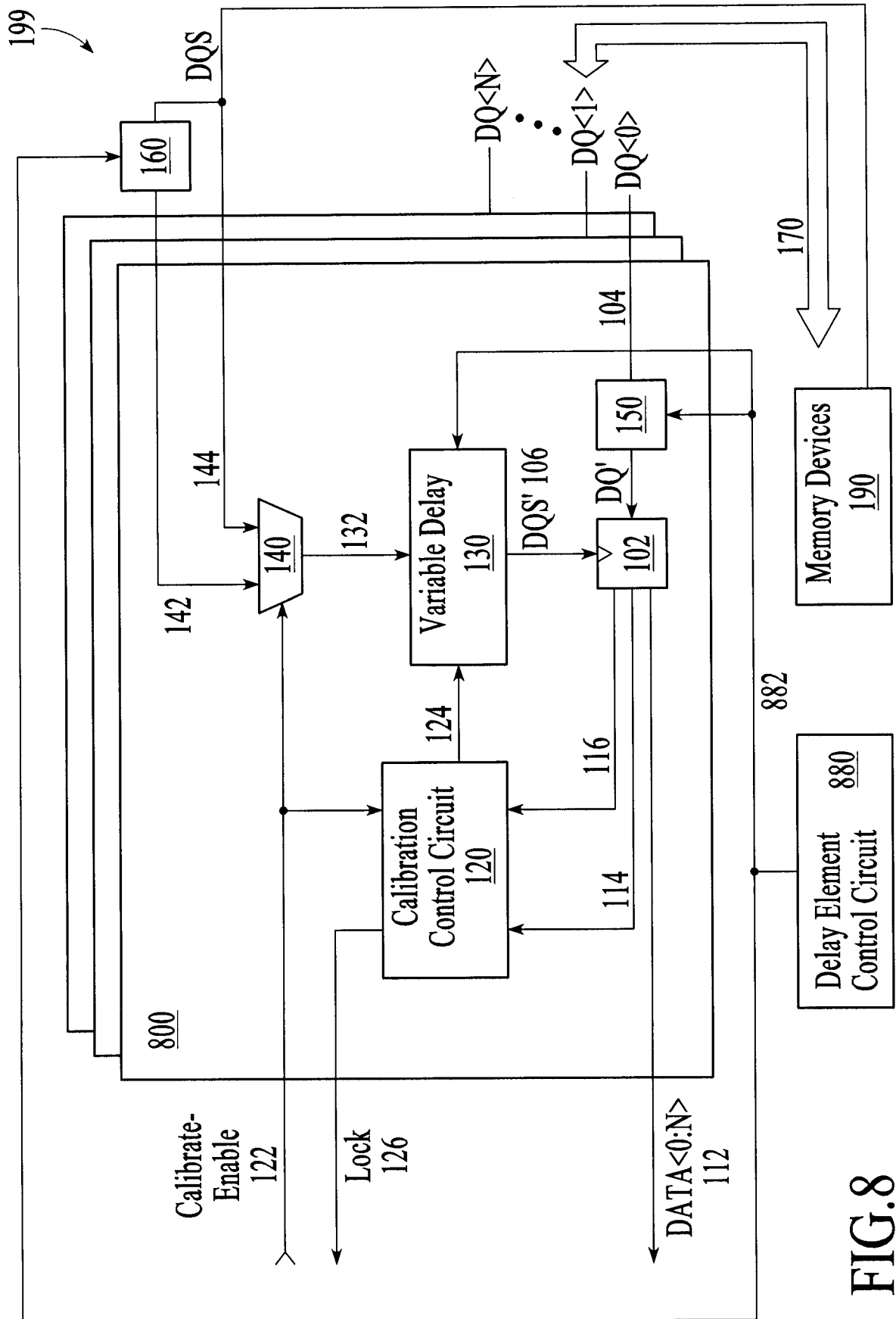


FIG. 8

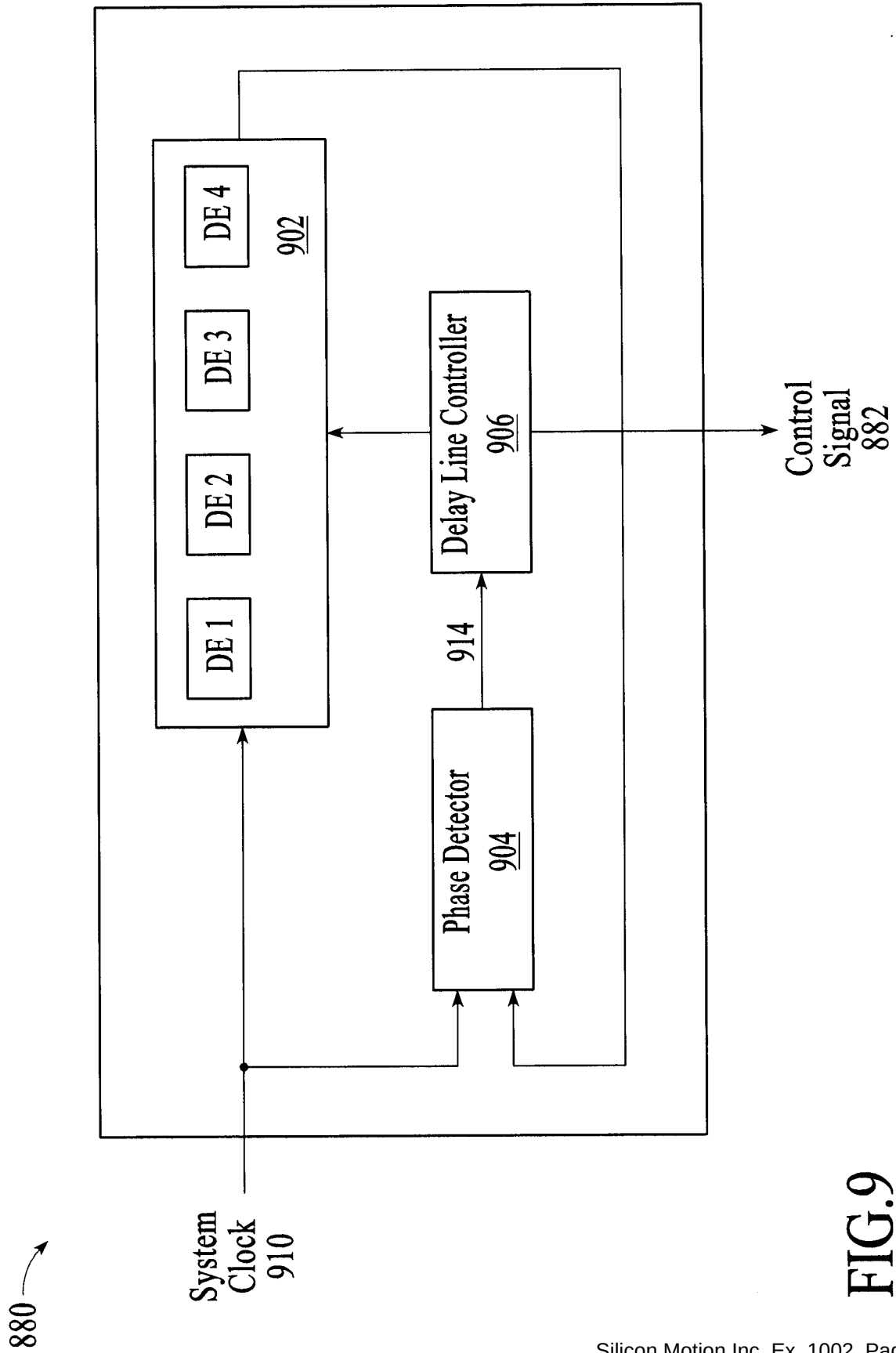
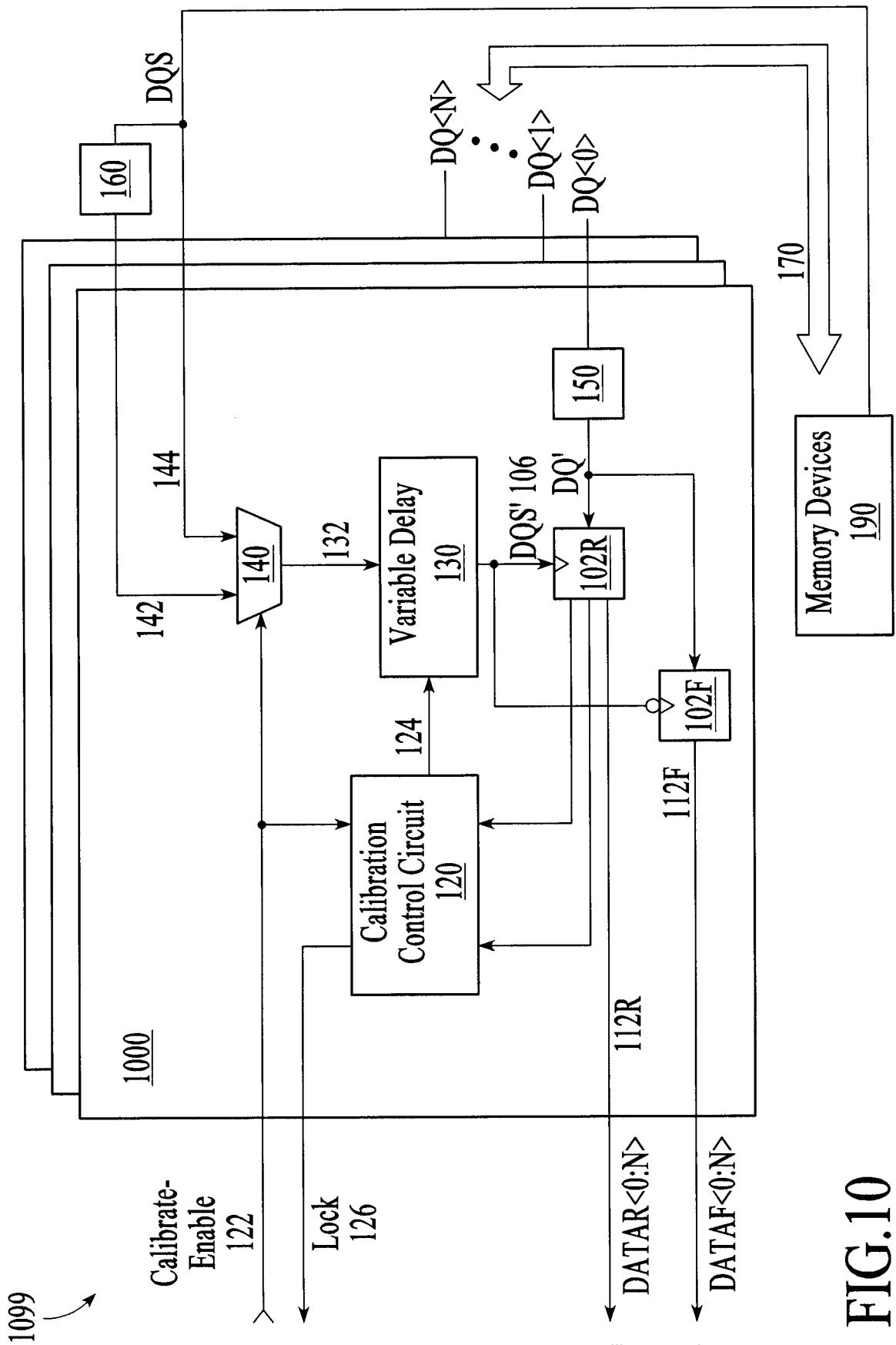


FIG.9



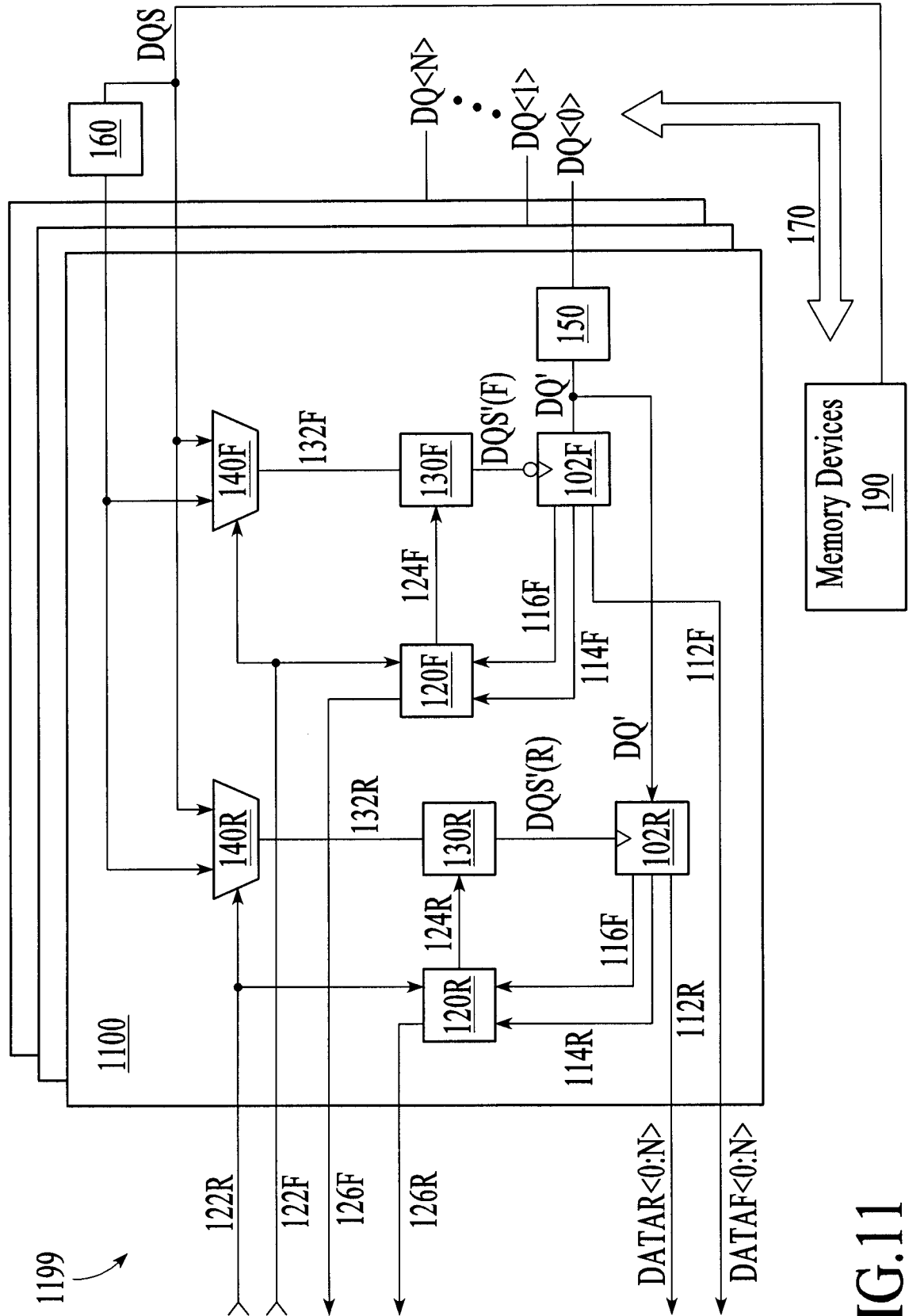


FIG.11

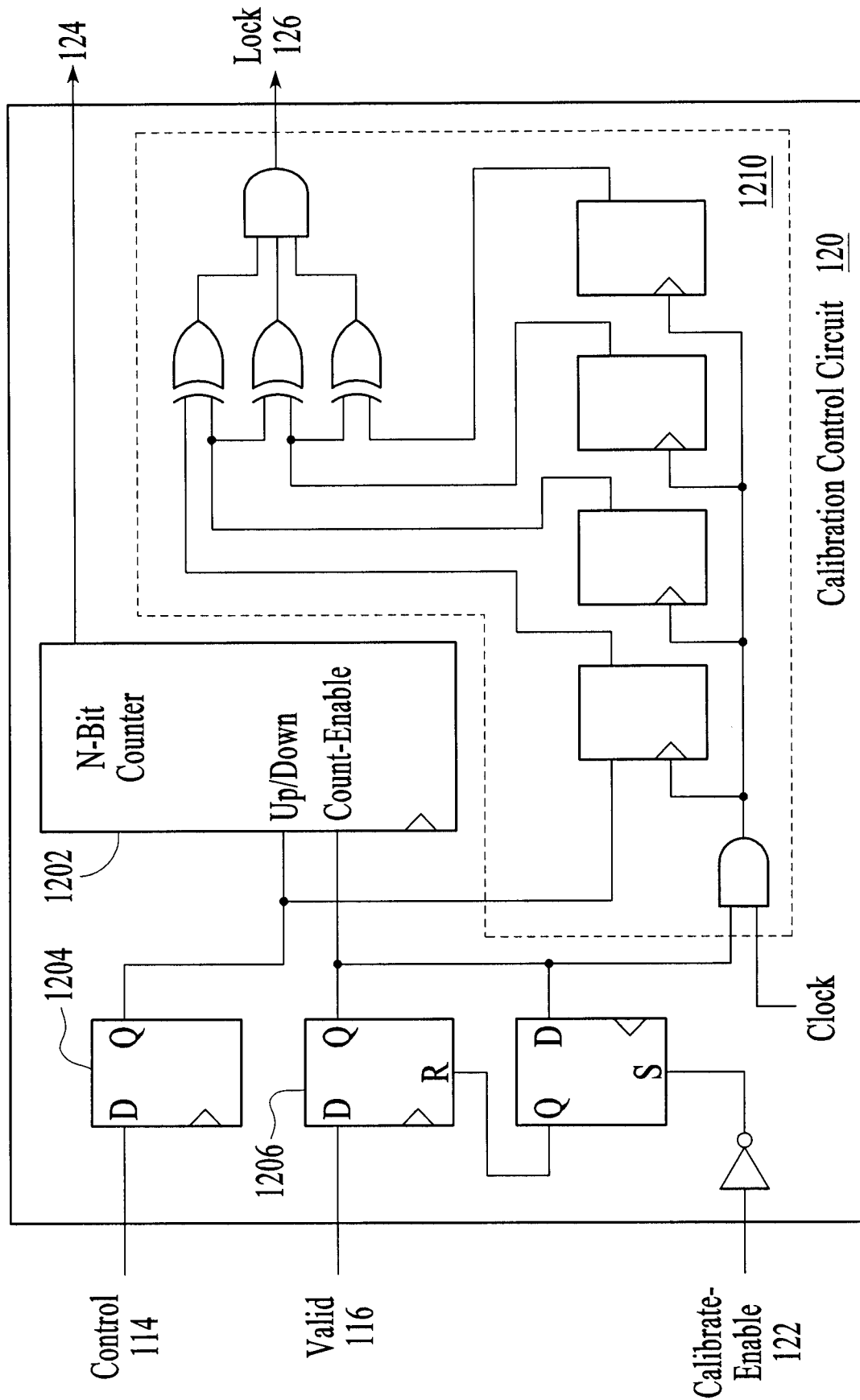


FIG.12

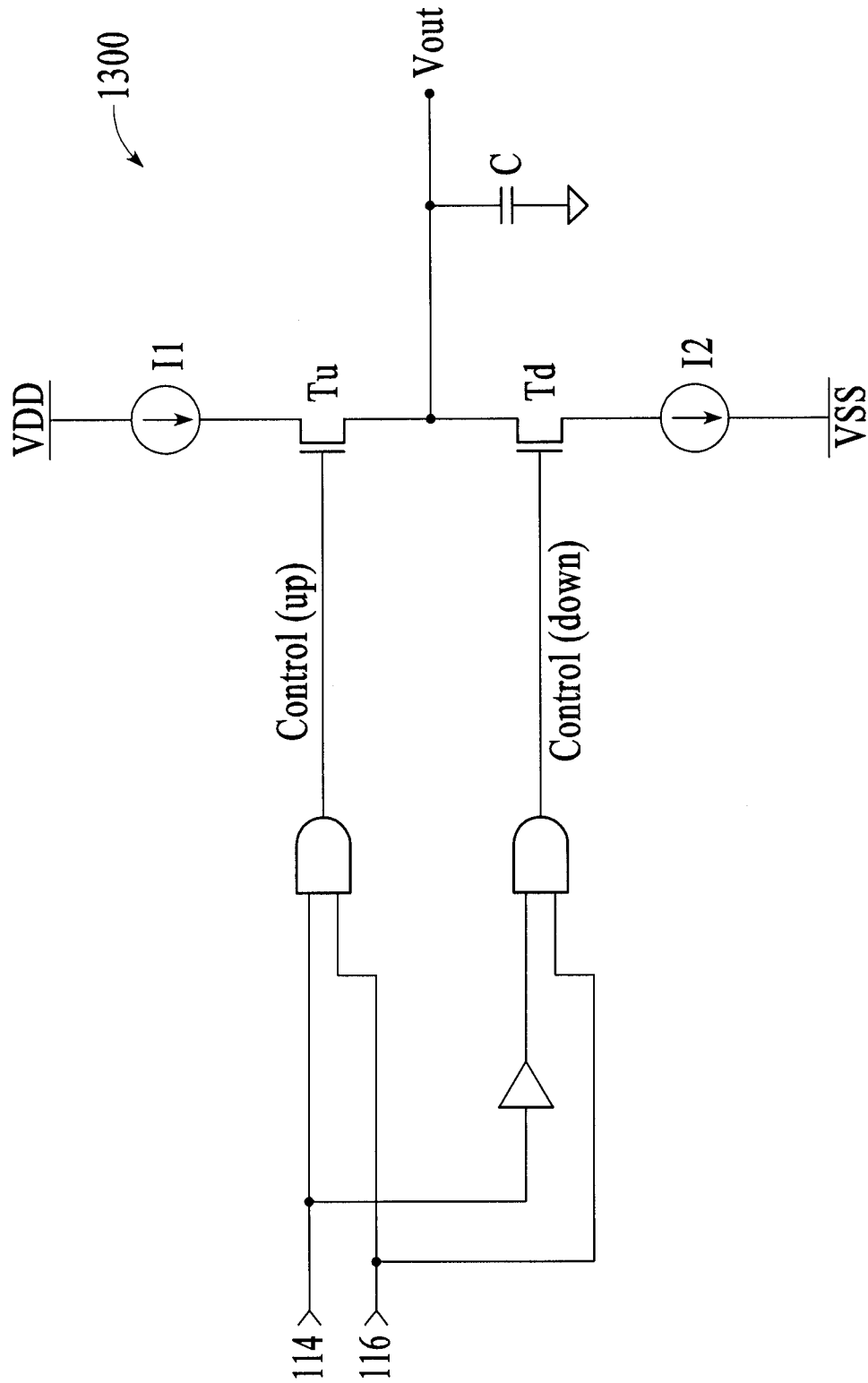


FIG.13

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: Scott C. BestApplication No./Patent No.: Unassigned Filed/Issue Date: Herewith (March 31, 2014)Titled: STROBE-OFFSET CONTROL CIRCUITRambus Inc., a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 015725, Frame 0507, or for which a copy thereof is attached.
- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:
1. From: _____ To: _____
- The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
2. From: _____ To: _____
- The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**

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Silicon Motion Inc. Ex. 1002, Page 134
Silicon Motion Inc. v. K. Mizra LLC, IPR2024-01241

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

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☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Lance M. Kreisman/

March 31, 2014

Signature

Date

Lance M. Kreisman

39,256

Printed or Typed Name

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in the attached transmittal letter.

- ☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

44429**OR**

- ☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

Name	Registration Number	Name	Registration Number

Please recognize or change the correspondence address for the application identified in the attached transmittal letter to:

- ☒ The address associated with the above-mentioned Customer Number.

OR

- ☐ The address associated with Customer Number:

OR

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Address

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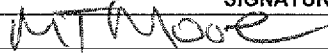
Telephone

Email

I am the Applicant:

- ☐ Inventor or Joint Inventor
- ☐ Legal Representative of a Deceased or Legally Incapacitated Inventor
- ☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign
- ☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document)

SIGNATURE of Applicant for Patent

Signature		Date	5-31-13
Name	Michael T. Moore	Telephone	408-462-8000
Title and Company	Deputy General Counsel, Intellectual Property, Rambus Inc.		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms for more than one signature, see below *.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Strobe-Offset Control Circuit		
First Named Inventor/Applicant Name:		Scott C. Best		
Filer:		Lance Martel Kreisman		
Attorney Docket Number:		RBS2.P005C5		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

Electronic Acknowledgement Receipt	
EFS ID:	18628095
Application Number:	14230558
International Application Number:	
Confirmation Number:	9057
Title of Invention:	Strobe-Offset Control Circuit
First Named Inventor/Applicant Name:	Scott C. Best
Customer Number:	44429
Filer:	Lance Martel Kreisman
Filer Authorized By:	
Attorney Docket Number:	RBS2.P005C5
Receipt Date:	31-MAR-2014
Filing Date:	
Time Stamp:	15:18:21
Application Type:	Utility under 35 USC 111(a)

Payment information:	
Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1600
RAM confirmation Number	1800
Deposit Account	506388
Authorized User	

File Listing:				
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part (if applicable) / Pages

1	Transmittal of New Application	RA356_RBS2_P005C5_Filing_Transmittal.pdf	275802 ef30edd3dd53c9f5044820254e782fa2c9eb9b1b	no	2
Warnings:					
Information:					
2	Application Data Sheet	RA356_RBS2_P005C5_ADS.pdf	1421657 5f0b58b9e75a162aed70155cf74af9ba87ed3a71	no	5
Warnings:					
Information:					
3	Specification	RA356_C1C1C1C1C1_RBS2_P005C5_Continuation.pdf	134078 de07598461c4c17690cabe4866297310dd37d092	no	34
Warnings:					
Information:					
4	Drawings-only black and white line drawings	RA356_RBS2_P005C5_Drawings.pdf	2438950 6435a9d9afaa8bdb8e567a93ec5b2e4ca2b28526	no	13
Warnings:					
Information:					
5	Transmittal Letter	RA356_RBS2_P005C5_373.pdf	118102 5f90f7c651c0ccd8a5338ce283254f428d800db1	no	3
Warnings:					
Information:					
6	Power of Attorney	RA356_RBS2_P005C5_POA_MM.pdf	98485 ba6a1b26f85ed5b042298aed09c180385177ad85	no	1
Warnings:					
Information:					
7	Fee Worksheet (SB06)	fee-info.pdf	32635 4af74318fd062fa07bc52c7e1b4d1fc7c42944f2	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			4519709		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.