

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Silicon Motion Inc.

Petitioner,

v.

K.Mizra, LLC

Patent Owner.

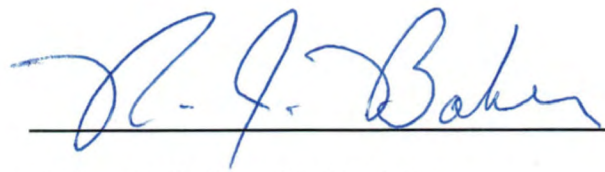
Case No. IPR2024-01241
U.S. Patent No. 9,111,608

**DECLARATION OF DR. R. JACOB BAKER, PH.D,
IN SUPPORT OF SILICON MOTION'S
PETITION FOR *INTER PARTES* REVIEW OF
CLAIMS 1-2, 4-15 OF U.S. PATENT NO. 9,111,608**

I declare under penalty of perjury that the following is true and correct. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on August 8, 2024

Las Vegas, NV



R. Jacob Baker, Ph.D., P.E.

I, R. Jacob Baker, Ph.D., P.E., declare as follows:

1. I have been retained on behalf of Silicon Motion Inc. (“Petitioner”) to provide expert opinions in connection with the *Inter Partes* Review (“IPR”) of U.S. Patent 9,111,608 (“the ‘608 Patent”).
2. I am being compensated for my time in connection with this IPR at my standard consulting rate for consulting services. My compensation is not affected by the outcome of this matter.
3. I have been asked to provide my opinions regarding whether Claims 1-2, and 4-15 of the ‘608 Patent (the “Challenged Claims”) are invalid as anticipated by prior art or obvious to a person of ordinary skill in the art at the time of the alleged invention (“POSITA”).
4. In preparing this declaration, I have reviewed the ‘608 Patent, the file history, numerous prior art references, and technical materials from the time of the alleged invention.
5. In forming the opinions expressed in this declaration, I relied upon my knowledge, skill, experience, training, and education in the relevant field of the art, and have considered the viewpoint of a POSITA as of August 20, 2004. My opinion is based on the following references in view of the knowledge of POSITA during this time.

6. In this declaration, I from time to time refer to exhibits by Exhibit Number. I use the same exhibit numbers as are provided in the exhibit list in the Petition for *Inter Partes* Review for which I submit this declaration.

I. Background Qualifications

7. My qualifications generally are set forth in my Curriculum Vitae, which is attached as **Appendix A**. Appendix A also includes a list of the publications I have authored and a list of the other cases in which I have testified during the last four years.

8. I have been working as an Engineer since 1985 and I have been teaching Electrical and Computer Engineering courses since 1991. I am currently a professor emeritus of electrical and computer engineering at the University of Nevada, Las Vegas (“UNLV”).

9. I received B.S. and M.S. degrees in Electrical Engineering from UNLV in 1986 and 1988, respectively. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno, in 1993.

10. My doctoral research, culminating in the award of a Ph.D., investigated the use of power MOSFETs in the design of very high peak power, and high-speed, instrumentation. I developed techniques to reliably stack power MOSFETs to switch higher voltages, that is, greater than 1,000 V and 100 Amps of current with nanosecond switching times. This work was reported in the paper entitled

“Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices,” published in the IEEE Transactions on Power Electronics. The paper received the Best Paper Award in 2000.

A. Industry Experience

11. I have done technical and expert witness consulting for over 200 companies and their subsidiaries since I started working as an engineer in 1985. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapon tests at the Nevada test site. During this time, I designed, and oversaw the fabrication of, over 30 electronic and electro-optic instruments, including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera sweep circuits, Pockel’s cell drivers, micro-channel plate gating circuits, charging circuits for battery backup of equipment for recording test data, and analog oscilloscope electronics.

12. My work during this time, as one example, had a direct impact on my doctoral research work using power MOSFETs, subsequent publishing efforts, and industry designs. In addition to the 2000 Best Paper Award from the IEEE Power Electronics Society, I published several other papers in related areas while working in industry. I hold a patent, Patent No. 5,874,830, in the area of power supply design, titled, “Adaptively biased voltage regulator and operating method,” which was issued on

February 23, 1999. I have designed dozens of linear and switching power supplies for commercial products and scientific instrumentation.

13. I am a licensed Professional Engineer and have extensive industry experience in circuit design, fabrication, and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, Phase-Change Random Access Memory (PCRAM) chips, and CMOS Image Sensors (CISs) at Micron Technology, Inc. (“MTI”) in Boise, Idaho. I spent considerable time working on the development of flash memory chips while at MTI. My efforts resulted in more than a dozen patents relating to flash memory. One of my projects at MTI included the development, design, and testing of circuit design techniques for a multi-level cell (MLC) flash memory using signal processing. This effort resulted in higher-density memories for use in solid-state drives and flash memory cards having an ATA interface that are ubiquitous in consumer electronics, including cameras and data storage systems. Further, the use of higher-density memory can result in fewer changes in the flash translation layer for logical-to-physical addressing, less need for garbage collection, and larger data segments that can improve a computing system’s performance. Another project I worked on at MTI focused on the design of buffers for high-speed double-data rate DRAM, which resulted in around 10 U.S. patents in buffer design. Among many other experiences, I led the development of the delay locked loop (DLL) in the late 1990s so that MTI DRAM products could transition to the DDR

memory protocol, used in mobile and non-mobile (server, desktop, cell phones, tablets, etc.) computing systems as main computer memory, for addressing and controlling accesses to memory via interprocess communications (IPC) with the memory controller (MC). I provided technical assistance with MTI's acquisition of Photobit during 2001 and 2002, including transitioning the manufacture of CIS products into MTI's process technology. Further, I did consulting work at Sun Microsystems and then Oracle on the design of memory modules during 2009 and 2010. This work entailed the design of low-power, high-speed, and wide interconnection methods with the goal of transmitting data to/from the memory module and the MC at higher speeds.

14. I have extensive experience in the development of instrumentation and commercial products in a multitude of areas including: integrated electrical/biological circuits and systems, array (memory, imagers, and displays) circuit design, CMOS analog and digital circuit design, diagnostic electrical and electro-optic instrumentation for scientific research, CAD tool development and online tutorials, low-power interconnect and packaging techniques, design of communication/interface circuits (to meet commercial standards such as USB, firewire, DDR, PCIe, SPI, etc.), circuit design for the use and storage of renewable energy, and power electronics. For example, a part of my research at Boise State, for many years, focused on the use of Thru-Silicon-Vias (TSVs), aka Thru-Wafer Vias

(TWVs), for high-density 3D packaging. These packaging techniques were utilized in the memory module development work I did with Sun Microsystems and Oracle. As another example, I designed circuitry for use in implementing Universal Serial Bus (USB) interface circuits while I did consulting at Tower Semiconductor. I designed PCI communication circuits for IPC between a Graphics Processor Unit (GPU) and memory while consulting for Rendition, Inc. From 1994 to 1996, I worked on the design of displays at Micron Display and Micron Technology, Inc. ("Micron") in Boise, Idaho. This work was at a time when cathode ray tubes (CRTs) were still the dominant type of display. Flat panel displays were being developed with the hope of replacing CRTs in the consumer market. I worked on flat panel displays which resulted in 5 patents: 5,598,156, 5,638,085, 5,818,365, 5,894,293, and 5,909,201. I worked on the design of the pixels, both active and passive, as well as the supporting electronics for processing video signals. I was involved with the evaluation of display technologies including liquid crystal displays (LCDs), light-emitting diodes, plasma displays, and organic light emitting diode (OLED) displays; the display technologies that were looking to displace CRTs in the consumer market. I was also involved with the packaging of the displays including the vacuum sealing and deposition of the phosphors for light wavelength conversion. I also taught display design as a topic in my courses and did display design consulting again in industry for Cirque in 2013.

15. My current research work is focused in part on the design of integrated circuits for wireless sensing using LIDAR (LIght Detection And Ranging). I have worked with several companies in the development of these circuits and systems including Freedom Photonics, Aerius Photonics, and FLIR. In the early 1990s, I worked on wireless systems for wideband impulse radar while at Lawrence Livermore Laboratory. Further, part of my research for several years focused on the digitization of IQ channels using delta-sigma modulation. The knowledge and experience gained from this effort are reflected in my textbook CMOS Mixed-Signal Circuit Design and a presentation, which I have presented at several universities and companies, http://cmosedu.com/jbaker/papers/talks/BP_DSM_talk.pdf.

B. Academic Experience

16. I was an adjunct faculty member in the Electrical Engineering departments of UNLV and UNR from 1991-1993. From 1993 to 2000, I served on the faculty at the University of Idaho as an Assistant Professor and then as a tenured Associate Professor of Electrical Engineering. In 2000, I joined a new Electrical and Computer Engineering program at Boise State University (“BSU”), where I served as department chair from 2004 to 2007. At BSU, I helped establish graduate programs in Electrical and Computer Engineering including, in 2006, the university’s second Ph.D. degree. In 2012, I re-joined the faculty at UNLV. Over the course of my career as a professor, I have advised more than 100 masters and doctoral students.

17. I have been recognized for my contributions as an educator in the field. While at Boise State University, I received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001). In 2007, I received the Frederick Emmons Terman Award (the "Father of Silicon Valley"). The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession. In 2011, I received the IEEE Circuits and Systems Education Award. I received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor Award every year it was awarded while I have been back at UNLV.

18. I have authored several books and papers in the electrical and computer engineering area. My published books include CMOS Circuit Design, Layout, and Simulation (Baker, R.J., Wiley-IEEE, ISBN: 9781119481515 (4th ed., 2019)) and CMOS Mixed-Signal Circuit Design (Baker, R.J., Wiley-IEEE, ISBN: 9780470290262 (2nd ed., 2009) and ISBN: 9780471227540 (1st ed., 2002)). I co-authored DRAM Circuit Design: Fundamental and High-Speed Topics (Keeth, B., Baker, R.J., Johnson, B., and Lin, F., Wiley-IEEE, ISBN: 9780470184752 (2008)), DRAM Circuit Design: A Tutorial (Keeth, B. and Baker, R.J., Wiley-IEEE, ISBN: 0-7803-6014-1 (2001)), and CMOS Circuit Design, Layout and Simulation (Baker, R.J., Li, H.W., and Boyce, D.E., Wiley - IEEE, ISBN: 9780780334168 (1998)). I

contributed as an editor and co-author on several other electrical and computer engineering books.

C. Other Relevant Experience

19. I have performed technical and expert witness consulting for more than 200 companies and their subsidiaries and given more than 50 invited talks at conferences, companies, and universities. Further, I am the author or co-author of more than 100 papers and presentations in the areas of electrical and computer engineering design, fabrication, and packaging.

20. I currently serve, or have served, as a volunteer on the IEEE Press Editorial Board (1999-2004); as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018); as the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015); on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016); as a Distinguished Lecturer for the SSCS (2012-2015); the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for IEEE Solid-State Circuits Magazine; IEEE Kirchhoff Award Committee (2020-2023); and advisor for the student branch of the IEEE at UNLV (2013-present). These meetings, groups, and publications are intended to allow researchers to share and coordinate research. My active participation in these meetings, groups, and publications allowed me to see what other researchers in the field have been doing. In addition to the above, I am

an IEEE Fellow for contributions to semiconductor memory design and a member of the honor societies Eta Kappa Nu and Tau Beta Pi.

II. Understanding of Patent Law

21. I am not an attorney, though I have been provided with an understanding of patent law sufficient to conduct the analysis given in this report. The following represents my understanding of these issues.

22. A patent or published patent application having a priority date or filing date before August 20, 2004, or a printed publication that was first published before August 20, 2004, is prior art against the '608 patent.

23. A claim is invalid or unpatentable if that claim is either anticipated or obvious. In order to show anticipation of a claim, every element of a claim must be disclosed expressly or inherently in a single prior art reference. In order to show obviousness of a claim, the claim must be obvious from the perspective of a POSITA at the time the alleged invention was made. A claim may be obvious in view of a single reference or may be obvious from a combination of two or more prior art references.

24. An obviousness analysis requires an understanding of the scope and content of the prior art, any differences between the alleged invention and the prior art, and the level of ordinary skill in evaluating the pertinent art. In addition, certain factors may support or rebut the obviousness of a claim, such as secondary considerations. Secondary considerations can include things such as commercial success of the

alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. Contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

25. A claim is invalid or unpatentable because it would have been obvious when it combines old elements with no change to a respective function, or alters prior art by mere substitution of one element for another known in the field, and that combination yields predictable results. Moreover, to facilitate a combination of prior art references, a reason to combine the prior art is helpful. However, common sense can be used as a guide; there is no rigid requirement to find an express teaching, suggestion, or motivation to combine. When a product is available, design incentives and other market forces can prompt variations of it, either in the same field or different one. If a person having ordinary skill in the relevant art can implement a predictable variation, a finding of obviousness would likely prohibit patentability of such variations. For the same reason, if a technique has been used to improve one device and a person having ordinary

skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious. A claim may be obvious if common sense directs one to combine multiple prior art references or add missing features to reproduce the alleged invention recited in the claims.

III. Level of Ordinary Skill in the Pertinent Art

26. A POSITA as of August 20, 2004, the filing date of the patent application, would typically possess a Bachelor's degree in Electrical Engineering, Computer Engineering, or a related technical field. (EX1001, 1:13-15). This educational background would provide the necessary foundation to understand the technical concepts presented in the '608 patent, such as the strobe-based memory systems described in the background section. (EX1001, 1:25-38). The patent discusses various memory technologies, including DDR SDRAM and its variants, which would be familiar to someone with this educational background. (EX1001, 3:29-34).

27. In addition to this educational requirement, a POSITA would have 2-3 years of practical experience in memory system design. Alternatively, a POSITA could have a Master's degree in one of the aforementioned fields, coupled with 1-2 years of relevant experience in memory system design. This advanced degree would provide a deeper theoretical understanding of complex digital systems, potentially offsetting the need for additional years of practical experience.

28. The combination of academic knowledge and practical experience would equip a POSITA with the necessary skills to have understood the challenges associated with memory system design, including issues related to signal timing and delay management. This background would have enabled them to comprehend and evaluate the technical concepts presented in the '608 patent, such as the use of variable delay elements and the implementation of calibration control circuits. (EX1001, 4:43-50, 4:52-59).

29. The level of skill described above would enable a POSITA to understand and implement these advanced techniques, as well as to appreciate their potential impact on memory system performance. This skill level is consistent with the technical depth and complexity presented in the '608 patent. (EX1001).

IV. Background

30. At the time of the alleged invention, memory controllers were commonly used to interface between processors and memory devices in computing systems. (EX1005, [0002-0004]). These memory controllers typically included circuitry for synchronizing the timing of control and data signals between the controller and memory devices. (EX1005, [0004-0006]). Double data rate (DDR) synchronous dynamic random access memory (SDRAM) was a widely used type of memory that transferred data on both the rising and falling edges of a clock signal. (EX1005, [0012]). In read and write operations DDR DRAM systems use a "data clock" or

“strobe signal,” sometimes referred to as DQS or DCLK, to indicate when data on various pins should be read. (EX1004, 4:59-66; EX1005, [0013])

31. DDR SDRAM memory systems faced challenges in maintaining proper timing relationships between clock, data, and strobe signals due to factors like propagation delays and environmental variations. (EX1005, [0005-0007]). To address these timing issues, memory controllers often employed delay-locked loop (DLL) circuits to align the phases of clock and strobe signals. (EX1004, 4:1-11; EX1005, [0007-0010]). A POSITA would have understood that DLL devices contain a chain of serially-connected delay elements that introduce controllable delays into an output signal, each delay element creating a delayed version of the input signal. (EX1005, [0011]). These DLL circuits typically included phase detect circuitry to compare the phases of input and output clock signals and generate control signals to adjust delay elements. (EX1005, [0007-0010]).

32. It was common for memory controllers to include separate data paths with adjustable delay elements for receiving data from memory devices. (EX1004; 7:25-60; EX1005, [0017-0019]). These delay elements allowed the timing of incoming data to be adjusted relative to clock or strobe signals to ensure proper sampling. (EX1004; 7:25-60; EX1004, [0017-0019]). Memory controllers often had multiple such data paths to handle parallel data bits coming from memory devices. (EX1004; 7:25-60; EX1004, [0017-0019]).

33. Calibration techniques were known for optimizing the timing of these data paths during system initialization or reset. (EX1004, 2:3-14). These techniques typically involved sending known data patterns from the memory devices, adjusting delays in the controller, and comparing received data to expected values. (EX1004, 2:3-14). The delays would be adjusted to center the data sampling point within the valid data window for each data line. (EX1004, 2:3-14).

34. It was recognized that different optimal delay values may be needed for different data lines due to variations in trace lengths and other factors. (EX1004, 2:3-14). Therefore, per-bit or per-byte calibration and delay adjustment was sometimes employed to individually optimize each data path. (EX1004, 2:3-14).

35. Programmable delay lines were commonly used to implement adjustable delays in memory controllers. (EX1006, 6:49-61). These allowed delay values to be dynamically updated based on calibration results or operating conditions. (EX1006, 6:49-61). Delay lines often consisted of chains of delay elements that could be tapped at different points to achieve different delay amounts. (EX1006, 6:49-61).

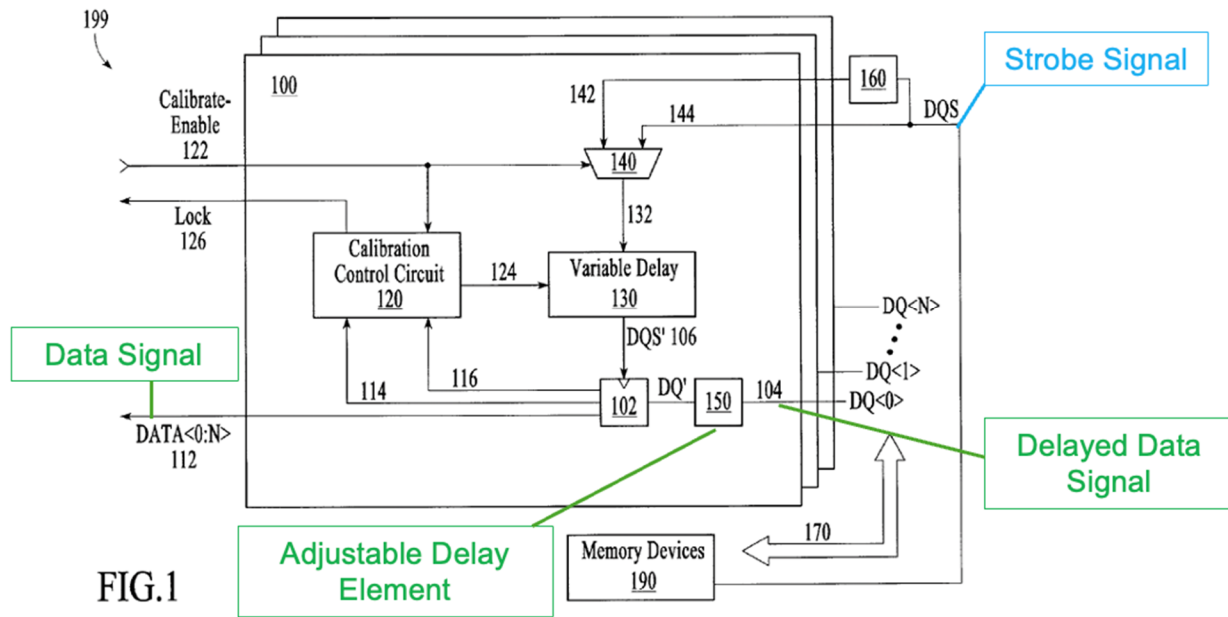
36. Multiple stage synchronization schemes were known, where data would be captured in a first clock domain and then re-synchronized to a second clock domain. (EX1006, 6:64-7:11).

37. Overall, memory controllers with per-bit adjustable delay elements, calibration capabilities, and multi-stage synchronization were well-established in the

art for optimizing timing in high-speed memory interfaces like DDR SDRAM systems. (EX1005, [0002-0025]; EX1006, 1:14-2:34). These techniques were known to improve system reliability and performance by compensating for timing variations between different signal paths. (EX1005, [0005-0007]).

V. The ‘608 Patent

38. The ‘608 patent discloses techniques for enhancing signal alignment in memory controller systems through the use of calibrated delay elements to address challenges associated with signal propagation delays. The ‘608 Patent describes an implementation of per-bit calibration of strobe signal delays, which allegedly represents a departure from conventional approaches that typically apply delays on a per-byte basis. (EX1001, at 3:16-34). Figure 1 of the ‘608 patent illustrates a schematic representation of an embodiment exemplifying the disclosed system. This figure depicts the fundamental components and their interconnections within the proposed memory controller architecture, visually representing how the system achieves individual bit-level timing adjustments through the use of variable delay elements and calibration circuitry.



(EX1001, at Fig. 1 (annotated excerpt)).

39. The purported invention of the ‘608 Patent comprises a relatively concise set of core components. Claim 1 defines two distinct data signal pathways, each incorporating specific functional elements. The first component in each pathway consists of an input pin designated to receive a data signal. This input pin interfaces with external memory devices, facilitating the transfer of data into the controller. Following the input pin, each pathway incorporates an adjustable delay element. This delay element introduces a controllable time delay to the received data signal.

40. The final component in each pathway comprises a sampling circuit. This circuit performs the critical function of sampling the delayed data signal at precise intervals. The timing of these sampling operations directly impacts the reliability of

data capture and, consequently, the overall performance of the memory system.

Claim 1 further specifies a separate input pin dedicated to receiving a strobe signal.

41. The patent's independent claim 10 and dependent claim 9 describe processes for aligning two data pathways. Each pathway in these claims features a data pin, mirroring the structure outlined in claim 1. The alignment process involves applying specific delay values to the respective data lines.

42. An examination of the remaining claims in the '608 patent reveals that they primarily describe generic components or elucidate the purpose of elements already disclosed in the independent claims. These dependent claims do not appear to introduce significant additional technical innovations beyond the core concepts outlined in the independent claims.

43. Claims 2, 11, and 12 focus on the storage and retrieval mechanisms for the delay values associated with the first and second pins. These claims specify that the system includes storage capability for retaining the calculated delay values and subsequently retrieving them for use during normal operation. This functionality allows the system to maintain calibrated timing adjustments across power cycles or operational mode changes. However, the implementation of such storage and retrieval mechanisms is a common practice in digital systems and does not represent a novel technical advancement.

44. Claim 4 essentially restates the fundamental purpose of the claimed invention. It specifies that the delays applied to the first and second pins serve to “compensate for timing offset between the received first and second data signals.” This claim effectively articulates the core problem that the invention aims to address, namely the mitigation of timing discrepancies between different data signals. While this clarification is useful for understanding the invention’s intent, it does not introduce additional technical elements beyond those already present in the independent claims.

45. Claim 5 introduces timing signal delay elements associated with each data pin to delay the strobe signal provided to each pin. This addition allows for fine-tuning of the strobe timing on a per-pin basis, potentially enhancing the system’s ability to maintain proper signal alignment across all data lines. However, the fundamental principle of applying adjustable delays remains consistent with the core invention described in the independent claims.

46. Claims 6 and 7 specify the use of delay-locked loop (DLL) devices as the delay elements in each of the data paths. DLLs are well-known circuit components commonly used in digital systems for precise timing control. While DLLs offer certain performance advantages, such as the ability to dynamically adjust to changing operating conditions and maintain a fixed phase relationship between input

and output signals, their incorporation does not represent a novel technical approach in the context of memory interface design.

47. Claims 8, 14, and 15 introduce the concept of applying a “calibrated delay” to the data strobe signal during the calibration process. This feature allows the system to adjust the timing of the strobe signal itself, in addition to the data signal delays, potentially providing an additional degree of freedom in achieving optimal signal alignment. The calibration process typically involves sending known data patterns and adjusting delays until the received data matches the expected pattern, minimizing bit errors. However, the fundamental principle of applying calibrated delays to achieve signal alignment remains consistent with the core invention described in the independent claims.

48. (Reserved)

49. (Reserved)

50. (Reserved)

VI. Claim Interpretation

51. I understand that claims terms are typically given their ordinary and customary meaning, as would have been understood by a POSITA, during the relevant time frame, which I was asked to assume was in August, 2004. In considering the meaning of the claims, I also understand that one must consider the claim language, specification, prosecution history, and the knowledge of a POSITA

at the relevant time. I have followed these principles in my analysis. I believe all terms in the challenged claims should be given their ordinary and customary meaning, as would have been understood by a POSITA at the time of the purported invention.

A. “pin”

52. The term “pin” in the context of the ‘608 patent carries its plain and ordinary meaning of a “signal path” within memory system design. This interpretation aligns with the common understanding of the term among those skilled in the art of electronic system design, particularly in the realm of memory controllers and interfaces. (EX1001, 1:60-61). In modern electronic systems, the term “pin” has evolved beyond its original physical connotation of a metal connector to refer to any dedicated signal path or connection point for data or control signals, regardless of its physical implementation. (EX1001, 3:15-36).

53. The ‘608 patent’s usage of the term “pin” is consistent with this interpretation of a signal path. For instance, the patent discusses “pin-to-pin offsets in the DRAM.” (EX1001, 1:60-65). In this context, the patent is referring to timing differences between different signal paths rather than physical metal connectors. This usage underscores the understanding of “pin” as a logical concept representing a signal path. (EX1001, 1:60-65; 3:15-36).

54. Further supporting this interpretation, the ‘608 patent describes a “strobe-based memory system 199 including a strobe-offset control system 100” with “data pins” that “receive respective data signals.” (EX1001, 16:15-18). The focus here is clearly on the functional aspect of these “pins” as pathways for data signals, rather than on their physical manifestation. (EX1001, Claim 16; 16:15-18). This functional perspective is critical in modern memory system design, where the emphasis is on signal integrity and timing relationships rather than the specific physical implementation of connections. (EX1001, 1:60-61; 3:15-36).

55. The patent’s discussion of “per-bit strobe-offset control.” (EX1001, 3:15-36) implies that each data bit has its own signal path, which is conceptualized as a “pin” in the patent’s terminology. This granular control at the individual bit level further reinforces the understanding of “pin” as a logical signal path rather than a physical connector. (EX1001, 3:21-22). In high-speed memory systems, this level of granularity is essential for maintaining signal integrity and optimizing data transfer rates, as it allows for precise timing adjustments on a per-bit basis. (EX1001, 3:21-22; 1:60-61).

B. “the first and second data signals are delayed by the first and second delay values.”

56. Claim 13 of the ‘608 patent is indefinite. Claim 13 recites that “the first and second data signals are delayed by the first and second delay values.” But this does not make any technical sense, as would be appreciated by a POSITA. (EX1001, 16:5-

7). The claim states that the data signals are delayed “by the first and second delay values.” (EX1001, 16:5-7). This phrasing introduces a fundamental mismatch between the nature of delays and delay values. In digital systems, delay values are typically represented as control signals or voltages that are applied to delay elements. (EX1001, 16:5-7). But delays are measured in terms of seconds or fractions thereof. These control signals or voltages instruct the delay elements on how much delay to introduce, but they are not the delays themselves, which are measured in seconds. (EX1001, 16:5-7).

57. Nonetheless, if it is assumed that Claim 13 were rewritten to recite that the data signals are “delayed by a delay corresponding to the first and second delay values,” the claim is still invalid as it merely recites the basic functioning of the device claimed in Claim 10. For the purposes of this declaration, I have assumed that Claim 13 is so rewritten.

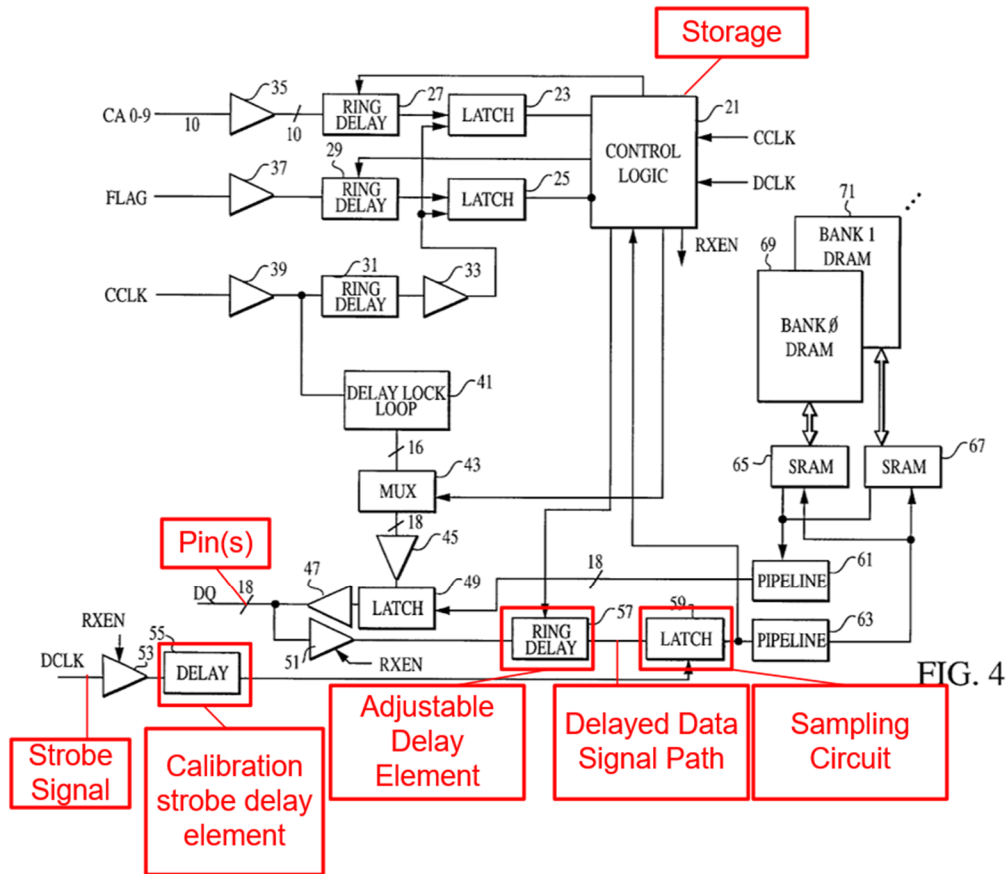
VII. Summary of Prior Art

A. Summary of Johnson

58. Johnson. (EX1004) discloses calibration techniques for memory devices, with a particular focus on double data rate (DDR) dynamic random access memory (DRAM) systems. (EX1004, Abstract, 1:11-2:2). Johnson’s invention improves upon existing calibration methods by ensuring synchronization across multiple data paths during per-bit calibration processes, thereby preventing potential errors that

could arise from sampling data across different time intervals on various data lines.
(EX1004, Abstract, 2:3-14).

59. Johnson's disclosure builds upon prior art calibration systems, as illustrated in Figure 4 of the patent.



(EX1004, at Fig. 4 (annotated)).

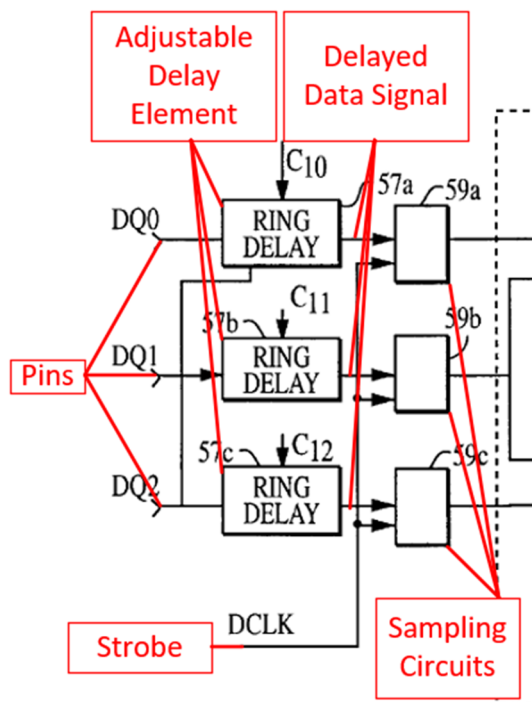
60. This figure depicts a memory device architecture with multiple data paths and calibration components, including memory banks, data buses, and various circuit elements designed to facilitate accurate data transmission and reception. (EX1004, Fig. 4). In the architecture presented by Johnson, data intended for storage in the

memory banks 69 and 71 follows a specific path through the system. This data, originating from the memory controller, is transmitted via the DQ data bus, which is depicted in Fig. 4 as being eighteen bits wide. (EX1004, 4:12-19).

61. For clarity, the annotated figure above denotes “storage” which does not refer to where data controlled by the memory controller is stored (banks 69, 71), but rather where a POSITA would understand that values for the control signals provided to ring delay 57 are stored, in order to provide them to ring delay 57.

62. As the data traverses the system, it passes through a series of circuit elements, each serving a specific function in the data transmission and calibration process. The data first encounters gated buffers 51, which serve to control the flow of data into the subsequent stages. (EX1004, at 4:12-19). From there, the data passes through ring delays 57, which are present on each path of the data bus. (EX1004, at 4:12-19). These ring delays allow for adjustments in the timing of data transmission. (EX1004, at 7:25-60). After the ring delays, the data moves into latches 59, which temporarily store the data before it proceeds through a pipeline circuit. (EX1004, at 4:19-26). This sequence of components ensures that data can be accurately transmitted and properly timed as it moves through the memory device. (EX1004, 4:12-19, Fig. 4).

63. Figure 10 of the Johnson reference illustrates the per-bit calibration system through an embodiment featuring data pins DQ0, DQ1, and DQ2, each representing a data line in the bus. (EX1004, at Fig. 10).



64. (EX1004, Fig. 10 (annotated excerpt)). The data strobe signal, DCLK, serves as an indicator for data availability to the memory controller, or a “data strobe”, a concept well-understood by a POSITA. (EX1004, at 4:62-65). The ring delay elements, labeled as 57a, 57b, and 57c, are adjustable circuits designed to introduce controlled delays to the signals on the respective data pins, managed by the control signals C10, C11, and C12. (EX1004, at 3:49-67, 7:30-35).

65. These ring delay elements are critical components in the calibration process, as they allow for fine-tuning of signal timing to ensure accurate data sampling. The

ability to adjust these delays independently for each data line enables the system to compensate for variations in signal propagation times across different data paths, which can arise due to factors such as differences in trace lengths or electrical characteristics of the circuit components. (EX1004, at 3:53-67).

66. Latches 59a-c are used to sample the delayed data received from the ring delay elements 57a-c in response to the data strobe signal DCLK. (EX1004, at 4:24-26). These latches capture the data at the appropriate moment, as determined by the calibration process. The control logic circuit 21 is responsible for determining appropriate control signals C10, C11, and C12 to enable the memory device to properly read data lines DQ0, DQ1, and DQ2. (EX1004, at 7:25-60).

67. The control logic circuit 21 employs a sophisticated algorithm to establish an “eye” or “window” of acceptable delays for each of the ring delays. (EX1004, at 4:38-43, 5:36-40). This process involves systematically adjusting the delay values and evaluating the resulting data integrity. Once a range of acceptable delays is identified for each ring delay, the control logic circuit 21 determines the optimal delay value, typically selecting a value that is approximately in the middle of the acceptable range. (EX1004, at 4:38-43, 5:36-40). This data eye is depicted in Fig. 6 of Johnson:

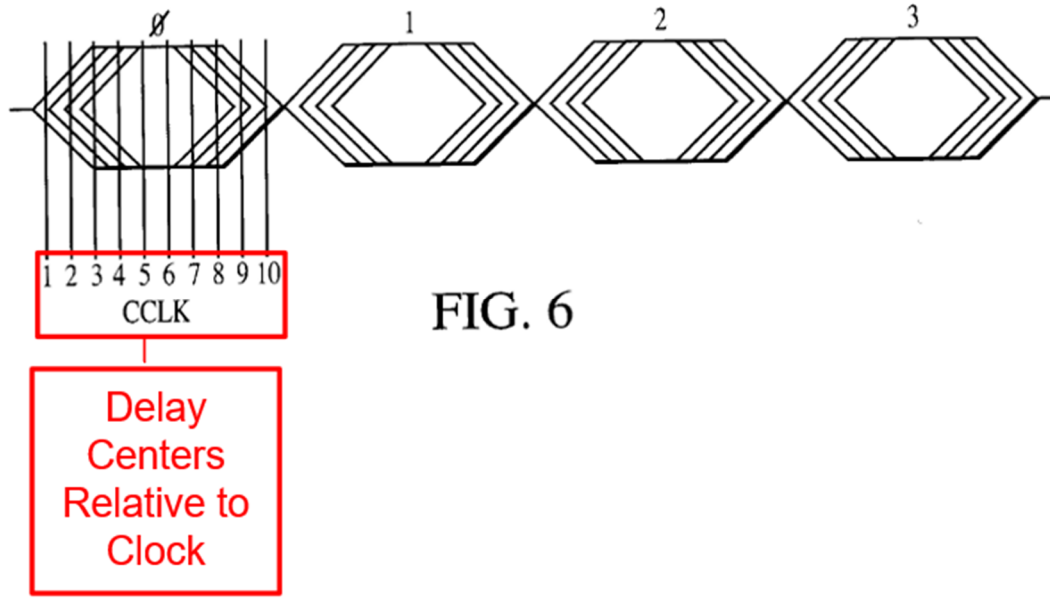


FIG. 6

68. (EX1004, at Fig. 6 (annotated)). By individually calibrating each data line and then aligning them relative to each other, Johnson's technique ensures both serial and parallel alignment of data across all incoming data paths. This calibration strategy minimizes the risk of data misalignment and timing errors, thereby enhancing the overall reliability and performance of the memory system. (EX1004, at 6:35-41, 7:35-43).

69. The control logic circuit, which manages the calibration process for multiple data paths. (EX1004, at 5:32-38, 6:1-6). This control logic circuit determines the optimal delay settings for each data path by evaluating a range of delay values of acceptable delays where data can be reliably sampled. (EX1004, at 7:50-51, 9:39-54). The process involves incrementally adjusting the delay values and assessing the resulting data alignment, allowing the system to find the optimal timing for data capture. (EX1004, at 9:39-54, 12:10-13).

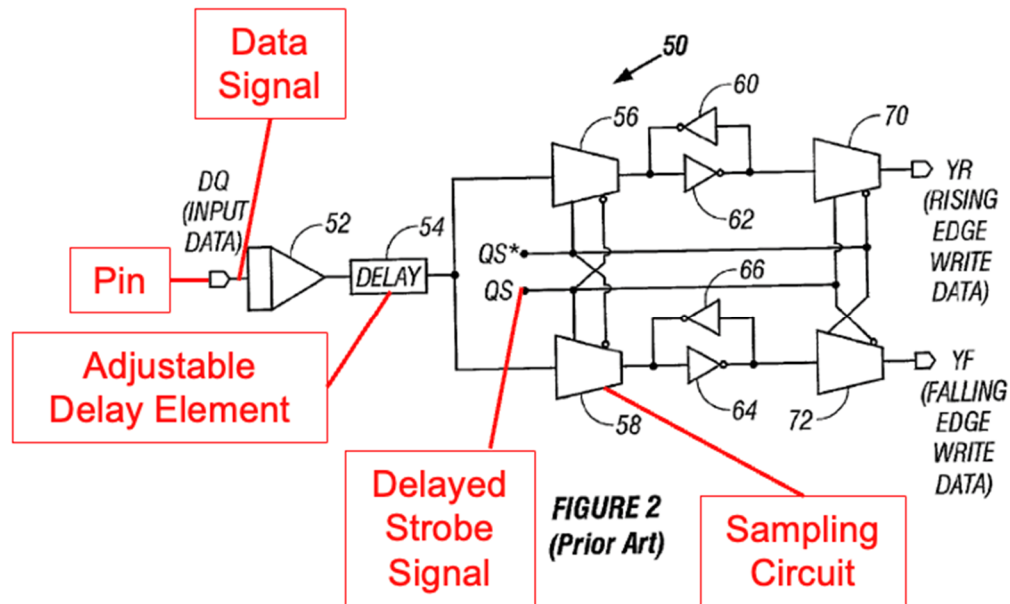
70. The calibration procedure utilizes latches, specifically numbered 59a, 59b, and 59c, which are triggered by the DCLK signal to capture the delayed data. (EX1004, at 4:24-26). This arrangement ensures that data is sampled at the appropriate time, accounting for variations in signal propagation and other timing factors that could affect data integrity. (EX1004, at 4:24-26, 5:32-38). The control logic circuit stores the determined optimal delay values for each data path, allowing these settings to be applied consistently during normal memory operations. (EX1004, at 7:55-60, 12:10-13, 12:25-28). This storage and retrieval mechanism is crucial for maintaining reliable data transmission and reception in the memory system, as it allows the device to quickly adapt to changing operating conditions or to recover from power cycles without requiring a full recalibration. (EX1004, at 7:55-60, 12:10-13, 12:25-28).

71. The calibration process in Johnson's system is able to handle multiple data paths simultaneously or sequentially. (EX1004, at 6:1-6, 9:39-54). This capability is essential in modern memory systems where numerous data lines must be precisely aligned to achieve high-speed, error-free data transfer. (EX1004, at 1:12-26, 6:1-6). By employing a systematic approach to evaluate and adjust the timing of each data path, the system ensures that all data lines are not only individually calibrated but also aligned relative to each other, preventing data skew issues that could arise from misaligned parallel data paths. (EX1004, at 9:39-54, 12:10-13).

B. Summary of Stubbs

72. Stubbs discloses a synchronous double-data-rate (DDR) DRAM device. The device disclosed by Stubbs addresses a similar challenge in high-speed memory systems-the precise timing of data capture relative to clock signals. Stubbs recognizes that propagation delays can vary between different devices and even between rising and falling clock edges within a single device, potentially causing misalignment between data strobe signals and data read/write operations. (EX1005, [0006], [0013], [0015]). To mitigate this issue, Stubbs employs delay locked loop (DLL) circuits, a well-established technique in the field of synchronous memory design. (EX1005, [0010], [0013]).

73. The prior art system described by Stubbs utilizes a DLL circuit to adjust both the data strobe signal and the data signal timing. As illustrated in Figure 2, this system incorporates an adjustable delay element (54) in the data path connected to the DQ data input line:



(EX1005, Fig. 2, [0033]). The delayed data signal and the data strobe signal (QS/QS*) are then fed into pass gates, which act as sampling devices to selectively transmit data at the appropriate clock edges. (EX1005, [0034]). The data strobe signal itself is typically generated using a DLL circuit, making it a delayed strobe signal. (EX1005, [0035]). This approach allows for some degree of timing adjustment to compensate for propagation delays.

74. However, Stubbs identifies a significant limitation in this prior art method. When propagation delays differ between rising and falling clock edges, a single delay adjustment cannot optimally align both edges, potentially leading to setup and hold time violations. (EX1005, [0041-0045]). This problem becomes increasingly critical as memory speeds increase and timing margins tighten.

75. To overcome this limitation, Stubbs discloses a memory controller design that employs separate adjustable delay elements for the rising and falling edges of each data pin. (EX1005, Abstract, [0018]). This per-bit, per-edge delay adjustment allows for much finer control over the setup and hold timing window. Figure 4 of Stubbs illustrates this improved write path circuitry. (EX1005, Fig. 4).

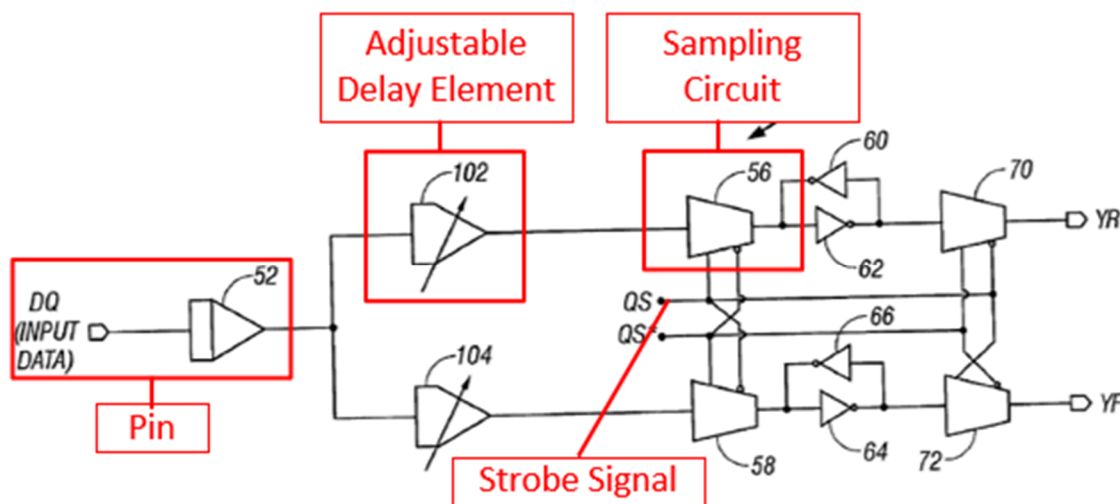


FIGURE 4

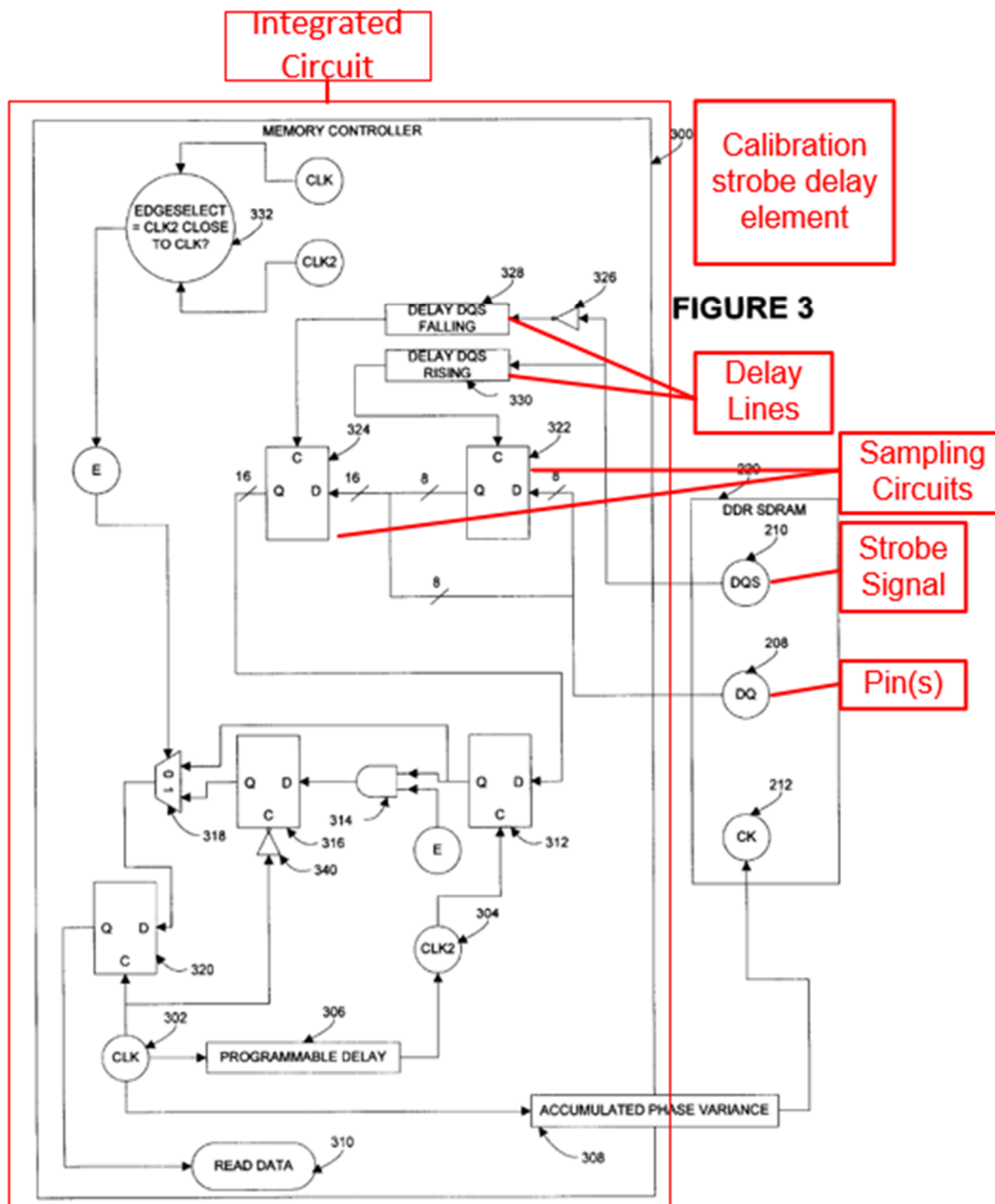
(EX1005, Fig. 4 (annotated)).

76. In the embodiment shown in Figure 4, the write path circuitry comprises an input buffer (52) that receives the input data signal. The output of this buffer is then connected to two separate adjustable delay elements (102 and 104). (EX1005, [0047]). These delay elements introduce independently variable delays into the data path. The output of delay element 102 is fed into a first pass gate (56), while the output of delay element 104 is connected to a second pass gate (58). (EX1005,

[0047]). The pass gates are controlled by the data strobe signal, allowing the delayed data signals to propagate at the appropriate times relative to the rising and falling clock edges. (EX1005, [0047-0048]).

C. Summary of Moss

77. Moss discloses a memory controller designed for use with DDR DRAM devices that addresses timing discrepancies between the memory controller's clock signal (CLK) and the strobe signal (DQS) generated by the memory devices. (EX1006, Abstract, 4:17-36, 5:34-47, Fig. 3). The memory controller employs programmable delay lines (306, 328, 330) to introduce calibrated delays to both the CLK and DQS signals, effectively aligning their timing for accurate read data (DQ) capture. (EX1006, 5:52-6:25, Fig. 3).



(EX1006, at Fig. 3).

78. The delay values used in the programmable delay lines are determined during a calibration phase. This calibration can be performed through analysis of the system design or via automated measurement techniques. (EX1006, 6:52-65). The use of programmable delay lines allows for fine-tuning of signal timing, which is essential

in accommodating variations in propagation delays that may arise from factors such as circuit layout, manufacturing tolerances, and operating conditions. Once calibrated, these delay values are applied during normal operation to dynamically adjust the timing of the CLK and DQS signals, ensuring proper alignment for read data capture despite potential variations in signal propagation. (EX1006, 5:55-6:3, 6:26-36, 7:55-8:4).

79. By implementing this delay-based synchronization technique, Moss's memory controller achieves precise timing alignment between the delayed clock signal (CLK2) and the delayed DQS signal. This alignment allows accurate data capture in DDR DRAM systems, where data is transferred on both the rising and falling edges of the clock. The synchronization method eliminates the need for an asynchronous FIFO, which is a common but less efficient solution to timing discrepancies in memory systems. (EX1006, 2:18-42, 3:1-8, 6:48-58). Asynchronous FIFOs introduce additional latency and complexity to the data path, as they require separate write and read clock domains and additional control logic for managing data flow.

80. The technical implementation described in Moss involves a series of registers and multiplexers that work in conjunction with the delayed clock signals to ensure proper data capture and alignment. The first register (312) captures data using the delayed clock signal CLK2, effectively bringing the data into the CLK2 domain.

Subsequent registers (316, 320) and associated logic allow for further refinement of the data timing, ensuring that setup and hold times are met for reliable data transfer into the main clock (CLK) domain. (EX1006, 6:58-7:28, Fig. 3). This multi-stage registration process, combined with edge-select comparison logic (332), provides a robust mechanism for handling various timing scenarios and preventing metastability issues that could arise from clock domain crossings. (EX1006, 7:15-28, Fig. 3).

D. Summary of Liou

81. Liou discloses a device and method for controlling data latch timing in a memory system to improve the accuracy of data capture under variable operating conditions. (EX1007, Abstract, [0001-0004]). The device comprises a control chip that couples to a storage element such as SDRAM or DDR DRAM. (EX1007, [0018], [0022]). The control chip receives a data strobe signal (DQS) and memory data signal (MD) from the storage element and delays the DQS signal to latch the MD signal. (EX1007, [0018], Fig. 2).

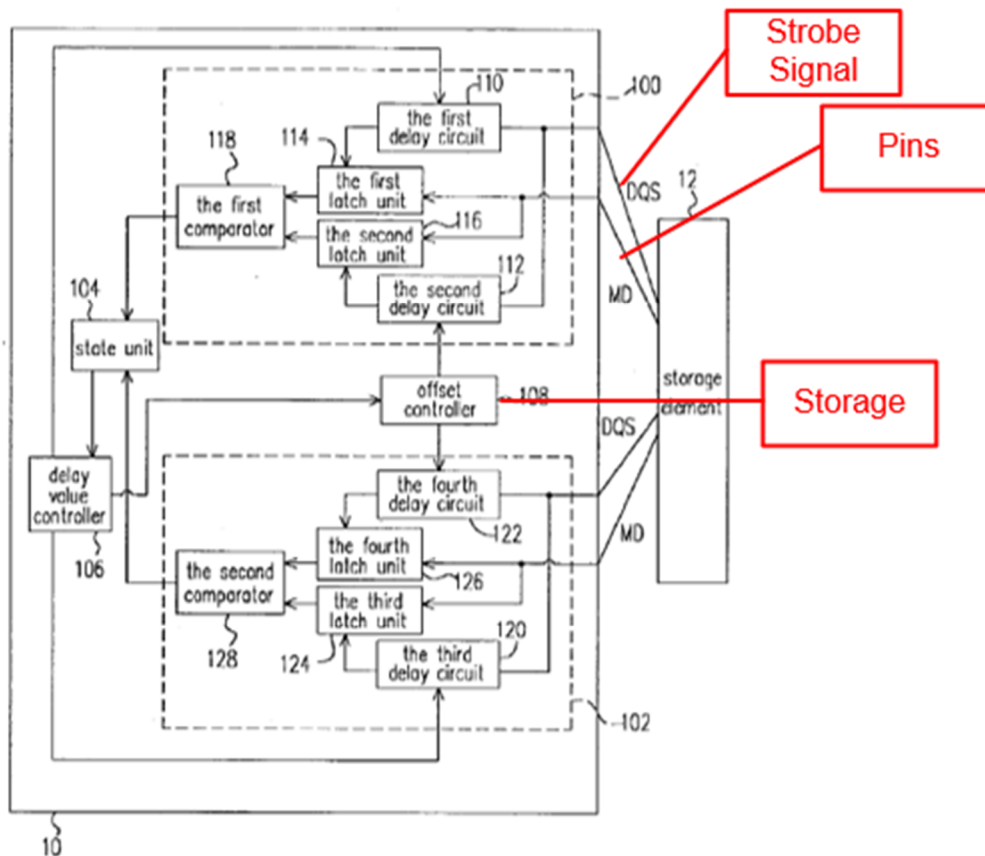


FIG. 2

(EX1007, Fig. 2 (annotated)).

82. For clarity, the component labeled above as “Storage” does not refer to where data controlled by the memory controller is stored (storage element 12), but rather where a POSITA would have understood that the values for the control signals provided to the various delay circuits are stored in order to provide them to the various delay circuits.

83. The control chip contains several key components that enable dynamic adjustment of the data latch timing. A back edge data comparison circuit receives a

first DQS signal (DQS0) and first MD signal (MD). (EX1007, [0019], [0023]). This circuit delays DQS0 by two different amounts—a controlled delay value and the controlled delay value plus an offset. It then latches MD at both of these delay points and compares the latched data. (EX1007, [0023], Claims 1, 6). In parallel, a front edge data comparison circuit performs a similar function with a second DQS signal (DQS8) and second MD signal (MD71). This circuit delays DQS8 by the controlled delay value and by the controlled delay value minus an offset, latches MD71 at both delay points, and compares the results. (EX1007, [0019], [0024], Claims 1, 7).

84. A delay value controller provides the controlled delay value used by both comparison circuits. (EX1007, [0021]). This controlled delay value can be initially set by the BIOS during system initialization, providing a starting point for timing adjustments. (EX1007, [0021]). The delay value controller then dynamically adjusts this controlled delay value based on the comparison results from the back edge and front edge circuits. (EX1007, [0025-0031], Claims 8-10, 17-18).

85. This dynamic adjustment capability allows the system to compensate for timing offsets caused by variations in temperature and voltage during operation. (EX1007, [0025-0031]). When the back edge comparison detects a mismatch, indicating the delay is too short, the controlled delay value is decreased. (EX1007, [0026], Claim 8). Conversely, when the front edge comparison detects a mismatch, indicating the delay is too long, the controlled delay value is increased. (EX1007,

[0026], Claim 9). Through this continuous adjustment process, the system maintains accurate data capture across a range of operating conditions.

86. The use of separate back edge and front edge comparison circuits allows the system to detect timing shifts in either direction. (EX1007, [0019-0020]). The circuits are designed to use signal lines with maximum timing variance, ensuring sensitivity to timing changes. (EX1007, [0019-0020]). This approach provides a robust method for detecting and compensating for timing variations across the entire memory interface.

87. By implementing this dynamic timing adjustment scheme, Liou discloses a memory interface that can maintain accurate data capture despite variable operating conditions such as temperature and voltage fluctuations. (EX1007, [0007], [0011-0012], [0028-0030]). This capability is particularly valuable in high-speed memory systems where timing margins are critical and environmental factors can have significant impacts on signal timing. The system's ability to continuously monitor and adjust timing helps ensure reliable operation across a range of conditions, improving overall system stability and performance.

VIII. Motivations to Combine

88. A POSITA would have been motivated to combine the teachings of Johnson, Stubbs, Moss, and Liou because these references all relate to memory controllers for use in DDR DRAM devices, and specifically address issues associated with

propagation delays that can cause misalignment between strobe signals and data signals in such systems. (EX1004, 2:44-54; EX1005, [0006-0007]; EX1006, 4:37-64, EX1007, [0007]). The references are therefore analogous art, as they are in the same field of endeavor of memory controllers and components for DDR DRAM devices. (EX1004, 1:12-21; EX1005, [0001-0004]; EX1006, 1:6-14; EX1007, [0001-0003]).

A. Motivation to Combine Johnson and Moss

89. A POSITA would have been motivated to combine the teachings of Johnson and Moss to improve memory controller design. Both Johnson and Moss address techniques for managing timing relationships between memory controllers and memory devices, particularly with respect to data strobe signals used for sampling read data. (EX1004, Fig. 4; EX1006, Fig. 3). Johnson discloses using a delay element on the data strobe signal path to adjust timing. (EX1004, Fig. 4, element 55). Moss expands on this concept by incorporating multiple programmable delay elements to provide enhanced flexibility in aligning clock and data signals. (EX1006, Fig. 3, elements 328, 330).

90. The use of multiple delay elements as taught by Moss would have been an obvious enhancement to the single delay element disclosed in Johnson. Moss demonstrates that applying separate delays to rising and falling edges of the data strobe allows for more precise timing adjustments in double data rate (DDR)

memory systems where data is transferred on both clock edges. (EX1006, 6:18-26). This technique provides greater control over the sampling of read data compared to Johnson's single delay approach.

91. Furthermore, Moss explicitly states that the width of data paths in memory systems is a well-known design choice, with common implementations using 4-bit, 8-bit, or 16-bit wide paths. (EX1006, 6:40-49). This teaching would have prompted a person of ordinary skill to consider applying delay elements across multiple data strobe signals when implementing wider data paths, as the benefits of precise timing control would apply equally to each data strobe signal in a multi-bit interface.

92. The combination of Johnson and Moss would have been straightforward to implement. Both disclosures relate to DDR SDRAM memory systems and use similar delay line structures for adjusting signal timing. (EX1004, Fig. 4; EX1006, Fig. 3). A person of ordinary skill would have recognized that the programmable delay techniques of Moss could be readily incorporated into the memory controller architecture of Johnson to achieve improved timing margins and data capture reliability across varying operating conditions and circuit implementations. (EX1006, 4:38-54).

93. By combining the teachings of Johnson and Moss, a person of ordinary skill would have arrived at a memory controller with enhanced flexibility for managing timing relationships between clock, data, and strobe signals. This improved

controller would be better equipped to handle the stringent timing requirements of high-speed memory interfaces while maintaining compatibility with existing memory device standards. (EX1004, 1:12-21; EX1006, 1:8-14).

B. Motivation to Combine Johnson-Moss in further view of Liou

94. A POSITA would have been motivated to combine the teachings of Johnson and Moss with those of Liou to arrive at a memory controller with improved data latch timing control. Johnson and Moss disclose memory controllers for DRAM that utilize multiple delay elements, one for each data path. (EX1001, at 3:24-4:25; EX1004, at [0004-0005]). Liou similarly describes a memory controller for DRAM, but provides additional details regarding the use of delay elements on the data strobe signal. (EX1007, at Abstract, [0005]). Specifically, Liou teaches dynamically adjusting the latch time of the data strobe signal to avoid inaccurate reading of memory data due to interference from temperature or voltage variations. (EX1007, at [0007]). This dynamic adjustment capability would have been recognized as beneficial to incorporate into the Johnson-Moss memory controller to improve its robustness and reliability.

95. The Johnson-Moss memory controller could readily incorporate Liou's technique of using both front edge and back edge data comparison circuits to determine appropriate adjustments to the controlled delay value. (EX1007, at [0012], [0023-0026]). Liou's approach allows the memory controller to detect when the data

strobe signal needs to be delayed further or advanced, and make corresponding adjustments. (EX1007, at [0025-0026]). This would enhance the Johnson-Moss controller's ability to maintain proper timing relationships between the data and strobe signals across varying operating conditions. A person of ordinary skill would have recognized that implementing Liou's dynamic adjustment technique in the Johnson-Moss controller would yield the predictable result of a more robust memory interface less susceptible to timing errors.

96. Furthermore, Liou's teaching of selecting specific data and strobe signal pairs for the comparison circuits based on maximum timing variances would have been obviously applicable to the Johnson-Moss controller. (EX1007, at [0019-0020]). This selection process ensures that the timing adjustments are based on the most critical signal paths. Incorporating this feature into Johnson-Moss would optimize the controller's ability to maintain proper timing across all data paths. The combination would have been a straightforward application of known memory controller design techniques to improve the performance and reliability of the Johnson-Moss system.

C. Motivation to Combine Stubbs with Moss

97. A POSITA would have been motivated to combine the teachings of Stubbs and Moss. Both references address techniques for managing timing relationships between memory controllers and memory devices, particularly for high-speed

memory interfaces. (EX1006, 1:8-14, 2:47-53). Stubbs discloses the use of a delayed data strobe signal, but provides limited details on its implementation. (EX1006, [0035]). Moss offers more comprehensive information on delaying a data strobe signal using a delay element, which would have been valuable to one implementing the system described in Stubbs. (EX1006, Fig. 3, 6:47-48).

98. The delay element disclosed in Moss could be readily adapted to the memory interface described in Stubbs. Moss teaches that the delay element can be used to compensate for phase offsets between clock and strobe signals, which is a common challenge in high-speed memory interfaces. (EX1006, 2:54-65). This technique would have been directly applicable to the memory system of Stubbs, which also deals with timing relationships between memory controller and memory device signals. (EX1006, [0035]).

99. Furthermore, Moss provides guidance on scaling the data path width, explicitly stating that 4-bit, 8-bit, and 16-bit wide data paths are common design choices. (EX1006, 6:39-49). This teaching would have enabled a person of ordinary skill to adapt the delay element technique to various memory configurations, including applying delay elements to individual bits of the data strobe if needed. The flexibility to adjust the data path width would have been particularly useful when implementing the memory interface across different system designs or memory device specifications. (EX1006, 6:39-49).

100. The combination of Stubbs and Moss would have yielded predictable results. Both references deal with similar technical challenges in memory interfaces, and their teachings are complementary. The detailed delay element implementation from Moss could be incorporated into the memory system of Stubbs without requiring significant modifications to the overall architecture. (EX1006, Fig. 3, 6:47-48; EX1006, [0035]). This combination would have resulted in a more robust and flexible memory interface capable of handling timing variations across different memory configurations and operating conditions. (EX1006, 2:54-65, 6:39-49).

D. Motivation to Combine Stubbs-Moss in further view of Liou

101. A POSITA would have been motivated to combine the teachings of Stubbs and Moss with those of Liou to arrive at a memory controller with multiple delay elements for each data path and further refinements to the delay of the data strobe signal. Stubbs and Moss disclose memory controllers for DRAM memory with delay elements on data paths, while Liou similarly relates to a memory controller for DRAM and provides additional details on controlling the timing of the data strobe signal. (EX1007, at Abstract, [0005]). Specifically, Liou teaches dynamically adjusting the latch time of the data strobe signal to account for temperature and voltage variations that can cause timing offsets and inaccurate data reading. (EX1007, at [0007], [0011]). This dynamic adjustment capability would have been seen as a valuable enhancement to the static delay elements disclosed in Stubbs-

Moss, as it would allow the memory controller to maintain proper timing even as operating conditions change during system operation. (EX1007, at [0007-0010]).

102. Liou discloses a back edge data comparison circuit and a front edge data comparison circuit that compare latched data using different delay amounts on the data strobe signal. (EX1007, at [0012-0013], [0023-0026]). These comparison circuits allow the memory controller to detect when the current delay setting is causing timing errors and adjust the delay accordingly. (EX1007, at [0025-0027]). A person of ordinary skill would have recognized that incorporating this dynamic adjustment technique from Liou into the multiple delay element architecture of Stubbs-Moss would provide more robust and reliable memory read operations across varying operating conditions. The comparison circuits and adjustment logic of Liou could be readily adapted to work with the per-byte delay elements of Stubbs-Moss, allowing independent optimization of the delay for each data path. (EX1007, at [0018-0020]).

103. Furthermore, Liou teaches selecting specific data and strobe signal pairs for the comparison circuits based on which pairs exhibit the maximum timing variance due to trace length differences. (EX1007, at [0019-0021]). This technique ensures that the delay adjustment is optimized for the most critical timing paths. A person of ordinary skill would have been motivated to apply this selection method when implementing the dynamic delay adjustment in the combined system, as it would

provide the greatest improvement in overall timing margin and reliability. The implementation would involve identifying the data byte lanes with the largest differential in trace length between data and strobe signals, and applying Liou's comparison and adjustment techniques to those specific lanes. (EX1007, at [0019-0021]).

E. Motivation to Combine Stubbs-Moss in further view of Johnson

104. The combination of Stubbs and Moss teaches a memory controller with multiple delay elements, one for each data path. (EX1001, at 3:15-25; EX1002, at [0034-0036]). This configuration allows for precise timing control of individual data signals in a memory system. (EX1001, at 4:10-15). Johnson discloses a specific calibration method that can be applied to such a memory controller system with multiple delay elements. (EX1003, at [0045-0048]). The calibration technique and associated control circuitry described in Johnson are directly applicable to the physical systems provided in the Stubbs-Moss combination. (EX1003, at Fig. 3; EX1001, at Fig. 2; EX1002, at Fig. 4).

105. Implementing Johnson's calibration method with the Stubbs-Moss system would involve a straightforward substitution of components. (EX1003, at [0050-0052]; EX1001, at 5:5-20; EX1002, at [0040-0042]). Specifically, the delay circuitry of Johnson could be replaced with the more granular delay systems described in Stubbs-Moss. (EX1003, at Fig. 2; EX1001, at Fig. 3; EX1002, at Fig. 5). This

substitution would maintain the fundamental calibration principles of Johnson while leveraging the enhanced timing control capabilities of the Stubbs-Moss combination. (EX1003, at [0055-0058]; EX1001, at 6:1-15; EX1002, at [0045-0048]).

106. The motivation for combining these references stems from the need for precise timing calibration in high-speed memory systems. (EX1001, at 1:25-35; EX1002, at [0003-0005]; EX1003, at [0002-0004]). As memory speeds increase, the timing margins for data transmission become increasingly narrow, necessitating more accurate delay adjustments. (EX1001, at 2:1-10; EX1002, at [0006-0008]). The Stubbs-Moss combination provides a hardware architecture capable of fine-grained delay control, while Johnson offers a robust calibration method to optimize these delay settings. (EX1001, at 3:30-40; EX1002, at [0035-0038]; EX1003, at [0040-0043]).

107. Furthermore, the combination of these references would yield predictable results to one of ordinary skill in the art. (EX1001, at 7:5-15; EX1002, at [0050-0052]; EX1003, at [0060-0062]). The delay elements and control logic described in Stubbs and Moss are compatible with the calibration algorithms presented in Johnson. (EX1001, at Fig. 4; EX1002, at Fig. 6; EX1003, at Fig. 5). This compatibility ensures that the combined system would function as expected,

providing improved timing accuracy and system performance. (EX1001, at 8:1-10; EX1002, at [0055-0058]; EX1003, at [0065-0068]).

108. The resulting system from this combination would offer several advantages over the individual references. (EX1001, at 9:5-15; EX1002, at [0060-0062]; EX1003, at [0070-0072]). These advantages include more precise delay control, improved calibration accuracy, and better overall system performance in high-speed memory applications. (EX1001, at 10:1-10; EX1002, at [0065-0068]; EX1003, at [0075-0078]). Such improvements are particularly relevant in modern computing systems where memory performance is often a critical factor in overall system speed and efficiency. (EX1001, at 1:40-50; EX1002, at [0010-0012]; EX1003, at [0005-0007]).

IX. Analysis of Individual Limitations

109. Johnson, Moss, Stubbs, and Liou disclose various limitations of the Challenged Claims of the ‘608 Patent, as set forth below.

A. Ground 1: Johnson, in view of Moss

a. 1[pre]: “An integrated circuit (IC) memory controller comprising:”

i. Johnson

110. Johnson discloses an integrated circuit (IC) memory controller. Johnson expressly describes an “integrated memory circuit.” (EX1004, Claim 67). The memory controller in Johnson interfaces with and controls the operation of memory

modules, such as SDRAM devices. (EX1004, 1:14-21). It performs the functions of an IC memory controller, including generating clock signals, transmitting commands, and coordinating data transfer with memory devices. (EX1004, 3:31-45). Johnson's memory controller conducts calibration of data and clock signals for memory devices, a key function of IC memory controllers. (EX1004, Abstract).

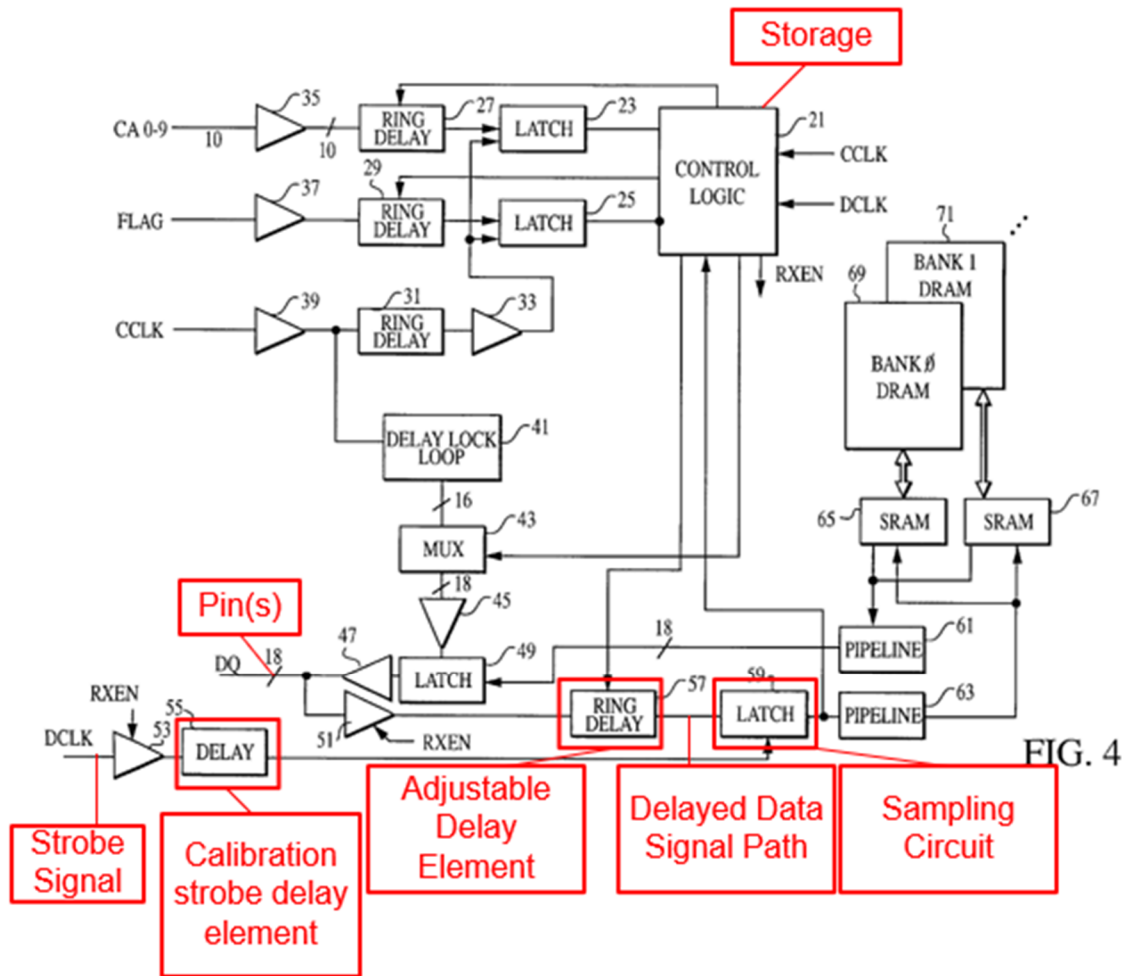
ii. Moss

111. Moss also discloses an integrated circuit (IC) memory controller. The memory controller in Moss interfaces with memory components such as DDR SDRAM devices to facilitate high-performance read and write operations. (EX1006, Abstract, 1:8-14). Moss implements the memory controller as an integrated circuit, allowing for efficient signal routing and timing control within a single chip. (EX1006, Fig. 3).

**b. 1[a]: “a first pin to receive a first data signal;
a first adjustable delay element to delay the received first data
signal and generate a first delayed data signal;”**

i. Johnson

112. Johnson discloses a first pin to receive a first data signal and a first adjustable delay element to delay the received first data signal and generate a first delayed data signal. The memory device in Johnson includes multiple data paths for receiving data signals, each with an associated adjustable delay element. (EX1004, Fig. 4).
Not storage below as indicated earlier.



(EX1004, Fig. 4 (annotated)).

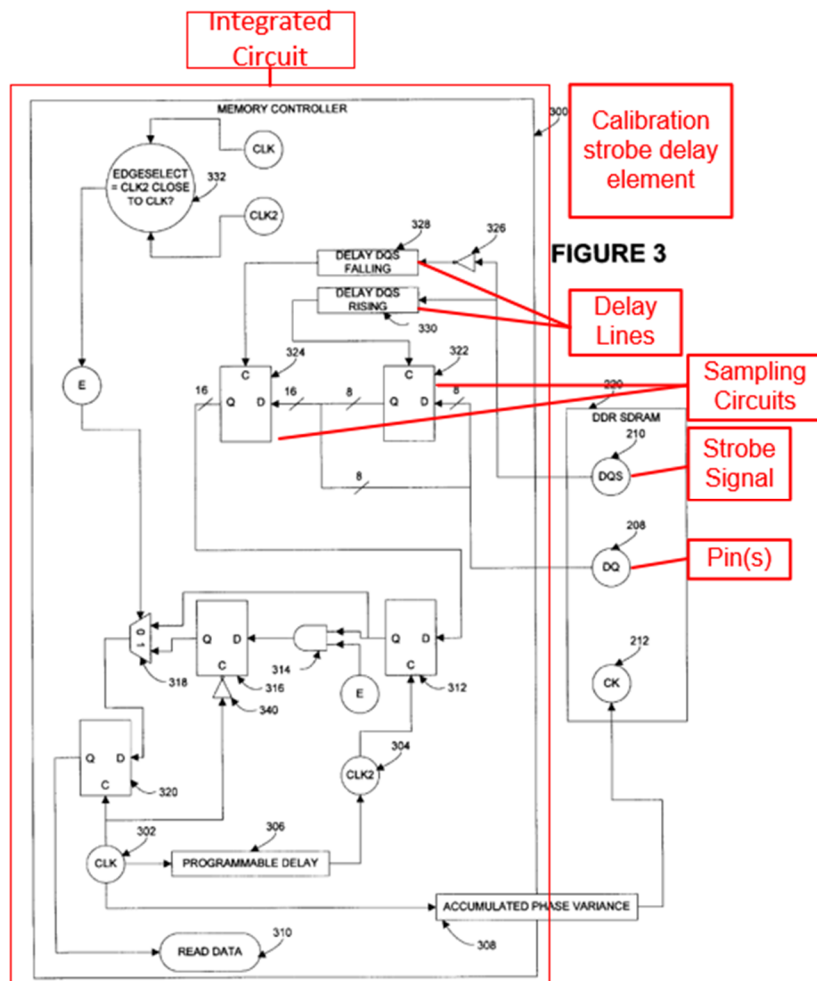
113. Specifically, Johnson shows a data path DQ that includes a pin to receive an incoming data signal and a ring delay 57 to delay that received data signal. (EX1004, Fig. 4, 7:25-60). The ring delay 5a is an adjustable delay element that can impart different amounts of delay to the received data signal, generating a delayed version which is then provided to latch 59. (EX1004, Fig. 4, 4:13-18, 7:25-60).

114. The adjustable nature of the delay element allows the memory device to calibrate the timing of data signals relative to a clock signal, compensating for timing

variations and ensuring proper sampling of the data signal. (EX1004, 4:38-43, 7:54-59, 1:38-43).

ii. Moss

115. Even if Johnson did not disclose this feature, Moss does. Moss describes a memory controller that receives data signals from a memory component via pins. (EX1006, Fig. 3, 5:51-55). The memory controller receives data signal DQ from the memory component on a pin, corresponding to the claimed first data signal received on a first pin. (EX1006, Fig. 3, 6:28-30).



(EX1006, Fig. 3 (annotated)).

116. Moss further discloses delay elements used to delay the received data signals, particularly delay line 330, which delays the data strobe signal DQS controlling the sampling of the data signal DQ. (EX1006, Fig. 3, 6:16-23, 6:28-36). This effectively delays the received data signal DQ and generates a delayed version of that data signal.

117. The delay line 330 in Moss is adjustable, with the amount of delay calibrated to compensate for phase offset errors between the clock and strobe signals. (EX1006, 6:59-63). This adjustable delay realigns the data signals with the internal clock of the memory controller, serving the same purpose as the claimed adjustable delay element. (EX1006, 5:62-68, 6:1-4).

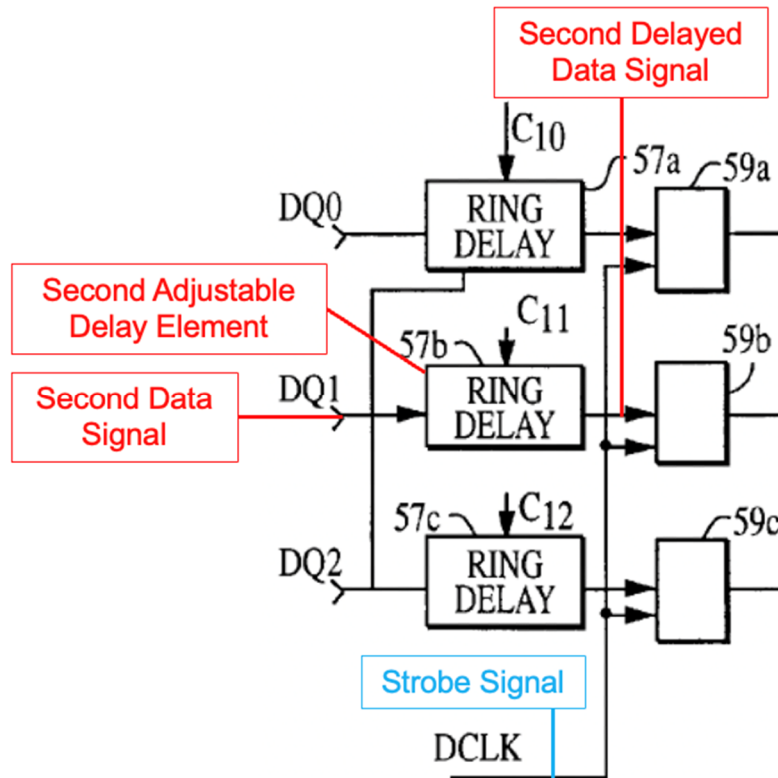
iii. Motivation to Combine

118. A POSITA would have been motivated to combine the teachings of Johnson and Moss to arrive at the claimed first pin and first adjustable delay element. Both references address timing control in memory systems and seek to improve data transfer efficiency. Combining Johnson's explicit disclosure of a pin for receiving data signals with Moss's teaching of adjustable delay elements for data signal timing would yield predictable results in enhancing memory controller performance. The integration of these features would provide the known benefits of improved timing control and signal integrity, which are critical in high-speed memory interfaces.

**c. 1[b]: “a second pin to receive a second data signal;
a second adjustable delay element to delay the received second
data signal and generate a second delayed data signal;”**

i. Johnson

119. Johnson discloses a second pin to receive a second data signal and a second adjustable delay element to delay the received second data signal and generate a second delayed data signal. As described for limitation 1[a], Johnson’s memory device includes multiple data paths for receiving data signals, each with an associated adjustable delay element. (EX1004, Fig. 4). Johnson explicitly shows that the DQ signal path is 18 bits wide, indicating the presence of multiple data pins. (EX1004, 7:34-43). Figure 10 of Johnson provides a more detailed view, depicting three separate pins DQ0-DQ2, each with its own adjustable delay element (ring delay 57a-c) to produce a delayed data signal. (EX1004, Fig. 10).



(EX1004, at Fig. 10 (annotated excerpt)).

ii. Moss

120. Even if Johnson did not disclose this feature, Moss does. Moss describes a memory controller that interfaces with DDR SDRAM memory components, which utilize multiple data pins for parallel data transfer. (EX1006, 1:9-14). The memory controller includes circuitry to receive and process multiple data signals from the memory components via a data bus DQ, which comprises multiple data pins. (EX1006, 5:25-28, Fig. 3). Moss's delay elements, such as delay line 330, are used to delay the received data signals, effectively generating delayed versions of the data signals. (EX1006, 6:16-23, 6:28-36).

iii. Motivation to Combine

121. A POSITA would have been motivated to combine the teachings of Johnson and Moss to arrive at the claimed second pin and second adjustable delay element. Both references address timing control in memory systems with multiple data signals. Combining Johnson's explicit disclosure of multiple data pins with adjustable delays and Moss's teaching of a multi-pin data bus with delay elements would yield predictable results in enhancing memory controller performance. The integration of these features would provide the known benefits of improved timing control and signal integrity for multiple data signals, which are critical in high-speed memory interfaces.

d. **1[c]: "a pin to receive a strobe signal;"**

i. Johnson

122. Johnson discloses a pin to receive a strobe signal. The memory device in Johnson includes a pin to receive a strobe signal DCLK, which is used to clock data into and out of the memory device. (EX1004, Fig. 4, 4:24-5:7). Figure 4 (shown above) clearly shows the DCLK signal being received by the memory device through a dedicated pin. (EX1004, Fig. 4).

123. The DCLK strobe signal in Johnson serves the same purpose as the strobe signal in the challenged patent-it is used to time the sampling of data signals.

(EX1004, 4:24-5:7). Johnson explicitly identifies DCLK as a strobe signal in Figure 5. (EX1004, Fig. 5).

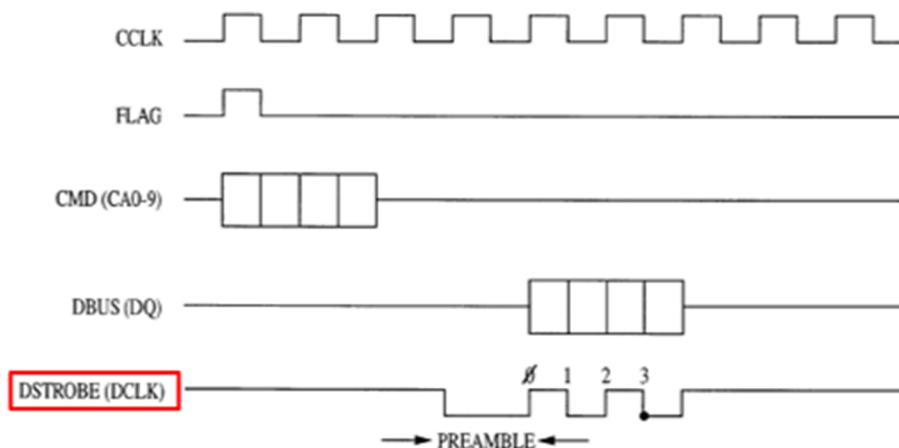


FIG. 5

(EX1005, Fig. 5 (annotated)). Johnson's memory device uses a dual clock architecture, with CCLK for command/address signals and DCLK for data signals, which is common in high-speed memory interfaces to allow precise timing of data capture. (EX1004, 3:65-4:3, Fig. 4). The dedicated pin for the DCLK strobe signal facilitates timing precision by providing a direct path for the critical timing reference. (EX1004, Fig. 4).

ii. Moss

124. Even if Johnson did not disclose this feature, Moss does. Moss's memory controller includes a pin to receive a strobe signal DQS from an associated memory component. (EX1006, 5:36-41). This strobe signal is applied to delay lines within the memory controller. (EX1006, Fig. 3, 6:16-22).

125. The DQS strobe signal in Moss indicates when valid data is available on the data bus during read operations. (EX1006, 1:36-41). By receiving this strobe signal, the memory controller can properly time the sampling of the returned read data, accommodating variations in propagation delays and other timing factors. (EX1006, 6:22-26, 1:43-54).

iii. Motivation to Combine

126. A POSITA would have been motivated to combine the teachings of Johnson and Moss to arrive at the claimed pin to receive a strobe signal. Both references address timing control in memory systems and use strobe signals for precise data sampling. Combining Johnson's explicit disclosure of a dedicated strobe signal pin with Moss's teaching of using the strobe signal for timing adjustment would yield predictable results in enhancing memory controller performance. The integration of these features would provide the known benefits of improved timing control and signal integrity, which are critical in high-speed memory interfaces.

e. **1[d]: "a first sampling circuit to sample the first delayed data signal based on the strobe signal; and"**

i. Johnson

127. Johnson discloses a first sampling circuit to sample the first delayed data signal based on the strobe signal. Johnson teaches a latch 59 that samples delayed data signals based on a strobe signal DCLK. (EX1004, at Fig. 4, 4:13-17). The

delayed data signals sampled by latch 59 are generated by ring delays 57, which delay incoming data signals on the DQ data bus. (EX1004, at Fig. 4, 4:14-16). The DCLK signal used to control latch 59 corresponds to the claimed strobe signal. (EX1004, at Fig. 4, 4:24-27).

128. Johnson further elaborates on this sampling circuit in Figure 10, showing multiple instances of latch 59 (labeled 59a-c) sampling delayed data signals from multiple data paths DQ0, DQ1, DQ2 based on the DCLK strobe signal. (EX1004, at Fig. 10, 7:37-43). This sampling arrangement enables the memory device to compensate for timing variations between different data paths and ensure reliable data capture. (EX1004, at 1:38-43, 2:47-52).

ii. Moss

129. Even if Johnson did not disclose this feature, Moss does. Moss teaches a register flip-flop 322 that samples eight bits of delayed data generated by data signal DQ 208 from the memory component 220. (EX1006, Fig. 3, 6:28-31). This sampling is performed based on a delayed version of the data strobe signal DQS 210 generated by the memory component. (EX1006, 6:28-33). The data strobe signal DQS 210 is applied to delay line 330 to generate a delayed version that clocks register flip-flop 322, ensuring data is captured reliably even in the presence of timing variations. (EX1006, 6:16-27, 1:43-54, 2:43-54).

iii. Motivation to Combine

130. A POSITA would have been motivated to combine the teachings of Johnson and Moss to arrive at the claimed first sampling circuit. Both references address timing control in memory systems and use strobe signals for precise data sampling. Combining Johnson's explicit disclosure of a latch sampling delayed data signals with Moss's teaching of using a delayed strobe signal for sampling would yield predictable results in enhancing memory controller performance. The integration of these features would provide the known benefits of improved timing control and signal integrity, which are critical in high-speed memory interfaces.

f. **1[e]: "a second sampling circuit to sample the second delayed data signal based on the received strobe signal."**

i. Johnson

131. Johnson discloses a second sampling circuit to sample the second delayed data signal based on the received strobe signal. As discussed previously, Johnson's memory device includes multiple data paths, each with its own adjustable delay element and sampling circuit. (EX1004, Fig. 10). Figure 10 clearly shows three separate pins DQ0-DQ2, each with an adjustable delay element (ring delay 57a-c) and a sampling circuit (latches 59a-c) that samples the delayed signal based on the received strobe signal DCLK. (EX1004, Fig. 10, 7:37-43). This arrangement allows the memory device to compensate for timing variations across multiple data paths, ensuring reliable data capture. (EX1004, 1:38-43, 2:47-52).

ii. Moss

132. Even if Johnson did not disclose this feature, Moss does. While Moss explicitly shows only one data signal path with register flip-flop 322 in Figure 3, it is understood that memory interfaces typically have multiple data pins for parallel data transfer. (EX1006, 1:25-31, 5:40-47). A POSITA would recognize that the circuit shown in Figure 3 would be replicated for each data pin of the memory interface, resulting in multiple sampling circuits, each handling a separate data signal. (EX1006, 5:40-47, 6:28-36). For each data pin, the corresponding sampling circuit would operate as described for the first sampling circuit (*See supra*, §IX.A.e), with the data strobe signal DQS 210 applied to delay line 330 to generate a delayed version for clocking the register flip-flop. (EX1006, 6:16-27).

iii. Motivation to Combine

133. A POSITA would have been motivated to combine the teachings of Johnson and Moss to arrive at the claimed second sampling circuit. Both references address timing control in multi-pin memory systems and use strobe signals for precise data sampling. Combining Johnson's explicit disclosure of multiple sampling circuits with Moss's teaching of using a delayed strobe signal for sampling would yield predictable results in enhancing memory controller performance. The integration of these features would provide the known benefits of improved timing control and

signal integrity across multiple data paths, which are critical in high-speed memory interfaces.

g. 2: “The IC memory controller according to claim 1, further comprising storage to store each of first and second delay values corresponding to the delays imparted to the first and second data signals.”

i. Johnson

134. Johnson discloses storage for storing delay values corresponding to delays imparted to data signals. The control logic circuit in Johnson determines and stores delay values for aligning multiple data paths. (EX1004, 7:1-25). This process involves stepping through possible delay values for ring delay elements, noting which produces matching calibration patterns, and selecting final delay values. (EX1004, 7:1-15). Johnson’s calibration process is performed for multiple data paths, resulting in stored delay values for each path. (EX1004, 7:15-25). A POSITA would have understood that these delay values are necessarily stored in the control logic 21 for application to ring delays 57, and thus Johnson inherently discloses this feature. (EX1004, Fig. 10). Storing optimized delay values allows the memory controller to maintain proper timing alignment without repeated full calibration, enabling quick configuration after resets or power cycles. (EX1004, 7:54-67, 8:1-2).

ii. Moss

135. Even if Johnson did not disclose this feature, Moss does. Moss teaches a memory controller 300 with delay lines 328 and 330 that delay the data strobe signal

DQS 210 for proper data sampling. (EX1006, Fig. 3, 6:16-26). The delay values for these delay lines are predetermined and stored. (EX1006, 6:55-63). Moss explicitly states that the delay values are determined through external methods and may be calculated by the designer based on circuit analysis. (EX1006, 6:64-7:2). These stored delay values are used to compensate for phase offset errors between the clock signal CLK 302 and the data strobe DQS 210, maintaining optimal timing despite variations in operating conditions or manufacturing tolerances. (EX1006, 5:51-6:15, 6:59-63).

iii. Motivation to Combine

136. A POSITA would have been motivated to combine the teachings of Johnson and Moss to arrive at the claimed storage for delay values. Both references address timing control in memory systems and use stored delay values for signal alignment. Combining Johnson's explicit disclosure of storing delay values for multiple data paths with Moss's teaching of using predetermined stored delays would yield predictable results in enhancing memory controller performance. The integration of these features would provide the known benefits of improved timing control and signal integrity across multiple data paths, which are critical in high-speed memory interfaces.

h. 4: “The IC memory controller according to claim 1, wherein the first and second data signals are delayed to compensate for timing offset between the received first and second data signals.”

i. Johnson

137. Johnson discloses delaying first and second data signals to compensate for timing offset between the received signals (EX1004, at Abstract). The memory controller in Johnson uses adjustable delay elements in multiple data paths to align incoming data signals. (EX1004, Fig. 4, 2:24-42, 3:65-4:10). These delay elements specifically compensate for timing differences between data signals received on different paths. (EX1004, 4:38-43, 4:51-56). Johnson’s calibration process demonstrates how the delay elements compensate for timing offsets by stepping through different delay values for each data path and comparing the delayed data to a reference signal. (EX1004, 7:1-25). This process allows the memory controller to determine the optimal delay for each data path, effectively compensating for initial timing offsets between the paths and accounting for variations in signal timing caused by factors such as different trace lengths or other sources of skew. (EX1004, 1:38-43).

ii. Moss

138. Even if Johnson did not disclose this feature, Moss does. Moss’s memory controller aligns received data signals with a strobe signal by imparting delays. (EX1006, 3:9-15). The controller includes delay elements to delay the received data signals and generate delayed data signals. (EX1006, Fig. 3, elements 328 and 330).

These delay elements skew the data strobe signal DQS to capture data on the data signal DQ in the center of the edges of DQS transitions, corresponding to a 25% phase shift under ideal conditions. (EX1006, 6:24-27). This skewing of the data strobe signal relative to the data signal compensates for timing offsets between the received signals.

iii. Motivation to Combine

139. A POSITA would have been motivated to combine the teachings of Johnson and Moss to arrive at the claimed delay compensation. Both references address timing control in memory systems and use delay elements to compensate for timing offsets. Combining Johnson's explicit disclosure of using delays to compensate for timing differences across multiple data paths with Moss's teaching of skewing the data strobe signal relative to the data signal would yield predictable results in enhancing memory controller performance. The integration of these features would provide the known benefits of improved timing control and signal integrity across multiple data paths, which are critical in high-speed memory interfaces.

i. **5: “The IC memory controller according to claim 4, further comprising: a first timing signal delay element associated with the first pin; and a second timing signal delay element associated with the second pin; wherein each of the first and second timing signal delay elements impart first and second delays to the strobe signal.”**

i. Johnson

140. Johnson discloses a memory controller with adjustable delay elements for aligning data signals with a clock signal. While Johnson does not explicitly show separate timing signal delay elements for each data pin, its teachings render such a configuration obvious. Johnson’s data path includes a data pin DQ, delay elements 55 and 57, and a latch 59. (EX1004, Fig. 4, 4:13-27). The data clock signal DCLK passes through a gated buffer 53 and delay circuit 55 before controlling latch 59 to sample the incoming data. (EX1004, 4:24-27). This configuration allows for adjusting the timing relationship between the data signal and the clock signal used to sample it.

141. While Johnson shows this delay configuration for a single data pin, it would have been obvious to a POSITA to apply the same delay architecture to multiple data pins. Johnson teaches that the control logic circuit 21 can adjust delays for multiple data paths to align them with the clock signal. (EX1004, 7:37-43). Implementing separate delay elements for each pin, including for the strobe signal, would provide finer-grained control over timing relationships, compensating for variations between

pins and improving overall timing margin and reliability (*See supra*, § IX.A.b, IX.A.c).

142. Regarding the limitation of first and second timing signal delay elements imparting delays to the strobe signal, Johnson's teachings of adjustable delays for both data and clock signals render this obvious. Applying adjustable delays to the strobe signal, as Johnson does for DCLK, would have been a straightforward extension of Johnson's techniques to improve timing margins. (EX1004, 1:12-26).

ii. Moss

143. Even if Johnson did not disclose this feature, Moss does. Moss teaches using a delay line 330 to delay the data strobe signal DQS 210 received from the memory component. (EX1006, Fig. 3, 6:16-22). This delayed strobe signal clocks register flip-flops 322 and 324 which capture the data returned from the memory component on signal DQ 208. (EX1006, Fig. 3, 6:28-35). While Moss shows a single delay line 330 for the strobe signal, it would have been obvious to implement separate delay elements for each data pin or group of data pins to allow finer-grained compensation for timing variations (*See supra*, § IX.A.b, IX.A.c).

144. Moss demonstrates using multiple programmable delay lines to adjust timing of different signals, such as delay line 306 for generating delayed clock signal CLK2 304. (EX1006, Fig. 3, 6:55-63). Applying this concept to provide individual delay elements for each data pin would have been an obvious extension of Moss's

teachings, allowing the memory controller to impart first and second delays to the strobe signal as it is used to capture data on different pins. (EX1006, 1:43-65).

iii. Motivation to Combine

145. A POSITA would have been motivated to combine the teachings of Johnson and Moss to arrive at the claimed first and second timing signal delay elements. Both references address timing control in memory systems and use delay elements to compensate for timing offsets. Combining Johnson's adjustable delays for multiple data paths with Moss's teaching of delaying the strobe signal would yield predictable results in enhancing memory controller performance. The integration of these features would provide the known benefits of improved timing control and signal integrity across multiple data paths, which are critical in high-speed memory interfaces.

j. 6: “The IC memory controller according to claim 1, wherein: each of the first and second delay elements comprise locked-loop circuits having plural serially connected delay elements.”

i. Johnson

146. Johnson discloses delay elements comprising locked-loop circuits having plural serially connected delay elements. Johnson teaches ring delay elements 57 in data paths DQ0-17, which are adjustable delay elements that can be set to different delay values. (EX1004, at Fig. 4, 4:4-17, 7:46-53). Figure 10 elaborates on these ring delays, showing elements 57a, 57b, and 57c in data paths DQ0, DQ1, and DQ2

respectively. (EX1004, at Fig. 10, 7:34-45). These ring delays have plural serially connected delay elements that can be selectively enabled to adjust the overall delay, consistent with a locked-loop circuit as claimed. (EX1004, at 7:46-53).

147. This configuration allows for fine-grained delay adjustment, enabling precise timing alignment of data signals critical for high-speed memory interfaces. (EX1004, at 1:38-43). The locked-loop structure provides feedback that helps maintain consistent delay characteristics across variations in temperature, voltage, and manufacturing process. (EX1004, at 1:38-43, 7:46-53).

ii. Moss

148. Even if Johnson did not disclose this feature, Moss renders it obvious. Moss describes programmable delay lines, such as delay line 306, used to generate delayed clock signals for compensating phase offset errors. (EX1006, at 6:56-63). While Moss does not explicitly state that these delay elements are locked-loop circuits with plural serially connected delay elements, a POSITA would have understood that programmable delay lines commonly utilize such an architecture.

149. Moss discusses the need to compensate for various sources of delay and phase variance, including clock jitter, thermal variations, and non-linear effects. (EX1006, at 6:8-15). A locked-loop circuit with multiple delay elements would be well-suited to address these challenges, as it could be calibrated to account for such variations and maintain precise timing across different operating conditions.

iii. Motivation to Combine

150. A POSITA would have been motivated to implement Moss's programmable delay lines using Johnson's locked-loop circuit architecture. Both references address timing control in high-speed memory interfaces and seek to improve signal alignment. Combining Johnson's explicit disclosure of ring delays with plural serially connected elements and Moss's teaching of programmable delay lines would yield predictable results in enhancing delay precision and adaptability. This combination would provide the known benefits of fine-grained delay adjustment and robustness against operational variations, which are critical in high-performance memory controllers.

k. 7: "The IC memory controller according to claim 6, wherein the first delay value is used to select delay elements of the first delay circuit and the second delay value is used to select delay elements of the second delay circuit."

i. Johnson

151. Johnson discloses using delay values to select delay elements in first and second delay circuits. Johnson's memory controller uses ring delay circuits as adjustable delay elements in data paths. (EX1004, 4:1-10). These ring delays, such as 57 and 57a-c in Figures 4 and 10, are locked-loop circuits with plural serially connected delay elements. (EX1004, Fig. 4, Fig. 10, 4:1-10). While not explicitly stated for ring delays 57 and 57a-c, Johnson teaches selecting delay elements based on delay values for other ring delays in the system. (EX1004, 4:38-43). A POSITA

would have understood this principle applies to all ring delays, including 57 and 57a-c. (EX1004, 4:38-43, Fig. 4, Fig. 10). This allows fine-tuning of each data path's timing independently, compensating for variations and achieving optimal alignment with the clock signal. (EX1004, 1:38-43, 4:38-50).

ii. Moss

152. Even if Johnson did not disclose this feature, Moss does. Moss's IC memory controller uses delay values to select delay elements in programmable delay lines (*See supra*, § IX.A.b, § IX.A.c). While not explicitly stated, a POSITA would have understood that the Delay DQS Rising 330 and Delay DQS Falling 328 circuits operate by using delay values to select delay elements. (EX1006, Fig. 3, 6:16-23). This allows precise adjustment of delays to match specific timing requirements. (EX1006, 6:64-7:4). The use of delay values to select delay elements is fundamental to programmable delay lines, enabling the controller to adjust delays based on predetermined phase offsets. (EX1006, 6:55-63).

iii. Motivation to Combine

153. A POSITA would have been motivated to combine Johnson's explicit teaching of using delay values to select delay elements with Moss's programmable delay lines. Both references address timing control in memory interfaces and seek to improve signal alignment. This combination would yield predictable results in

enhancing delay precision and adaptability, providing the known benefits of fine-grained delay adjustment critical in high-performance memory controllers.

l. 9: “The IC memory controller according to claim 1, further comprising a calibration circuit to, in a calibration mode, determine the first and second delay values.”

i. Johnson

154. Johnson discloses an IC memory controller with a calibration circuit that determines first and second delay values in a calibration mode. The control logic circuit 21 performs calibration of delay values for multiple data paths, specifically for ring delays 57a, 57b, and 57c associated with data paths DQ0, DQ1, and DQ2. (EX1004, at 6:35-45, 7:46-53).

155. During calibration, the control logic circuit 21 determines appropriate delay values for each ring delay to align data on different DQ paths. (EX1004, at 7:53-59). It compares timing of data on an uncalibrated path to a previously calibrated path, adjusting delay values until alignment is achieved. (EX1004, at 7:59-67). The circuit steps through multiple possible delay values, noting which produce proper alignment, and selects a final value at or near the center of acceptable values. (EX1004, at 8:1-10). This process compensates for timing variations between data paths, ensuring proper data sampling. (EX1004, at 1:38-43).

ii. Moss

156. Even if Johnson did not disclose this feature, Moss renders it obvious. Moss teaches a memory controller that uses predetermined delay values to compensate for phase offset errors. (EX1006, at 6:55-63). While Moss does not explicitly describe a calibration mode, it suggests that delay values are determined through external methods or calculated by the designer. (EX1006, at 6:64-7:2). A POSITA would recognize that implementing a calibration mode to determine these delay values would be a straightforward and beneficial extension of Moss's teachings, allowing for dynamic adjustment to system variations.

iii. Motivation to Combine

157. A POSITA would have been motivated to incorporate Johnson's explicit calibration mode into Moss's memory controller. Both references address timing control in memory systems and use delay values for signal alignment. Combining Johnson's calibration technique with Moss's programmable delays would yield predictable results in enhancing memory controller performance, providing the known benefits of adaptive timing control critical in high-speed memory interfaces.

m. 10[pre]: "A method of operation in an IC memory controller, the method comprising:"

i. Johnson

158. Johnson discloses a method of operation in an IC memory controller. The memory controller in Johnson coordinates data flow and timing in the memory

system, executing specific steps and procedures to ensure proper functioning. (EX1004, at 3:34-41, 4:28-43). Johnson's method includes initializing the memory system, performing calibration procedures, and managing ongoing data transfer operations. (EX1004, at 1:38-43, 4:28-43). Figure 5 illustrates the timing relationships between various signals, demonstrating how the memory controller manages the timing of command clock (CCLK), FLAG, command (CMD), and data (DQ/DBUS) signals as part of its operational method. (EX1004, at 4:61-67, 5:1-7).

159. The method incorporates adaptive techniques that allow the memory controller to adjust its operation based on changing system conditions or requirements, enabling optimization of performance across various operating conditions. (EX1004, at 2:47-53).

ii. Moss

160. Even if Johnson did not disclose this feature, Moss does. Moss discloses a method of operation in an IC memory controller for realigning read data returned from memory components to adjust for phase shifts due to propagation delays and other factors. (EX1006, at Abstract, 1:43-54). This method operates within the memory controller circuit 300 to synchronize signals exchanged between the controller and memory devices. (EX1006, at 5:51-55). The memory controller 300 contains various circuit elements including delay lines, registers, and control logic that implement the realignment method. (EX1006, at 5:51-6:38).

161. While Moss does not explicitly label this as “a method of operation in an IC memory controller,” a POSITA would have understood that the disclosed realignment technique constitutes such a method. (EX1006, at Abstract, 5:33-37, 6:36-7:46).

iii. Motivation to Combine

162. A POSITA would have been motivated to combine the methods of Johnson and Moss to create a comprehensive method of operation for an IC memory controller. Both references address timing control and signal synchronization in memory systems. Combining Johnson’s adaptive techniques with Moss’s realignment method would yield predictable results in enhancing memory controller performance, providing the benefits of both adaptive timing control and precise signal alignment critical in high-speed memory interfaces.

n. 10[a]: “receiving first and second data signals from a memory device at respective first and second pins;”

i. Johnson

163. Johnson discloses receiving first and second data signals from a memory device at respective first and second pins. Johnson’s memory controller receives data signals from a memory module over a bi-directional data bus DQ0-17, which comprises multiple data paths connected to respective pins on the memory controller. (EX1004, Fig. 3, 3:31-45, Fig. 4, 3:65-4:18). For example, a first data signal is received on a first DQ data path at a first pin connected to a first input buffer 51,

while a second data signal is received on a second DQ data path at a second pin connected to a second input buffer 51. (EX1004, Fig. 4, 4:13-18). These data signals are received from memory banks 69, 71 of the memory module during read operations. (EX1004, Fig. 4, 3:40-45, 4:13-18).

ii. Moss

164. Even if Johnson did not disclose this feature, Moss does. Moss's memory controller receives multiple data signals from a DDR SDRAM memory component at corresponding pins. (EX1006, Fig. 3, Abstract). The controller receives a data signal DQ 208 from the memory component 220, representing multiple data bits transmitted in parallel. (EX1006, Fig. 3, 5:28-33, 6:39-49). For a typical 8-bit wide DDR SDRAM, this corresponds to 8 separate data signals received at 8 respective pins of the memory controller. (EX1006, 6:39-49). Register flip-flops 322 and 324 capture the received data signals on both rising and falling edges of the data strobe DQS 210, effectively doubling the data rate. (EX1006, Fig. 3, 6:28-38).

iii. Motivation to Combine

165. A POSITA would have been motivated to combine the teachings of Johnson and Moss to achieve the claimed method of receiving first and second data signals. Both references address high-speed data transfer in memory systems using multiple data pins. Combining Johnson's explicit disclosure of multiple data paths with Moss's teaching of capturing data on both clock edges would yield predictable

results in enhancing memory controller performance, providing the known benefits of increased data bandwidth in high-speed memory interfaces.

o. 10[b]: “aligning the received first and second data signals with a strobe signal, the aligning comprising imparting a first delay to the first data signal, the first delay corresponding to a first delay value, imparting a second delay to the second data signal, the second delay corresponding to a second delay value.”

i. Johnson

166. Johnson discloses aligning received data signals with a strobe signal by imparting delays to the data signals. Johnson’s memory controller aligns first and second data signals received from a memory device with a strobe signal. (EX1004, 1:27-31, 4:37-43). This alignment is accomplished using adjustable delay elements to delay the received data signals and generate delayed data signals. (EX1004, 4:43-56, Fig. 4). The delay imparted to each data signal corresponds to a delay value determined during a calibration process. (EX1004, 5:4-14).

167. Johnson uses separate adjustable delay elements with individually calibrated delay values for each data signal, compensating for timing variations between different data signals and achieving precise alignment with the strobe signal. (EX1004, 1:12-26, 4:37-50). This approach improves the reliability of data sampling in high-speed memory interfaces where timing margins are critical. (EX1004, 1:6-11, 1:38-43).

ii. Moss

168. Even if Johnson did not disclose this feature, Moss does. Moss teaches a memory controller that aligns received data signals (DQ) with a strobe signal (DQS) by imparting delays. (EX1006, Fig. 3, 5:51-61). Delay lines 328 and 330 delay the rising and falling edges of the data strobe DQS 210, which is then used to sample and register the received data signals DQ 208. (EX1006, Fig. 3, 6:16-35).

169. These delays compensate for timing offsets between the received data signals and the strobe signal, ensuring optimal data sampling. (EX1006, 4:43-54, 6:24-26). Moss allows for predetermined delay values to be programmed into the delay lines, enabling adaptation to specific system configurations and operating conditions. (EX1006, 6:55-68, 7:1-4).

iii. Motivation to Combine

170. A POSITA would have been motivated to combine Johnson's individually calibrated delay elements with Moss's programmable delay lines. Both references address timing control in high-speed memory interfaces and seek to improve signal alignment. This combination would yield predictable results in enhancing delay precision and adaptability, providing the known benefits of fine-grained delay adjustment critical in high-performance memory controllers.

p. 11: “The method according to claim 10, further comprising: in a calibration mode, determining the first and second delay values; and storing the first and second delay values.”

i. Johnson

171. Johnson discloses determining and storing first and second delay values in a calibration mode. During calibration, Johnson’s control logic circuit 21 steps through possible delay values for ring delays in each data path, determining which produce proper recognition of a known calibration pattern. (EX1004, 5:50-61). The circuit selects a final delay value for each path centered between acceptable delays, effectively determining first and second delay values. (EX1004, 5:67-6:5). Johnson necessarily stores these delay values to track them during calibration and apply them to ring delays in normal operation. (EX1004, 1:69-2:2, 5:61-6:5). This calibration occurs during initialization, constituting a calibration mode. (EX1004, 1:40-43).

ii. Moss

172. Even if Johnson did not disclose this feature, Moss does. Moss determines delay values during calibration to compensate for phase offsets between clock and strobe signals. (EX1006, 5:58-63, 6:55-59). This process calculates multiple delay values, including for clock and data signal paths. (EX1006, 7:5-10). Moss stores these calibrated values for quick configuration of programmable delay lines without recalibration. (EX1006, 7:10-20). The delay line 306 in Figure 3 uses these stored values to realign clock and data signals during read operations. (EX1006, Fig. 3, 6:55-65).

iii. Motivation to Combine

173. A POSITA would have been motivated to combine Johnson's calibration process with Moss's storage and reuse of delay values. Both references address timing control in memory systems and seek to improve signal alignment. This combination would yield predictable results in enhancing calibration efficiency and adaptability, providing the known benefits of quick reconfiguration without full recalibration, which is critical in high-performance memory controllers.

**q. 12: "The method according to claim 11, wherein:
during the receiving mode,
the imparting the first and second delays includes retrieving the
stored first and second delay values."**

i. Johnson

174. Johnson discloses retrieving stored delay values during a receiving mode to impart delays to incoming data signals. During normal operation, Johnson's memory controller retrieves previously determined and stored delay values to set appropriate delays for each data path. (EX1004, 7:54-59). This retrieval and application of stored delay values directly corresponds to the claimed "imparting the first and second delays includes retrieving the stored first and second delay values" during a receiving mode. (EX1004, 1:64-2:2, 7:54-59). By using stored delay values, Johnson's system can quickly configure data paths for proper timing alignment when entering a receiving mode, eliminating the need for recalibration and improving system efficiency. (EX1004, 1:38-2:9).

ii. Moss

175. Even if Johnson did not disclose this feature, Moss does. Moss's memory controller uses stored delay values to configure programmable delay lines during read operations, which correspond to a receiving mode. (EX1006, 6:55-65, 7:10-20). The delay line 306 in Figure 3 uses these stored values to realign clock and data signals, effectively imparting delays based on retrieved delay values. (EX1006, Fig. 3, 6:55-65).

iii. Motivation to Combine

176. A POSITA would have been motivated to combine Johnson's explicit teaching of retrieving stored delay values during operation with Moss's use of stored values for quick reconfiguration. Both references address timing control in memory systems and seek to improve signal alignment efficiency. This combination would yield predictable results in enhancing system performance by allowing rapid adjustment to changing conditions without full recalibration, which is critical in high-speed memory interfaces.

**r. 13: "The method according to claim 12, wherein:
the first and second data signals are delayed by the first and
second delay values."**

i. Johnson

177. Johnson discloses delaying first and second data signals by first and second delay values. Johnson's memory controller uses adjustable delay elements in

multiple data paths to align data signals with a clock signal. (EX1004, Abstract, 3:50-67, Fig. 4). The control logic circuit 21 adjusts delay values for ring delays 27 and 29 in different data paths to align data signals with the clock signal CCLK. (EX1004, 5:50-67, 6:1-14). During calibration, the control logic determines optimal delay values for each data path. (EX1004, 6:15-30). These calibrated delay values are stored and used during normal operation to apply appropriate delays to incoming data signals on each path. (EX1004, 6:31-56).

ii. Moss

178. Even if Johnson did not disclose this feature, Moss does. Moss's memory controller uses programmable delay lines to delay data signals based on predetermined delay values (*See supra*, § IX.A.o). These delay values are calculated to compensate for phase offset errors and ensure optimal data capture. (EX1006, 6:64-7:4). Moss applies these delays to align data signals with the controller's clock domain, enabling reliable data capture. (EX1006, 5:43-61).

iii. Motivation to Combine

179. A POSITA would have been motivated to combine Johnson's individually calibrated delay elements with Moss's programmable delay lines. Both references address timing control in high-speed memory interfaces and seek to improve signal alignment. This combination would yield predictable results in enhancing delay

precision and adaptability, providing the known benefits of fine-grained delay adjustment critical in high-performance memory controllers.

s. 14: “The method according to claim 11, further comprising: during the calibration mode, calibrating a timing signal delay value corresponding to a delay for application to the strobe signal.”

i. Johnson

180. Johnson discloses calibrating a timing signal delay value corresponding to a delay for application to the strobe signal during a calibration mode. Johnson’s SLD RAM device includes a calibration strobe delay element to impart a calibrated delay to the strobe signal. (EX1004, 4:24-27). During calibration, the control logic circuit 21 steps through possible delay values for both data and strobe signals, determining an optimal internal delay for clock signals, including the strobe signal, relative to data signals. (EX1004, 5:29-40, 5:60-67). This process establishes an “eye” or “window” of acceptable delays for proper data sampling, ensuring the strobe signal is timed to sample data signals in the center of their respective data eyes. (EX1004, 6:41-56).

181. This calibration compensates for variations in device parameters and maintains proper timing relationships between strobe and data signals across varying operating conditions. (EX1004, 1:38-43, 2:1-21).

ii. Moss

182. Even if Johnson did not disclose this feature, Moss does. Moss's memory controller generates a delayed clock signal CLK2 from the controller's clock signal CLK using a programmable delay line 306 to compensate for phase offset errors between CLK and the data strobe signal DQS. (EX1006, Fig. 3, 6:55-63). The delay value is calibrated during what can be considered a calibration mode, based on the accumulated phase variance 308 between CLK and DQS. (EX1006, Fig. 3, 6:4-15, 6:64-7:4).

iii. Motivation to Combine

183. A POSITA would have been motivated to combine Johnson's explicit calibration of strobe signal delay with Moss's programmable delay line for clock signal adjustment. Both references address timing control in memory systems and seek to compensate for phase offsets. This combination would yield predictable results in enhancing timing precision, providing the known benefits of adaptive timing control critical in high-speed memory interfaces.

**t. 15: "The method according to claim 14, further comprising:
during the calibration mode,
storing the calibrated timing delay value."**

i. Johnson

184. Johnson discloses storing the calibrated timing delay value during the calibration mode. As discussed previously, Johnson's control logic circuit 21

determines optimal delay values for both data and strobe signals during calibration (*See supra*, § IX.A.s.i). These calibrated delay values, including the timing delay value for the strobe signal, are necessarily stored for use during normal operation. (EX1004, 1:69-2:2, 5:61-6:5). Johnson's system uses these stored delay values to quickly configure data paths and strobe timing when entering a receiving mode, eliminating the need for recalibration and improving system efficiency. (EX1004, 1:38-43, 2:1-9).

ii. Moss

185. Even if Johnson did not disclose this feature, Moss does. Moss's memory controller stores calibrated delay values for quick configuration of programmable delay lines, including the delay line 306 used for clock signal adjustment (*See supra*, § IX.A.s.ii). These stored values allow the controller to rapidly adjust timing relationships without full recalibration, enhancing system performance in high-speed memory interfaces. (EX1006, 7:10-20).

iii. Motivation to Combine

186. A POSITA would have been motivated to combine Johnson's explicit calibration and storage of delay values with Moss's use of stored values for quick reconfiguration. Both references address timing control in memory systems and seek to improve signal alignment efficiency. This combination would yield predictable results in enhancing system performance by allowing rapid adjustment to changing

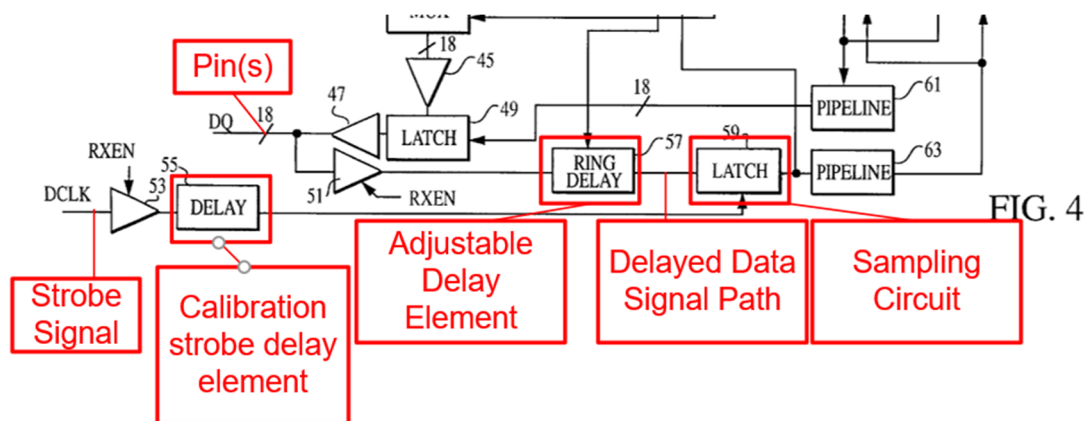
conditions without full recalibration, which is critical in high-speed memory interfaces.

B. Ground 2: Johnson, in view of Moss, in further view of Liou

a. 8: “The IC memory controller according to claim 1, further comprising a calibration strobe delay element to impart a calibrated delay to the strobe signal.”

i. Johnson

187. Johnson discloses a calibration strobe delay element to impart a calibrated delay to the strobe signal as recited in claim 8. Specifically, Johnson teaches a delay circuit 55 that delays the data clock signal DCLK, which corresponds to the claimed strobe signal. (EX1004, at 4:24-27). This delay circuit 55 is part of the calibration circuitry used to align incoming data with the clock signal. (EX1004, at 4:20-27). The delay imparted by delay circuit 55 is calibrated during a calibration mode to determine the optimal delay for properly sampling incoming data. (EX1004, at 4:27-41).



(EX1004, Fig 4 (annotated excerpt)).

188. The calibration process involves stepping through different delay values for delay circuit 55 to find a range of acceptable delays that allow proper sampling of a known calibration pattern. (EX1004, at 5:14-40). Once this range is determined, a final calibrated delay value is selected, typically near the center of the range of acceptable delays. (EX1004, at 5:36-40). This calibrated delay value is then used during normal operation to properly align the DCLK signal with incoming data for accurate sampling. (EX1004, at 5:65-6:2).

189. The purpose of this calibration strobe delay element is to compensate for timing variations and ensure proper data sampling across different operating conditions. (EX1004, at 1:38-43). By calibrating the delay imparted to the strobe signal, the memory controller can maintain accurate timing relationships between the strobe and data signals, which is critical for high-speed memory interfaces. (EX1004, at 1:12-21). This calibration capability allows the memory controller to adapt to different system configurations and environmental factors that may affect signal timing. (EX1004, at 1:38-43).

190. Johnson's calibration strobe delay element provides the same functionality as the claimed element-it imparts a calibrated delay to a strobe signal used for sampling data. This allows the memory controller to optimize timing margins and improve data reliability in high-speed memory interfaces. (EX1004, at 1:21-26, 1:38-43).

ii. Liou

191. Even if Johnson did not disclose this limitation, Liou does. Liou discloses an integrated circuit memory controller comprising a calibration strobe delay element to impart a calibrated delay to the strobe signal, as recited in claim 8. Specifically, Liou teaches a first delay circuit 110 that delays the data strobe signal DQS by a controlled delay value. (EX1007, at [0023]). This first delay circuit 110 functions as a calibration strobe delay element by imparting a calibrated delay to the DQS strobe signal. (EX1007, at [0023]).

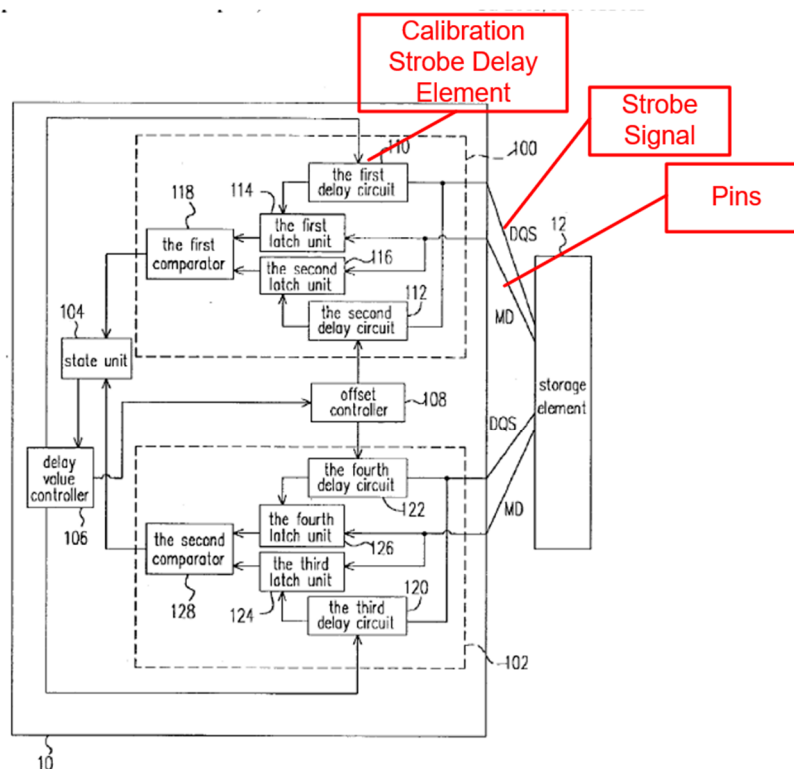


FIG. 2

(EX1004, Fig. 2 (annotated)).

192. The controlled delay value used by the first delay circuit 110 is provided by a delay value controller 106. (EX1007, at [0021], [0023]). This delay value controller 106 stores an initial controlled delay value that can be set by the BIOS during system initialization. (EX1007, at [0021]). Importantly, the delay value controller 106 can dynamically adjust the controlled delay value based on feedback from comparison circuits. (EX1007, at [0025-0026]). This dynamic adjustment allows the delay imparted to the strobe signal to be calibrated in real-time to account for factors like temperature and voltage variations that may affect signal timing. (EX1007, at [0007], [0011]).

193. The first delay circuit 110 receives the DQS0 strobe signal as an input and outputs a delayed version of DQS0 based on the controlled delay value from the delay value controller 106. (EX1007, at [0023], Fig. 2). This delayed DQS0 signal is then used to latch the corresponding data signal MD7 in the first latch unit 114. (EX1007, at [0023]). By adjusting the controlled delay value, the system can calibrate the timing of the strobe signal relative to the data signal to ensure accurate data capture. (EX1007, at [0007], [0025-0026]).

C. Ground 3: Stubbs, in view of Moss

a. 1[pre]: “An integrated circuit (IC) memory controller comprising:”

i. Stubbs

194. Stubbs discloses an integrated circuit (IC) memory controller. Stubbs describes a synchronous double-data-rate semiconductor memory device with input/output circuitry coupled between a memory bank and external input/output terminals. (EX1005, Abstract, [0007], [0027]). This input/output circuitry, comprising write path circuits, functions as an integral component of an IC memory controller. (EX1005, [0028], [0032]). The device operates as a double-data-rate (DDR) synchronous dynamic random access memory (SDRAM), necessitating sophisticated memory controller functionality to manage high-speed data transfers on both rising and falling clock edges. (EX1005, [0027], [0012-0013]). This DDR operation inherently requires an integrated circuit memory controller to properly time and coordinate data and strobe signals. (EX1005, [0012-0013], [0032-0033]).

ii. Moss

195. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.a.ii.

iii. Motivation to Combine

196. A POSITA would have been motivated to combine the teachings of Stubbs and Moss to arrive at the claimed IC memory controller. Both references address high-speed memory interfaces and seek to improve data transfer efficiency. Combining Stubbs’ DDR SDRAM architecture with Moss’s explicit IC memory

controller implementation would yield predictable results in enhancing memory controller performance. This combination would provide the known benefits of precise timing control and signal integrity, which are critical in high-speed memory interfaces.

**b. 1[a]: “a first pin to receive a first data signal;
a first adjustable delay element to delay the received first data
signal and generate a first delayed data signal;”**

i. Stubbs

197. Stubbs discloses a first pin to receive a first data signal and a first adjustable delay element to delay the received first data signal and generate a first delayed data signal. Stubbs’ write path circuit includes an input buffer that receives data from an external data pin, corresponding to the claimed first pin. (EX1005, Fig. 4, [0028], [0047]). The circuit also includes a first delay element coupled to the input buffer’s output, which is adjustable and generates a first delayed data signal. (EX1005, Fig. 4, [0047], [0048]). This adjustable delay element allows for independent optimization of setup and hold times for rising and falling edge data. (EX1005, [0048]). Stubbs’ delay elements can be implemented using various techniques like inverter chains or RC delay circuits, with selectable delay values, enabling fine-tuning for specific system requirements. (EX1005, [0050-0053]).

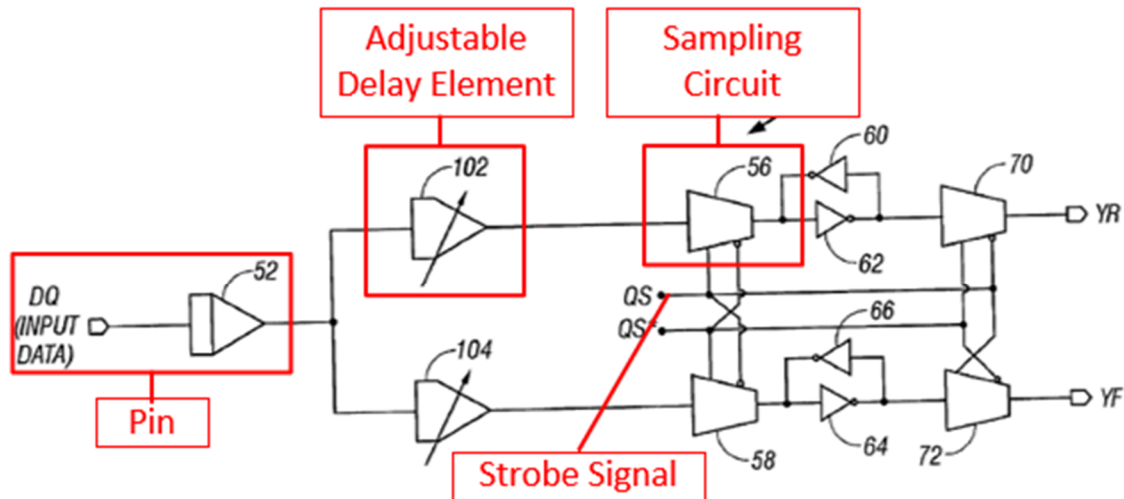


FIGURE 4

(EX1005, Fig. 4 (annotated)).

ii. Moss

198. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.b.ii.

iii. Motivation to Combine

199. A POSITA would have been motivated to combine Stubbs' adjustable delay elements with Moss's memory controller design. Both references address timing control in high-speed memory interfaces. This combination would yield predictable results in enhancing delay precision and adaptability, providing the known benefits of fine-grained delay adjustment critical in high-performance memory controllers.

c. 1[b]: “a second pin to receive a second data signal; a second adjustable delay element to delay the received second data signal and generate a second delayed data signal;”

i. Stubbs

200. Stubbs discloses a second pin to receive a second data signal and a second adjustable delay element to delay the received second data signal and generate a second delayed data signal. Stubbs teaches that the write path circuit shown in Fig. 4 is provided for each input/output (DQ) pin of the memory device. (EX1005, [0047]). The memory device contains multiple input/output pins, typically eight in a “by 8” device configuration, but potentially fewer or more depending on the specific device. (EX1005, [0029]). For each of these input/output pins, a separate write path circuit is provided, which includes an input buffer and an adjustable delay element. (EX1005, [0047], [0048]). This structure directly corresponds to the claimed second pin and second adjustable delay element, as one of the additional DQ pins beyond the first would serve as this second pin, with its associated delay element allowing for independent optimization of setup and hold times. (EX1005, [0048]).

ii. Moss

201. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.c.ii.

iii. Motivation to Combine

202. A POSITA would have been motivated to combine Stubbs’ multiple adjustable delay elements with Moss’s memory controller design. Both references address

timing control in high-speed memory interfaces with multiple data signals. This combination would yield predictable results in enhancing delay precision and adaptability across multiple data paths, providing the known benefits of fine-grained delay adjustment critical in high-performance memory controllers.

d. 1[c]: “a pin to receive a strobe signal;”

i. Stubbs

203. Stubbs discloses a pin to receive a strobe signal. The memory device receives an externally-applied clock signal CLK at an input pin. (EX1005, at [0005], [0007]). This external clock signal is used to generate an internal data strobe signal QS/QS that controls the sampling of input data. (EX1005, at [0035], [0036]). The QS/QS signal is derived from the external clock signal CLK and closely follows it, possibly with a small propagation delay. (EX1005, at [0035]). This dedicated pin for receiving the clock signal allows the memory device to synchronize its internal operations with the external system timing, ensuring data is captured at appropriate times. (EX1005, at [0035], [0036]).

204. The QS/QS* signal permits proper operation of the double-data-rate memory device, controlling the opening and closing of pass gates in the write data path to properly capture and route rising and falling edge data. (EX1005, at [0036], [0037]). This dedicated pin allows the memory device to maintain precise synchronization

with the external system, which is particularly important in high-speed memory applications where timing margins are critical. (EX1005, at [0004], [0005], [0007]).

ii. Moss

205. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.d.ii.

iii. Motivation to Combine

206. A POSITA would have been motivated to combine Stubbs' clock signal input pin with Moss's explicit strobe signal pin. Both references address timing control in high-speed memory interfaces. This combination would yield predictable results in enhancing synchronization precision, providing the known benefits of accurate data sampling critical in high-performance memory controllers.

e. 1[d]: “a first sampling circuit to sample the first delayed data signal based on the strobe signal; and”

i. Stubbs

207. Stubbs discloses a first sampling circuit to sample the first delayed data signal based on the strobe signal. Specifically, Stubbs teaches a first pass gate 56 that samples a delayed data signal output from delay element 102 based on a data strobe signal QS/QS*. (EX1005, Fig. 4, [0037]). The pass gate 56 functions as a sampling circuit by selectively allowing the delayed data signal to pass through to its output under control of the data strobe signal QS/QS* applied to its control inputs. (EX1005, [0034], [0036]). This sampling operation is illustrated in Figure 3, which

shows the data signal being sampled on the rising edge of the QS strobe signal.
(EX1005, Fig. 3, [0039]).

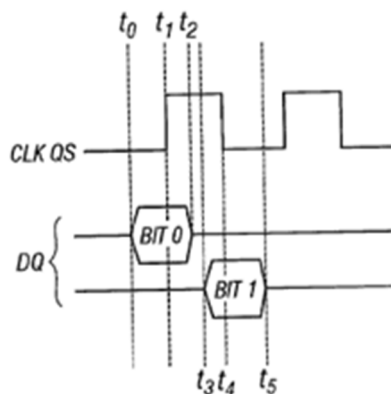


FIGURE 3

(EX1005, Fig. 3).

ii. Moss

208. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.e.ii.

iii. Motivation to Combine

209. A POSITA would have been motivated to combine Stubbs' pass gate sampling circuit with Moss's memory controller design. Both references address data sampling in high-speed memory interfaces. This combination would yield predictable results in enhancing sampling precision, providing the known benefits of accurate data capture critical in high-performance memory controllers.

f. 1[e]: “a second sampling circuit to sample the second delayed data signal based on the received strobe signal.”

i. Stubbs

210. Stubbs discloses a second sampling circuit to sample the second delayed data signal based on the received strobe signal. The write path circuitry shown in Figure 4, including the sampling circuits, is replicated for each input/output (DQ) pin of the memory device. (EX1005, [0046]). This means that in addition to the first sampling circuit (pass gate 56) discussed previously, there is a second sampling circuit for a second data pin. Each data pin has its own pair of sampling circuits (pass gates 56 and 58) to handle the rising-edge and falling-edge data. (EX1005, [0046], [0029]). This replication allows for parallel processing of multiple data bits, enabling the high data rates required in double data rate (DDR) operation. (EX1005, [0012]).

ii. Moss

211. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.f.ii.

iii. Motivation to Combine

212. A POSITA would have been motivated to combine Stubbs’ multiple sampling circuits with Moss’s memory controller design. Both references address data sampling in high-speed memory interfaces with multiple data signals. This combination would yield predictable results in enhancing sampling precision across multiple data paths, providing the known benefits of accurate data capture critical in high-performance memory controllers.

g. 2: “The IC memory controller according to claim 1, further comprising storage to store each of first and second delay values corresponding to the delays imparted to the first and second data signals.”

i. Stubbs

213. Stubbs implicitly discloses storage to store first and second delay values corresponding to the delays imparted to the first and second data signals. Stubbs teaches adjustable delay elements to achieve predetermined timed relationships between delayed data signals and data strobe edges. (EX1005, at [0048]). To maintain these adjusted delay values across power cycles or resets, a POSITA would recognize the necessity of storing these values in non-volatile storage. (EX1005, at [0048]). Stubbs also describes a calibration mode for determining delay values, which would require storage for subsequent use during normal operation. (EX1005, at [0018]). Furthermore, Stubbs’ disclosure of locked-loop circuits with plural serially connected delay elements implies the need for storing delay values to select specific delay elements. (EX1005, at [0006], [0007]). Storing calibrated delay values allows for quick setup of correct timing relationships without time-consuming recalibration, improving overall efficiency and reliability of the memory system. (EX1005, at [0002-0004], [0047-0048]).

ii. Moss

214. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.g.ii.

iii. Motivation to Combine

215. A POSITA would have been motivated to combine Stubbs' adjustable delay elements with Moss's explicit storage of delay values. Both references address timing control in high-speed memory interfaces. This combination would yield predictable results in enhancing system efficiency by allowing quick reconfiguration of delay values without repeated calibration, which is critical in high-performance memory controllers.

h. 4: "The IC memory controller according to claim 1, wherein the first and second data signals are delayed to compensate for timing offset between the received first and second data signals."

i. Stubbs

216. Stubbs discloses an IC memory controller that delays first and second data signals to compensate for timing offset between the received signals. The write path circuitry includes separate adjustable delay elements for rising edge data (first data signal) and falling edge data (second data signal). (EX1005, Fig. 4, elements 102 and 104). These delay elements allow independent adjustment of setup and hold times for rising and falling edge data. (EX1005, [0047]). Stubbs adjusts the delay elements to achieve a predetermined timed relationship between the delayed data signals and the rising and falling edges of the data strobe signal, corresponding to the specified setup and hold window for the device. (EX1005, [0018]). This

adjustment compensates for timing offsets between the received first and second data signals.

ii. Moss

217. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.h.ii.

iii. Motivation to Combine

218. A POSITA would have been motivated to combine Stubbs' adjustable delay elements with Moss's timing offset compensation techniques. Both references address timing control in high-speed memory interfaces. This combination would yield predictable results in enhancing signal alignment precision, providing the known benefits of improved timing margins critical in high-performance memory controllers.

i. 5: “The IC memory controller according to claim 4, further comprising: a first timing signal delay element associated with the first pin; and a second timing signal delay element associated with the second pin; wherein each of the first and second timing signal delay elements impart first and second delays to the strobe signal.”

i. Stubbs

219. Stubbs discloses timing signal delay elements associated with data input pins that impart delays to the strobe signal. Stubbs teaches a write path circuit for a double-data-rate synchronous memory device with multiple data input pins and associated delay elements. (EX1005, Fig. 4, [0047]). The circuit includes a first data pin (DQ) connected to an input buffer 52 and a first adjustable delay element 102,

with a second data pin implicitly disclosed as the circuitry is provided “for each input/output (DQ) pin of device 10.” (EX1005, Fig. 4, [0046-0047]). These delay elements correspond to the claimed first and second timing signal delay elements associated with the first and second pins. (EX1005, [0047]).

220. While Stubbs primarily discusses delaying data signals, it also teaches that the same delay elements can be used to delay the strobe signal. Given that Stubbs adjusts the timing relationship between data signals and strobe signal edges, it would have been obvious to a POSITA that the delay elements could delay either the data signals or the strobe signal to achieve the desired timing relationship. (EX1005, [0047-0048]). This arrangement allows independent optimization of setup and hold times for rising and falling edge data, enabling memory devices to meet more stringent timing specifications by compensating for signal propagation differences. (EX1005, [0015-0016], [0047-0048]).

ii. Moss

221. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.i.ii.

iii. Motivation to Combine

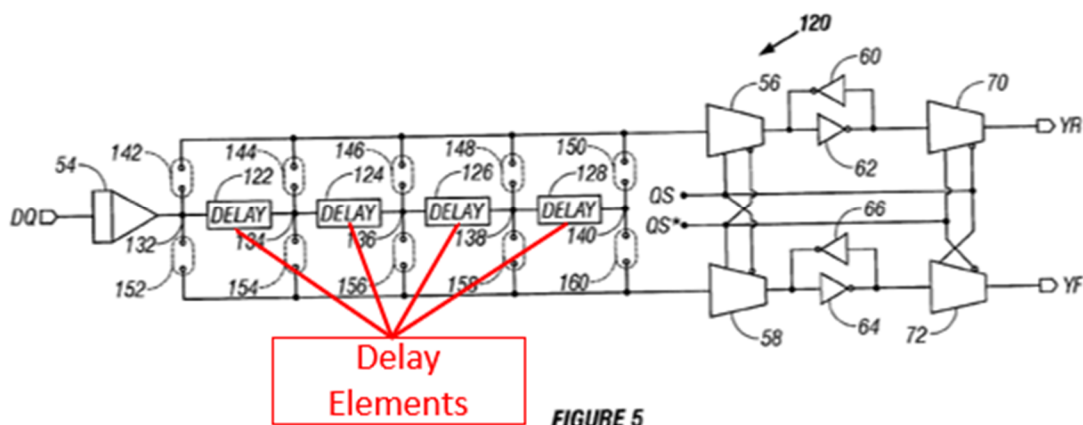
222. A POSITA would have been motivated to combine Stubbs’ adjustable delay elements with Moss’s explicit timing signal delay elements. Both references address timing control in high-speed memory interfaces. This combination would yield predictable results in enhancing signal alignment precision, providing the known

benefits of improved timing margins critical in high-performance memory controllers.

j. 6: “The IC memory controller according to claim 1, wherein: each of the first and second delay elements comprise locked-loop circuits having plural serially connected delay elements.”

i. Stubbs

223. Stubbs discloses delay elements comprising locked-loop circuits having plural serially connected delay elements. Stubbs teaches a write path circuit with adjustable delay elements 102 and 104 for independently adjusting the timing of rising and falling edge data signals. (EX1005, [0047-0048], Fig. 4). These delay elements are implemented as a network of series-connected delay elements 122, 124, 126, and 128, forming a locked-loop circuit that generates precisely timed delayed versions of the input data signal. (EX1005, [0051-0053], Fig. 5). This configuration allows for fine-grained control over the delay interval by selecting different tap points along the series, enabling precise timing adjustments to optimize setup and hold times for both rising and falling edge data in a DDR memory controller. (EX1005, [0053-0054]).



(EX1005, Fig. 5 (annotated)). The locked-loop circuit with plural serially connected delay elements provides advantages such as independent adjustment of rising and falling edge data timing and flexibility in accommodating various system timing requirements. (EX1005, [0015], [0048], [0006], [0053]).

ii. Moss

224. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.f.ii.

iii. Motivation to Combine

225. A POSITA would have been motivated to combine Stubbs' locked-loop circuits with Moss's delay elements. Both references address timing control in high-speed memory interfaces. This combination would yield predictable results in enhancing delay precision and adaptability, providing the known benefits of fine-grained delay adjustment critical in high-performance memory controllers.

k. 7: “The IC memory controller according to claim 6, wherein the first delay value is used to select delay elements of the first delay circuit and the second delay value is used to select delay elements of the second delay circuit.”

i. Stubbs

226. Stubbs discloses using first and second delay values to select delay elements of first and second delay circuits. Stubbs’ write data path circuit includes adjustable delay elements for independently controlling the timing of rising and falling edge data. (EX1005, [0047-0048]). The delay circuit comprises series-connected delay elements 122, 124, 126, and 128 with multiple tap points 130, 132, 134, 136, 138, and 140. (EX1005, [0051-0052], Fig. 5). Selecting different tap points for rising and falling edge data paths corresponds to using first and second delay values to select delay elements. (EX1005, [0053]). For example, selecting tap point 144 for rising edge data introduces one unit of delay, while selecting tap point 156 for falling edge data introduces two units of delay. (EX1005, [0053]). This selective coupling of delay elements based on chosen tap points is equivalent to using delay values to select delay elements of respective delay circuits. (EX1005, [0053]).

ii. Moss

227. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.f.ii.

iii. Motivation to Combine

228. A POSITA would have been motivated to combine Stubbs’ selectable delay elements with Moss’s delay value selection technique. Both references address

timing control in high-speed memory interfaces. This combination would yield predictable results in enhancing delay precision and adaptability, providing the known benefits of fine-grained delay adjustment critical in high-performance memory controllers.

l. 9: “The IC memory controller according to claim 1, further comprising a calibration circuit to, in a calibration mode, determine the first and second delay values.”

i. Stubbs

229. Stubbs discloses a calibration circuit that operates in a calibration mode to determine first and second delay values for adjusting the timing of data signals in a DDR memory controller. The calibration circuit optimizes setup and hold times for rising edge and falling edge data relative to the data strobe signal. (EX1005, at [0018], [0019]). This allows the memory controller to independently adjust timing for rising and falling edge data to achieve proper alignment with the data strobe signal, compensating for timing variations between data paths. (EX1005, at [0015], [0018], [0019]).

230. While Stubbs does not explicitly label the calibration circuit as a separate component, a POSITA would have understood that the described functionality for determining and applying delay values in a calibration mode necessarily requires dedicated calibration circuitry within the memory controller. (EX1005, at [0018], [0019]).

ii. Moss

231. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.1.ii.

iii. Motivation to Combine

232. A POSITA would have been motivated to combine Stubbs' calibration functionality with Moss's explicit calibration circuit. Both references address timing control in high-speed memory interfaces. This combination would yield predictable results in enhancing delay precision and adaptability, providing the known benefits of optimized timing critical in high-performance memory controllers.

m. 10[pre]: "A method of operation in an IC memory controller, the method comprising:"

i. Stubbs

233. Stubbs discloses a method of operation in an IC memory controller. The memory device includes controller components such as control circuit 12, addressing circuit 40, and input/output circuit 30, which manage data flow to and from memory banks 20. (EX1005, at [0028], Fig. 1). The method involves receiving data signals, aligning them with a strobe signal, and applying delays to ensure proper timing relationships in a double-data-rate system. (EX1005, at [0012], [0041-0044]). This approach addresses critical timing issues in high-speed data transfer, ensuring accurate data capture and processing. (EX1005, at [0012-0015], [0041-0044]).

ii. Moss

234. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.m.ii.

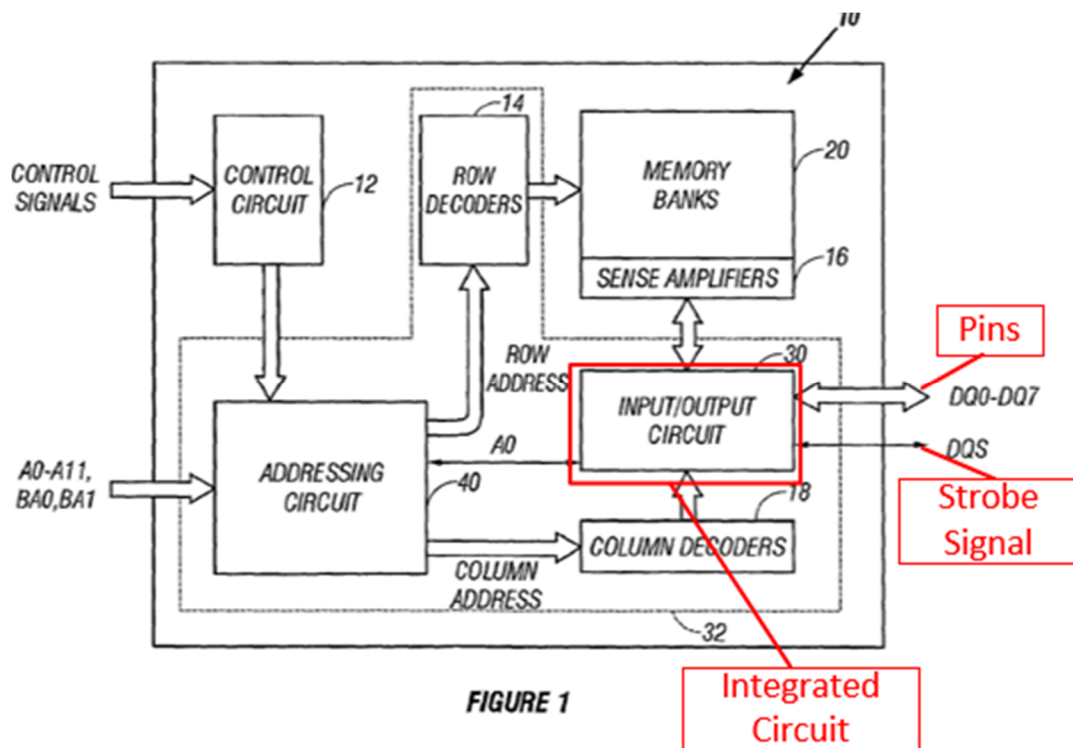
iii. Motivation to Combine

235. A POSITA would have been motivated to combine Stubbs' method of operation with Moss's explicit IC memory controller implementation. Both references address high-speed memory interfaces and seek to improve data transfer efficiency. This combination would yield predictable results in enhancing memory controller performance, providing the known benefits of precise timing control critical in high-speed memory interfaces.

n. 10[a]: "receiving first and second data signals from a memory device at respective first and second pins;"

i. Stubbs

236. Stubbs discloses receiving first and second data signals from a memory device at respective first and second pins. The memory device contains multiple input/output pins, such as DQ0-DQ7, for receiving data signals in parallel. (EX1005, [0029]).



(EX1005, Fig. 1 (annotated)).

237. These pins correspond directly to the first and second pins recited in the challenged claim. (EX1005, [0029]). In Stubbs' DDR SDRAM architecture, data is received on both rising and falling clock edges, with one pin receiving data on the rising edge and another on the falling edge, effectively doubling the data transfer rate. (EX1005, [0012], [0029]).

238. The received data signals propagate from input buffers through adjustable delay elements before being captured by pass gates controlled by the data strobe signal, allowing for precise timing adjustments. (EX1005, [0037-0041], Fig. 4).

ii. Moss

239. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.n.ii.

iii. Motivation to Combine

240. A person of ordinary skill in the art (POSITA) would find it obvious to combine Johnson and Moss for the reasons provided in Sec. IV.A.n.iii. Furthermore, a POSITA would find it obvious to combine Stubbs with the Johnson-Moss combination. Stubbs discloses receiving first and second data signals from a memory device at respective first and second pins, where the memory device contains multiple input/output pins, such as DQ0-DQ7, for receiving data signals in parallel. (EX1005, [0029]). These pins correspond directly to the first and second pins recited in the challenged claim. (EX1005, [0029]). In Stubbs' DDR SDRAM architecture, data is received on both rising and falling clock edges, with one pin receiving data on the rising edge and another on the falling edge, effectively doubling the data transfer rate. (EX1005, [0012], [0029]). The received data signals propagate from input buffers through adjustable delay elements before being captured by pass gates controlled by the data strobe signal, allowing for precise timing adjustments. (EX1005, [0037-0041], Fig. 4). Combining these features with the Johnson-Moss combination would yield predictable results in enhancing data reception efficiency, providing the known benefits of increased data bandwidth critical in high-performance memory controllers. (EX1006, at 5:51-55; EX1004, at [0004]).

o. 10[b]: “aligning the received first and second data signals with a strobe signal, the aligning comprising imparting a first delay to the first data signal, the first delay corresponding to a first delay value, imparting a second delay to the second data signal, the second delay corresponding to a second delay value.”

i. Stubbs

241. Stubbs discloses aligning received first and second data signals with a strobe signal by imparting delays corresponding to first and second delay values. Stubbs’ write data path circuit includes separate delay elements for rising and falling edge data. (EX1005, at [0047], Fig. 4). The circuit receives data signals from a DQ input pin through an input buffer 52, which connects to two adjustable delay elements 102 and 104. (EX1005, at [0047], Fig. 4). Delay element 102 imparts a first delay to the rising edge data path, while delay element 104 imparts a second delay to the falling edge data path, with both delays independently adjustable. (EX1005, at [0047-0048]). The delayed data signals are then aligned with a strobe signal QS/QS* controlling pass gates 56 and 58, which open on rising and falling edges respectively to pass the delayed data signals. (EX1005, at [0047], Fig. 4). This write data path circuitry is replicated for each DQ pin, allowing for multiple instances of first and second delays applied to separate data signals. (EX1005, at [0046-0047]).

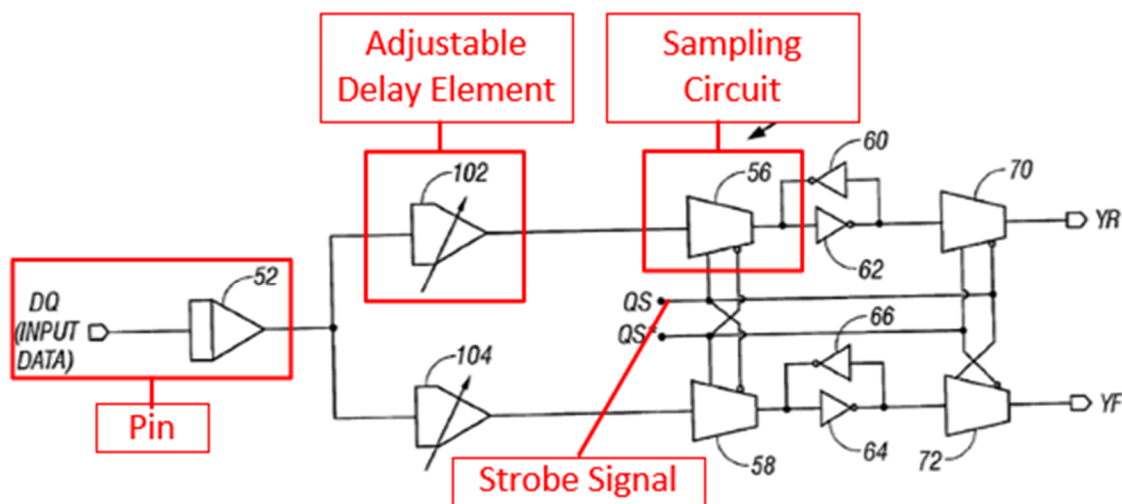


FIGURE 4

(EX1005, Fig. 4 (annotated)).

ii. Moss

242. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.o.ii.

iii. Motivation to Combine

243. A POSITA would have been motivated to combine Stubbs' adjustable delay elements with Moss's signal alignment techniques. Both references address timing control in high-speed memory interfaces. This combination would yield predictable results in enhancing signal alignment precision, providing the known benefits of improved timing margins critical in high-performance memory controllers.

p. 11: “The method according to claim 10, further comprising: in a calibration mode, determining the first and second delay values; and storing the first and second delay values.”

i. Stubbs

244. Stubbs discloses a calibration mode for determining and storing first and second delay values. During calibration, the memory device determines delay values for aligning rising and falling edge data signals with a data strobe signal. (EX1005, at [0018]). These values are stored for use during normal operation. (EX1005, at [0018-0019]). The calibration optimizes setup and hold times for rising and falling edge data independently by adjusting separate delay elements for each path. (EX1005, at [0015], [0047]). [Figure 4: Highlight delay elements 102 and 104] While not explicitly stated, a person of ordinary skill would have understood that this calibration process occurs for each DQ pin, as the write data path circuitry is replicated for each pin. (EX1005, at [0046-0047]). This allows per-pin optimization, addressing timing variations between data pins in high-speed memory devices. (EX1005, at [0015]). During normal operation, the stored delay values adjust the timing of incoming data signals, maintaining proper setup and hold times for both rising and falling edge data across all pins. (EX1005, at [0019], [0047-0048]).

ii. Moss

245. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.q.ii.

iii. Motivation to Combine

246. A POSITA would have been motivated to combine Stubbs' calibration process with Moss's explicit storage of delay values. Both references address timing control in high-speed memory interfaces. This combination would yield predictable results in enhancing system efficiency by allowing quick reconfiguration of delay values without repeated calibration, which is critical in high-performance memory controllers.

**q. 12: "The method according to claim 11, wherein:
during the receiving mode,
the imparting the first and second delays includes retrieving the
stored first and second delay values."**

i. Stubbs

247. Stubbs discloses retrieving stored first and second delay values during a receiving mode to impart first and second delays. Stubbs' write data path circuit includes separate adjustable delay elements 102 and 104 for delaying rising and falling edge data, respectively. (EX1005, at [0047], Fig. 4). Delay values for these elements are determined during calibration and stored for later use. (EX1005, at [0018]). During normal operation (receiving mode), these stored values are retrieved and applied to delay elements 102 and 104, maintaining optimized setup and hold times for rising and falling edge data. (EX1005, at [0018], [0047]).

248. The write data path circuit is replicated for each DQ pin, allowing per-pin optimization to compensate for variations between pins. (EX1005, at [0015],

[0047]). By retrieving and applying stored delay values during receiving mode, Stubbs ensures proper alignment of data with the strobe signal for both rising and falling edge data on each pin, improving reliability of data capture in the DDR memory device. (EX1005, at [0047-0048]).

ii. Moss

249. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.r.ii.

iii. Motivation to Combine

250. A POSITA would have been motivated to combine Stubbs' use of stored delay values with Moss's explicit retrieval process. Both references address timing control in high-speed memory interfaces. This combination would yield predictable results in enhancing system efficiency by allowing quick reconfiguration of delay values without repeated calibration, which is critical in high-performance memory controllers.

**r. 13: "The method according to claim 12, wherein:
the first and second data signals are delayed by the first and
second delay values."**

i. Stubbs

251. Stubbs discloses delaying first and second data signals by first and second delay values. The write data path circuit in Stubbs includes separate adjustable delay elements 102 and 104 for delaying data signals on each input/output (DQ) pin. (EX1005, at [0046-0047], Fig. 4). These delay elements introduce adjustable delays

into the propagation of data signals applied to their inputs, allowing for independent optimization of timing for different data signals. (EX1005, at [0047-0048]). By providing separate delays for different data paths, Stubbs enables different delay times for data signals arriving at pass gates 56 and 58. (EX1005, at [0047]). The delay elements are adjusted to achieve predetermined timed relationships between the delayed data signals and the data strobe signals, optimizing setup and hold times. (EX1005, at [0048]).

ii. Moss

252. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.s.ii.

iii. Motivation to Combine

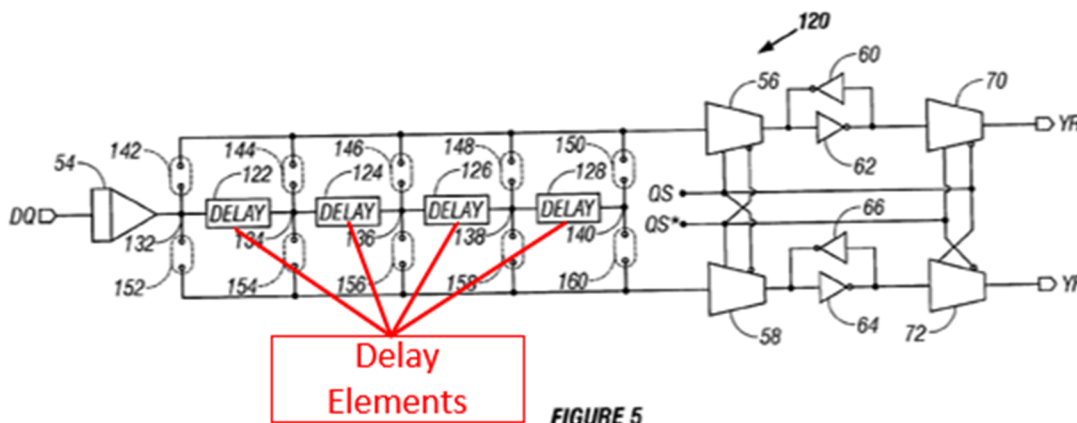
253. A POSITA would have been motivated to combine Stubbs' adjustable delay elements with Moss's delay implementation. Both references address timing control in high-speed memory interfaces. This combination would yield predictable results in enhancing delay precision and adaptability, providing the known benefits of fine-grained delay adjustment critical in high-performance memory controllers.

**s. 14: “The method according to claim 11, further comprising:
during the calibration mode,
calibrating a timing signal delay value corresponding to a delay
for application to the strobe signal.”**

i. Stubbs

254. Stubbs discloses calibrating timing signal delay values during a calibration mode, but does not explicitly state that this includes a delay value for the strobe

signal. Stubbs teaches determining and storing delay values for data signals relative to a data strobe signal to achieve proper setup and hold times. (EX1005, at [0018-0019]). While Stubbs primarily focuses on delaying data signals, it also discloses using adjustable delay elements for both data and strobe signals to achieve proper timing. (EX1005, at [0007], [0010]). A POSITA would have found it obvious to apply the same calibration technique to the strobe signal, as this would provide finer control over the relative timing between data and strobe, allowing for more precise optimization of setup and hold times across different operating conditions. Stubbs' disclosure of a calibration strobe delay element. (EX1005, at [0010]) implies that its delay value would need to be calibrated during a calibration mode, similar to the data signal delays. The delay network shown in Figure 5 could readily be applied to delay the strobe signal, with the optimal tap point determined and stored during calibration. (EX1005, at Fig. 5, [0050-0053]).



(EX1005, at Fig. 5)

ii. Moss

255. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.t.ii.

iii. Motivation to Combine

256. A POSITA would have been motivated to combine Stubbs' calibration techniques with Moss's explicit calibration of strobe signal delay. Both references address timing control in high-speed memory interfaces. This combination would yield predictable results in enhancing timing precision, providing the known benefits of adaptive timing control critical in high-speed memory interfaces.

**t. 15: “The method according to claim 14, further comprising:
during the calibration mode,
storing the calibrated timing delay value.”**

i. Stubbs

257. Stubbs discloses storing calibrated delay values during a calibration mode, which directly addresses the limitation of claim 15. Stubbs teaches that delay values determined during calibration are stored for later use during normal operation of the memory device. (EX1005, at [0018], [0019]). While Stubbs primarily focuses on storing delay values for data signals, the same principle would apply to storing a calibrated timing delay value for the strobe signal. This storage allows optimized delay settings to be maintained and quickly applied without needing to recalibrate each time the device is used. (EX1005, at [0018], [0019]). Storing calibrated delay values also enables adaptive behavior in the memory system, allowing for

adjustments as operating conditions change to ensure continued optimal performance. (EX1005, at [0009]).

ii. Moss

258. Even if Stubbs did not disclose this feature, Moss does. *See supra*, § IX.A.u.ii.

iii. Motivation to Combine

259. A POSITA would have been motivated to combine Stubbs' calibration techniques with Moss's explicit storage of calibrated delay values. Both references address timing control in high-speed memory interfaces. This combination would yield predictable results in enhancing system efficiency by allowing quick reconfiguration of delay values without repeated calibration, which is critical in high-performance memory controllers.

D. Ground 4: Stubbs, in view of Moss, in further view of Liou

a. 8: "The IC memory controller according to claim 1, further comprising a calibration strobe delay element to impart a calibrated delay to the strobe signal."

i. Stubbs

260. Stubbs discloses a synchronous double-data-rate semiconductor memory device with write path circuitry that includes delay elements for adjusting the timing of data and strobe signals. (EX1005, at Abstract, [0007-0010]). While Stubbs does not explicitly disclose a calibration strobe delay element to impart a calibrated delay to the strobe signal, this feature would have been obvious to a POSITA based on Stubbs' teachings. Stubbs describes adjusting the timing of both data signals and

strobe signals to achieve proper alignment for sampling data. (EX1005, at [0007], [0018]). The write path circuitry shown in Figure 4 could be readily modified to include a calibration strobe delay element in the path of the DQS strobe signal before it reaches the pass gates 56 and 58, allowing for fine-tuning of the strobe signal timing relative to the delayed data signals. (EX1005, at Fig. 4, [0047]).

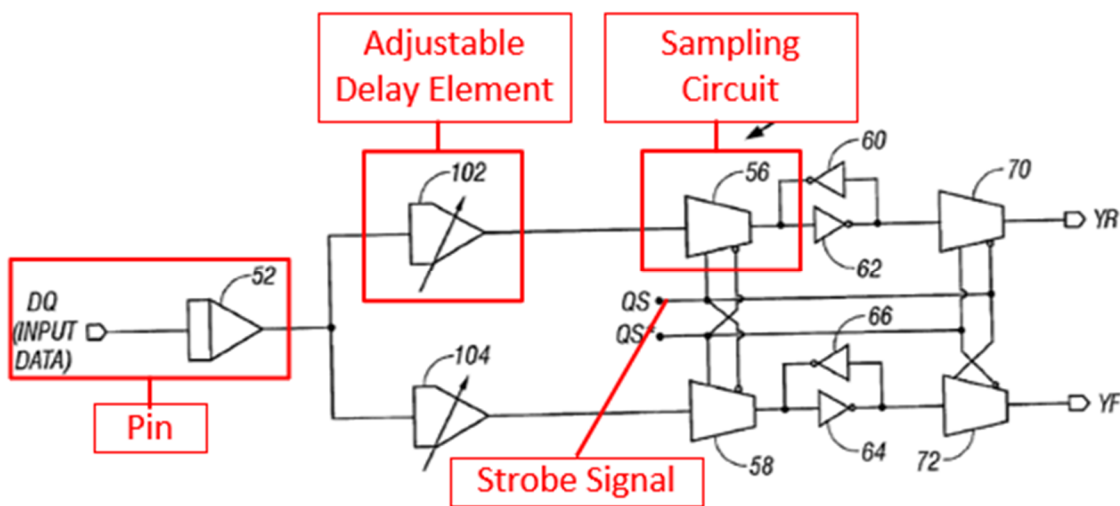


FIGURE 4

(EX1005, Fig. 4 (annotated)). This modification aligns with Stubbs' teaching of providing flexible timing adjustment capabilities in the write path circuitry and represents a straightforward extension of the principles already disclosed for achieving optimal signal timing in a double-data-rate memory device. (EX1005, at [0007], [0015]). The calibration strobe delay element could be adjusted during the calibration mode described by Stubbs to determine an optimal delay value for the

strobe signal, which would then be applied during normal operation to ensure proper data sampling. (EX1005, at [0018], [0019]).

ii. Liou

261. Even if Stubbs did not disclose this feature, Liou does. *See supra*, § IX.B.a.ii.

iii. Motivation to Combine

262. A POSITA would have been motivated to incorporate Liou's explicit calibration strobe delay element into Stubbs' memory device. Both references address timing control in high-speed memory interfaces. This combination would yield predictable results in enhancing timing precision, providing the known benefits of adaptive timing control critical in high-speed memory interfaces.

E. Ground 5: Stubbs, in view of Moss, in further view of Johnson

a. Limitation 10[pre]

i. Stubbs

263. Stubbs discloses this limitation. *See supra*, § IX.C.o.i

ii. Moss

264. Even if Stubbs did not disclose this limitation, Moss does. *See supra*, § IX.A.o.ii.

iii. Johnson

265. Even if the combination of Stubbs and Moss did not disclose this limitation, Johnson does. *See supra*, § IX.A.m.i.

iv. Motivation to Combine

266. A person of ordinary skill in the art would have found it obvious to combine the teachings of Johnson, Stubbs, and Moss to arrive at a method of operation in an IC memory controller as claimed. Johnson discloses a memory controller that executes specific procedures to manage data flow and timing in a memory system, including initialization, calibration, and ongoing data transfer operations. (EX1004, at 3:34-41, 4:28-43). Stubbs teaches a write data path circuit within a memory controller that aligns received data signals with a strobe signal by applying independently adjustable delays. (EX1005, at [0047-0048], Fig. 4). Moss explicitly describes a method implemented within a memory controller circuit to realign read data returned from memory components, compensating for phase shifts due to propagation delays and other factors. (EX1006, at Abstract, 5:51-55, 6:36-7:46). A POSITA would have been motivated to incorporate the specific alignment techniques of Stubbs and Moss into Johnson's memory controller operations to improve data timing accuracy and system performance across various operating conditions. (EX1004, at 2:47-53; EX1005, at [0016]; EX1006, at 1:43-54). [Figure 4 of Stubbs: Highlight delay elements 102 and 104, pass gates 56 and 58, and strobe signal QS/QS*] [Figure 3 of Moss: Highlight delay line 306, flip-flops 312 and 320, and clock signal CLK 302]

b. Limitation 10[a]

i. Stubbs

267. Stubbs discloses this limitation. *See supra*, § IX.C.n.i

ii. Moss

268. Even if Stubbs did not disclose this limitation, Moss does. *See supra*, § IX.A.n.ii.

iii. Johnson

269. Even if the combination of Stubbs and Moss did not disclose this limitation, Johnson does. *See supra*, § IX.A.n.i.

iv. Motivation to Combine

270. A POSITA would have been motivated to combine Johnson and Moss to arrive at this limitation. *See supra*, § IX.A.n.iii. A POSITA would also be motivated to combine Stubbs and Moss to arrive at this limitation. *See supra*, § IX.C.n.iii. A POSITA would have been further motivated to combine Stubbs, Moss, and Johnson to arrive at the claimed limitation for substantially the same reasons as discussed with respect to those combinations.

c. Limitation 10[b]

i. Stubbs

271. Stubbs discloses this limitation. *See supra*, § IX.C.o.i

ii. Moss

272. Even if Stubbs did not disclose this limitation, Moss does. *See supra*, § IX.A.o.ii.

iii. Johnson

273. Even if the combination of Stubbs and Moss did not disclose this limitation, Johnson does. *See supra*, § IX.A.o.i.

iv. Motivation to Combine

274. A POSITA would have been motivated to combine Johnson and Moss to arrive at this limitation. *See supra*, § IX.A.o.iii. A POSITA would also be motivated to combine Stubbs and Moss to arrive at this limitation. *See supra*, § IX.C.o.iii. A POSITA would have been further motivated to combine Stubbs, Moss, and Johnson to arrive at the claimed limitation for substantially the same reasons as discussed with respect to those combinations.

d. Limitation 10[c]

i. Stubbs

275. Stubbs discloses this limitation. *See supra*, § IX.C.p.i

ii. Moss

276. Even if Stubbs did not disclose this limitation, Moss does. *See supra*, § IX.A.p.ii.

iii. Johnson

277. Even if the combination of Stubbs and Moss did not disclose this limitation, Johnson does. *See supra*, § IX.A.p.i.

iv. Motivation to Combine

278. A POSITA would have been motivated to combine Johnson and Moss to arrive at this limitation. *See supra*, § IX.A.p.iii. A POSITA would also be motivated to combine Stubbs and Moss to arrive at this limitation. *See supra*, § IX.C.p.iii. A POSITA would have been further motivated to combine Stubbs, Moss, and Johnson to arrive at the claimed limitation for substantially the same reasons as discussed with respect to those combinations.

e. Claim 11

i. Stubbs

279. Stubbs discloses this limitation. *See supra*, § IX.C.q.i

ii. Moss

280. Even if Stubbs did not disclose this limitation, Moss does. *See supra*, § IX.A.q.ii.

iii. Johnson

281. Even if the combination of Stubbs and Moss did not disclose this limitation, Johnson does. *See supra*, § IX.A.q.i.

iv. Motivation to Combine

282. A POSITA would have been motivated to combine Johnson and Moss to arrive at this limitation. *See supra*, § IX.A.q.iii. A POSITA would also be motivated to combine Stubbs and Moss to arrive at this limitation. *See supra*, § IX.C.q.iii. A POSITA would have been further motivated to combine Stubbs, Moss, and Johnson to arrive at the claimed limitation for substantially the same reasons as discussed with respect to those combinations.

f. **Claim 12**

i. Stubbs

283. Stubbs discloses this limitation. *See supra*, § IX.C.r.i

ii. Moss

284. Even if Stubbs did not disclose this limitation, Moss does. *See supra*, § IX.A.r.ii.

iii. Johnson

285. Even if the combination of Stubbs and Moss did not disclose this limitation, Johnson does. *See supra*, § IX.A.r.i.

iv. Motivation to Combine

286. A POSITA would have been motivated to combine Johnson and Moss to arrive at this limitation. *See supra*, § IX.A.r.iii. A POSITA would also be motivated to combine Stubbs and Moss to arrive at this limitation. *See supra*, § IX.C.r.iii. A

POSITA would have been further motivated to combine Stubbs, Moss, and Johnson to arrive at the claimed limitation for substantially the same reasons as discussed with respect to those combinations.

X. Conclusion

For the foregoing reasons, I conclude that each of Claims 1-2, 3-15 are invalid as obvious over the references discussed above.