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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SILICON MOTION INC.,
Petitioner

v.

K.MIZRA LLC,
Patent Owner

Case IPR2024-01241

U.S. Patent No. 9,111,608

PATENT OWNER'S PRELIMINARY RESPONSE

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I. INTRODUCTION

Pursuant to 35 U.S.C. § 313 and 37 C.F.R. § 42.107, K.Mizra LLC (“Patent Owner”) submits this Preliminary Response to Silicon Motion, Inc.’s (“Petitioner”) Petition for *Inter Partes* Review (“Petition,” Paper 1), challenging Claims 1-2, 4-15 of U.S. Patent 9,111,608 (the “’608 Patent”) (Ex. 1001).

The ’608 Patent claim systems and methods for calibrating a controller for high-speed memory on a per-pin basis to improve the controller’s ability to read data out of the memory. Petitioner asserts the challenged claims are obvious by cobbling together references describing high-speed memory with a generic controller that does not calibrate on a per-pin basis. Petitioner takes a scattershot approach alleging that every limitation is disclosed by every reference, and in some cases mischaracterizing what is disclosed. Petitioner also fails to articulate sufficient reasons that one of ordinary skill would seek to combine the references as alleged to achieve the inventions of the ’608 Patent.

For at least these reasons detailed below, Petitioner cannot show that any of the challenged claims are reasonably likely to be found unpatentable, and the Board should not institute *inter partes* review.

II. THE '608 PATENT AND THE CHALLENGED CLAIMS

A. Overview of the '608 Patent

The '608 Patent is directed to memory controllers as Petitioner acknowledges. *See* Ex. 1001 at 3:16-34; *see also* Petition at 6. The '608 Patent explains that “[t]he transfer of information and signals required among the components of [high-speed processor-based electronic systems] has led to increasing demands for interfaces to support the efficient high-speed transfer of information.” Ex. 1001 at 1:34-40. “Examples of such interfaces include the interfaces between processors and memory devices of high-speed systems,” i.e. memory controllers. *Id.* at 1:38-40.

The '608 Patent addresses “issues [that] arise regarding the timing of [] data transfer, particularly where a memory controller receives data sent by a double data rate DRAM attached thereto using a strobe-based method.” *Id.* at 1:48-52. A “strobe-based method” is one in which “a strobe signal (also referred to as the DQS signal) is edge-aligned to and accompanies a data signal (also referred to as the DQ signal) sent by the DRAM.” *Id.* at 1:53-55. The strobe or “DQS is used by the controller to capture the data signal sent by the DRAM.” *Id.* at 1:55-57. In prior art systems, “the DQS signal is delayed by some fixed amount” and “then used as a common sample clock for each of the DQ input receivers” at the controller. *Id.* at 1: 58-62. As the '608 Patent explains, this use of a single delay for each of the DQ input receivers (“typically a byte or 8 bits sent in parallel”) cannot provide the “the ideal amount of

strobe-delay for every pin.” *Id.* at 1:62-66. Accordingly, the ’608 Patent identifies “a need in high-speed, strobe-based memory systems, for *per-pin (data bit) strobe-offset* control and timing calibration to minimize DQS-to-DQ timing offsets for each DQ pin individually, yielding more robust, higher-speed systems.” *Id.* at 2:21-25 (emphasis added).

The ’608 Patent addresses this need for per-pin calibration in a strobe-based system by teaching “systems/methods [that] generate the optimal per-bit strobe signals by automatically calibrating per-bit offset timing between data signals DQ<X> of individual data lines (where DQ<X> represents any one of a number of data lines DQ<N:0>, where X is any of data lines 0, 1, 2 . . . N) and corresponding strobe signals DQS.” *Id.* at 3:23-29. “The strobe-offset control system generally includes a calibration control circuit coupled to a variable delay element, both of which couple to a receiver.” *Id.* at 3:37-39. Figure 1 demonstrates an embodiment:

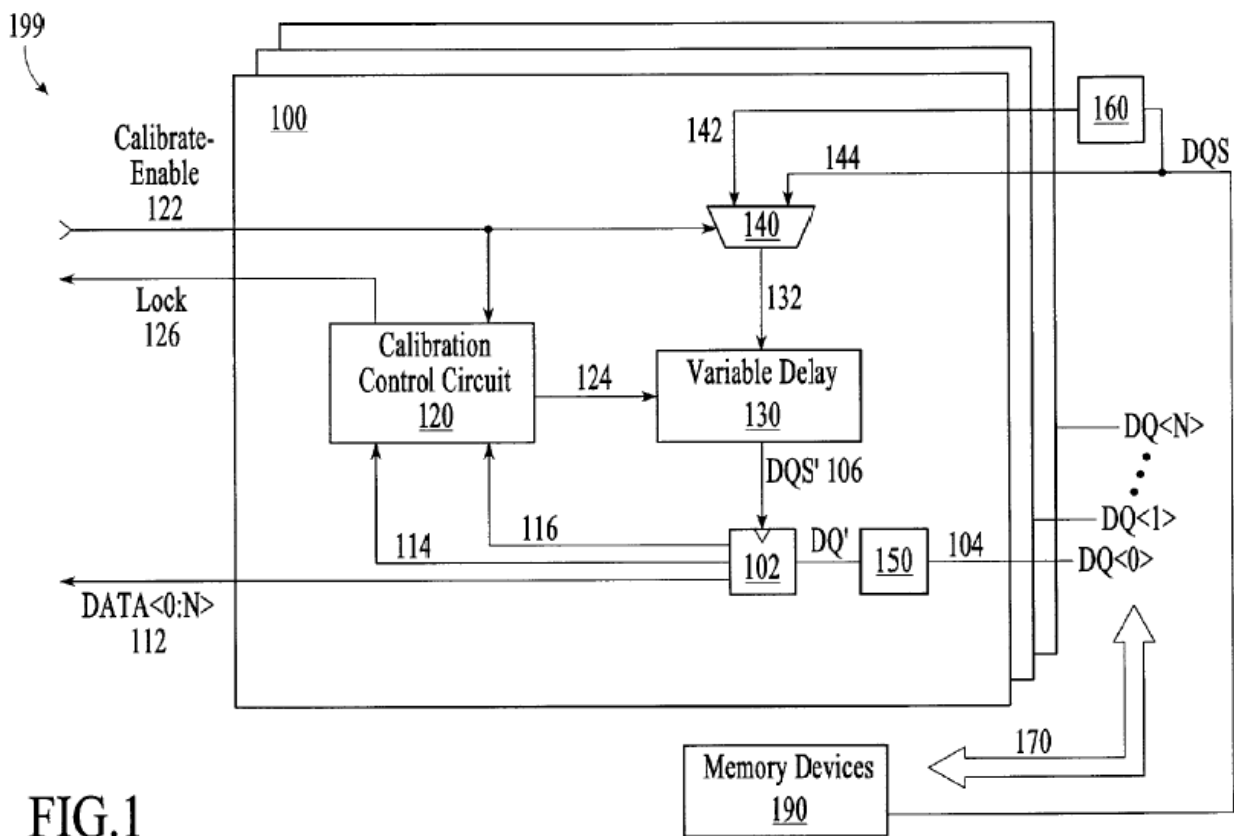


FIG.1

Ex. 1001, Fig. 1

The '608 Patent teaches “a strobe-offset control system **100** for individual data line strobe-offset control,” i.e. for each data line DQ<0> through DQ<N>. *Id.* at 4:15-33. The “strobe-offset control system **100** [] includes a calibration control circuit **120**” “under control of a memory controller or other device . . . [which] operates in a calibration mode to adjust an amount of the delay or offset applied by the variable delay element **130** to versions of the strobe signal.” *Id.* at 4:55-62. During calibration, “[t]he receiver/phase detector **102** compares the phase relationship between the strobe signal DQS’ and the delayed data signals DQ<X>’

for each received data bit, and provides those comparison results to the calibration control circuit **120**.” *Id.* at 5:40-49. The calibration control circuit **120** will adjust the delay provided by one or both of the variable delay elements **130** and/or **150** in order to approximately edge-align the data and strobe signals. *Id.* at 5:45-61.

The ’608 Patent claims an IC memory controller and method for operating an IC memory controller in accordance with these teachings that align data and strobe signals received from a memory for each bit of an N-bit wide data path. The challenged claims are further detailed in the next section.

B. Challenged Claims

The Petition challenges claims 1-2, 4-15 of the ’608 Patent. Claims 1 and 10 are independent claims. Claims 2, and 4-9 depend from claim 1, and claims 11-15 depend from claim 10. The Petition provides a listing of all the challenged claims at pages viii-ix.

The independent claims are reproduced below:

Claim 1 recites:

1. An integrated circuit (IC) memory controller comprising:
 - a first pin to receive a first data signal;
 - a first adjustable delay element to delay the received first data signal and generate a first delayed data signal;
 - a second pin to receive a second data signal;

a second adjustable delay element to delay the received second data signal and generate a second delayed data signal;
a pin to receive a strobe signal;
a first sampling circuit to sample the first delayed data signal based on the strobe signal; and
a second sampling circuit to sample the second delayed data signal based on the received strobe signal.

Consistent with the teachings of the '608 Patent discussed in the preceding section, independent claim 1 requires a memory controller that has at least two pins that each receive a data signal, adjustable delays for each data signal, a pin to receive a strobe signal, and sampling circuits to sample the delayed data signals based on the strobe signal. The other independent claim 10 requires a method of operating such a memory controller.

Claim 10 recites:

10. A method of operation in an IC memory controller, the method comprising:
receiving first and second data signals from a memory device at respective first and second pins;
aligning the received first and second data signals with a strobe signal, the aligning comprising
imparting a first delay to the first data signal, the first delay corresponding to a first delay value,
imparting a second delay to the second data signal, the second delay corresponding to a second delay value.

III. LEVEL OF ORDINARY SKILL

For the limited purpose of this Preliminary Response, Patent Owner does not contest Petitioner's definition of a person of ordinary skill in the art, but it reserves the right to do so in the event that trial is instituted.

IV. CLAIM CONSTRUCTION

Patent Owner submits that the Board need not construe any claim term in a particular manner to arrive at the conclusion that the Petition is substantively deficient. *See Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“need only be construed ‘to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))). Patent Owner expressly reserves the right to address any and all claim constructions in the Petition whether explicit or implicit if trial were to be instituted or in any other or subsequent proceedings.

V. APPLICABLE LEGAL STANDARDS

The Board may only grant a petition for *inter partes* review where “the information presented in the petition ... shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); 37 C.F.R. § 42.108(c). Petitioner bears the burden of showing that this statutory threshold has been met. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756 (Aug. 14, 2012) (“The Board ... may institute

a trial where the petitioner establishes that the standards for instituting the requested trial are met”).

A. Obviousness

Section 103 of the Patent Act provides that “[a] patent may not be obtained . . . if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a). The obviousness analysis requires several threshold inquiries: the level of ordinary skill in the art must be established; the scope and content of the prior art must be determined; and any differences between the prior art and the claims at issue must be ascertained. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

1. Claims cannot be found obvious if an element is absent.

If a single element of the claim is absent from the prior art, the claim cannot be considered obvious. *See CFMT, Inc. v. YieldUp Int’l Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003) (“Obviousness requires a suggestion of all limitations in a claim.”) (citing *In re Royka*, 490 F.2d 981, 985 (C.C.P.A. 1974)); *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversing obviousness rejection where prior art did not teach or suggest all claim limitations); *Garmin Int’l, Inc. v. Patent of Cuozzo Speed Techs. LLC*, IPR2012-00001, Paper 15 at 15 (PTAB Jan. 9, 2013) (refusing to

institute an *inter partes* review under 35 U.S.C. § 103 where prior art did not disclose all claim limitations).

Additionally, it is improper to use the challenged claim as a roadmap to piece together disparate disclosure using hindsight bias. *See InTouch Techs., Inc. v. VGo Comm'ns., Inc.*, 751 F.3d 1327, 1351 (Fed. Cir. 2014) (reversing obviousness where “[i]t appears that [the expert] relied on the [] patent itself as her roadmap for putting what she referred to as pieces of a ‘jigsaw puzzle’ together.”); *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007) (“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning.”).

2. A petition must address the Graham factors.

Obviousness is resolved on a number of factual determinations “including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of ordinary skill in the art.” *See Graham*, 383 U.S. at 17-18. Petitions for *inter partes* reviews “must address the Graham factors.” *Eizo Corp. v. Barco N.V.*, IPR2014-00358, Paper 11 at 29-30 (PTAB July 23, 2014).

3. A petition must provide articulated reasoning with rational underpinning to combine and/or modify references.

The conclusion of obviousness based on a combination of references must also be supported with explicit analysis of a reason to combine those references. *KSR*

Int'l Co. v. Teleflex Inc., 550 U.S. 398, 418 (2007). The Federal Circuit has stated that such reasons must be more than “mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006); *accord Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 (Fed. Cir. 2008) (agreeing with the district court’s reasoning that “some kind of motivation must be shown from some source, so that the jury can understand why a person of ordinary skill would have thought of either combining two or more references or modifying one to achieve the patented method”); *see also LG Elecs., Inc. v. Cellular Commc’ns Equip. LLC*, IPR2016-00197, Paper 7 at 7-11 (PTAB April 29, 2016) (faulting a petition’s obviousness analysis for lack of sufficient articulated reasons with rational underpinnings for modifying references to achieve particular elements required in the claims).

Furthermore, “[d]emonstrating that a reference is analogous art or relevant to the field of endeavor of the challenged patent is not sufficient to establish that one of ordinary skill would have had reason to combine its teachings with other prior art in the manner set forth in the claim.” *Johns Manville Corp. v. Knauf Insulation, Inc.*, IPR2018-00827, Paper 9 at 10 (PTAB Oct. 16, 2018) (citing *See Securus Techs., Inc. v. Global Tel*Link Corp.*, 701 F. App’x 971, 977 (Fed. Cir. 2017) (“a broad characterization of [prior art references] as both falling within the same alleged field

. . . without more, is not enough for [Petitioner] to meet its burden of presenting a sufficient rationale to support an obviousness conclusion”). “Mere compatibility of the references is likewise not sufficient.” *Id.* (citing *Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993 (Fed. Cir. 2017) (it is not enough to show that “a skilled artisan, once presented with the two references, would have understood that they could be combined”).

VI. SUMMARY OF THE PRIOR ART REFERENCES

Petitioner relies on the Johnson, Moss, and Stubs references in the proposed grounds addressed to the independent claims. Because the Liou reference is only included in grounds addressed to dependent claims (Grounds 2 and 5), Patent Owner reserves the right to address its disclosure and any related arguments if *inter partes* review is instituted. A brief summary of the Johnson, Moss and Stubs references follows.

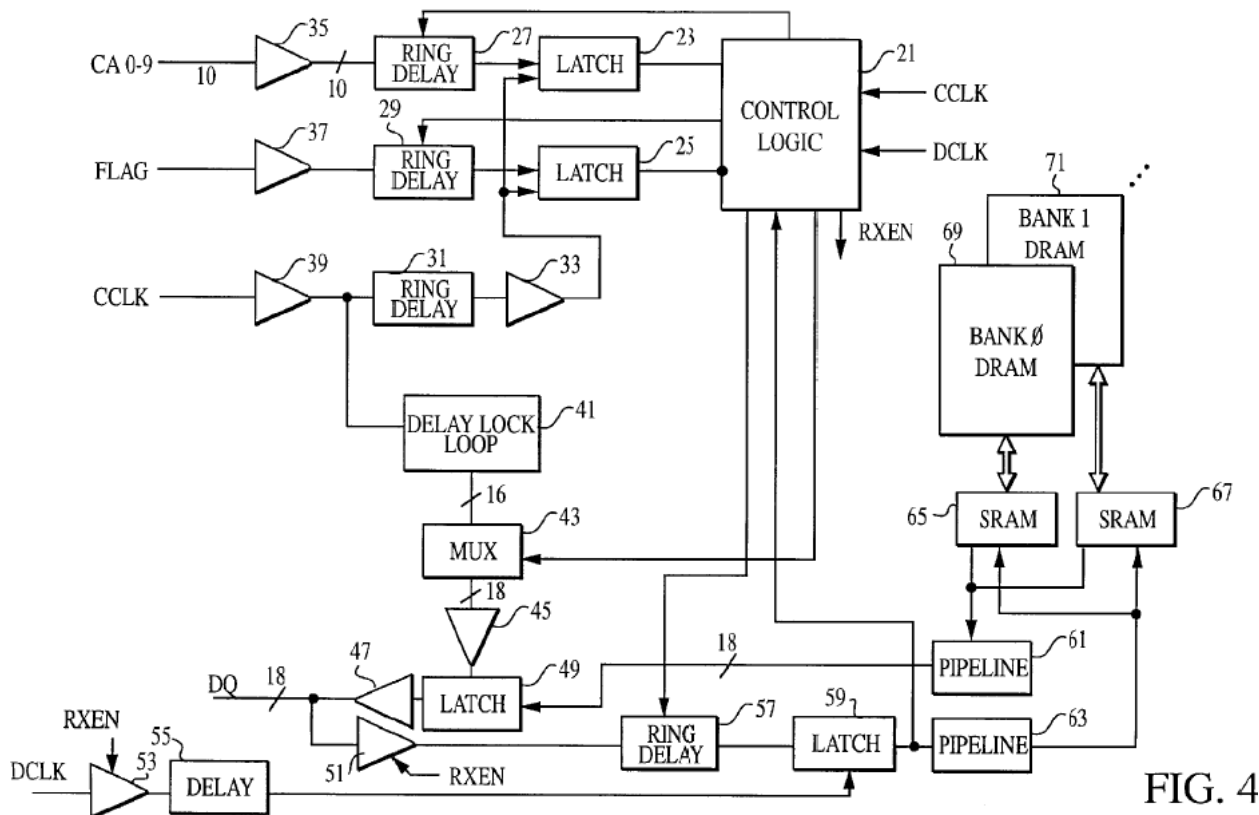
A. Overview of Johnson

Petitioner relies on U.S. Patent No. 6,434,081 to Johnson et al. as a reference in each of Grounds 1, 2, and 5. *See, e.g.*, Petition at 10-11. Johnson discloses “an improved binary calibration technique which is useful for calibrating the timing of control and data signals in memory devices, for example, SLDRAM memory devices.” Ex. 1004 at 1:5-8; *cf.* Petition at 12. That is, the Johnson patent titled “Calibration Technique for Memory Devices,” relates to and discloses calibration

techniques for memories—not for memory controllers. In fact, the only discussions of a memory controller in Johnson describe a memory controller providing signals and data to the memory device. *See, e.g.*, Ex. 1004 at 3:33-40; 4:11-22. There is no discussion of the inner workings of the memory controller.

Instead, Johnson focuses on problems associated with calibrating a memory device, such as an SLDRAM (SyncLink dynamic random access memory). *Id.* at 1:13-20; 1:42-2:2. Johnson explains that prior art memory calibration methods required the controller to transmit a known sequence of data to the memory to allow the memory to calibrate the appropriate delay. *Id.* Johnson explains, however, that when “this calibration procedure is independently carried out for each incoming data path” it “may take some time and [] also may, in extreme cases, cause the data ‘eye’ on different incoming data paths to be aligned on different edges of the clock signal.” *Id.* at 2:9-14. In summary, Johnson describes the problem it seeks to address as “even though serial calibration of each data line relative to the clock CCLK has been achieved, there is still a possibility for misalignment in a parallel direction across all of the data paths.” *Id.* at 2:37-41.

Johnson’s solution to the identified problem is provided through the circuitry of the SLDRAM memory module shown in Figure 4:



Ex. 1004, Fig. 4

Johnson’s solution is to transmit a known synchronizing pattern to the memory and provide control logic **21** that samples and stores “patterns representing which delay values for the ring delays **27** and **29** provide for a correct sampling and recognition of the” synchronizing pattern. *Id.* at 4:31-48. Johnson discloses that this “calibration process may be carried out on any *one* of the data paths of the command bus CA0-9 and any *one* of the receive data paths of the data bus DQ (although for the latter the DCLK signal is used for clocking).” *Id.* at 4:55-59 (emphasis added).

Johnson acknowledges that “[a]lthough the same calibration procedure may also be applied to each of the CMD data paths CA0-9 and to each of the data paths

of the DQ bus . . . this will not ensure parallel alignment of the data across all of the incoming data paths,” i.e. the problem that Johnson seeks to address. *Id.* at 6:7-14. Instead, Johnson discloses that “[a]fter one of the incoming data paths, e.g., FLAG, is serially aligned in the manner described above with reference to FIGS. 1-7, the control logic circuit **21** then compares the newly aligned calibration pattern on the aligned data path, e.g., FLAG, with the calibration pattern from another data line, e.g., CA<0>, which is to be aligned.” *Id.* at 6:55-60. Alternatively, Johnson discloses that, rather than calibrating all the remaining paths to the initial one, the next data path can be calibrated to the “just calibrated data path.” *Id.* at 7:25-29.

Thus, unlike the '608 Patent, Johnson discloses techniques for calibrating a memory device, not a memory controller. That is, while the '608 Patent is about receiving read data into a memory controller, Johnson is about receiving write data into a DRAM. Moreover, as discussed above in Section II.A, the '608 Patent sought to provide per-pin (data bit) strobe-offset control and timing calibration for high-speed, *strobe-based* memory systems. Ex. 1001 at 1:62-66. Johnson instead seeks to provide a timing-calibrated system based on a known pattern—an approach that the '608 Patent sought to avoid in favor of a strobe-based solution. *See* Ex. 1001 at 2:4-25. And finally, rather than disclosing a per-bit calibration scheme relative to a strobe as in the '608 Patent, Johnson seeks to provide alignment “in a parallel direction

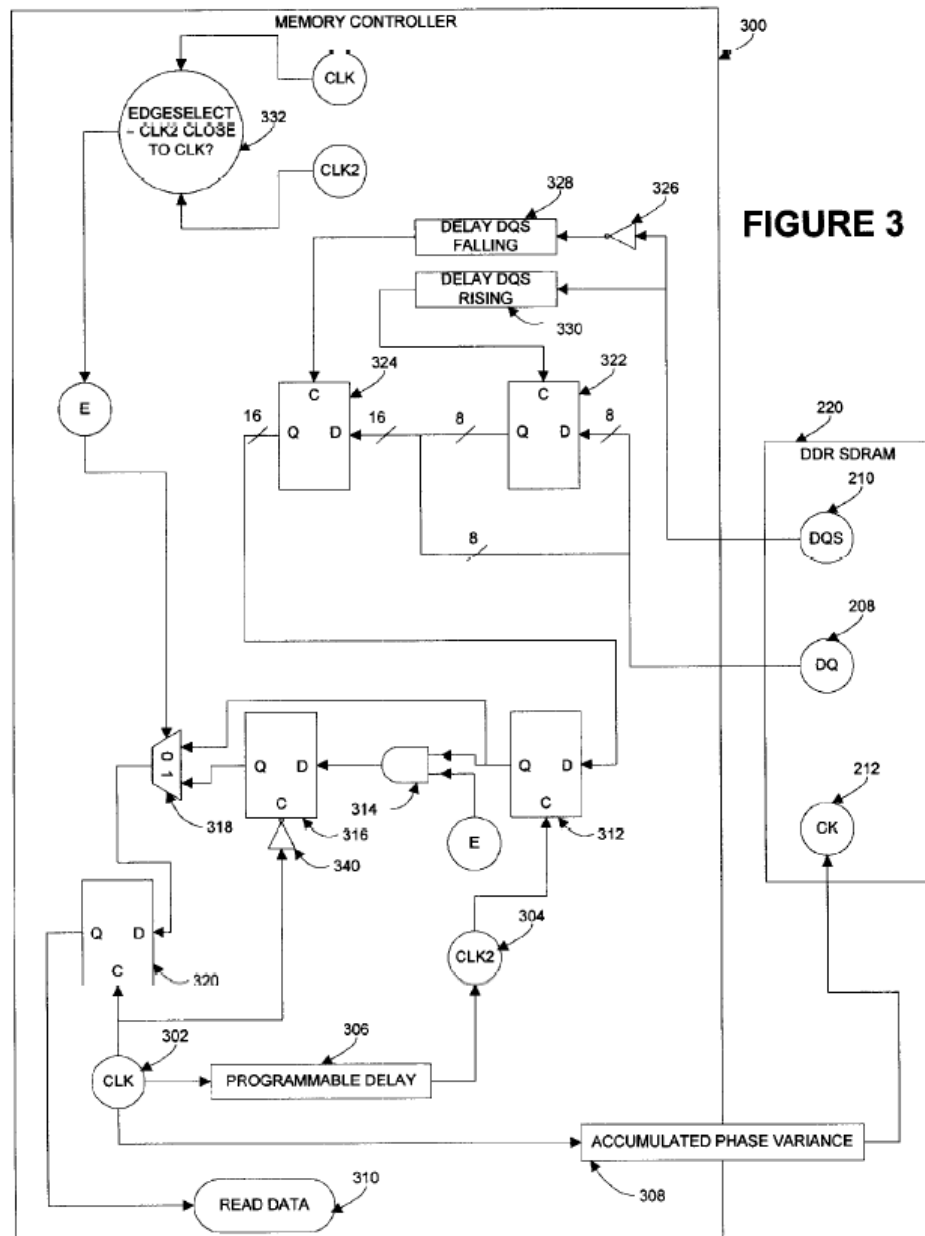
across all of the data paths” rather than serial calibration relative to the clock. Ex. 1004 at 2:37-41; *see also* 6:7-14; 6:55-60; 7:25-29.

B. Overview of Moss

Petitioner relies on U.S. Patent No. 6,646,929 to Moss et al. as a reference in all Grounds 1-5. *See, e.g.*, Petition at 10-11. Moss was identified during prosecution of the '608 Patent and is listed on its cover. Ex. 1001 at p.2.

Moss “relates to methods and associated structure for synchronizing the process of reading data between high-performance memory components and the associated memory controller device.” Ex. 1006 at 1:10-14. Moss identifies the problem it seeks to address as “a need [] for an improved method and structure for synchronization of clocks and strobes in the return of read data from a high-performance memory subsystem.” *Id.* at 2:39-42.

To address this problem, Moss discloses methods and structures where “returned read data is captured (registered) using a delayed version of the memory controller’s clock signal that is delayed to re-align with the strobe signal generated by the memory component.” *Id.* at 2:51-54. Moss discloses a block diagram of its disclosed structure in Figure 3:



Ex. 1006, Fig. 3.

Moss discloses that “[d]ata received at the memory controller is first registered in the data strobe (DQS **210**) clocking domain and then reregistered in the domain of CLK **302** delayed appropriately to compensate for measured or calculated

phase offset.” *Id.* at 5:63-67. “More specifically, the registered data from the DQS domain is registered in the CLK2 domain—a clock derived from CLK through a *predetermined* delay element.” *Id.* at 5:67-6:3 (emphasis added). “Delayed clock signal CLK2 304 is delayed a sufficient amount to compensate for phase offset errors between clock 302 and data strobe DQS 210.” *Id.* at 6:58-61.

As Moss explains in summary, “[t]he delay is programmed in accordance with a predetermined delay determined from the circuit design.” *Id.* at 2:54-56. Moss discloses nothing about how to determine such delay value “[r]ather . . . [Moss] relates to use of such a predetermined delay value to adapt and re-align the registering of the returned read data.” *Id.* at 2:59-63.

Moss does not disclose anything about calibrating on a per-pin or per-bit basis as in the ’608 Patent. Moreover, it does not disclose any circuitry or mechanism for determining the appropriate delay value. And finally, despite Petitioner’s assertions that Moss discloses “*programmable* delay lines (306, 328, 330)” (Petition at 9 (emphasis added)), there is no indication in Moss that delay lines 328 or 330 are programmable. In fact, Moss clearly refers to delay line 306 as “programmable” but does not for either delay line 328 or 330. *See, e.g., id.* at 6:54; Fig. 3.

C. Overview of Stubbs

Petitioner relies on U.S. Patent Appl’n Publ’n No. 2003/0099135 to Stubbs as a reference in each of Grounds 3-5. *See, e.g.,* Petition at 11. Stubbs, like Johnson, is

about memory not memory controllers. It is titled “Per-Bit Set-Up and Hold Time Adjustment for Double-Data Rate Synchronous DRAM.” Ex. 1005 at 1. The word “controller” does not appear anywhere in the specification, and at most it discloses signals coming into a DRAM, but certainly nothing about the structure or operation of a controller.

It is difficult then to reconcile the Stubbs reference with Petitioner’s statement: “Stubbs (EX1005) discloses a memory controller for a DDR DRAM device.” Petition at 15. Petitioner relies on two figures from Stubbs. The first is Figure 2, which Stubbs describes as “a schematic/block diagram of a portion of write data path circuitry in a prior art memory device.” Ex. 1005 at [0022].

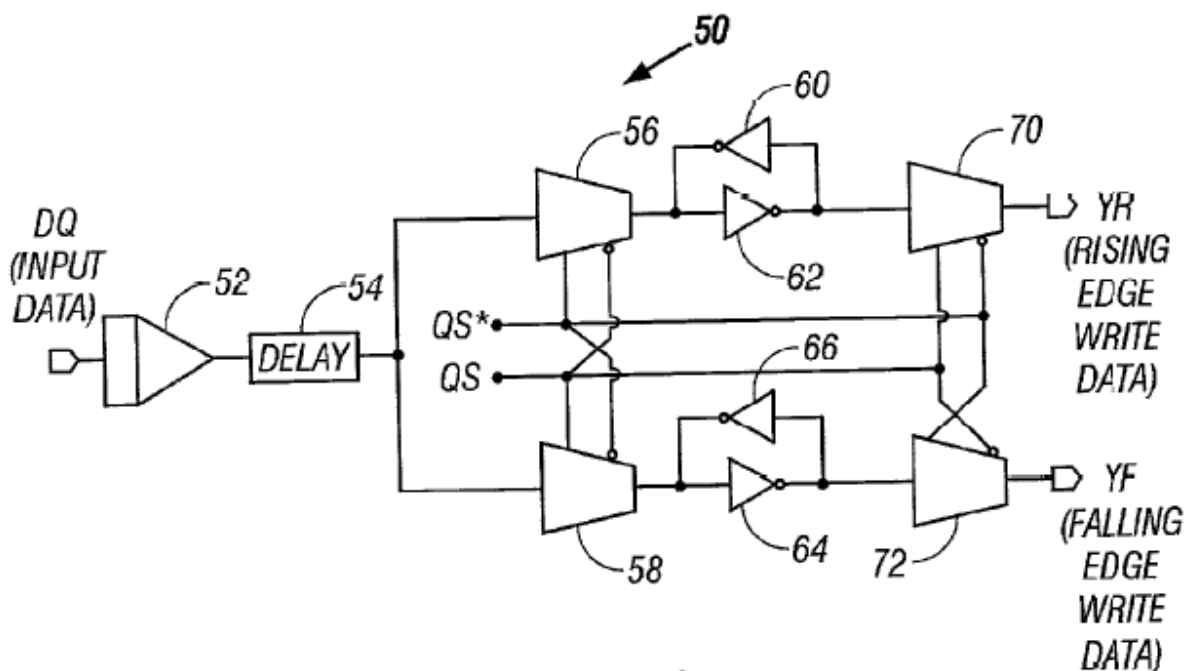


FIGURE 2
(Prior Art)

Ex. 1005, Fig. 2.

Petitioner also relies on Figure 4, which Stubbs describes as “a schematic/block diagram of write data path circuitry” i.e. circuitry for writing to a memory. *Id.* at [0024]. These two embodiments, and indeed everything in Stubbs, are about write paths for memories. Thus, while Petitioner represents that “Stubbs explains that a known problem is that different devices can have different propagation delays, causing misalignment between a data strobe and a data read/write operation” (Petition at 15 (emphasis added)), Stubbs only addresses write paths.

VII. THE PETITION DOES NOT ESTABLISH A REASONABLE LIKELIHOOD OF SUCCESS

To justify the institution of an *inter partes* review, a petitioner must establish that there is a “reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). Petitioner has not met its burden of establishing a reasonable likelihood of success at least because the Petition fails to show that one of ordinary skill would have chosen to combine the cited elements to achieve the claimed inventions of the ’608 Patent in addition to inaccurately characterizing the disclosure of those references. Consequently, the Board should deny the Petition and decline to institute the *inter partes* review.

A. The Petition Fails to Sufficiently Articulate Reasons to Combine the Disparate Elements of the References.

Petitioner asserts five proposed grounds, each a combination of two or more references. *See* Petition at Sections X-XIV (pp.25-72). With two exceptions, Petitioner alleges that every single limitation of the independent and dependent claims is disclosed by each of the cited references. *Id.* The two exceptions, not relevant to this Preliminary Response, are (1) for Ground 1, dependent claim 9, Petitioner alleges only that “Moss renders [the claim limitation] obvious” (Petition at 39); and (2) for Ground 2, dependent claim 8, Petitioner does not allege Moss discloses the limitation, but the other two references do (Petition at 47-48).

The result is that Petitioner has failed to clearly articulate what the purported combination being asserted for each claim or claim limitation actually is or why a particular element would be selected from a given reference or not. *See Sisvel Int'l S.A. v. Sierra Wireless, Inc.*, 82 F.4th 1355, 1364 (Fed. Cir. 2023) (“they never made clear to the Board what portions of the references were being combined and why a skilled artisan would identify those particular elements for a combination.”). Moreover, when Petitioner pieces together various structures and disclosures from the cited references to allegedly cobble together the claimed invention, Petitioner fails to show that a person of ordinary skill would have been motivated to combine such elements (and/or incorrectly characterizes the disclosure).

“Obviousness [] requires ‘a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does.’” *Johns Manville Corp. v. Knauf Insulation, Inc.*, IPR2018-00827, Paper 9 at 13 (PTAB Oct. 16, 2018) (quoting *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007)). “[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.” *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (emphasis in original; citations omitted); *see also Virtek Vision Int’l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 886-87 (Fed. Cir. 2024) (quoting same). The Petition fails to meet this standard for the combinations it proposes. The Petition’s purported motivations to combine these references are addressed in turn below.

1. The Petition’s General Motivations to Combine Are Insufficient.

Petitioner asserts that “[e]ach of Johnson, Stubbs, Moss, and Liou relate to memory controllers for use in DDR DRAM devices” Petition at 22. This is incorrect because as noted above neither Johnson nor Stubbs disclose a memory controller. *See supra* Sections VI.A & VI.C. In Johnson, the only discussions of a memory controller describe a memory controller providing signals and data to the memory device; there are no discussions of how the memory controller operates. *See, e.g.*, Ex. 1004 at 3:33-40; 4:11-22. Stubbs likewise at most discloses signals

coming into a DRAM, but it does not describe the structure or operation of a controller or even use the word “controller.” *See* Ex. 1005.

Petitioner relies on this argument merely to suggest that the references “are analogous art because they are in the same field of endeavor.” Petition at 22. Notwithstanding the inaccurate characterizations of Johnson and Stubbs, Petitioner’s assertion that the references are analogous art is not alone sufficient to articulate a motivation to combine. *See, e.g., Sisvel Int’l S.A. v. Sierra Wireless, Inc.*, 82 F.4th 1355, 1364 (Fed. Cir. 2023) (“We agree with the Board that Cross-Appellants’ first, second, and third reasons to combine were merely assertions that the references were analogous art, which, without more, is an insufficient articulation for motivation to combine.”). Accordingly, the Petition must provide some additional reasons to combine the references as asserted.

2. The Petition’s Motivations to Combine Johnson and Moss Are Insufficient.

Petitioner asserts that “[a] POSITA in possession of Johnson would look to Moss for further disclosure on systems and methods for delaying the data strobe (DQS) signal to produce an improved memory controller.” Petition at 22. The purported reasoning is because Johnson discloses one delay element (on write circuitry for a memory) that a POSITA “would look to Moss to incorporate a plurality of delay elements to the data strobe signal” “[t]o provide enhanced flexibility.” *Id.*

These conclusory assertions are insufficient to articulate a motivation to combine. Petitioner ignores and fails to address the fact that the circuitry in Johnson is write circuitry for a memory, and Petitioner offers no reason why a POSITA would look to the controller described in Moss to modify the memory in Johnson. Petitioner cannot gloss over the distinction between timing issues for writing data into a DRAM as opposed to reading data into a memory controller. The relationship between data and strobe signals are different for read and write data, and the controller and memory are in different clock domains with different constraints on how they receive data. Indeed, Moss discusses how to deal with different clock domains in the context of its disclosed invention (e.g., Ex. 1006 at 5:60-6:3), and to the extent Petitioner asserts that various circuitry and processes from a memory should be ported into such a system, or vice versa, a POSITA would require more detailed motivation for how and why.

Petitioner also ignores that neither Johnson nor Moss address providing delay on a per-bit basis. In fact, Johnson explicitly teaches that only one data path should be aligned before using that calibration for remaining paths. *See supra* Section VI.A; Ex. 1004 at 6:55-60; 7:25-29. Moss likewise does not address calibrating on a per bit basis. Moss's reference to different bit-widths for the data path are also neither here nor there. Regardless of what the size of the data path is, neither Johnson nor Moss teach or suggest calibration on a per bit basis of such a path. (And a single bit

data path would not be relevant to the challenged claims). Petitioner also relies on its expert's declaration which includes more words but the same substance and similarly makes the incorrect assertion that Moss "could be readily incorporated into *the memory controller architecture of Johnson*" since Johnson contains no memory controller architecture. *See* Ex. 1003 at ¶92.

3. The Petition's Motivations to Combine Stubbs and Moss Are Insufficient.

Petitioner's asserted reasons to combine Stubbs and Moss are essentially the same, if not less detailed than its assertions regarding Johnson and Moss. *See* Petition at 24. These assertions are conclusory and suffer from the same issues identified for the Johnson and Moss combination.

4. The Petition's Motivations to Combine Stubbs-Moss And Johnson Are Insufficient.

Petitioner's asserted reasons to add Johnson to the combination of Stubbs and Moss provide no further detail on the purported motivations. *See* Petition at 25. These assertions are conclusory and again suffer from the same issues identified for the other combinations above.

B. Petitioner's Proposed Grounds Fail to Demonstrate Obviousness of Any Independent Claims.

Petitioner has failed to demonstrate that either of independent claims 1 or 10 is obvious over the cited combinations in Grounds 1, 3, or 5. Because the remaining challenged claims all depend from these independent claims, should the Board agree

that trial should not be instituted on these claims, it necessarily follows that trial should not be instituted on the dependent claims, including claim 8 addressed in Grounds 2 and 4. Accordingly, Patent Owner briefly addresses the flaws in Grounds 1, 3, and 5 as they pertain to independent claims 1 and 10 below.

1. Ground 1: The Petition Fails to Demonstrate Obviousness Over Johnson in View of Moss.

Petitioner asserts that various aspects of Johnson and Moss could be combined to disclose the invention of claim 1 of the '608 Patent. Petition at 25-33. The proposed combination fails for at least few reasons. First, Johnson does not disclose a memory controller as discussed above. *See supra* Section VI.A. Here, however, Petitioner states that “Johnson describes an ‘integrated memory circuit’” (Petition at 25) in contrast to its statements elsewhere in the Petition suggesting that Johnson describes memory controllers (*e.g.*, Petition at 40 (“Johnson teaches a method of operation in an IC memory controller”).

Second, neither the disclosure from Johnson or Moss disclose element 1[a] requiring “a first *pin to receive a first data signal*” and “a first *adjustable delay element* to delay the received first data signal and generate a first delayed data signal.” Petition at 26 (emphasis added). For Johnson, the identified circuitry is a write path for a memory so it discloses no pin to “receive a first data signal” in a controller. *See* Ex. 1004 at 4:12-18; *see also supra* Section. VI.A. As to Moss, Petitioner incorrectly asserts that it includes delay line 330 is an adjustable delay.

Petition at 27. There is no indication in Moss that delay line 330 is adjustable. *See supra* Section VI.B. This same issue arises with Petitioner’s assertions for element 1[b] when it again asserts that Johnson discloses a pin to receive data, although this time pointing to a different embodiment (Johnson’s Fig. 4) and that Moss’s delay line is adjustable. Petition at 28-29.

For at least these reasons, Petitioner has failed to demonstrate its proposed combination of Johnson and Moss render claim 1 obvious. These reasons in addition to the issues identified above for motivation to combine, Petitioner’s insistence that each reference discloses every element without acknowledging which reference is missing the element, and which disclosure should be added to reach the claimed limitations further illustrate that Petitioner has failed to clearly articulate obviousness of claim 1 under Ground 1. *See Sisvel Int’l S.A. v. Sierra Wireless, Inc.*, 82 F.4th 1355, 1364 (Fed. Cir. 2023). Petitioner makes the same arguments for the other challenged independent claim 10 which fails for the same reasons. *See* Petition at 40-43.

2. Ground 3: The Petition Fails to Demonstrate Obviousness Over Stubbs in View of Moss.

Petitioner’s proposed combination of Stubbs and Moss fails for very similar reasons to those identified for Ground 1. First, Stubbs does not disclose a memory controller as discussed above. *See supra* Section VI.C. Here, however, Petitioner states that “Stubbs describes a semiconductor memory device with input/output

circuitry that functions as an integral component of an IC memory controller.” Petition at 48. As noted above, Stubbs does not even use the word “controller” and at most discloses the signals coming into a DRAM.

Second, neither the disclosure from Stubbs or Moss disclose element 1[a] requiring “a first *pin to receive a first data signal*” and “a first *adjustable delay element* to delay the received first data signal and generate a first delayed data signal.” Petition at viii (emphasis added); *id.* at 49. For Stubbs, the identified circuitry is a write path for a memory so it discloses no pin to “receive a first data signal” in a controller. *See* Ex. 1005 at [0024]; *see also supra* Section.VI.C. In fact, Petitioner refers to it as a write path but does not acknowledge or address the issue. *See* Petition at 49. As to Moss, Petitioner incorrectly asserts that it includes delay line 330 is an adjustable delay. Petition at 50. There is no indication in Moss that delay line 330 is adjustable. *See supra* Section VI.B. This same issue arises with Petitioner’s assertions for element 1[b] when it again asserts that Stubbs discloses a pin to receive data and that Moss’s delay line is adjustable. Petition at 50.

For at least these reasons, Petitioner has failed to demonstrate its proposed combination of Stubbs and Moss render claim 1 obvious. These reasons in addition to the issues identified above for motivation to combine, Petitioner’s insistence that each reference discloses every element without acknowledging which reference is missing the element, and which disclosure should be added to reach the claimed

limitations further illustrate that Petitioner has failed to clearly articulate obviousness of claim 1 under Ground 3. *See Sisvel Int'l S.A. v. Sierra Wireless, Inc.*, 82 F.4th 1355, 1364 (Fed. Cir. 2023). Petitioner makes the same arguments for the other challenged independent claim 10 which fails for the same reasons. *See* Petition at 59-62.

3. Ground 5: The Petition Fails to Demonstrate Obviousness Over Stubbs-Moss in View of Johnson.

Petitioner asserts that the combination of Stubbs in view of Moss as addressed in Ground 3 further combined with Johnson renders obvious independent method claim 10. Petition at 68-70. Petitioner, however, makes no new substantive arguments and all of the issues addressed previously in this Preliminary Response would apply. The addition of another reference however only compounds the issues already discussed with Petitioner's purported motivations to combine and ambiguity as to what one of ordinary skill would combine from the different references. For these reasons and in addition to those addressed to Grounds 1 and 3, Petitioner has failed to clearly articulate obviousness of claim 10 under Ground 5.

VIII. PATENT OWNER'S FINAL COMMENTS

Patent Owner does not concede the legitimacy of any arguments in the Petition that are not specifically addressed herein, and expressly reserves the right to rebut any such arguments in its Patent Owner Response if *inter partes* review is instituted. Similarly, Patent Owner also does not concede any underlying contentions in the

Petition and reserves the right to rebut them later. Additionally, Patent Owner is not limited to the arguments presented here in this Preliminary Response, but expressly reserves the right to raise further arguments, including claim construction arguments, not presented in this Preliminary Response.

IX. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board decline to institute *inter partes* review of the '608 patent.

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CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that this Preliminary Response complies with the type-volume limits of 37 C.F.R. § 42.24(b)(1) because it contains 6,017 words, excluding the parts of this Patent Owner's Preliminary Response that are exempted by 37 C.F.R. § 42.24(a), according to the word processing system used to prepare this Patent Owner's Preliminary Response.

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing Patent Owner's Preliminary Response was served on December 10, 2024, to Lead and Back-up Counsel for Petitioner at the service address provided in Petitioner's Mandatory Notices:

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