

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SILICON MOTION INC.,
Petitioner

v.

K.MIZRA, LLC,
Patent Owner.

IPR2024-01241
Patent 9,111,608 B2

Before MITCHELL G. WEATHERLY, MICHELLE N. WORMMEESTER,
and AARON W. MOORE, *Administrative Patent Judges*.

MOORE, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background*

Silicon Motion Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–2 and 4–15 (the “challenged claims”) of U.S. Patent No. 9,111,608 B2 (Ex. 1001, “the ’608 patent”). *See* Paper 1 (“Pet.”), 10–11. K.Mizra, LLC (“Patent Owner”) filed a Preliminary Response. *See* Paper 6 (“Prelim. Resp.”).

Under 35 U.S.C. § 314 and 37 C.F.R. § 42.4, we have authority to determine whether to institute an *inter partes* review. An *inter partes* review may not be instituted unless it is determined that “the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314 (2018); *see also* 37 C.F.R. § 42.4(a) (2020) (“The Board institutes the trial on behalf of the Director.”).

For the reasons provided below, and based on the present record, we determine that Petitioner has demonstrated a reasonable likelihood that it will prevail in showing the unpatentability of at least one of the challenged claims. Accordingly, we institute an *inter partes* review on all grounds set forth in the Petition.

B. *Related Proceedings*

The parties identify *K.Mizra, LLC v. Silicon Motion Inc.*, No. 2:24-cv-00101 (E.D. Tex. Feb. 15, 2024), as involving the ’608 patent and also identify, as related, U.S. Patent Application 18/094,895, which claims priority to the application that issued as the ’608 Patent. *See* Pet. 2; Paper 3, 2–3.

C. The '608 Patent

The '608 patent is titled “Strobe-offset control circuit” and it “relates to systems and methods for transferring information among memory devices and a memory controller.” Ex. 1001, 1:21–23.

The patent explains that “[o]ne memory type typically used in high-speed processing systems is double-data rate dynamic random access memory (DRAM),” which “is typically twice as fast as a single data rate DRAM running at the same clock speed because a double-data rate DRAM transfers data on both the rising and falling edge of the clock.” Ex. 1001, 1:41–46. The patent states that “issues arise [with DRAM] regarding the timing of the data transfer, particularly where a memory controller receives data sent by a double data rate DRAM . . . using a strobe-based method.” *Id.* at 1:49–52.

In a strobe-based method, “a strobe signal (also referred to as the DQS signal) is edge-aligned to and accompanies a data signal (also referred to as the DQ signal) sent by the DRAM.” Ex. 1001, 1:53–55. The DQS signal is delayed and “then used as a common sample clock for each of the DQ input receivers in typically a byte or 8 bits of data sent in parallel.” *Id.* at 1:61–63. However, due to system and pin-to-pin offsets in the DRAM, “one strobe-delay value for the whole byte cannot be the ideal amount of strobe-delay for every pin” and “requiring manual adjustments of these offsets in a production memory system tends to be expensive.” *Id.* at 1:65–2:3.

The patent further explains that the offset problem can be addressed with a calibration technique in which the “DRAM can be instructed to provide a known pattern to the controller,” which “adjusts its read-clock timing position to determine the pass-fail regions” and then “chooses an optimal read-clock position centered within the known passing region.” Ex.

1001, 2:7–15. Then, a strobe-delay value is determined for the optimal read-clock position. *See id.* at 2:15–16.

The patent explains that although the timing-calibrated memory systems can give better performance than strobe-based memory systems that use per-byte strobes, they are “substantially more complex.” Ex. 1001, 2:17–20. The patent concludes that “there is a need in high-speed, strobe-based memory systems, for per-pin (data bit) strobe-offset control and timing calibration to minimize DQS-to-DQ timing offsets for each DQ pin individually, yielding more robust, higher-speed systems.” *Id.* at 2:20–25.

Figure 1 of the '608 patent is a block diagram of one embodiment of a strobe-based memory system:

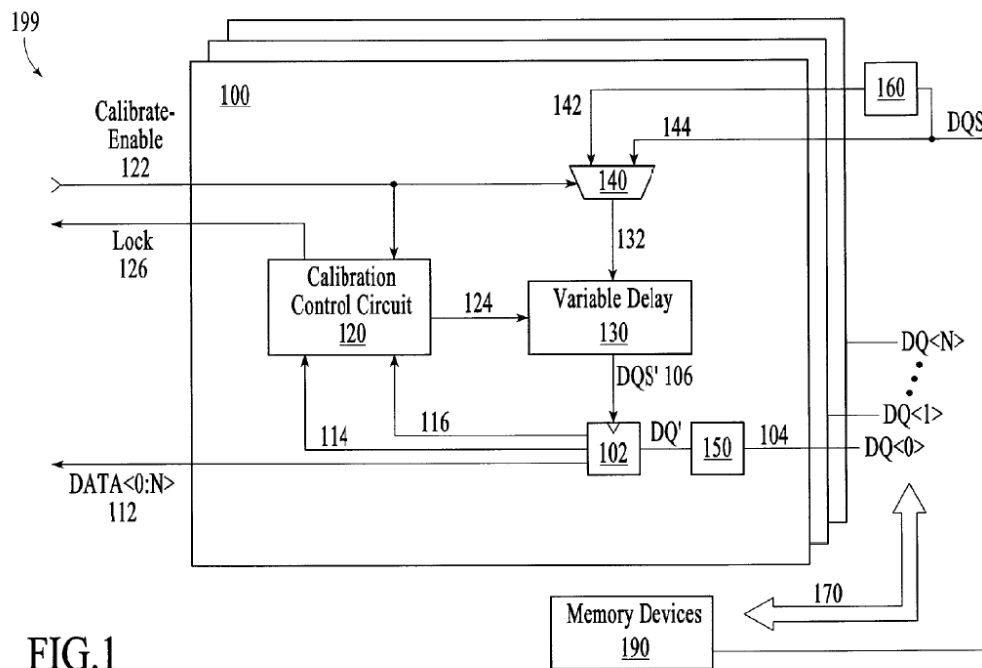


FIG.1

“FIG. 1 is a block diagram of a strobe-based memory system including a strobe-offset control system for individual data line strobe-offset control.” Ex. 1001, 2:36–38.

The system “includes a receiver 102 with a data input coupled to a data signal DQ<X> via a data line 104 through at least one data delay

element 150,” where “[t]he data signal DQ<X> includes information of one data bit of an N-bit wide data byte transferred to the receiver 102 from one or more memory devices 190 via one or more signal lines or buses 170.”

Ex. 1001, 4:25–30. The receiver “samples the data signal DQ<X> in response to the sample signal DQS’ 106 . . . and outputs data signal 112 that includes data <0:N>.” *Id.* at 4:30–32.

The system “also includes a multiplexer 140 that receives a delayed strobe signal at a first input 142 and a strobe signal DQS at a second input 144.” Ex. 1001, 4:34–36. The multiplexer, “under control of a memory controller or other device (not shown) via a calibrate-enable signal 122, provides one of the delayed strobe signal or the strobe signal DQS to an input 132 of a variable delay element 130.” *Id.* at 4:38–42.

The variable delay element 130 “generates sample signals DQS’ 106 by applying a delay to the signals received at the input 132” and “outputs the sample signal DQS’ via line 106 to the receiver 102.” Ex. 1001, 4:44–54.

The system also includes a calibration control circuit 120 which “under control of a memory controller or other device (not shown) of the memory system 199 via a calibrate-enable signal 122, operates in a calibration mode to adjust an amount of the delay or offset applied by the variable delay element 130 to versions of the strobe signal.” Ex. 1001, 4:58–62. The calibration control circuit 120 uses “an adjustment control signal 114 that affects the amount of offset applied by the variable delay element 130” and “an optional adjustment valid signal 116 from the receiver 102 that indicates when information of the adjustment control signal 114 is valid.” *Id.* at 4:67–5:5.

The patent explains that “the data signal DQ<X> . . . couples to the receiver 102 through at least one data delay element 150” and “the transmitted data signal DQ<X> is edge-aligned to the transmitted strobe signal DQS.” Ex. 1001, 5:17–22. “The data delay element 150 applies pre-specified delay to the received data signal (DQ<X>), and couples a delayed version of the data signal (DQ<X>') to the receiver 102.” *Id.* at 5:22–26.

The system operates in calibration and receiver modes. In the calibration mode, the receiver 102 “compares the phase relationship between the strobe signal DQS' and the delayed data signals DQ<X>' for each received data bit, and provides those comparison results to the calibration control circuit 120 via the adjustment control signal 114.” Ex. 1001, 5:41–45. In response to the adjustment control signal 114 (and optionally the adjustment valid signal 116), “the calibration control circuit 120 will adjust the delay control signal 124 which affects the delay value applied to the strobe signal DQS via the variable delay circuit 130.” *Id.* at 5:45–49.

The patent explains that “the calibration control circuit 120 can also store the information for subsequent use and/or processing,” “the information can be used to characterize the corresponding data paths of the memory system,” and “the data of this characterization can be used to generate offsets for use by the memory controller in memory write operations.” Ex. 1001, 5:67–6:6.

Figure 2 shows the steps of the calibration mode. The system configures the multiplexer to provide a strobe signal (step 204), the receiver is configured to compare timing of the edge positions of the strobe and data signals (step 206), a dummy read of the memory is initiated (step 208), any phase difference between the sample signal and the data signal is detected

(step 210), the offset applied to each sample signal is adjusted (step 212), and the lock signal is output (step 214). *See* Ex. 1001, 6:9–54,

Figure 3 shows the steps of the receiver mode. The multiplexer is configured to provide a delayed version of the strobe signal (step 304), the delayed strobe signal is provided as a sample signal (step 306), the delayed strobe signal is adjusted using the optimal offset (step 308), and the adjusted signal is output as the sample signal (step 310). *See* Ex. 1001, 6:55–8:20.

D. Illustrative Claims

Of the challenged claims, claims 1 and 10 are independent and are reproduced below:

1. An integrated circuit (IC) memory controller comprising:
 - a first pin to receive a first data signal;
 - a first adjustable delay element to delay the received first data signal and generate a first delayed data signal;
 - a second pin to receive a second data signal;
 - a second adjustable delay element to delay the received second data signal and generate a second delayed data signal;
 - a pin to receive a strobe signal;
 - a first sampling circuit to sample the first delayed data signal based on the strobe signal; and
 - a second sampling circuit to sample the second delayed data signal based on the received strobe signal.
10. A method of operation in an IC memory controller, the method comprising:
 - receiving first and second data signals from a memory device at respective first and second pins;
 - aligning the received first and second data signals with a strobe signal, the aligning comprising
 - imparting a first delay to the first data signal, the first delay corresponding to a first delay value,

imparting a second delay to the second data signal, the second delay corresponding to a second delay value.

E. Asserted Grounds of Unpatentability

Petitioner contends that the challenged claims are unpatentable under 35 U.S.C. § 103(a) on the following grounds:

Claims Challenged	Basis	References
1–2, 4–7, 9–15	§ 103	Johnson, ¹ Moss ²
8	§ 103	Johnson, Moss, Liou ³
1–2, 4–7, 9–15	§ 103	Stubbs, ⁴ Moss
8	§ 103	Stubbs, Moss, Liou
10–12	§ 103	Stubbs, Moss, Johnson

See Pet. 10–11. Petitioner also relies on a Declaration of R. Jacob Baker, Ph.D, filed as Exhibit 1003.

II. DISCUSSION

A. Patentability

A claim is unpatentable under 35 U.S.C. § 103 if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying

¹ U.S. Patent No. 6,434,081 (Exhibit 1004).

² U.S. Patent No. 6,646,929 (Exhibit 1006).

³ U.S. Pub. No. 2003/0179611 (Exhibit 1007).

⁴ U.S. Pub. No. 2003/0099135 (Exhibit 1005).

factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, objective evidence of non-obviousness.⁵ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

1. Level of Ordinary Skill in the Art

Petitioner asserts that one of ordinary skill in the art “would have at least a Bachelor’s degree in Electrical Engineering, Computer Engineering, or a related field, and 2-3 years of experience in memory system design,” or, alternatively, “a Master’s degree in one of those fields and 1-2 years of relevant experience.” Pet. 9 (citing Ex. 1003 ¶¶ 26–29). Patent Owner “does not contest Petitioner’s definition of a person of ordinary skill in the art, but it reserves the right to do so in the event that trial is instituted.” Prelim. Resp. 7. There being no present dispute, we adopt Petitioner’s formulation for purposes of this decision.

2. Claim Construction

A claim “shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b).” 37 C.F.R. § 42.100(b) (2020).

Petitioner asserts that “that no construction is necessary for any terms for the purposes of this Petition as the challenged claims are invalid under any reasonable construction.” Pet. 9. Patent Owner states that “the Board need not construe any claim term in a particular manner to arrive at the conclusion that the Petition is substantively deficient.” Prelim. Resp. 7.

⁵ At this stage of the proceeding, Patent Owner has not presented objective evidence of non-obviousness.

In view of the parties' positions, we determine that we need not expressly construe any terms for purposes of this Decision.

3. *Overview of the Primary References*

a) *Johnson*

Johnson is titled "Calibration Technique for Memory Devices" and generally describes "an improved binary calibration technique which is useful for calibrating the timing of control and data signals in memory devices, for example, SDRAM memory devices." Ex. 1004, 1:5–8.

With reference to Figures 1 and 2, reproduced below, Johnson describes a problem with a prior art calibration scheme. In Figure 1, the bits of the separate paths (CA<0> etc.) are skewed by half the width of the bits. Johnson explains that the incoming data bits may then be serially aligned, such that the edges line up, but that "it is possible that the data bits in one data path are misaligned, or aligned to an edge of the clock opposite to that of another data path." Ex. 1004, 2:31–33. This is shown in Figure 2, where the bits are edge-aligned, but may be offset by the width of an entire bit:

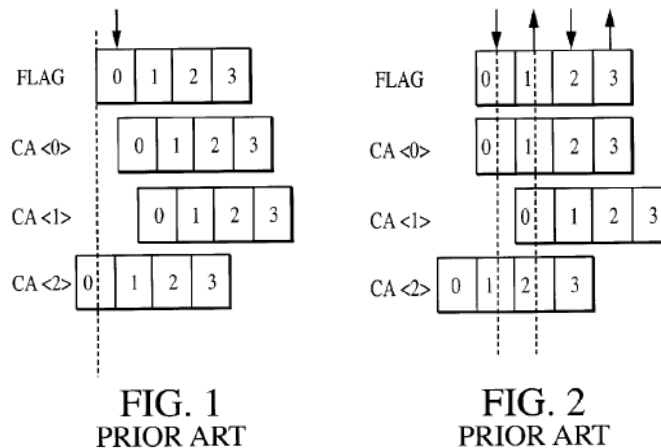


Figure 1 "illustrates raw data incoming on four different incoming data paths of a memory device" and Figure 2 "illustrates a serial alignment of the data bits incoming on the different data paths shown in [Figure 1]." Ex. 1004, 2:59–62.

Johnson describes a method to address that problem by aligning the bits in both the “serial” direction, as shown in Figure 2, and in the “parallel” direction, where the corresponding bits of each data path are correctly aligned with each other.

Johnson’s Figure 3, copied below, shows an exemplary environment in which the described invention may be used.

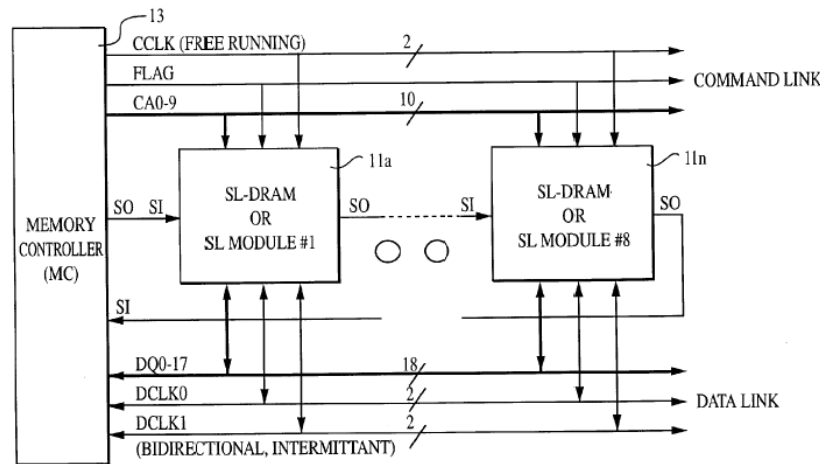


FIG. 3

Figure 3 “illustrates an SLD RAM bus topology with which [Johnson’s] invention may be used.” Ex. 1004, 2:63–64.

This system includes “a plurality of SLD RAM modules 11a . . . 11n which are accessed and controlled by a memory controller 13,” and “a command link to each of the SLD RAM modules” that “includes a clock signal CCLK on inverted and non-inverted clock signal paths, a 1 bit FLAG signal on a FLAG data path, and a 10 bit command bus data path CA0-9.” Ex. 1004, 3:31–38. “SLDRAM input/output enabling signals SO, SI are provided from memory controller 13 in daisy chain fashion” and “a bi-directional data bus DQ0-17 is provided between memory controller 13 and each of the SLD RAM modules . . . as are bi-directional data clocks DCLK0

and DCLKI.” *Id.* at 3:37–43. The clocks are “used to strobe input/output data into and out of the SLD RAM modules.” *Id.* at 3:43–44.

Figure 4, reproduced below, shows a “relevant portion of one of the SLD RAM modules,” including “a control logic circuit 21, latches 23, 25, 49, 59, delay devices 27, 29, 31, 55, 57 which may be ring delay devices, buffers 35, 37, 39, 33, 45, 47, 51, 53, a delay lock loop 41, multiplexer 43, pipeline circuits 61, 63, SRAM input/output circuits 65 and 67, and respective memory banks Bank0 and Bank1 69, 71.” Ex. 1004, 3:47–54.

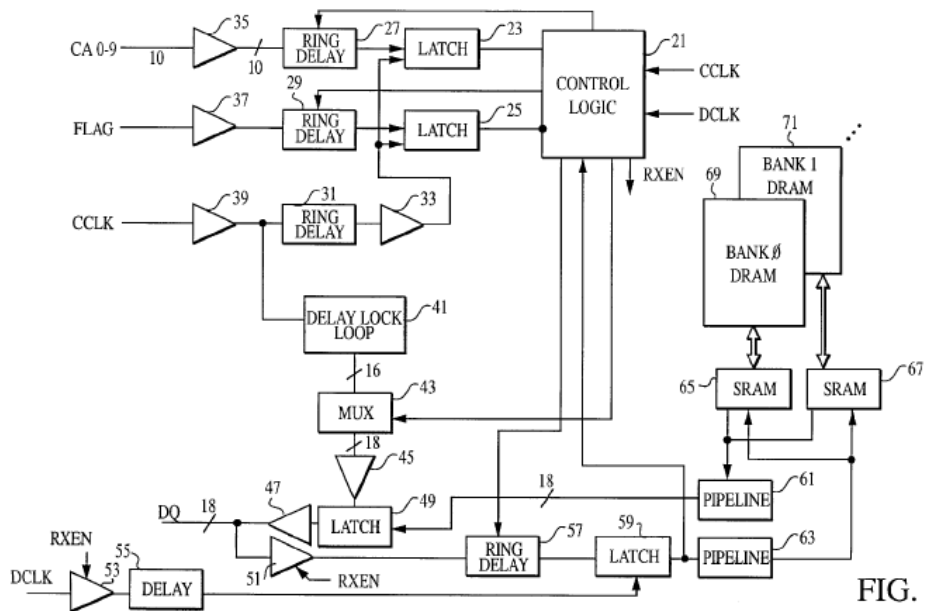


FIG. 4

Figure 4 “illustrates a portion of the SLD RAM module shown in [Johnson’s Figure 3].” Ex. 1004, 2:66–67.

The multiplexer “provides 18 clock output signals through respective buffers 45 to 18 latches 49 which latch data output from the memory banks 69, 71,” and “[t]he output data from memory banks 69, 71 pass into SRAMS 65, 67 which act as I/O buffers and pass through pipeline circuit 61 before being loaded into latches 49.” Ex. 1004, 4:3–8. “The output data latched in

latches 49 is provided to . . . buffer amplifiers 47 and from there is passed back to memory controller 13 (FIG. 3) via data bus DQ.” *Id.* at 4:8–11.

Conversely, “[d]ata which is to be input to memory banks 69, 71 is supplied by memory controller 13 (FIG. 3) on the DQ data bus, is passed through gated buffers 51 through ring delays 57 on each path of the data bus, into latches 59, through pipeline circuit 63,” and then “into buffer SRAM 65, 67 and into a memory bank 69, 71.” Ex. 1004, 4:12–18.

In order to ensure proper timing, the “circuit must be synchronized to ensure that the incoming data is properly clocked in by the clock signals CCLK and DCLK.” Ex. 1004, 4:27–31. This is accomplished by applying a 2N bit synchronizing pattern to each of the data input paths CA0-9 and FLAG while the data pattern is sampled in latches 23 and 25 by the delayed clock signal CCLK. *See id.* at 4:31–36. The control logic circuit “steps through all possible delay positions of ring delays 27 and 29 as the data sampling is performed and stores patterns representing which delay values for the ring delays 27 and 29 provide for a correct sampling,” establishing an “eye” or “window” of acceptable delays for each of the ring delays. *See id.* at 4:36–44. “[T]he control logic circuit 21 determines the ‘best’ delay value as that value which is approximately in the middle of the window.” *Id.* at 4:46–48. This results in the serial alignment shown in Figure 2, but, as noted, it may result in parallel misalignment. Johnson’s stated improvement is a method to ensure both serial and parallel alignment.

Johnson's parallel alignment is accomplished with the control logic circuit 21 detailed in Figure 9, which is reproduced below.

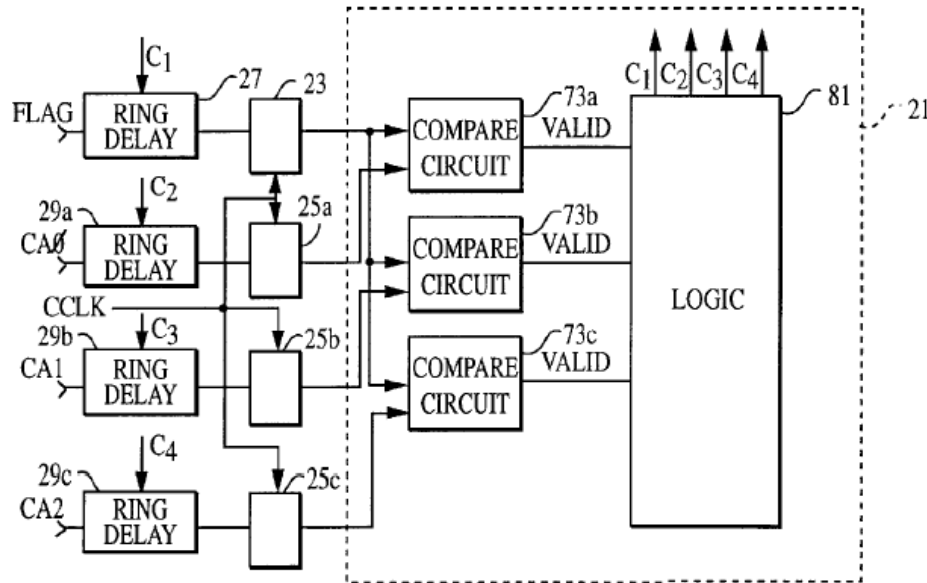


FIG. 9

Figure 9 “illustrates an exemplary circuit for implementing a first embodiment of [Johnson’s] invention.” Ex. 1004, 3:11–12.

This figure shows a “a plurality of compare circuits 73a, 73b, 73c for the illustrated data paths FLAG, CA<0>, CA<1>, and CA<2> which are representative of the data paths FLAG, and CA0-9 and DQ0-17.” Ex. 1004, 6:43–46. “[S]ignals C1, C2, C3, C4 [are] used by the logic 81 to control the delay settings of the ring delays 27, 29a, 29b, 29c, respectively,” and “VALID signals are generated by the compare circuits 73a, 73b, 73c to signal whether the synchronization pattern is properly recognized to the logic 81.” *Id.* at 6:49–54.

To achieve parallel alignment, one of the incoming data paths is serially aligned, as described above, and “the control logic circuit 21 then compares the newly aligned calibration pattern on the aligned data path . . .

with the calibration pattern from another data line . . . which is to be aligned.” Ex. 1004, 6:55–60. The circuit “establishes an initial delay value for the ring delay 29 . . . of the CA<0> line and compares the outputs from the latch circuit 23 of the previously aligned data path with the latch circuit 25a of the data path undergoing calibration.” *Id.* at 6:61–65. The circuit will increment the ring delay looking for a match in the calibration patterns from latches 23 and 25a. *See id.* at 6:65–7:2. “This establishes a range of delays where the data on data path CA<0> is both serially aligned as well as aligned in parallel with data on the FLAG data path” and “[t]he control logic circuit 21 will then set the delay value for ring delay 29a as a value at or near the center of the delay values which produced a match of the calibration patterns emerging from the latch circuits 23 and 25a.” *Id.* at 7:8–20.

Figure 10 illustrates how the circuit “can also be arranged to compare a next data path to be calibrated to a just calibrated data path and control the incremental adjustment of the ring delay for the new data path in the [same] manner.” *Id.* at 7:25–28.

b) Stubbs

Stubbs is titled “Per-bit set-up and hold time adjustment for double-data rate synchronous dram” and “relates to an apparatus and corresponding method by which data is written to a synchronous, double-data-rate semiconductor memory device.” Ex. 1005 ¶ 17.

Stubbs identifies “a recent development in the evolution of synchronous DRAM technology,” the “so-called ‘double data rate (DDR) DRAM’” in which “data is written into data buffers on both the rising and falling edges of each clock cycle, thus providing twice as much data as a conventional SDRAM for a given system clock speed.” Ex. 1005 ¶ 12.

The reference explains that “[d]ue to the high speed data transfers, DDR SDRAMs use a bi-directional data strobe signal (DQS) to register the data being input or output on both edges (rising and falling) of a system clock” and that “[a]ccording to industry standards, when data is being received by a DDR SDRAM, the DQS has a known latency which can vary between $3/4$ of a system clock cycle (minimum latency) to $[5/4]$ of the clock cycle (maximum latency).” Ex. 1005 ¶ 13. Due to the latency variation, “[w]hen data is being received by a DDR SDRAM, the system clock cannot be properly . . . synchronized with the input data.” *Id.*

The variation in latency can be addressed with “a delay element in the write data path to internally delay data relative to the data strobe,” where, “[b]y making the delay element variable, the input setup and hold times can be adjusted to ensure that specified setup and hold times are achieved.” Ex. 1005 ¶ 15.

There is a further problem, however, which is that “the setup and hold window can be different for the data clocked in on the rising edge than for the data clocked in on the falling edge,” causing “the total setup and hold window for the input pin [to] the overlap of the windows for the two clock edges, which can be larger than permissible according to the memory device’s specification.” Ex. 1005 ¶ 15. That is the problem Stubbs was seeking to address and the solution, as described below, was to replace the single delay element on the data line with one variable delay element for the path corresponding to the rising edge of the clock signal and another variable delay element for the path corresponding to the falling edge of the clock signal. *See* Ex. 1005 ¶¶ 45–47.

Figure 4 of Stubbs shows an implementation with two variable delay elements 102 and 104:

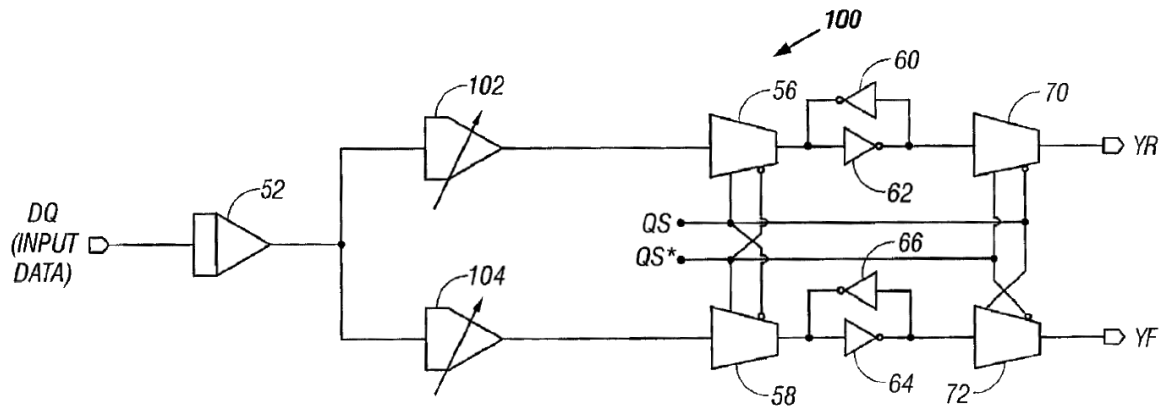


FIGURE 4

Figure 4 “is a schematic/block diagram of write data path circuitry in accordance with one embodiment of the invention.” Ex. 1005 ¶ 24.

This figure shows input buffer 52, gates 56, 58, 70, and 72, and buffer/boost inverter pairs 60/62 and 64/66. Ex. 1005 ¶ 47. It also shows “a pair of adjustable delay elements 102 and 104” that are “adapted to introduce a delay into the propagation of data signals applied to their inputs.” *Id.* The delayed data signal output of adjustable delay 102 is applied to the input of pass gate 56, and the delayed data signal output of adjustable delay 104 is applied to the input of pass gate 58. *See id.*

Stubbs explains that “[i]t will be apparent to those of ordinary skill in the art that by providing separate delays for the rising edge data path . . . and the falling edge data path . . . , the delay in the arrival of the DQ data signal at the input of pass gate 56 can be different than the delay in the arrival of the DQ data signal at the input of pass gate 58.” Ex. 1005 ¶ 47. This allows “the worst-case setup and hold times for rising edge data” to be “optimized

independently from the worst-case setup and hold times for the falling edge data.” *Id.*

4. *Analysis of Claim 1 in View of Johnson and Moss*

Grounds 1 and 2 position Johnson as a base reference, alternatively citing Moss and Liou for certain features. *See* Pet. 25–48.

For claim 1, Petitioner argues that, if the preamble is limiting, Johnson discloses a “memory controller.” *See* Pet. 25.

With regard to element 1[a],⁶ Petitioner argues that Johnson’s Figure 4 “shows a data path DQ that includes a pin to receive an incoming data signal and a ring delay 57 to delay that received data signal.” Pet. 26 (citing Ex. 1003 ¶¶ 112–114; Ex. 1004, Fig. 4, 7:25–60).

For element 1[b],⁷ Petitioner points to Figure 10, arguing that “Johnson also discloses a ‘second pin to receive a second data signal’ (signal DQ1), a ‘second adjustable delay element’ (ring delay 57b) that generates a ‘second delayed data signal’ (input to latch 59b).” Pet. 28 (citing Ex. 1003 ¶ 199; Ex. 1004, 4:36–52, 7:24–60).

With regard to element 1[c],⁸ Petitioner asserts that “Johnson discloses a pin to receive a strobe signal DCLK, which is used to clock data into and out of the memory device.” Pet. 29 (citing Ex. 1003 ¶¶ 122–123; Ex. 1004, Fig. 4, 4:24–5:7).

⁶ “a first pin to receive a first data signal; a first adjustable delay element to delay the received first data signal and generate a first delayed data signal”

⁷ “a second pin to receive a second data signal; a second adjustable delay element to delay the received second data signal and generate a second delayed data signal”

⁸ “a pin to receive a strobe signal”

For element 1[d],⁹ the Petition points to Figure 10, and, specifically, “latch 59a [which] serves as a ‘first sampling circuit to sample the first delayed data signal based on the strobe signal.’” Pet. 30 (citing Ex. 1003 ¶¶ 127–128; Ex. 1004, 4:12–26).

Finally, for element 1[e],¹⁰ Petitioner contends that, Johnson, in Figure 10, “discloses a ‘second sampling circuit to sample the second delayed data signal based on the strobe signal’ with respect to the data path originating from DQ1, through ring delay 57b and latch 59b.” Pet. 32 (citing Ex. 1003 ¶ 131).

Patent Owner argues that Petitioner’s showing regarding a motivation to combine Johnson and Moss is inadequate. *See* Prelim. Resp. 20–24. We tend to agree. In the “Motivation to Combine Johnson and Moss” section, the Petition first asserts that “Johnson and Moss are in the same field of endeavor,” which is insufficient without more to provide a motivation. *See, e.g., Sisvel Int’l S.A. v. Sierra Wireless, Inc.*, 82 F.4th 1355, 1364 (Fed. Cir. 2023). The Petition then asserts that “[t]o provide enhanced flexibility, [one of ordinary skill in the art] in possession of Johnson would look to Moss to incorporate a plurality of delay elements to the data strobe signal.” Pet. 22. This is not persuasive because (a) Petitioner argues that Johnson already provides a plurality of delay elements, (b) Petitioner fails to explain where or how additional delay elements from Moss would be added to Johnson, and (c) Petitioner fails to explain how or why the modification would “provide enhanced flexibility,” or even what “enhanced flexibility” might mean in

⁹ “a first sampling circuit to sample the first delayed data signal based on the strobe signal”

¹⁰ “a second sampling circuit to sample the second delayed data signal based on the received strobe signal”

this context. Petitioner also argues that “Moss further discloses that the size of the data path – i.e. the number of data pins in each data path – is a design choice well within the knowledge and ability of a POSITA, and expressly recites examples of 4, 8, and 16-bit wide data paths.” Pet. 23. We agree that varying the width of the data path would have been within level of ordinary skill and would have depended on the particular application, but the Petition fails to explain how or why that would have made it obvious to incorporate various elements of Moss into Johnson.

Although we find the motivation lacking, the Petition asserts that all of the features of claim 1 are found in Johnson, so we turn to Patent Owner’s other arguments.

Patent Owner’s second argument is that “Johnson does not disclose a memory controller.” Prelim. Resp. 25. This argument fails for two reasons.

First, the subject claim language appears in the preamble, and Patent Owner has not made any effort to overcome the “general rule [that] preamble language is not treated as limiting.” *Aspex Eyewear, Inc. v. Marchon Eyewear, Inc.*, 672 F.3d 1335, 1347 (Fed. Cir. 2012) (citing *Allen Eng’g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1346 (Fed. Cir. 2002)). Here, the preamble does not provide antecedent basis for any element in the body of the claim, the body of the claim appears to define a structurally complete invention, and the claim appears to use the preamble only to state a purpose or intended use for the invention (as part of a memory controller). *See Arctic Cat Inc. v. GEP Power Products, Inc.*, 919 F.3d 1320, 1328 (Fed. Cir. 2019); *Catalina Mktg. Int’l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002)). The parties may address this issue as a matter of

claim construction during the trial, but, on this record, we see no reason to determine whether the preamble is limiting.

Second, even if the preamble were limiting, we note that Johnson’s calibration circuitry bears the same relationship to the “memory controller” as the calibration circuitry disclosed in the ’608 patent, which explains that it operates “under control of a memory controller or other device,” which is “not shown.” Ex. 1001, 4:38–39. Both the subject circuitry of the ’608 patent and the subject circuitry of Johnson sit between a memory controller and the memory devices. Patent Owner’s argument thus appears to amount to a line drawing exercise—whether “memory controller” includes the calibration components—and we see no reason to treat the analogous disclosures of the patent and the prior art differently in that respect.

Patent Owner’s third argument is that the combination does not disclose “a first pin to receive a first data signal” and “a first adjustable delay element to delay the received first data signal and generate a first delayed data signal.” See Prelim. Resp. 25. Specifically, Patent Owner contends that “[f]or Johnson, the identified circuitry is a write path for a memory so it discloses no pin to ‘receive a first data signal’ in a controller. *Id.* (citing Ex. 1004 at 4:12–18). To the extent this argument is understood, it is not persuasive. We consider “pin” in this context to refer to an input or output of a circuit component, and find, on this record at least, that data signals on Johnson’s data lines DQ would be received at a “pin” and then pass through ring delays 57, generating a delayed data signal. To the extent this argument is about the circuitry not being in a “controller,” it is unavailing because, as explained above, that is not required by the claim or,

alternately, Johnson's control circuitry is part of a controller in the same way the '608 patent's calibration circuitry is part of a controller.

Because we agree with Petitioner's analysis and find Patent Owner's arguments regarding Johnson unpersuasive, we conclude that Petitioner has shown a reasonable likelihood of proving claim 1 unpatentable as obvious in view of Johnson.

We do, however, have a couple of observations that the parties may wish to address during trial. First, Petitioner appears to rely on Figure 4, which is used in Johnson's discussion of serial alignment, for the first pin and delay element, but on Figure 10, which is used in Johnson's discussion of parallel alignment, for the second pin and delay element. The parties may consider whether that presents a problem, particularly where the description associated with Figure 10 describes how "a first data path, e.g., DQ0, is serially aligned to DCLK using the technique described with reference to FIGS. 1-7," and the "remaining DQ1-17 data paths can then be aligned by comparing the calibration pattern of a subsequent non-aligned data path to the calibration pattern which exists on a previously aligned data path." Ex. 1004, 7:36–42. Second, the parties may wish to consider whether Figure 4 and its associated description are sufficient to establish unpatentability without reference to Figure 10, and whether the Petition would support a finding on that basis.

4. *Analysis of Claim 1 in View of Stubbs and Moss*

Grounds 3 through 5 present Stubbs as a base reference, optionally adding Moss and Liou or Johnson for certain features. *See* Pet. 48–72.

For the preamble of claim 1, Petitioner argues that Stubbs discloses a memory controller. *See* Pet. 48–49.

With regard to element 1[a],¹¹ Petitioner argues that “Stubbs’ write path circuit includes an input buffer that receives data from an external data pin, corresponding to the claimed first pin, and a first delay element coupled to the input buffer’s output, which is adjustable and generates a first delayed data signal.” Pet. 49 (citing Ex. 1003 ¶ 197; Ex. 1005, Fig. 4, ¶¶ 47–48).

For element 1[b],¹² Petitioner argues that “[f]or each of [the] input/output pins, a separate write path circuit is provided, which includes an input buffer and an adjustable delay element, directly corresponding to the claimed second pin and second adjustable delay element.” Pet. 50 (citing Ex. 1003 ¶ 200; Ex. 1005 ¶¶ 47–48).

With regard to element 1[c],¹³ Petitioner asserts that “Stubbs teaches a pin to receive a strobe signal, where the memory device receives an externally-applied clock signal CLK at an input pin that is used to generate an internal data strobe signal QS/QS for controlling input data sampling.” Pet. 51 (citing Ex. 1003 ¶¶ 203–204; Ex. 1005 ¶¶ 5, 7, 35–36).

For element 1[d],¹⁴ Petitioner asserts that “Stubbs teaches a first pass gate 56 that samples a delayed data signal output from delay element 102 based on a data strobe signal QS/QS*.” Pet. 52 (citing Ex. 1003 ¶ 207; Ex. 1005, Fig. 4, ¶ 37).

¹¹ “a first pin to receive a first data signal; a first adjustable delay element to delay the received first data signal and generate a first delayed data signal”

¹² “a second pin to receive a second data signal; a second adjustable delay element to delay the received second data signal and generate a second delayed data signal”

¹³ “a pin to receive a strobe signal”

¹⁴ “a first sampling circuit to sample the first delayed data signal based on the strobe signal”

Finally, for element 1[e],¹⁵ Petitioner contends that “Stubbs teaches that the write path circuitry shown in Figure 4, including the sampling circuits, is replicated for each input/output (DQ) pin of the memory device, meaning there is a second sampling circuit for a second data pin.” Pet. 53 (citing Ex. 1003 ¶ 210; Ex. 1005 ¶ 46).

For these grounds, Patent Owner argues only that the “combination of Stubbs and Moss fails for very similar reasons to those identified for Ground 1,” namely that “Stubbs does not disclose a memory controller” and that neither reference discloses “element 1[a] requiring ‘a first pin to receive a first data signal’ and ‘a first adjustable delay element to delay the received first data signal and generate a first delayed data signal.’” Prelim. Resp. 26–27. We find these arguments unpersuasive for the reasons provided above in the discussion of those same arguments as raised for Grounds 1 and 2.

Because we agree with Petitioner’s analysis and find Patent Owner’s arguments regarding Stubbs unpersuasive, we conclude that Petitioner has shown a reasonable likelihood of proving claim 1 unpatentable as obvious in view of Stubbs.

5. *Remaining Claims*

At this stage, Patent Owner does not separately challenge Petitioner’s contentions as to claims 2 and 4–15. Having reviewed Petitioner’s arguments and evidence for these claims, we are persuaded that Petitioner’s showing for claims 2 and 4–15 is sufficient for purposes of this Decision. *See* Pet. 25–47, 53–71.

¹⁵ “a second sampling circuit to sample the second delayed data signal based on the received strobe signal”

III. CONCLUSION

After considering the evidence and arguments presented in the current record, we determine that Petitioner has demonstrated a reasonable likelihood of success in proving that at least one of the challenged claims of the '608 patent is unpatentable. We therefore institute trial on all challenged claims and grounds raised in the Petition. *See PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (2018) (a decision whether to institute an *inter partes* review “require[s] a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition”).

At this stage of the proceeding, we have not made a final determination as to the patentability of any challenged claim or as to the construction of any claim term.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–2 and 4–15 of the '608 patent is instituted with respect to all grounds set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '608 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

IPR2024-01241
Patent 9,111,608 B2

PETITIONER:

Jeffrey Johnson
Parker Hancock
BAKER BOTTS L.L.P.
Jeffrey.Johnson@bakerbotts.com
Parker.Hancock@bakerbotts.com

PATENT OWNER:

David T. DeZern
Justin B. Kimble
NELSON BUMGARDNER CONROY P.C.
david@nelbum.com
justin@nelbum.com