Nader Bagherzadeh, Ph.D.

Expertise

- Digital Signal Processing Architectures
- Processor Architectures (VLIW, Superscalar)
- VLSI Design
- Computer Networks & Digital Telecommunication
- Computer Graphics
- Memory System Architecture
- DRAM, SRAM, EEPROM, and Flash memory
- Automotive Computing
- Error Detection and Correction
- Machine Learning Accelerators

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Education

Year	College/University	Degree
1987	The University of Texas at Austin	Ph.D., Computer Engineering
1979	The University of Texas at Austin	MS, Electrical Engineering
1977	The University of Texas at Austin	BS (with honors), Electrical Engineering

Employment History

From:	1987	**University of California at Irvine**
To:	Present	Irvine, CA
	Position:	*2003- Present: Professor, Department of Electrical Engineering and Computer Science* *1998-2002: Professor and Chair, ECE/EECS Department* *1993-1997: Associate Professor, ECE Department* *1987-1992: Assistant Professor, ECE Department*

From:	1980	**AT&T Bell Labs**
To:	1984	Holmdel, NJ
	Position:	*Member of Technical Staff, No.5 ESS Hardware/Software T1Line Interface Design*

Awards and Honors

1973-77	Dean's honor roll for six semesters; UT Austin
1984	Outstanding achievement award; AT&T Bell Labs
2002	Best Paper award in IEEE Transactions on VLSI Design
2002	Best Student Paper award in the proceedings of ASPDAC'02
2014	Khwarizmi International Award
2014	IEEE Fellow
2015	Professor of the Year for the EECS Department, UCI
2020	Best Paper award in the proceedings of IEEE EDGE Computing

Consulting History

From:	2006	**STEC**
To:	2008	Irvine, CA
	Duties:	Flash memory CODEC design and evaluation

From:	2006	**Tialinx**
To:	2008	Newport Beach, CA
	Duties:	Radar DSP board design and evaluation

From:	2000	**Morpho Technologies**
To:	2005	Irvine, CA
	Duties:	Co-Founder; DSP design for communication and multimedia systems

Litigation Support Experience

Date:	2024	**Kirkland & Ellis LLP**
	Case	*TCL Electronics Holdings Ltd. vs. Intellectual Ventures I LLC*
	Project:	Expert Witness for TCL
	Status:	IPR pending
	Contact:	Russell Levine 300 North LaSalle Chicago, IL 60654 Direct Dial: (312) 862 2466 Rusell.levine@kirkland.com

Date:	2024	**Covington & Burling LLP**
	Case	*Redstone Logics LLC v. Samsung Electronics Co., Ltd.*
	Project:	Expert Witness for Samsung Electronics Co., Ltd.
	Status:	IPR pending
	Contact:	Ali Mojibi 1999 Avenue of the Stars Los Angeles, CA 90067-4643 (424) 332 4803 amojibi@cov.com

Date:	2023	**Finnegan, LLP**
	Case	TBD
	Project:	Expert Witness for Nissan Motor Co.
	Status:	In progress
	Contact:	Luke McCammon 901 New York Avenue, N.W. Washington, D.C., 20001 Direct Dial: (202) 408-4273 Luke.McCammon@finnegan.com

Date:	2023	**REICHMAN JORGENSEN LEHMAN & FELDBERG LLP**
	Case	TBD
	Project:	Expert Witness for Valtrus Innovation Ltd
	Status:	In progress
	Contact:	Patrick Colsher 100 Marine Parkway, Suite 300 Redwood Shores, CA 94065 Direct Dial: (650) 623-1427 pcolsher@reichmanjorgensen.com

Date:	2023	**McKool Smith**
	Case	*TexasLDPC Inc. v Broadcom Inc., LSI Corporation, Avago Technologies U.S., Inc.; C.A. No. 18-1966-SB*
	Project:	Expert Witness for Broadcom
	Status:	Dismissed without prejudice
	Contact:	Steven Rizzi One Manhattan West

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Date: 2023 **Caldwell Cassidy & Curry**
Case BeSang Inc. v. Intel and/or Micron, CIVIL ACTION NO. 2:23-CV-00028-JRG-RSP and Case No. 3:23-cv-00113-HZ
Project: Expert Witness for BeSang
Status: Stay
Contact: Bjorn A. Blomquist
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Date: 2023 **Mintz**
Case Daedalus v. Qualcomm Inc. and Samsung Electronics Co.
Project: Expert Witness for Daedalus Prime LLC
Status: ITC, provided technical support without rendering an opinion in a report. Case is closed.
Contact: Peter F. Snell
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Date: 2022 **Arnold & Porter**
Case Rex Computing, Inc. v. Cerebras Systems Inc.
Project: Expert Witness for Rex Computing, IPR Petition by Cerebras
Status: Board sided with Rex and did not grant the petition
Contact: Nicolas Lee,
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Date: 2022 **Quinn Emanuel Urquhart & Sullivan, LLP,**
Case MediaTek Inc. v. NXP Semiconductors N.V.
Project: Expert Witness for Media Tek
Status: Settled
Contact: Jordan B. Kaericher
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Los Angeles, CA 90017
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Date: 2022 **Bartlit Beck LLP**
Case Viasat vs. Kioxia and Western Digital, Patent Litigation Consulting
Project: Expert Witness for Viasat. Provided declaration
Status: IPR; Board decided in favor of Viasat
Contact: Scott McBride
54 West Hubbard Street
Chicago, IL 60654
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Date: 2022 **Arch & Lake LLP**
Case Autel v. Hunter Engineering Company
Project: Expert Witness for Autel. Provided patent analysis
Status: Inactive
Contact: Hao Tan,
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Chicago, IL 60601
Direct Tel.: (312) 558-1368
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Date: 2022 **Adhoot & Wolfson PC and Miller Shah LLP**
Case Winnie Clark et al v. American Honda Motor Co., Inc.,
Project: Brief discussion for the Class; no additional duties
Status: Class Action Consideration
Contact: Christopher Stiner
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cstiner@ahdootwolfson.com

Date: 2021 **Kilpatrick Townsend, LLP**
Case Autel Intelligent Tech. Corp., LTD vs. Orange Electronic Co., LTD
Project: Expert Witness for Autel. Provided IPR declaration
Status: Pending IPR Decision
Contact: David A. Reed,
Suite 2800, 1100 Peachtree Street NE
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Company: (404) 815-6500
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Date: 2021 **Desmarais LLP**
Case AMD, QCM, and STM vs. Monterey Research
Project: Expert Witness for Monterey. Provided IPR declarations and was deposed.
Status: Settled
Contact: Jordan Malz,
230 Park Avenue
New York, NY 10169
Direct Tel.: (212) 351-5497
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Date: 2020 **Devlin Law Firm LLC**
Case Engagement for Assistance with Certain Patents Asserted by Flash-Control, LLC
Project: Expert Witness for Flash Control. Provided IPR declaration and was deposed.
Status: Pending IPR Decision
Contact: Jim Lennon,
1526 Gilpin Avenue
Wilmington, Delaware 19806
Tel.: (302) 449-9010
Cell: (302) 593-4486
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Date: 2019 **The Honorable David O. Carter**

	Case	Limestone Memory Systems vs. Micron Technology, et al.
	Project:	Special Master for Judge Carter
	Status:	Settled
	Contact:	Judge David O. Carter, Ronald Reagan Federal Building, United States Courthouse 411 West Fourth Street, Courtroom 9D Santa Ana, CA 92701-4516

Date:	2018	**Arnold & Porter Kaye Scholer LLP**
	Case	Samsung Electronics Co. Ltd. vs. Home Semiconductor Corp.
	Project:	Expert Witness for Samsung
	Status:	Case dismissed
	Contact:	Ali Sharifahmadian, 601 Massachusetts Ave., NW Washington, DC 20001-3743 (202) 942 6370 Ali.Sharifahmadian@arnoldporter.com

Date:	2018	**Fried, Frank, Harris, Shriver & Jacobson LLP**
	Case	Intel Corp. vs. Godo Kaisha IP Bridge 1
	Project:	Expert Witness for IP Bridge
	Status:	Closed IPR
	Contact:	Robert Masters, 801 17th Street, NW Washington, DC 20006 (202) 639 7370 robert.masters@friedfrank.com

Publications

Journals Refereed

j1 P. Suhler, N. Bagherzadeh, M. Malek, and N. Iscoe, "Software authorization systems," *IEEE Software*, pp. 34-41, September 1986.

j2 A. Guzman, E. Krall, P. McGehearty, and N. Bagherzadeh, "Performance of symbolic applications on a parallel architecture," *International Journal of Parallel Programming*, vol. 16, no.3, pp. 183-214, 1987.

j3 Y. Moon, N. Bagherzadeh, and J. Sklansky, "A macropipelined multicomputer architecture for image analysis," *Journal of the Optical Society of America*, pp. 951-962, 1989.

j4 D. Blough and N. Bagherzadeh, "Near-optimal message routing and broadcasting in faulty hypercubes," *International Journal of Parallel Programming*, vol. 19, no. 5, pp. 405-423, 1990.

j5 N. Bagherzadeh, S. Heng, and C. Wu, "A parallel asynchronous garbage collection algorithm for distributed systems," *IEEE Transactions on Knowledge and Data Engineering*, vol. 3, no. 1, pp. 100-107, March 1991.

j6 A. Kavianpour and N. Bagherzadeh, "Application of three-valued logic for distributed termination detection," *International Journal of Computers and Electrical Engineering*, vol. 17, no. 2, pp. 65-74, 1991.

j7 A. Kavianpour and N. Bagherzadeh, "Finding circular shapes in an image on a pyramid architecture," *Pattern Recognition Letters,* vol. 13, no. 12, pp. 843-848, December 1992.

j8 N. Bagherzadeh and K. Hawk, "Parallel implementation of the auction algorithm on the Intel hypercube," *Journal of Computer and Software Engineering*, vol. 1, no. 1, pp. 17-32, 1993.

j9 A. Abnous, C. Christensen, J. Gray, J. Lenell, A. Naylor, and N. Bagherzadeh, "Design and implementation of the 'Tiny RISC' microprocessor," *Journal of Microprocessors and Microsystems,* vol. 16, no. 4, pp.187-193, 1992.

j10 A. Abnous and N. Bagherzadeh, "Pipelining and bypassing in a VLIW processor," *IEEE Transactions on Parallel and Distributed Systems*, vol. 5, no. 6, pp. 658-664, June 1994.

j11 A. Kavianpour and N. Bagherzadeh, "A systematic approach for mapping application tasks in hypercubes," *IEEE Transactions on Computers*, vol. 42, no. 6, pp. 742-746, June 1993.

j12 A. Kavianpour and N. Bagherzadeh, "Parallel algorithms for line detection on a pyramid architecture," *International Journal of Pattern Recognition and Artificial Intelligence*, Vol. 8, no.1, pp. 337-349, 1994.

j13 C. Bowen and N. Bagherzadeh, "Image processing applications in C++ on a hypercube multicomputer," *International Journal of Computers and Electrical Engineering*, vol. 19, no. 5, pp. 351-364,1993.

j14 A. Kavianpour, S. Shoari, and N. Bagherzadeh, "A new approach for circle detection on multiprocessors," *Journal of Parallel and Distributed Computing*, vol. 20, no. 2, pp. 256-260, February 1994.

j15 S. Latifi and N. Bagherzadeh, "Incomplete star: An incrementally scalable network based on the star graph," *IEEE Transactions on Parallel and Distributed Systems*, vol. 5, no. 1, pp. 97-102, January 1994.

j16 N. Bagherzadeh, N. Nassif, and S. Latifi, "A routing and broadcasting scheme on faulty star graphs," *IEEE Transactions on Computers*, Vol 42, no. 11, pp 1398-1403, November 1993.

j17 J. Gray, A. Naylor, A. Abnous, and N. Bagherzadeh, "VIPER: a VLIW integer microprocessor," *IEEE Journal of Solid States and Circuits*, Vol. 28, no. 12, pp 1377-1383, December 1993.

j18 J. Lenell and N. Bagherzadeh, "A performance comparison of several superscalar processor models with a VLIW processor," *Journal of Microprocessors and Microsystems*, Vol 18, no. 3, pp 232-242, 1994.

j19 A. Kavianpour, N. Bagherzadeh, and S. Shoari, “Finding elliptical shapes in an image using a pyramid architecture, ” *International Journal of Computers and Electrical Engineering*, vol. 21, no. 1, pp. 69-75, Jan 1995.

j20 S. Latifi, M. M. de Azevedo, and N. Bagherzadeh, “A star-based I/O-bounded network for massively parallel systems,” *IEE Proceedings-Computers and Digital Techniques*, Vol. 142, No. 1, January 1995.

j21 M. M. de Azevedo, N. Bagherzadeh, and S. Latifi, "Broadcasting algorithms for the star-connected cycles interconnection network," *Journal of Parallel and Distributed Computing*, 25, 209-222 (1995).

j22 S. Wallace and N. Bagherzadeh, "Performance issues of a superscalar microprocessor," *Microprocessors and Microsystems*, Vol. 19, No. 4, pp 187-199 (1995).

j23 A. Abnous and N. Bagherzadeh, "Architectural design and analysis of a VLIW processor," *International Journal of Computers and Electrical Engineering*, Vol 21, No. 2, pp 119-142 (1995).

j24 T. Kato and N. Bagherzadeh, "A novel superscalar architecture using scheduling patterns and performance analysis," *The Transactions of the Institute of Electronics, Information, and Communication Engineers D-I*, Vol.J78-D-I, No. 9, pp 809-819 (1995).

j25 N. Bagherzadeh and M. Dowd, "Computation in faulty stars," *IEEE Transactions on Reliability*, Vol 44, No. 1, pp 114-119 (1995).

j26 N. Bagherzadeh, M. Dowd, and S. Latifi, "A well-behaved enumeration of star graphs," *IEEE Transactions on Parallel and Distributed Systems*, Vol 6, No. 5, pp 531-535, May (1995).

j27 M. M. de Azevedo, N. Bagherzadeh, M. Dowd, and S. Latifi, "Some topological properties of star connected cycles," *Information Processing Letters*, 58, pp 81-85 (1996).

j28 N. Bagherzadeh, M. Dowd, and N. Nassif, "Embedding an arbitrary binary tree into the star graph," *IEEE Transactions on Computers*, Vol 45, No. 4, pp 475-481 (1996).

j29 N. Bagherzadeh and M. Dowd, "Problems on routing bounded distance assignments in hypercubes," *Computer Systems-Science and Engineering*, Vol 11, No. 4, pp 221-226, July (1996).

j30 S. Latifi and N. Bagherzadeh, "On cluster-star graph and its properties," *Computer Systems-Science and Engineering*, Vol 11, No. 3, pp 145-149, May (1996).

j31 S. Shoari and N. Bagherzadeh, "Computation of the fast fourier transform on the star-connected cycle networks," *International Journal of Computers and Electrical Engineering*, Vol 22, No. 4, pp 235-246 (1996).

j32 N. Nassif and N. Bagherzadeh, "A grid embedding into the star graph for image analysis solutions," *Information Processing Letters*, Vol. 60, No. 5, pp 255-260 (1996).

j33 S. Latifi, N. Bagherzadeh, and R. Gajjala, "Fault-tolerant embedding of linear arrays and rings in the star graph," *International Journal of Computers and Electrical Engineering*, Vol 23, No. 2, pp 95-107 (1997).

j34 S. Latifi and N. Bagherzadeh, "On embedding rings into a star-related network," *Information Sciences*, Vol. 99, No. 1-2, pp 21-35 (1997)

j35 S. Shoari, N. Bagherzadeh, T. Milner, and J. S. Nelson, "Moment algorithms for blood vessel detection in infrared images of laser-heated skin," *International Journal of Computers and Electrical Engineering,* Vol 23, No. 5, January (1998).

j36 M. M. de Azevedo, N. Bagherzadeh, M. Dowd, and S. Latifi, "Average distance and routing algorithms in the star-connected cycles interconnection network," *International Journal of Science and Technology-Special Issue of Computer in Scientia Iranica,* Vol. 3, No. 4, (1997).

j37 N. Bagherzadeh, M. Dowd, and S. Latifi, "Faster Column Operations in Star Networks," *Telecommunication Systems,* Vol. 10, Nos. 1, 2 (1998).

j38 M. M. de Azevedo, N. Bagherzadeh, and S. Latifi, "Low expansion packings and embeddings of hypercubes into star graphs: a performance-oriented approach," *IEEE Transactions on Parallel and Distributed Systems,* Vol. 9, No. 3, (1998).

j39 S. Shoari, N. Bagherzadeh, D. Goodman, T.E. Milner, D. J. Smithies, and J.S. Nelson, "A parallel algorithm for pulsed laser infrared tomography," *Pattern Recognition Letters,* 19 (1998).

j40 S. Wallace and N. Bagherzadeh, "A scalable register file architecture for superscalar processors," *Microprocessors and Microsystems,* Vol. 22, No. 1, (1998).

j41 S. Wallace and N. Bagherzadeh, "Modeled and measured instruction fetching performance for superscalar microprocessors," *IEEE Transactions on Parallel and Distributed Systems,* Vol. 9, No. 6, (1998).

j42 N. Nassif and N. Bagherzadeh, "Image component labeling on the star graph using divide and conquer," *IEE Proceedings-Computers and Digital Techniques,* Vol. 145, No. 1, (1998).

j43 M. Lee, G. Lu, H. Singh, N. Bagherzadeh, F. Kurdahi, E. Filho, and V. Castro Alves, "MorphoSys A Reconfigurable Computing Chip," *IEEE Circuits and Systems Newsletter,* Vol. 10, No 1, March/April 1999.

j44 M. Lee, H. Singh, G. Lu, N. Bagherzadeh, F. Kurdahi, E. Filho, and V. Castro Alves, "Design and Implementation of the MorphoSys Reconfigurable Computing

Processor," *Journal of Signal Processing Systems for Signal, Image, and Video technology,* Vol. 24, No. 2/3, pp. 147-164, March 2000.

j45 H. Singh, M. Lee, G. Lu, F. Kurdahi, N. Bagherzadeh, and E. Filho, "MorphoSys: An Integrated Reconfigurable System for Data-Parallel and Computation-Intensive Applications," *IEEE Transactions on Computers,* Vol. 49, No. 5, pp. 465-481 (2000).

j46 R. Maestre, F. Kurdahi, M. Fernandez, R. Hermida, N. Bagherzadeh, and H. Singh, "Kernel scheduling techniques for efficient solution of space exploration in reconfigurable computing," *EUROMICRO Journal of Systems Architecture on Modern Methods and Tools in Digital System Design*, 2000.

j47 R. Maestre, F. Kurdahi, M. Fernandez, R. Hermida, N. Bagherzadeh, and H. Singh, "A Formal Approach to Context Scheduling for Multi-context Reconfigurable Architectures," *IEEE Transactions on VLSI Design-Special Issue on Reconfigurable Computing*, Vol. 9, Issue 1, pp. 173-185, Feb 2001.

j48 R. Maestre, F. Kurdahi, M. Fernandez, R. Hermida, N. Bagherzadeh, and H. Singh, "A Framework for Reconfigurable Computing: Task Scheduling and Context Management," *IEEE Transactions on VLSI Design-Special Issue on System Level Design*, Vol. 9, Issue 6, pp. 858-873, Dec 2001 (Best Paper Award).

j49 P. Chou, J. Liu, D. Li, and N. Bagherzadeh, "IMPACCT: Methodology and Tools for Power-Aware Embedded Systems," *Kluwer Design Automation of Embedded Systems*, pp. 205-232, October 2002.

j50 J. Liu, P. Chou, and N. Bagherzadeh, "Power-Aware Task Motion for Enhancing Dynamic Range of Embedded Systems with Renewable Energy Sources in Proceedings of the Workshop on Power Aware Computer Systems," in *Lecture Notes in Computer Science* (LNCS), Springer-Verlag, pp. 84--99. 2002.

j51 R. Maestre, F. Kurdahi, M. Fernandez, R. Hermida, N. Bagherzadeh, and H. Singh, "A Framework for Reconfigurable Computing: Task Scheduling and Context Management-a Summary," *Circuits and Systems Magazine*, IEEE, Vol. 2, Issue 4, pp. 48-51, 2002.

j52 M. Sanchez-Elez, H. Du, N. Tabrizi, Y. Lung, N. Bagherzadeh, and M. Fernandez, "Algorithm Optimizations and Mapping Scheme for Interactive Ray Tracing on a Reconfigurable Architecture," *Computers & Graphics*, 2003

j53 G. Venkataramani, W. Najjar, F. Kurdahi, N. Bagherzadeh, W. Bohm and J. Hammes, "Automatic Compilation to a Coarse-grained Reconfigurable System-on-Chip," *ACM Trans. on Embedded Computing Systems*, November 2003.

j54 B. Gorjiara, N. Bagherzadeh, and P. Chou, "Ultra-fast and Efficient Algorithm for Energy Optimization by Gradient-based Stochastic Voltage and Task Scheduling,"

ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 12 , Issue 4 (September 2007)

j55 J. Bahn, S. Lee, and N. Bagherzadeh, "Design of a Router for Network-on-Chip," *International Journal of High Performance Systems Architecture,* 2007 - Vol. 1, No.2 pp. 98 - 105

j56 A. Niktash, H. Parizi, and N. Bagherzadeh, "A Reconfigurable Processor for Forward Error Correction," *ARCS 2007,* LNCS 4415, pp. 1-13, 2007

j57 J. Bahn and N. Bagherzadeh, "Design of Simulation and Analytical Models for a 2D-meshed Asymmetric Adaptive Router," *Computers & Digital Techniques, IET,* Volume 2, Issue 1, January 2008 Page(s):63 - 73

j58 F. Rivera, M. Sanchez-Elez, R. Hermida, and N. Bagherzadeh, "Scheduling methodology for conditional execution of kernels onto multicontext reconfigurable architectures," *Computers & Digital Techniques, IET,* Volume 2, Issue 3, May 2008 Page(s):199 - 213

j59 J. Bahn, S. Lee, Y. Yang, J. Yang, and N. Bagherzadeh, "On Design and Application Mapping of a Network-on-Chip (NoC) Architecture," *Parallel Processing Letters (PPL),* Volume: 18, Issue: 2 (June 2008), pp. 239 - 255

j60 N. Tabrizi and N. Bagherzadeh, "An ASIC Design and Formal Analysis of a Novel Pipelined and Parallel Sorting Accelerator," *Integration, The VLSI Journal,* Volume 41, Issue 1 (January 2008), Pages 65-75

j61 S. Lee, J. Bahn, Y. Yang, and N. Bagherzadeh, "A Generic Network Interface architecture for a Networked Processor Array (NePA)," *ARCS 2008,* LNCS 4934, pp. 247–260, 2008

j62 J. Bahn, J. Yang, W. Hu, and N. Bagherzadeh, "Parallel FFT Algorithms on Network-on-Chips," *Journal of Circuits, Systems, and Computers* 18(2): 255-269, 2009.

j63 F. Bagci, F. Kluge, T. Ungerer, and N. Bagherzadeh, "Optimisations for LocSens - an Indoor Location Tracking System Using Wireless Sensors," *International Journal of Sensor Networks (IJSNET)*, Vol. 6, Nos. 3/4, 2009.

j64 J. Bahn and N. Bagherzadeh, "On-Chip Interconnection Network with an Efficient Parallel Buffer
Structure and Generic Traffic," *Scientia Iranica*, Computer Science & Engineering and Electrical Engineering. Vol. 16, No. 2, pp. 104-118, 2009.

j65 M. Sanchez-Elez, N. Bagherzadeh, and R. Hermida, "A Framework for Low Energy Data Management in Reconfigurable Multi-Context Architectures," *Journal of Systems Architecture*, 2009, Pages 127-139

j66 S. Lee and N. Bagherzadeh, "A Variable Frequency Link for a Power-Aware Network-on-Chip (NoC))," *INTEGRATION, the VLSI Journal,* 42 (2009) 479–485

j67 S. Lee and N. Bagherzadeh, "A High Level Power Model for Network-on-Chip (NoC) Router," *Computers and Electrical Engineering,* 35 (2009) 837–845

j68 Y. Yang, J. Bahn, S. Lee, J. Yang, and N. Bagherzadeh, "Parallel Processing for Block Ciphers on a Fault Tolerant Networked Processor Array," *International Journal of High Performance Systems Architecture,* Vol. 2, Nos. 3/4, 2010

j69 J. Yang, S. Lee, C. Chen, and N. Bagherzadeh, "Ray Tracing on a Networked Processor Array," *International Journal of Electronics*, 2010, 97(10):1193-1205

j70 F. Bagci, T. Ungerer, and N. Bagherzadeh, "Multi-level Security in Wireless Sensor Networks," *International Journal on Advances in Software*, Vol. 4, No. 6, 2010.

j71 C. Wang, W. Hu, S. Lee, and N. Bagherzadeh, "Area and Power-Efficient Innovative Congestion-Aware Network-on-Chip," *Journal of Systems Architecture*, Volume 57 Issue 1, Pages 24-38, January, 2011

j72 A. Hatanaka and N. Bagherzadeh, "A Scheduling Approach for Distributed Resource Architectures with Scarce Communication Resources," *Int. J. High Performance Systems Architecture,* Vol. 3, No. 1, Pages 12-22, 2011

j73 C. Wang and N. Bagherzadeh, "High-throughput Differentiated Service Provision Router Architecture for Wireless Network-on-Chip," *Int. J. High Performance Systems Architecture,* Vol. 4, No. 1, Pages 38-56, 2012

j74 F. Bolanos, J. Aedo, F. Rivera, and N. Bagherzadeh, "Mapping and Scheduling in Heterogeneous NoC through Population-Based Incremental Learning," *Journal of Universal Computer Science,* vol. 18, no. 7 (2012), 901-916

j75 W. Hu, C. Chen, J. Bahn, and N. Bagherzadeh, "Parallel Low-Density Parity Check Decoding on a Network-on-Chip-Based Multiprocessor Platform," *IET Computers & Digital Techniques*, Vol. 6, Issue. 2, pp. 86–94, 2012

j76 A. Hatanaka and N. Bagherzadeh, "A Software Pipelining Algorithm of Streaming Applications with Low Buffer Requirements," *Transactions D: Computer Science & Engineering and Electrical Engineering,* Vol. 19, No. 3, Pages 627-634, 2012

j77 H. Abdullah, H. A. Elsadek, H. E. ElDeeb, and N. Bagherzadeh, "Fractional Derivatives Based Scheme for FDTD Modeling of nth-Order Cole–Cole Dispersive Media," *IEEE Antennas and Wireless Propagation Letters,* Vol. 11, Pages 281-284, 2012

j78 A. Alhussien, C. Wang, and N. Bagherzadeh, "Design and Evaluation of a High Throughput Robust Router for Network-on-Chip," *IET Computers & Digital Technique,* Vol. 6, Issue. 3, pp. 173–179, 2012

j79 C. Wang, W. Hu, and N. Bagherzadeh, "A Load-Balanced Congestion-Aware Wireless Network-on-Chip Design for Multi-Core Platforms," *Microprocessors and Microsystems,* Vol. 36, Issue. 7, pp. 555-570, 2012

j80 S. Azampanah, A. Khademzadeh, N. Bagherzadeh, M. Janidarmian, and R. Shojaee "Contention-Aware Selection Strategy for Application-Specific Network-on-Chip," *IET Computers & Digital Technique,* Vol. 7, Issue. 3, pp. 105-114, 2013

j81 F. Bolanos, F. Rivera, J.E. Aedo, and N. Bagherzadeh, "From UML Specifications to Mapping and Scheduling of Tasks into a NoC, with Reliability Considerations," *Journal of Systems Architecture,* Vol. 59, Issue 7, pp. 429-440, 2013

j82 X. Wang, M. Yang, Y. Jiang, M. Palesi, P. Liu, T. Mak, and N. Bagherzadeh, "Efficient Multicast Schemes for 3-D Networks-on-Chip," *Journal of Systems Architecture,* Vol. 59, Issue 9, pp. 693-708, 2013

j83 A. Alhussien, F. Verbeek, B. van Gastel, N. Bagherzadeh, and J. Schmaltz, "Fully Reliable Dynamic Routing Logic for a Fault-Tolerant NoC Architecture," *Journal of Integrated Circuits and Systems,* Vol. 8, Issue. 1, pp. 43-53, 2013

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Professional Associations and Achievements

- Fellow Member, Institute of Electrical and Electronics Engineers (IEEE)
- Member, IEEE Computer Society

Extramural Funding (over 8 million dollars)

- (with Dan Gajski, Lubomir Bic, and Kane Kim), 32 node Intel hypercube, *Information and Computer Science and Engineering (CISE) Research Instrumentation - NSF*, $187,274, 1990. This equipment is shared with other co-principles to study parallelism.

- (with Jack Sklansky), "Multiprocessor Architecture for Image Processing," $26,700. A MICRO Research Proposal with Rockwell International, 1990-91.

- (with Alex Nicolau), "Design of a RISC Based Multiprocessor for a Fine-Grain Optimizing Compiler," $33,900. A MICRO Research Proposal with Northrop Corporation, 1990-91.

- (with Dan Gajski), "Design of a RISC Cluster VLSI Chip," $120,000. A Western Digital Fellowship in VLSI Systems Engineering; support for two students for two years at $30,000 per fellow per year (this amount includes a stipend of $18,000, tuition and fees, $3,000 for their project, and the remainder for the use of the Electrical and Computer Engineering Department)

- (with Kevin Tsai and Jack Sklansky), "A Hypermesh Architecture for Image Multiprocessing," $20,000. A MICRO Research Proposal with Rockwell International, 1990-1991.

- ARMY faculty fellowship, $10,000, 1990.

- From Sony Corporation for support of advanced computer architecture design, $30,000, Tokyo, Japan, 1990.

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- From NKK Corporation for support of advanced computer architecture design, $129,000, Tokyo, Japan, 1991-92.

- "A Quantitative Performance Comparison of a VLIW and Superscalar Architectures," $30,000, a MICRO Research Proposal with Unitec, 1992-93.

- From Asahi Chemical for support of advanced computer architecture design, $40,000, 1993-94.

- (with Douglas Blough), Intel MICRO project for iPSC/860 list price ($265,000) plus cash donation from the state ($15,000), 1994.

- "Software techniques for improving the efficiency of superscalar microprocessors," ($25,000 from Unitech Research Inc), ($11,247 from UC MICRO), 1995.

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- (with Fadi Kurdahi), "Dynamically reprogrammable architecture: a new approach to adaptive computing," $1,182,000 DARPA, 1997-2000.

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- (with Fadi Kurdahi), "Using low power reconfigurable computing for high-speed and wireless network appliances," $200,000, CoRe (with Broadcom), 2000-2002

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- (with Chou), "Mission Aware Power Management," $680, 000, DARPA PACC Phase II, 2002-2004

- "Design and Implementation of Automatic Parallel Detection Layer,", $24,000, NSF-INT (Egypt), 2001-2003

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- "Development of FDTD Accelerator for 3D Mutual Interaction Between Human Body and Radiation From Wireless Devices," $28,500, NSF, 2005-2008

- "Autonomic and Organic Real-time SoC Design," €5,000, Bavaria California Technology Center (BaCaTec), 2004-2006

- "Task Management on a Reconfigurable Architecture," €10,200, Uuniversidad Complutense, Madrid**,** 2006-2007

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