UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TCL ELECTRONICS HOLDINGS LTD. And TCL INDUSTRIES HOLDINGS CO., LTD.,
Petitioner,

v.

INTELLECTUAL VENTURES I LLC,
Patent Owner.

Case IPR2024-01245

U.S. PATENT NO. 7,089,443

DECLARATION OF SYLVIA D. HALL-ELLIS, PH.D.

I. INTRODUCTION

1. My name is Sylvia D. Hall-Ellis. I have been retained as an expert by Counsel for TCL Electronics Holdings Ltd. and TCL Industries Holdings Co. (referred to herein as "TCL").

2. I have written this declaration at the request of TCL to provide my expert opinion regarding the authenticity and public availability of several publications. My declaration sets forth my opinions in detail and provides the basis for my opinions regarding the public availability of these publications.

3. I reserve the right to supplement or amend my opinions, and basis for them, in response any additional evidence, testimony, discovery, argument, and/or other additional information that may be provided to me after the date of this declaration.

4. I am being compensated for my time spent working on this matter at my normal consulting rate of $400 per hour, plus reimbursement for any additional reasonable expenses. My compensation is not in any way tied to the content of this declaration, the substance of my opinions, or the outcome of this proceeding. I have no other interests in this proceeding or with any of the parties.

5. All of the materials that I considered are discussed explicitly in this declaration.

II. QUALIFICATIONS

6. I am currently an Adjunct Professor in the School of Information at San José State University. I obtained a Master of Library Science from the University of North Texas in 1972 and a Ph.D. in Library and Information Science from the University of Pittsburgh in 1985. Over the last fifty years, I have held various positions in the field of library and information resources. I was first employed as a librarian in 1966 and have been involved in the field of library sciences since, holding numerous positions.

7. I am a member of the American Library Association ("ALA") and its Association for Library Collections & Technical Services ("ALCTS") Division, and I served on the Committee on Cataloging: Resource and Description (which wrote the new cataloging rules) and as the chair of the Committee for Education and Training of Catalogers and the Competencies and Education for a Career in Cataloging Interest Group. I also served as the Chair of the ALCTS Division's Task Force on Competencies and Education for a Career in Cataloging. Additionally, I served as the Chair for the ALA Office of Diversity's Committee on Diversity, as a member of the REFORMA National Board of Directors, and as a member of the Editorial Board for the ALCTS premier cataloging journal, *Library Resources and Technical Services,* as a Co-Chair of the Membership Committee for the Library Research Round Table (LRRT) of the American Library

Association, and as a member of the LRRT Nominating Committee. Currently I serve as a member of the CORE Margaret Mann Citation Committee.

8. I have also given over one-hundred presentations in the field, including several on library cataloging systems and Machine-Readable Cataloging ("MARC") standards. My current research interests include library cataloging systems, metadata, and organization of electronic resources.

9. I have been deposed thirty-five times: (1) *Symantec Corp. vs. Finjan*, *Inc.,* Petition for *Inter Partes Review* of U.S. Patent No. 7,613,926, May 26, 2016, on behalf of Symantec Corp.; (2) *Symantec Corp. vs. Finjan*, *Inc.,* Northern District of California, 14-cv-299-HSG, on behalf of Symantec Corp., September 14, 2017; (3) one deposition for ten matters: *Intellectual Ventures I LLC vs. AT&T Mobility LLC*; AT&T Mobility II LLC, New Cingular Wireless Services, Inc., SBC Internet Services, Inc., Wayport, Inc., and Cricket Wireless LLC, C.A. No. 12-193 (LPS); *Intellectual Ventures II LLC vs. AT&T Mobility LLC*; AT&T Mobility II LLC, New Cingular Wireless Services, Inc., SBC Internet Services, Inc., Wayport, Inc., and Cricket Wireless LLC, C.A. No. 13-1631 (LPS); *Intellectual Ventures I LLC vs. T-Mobile USA, Inc. and T-Mobile US, Inc.,* C.A. No. 13-1632 (LPS); *Intellectual Ventures II LLC vs. T-Mobile USA, Inc. and T-Mobile US, Inc.,* C.A. No. 13-1633 (LPS); *Intellectual Ventures I LLC, vs. Nextel Operations, Inc., Sprint Spectrum L.P., Boost Mobile, LLC and Virgin Mobile USA, L.P.,* C.A. No. 13-1634

(LPS); *Intellectual Ventures II LLC vs. Nextel Operations, Inc., Sprint Spectrum L.P., Boost Mobile, LLC and Virgin Mobile USA, L.P.,* C.A. No. 13-1635 (LPS); *Intellectual Ventures I LLC, vs. United States Cellular Corporation*, C.A. No. 13-1636 (LPS); *Intellectual Ventures I LLC vs. United States Cellular Corporation*, C.A. No. 13-1637 (LPS); *Intellectual Ventures II LLC vs. AT&T Mobility LLC*, *AT&T Mobility II LLC, New Cingular Wireless Services, Inc.,* C.A. No. 15-799 (LPS); *Intellectual Ventures I LLC vs. T-Mobile USA, Inc. and T-Mobile US, Inc.,* C.A. No. 15-800 (LPS), on behalf of AT&T Mobility LLC; AT&T Mobility II LLC, Boost Mobile, LLC Cricket Wireless LLC, Nextel Operations, Inc., New Cingular Wireless Services, Inc., SBC Internet Services, Inc., Sprint Spectrum L.P., T-Mobile USA, Inc., T-Mobile US, Inc., United States Cellular Corporation Virgin Mobile USA, L.P., and Wayport, Inc., November 15, 2016; (4) *Hitachi Maxell, LTD., v. Top Victory Electronics (Taiwan) Co. Ltd., et al.,* Eastern District of Texas, 2:14-cv-1121 JRG-RSP (E.D. Texas), on behalf of Top Victory Electronics (Taiwan) Co. LTD, *et. al.,* January 20, 2016; (5) *Sprint Spectrum, L.P. vs. General Access Solutions, Ltd*., Petition for *Inter Partes Review* of U.S. Patent No. 7,173,916, on behalf of Sprint Spectrum L.P., July 13, 2018; (6) *Nichia Corporation vs. Vizio, Inc*., Central District of California, 8:16-cv-00545; on behalf of Vizio, Inc., October 12, 2018; (7) *Intellectual Ventures I LLC, vs. T-Mobile USA, Inc., T-Mobile US, Inc., Ericsson Inc., and Telefonaktiebolaget LM Ericsson*,

Middle District of Florida, 2:17-cv-00557 (JRG), on behalf of T-Mobile USA, Inc., T-Mobile US, Inc., Ericsson Inc., and Telefonaktiebolaget LM Ericsson, October 19, 2018; (8) Pfizer, Inc. vs. Biogen, Inc., Petition for *Inter Partes Review* of U.S. Patent No. 8,821,873, on behalf of Pfizer, November 3, 2018; (9) *Finjan, Inc. vs. ESET, LLC and ESET SPOL. S.R.O.,* Southern District of California, 3:17-cv-00183-CAB-BGS, on behalf of ESET, January 15, 2019; (10) *Finjan, Inc. vs. Cisco Systems, Inc.,* Northern District of California, 5:17-cv-00072-BLF-SVK, on behalf of Cisco Systems, Inc., September 6, 2019; (11) *Facebook, Inc., Instagram, LLC and Whatsapp Inc. vs. Blackberry Limited*, Petition for *Inter Partes Review* of U.S. Patent No. 9,349,120 B2, on behalf of Facebook, Inc., Instagram, LLC and Whatsapp Inc. December 20, 2019; (12) *3Shape A/S and Shape Inc. v. Align Technology, Inc.,* Petition for *Inter Partes Review* of U.S. Patent No. 7,156,661, IPR2020-00222 and IPR2020-00223, August 10, 2020, on behalf of 3Shape A/S and 3Shape Inc.; (13) *Finjan Inc. v. Rapid7, Inc. and Rapid7 LLC*, District of Delaware, 1:18-cv-01519-MN, September 15, 2020; (14) *VLSI Technology LLC v. Intel Corporation*, Western District of Texas, 6:19-cv-00254, 6:19-cv-00255, 6:19-cv-00256, on behalf of Intel Corporation, September 23, 2020; (15) *Finjan Inc. v. Sonicwall, Inc.,* Northern District of California, 5:17-cv-04467-BLF-HRL, on behalf of Sonicwall, Inc., October 27, 2020; (16) *VLSI Technology, LLC v. Intel Corporation*, District of Delaware, 1:18-cv-00966-CFC-CJB, February 5, 2021, on

behalf of the Intel Corporation; (17) *Unified Patents, LLC v. Good Kaisha IP Bridge 1*, Petition for *Inter Partes Review* of U. S. Patent 7,817,868, February 11, 2021, on behalf of Unified Patents; (18) *Finjan, Inc. v. Qualsys, Inc.,* Northern District of California, 4:18-cv-07229-YGR, March 1, 2021, on behalf of Qualsys, Inc.; (19) *Qualcomm, Inc. v. Monterey Research LLC*, Petition for *Inter Partes Review* of U. S. Patent 6,534,805, May 6, 2021, on behalf of Qualcomm, Inc.; (20) *Hulu, LLC v. Sound View Innovations, LLC*, Petition for *Inter Partes Review* of U. S. Patent 5,806,062, May 14, 2021, on behalf of Hulu, LLC; (21) *VLSI Technology LLC v. Intel Corporation*, Western District of Texas, 6:19-cv-00254, 6:19-cv-00255 and 6:19-cv-00256, August 3, 2021, on behalf of Intel Corporation; (22) *Liquidia Technologies, Inc. v. United Therapeutics Corporation*, Petition for *Inter Partes Review* of U. S. Patent 10,716,793 B2, October 20, 2021, on behalf of Liquidia Technologies, Inc.; (23) *EcoFactor, Inc. v. Google, Inc.,* Western District of Texas, 6:20-cv-00075 (ADA), 6:20-0078-ADA, and 6:20-cv-00080 ADA, October 27, 2021, on behalf of Google, Inc.; (24) *Liquidia Technologies, Inc. v. United Therapeutics Corporation*, Petition for *Inter Partes Review* of U. S. Patent 10,716,793 B2, March 11, 2022, on behalf of Liquidia Technologies, Inc.; (25) *Juniper Networks, Inc. v. Swarm Technology LLC*, Petition for *Inter Partes Review* of U. S. Patent 9,852,004, May 5, 2022, on behalf of Juniper Networks, Inc.; (26) *ParkerVision, Inc. v. Intel Corporation*, Western District of Texas, 6:20-cv-108

(ADA), October 26, 2022, on behalf of the Intel Corporation; (27) *CommScope v. TQ Delta*, Petition for *Inter Partes Review* of U. S. Patents 9,094,348 and 10,833,809, February 16, 2023, on behalf of CommScope; (28) *WSOU Investments d/b/a Brazos v. Salesforce.com, Inc.* for Western District of Texas, 6:20-cv-01164-ADA and 6:20-cv-01170-ADA, April 18, 2023, on behalf of Salesforce; (29) *Regents of the University of Minnesota v. AT&T Mobility LLC*, District of Minnesota, 14:cv-4999-JRT-TNL & 14-cv-4669-JRT-TNL, May 18, 2023, on behalf of AT & T Mobility LLC; (30) *VLSI Technology LLC v. Intel Corporation*, Northern District of California, 5:17-cv-0571-BLF-NC, July 11, 2023, on behalf of Intel Corporation; (31) *Trustees of Purdue University v. ST Microelectronics*, Western District of Texas, 6:21-cv-00727-ADA, July 27, 2023, on behalf of ST Microelectronics; (32) *Advanced Micro Devices, Inc. v. Realtek Semiconductor Corp.,* Petition for *Inter Partes Review* of U. S. Patents 7,936,245 & 9,590,582, August 10, 2023, on behalf of Advanced Micro Devices, Inc.; (33) Motif Foodworks, Inc. v. Impossible Foods, Inc., Petition for *Inter Partes Review* of U. S. Patent 9,943,096, August 24, 2023, on behalf of Motif Foodworks, Inc.; (34) *Network System Technologies, LLC v. Texas Instruments, Inc.*, Eastern District of Texas, 2:22-cv-00482-RWS, March 20, 2024, on behalf of Texas Instruments, Inc.; and, (35) *Pardalis Technology Licensing, LLC v. International Business Machines, Corporation*, Eastern District of Texas, 2:22-cv-00452, May 23, 2024, on behalf of

International Business Machines, Corporation. I have testified at trial three times: (1) *Advanced Micro Devices, Inc. v. Realtek Semiconductor Corp.,* U. S. Patents 7,936,245 & 9,590,582, October 20, 2023, International Trade Commission, Washington, DC, on behalf of Advanced Micro Devices, Inc.; (2) *Trustees of Purdue University v. ST Microelectronics*, Western District of Texas, 6:21-cv-00727-ADA, November 29, 2023, on behalf of ST Microelectronics; and, (3) *Certain Power Converter Modules and Computing Systems Containing the Same*, Investigation ITC-337-TA-1370, International Trade Commission, May 1, 2024, on behalf of Delta Electronics, Inc.

10. My full *curriculum vitae* is submitted herewith as Exhibit G.

III. PRELIMINARIES

11. *Scope of this declaration.* I am not an attorney and will not offer opinions on the law. I am, however, rendering my expert opinion on the authenticity of the documents referenced herein and on when and how each of these documents was disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art, exercising reasonable diligence, could have located the documents before January 23, 2003.

12. I am informed by counsel that an item is considered authentic if there is sufficient evidence to support a finding that the item is what it is claimed to be. I am also informed that authenticity can be established based on the contents of the

documents themselves, such as the appearance, contents, substance, internal patterns, or other distinctive characteristics of the item, taken together with all of the circumstances. I am further informed that an item is considered authentic if it is at least 20 years old, in a condition that creates no suspicion of its authenticity, and in a place where, if authentic, it would likely be. Lastly, I have been informed that a document's authenticity can be established by comparison with an authentic specimen.

13. I am informed by counsel that a printed publication qualifies as publicly accessible as of the date it was disseminated or otherwise made available such that a person interested in and ordinarily skilled in the relevant subject matter could locate it through the exercise of ordinary diligence.

14. While I understand that the determination of public accessibility under the foregoing standard rests on a case-by-case analysis of the facts particular to an individual publication, I also understand that a printed publication is rendered "publicly accessible" if it is cataloged and indexed by a library such that a person interested in the relevant subject matter could locate it (*i.e.*, I understand that cataloging and indexing by a library is sufficient, though there are other ways that a printed publication may qualify as publicly accessible). One manner of sufficient indexing is indexing according to subject matter category. I understand that the cataloging and indexing by a single library of a single instance of a particular

printed publication is sufficient, even if the single library is in a foreign country. I understand that, even if access to a library is restricted, a printed publication that has been cataloged and indexed therein is publicly accessible so long as a presumption is raised that the portion of the public concerned with the relevant subject matter would know of the printed publication. I also understand that the cataloging and indexing of information that would guide a person interested in the relevant subject matter to the printed publication, such as the cataloging and indexing of an abstract for the printed publication, is sufficient to render the printed publication publicly accessible.

15. I understand that routine business practices, such as general library cataloging and indexing practices, can be used to establish an approximate date on which a printed publication became publicly accessible.

A. Persons of Ordinary Skill in the Art

16. I am told by counsel that the subject matter of this proceeding relates generally to globally asynchronous locally synchronous processor systems.

17. I have been informed by counsel that a "person of ordinary skill in the art at the time of the inventions" is a hypothetical person who is presumed to be familiar with the relevant field and its literature at the time of the inventions. This hypothetical person is also a person of ordinary creativity, capable of understanding the scientific principles applicable to the pertinent field.

18. I am told by counsel that persons of ordinary skill in this subject matter or art would have had at least a Master of Science degree from an accredited program in electrical engineering, computer engineering, or the equivalent and at least two years' experience with computing systems, processor technology, or a related field. Additional education could substitute for professional experience, and vice versa.

19. It is my opinion that such a person would have been engaged in research, learning through study, and practice in the field and possibly through formal instruction the bibliographic resources relevant to his or her research. By not later than the late 1990s (and more specifically, 1998), such a person would have had access to a vast array of long-established print resources in the field, as well as to a rich set of online resources providing indexing information, abstracts, and full text services for publications relevant to the field of this dispute.

B. Authoritative Databases

20. In preparing this declaration, I used authoritative databases, such as the OCLC WorldCat, the Library of Congress Online Catalog, and the U. S. Copyright Office database, to confirm citation details of the publication discussed.

21. *OCLC WorldCat Database.* The OCLC was created "to establish, maintain and operate a computerized library network and to promote the evolution of library use, of libraries themselves, and of librarianship, and to provide

processes and products for the benefit of library users and libraries, including such objectives as increasing availability of library resources to individual library patrons and reducing the rate of rise of library per-unit costs, all for the fundamental public purpose of furthering ease of access to and use of the ever-expanding body of worldwide scientific, literary and educational knowledge and information."[1] Among other services, OCLC and its members are responsible for maintaining the WorldCat database,[2] used by independent and institutional libraries throughout the world.

22. *U. S. Copyright Office.* Created by Congress in 1897, the Copyright Office is responsible for administering a complex and dynamic set of laws, which include registration, the recordation of title and licenses, a number of statutory licensing provisions, and other aspects of the *1976 Copyright Act* and the *1998 Digital Millennium Copyright Act*. The public catalog in the Copyright Office includes information filed since 1978.[3] Individuals can search by title, personal or corporate name, key word, registration number, and document number. Works filed before 1978 can be located through the Copyright Public Records Reading

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[1] Third Article, Amended Articles of Incorporation of OCLC Online Computer Library Center, Incorporated (available at https://www.oclc.org/content/dam/oclc/membership/articles-of-incorporation.pdf)

[2] http://www.worldcat.org/

[3] https://cocatalog.loc.gov/cgi-bin/Pwebrecon.cgi?DB=local&PAGE=First

Room.[4] A researcher can find the date on which an item was published and deposited for copyright.

C. Indexing

23. A researcher may discover material relevant to his or her topic in a variety of ways. One common means of discovery is to search for relevant information in an index of periodical and other publications. Having found relevant material, the researcher will then normally obtain it online, look for it in libraries, or purchase it from a publisher, a bookstore, a document delivery service, or other provider. Sometimes, the date of a document's public accessibility will involve both indexing and library date information. However, date information for indexing entries is often unavailable. This is especially true for online indices.

24. Indexing services use a wide variety of controlled vocabularies to provide subject access and other means of discovering the content of documents. The formats in which these access terms are presented vary from service to service.

25. Before the widespread development of online databases to index articles in journals, magazines, conference papers, and technical declarations, libraries purchased printed volumes of indices. Graduate library school education mandated that students learn about the bibliographic control of disciplines, the prominent indexing volumes, and searching strategies required to use them

[4] https://www.copyright.gov/circs/circ23.pdf

effectively and efficiently. Half of the courses that I studied in library school were focused on bibliography and resources in academic disciplines.

26. Librarians consulted with information seekers to verify citations, check availability in union catalogs, printed books catalogs, and the OCLC database, and make formal requests for materials, *e.g.*, books, conference proceedings, journal articles. Requests were transmitted using Telex machines, rudimentary email systems, and the United States Postal Service. During my career, I have performed and supervised staff who handled these resource sharing tasks.

27. A major firm known for the breadth of subjects and comprehensive treatment in the preparation of index volumes, the H. W. Wilson Company offered these reference resources since the firm was founded in 1898. The *Reader's Guide to Periodical Literature* is one of the best-known titles available from H. W. Wilson. Each volume includes a comprehensive index for 300 of the most popular and important periodicals published in the United States and Canada. Information seekers have subject access expressed in plain language terminology, author access, and cross references to find the desired results from their searches. The family of index titles included *Science & Technology Index*, *Business Periodicals*, *Applied Science & Technology Index, Humanities Index, Biological & Agricultural*

Index, and *Industrial Arts Index*. These printed indices have been superseded by digital database offerings available to information seekers through Ebsco.

28. Online indexing services commonly provide bibliographic information, abstracts, and full-text copies of the indexed publications, along with a list of the documents cited in the indexed publication. These services also often provide lists of publications that cite a given document. A citation of a document is evidence that the document was publicly available and in use no later than the publication date of the citing document.

IV. LIBRARY CATALOGING PRACTICES

A. MARC RECORDS AND THE ONLINE LIBRARY CATALOG

29. I am fully familiar with the library cataloging standard known as the MARC standard, which is an industry-wide standard method of storing and organizing library catalog information.[5] MARC was first developed in the 1960s by the Library of Congress. A MARC-compatible library is one that has a catalog consisting of individual MARC records for each of its items. Today, MARC is the primary communications protocol for the transfer and storage of bibliographic

[5] The full text of the standard is available from the Library of Congress at http://www.loc.gov/marc/bibliographic/.

metadata in libraries.[6]

30. MARC is a framework into which descriptive bibliographic data are transcribed to interact with the software in online library catalogs to provide access to books, journals, and other resources in the collection. The bibliographic data provide points of access and can be searched by a person of ordinary skill in the art ("POSITA") to identify and obtain resources in the library collection. An information seeker (or POSITA) can search a local online library catalog or the holdings of a group of libraries in a state or region or in the global catalog WorldCat.

31. MARC records are not designed for public viewing. Although a significant number of libraries provide access to the MARC version of a bibliographic record, the public display is designed to show information in a succinct manner that is quickly understood and useful to the information seeker.

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[6] Almost every major library in the world is MARC-compatible. *See, e.g.*, *MARC Frequently Asked Questions (FAQ)*, Library of Congress, https://www.loc.gov/marc/faq.html (last visited June 13, 2024) ("MARC is the acronym for MAchine-Readable Cataloging. It defines a data format that emerged from a Library of Congress-led initiative that began nearly forty years ago. It provides the mechanism by which computers exchange, use, and interpret bibliographic information, and its data elements make up the foundation of most library catalogs used today."). MARC is the ANSI/NISO Z39.2-1994 (reaffirmed 2016) standard for Information Interchange Format.

Libraries determine the default search for the online catalog to make the entry of search terms efficient and result in a successful search. Information seekers can enter a keyword, title, author, or standard number for the item. Libraries may also provide a search capability called "Summon" that allows the information seeker to enter known information about the item to conduct a search.

32. Since at least the early 1970s and continuing to the present day, MARC has been the primary communications protocol for the transfer and storage of bibliographic metadata in libraries.[7] As explained by the Library of Congress:

> You could devise your own method of organizing the bibliographic information, but you would be isolating your library, limiting its options, and creating much more work for yourself. Using the MARC standard prevents duplication of work and allows libraries to better share bibliographic resources. Choosing to use MARC enables libraries to acquire cataloging data that is predictable and reliable. If a library were to develop a "home-grown" system that did not use MARC records, it would not be taking advantage of an industry-wide standard whose primary purpose is to foster communication of information.

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[7] A complete history of the development of MARC can be found in *MARC: Its History and Implications* by Henrietta D. Avram (Washington, DC: Library of Congress, 1975) and available online from the Hathi Trust (https://babel.hathitrust.org/cgi/pt?id=mdp.39015034388556;view=1up;seq=1; last visited June 13, 2024).

> Using the MARC standard also enables libraries to make use of commercially available library automation systems to manage library operations. Many systems are available for libraries of all sizes and are designed to work with the MARC format. Systems are maintained and improved by the vendor so that libraries can benefit from the latest advances in computer technology. The MARC standard also allows libraries to replace one system with another with the assurance that their data will still be compatible.

Why Is a MARC Record Necessary? LIBRARY OF CONGRESS, http://www.loc.gov/marc/umb/um01to06.html#part2 (last visited June 13, 2024).

33. Examining the MARC records for a specific item reveals the comprehensive data transcribed about a particular item at the time that cataloging and classification occurred. In addition to the creator, title, subjects, and standard numbers, additional information may provide additional and relevant data depending on the type of resource. Understanding the full extent of bibliographic data for an item and the points of access associated with it provides essential information that can be used to determine the indexing and public availability for documents described in this Declaration.

B. MARC RECORDS

34. A MARC record comprises several fields, each of which contains specific data about the work. Each field is identified by a standardized, unique, three-digit code corresponding to the type of data that follow. For example, a

work's title is recorded in field 245, the primary author or creator of the work is recorded in field 100, an item's International Standard Book Number ("ISBN") is recorded in field 020, an item's International Standard Serial Number ("ISSN") is recorded in field 022, an item's Library of Congress call number is recorded in field 050, and the publication date is recorded in field 260 under the subfield "c." *Id.*[8] If a work is a periodical, then its publication frequency is recorded in field 310, alternate publication frequency is recorded in field 321, and the publication dates (*e.g.*, the first and last publication) are recorded in field 362, which is also referred to as the enumeration/chronology field. *See* http://www.loc.gov/marc/bibliographic/bd3xx.html (last visited June 13, 2024).

35. The library that created the record is recorded in Field 040 in subfield "a" with a unique library code. When viewing the MARC record online via Online Computer Library Center's ("OCLC") bibliographic database, hovering over this code with the mouse reveals the full name of the library. I used this method of "mousing over" the library codes in the OCLC database to identify the originating

[8] In some MARC records, field 264 is used rather than field 260 to record publication information. *See* http://www.loc.gov/marc/bibliographic/bd264.html (last visited June 13, 2024) ("Information in field 264 is similar to information in field 260 (Publication, Distribution, etc. (Imprint)). Field 264 is useful for cases where the content standard or institutional policies make a distinction between functions").

library for the MARC records discussed in this Declaration. Where this "mouse over" option was not available, I consulted the Directory of OCLC Libraries to identify the institution that created the MARC record.[9]

36. MARC records also include several fields that include subject matter classification information. An overview of MARC record fields is available through the Library of Congress at http://www.loc.gov/marc/bibliographic/. For example, 6XX fields are termed "Subject Access Fields." *See* http://www.loc.gov/marc/bibliographic/bd6xx.html. Among these, for example, is the 650 field; this is the "Subject Added Entry – Topical Term" field. *See* http://www.loc.gov/marc/bibliographic/bd650.html. The 650 field is a "[s]ubject added entry in which the entry element is a topical term." *Id.* These authenticated subject entries "are assigned to a bibliographic record to provide access according to generally accepted thesaurus-building rules (*e.g.*, *Library of Congress Subject Headings* (LCSH), *Medical Subject Headings* (MeSH))." *Id.*

37. Further, MARC records include call numbers, which themselves indicate a subject and physical location within the library collections. For example, the 050 field is the "Library of Congress Call Number." *See* http://www.loc.gov/marc/bibliographic/bd050.html (last visited April 20, 2024). A defined portion of the Library of Congress Call Number is the classification

[9] https://www.oclc.org/en/contacts/libraries.html

number, and "source of the classification number is *Library of Congress Classification* and the *LC Classification-Additions and Changes*." *Id.* Thus, included in the 050 field is a subject matter classification. Each item in a library has a single classification number. A library selects a classification scheme (*e.g.*, the Library of Congress Classification scheme just described or a similar scheme such as the Dewey Decimal Classification scheme or the National Library of Medicine Classification scheme) and uses it consistently. When the Library of Congress assigns the classification number, it appears as part of the 050 field. If a local library assigns the classification number, it appears in a 090 field. In either scenario, the MARC record includes a classification number that represents a subject matter classification.

38. Each item in a library has a single classification number. A library selects a classification scheme (*e.g.*, the Library of Congress Classification scheme just described or a similar scheme such as the Dewey Decimal Classification scheme) and uses it consistently. When the Library of Congress assigns the classification number, it appears as part of the 050 field, as discussed above. For MARC records created by libraries other than the Library of Congress (*e.g.*, a university library or a local public library), the classification number may appear in a 09X (*e.g.*, 090) field. *See* http://www.loc.gov/marc/bibliographic/bd09x.html (last visited June 13, 2024).

C. OCLC

39. The OCLC was created "to establish, maintain and operate a computerized library network and to promote the evolution of library use, of libraries themselves, and of librarianship, and to provide processes and products for the benefit of library users and libraries, including such objectives as increasing availability of library resources to individual library patrons and reducing the rate of rise of library per-unit costs, all for the fundamental public purpose of furthering ease of access to and use of the ever-expanding body of worldwide scientific, literary and educational knowledge and information."[10] Among other services, OCLC and its members are responsible for maintaining the WorldCat database (http://www.worldcat.org/), used by independent and institutional libraries throughout the world.

40. OCLC also provides its members online access to MARC records through its OCLC bibliographic database. When an OCLC member institution acquires a work, it creates a MARC record for this work in its computer catalog system in the ordinary course of its business. MARC records created at the Library of Congress were initially tape-loaded into the OCLC database through a

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[10] Third Article, Amended Articles of Incorporation of OCLC Online Computer Library Center, Incorporated (available at https://www.oclc.org/content/dam/oclc/membership/articles-of-incorporation.pdf).

subscription to MARC Distribution Services daily or weekly. Once the MARC record is created by a cataloger at an OCLC member institution or is tape-loaded from the Library of Congress, the MARC record is then made available to any other OCLC members online, and therefore made available to the public. Accordingly, once the MARC record is created by a cataloger at an OCLC member institution or is tape-loaded from the Library of Congress or another library anywhere in the world, any publication corresponding to the MARC record has been cataloged and indexed according to its subject matter such that a person interested in that subject matter could, with reasonable diligence, locate and access the publication through any library with access to the OCLC bibliographic database or through the Library of Congress.

41. When an OCLC member institution creates a new MARC record, OCLC automatically supplies the date of creation for that record. The date of creation for the MARC record appears in the fixed field (008), characters 00 through 05. The MARC record creation date reflects the date on which the item was first acquired or cataloged. Initially, field 005 of the MARC record is automatically populated with the date the MARC record was created in year, month, day format (YYYYMMDD) (some of the newer library catalog systems also include hour, minute, second (HHMMSS)). Thereafter, the library's computer system may automatically update the date in field 005 every time the library

updates the MARC record (*e.g.*, to reflect that an item has been moved to a different shelving location within the library). Field 005 is visible when viewing a MARC record via an appropriate computerized interface. The initial field 005 date (*i.e.*, the date the MARC record was created) does appear. The date upon which the most recent update to field 005 occurred also appears in field 005. Thus, when an item's MARC record has been printed to hardcopy—as is the case with the exhibits to this declaration—the date reflected next to field 008 is necessarily on or after the date the library first cataloged and indexed the underlying item.

42. Once one library has cataloged and indexed a publication by creating a MARC record for that publication, other libraries that receive the publication do not create additional MARC records—the other libraries instead rely on the original MARC record. They may update or revise the MARC record to ensure accuracy, but they do not replace or duplicate it. This practice does more than save libraries from duplicating labor, it also enhances the accuracy of MARC records. It also allows librarians around the world to know that a particular MARC record is authoritative. In contrast, a hypothetical system wherein duplicative records were created would result in confusion as to which record is authoritative.

43. The date of creation of the MARC record by a cataloger at an OCLC member institution reflects when the underlying item is accessible to the public. Upwards of two-thirds to three-quarters of book sales to libraries come from a

jobber or wholesaler for online and print resources. These resellers make it their business to provide books to their customers as fast as possible, often providing turnaround times of only a single day after publication. Libraries purchase a significant portion of the balance of their books directly from publishers themselves, which provide delivery on a similarly expedited schedule. In general, libraries make these purchases throughout the year as the books are published and shelve the books as soon thereafter as possible in order to make the books available to their patrons. Thus, books are generally available at libraries across the country within just a few days of publication.

V. PUBLICATIONS

A. Iyer, Anoop, and Diana Marculescu. "Power Efficiency of Voltage Scaling in Multiple Clock, Multiple Voltage Cores." *IEEE/ACM International Conference on Computer Aided Design, 2002* (pp. 379-386). ICCAD 2002. Piscataway, NJ: IEEE; New York: ACM, c2002. ("Iyer") [Exhibit A]

44. Attached hereto as Exhibit A is a copy of a conference paper published in the volume titled *IEEE/ACM International Conference on Computer Aided Design, 2002* found in the Linda Hall Library of Science, Engineering & Technology (Kansas City, Missouri). The conference paper titled "Power Efficiency of Voltage Scaling in Multiple Clock, Multiple Voltage Cores" by Anoop Iyer and Diana Marculescu (hereafter "Iyer") appears beginning on page 379. The IEEE/ACM International Conference on Computer Aided Design, 2002

was held on November 10-14, 2002, in San José, California. The Iyer conference paper was presented as part of Session 5D, Low Power and Transistor Level Optimization (Exhibit A, page 10). Exhibit A is a true and correct copy of the Iyer conference paper (pages 379-386). I obtained this copy of the conference paper from the Linda Hall Library of Science, Engineering & Technology. Specifically, the text of the Iyer conference paper is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Exhibit A was found within the custody of a library – a place where, if authentic, a copy of this conference proceedings volume would likely be. Exhibit A is a true and correct copy in a condition that creates no suspicion about authenticity.

45. The Iyer conference paper is also available in the *IEEE Xplore* database[11] and the *ACM Digital Library*.[12] The *IEEE Xplore* entry indicates that the Iyer conference paper was posted on January 29, 2003; the *ACM Digital Library* entry indicates that the Iyer conference paper was posted on November 10, 2002.

46. Attached hereto as Attachment 1A is a true and correct copy of the MARC record for this conference proceedings volume from the Linda Hall Library

[11] https://ieeexplore.ieee.org/document/1167562

[12] https://dl.acm.org/doi/10.1145/774572.774629

of Science, Engineering & Technology online catalog. Library ownership is indicated by the presence of the library's code ("LHL") in the 049 field. The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. I personally identified and retrieved the library catalog record which is Attachment 1A.

47. Based on finding a print copy of Exhibit A in the Linda Hall Library of Science, Engineering & Technology and MARC record in its online library catalog attached as Attachment 1A, it is my opinion that the book titled *IEEE/ACM International Conference on Computer Aided Design, 2002* was cataloged in the Linda Hall Library of Science, Engineering & Technology on November 26, 2002, as shown in field 008 ("021126"). The Iyer conference paper was publicly available at the Linda Hall Library of Science, Engineering & Technology as of November 26, 2002.

48. Attached hereto as Attachment 1B is a true and correct copy of the MARC record for the book titled *IEEE/ACM International Conference on Computer Aided Design, 2002* obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 1B. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 1B, that library code is "LHL," which means that the MARC record for this conference proceedings volume was cataloged at the

Linda Hall Library of Science, Engineering & Technology. As can be seen in the MARC record for this exhibit, a cataloger at the Linda Hall Library of Science, Engineering & Technology created OCLC record number 51071148 on November 26, 2002, as shown in field 008 ("021126"). The library community continues to update this MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on October 23, 2023, as shown in field 005 ("20231023").

49. Attachment 1B further includes an entry in field 050 ("TK7874 $b .I1557 2002")—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system) and an entry in field 082 ("621.395 $b I221 2002")—as described above, a subject matter classification number consistent with the Dewey Decimal classification system. Attachment 1B also shows that Exhibit A was catalogued with four descriptor terms reading "Electronic circuit design $x Data processing $v Congresses" (see Attachment 1C, Library of Congress subject heading sh2008102924), "Computer-aided design $v Congresses" (see Attachment 1D, Library of Congress subject heading sh2008101464), "Electronic circuits $x Testing $v Congresses" (see Attachment 1E, Library of Congress subject heading sh85042282 and Attachment 1F, Library of Congress subject heading sh85031115), and "Integrated circuits $x Design and construction $x Data

processing $v Congresses" (see Attachment 1G, Library of Congress subject heading sh85067119 and Attachment 1F, Library of Congress subject heading sh85031115) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 1B was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650 entries. Further, as of November 26, 2002, the MARC record attached hereto as Attachment 1B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that acquired the conference proceedings volume, which means that the corresponding publication was publicly available on or before that same date through any library with access to the OCLC bibliographic database or through an individual library.

50. Further supporting my opinion that Exhibit A was publicly accessible to ordinarily skilled and interested researchers in the field is the fact that the book titled *IEEE/ACM International Conference on Computer Aided Design, 2002* was registered with the U. S. Copyright Office as item TX0005639057 on December 4, 2002, and indicated a publication date of November 10, 2002 (see Attachment 1H, U. S. Copyright Office Public Catalog). As noted above, this would have provided a POSITA with keyword searching capabilities and other tools to locate this book.

51. WorldCat indicates that the book titled *IEEE/ACM International*

Conference on Computer Aided Design, 2002 as cataloged at the Linda Hall Library of Science, Engineering & Technology is currently available from 54 libraries.[13] In view of the above, the print version of the book titled *IEEE/ACM International Conference on Computer Aided Design, 2002* was publicly available on November 26, 2002, because by that date it had been received, cataloged, and indexed in the Linda Hall Library of Science, Engineering & Technology and made part of the OCLC bibliographic database. For these reasons, it is my opinion that Exhibit A was published and publicly accessible on November 26, 2002.

B. Liljeberg, Pasi K., Juha P. Plosila, and Jouni A. Isoaho. "Asynchronous Interface for Locally Clocked Modules in ULSI Systems." *ISCAS 2001: the 2001 IEEE International Symposium on Circuits and Systems Conference Proceedings* (vol. 4, pp. 170-173). 5 vols. Piscataway, NJ: IEEE, 2001. ("Liljeberg") [Exhibit B]

52. Attached hereto as Exhibit B is a copy of a conference paper published in the five-volume set titled *ISCAS 2001: the 2001 IEEE International Symposium on Circuits and Systems Conference Proceedings* found in the Linda Hall Library of Science, Engineering & Technology (Kansas City, Missouri). The conference paper titled "Asynchronous Interface for Locally Clocked Modules in ULSI System" by Pasi K. Liljeberg, Juha P. Plosila, and Jouni A. Isoaho (hereafter "Liljeberg") appears beginning on page 170 in volume 4. The 2001 IEEE International Symposium on Circuits and Systems Conference Proceedings was

[13] https://search.worldcat.org/title/51071148

held on May 6-9, 2001, in Sydney, New South Wales, Australia. The Liljeberg conference paper was presented as part of the Digital VLSI Circuits section of the VLSI Systems and Applications Track (Exhibit B, page 8). Exhibit B is a true and correct copy of the Liljeberg conference paper (volume 4, pages 170-173). I obtained this copy of the conference paper from the Linda Hall Library of Science, Engineering & Technology. Specifically, the text of the Lilijeberg conference paper is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Exhibit B was found within the custody of a library – a place where, if authentic, a copy of this conference proceedings five-volume set would likely be. Exhibit B is a true and correct copy in a condition that creates no suspicion about authenticity.

53. The Liljeberg conference paper is also available in the *IEEE Xplore* database[14] and the digital repository *ResearchGate*.[15] The *IEEE Xplore* entry indicates that the Liljeberg conference paper was posted on August 7, 2002.

54. Attached hereto as Attachment 2A is a true and correct copy of the

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[14] https://ieeexplore.ieee.org/document/922199

[15] https://www.researchgate.net/publication/3896141_Asynchronous_interface_for_locally_clocked_modules_in_ULSI_systems

MARC record for this conference proceedings five-volume set from the Linda Hall Library of Science, Engineering & Technology online catalog. Library ownership is indicated by the presence of the library's code ("LHL") in the 049 field. The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. I personally identified and retrieved the library catalog record which is Attachment 2A.

55. Based on finding a print copy of Exhibit B in the Linda Hall Library of Science, Engineering & Technology and MARC record in its online library catalog attached as Attachment 2A, it is my opinion that the five-volume set titled *ISCAS 2001: the 2001 IEEE International Symposium on Circuits and Systems Conference Proceedings* was cataloged in the Linda Hall Library of Science, Engineering & Technology on May 1, 2001, as shown by the date in the gutter ("5-1-01") on page 5 of Exhibit B. The Liljeberg conference paper was publicly available at the Linda Hall Library of Science, Engineering & Technology as of May 1, 2001.

56. Attached hereto as Attachment 2B is a true and correct copy of the MARC record for the five-volume set titled *ISCAS 2001: the 2001 IEEE International Symposium on Circuits and Systems Conference Proceedings* obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 2B. As previously noted, the library

that created the record is recorded in field 040 with a unique library code. For Attachment 2B, that library code is "NSA," which means that the MARC record for this conference proceedings five-volume set was cataloged at the National Security Agency Library (Fort George G. Meade, Maryland). As can be seen in the MARC record for this exhibit, a cataloger at the National Security Agency Library created OCLC record number 46823428 on April 26, 2001, as shown in field 008 ("010426"). The library community continues to update this MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on January 5, 2023, as shown in field 005 ("20230105").

57. Attachment 2B further includes an entry in field 050 ("TK7801 $b .I245 2001")—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system). Attachment 2B also shows that Exhibit B was catalogued with five descriptor terms reading "Electronics $v Congresses" (see Attachment 2C, Library of Congress subject heading sh2008102883), "Signal processing $x Digital techniques $v Congresses" (see Attachment 2D, Library of Congress subject heading sh2008111654), "Electronic circuits $v Congresses" (see Attachment 2E, Library of Congress subject heading sh2008102920), "Neural networks (Computer science) $v Congresses" (see Attachment 2F, Library of Congress subject heading sh2008108385), and "Integrated circuits $x Very large

scale integration $v Congresses" (see Attachment 2G, Library of Congress subject heading sh2008104263) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 2B was indexed according to its subject matter by virtue of at least two independently sufficient classifications: the field 050 entry and the field 650 entries. Further, as of April 26, 2001, the MARC record attached hereto as Attachment 2B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that acquired the conference proceedings volume, which means that the corresponding publication was publicly available on or before that same date through any library with access to the OCLC bibliographic database or through an individual library.

58. Further supporting my opinion that Exhibit B was publicly accessible to ordinarily skilled and interested researchers in the field is the fact that the five-volume set titled *ISCAS 2001: the 2001 IEEE International Symposium on Circuits and Systems Conference Proceedings* was registered with the U. S. Copyright Office as item TX0005387058 on May 25, 2001, and indicated a publication date of May 6, 2001 (see Attachment 2H, U. S. Copyright Office Public Catalog). As noted above, this would have provided a POSITA with keyword searching capabilities and other tools to locate this book.

59. WorldCat indicates that the five-volume set titled *ISCAS 2001: the*

2001 IEEE International Symposium on Circuits and Systems Conference Proceedings as cataloged at the National Security Agency Library is currently available from 300 libraries.[16] In view of the above, the print version of the five-volume set titled *ISCAS 2001: the 2001 IEEE International Symposium on Circuits and Systems Conference Proceedings* was publicly available on May 6, 2001, because by that date it had been cataloged and indexed in the National Security Agency Library, made part of the OCLC bibliographic database, and received in the Linda Hall Library of Science, Engineering Technology. For these reasons, it is my opinion that Exhibit B was published and publicly accessible on May 6, 2001.

C. Moore, Simon, George Taylor, Robert Mullins, and Peter Robinson. "Point to Point GALS Interconnect." *ASYNC 2002: Eighth International Symposium on Asynchronous Circuits and Systems Proceedings* (pp. 69-75). Piscataway, NJ: IEEE, 2002. ("Moore 2002") [Exhibit C]

60. Attached hereto as Exhibit C is a copy of a conference paper published in the volume titled *ASYNC 2002: Eighth International Symposium on Asynchronous Circuits and Systems Proceedings* found in the Linda Hall Library of Science, Engineering & Technology (Kansas City, Missouri). The conference paper titled "Point to Point GALS Interconnect" by Simon Moore, George Taylor, Robert Mullins, and Peter Robinson (hereafter "Moore 2002") appears beginning

[16] https://search.worldcat.org/title/46823428

on page 69. The Eighth International Symposium on Asynchronous Circuits and Systems was held on April 8-11, 2002, in Manchester, England. The Moore conference paper was presented as part of Paper Session 3, Mixed Synchronous/Asynchronous Communication and Design (Exhibit C, page 5). Exhibit C is a true and correct copy of the Moore 2002 conference paper (pages 69-75). I obtained this copy of the conference paper from the Linda Hall Library of Science, Engineering & Technology. Specifically, the text of the Moore conference paper is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Exhibit C was found within the custody of a library – a place where, if authentic, a copy of this conference proceedings volume would likely be. Exhibit C is a true and correct copy in a condition that creates no suspicion about authenticity.

61. The Moore 2002 conference paper is also available in the *IEEE Xplore* database.[17] The *IEEE Xplore* entry indicates that the Moore 2002 conference paper was posted on August 7, 2002.

62. Attached hereto as Attachment 3A is a true and correct copy of the MARC record for this conference proceedings volume from the Linda Hall Library of Science, Engineering & Technology online catalog. Library ownership is

[17] https://ieeexplore.ieee.org/document/1000297?arnumber=1000297

indicated by the presence of the library's code ("LHL") in the 049 field. The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. I personally identified and retrieved the library catalog record which is Attachment 3A.

63. Based on finding a print copy of Exhibit C in the Linda Hall Library of Science, Engineering & Technology and MARC record in its online library catalog attached as Attachment 3A, it is my opinion that the book titled *ASYNC 2002: Eighth International Symposium on Asynchronous Circuits and Systems Proceedings* was cataloged in the Linda Hall Library of Science, Engineering & Technology on April 17, 2002, as shown in field 008 ("020417"). The Moore 2002 conference paper was publicly available at the Linda Hall Library of Science, Engineering & Technology as of April 17, 2002.

64. Attached hereto as Attachment 3B is a true and correct copy of the MARC record for the book titled *ASYNC 2002: Eighth International Symposium on Asynchronous Circuits and Systems Proceedings* obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 3B. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 3B, that library code is "LHL," which means that the MARC record for this conference proceedings volume was cataloged at the Linda Hall Library of Science,

Engineering & Technology. As can be seen in the MARC record for this exhibit, a cataloger at the Linda Hall Library of Science, Engineering & Technology created OCLC record number 4960090 on April 17, 2002, as shown in field 008 ("020417"). The library community continues to update this MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on October 31, 2023, as shown in field 005 ("20231031").

65. Attachment 3B further includes an entry in field 050 ("TK7868.A79 $b I57 2002")—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system). Attachment 3B also shows that Exhibit C was catalogued with three descriptor terms reading "Asynchronous circuits $v Congresses" (see Attachment 3C, Library of Congress subject heading sh93006345 and Attachment 1F, Library of Congress subject heading sh85031115), "Computers, Pipeline $v Congresses" (see Attachment 3D, Library of Congress subject heading sh85029569 and Attachment 1F, Library of Congress subject heading sh85031115), and "Embedded computer systems $v Congresses" and (see Attachment 3E, Library of Congress subject heading sh2008102939) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 3B was indexed according to its subject matter by virtue of at least two independently sufficient classifications: the field

050 entry and the field 650 entries. Further, as of April 17, 2002, the MARC record attached hereto as Attachment 3B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that acquired the conference proceedings volume, which means that the corresponding publication was publicly available on or before that same date through any library with access to the OCLC bibliographic database or through an individual library.

66. Further supporting my opinion that Exhibit C was publicly accessible to ordinarily skilled and interested researchers in the field is the fact that the book titled *ASYNC 2002: Eighth International Symposium on Asynchronous Circuits and Systems Proceedings* was registered with the U. S. Copyright Office as item TX0005519824 on May 3, 2002, and indicated a publication date of April 8, 2002 (see Attachment 3F, U. S. Copyright Office Public Catalog). As noted above, this would have provided a POSITA with keyword searching capabilities and other tools to locate this book.

67. WorldCat indicates that the book titled *ASYNC 2002: Eighth International Symposium on Asynchronous Circuits and Systems Proceedings* as cataloged at the Linda Hall Library of Science, Engineering & Technology is currently available from 298 libraries.[18] In view of the above, the print version of the book titled *ASYNC 2002: Eighth International Symposium on Asynchronous*

[18] https://search.worldcat.org/title/49600907

Circuits and Systems Proceedings was publicly available on April 17, 2002, because by that date it had been received, cataloged, and indexed in the Linda Hall Library of Science, Engineering & Technology and made part of the OCLC bibliographic database. For these reasons, it is my opinion that Exhibit C was published and publicly accessible on April 17, 2002.

D. Njølstad, Tormod, Odd Tjore, Kjetil Svarstad, Lars Lundheirn, Tor Ø. Vedal, Jukka Typpö, Tor Ramstad, Lars Wanhammar, Einar J. Aas, and Helge Danielsen. "A Socket Interface for GALS Using Locally Dynamic Voltage Scaling for Rate-Adaptive Energy Saving." ***14th Annual IEEE International ASIC/SOC Conference Proceedings*** **(pp. 110-116). Piscataway, NJ: IEEE, 2002. ("Njølstad") [Exhibit D]**

68. Attached hereto as Exhibit D is a copy of a conference paper published in the volume titled *14th Annual IEEE International ASIC/SOC Conference Proceedings* found in the Linda Hall Library of Science, Engineering & Technology (Kansas City, Missouri). The conference paper titled "A Socket Interface for GALS Using Locally Dynamic Voltage Scaling for Rate-Adaptive Energy Saving" by Tormod Njølstad, Odd Tjore, Kjetil Svarstad, Lars Lundheirn, Tor Ø. Vedal, Jukka Typpö, Tor Ramstad, Lars Wanhammar, Einar J. Aas, and Helge Danielsen (hereafter "Njølstad") appears beginning on page 110. The 14th Annual IEEE International ASIC/SOC Conference was held on September 12-15, 2001, in Arlington, Virginia. The Njølstad conference paper was presented as part of the T2 Session, Digital Design Methodologies (Exhibit D, page 8). Exhibit D is

a true and correct copy of the Njølstad conference paper (pages 110-116). I obtained this copy of the conference paper from the Linda Hall Library of Science, Engineering & Technology. Specifically, the text of the Njølstad conference paper is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Exhibit D was found within the custody of a library – a place where, if authentic, a copy of this conference proceedings volume would likely be. Exhibit D is a true and correct copy in a condition that creates no suspicion about authenticity.

69. The Njølstad conference paper is also available in the *IEEE Xplore* database.[19] The *IEEE Xplore* entry indicates that the Njølstad conference paper was posted on August 7, 2002.

70. Attached hereto as Attachment 4A is a true and correct copy of the MARC record for this conference proceedings volume from the Linda Hall Library of Science, Engineering & Technology online catalog. Library ownership is indicated by the presence of the library's code ("LHL") in the 049 field. The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. I personally identified and retrieved the library catalog record which is Attachment 4A.

[19] https://ieeexplore.ieee.org/document/954682

71. Based on finding a print copy of Exhibit D in the Linda Hall Library of Science, Engineering & Technology and MARC record in its online library catalog attached as Attachment 4A, it is my opinion that the book titled *14th Annual IEEE International ASIC/SOC Conference Proceedings* was cataloged in the Linda Hall Library of Science, Engineering & Technology on September 25, 2001, as shown in field 008 ("010925"). The Njølstad conference paper was publicly available at the Linda Hall Library of Science, Engineering & Technology as of September 25, 2001.

72. Attached hereto as Attachment 4B is a true and correct copy of the MARC record for the book titled *14th Annual IEEE International ASIC/SOC Conference Proceedings* obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 4B. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 4B, that library code is "LHL," which means that the MARC record for this conference proceedings volume was cataloged at the Linda Hall Library of Science, Engineering & Technology. As can be seen in the MARC record for this exhibit, a cataloger at the Linda Hall Library of Science, Engineering & Technology created OCLC record number 48022773 on September 25, 2001, as shown in field 008 ("010925"). The library community continues to update this MARC record to meet current cataloging rules. The most recent

enhancement to the MARC record occurred on February 10, 2024, as shown in field 005 ("20240210").

73. Attachment 4B further includes an entry in field 050 ("TK7874.6 $b I34 2001")—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system) and an entry in field 082 ("621.3950285")—as described above, a subject matter classification number consistent with the Dewey Decimal classification system. Attachment 4B also shows that Exhibit D was catalogued with a descriptor term reading "Application-specific integrated circuits $v Congresses" (see Attachment 4C, Library of Congress subject heading sh89004045 and Attachment 1F, Library of Congress subject heading sh85031115) in the 650 field. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 4B was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650 entry. Further, as of September 25, 2001, the MARC record attached hereto as Attachment 4B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that acquired the conference proceedings volume, which means that the corresponding publication was publicly available on or before that same date through any library with access to the OCLC bibliographic

database or through an individual library.

74. Further supporting my opinion that Exhibit D was publicly accessible to ordinarily skilled and interested researchers in the field is the fact that the book titled *14th Annual IEEE International ASIC/SOC Conference Proceedings* was registered with the U. S. Copyright Office as item TX0005539519 on February 28, 2002, and indicated a publication date of September 12, 2001 (see Attachment 4D, U. S. Copyright Office Public Catalog). As noted above, this would have provided a POSITA with keyword searching capabilities and other tools to locate this book.

75. WorldCat indicates that the book titled *14th Annual IEEE International ASIC/SOC Conference Proceedings* as cataloged at the Linda Hall Library of Science, Engineering & Technology is currently available from 49 libraries.[20] In view of the above, the print version of the book titled *14th Annual IEEE International ASIC/SOC Conference Proceedings* was publicly available on September 25, 2001, because by that date it had been received, cataloged, and indexed in the Linda Hall Library of Science, Engineering & Technology and made part of the OCLC bibliographic database. For these reasons, it is my opinion that Exhibit D was published and publicly accessible on September 25, 2001.

E. Hemani, A., T. Meincke, S. Kumar, A. Postula, T. Olsson, P. Nilsson, J. Oberg, P. Ellervee, and D. Lundqvist. "Lowering Power Consumption in Clock by Using Globally Asynchronous

[20] https://search.worldcat.org/title/48022773

Locally Synchronous Design Style." ***Proceedings 1999: Design Automation Conference 36th*** **(pp. 873-878). New York: Association for Computing Machinery, 1999. ("Hemani") [Exhibit E]**

76. Attached hereto as Exhibit E is a copy of a conference paper published in the volume titled *Proceedings 1999: Design Automation Conference 36th* found in the Kurt K. Wendt Engineering Library at the University of Wisconsin – Madison. The conference paper titled "Lowering Power Consumption in Clock by Using Globally Asynchronous Locally Synchronous Design Style" by A. Hemani, T. Meincke, S. Kumar, A. Postula, T. Olsson, P. Nilsson, J. Oberg, P. Ellervee, and D. Lundqvist (hereafter "Hemani") appears beginning on page 873. The 36th Design Automation Conference (DAC '99) was held on June 21-25, 1999, in New Orleans, Louisiana. The Hemani conference paper was presented as part of Session 48, Low Power System Design Techniques (Exhibit E, page 13). Exhibit E is a true and correct copy of the Hemani conference paper (pages 873-878). I obtained this copy of the conference paper from the Kurt K. Wendt Engineering Library at the University of Wisconsin – Madison. Specifically, the text of the Hemani conference paper is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Exhibit E was found within the custody of a library – a place where, if authentic, a copy of this conference proceedings volume would likely be. Exhibit E is a true and correct

copy in a condition that creates no suspicion about authenticity.

77. The Hemani conference paper is also available in the *IEEE Xplore* database,[21] the *ACM Digital Library*,[22] and the digital repository *ResearchGate*.[23] The *IEEE Xplore* entry indicates that the Hemani conference paper was posted on August 6, 2002. The *ACM Digital Library* entry indicates that the Hemani conference paper was posted on June 1, 1999.

78. Attached hereto as Attachment 5A is a true and correct copy of the MARC record for this conference proceedings volume from the Kurt K. Wendt Engineering Library at the University of Wisconsin – Madison online catalog. Library ownership is indicated by the presence of the library's code ("GZM") in the 049 field. The library continues to update this MARC record and enhanced the MARC record to meet current cataloging rules. I personally identified and retrieved the library catalog record which is Attachment 5A.

79. Based on finding a print copy of Exhibit E in the Kurt K. Wendt Engineering Library at the University of Wisconsin – Madison and MARC record

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[21] https://ieeexplore.ieee.org/document/782202

[22] https://dl.acm.org/doi/10.1145/309847.310091

[23] https://www.researchgate.net/publication/221059998_Lowering_Power_Consumption_in_Clock_by_Using_Globally_Asynchronous_Locally_Synchronous_Design_Style

in its online library catalog attached as Attachment 5A, it is my opinion that the MARC record for the book titled *Proceedings 1999: Design Automation Conference 36th* was created for the Kurt K. Wendt Engineering Library at the University of Wisconsin – Madison on September 17, 1999, as shown in field 008 ("990917"). The Hemani conference paper was publicly available in the Kurt K. Wendt Engineering Library at the University of Wisconsin – Madison as of September 17, 1999.

80. Attached hereto as Attachment 5B is a true and correct copy of the MARC record for the book titled *Proceedings 1999: Design Automation Conference 36th* obtained from the OCLC bibliographic database. I personally identified and retrieved the MARC record that is Attachment 5B. As previously noted, the library that created the record is recorded in field 040 with a unique library code. For Attachment 5B, that library code is "NAT," which means that the MARC record for this conference proceedings volume was cataloged at the NASA Langley Research Center Library (Stennis Space Center, Mississippi). As can be seen in the MARC record for this exhibit, a cataloger at the NASA Langley Research Center Library created OCLC record number 42345912 on September 10, 1999, as shown in field 008 ("990910"). The library community continues to update this MARC record to meet current cataloging rules. The most recent enhancement to the MARC record occurred on November 21, 2023, as shown in

field 005 (“20231121”).

81. Attachment 5B further includes an entry in field 050 (“TJ211 $b .D4 1999”)—as described above, a subject matter classification number consistent with the Library of Congress classification system (analogous to the Dewey Decimal classification system) and an entry in field 082 (“620.0042”)—as described above, a subject matter classification number consistent with the Dewey Decimal classification system. Attachment 5B also shows that Exhibit E was catalogued with three descriptor terms reading “Engineering design $x Data processing $v Congresses” (see Attachment 5C, Library of Congress subject heading sh2008103073), “Computer-aided design $v Congresses” (see Attachment 1D, Library of Congress subject heading sh2008101464), and “Computer graphics $v Congresses” (see Attachment 5D, Library of Congress subject heading sh2008100018) in the 650 fields. Thus, as of its cataloging, the publication corresponding to the MARC record attached hereto as Attachment 5B was indexed according to its subject matter by virtue of at least three independently sufficient classifications: the field 050 entry, the field 082 entry, and the field 650 entries. Further, as of September 10, 1999, the MARC record attached hereto as Attachment 5B was accessible through any library with access to the OCLC bibliographic database or the online catalog at a library that acquired the conference proceedings volume, which means that the corresponding publication

was publicly available on or before that same date through any library with access to the OCLC bibliographic database or through an individual library.

82. Further supporting my opinion that Exhibit E was publicly accessible to ordinarily skilled and interested researchers in the field is the fact that the book titled *Proceedings 1999: Design Automation Conference 36th* was registered with the U. S. Copyright Office as item TX0005031904 on August 24, 1999, and indicated a publication date of June 21, 1999 (see Attachment 5E, U. S. Copyright Office Public Catalog). As noted above, this would have provided a POSITA with keyword searching capabilities and other tools to locate this book.

83. WorldCat indicates that the book titled *Proceedings 1999: Design Automation Conference 36th* as cataloged at the NASA Langley Research Center Library is currently available from 328 libraries.[24] In view of the above, the print version of the book titled *Proceedings 1999: Design Automation Conference 36th* was publicly available on September 17, 1999, because by that date it had been received, cataloged, and indexed in the Kurt K. Wendt Engineering Library at the University of Wisconsin – Madison and made part of the OCLC bibliographic database. For these reasons, it is my opinion that Exhibit E was published and publicly accessible on September 17, 1999.

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[24] https://search.worldcat.org/title/42345912

F. Moore, Simon W., George Taylor, Bob Mullins, and Peter Robinson. *Channel Communication Between Independent Clock Domains.* Cambridge, England: University of Cambridge Computer Laboratory, 2001. ("Moore 2001") [Exhibit F]

84. Attached hereto as Exhibit F is a copy of a technical report titled *Channel Communication Between Independent Clock Domains* prepared by Simon W. Moore, George Taylor, Bob Mullins, and Peter Robinson of the Computer Laboratory at the University of Cambridge (Cambridge, England) (hereafter "Moore 2001"). Exhibit F is a true and correct copy, which I obtained from the digital repository *Academia.edu*.[25] Academics around the world use the digital repository *Academia.edu* to share their research and have uploaded more than 55 million papers that are read by more than 99 million academics, professionals, and students every month. The Moore 2001 technical report is also available through the digital repository *Semantic Schoolar*.[26] Specifically, the text of Exhibit F is complete; no pages are missing, and the text on each page appears to flow seamlessly from one page to the next; further, there are no visible alterations to the document. Exhibit F is a true and correct copy in a condition that creates no

---

25 https://www.academia.edu/26868125/Channel_Communication_Between_Independent_Clock_Domains?uc-g-sw=13639614

26 https://www.semanticscholar.org/paper/Channel-Communication-Between-Independent-Clock-Moore-Taylor/62d44f2a121ee5cda912aed827e1449783fb0cc7

suspicion about its authenticity.

85. Research at the Computer Laboratory at the University of Cambridge was supported by a grant funded by the Engineering and Physical Sciences Research Council (EPSRC) as noted on page 4 of Exhibit F (Attachment 6A).[27] The grant funding period was September 28, 1998, through June 27, 2002. The work was also supported by Cambridge Consultants, Limited and AT&T Labs Cambridge.

86. Further, lead author Moore cites the technical report titled *Channel Communication Between Independent Clock Domains* (Exhibit F) on his curriculum vitae (CV) as early as August 16, 2002 (Attachment 6B).[28] The technical report was identified as a workshop paper for the Fifth ACiD-WG Workshop, Nauchâtel (Switzerland) in 2001. *Google Scholar* indicates that four versions of the technical report are available (Attachment 6C).[29] Dr. Moore's current *Google Scholar* listing indicates that the technical report was presented at

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[27] https://gow.epsrc.ukri.org/NGBOViewGrant.aspx?GrantRef=GR/L86326/01

[28] https://web.archive.org/web/20020816081517/http://www.cl.cam.ac.uk/users/swm11/cv/index.html

[29] https://scholar.google.co.uk/scholar?oi=bibs&hl=en&cluster=11420818632738068007

the First ACiD-WG Workshop of the European Commission's Fifth Framework Programme (Attachment 6D).[30]

87. A technical report exhibits the following characteristics: the technical report is attributed to one or more creators or authors (in this case Simon W. Moore, George Taylor, Bob Mullins, and Peter Robinson) who affix a date of creation (in this case 2001), recognize one or more outside funding agencies (in this case the Engineering and Physical Sciences Research Council), a list of scholarly references (in this case 8 references), and publishes the document through a sponsoring institution or organization (in this case the Computer Laboratory at the University of Cambridge).

88. Based on finding a digital copy of Exhibit F on the Internet, it is my opinion that the technical report titled *Channel Communication Between Independent Clock Domains* was available to the public by August 16, 2002. It is also my opinion that there is no reason to doubt the authenticity of Exhibit F given its appearance, contents, and the web address from which it was obtained.

---

30 https://scholar.google.co.uk/citations?view_op=view_citation&hl=en&user=hPhDxHwAAAAJ&cstart=100&pagesize=100&citation_for_view=hPhDxHwAAAAJ:mVmsd5A6BfQC

VI. SUMMARY OF OPINIONS

89. In view of the foregoing, it is my opinion that the publications described above were publicly available no later than the corresponding date listed in the table below:

Exhibit	Publication	Publicly Available On or After
A	Iyer, Anoop, and Diana Marculescu. "Power Efficiency of Voltage Scaling in Multiple Clock, Multiple Voltage Cores." *IEEE/ACM International Conference on Computer Aided Design, 2002* (pp. 379-386). ICCAD 2002. Piscataway, NJ: IEEE; New York: ACM, c2002.	November 26, 2002
B	Liljeberg, Pasi K., Juha P. Plosila, and Jouni A. Isoaho. "Asynchronous Interface for Locally Clocked Modules in ULSI Systems." *ISCAS 2001: the 2001 IEEE International Symposium on Circuits and Systems Conference Proceedings* (vol. 4, pp. 170-173). 5 vols. Piscataway, NJ: IEEE, 2001.	May 6, 2001
C	Moore, Simon, George Taylor, Robert Mullins, and Peter Robinson. "Point to Point GALS Interconnect." *ASYNC 2002: Eighth International Symposium on Asynchronous Circuits and Systems Proceedings* (pp. 69-75). Piscataway, NJ: IEEE, 2002.	April 17, 2002
D	Njølstad, Tormod, Odd Tjore, Kjetil Svarstad, Lars Lundheirn, Tor Ø. Vedal, Jukka Typpö, Tor Ramstad, Lars Wanhammar, Einar J. Aas, and Helge Danielsen. "A Socket Interface for GALS Using Locally Dynamic Voltage Scaling for Rate-Adaptive Energy Saving." *14th Annual IEEE International ASIC/SOC Conference Proceedings* (pp. 110-116). Piscataway, NJ: IEEE, 2002.	September 25, 2001

Exhibit	Publication	Publicly Available On or After
E	Hemani, A., T. Meincke, S. Kumar, A. Postula, T. Olsson, P. Nilsson, J. Oberg, P. Ellervee, and D. Lundqvist. "Lowering Power Consumption in Clock by Using Globally Asynchronous Locally Synchronous Design Style." *Proceedings 1999: Design Automation Conference 36th* (pp. 873-878). New York: Association for Computing Machinery, 1999.	September 17, 1999
F	Moore, Simon W., George Taylor, Bob Mullins, and Peter Robinson. *Channel Communication Between Independent Clock Domains.* Cambridge, England: University of Cambridge Computer Laboratory, 2001.	August 16, 2002

90. In signing this Declaration, I recognize that the Declaration will be filed as evidence in a case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

91. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

/s/



July 30, 2024

Sylvia D. Hall-Ellis, Ph.D.

EXHIBIT A

IEEE/ACM INTERNATIONAL CONFERENCE
ON COMPUTER AIDED DESIGN

ICCAD-2002

A CONFERENCE FOR THE CAD PROFESSIONAL



November 10 - 14, 2002
DoubleTree Hotel
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FOREWORD

On behalf of the ICCAD 2002 Executive and Technical Program Committees, we would like to welcome you to the International Conference on Computer-Aided Design, November 10th through 14th at the DoubleTree Hotel in San Jose. In addition to the outstanding technical program that one expects every year from ICCAD, this year we will also review 20 years of past accomplishments and take new steps forward to begin the next 20 years of ICCAD.

To celebrate our anniversary, there will be a special dinner with host William H. Joyner, Jr., taking a lighthearted look at the past 20 years of ICCAD and the people who represented it. Attendees will also receive a copy of a special edition book: "The Best of ICCAD - 20 Years of Excellence in Computer-Aided Design", compiled by Andreas Kuehlmann. The papers in the book represent works that originated from the past two decades of ICCAD and were selected by a committee that included all of the former conference chairs and several international research leaders. The book includes commentaries on the historic impact and context of the various works.

This year, some of the conference activities begin on Sunday, November 10th, with a Workshop on Open Source and Open Standards. The workshop will include three parallel tracks covering: the OpenAccess effort, an open source circuit simulator, SystemC, SystemVerilog, OpenVera and ForSpec, and TestBuilder and Sugar. Following the workshop sessions the participants will all be invited to a panel "Open Source: EDA's Next Wave or Yesterday's Hype?", moderated by Larry Nagel. For the students on Sunday, ACM/SIGDA is sponsoring a CADathlon, a new programming contest that challenges students in their CAD knowledge, and their problem solving, programming, and teamwork skills. The competition is open to all graduate students who are currently enrolled full-time in a Ph.D. granting institution.

The ICCAD 2002 conference officially begins on Monday with the opening keynote by Chekib Akrout, Director, Microprocessor Development, IBM Corp., titled: "The Future of Electronic Games and the Impact on Design Automation." The technical program, organized by Andreas Kuehlmann and Hidetoshi Onodera, follows with 35 technical paper sessions comprised of 105 papers that were chosen from 381 submissions. We are particularly excited about two invited sessions that include 6 papers from international design experts that focus on emerging and low power design issues. Recognizing that the integrated circuit landscape has changed over the past twenty years, it is apparent that future design and EDA research must be done in tighter collaboration than ever before. These sessions represent ICCAD's first steps toward taking a leadership role in spawning more collaborative design and EDA research for the next 20 years. Our Monday evening panel moderated by John Cohn, "CAD for CAD's Sake? Are CAD and Design Diverging?" will further explore the increasing importance of CAD and design collaboration moving forward.

The technical program also includes five exciting embedded tutorials on MTCMOS, Nanotechnology, Challenges in Sub-wavelength Lithography, The A to Z of SOCs, and SAT and ATPG in Synthesis and Verification. The conference concludes on Thursday, November 14th with four new full-day tutorials: 1) High Performance Integrated Circuit Analysis and Design Including On-Chip Inductance, 2) FPGAs: Computer-Aided Design, Applications and Future Architectures, 3) Specification and Design of Multimillion Gate SOCs, and 4) Placement - the Key Problem in Physical Design.
we are certain that you will enjoy the conference and the festivities of our 20th anniversary celebration. We look forward to a great close of the first twenty years and an exciting kick-off for the next 20 years of ICCAD.



Larwrence T. Pileggi
General Chair



Andreas Kuehlmann
Technical Program Chair

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Power Efficiency of Voltage Scaling in Multiple Clock, Multiple Voltage Cores*

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Abstract

Due to increasing clock speeds, increasing design sizes and shrinking technologies, it is becoming more and more challenging to distribute a single global clock throughout a chip. In this paper we study the effect of using a Globally Asynchronous Locally Synchronous (GALS) organization for a superscalar, out-of-order processor, both in terms of power and performance. To this end, we propose a novel modeling and simulation environment for multiple clock cores with static or dynamically variable voltages for each synchronous block. Using this design exploration environment we were able to assess the power/performance tradeoffs available for Multiple Clock, Single Voltage (MCSV), as well as Multiple Clock, Dynamic Voltage (MCDV) cores. Our results show that MCSV processors are 10% more power efficient when compared to single-clock single voltage designs with a performance penalty of about 10%. By exploiting the flexibility of independent dynamic voltage scaling the various clock domains, the power efficiency of GALS designs can be improved by 12% on average, and up to 20% more in select cases. The power efficiency of MCDV cores becomes comparable with the one of Single Clock, Dynamic Voltage (SCDV) cores, while being up to 8% better in some cases. Our results show that MCDV cores consume 22% less power at an average 12% performance loss.

1 Introduction

Power consumption has become a critical issue in processor design, not only in embedded or portable environments, but also for high-end systems where performance has been the chief design constraint. Due to increased levels of complexity and integration, power density increases dramatically with shrinking device sizes and costly packaging and cooling techniques have to be employed to preserve the reliability and correct operation of core processors. Although performance is still the main selling factor in the high-end processor market, solutions that drastically reduce power requirements while still preserving the performance constraints are desirable. A large component of the power budget in high-end processors is the clock power consumption. Most conventional microprocessor designs are synchronous in their construction; that is, they have a global clock signal which provides a common timing reference for the operation of all the circuitry on the chip. On the other hand, fully asynchronous designs built using self-timed circuits do not have any global timing reference; examples of this design style are given in Sutherland's work on *Micropipelines* [1]. Globally Asynchronous Locally Synchronous systems (which we refer to as GALS systems in this paper) are an intermediate style of design between these two. GALS systems contain several independent synchronous blocks which operate with their own local clocks and communicate asynchronously with each other. The main feature of these systems is the absence of a global timing reference and the use of several distinct local clocks (or clock domains), possibly running at different frequencies.

In the microprocessor industry, global clock distribution issues are perhaps the best motivating factor for the study of GALS systems. With each technology shrink, the clock distribution network of a large chip grows rapidly in complexity and requires large design effort, power and die area. For instance in the Alpha 21264 processor, the global and major clock grids alone consume a third of its total power budget. Ronen *et al.* mention the worsening interconnect and clock distribution problem [2] and advocate global asynchrony as a possible solution. Since products in this arena have to have the highest performance at the lowest possible power cost, early design exploration tools for assessing the impact of asynchrony on both performance and power are needed.

In this paper, we describe the development of a *modeling* and *simulation* framework for GALS high end processors. Using this framework, we address the following issues:

- If we design a microprocessor in a GALS style with multiple clock domains (also called Multiple Clock, Single Voltage, or MCSV core), how much performance overhead will it incur over a fully synchronous machine?
- Will the elimination of the global clock network help in reducing the power requirements of the processor, as it has been claimed before?
- How can we exploit the extra flexibility offered by independent clock domains in a GALS processor and what is the impact of using a Multiple Clock Dynamic Voltage (MCDV) scheme on power/performance metrics?

Our analysis shows that GALS (MCSV) processors are not necessarily better in terms of *power consumption* than fully synchronous designs as it has been claimed before. Moreover, there is also a decrease in performance due to the asynchronous communication overhead and this can have adverse effects on overall energy consumption. The energy savings obtained by the elimination of the global clock are offset by the additional power consumed due to longer execution times. The use of dynamic voltage scaling in MCDV cores improves the situation for some applications by providing up to 20% additional power savings.

1.1 Related Work

Sutherland's paper on *Micropipelines* [1] contains the classic introduction to asynchronous design. The Amulet processor core developed at Manchester, which implements the ARM instruction set, is in its third generation and is commercially viable [3]. As Ronen *et al.* mention in

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[2], the worsening interconnect and clock distribution problem, as well as the burden of high clock power cost can be potentially solved by employing a global asynchronous design as a possible solution. GALS systems have been studied in detail by Chapiro in his 1984 thesis [4]. His work covers metastability issues in GALS systems and outlines a stretchable clocking strategy which provides a mechanism for asynchronous communication. Hemani *et al.* estimated in [5] the clock power savings in GALS designs compared to synchronous designs. However, their work targets a regular ASIC design flow with simpler clocking strategies rather than the aggressive clock distribution networks used in microprocessors.

Of great importance in GALS designs is the choice of the asynchronous communication mechanism between various synchronous blocks. Chelcea and Nowick propose in [6] the use of FIFOs as a low-latency asynchronous communication mechanism between synchronous blocks. Muttersbach *et al.* have implemented asynchronous wrappers around synchronous blocks [7]; they have used these wrappers along with asynchronous memory blocks to implement an ASIC and have thus proved the feasibility of GALS design in silicon. A similar system has been proposed by Moore *et al.* in [8]; pausible clocking for GALS systems has been described by Yun and Dooply in [9].

Dynamic voltage scaling (DVS) has been widely studied and implemented commercially. The use of multiple power grids and their implications in area overhead have been discussed in [10]. The difference in pipeline stage latencies has been explored for lowering the power requirements at system level, but for a specialized communication Myrinet GAM pipeline in a dynamic voltage scaling environment [11]. In [12], an example of adaptive dynamic voltage scaling in a system with self-timed circuits is presented. In that case, the traffic information in the communication buffers is used to adapt the supply voltage of various components. Finally, [13] presents a study of GALS processor systems and is the closest to our work. There, the authors use a communication scheme based on asynchronous FIFOs and stoppable clocks. The voltage assignment mechanism is an oracle-based scheme which finds the optimal voltages to be applied to different clock domains in a GALS processor.

The problem of power modeling at high levels of abstraction (system, software and microarchitectural level) has recently started to gain a lot of attention. Wattch [14] presents an advanced microarchitectural power simulator based on parameterized power models which are proven to be within 10% accurate when compared to three different high-end microprocessors. Wattch is based on SimpleScalar [15] which is a detailed, cycle-accurate simulator for superscalar, out-of-order cores. However, none of these simulators assume multiple clock domains or fine grain power management using dynamic adaptation of voltages and clock speeds.

1.2 Organization and Scope

The rest of this paper is organized as follows. Section 2 presents the motivation behind our proposed GALS architecture. In section 3, we describe some practical issues related to defining synchronous blocks, the proposed architecture and our scheme for dynamic clock management. The simulation and modeling environment is presented in section 4 while section 5 summarizes our experimental results. We conclude in section 6 with some final remarks.

2 Motivation

The idea of GALS system design is in itself quite old [4]. Interest in GALS design is now growing, mainly due to the global clock distribution problem. Trends of increasing die sizes and rising transistor counts may soon lead to a situation in which distributing a high-frequency global clock signal with low skew throughout a large die is prohibitively expensive in terms of design effort, die area, and power dissipation. GALS systems eliminate the need for careful design and fine-tuning of a global clock distribution network. While asynchronous systems eliminate the clock altogether, the industry is not yet ready to switch to a completely asynchronous design style mostly because design tools in this arena are not as mature as those for synchronous design.

2.1 Clock Power

In cutting-edge processor designs, the clock distribution network is one of the most power-hungry parts. For instance, the Alpha 21264 had a clock distribution network which consumed 24 watts out of the processor's total power budget of 72 watts. High power is not only an issue for mobile devices, but is also an issue for other chips; for instance in the first generation Alpha, the single-line driver of the clock grid led to thermal management problems since the continuous switching at the driver led to a very high temperature at the chip's center and hence a high temperature gradient [16]. Power has thus become a first-class constraint in clock system design.

2.2 Clock Skew

Restle *et al.* have argued in [17] that clock skew arises mainly due to process variations in the tree of buffers driving the clock. Since device geometries will continue to shrink and clock frequencies and die sizes will continue to increase, global clock skew induced by such process variations can only get worse. Hence we argue that we will reach a point where clock skew will eat up a significant proportion of the cycle time and thus, will directly affect performance. For instance, the first release of Intel's Itanium core had a clock skew that was 9% of the cycle time using traditional clock distribution techniques; using a network of active deskewing elements [18], the clock skew was reduced to 2% of the cycle time. While techniques like active deskewing help to push the envelope for clocked systems further, they come at additional cost in terms of die area and power dissipation. At some point, pushing the limits of global clock distribution networks will lead to diminishing marginal returns. At that stage, GALS design techniques will come in useful.

2.3 Multiple-Clock Dynamic-Voltage Designs

Most of applications running on core processors (be it high-end, embedded or application specific) exhibit a wide range of run-time profiles, both within and across applications. This is mainly manifested via non-uniform resource usage, as well as bursty communication patterns among various parts of the pipeline. One such example is the fetch stage during which the I-cache is accessed and instructions are brought into the fetch queue. While an I-cache miss is being resolved, the issue and execution stages of the pipeline may proceed at their own pace until no more instructions advance in the pipeline due to pending dependencies. A similar situation may appear in case of non-blocking D-cache misses. In this case, multiple outstanding D-cache misses are resolved while instructions may proceed normally through the pipeline. In addition, if there are instructions non-critical to the overall performance (e.g., infrequent floating point operations in integer applications), their execution may proceed at a lower speed without significantly affecting performance. While multiple clock domains offer this flexibility, they also come with additional potential for power savings. Such synchronous blocks whose speed may be gracefully scaled down, can also run at a lower voltage, thus providing additional power savings.

Since usage profiles and communication patterns among pipeline stages vary within and across applications, such MCDV cores should be

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able to dynamically adapt the speed and corresponding voltage for each synchronous block such that overall performance is kept within certain limits. As it will be shown later, a MCDV core can be better than a fully synchronous core as far as their power-performance trade-off is concerned given certain specific conditions.

2.4 Theoretical Efficiency of Voltage Scaling in MCDV Cores

In this section, we provide some theoretical results on the efficiency of using fine-grained dynamic voltage scaling in multiple-clock dynamic voltage cores. We assume that the following hold:

- We consider the case of pipelined cores in which each clock domain i has n_i pipe stages, with L_i total load on the critical path of the clock domain.
- The switched capacitance for each clock domain is C_i. The voltage and clock speed associated with clock domain i are $V_{dd,i}$ and f_i, with

$$f_i \propto \frac{(V_{dd,i}-V_t)^\alpha}{V_{dd,i}}$$

where α is a technology-dependent factor, which is 1.2 to 1.6 for current technologies [19] and V_t is the threshold voltage.

Lemma 1 *Assuming a linear pipeline organization (without feedback paths), the SCDV pipeline achieves better energy savings than the MCDV under the same slowdown factor per computation, if the switched capacitance per clock domain C_i is proportional to the total load on the critical path L_i.*

Proof We assume that the SCDV base pipeline is run at a voltage V_{dd} such that the latency per computation is the same as the MCDV pipeline with k clock domains, each running at voltage $V_{dd,i}$ $(i=1,2,\ldots,k)$. We also assume that between clock domains $(i,i+1)$ there exists a load overhead of l_i due to synchronization and voltage level conversion. To achieve the same latency, the following has to hold:

$$(L_1+l_1)\frac{V_{dd,1}}{(V_{dd,1}-V_t)^\alpha}+(L_2+l_2)\frac{V_{dd,2}}{(V_{dd,2}-V_t)^\alpha}+\ldots+L_k\frac{V_{dd,k}}{(V_{dd,k}-V_t)^\alpha}=$$

$$(L_1+\ldots+L_k)\frac{V_{dd}}{(V_{dd}-V_t)^\alpha}$$

or

$$\sum_{i=1}^{k}\frac{L_i V_{dd,i}}{(v_{dd,i}-V_t)^\alpha} < \left(\sum_{i=1}^{k}L_i\right)\frac{V_{dd}}{(V_{dd}-V_t)^\alpha} \quad (1)$$

Consider the function

$$f(x)=\frac{\sqrt{x}}{(\sqrt{x}-V_t)^\alpha}$$

which is convex. Thus,

$$\sum_{i=1}^{k}L_i f(V_{dd,i}^2) \geq \left(\sum_{i=1}^{k}L_i\right) f\left(\frac{\sum_{i=1}^{k}L_i V_{dd,i}^2}{\sum_{i=1}^{k}L_i}\right) \quad (2)$$

Function f is also monotonically decreasing; thus from (1) and (2) and from the proportionality of C_j with L_j for all clock domains $j=1,2,\ldots,k$, that is,

$$\frac{C_j}{\sum_{i=1}^{k}C_i}=\frac{L_j}{\sum_{i=1}^{k}L_i}$$

we get

$$\sum_{i=1}^{k}C_i V_{dd,i}^2 \geq \left(\sum_{i=1}^{k}C_i\right)V_{dd}^2$$

which shows that the SCDV pipeline performs better energy-wise than the MCDV for the same slowdown factor (or performance penalty) under the assumptions of Lemma 1.

This result is in fact a generalization of the optimal voltage scheduling problem for applications with hard real-time constraints. Ishihara and Yasuura showed in [20] that using a single voltage level in a dynamic voltage scheduling environment achieves the best energy savings under given performance constraints.

The general problem is, however, far from being that simple. In fact, in most designs, there is no relationship between the load on the critical path and the corresponding switched capacitance for that clock domain. We show in the following a necessary condition for fine-grained dynamic voltage assignment to different clock domains for achieving better energy savings for MCDV when compared to SCDV.

Lemma 2 *In case of a 2-clock domain pipeline, if the switched capacitance per clock domain C_i is **not** proportional to the load on the critical path L_i, MCDV cannot achieve better energy savings than SCDV for the same slowdown factor, unless the lower voltage is applied to the stage which satisfies the relation*

$$\frac{C_1}{C_1+C_2} > \frac{L_1}{L_1+L_2}$$

Proof As in Lemma 1, we have $L_1V_{dd,1}^2+L_2V_{dd,2}^2 \geq (L_1+L_2)V_{dd}^2$ if (1) is satisfied for $k=2$. For the MCDV to be better in terms of energy than the SCDV, we need

$$\frac{L_1V_{dd,1}^2+L_2V_{dd,2}^2}{L_1+L_2} \geq V_{dd}^2 \geq \frac{C_1V_{dd,1}^2+C_2V_{dd,2}^2}{C_1+C_2}$$

From the above, we get

$$V_{dd,1} \leq V_{dd,2}$$

This result confirms our intuition that in order to achieve energy savings in MCDV versus the SCDV design for the same slowdown factor, lower voltages should be applied to the more power consuming clock domains if they are also contributing the least to the end-to-end latency per computation. We will consider the results provided by these two lemmas when we define the control strategy based on the application profile.

We point out that the above results hold only for linear pipelines, without feedback paths. While this is not the case even for the simplest processor cores (which have to bypass results among different execution stages) it can be considered as such since usually some of the feedback paths are not on the critical path, and thus, they don't affect overall performance. In addition, if multiple computations are executed in parallel (as in the case of high-end processors), computations off the critical path can be executed at a lower voltage, without affecting the overall performance, for a given slowdown factor. We present in the following sections an adaptive approach for GALS processors which is able to tune the operating voltage of different clock domains, according to the usage of that clock domain.

3 GALS Architecture Design

We discuss below some issues involved in GALS design, specifically focusing on superscalar out-of-order microprocessors, examples of which are the Alpha and Pentium families of processors. These designs extract a high level of instruction-level parallelism from the code using out-of-order and speculative execution and have the capability of issuing and executing several instructions at the same time. Our focus is on architecture level issues. GALS design involves many other complicated issues at the circuit and system levels which we do not attempt to address, for instance:

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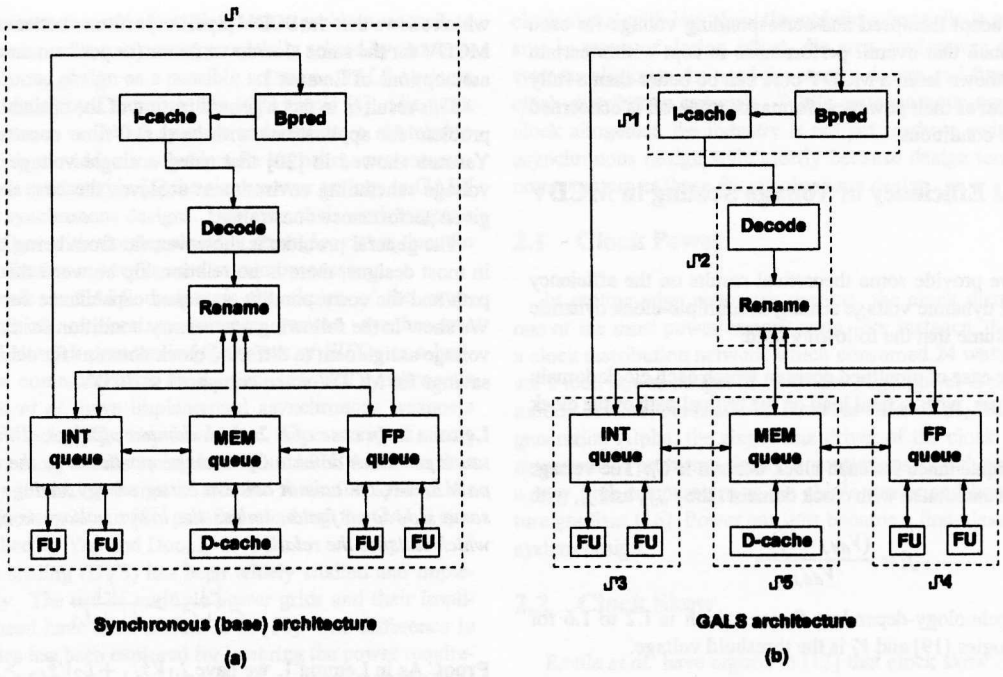


Figure 1. Base vs. GALS machine organization

- **Metastability resolution:** The problem of metastable signals and techniques for metastability resolution using synchronizers and arbiters has been the focus of research in asynchronous design. Our approach uses asynchronous FIFOs [6] between clock domains and this in turn relies on synchronizers. For comparison, we have also included models for FIFOs using arbiters for clock pausing whenever metastable conditions occur [9, 13].
- **Local clock generation:** Each clock domain in a GALS system needs its own local clock generator; ring oscillators have been proposed as a viable clock generation scheme [4, 7]. We assume that we can use ring oscillators in each synchronous block in the GALS processor.
- **Failure modeling:** A system with multiple clock domains is prone to synchronization failures; we do not attempt to model these since their probabilities are miniscule (but non-zero) and our work does not target mission-critical systems.

3.1 Defining Synchronous Blocks

Hemani *et al.* have described an automated strategy for defining locally synchronous blocks in a GALS design [5]. Starting from a hierarchical RTL description of the system, their method uses iterative refinement to get an optimal partitioning of the system into a number of synchronous blocks, using clock power as an objective function for optimization. In a custom-designed system like a high-end microprocessor core, performance requirements justify manual intervention in the partitioning phase. Since the primary motivation behind GALS design is to avoid distributing a common clock signal over large areas, the strategy for partitioning the design into synchronous blocks will largely be dictated by physical design aspects. However, since asynchrony can lead to higher latencies, it is crucial to take architecture issues into account when partitioning the design.

In the traditional superscalar out-of-order processor model shown in Figure 1 (a), the *instruction flow* consists of fetching instructions from the instruction cache, using the branch predictor for successive fetch addresses. The *register dataflow* consists of issuing instructions out of the instruction window to the integer and FP units and forwarding results to dependent instructions. The *memory dataflow* consists of issuing loads to the data cache and forwarding data to dependent instructions. Introducing high latencies in any of these three crucial flows will have an impact on the processor's performance.

The level 1 instruction cache and the branch predictor taken together are a good candidate for one synchronous block corresponding to the front-end of the pipeline. In some architectures, notably in CISC architectures like Intel's IA-32, the decode logic has large area and consists of several pipe stages; in such cases, decode would be a good candidate for another synchronous block.

Inside the out-of-order execution core, it is difficult to make generalizations and say which parts of the core may be decoupled without much overhead and which may not; such decisions are very specific to the microarchitecture and the instruction set of the processor. Area and clock distribution considerations obviously suggest a partitioning to some extent. For instance in the 21264 Alpha the 'major clocks' (tapped from the global clock and distributed locally) are defined this way, based mostly on the top-level hierarchy of the design; these clocks suggest a partitioning system for that specific implementation. The 21264 has the following major clocks [21]: (1) instruction fetch and branch predict (2) bus interface unit (3) integer issue and execution units (4) floating point issue and execution units (5) load/store unit (6) pad ring. Guided by this, we have chosen synchronous blocks for our GALS design, which we describe below.

3.2 The Proposed GALS Architecture

To compare GALS with synchronous microarchitecture organization, we have chosen to have five clock domains in the GALS design. This decision was driven by the functional organization of our processor and by the physical design of similarly organized cores. Figure 1 shows the

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Stage	Operation	Domains
1	Fetch from I-cache	1
2	Decode	2
3	Register rename, Regfile read	2
4	Dispatch into issue queue	2, 3/4/5
5	Issue to functional unit	3/4/5
6	Execute	3/4/5
7	Wakeup, Writeback	3/4/5
8	Regfile write, Commit	3/4/5, 2

Table 1. Pipeline stages in our processor models

pipeline structure we studied. In the base (synchronous) model, all the modules run off the same clock. In the GALS model, various regions are clocked using different clock signals independent of each other. The first stage of the pipeline consists of an instruction cache and branch prediction unit (clock domain 1). The next stages are instruction decode and register rename (clock domain 2). There are three issue queues in the design: one for integer instructions (clock domain 3), one for floating-point instructions (clock domain 4) and one for loads and stores (clock domain 5). In the GALS processor, the integer ALUs and the integer issue queue are in the same clocking region. This ensures that dependent instructions within the integer issue queue can be issued back-to-back as soon as operands are available. Similarly, floating-point ALUs and the floating-point issue queue share one clock, and the data-cache and memory issue queue share one clock.

Table 1 gives a summary of the pipeline stages in the processor models we developed for our experiments, along with a listing of the clock domains of the GALS machine which are involved in each pipe stage.

3.3 Asynchronous Communication Mechanisms

In the synchronous version, communication between successive logic blocks is done using regular pipeline registers. In a GALS design, the choice of an asynchronous communication mechanism is critical. Many methods have been proposed for clocking GALS systems with *stretchable clocks* [4, 7, 8]. Such clocking systems manage asynchronous communication between two clock domains by stretching one phase of both the clocks while the handshaking and data transfer takes place. This is typically done using an arbiter element inside the loop of a ring oscillator. While this mechanism provides an elegant and fail-safe method of communication, it also stalls both the synchronous blocks during the transaction.

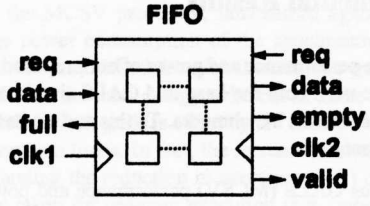


Figure 2. Asynchronous FIFO for interfacing two clock domains

Chelcea and Nowick have presented in [6] a design for a low-latency token-ring based FIFO which can be used for asynchronous communication between synchronous blocks. The interfaces to the FIFO are shown in Figure 2. Their design uses *full* and *empty* signals to indicate the occupancy of the FIFO. The *empty* signal is controlled by the producer of data into the FIFO and is synchronized to the consumer's clock; similarly, the *full* signal is controlled by the consumer and is synchronized into the producer's clock. A few modifications are made to the circuit to account for latencies in synchronization and to prevent deadlock. In addition to providing high throughput in the steady state, the design has low latency when compared to other methods we tried and tested. Since the focus of our work is at a higher level of abstraction, a complete description of the operation of the circuit can be found in [6]. We have included a cycle-accurate model of this FIFO in our simulation environment.

Semeraro *et al.* [13] have also used a FIFO-based communication mechanism for their multiple clock domain implementation. In their case, metastability is resolved by stopping clocks only when the rising clock edges of the producer and consumer clock domains are within a certain threshold. For comparison, we have also included this FIFO model in our simulation environment.

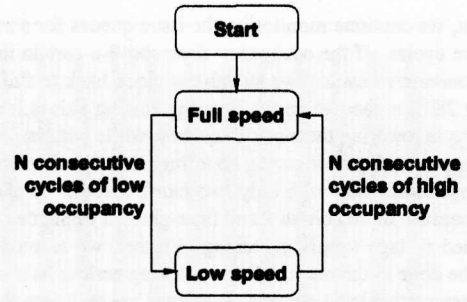


Figure 3. Outline of Dynamic Clock Management

3.4 Dynamic Clock and Voltage Management

Since there are several independent clocks in a GALS design, we have the flexibility of designing various logic blocks to operate at different frequencies. In addition, if we have a balanced pipeline design to start with, we can slow down synchronous blocks that are off the critical path of the design while keeping the others running at full speed. The slower clock domains could also operate at a smaller supply voltage, thus producing additional power savings. The relation between supply voltage V_{dd} and logic delay (or cycle time) D is governed by the following equation:

$$D \propto \frac{V_{dd}}{(V_{dd} - V_t)^{\alpha}} \quad (3)$$

where V_t is the threshold voltage of the transistor and α is 1.2 to 1.6 for the current technologies. Since energy consumption in CMOS is dependent on the *square* of the supply voltage, reducing supply voltage can lead to significant energy benefits.

We propose a multiple-clock dynamic-voltage core processor where the speed and voltage of each synchronous block are adapted dynamically based on the application profile. Our method for dynamic clock management involves changing the operating frequencies (and supply voltages) of the integer, memory and floating-point clock domains in the GALS processor (indicated as clock domains 3, 4 and 5 in Figure 1). We do not try to slow down the front-end stages since the front-end bandwidth is critical to most applications.

Figure 3 shows the outline of our method. The processor starts up with all clocks running at full speed. To minimize the performance impact of clock speed reduction, we monitor the occupancy of each issue queue and we reduce the frequency to a lower value only when the queue occupancy drops below a low threshold for N consecutive cycles. Since the execution characteristics may be different even within different parts of the same

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application, we continue monitoring the issue queues for a number of N consecutive cycles. If the occupancy rises above a certain threshold for these N consecutive cycles, we switch the clock back to full speed. We found that 2K is a good value for N; using smaller values leads to many false alarms in lowering the clock frequency, while with larger values we lose out on potential power saving opportunities. This implementation is a simple hysteresis loop with only two clock speeds; we chose to keep it simple because more complex and finer-grained implementations need finer-grained voltage supply switching. Further, we assume that useful work can be done in the intermediate switching periods as shown in [22]. We also assume that level-conversion circuits are built into the drivers of the asynchronous FIFOs to interface clock domains running at different voltages.

4 GALS Simulation Framework

4.1 Event-driven Timing Simulation

We have used a general-purpose event-driven simulation engine which can be used to simulate any asynchronous system, synchronous (clocked) system, or a system which contains both asynchronous and synchronous components [23].

To set the system in motion, we need to insert one or more starting events into the event queue. The queue contains events sorted in increasing order of their scheduled times. To process the queue, we read successive events from the head of the queue and execute them by calling the appropriate action functions. To simulate systems with multiple clocks, we need to insert one event for each clock domain; for each such event, we need to specify a period of execution. When the execution engine processes such a periodic event, it schedules another instance of the same event into the queue, thus representing the next cycle of execution of the clocked system. Using this system, we can simulate any mixture of multiple clocks running at different speeds with specific or random starting phases.

4.2 Performance and Power Modeling

To evaluate the architecture proposed above, we wrote models of both the synchronous and GALS processors based on the SimpleScalar toolset [15]. To simulate the GALS machine, we made use of the event-driven simulation engine described above. We have set up five clock domains in our simulator and in the first set of experiments, had all the clocks running at the same speed. The starting phase of each clock was set to a random value at runtime.

We have used the Wattch framework [14] to add power models to our processor simulation framework, including power consumption of the asynchronous FIFOs. Wattch is an activity-driven power simulator which has been shown to be within 5 to 10% accurate when compared to real processors. Wattch provides switching capacitance modeling for structures like ALUs, caches, arrays and buses in a processor. These are integrated into our base and GALS simulators to provide energy statistics. We have also modeled unused units as consuming 10% of their total power consumption to account for leakage and the overheads associated with clock gating.

In addition to modeling the switching capacitance of memories and buses inside the processor, we have also modeled the switching capacitance of clock grids. For the synchronous base processor model, we assumed a clock distribution hierarchy resembling that of the 21264 Alpha processor. We modeled one global clock grid and five local clock grids corresponding to the five clock domains discussed above. The areas and metal densities of each clock grid were approximated by the numbers published for the 21264 processor. For the GALS processor, since there is no global clock, we eliminated the switching capacitance of the global clock grid and retained the five major clock grids, corresponding to the distribution networks for each of the synchronous blocks. In all cases, we have assumed that clock gating is used to reduce the power consumption of unused modules.

Fetch and decode rate	4 inst/cycle
Integer issue queue size	20
FP issue queue size	16
Memory issue queue size	16
Integer registers	72
FP registers	72
L1 data cache	16KB 4-way 1 cycle latency
L1 instruction cache	16KB direct-mapped 1 cycle latency
L2 unified cache	256KB 4-way 6 cycles latency
FIFO Size	4 entries, up to 4 inst/entry
Integer issue queue thresholds	7/9
FP issue queue thresholds	3/5
Memory issue queue thresholds	5/8
Threshold for clock pausing	30% of the largest clock period
Aggressive mode	FP 2.4 slowdown Mem 1.2 slowdown
Moderate mode	Int 1.8 slowdown FP 1.2 slowdown Mem 1.2 slowdown

Table 2. Microarchitecture organization

Table 2 shows some details of the microarchitecture. The low and high occupancy thresholds for the three queues were chosen close to half of their maximum size, and less in the case of FP queue where a higher threshold may trigger a larger performance loss. We have used two different modes of operation: an *aggressive* mode for benchmarks that have a low number of FP operations which don't affect much performance, but do affect energy (in this case Lemma 2 is applicable); and a *moderate* mode for applications with an almost equal mix of integer, FP and memory operations. The aggressive mode was used for all benchmarks, except *swim*, *fpppp* and *epic*.

5 Experimental Results

To assess the performance and power of our proposed GALS processor design, we have used both the base and GALS simulators on a subset of Spec95 and Mediabench benchmarks. To this end we have performed two sets of experiments:

1. Base versus GALS (MCSV) performance and power analysis with all synchronous blocks of the MCSV system running at the same clock frequency and supply voltage. Both the synchronizer (MCSV) and pausible clock (MCSV-P) cases have been considered.
2. Base versus a multiple-clock, dynamic-voltage GALS design (MCDV), implemented as discussed in section 3.4. Both the synchronizer (MCDV) and pausible clock (MCDV-P) cases have been considered.

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5.1 Power and Performance Analysis

On the base and MCSV models, we ran benchmarks from the Spec95 and Mediabench CPU benchmark suites to obtain indications of power and performance trends. In the first set of experiments, we kept all the local clock frequencies in the MCSV model equal. The relative stagger between the clock signals was set at runtime to random values. Not surprisingly, the MCSV processor is slowed down by asynchronous communication and does not perform as well as the synchronous processor. Figure 4 shows the relative slowdown of various benchmarks running on the MCSV processor when compared to the synchronous processor. On an average, the benchmarks we ran on MCSV were slower by 10% for MCSV and by 9% for MCSV-P. As expected, the *fppp* benchmark had the lowest performance hit. This is due to the application's exceptionally small proportion of branch instructions; on an average only one in every 67 instructions is a branch in this benchmark, while most other applications have one branch for every five or six instructions. This indicates that the asynchronous FIFO models used in our design have good throughput in the steady state when there are no branch mispredictions. This also suggests that branch mispredictions will prove more expensive in the MCSV model due to its longer recovery pipeline.

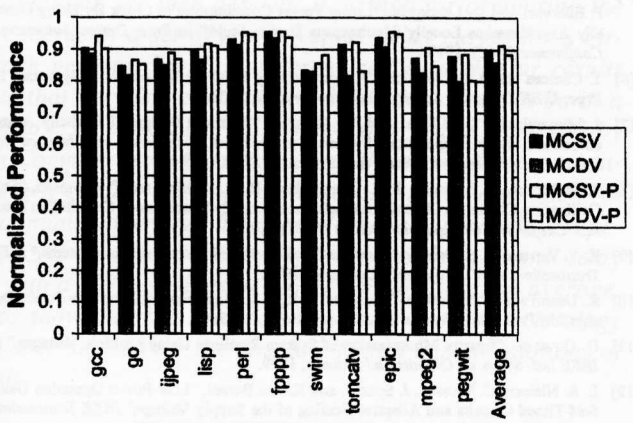


Figure 4. Performance of the GALS model relative to the base model

Figures 5, 6 and 7 show the relative average power and total energy consumption of the MCSV processor, normalized against the total energy and average power consumption of the synchronous processor respectively. With the removal of the global clock, we get in some cases up to 5% reduction in the total energy, whereas in some cases the power savings due to global clock grids is offset by the extra power consumption due to longer execution times. In fact, the increase in total energy in these cases (notwithstanding the reduction in average power) can be attributed to the extra time taken for program execution (e.g., *mpeg2* and *pegwit*). For the benchmarks we tested, though, the total energy is higher on average by 1% for MCSV and about the same for MCSV-P, while the average power consumption is reduced by 10% and 12%, respectively.

On close examination of other statistics in the processor pipeline, we can see that the introduction of asynchronous communication latencies inside the design has led to various other overheads which in some cases offset the power gains due to the absence of global clock. For instance, the the average time taken by each instruction from the fetch to the commit stage increases by 65% on average for all benchmarks in the GALS processor, out of which 25% is spent in the FIFOs and 40% is the overhead

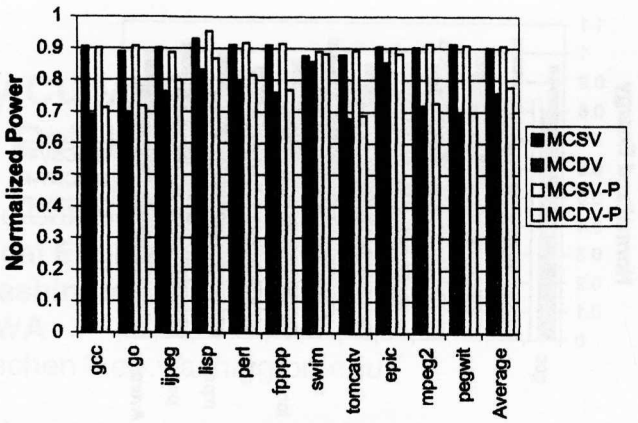


Figure 5. Normalized power

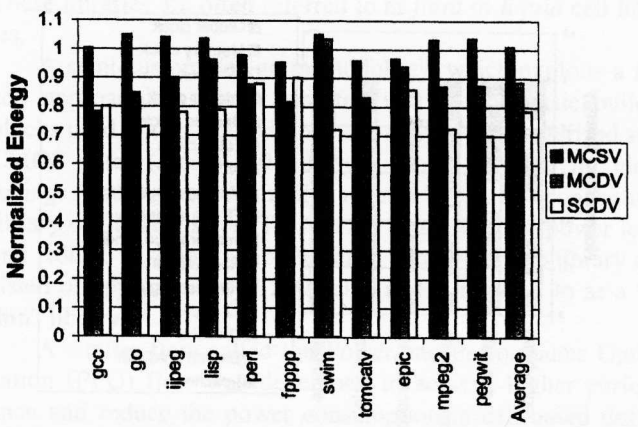


Figure 6. Normalized energy (FIFOs with synchronizers)

due to the longer recovery pipeline and due to slower result updates. This is because the addition of asynchronous communication channels leads to an increase in the effective length of the pipeline. This increase in pipeline length in the MCSV processor also leads to 17% higher speculative execution on the average across the benchmarks we tested. Similarly, the average number of in-flight instructions in the pipeline is higher in the GALS model; so is the average occupancy of the register allocation tables and issue queues. For instance the integer register allocation table occupancy went up from 15 in base to 23 in MCSV for the *ijpeg* benchmark. All these factors lead to higher switching activity in the MCSV machine and the power savings we get from eliminating the global clock grid may be offset by this extra switching. Hence, we conclude that eliminating the global clock and using several local clocks cannot by itself lead to dramatic power savings.

5.2 Analysis of MCDV cores

For this set of experiments, we have compared the base (fully synchronous) and the MCDV machine which is capable of dynamically changing the clock speeds and voltages for various synchronous blocks. In this case, we have implemented the scheme described in Section 3.4 with a value of $\alpha = 1.6$. We have considered a window size of 2K cycles for monitoring the size of the three queues. As it can be seen in Figures 4, 5, 6 and 7 (columns MCDV and MCDV-P), the average power is reduced by an additional 12% on average, with an average additional decrease in

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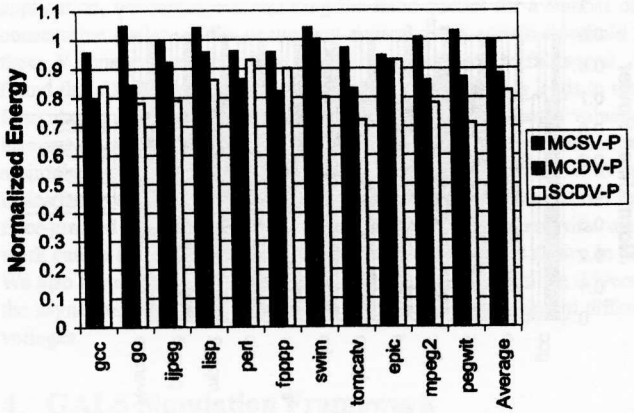


Figure 7. Normalized energy (FIFOs with pausible clocks)

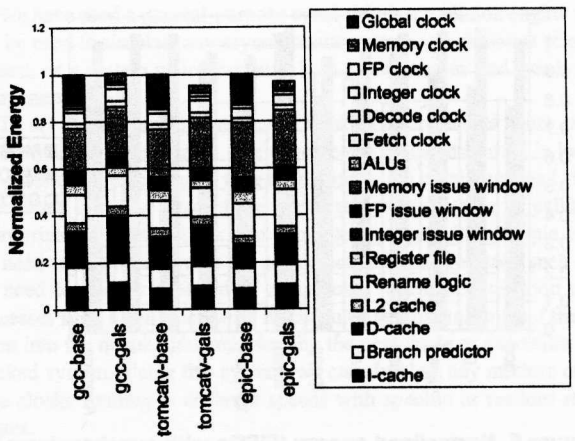


Figure 8. Breakdown of total energy for base vs. GALS

performance of only 2%. Total energy is also decreasing by an additional average of 12%.

To compare the efficiency of using dynamic clock and voltage management, we report under SCDV (Single Clock, Dynamic Voltage) in Figures 6 and 7 the normalized energy values obtained for the same performance penalty as the MCDV design if the fully synchronous core were run at a lower supply voltage. As it can be seen, the SCDV core is more energy-efficient than the MCDV core for 7 of the total of 11 benchmarks tested. In case of *gcc*, *perl*, *fpppp* and *epic* MCDV and MCDV-P are either comparable, or up to 8% better than their synchronous counterpart.Overall, an average power reduction of 22% is achieved at 12% loss in performance.

Finally, we show the breakdown of average power values for a few benchmarks considered in the base (fully synchronous) and GALS (MCSV) cores. As it can be seen in Figure 8, the total clock power is reduced due to the elimination of the global clock. However, due to increased execution time and higher speculation, the power consumed by the front-end increases slightly, as does the power consumption for the D-cache and execution core.

6 Conclusion

In this paper, we have used a power/performance modeling and analysis framework for high-end, superscalar out-of-order processors using multiple clocks, and possibly multiple, dynamically adjustable voltages to show a direct comparison of power and performance of a GALS (MCSV) design against a comparable synchronous design. The experimental evidence shows that the overhead associated with GALS processors can sometimes offset the power savings achieved in the clock power, although in a few cases, the average power cost is decreased by up to 12% and on average by 10% for the benchmarks considered. Nevertheless, the presence of independent clocks in the design permits a fine-grained trade-off between speed and power. We have shown that MCDV designs may be up to 8% more power efficient than their fully synchronous counterpart in select cases. Overall, by using fine grain clock speed and voltage adaptation, an average power savings of 22% (up to 32%) can be achieved with 12% average loss in performance.

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EXHIBIT B

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General Co-Chairs Message and Invitation to ISCAS 2001 – A CAS Odyssey

In 2000, Sydney sported the Olympics. In 2001, Sydney will witness the worldwide Circuits and Systems community reporting the newest and brightest ideas in Circuits and Systems for Mixed-Technology Systems.

Sydney's Olympic legacy is the Circuits and Systems community's inheritance for a week in May 2001. The absolutely modern conference venue, international hotels, sparkling harbour, tempting nightlife, and temperate mid-autumn weather (we hope) will combine to create a memorable event – a historic first for ISCAS being in the Southern Hemisphere.

We invite you to join the rest of your global CAS community for stimulating and timely tutorials on Sunday, followed on Monday, Tuesday and Wednesday by the best, carefully selected technical papers presenting the year's innovations, inventions, achievements and new directions in Circuits and Systems. The Sydney Keynote Speakers will celebrate the contributions and the ground breaking directions that the global industry, underpinned by circuits and systems theory and practice, has made and is planning. These are the events that will help drive our world through the 21st century.

ISCAS 2001 is an event not to miss. The technical and social program will provide outstanding networking opportunities for all involved in the theory, design and practice of circuits and systems. The technical program will follow the traditional ISCAS format. The tutorials are a mix of full-day and half-day offerings, and have been subsidized to enable everyone to join the program. Technical papers have been organized into 16 parallel sessions. Three Sessions are devoted to interactively presented full papers, in the Conference Centre's prime meeting rooms overlooking Darling Harbour, a harbour within Sydney Harbour. The interactive sessions are a special feature of ISCAS 2001 where authors present the kernel of their paper's innovation and excitement, and then defend their views over the following hour to all who walk past the visualization placards, summarizing the paper, and question its philosophy and results. It is a welcome return to an Athenian style presentation and defense of excellent technical work.

The final session on Wednesday afternoon holds a surprise special event – A Successful Entrepreneur's Session: *Generating Wealth from Circuits and Systems R&D (not in Silicon Valley)* - with three Entrepreneur Presentations and a forum – Atmosphere, Radiata and ResMed which have generated wealth approaching US$2bn by exploiting good ideas – and a forum discussion followed by a great Aussie BBQ – complete with prawns (viz shrimp).

The whole symposium is at one modern venue that has excellent facilities and has closely spaced theatres that allow for quick changes between sessions. And we promise to keep to advertised timing so that you can catch the odd 'must-see' paper in a session other than the one that is your main interest.

The social program promises to intersperse the intense technical exchanges with warm and engaging intercourse. On Sunday evening, après tutorials, we are planning an opening Australiana theme reception; on Tuesday evening the Symposium banquet will be held in the Convention Centre's new ballroom, adjacent to the Harbour with its sparkling dual city lights and deep warm water reflections; and to close our Symposium the Aussie BBQ.

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