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# ASYNCHRONOUS INTERFACE FOR LOCALLY CLOCKED MODULES IN ULSI SYSTEMS

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## ABSTRACT

This paper describes an approach to construct globally asynchronous locally synchronous ULSI systems. The architecture employs interface units which communicate asynchronously with each other and synchronously with locally clocked modules. Interface units feature elastic burst-mode data transfer to reduce the number of synchronizations. The architecture allows the use of different clocks in synchronous modules and makes thereby modular design possible.

## 1. INTRODUCTION

The distribution of a high frequency clock signal will be an essential problem in the future ULSI systems containing hundreds of millions of transistors. As the clock frequency goes higher the clock skew and system level timing will develop into even more important issues as they are in today's systems. Also, the system-on-chip design strategy brings new challenges to manage system level timing and to arrange an efficient interaction between separate modules.

A viable alternative to overcome the problems of a globally clocked system is the globally asynchronous locally synchronous approach [1, 4], where each distinct module of the system is synchronized to an optimized local clock, and communication between these modules is arranged asynchronously. As a solution, we present in this paper an interface design which manages asynchronous data transfer and communication between synchronous modules. To accomplish this, each synchronous module is equipped with an interface unit which transfers data and control signals from asynchronous domain to synchronous domain and vice versa. Each of these synchronous modules can use an independent local clock which is unrelated to the other clocks in the system. Therefore, the problem of global clocking and clock skew are not any more system level design issues. Instead, the clock skew and routing problems are limited only to a locally synchronous module which is relatively small compared to the whole system. This simplifies the design process of a complex system enabling easy re-usage of different synchronous modules. Furthermore, the asynchronously controlled stoppable clocks make the automatic power-down operation of currently idle blocks possible [5].

## 2. SYSTEM ARCHITECTURE

Every locally synchronous module in the proposed architecture is equipped with a synchronous/asynchronous interface unit (*SAInt*) [3] which takes care of inter-block communication working as a "wrapper" around a synchronous module. *SAInt* has an asynchronous external interface with other system blocks, i.e., other *SAInt* units, and a synchronous internal interface with the local module. The structure of a system with one master module and two server modules is depicted in Figure 1.

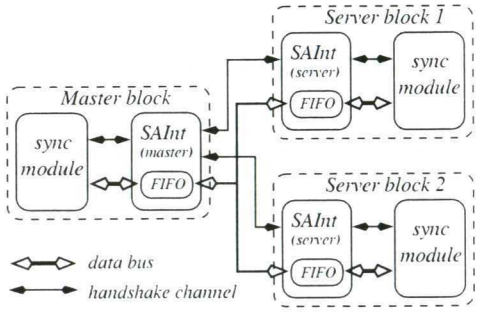



Figure 1: Architecture of system with *SAInt* units.

Two different types of interface units are needed to construct a flexible and fast communication network. A *master-type* unit initiates data transmission and fetching. A *server-type* unit, in turn, basically just responds to the action requested by the master, receive or send, and informs the master its current status: ready, busy or idle.

The asynchronous interface between two modules is a 4-phase handshake channel [2] which consists of a bidirectional data bus, two status signals indicating that the last



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data word is sent to or has been fetched from the server party, and three request and four acknowledgement signals which are used to initialize communication and control data transfer between the master and server units.

A master-type *SAInt* can have any number of server units to which it allocates different operations in a sequential fashion. As soon as a server receives its input data, it starts to operate in parallel with the other servers. Correspondingly, a server type interface unit can be connected to arbitrarily many master units via a set of arbitration circuits. In the proposed architecture, the frequency of the local clock in a server party can be optimized for the involved synchronous module. The system can also be configured to use a pausable ring oscillator-type [4, 7] clock source.

The system structure presented in this paper is targeted to ULSI systems, where each involved locally synchronous module requires a large number of input data words per operation, and produces a large number of output data words. Furthermore, it is assumed that the latency of each operation is several clock cycles.

## 3. INTERFACE UNITS

The interface units contain a synchronous controller *Synctl* and an asynchronous controller *Asynctl*. The latter takes care of the external interface with another *SAInt* unit, while the synchronous unit controls internal communication with the local synchronous module. A dual-port RAM is used as a FIFO queue for bidirectional data transfer. The ports of this memory can be accessed simultaneously. One of them is controlled asynchronously by *Asynctl*, the other synchronously by *Synctl*. The controllers have the related counters *Scount* and *Acount* which provide the required addresses for the memory access. In order to prevent FIFO queue overruns and underruns, *Synctl* has to be able to read the value of *Acount*, and *Asynctl* has to be able to read the value of *Scount*. To accomplish this, the write and read accesses to the auxiliary counter register, containing a past value of the asynchronous counter *Acount*, take place through an arbiter unit. The *Asynctl* can read the value of *Scount* through a synchronizer.

The server unit, depicted in Figure 2, contains also a clock control unit *Clkctl* which pauses the local clocks of the interface unit and local synchronous module if no data is available or the module is idle. The unit executes repeatedly three successive tasks. In the (1) *data receiving mode*, data provided by a master-type SAInt unit of another system block, are transferred to the local synchronous module through the FIFO queue. The asynchronous counter *Acount* generates the write addresses for the memory, the synchronous counter *Scount* the read addresses, respectively. In the (2) *computation mode*, *SAInt* awaits the clocked module to complete its data processing. In the (3) *data transmission mode*, the computation results are transferred to the master system block through the FIFO queue. The roles of the counters are now interchanged. We call the implemented flexible data transfer protocol between the asynchronous and synchronous domains the *elastic burst-mode* transfer, where the data words are transferred in variable-length bursts. The length of a write or read burst depends on the size of the FIFO queue and the difference between the speeds of the controllers. The fundamental property of the elastic burst-mode transfer is that the controllers interact only when it is absolutely necessary, i.e., when the FIFO queue appears to be empty or full. This improves performance and reliability, because the number of time-consuming synchronizations and thereby the rate of possible synchronization failures are reduced.

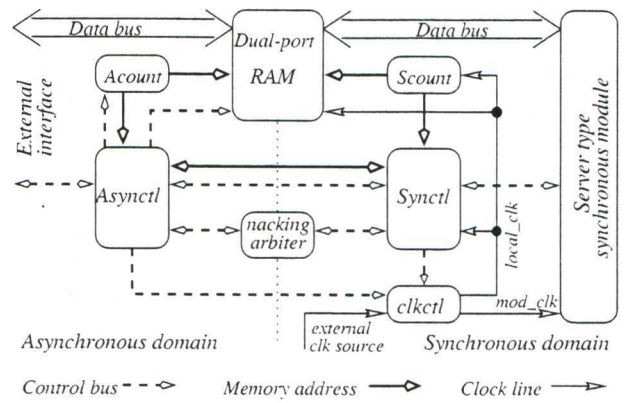



Figure 2: Server-type *SAInt* architecture

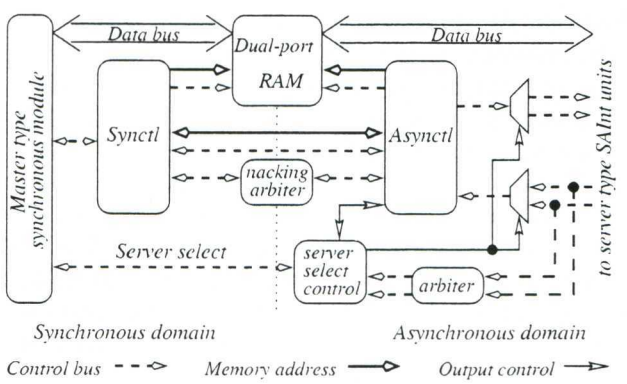



Figure 3: Master-type *SAInt* architecture

The master executes basically the same three tasks as the server, but in a different order. First it awaits activation



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from the local module, transmits then data to the server, and finally fetches data from the server, when there is data available and the master is inclined to do so. The structure of a master, which can be connected to two server units, is depicted in Figure 3. The memory address counters have been included in the related control units, *Synctl* and *Asynctl*.

The master controls the shared bidirectional data bus and allocates operations to the server units. The *server select controller* is used to select an appropriate server unit to be activated. The order of the incoming acknowledgement signals sent by the servers, and thereby the data source of the fetch procedure, can be chosen in two different ways. In the "first-ready first-served" approach, the acknowledgement signals are arbitrated, and the result of the arbitration determines which data source is to be selected. On the other hand, if the incoming data is needed in a specific order, the multiplexers can be easily forced to the appropriate state, and the unit is suspended until the required acknowledgement arrives.

## 4. CMOS IMPLEMENTATION

The *SAInt* units have been designed using Alcatel 0.35 $\mu$m technology in the Cadence 4.4.3. IC design environment. The synchronous part of the system and the 32x16-bit dual-port RAM has been designed with VHDL, and the asynchronous part by mixing VHDL and transistor level design. The total transistor count of the server-type *SAInt* which is connected only to a single master is 18482 of which 16088 is required by the dual-port memory and bidirectional bus-related multiplexers and tristate buffers. Hence, the control logic contains 2394 transistors. The size of the master-type *SAInt* is approximately the same, if it is connected only to one server unit. However, the transistor count of a *SAInt* unit increases, due to the multiplexing and arbitration circuits, if multiple units are connected together.

The implementation of the clock control unit of the server-type *SAInt* is presented in Figure 4. *Asynctl* activates this unit by sending an asynchronous request signal in parallel with writing the first data word to the FIFO queue. We have designed a customized pulse-driven synchronizer circuit which maximizes the metastability recovery time between two consecutive sampling points. If both address counter values are equal in receive and transmission mode, indicating that the FIFO queue is empty or full, *local_clk* and *mod_clk* are paused. Hence, at every rising edge of *mod_clk*, there is data available.

The arbitration circuitry, which is required to provide mutual exclusion between possible concurrent requests from *Asynctl* and *Synctl* to access the asynchronous address counter, is depicted in Figure 5. The interface unit employs a one-channel nacking arbiter to speed up the memory read and write sequences. One of the ports of this arbiter returns

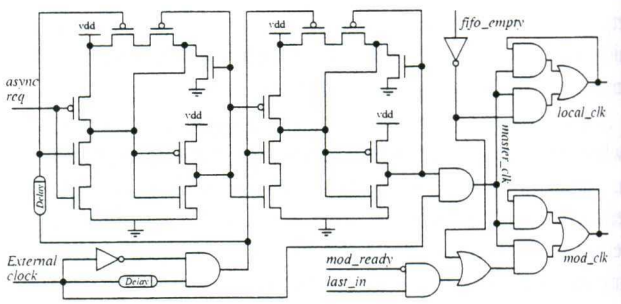



Figure 4: Clock control unit.

a negative acknowledgement, *nack_a*, in the case when the arbiter is already reserved by the other channel, and a positive acknowledgement, *ack_a*, if access is granted to *Asynctl*. The other port, connected to *Synctl*, works as a normal arbiter port. The nacking property can be disabled by a mode signal, in which case both ports operate as normal arbiter ports and no negative acknowledgements will be generated. The one-channel nacking arbiter is constructed by combining two mutual exclusion element (MUTEX) circuits [6] and modifying the state holding input stages.

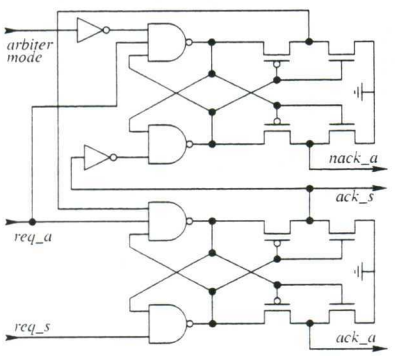



Figure 5: One-channel nacking arbiter.

The use of the nacking arbiter significantly improves the performance of the asynchronous domain. When the arbiter sends an acknowledgement to *Asynctl*, this can store the current value of the address counter *Acount* to a local register and start a new FIFO write or read procedure. In the case of a negative acknowledgement, it does not update the register, because the synchronous controller is reading this. However, *Asynctl* can start a new FIFO access procedure immediately. Hence, the nacking arbiter enables parallel operation of the controllers without interrupts as long as the FIFO is not full or empty.



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## 5. SIMULATION RESULTS

Extensive SPICE-level simulations were performed with the Cadence Analog Artist tool. Typical transient response waveforms of some control lines of the server-type *SAInt* in the data receiving mode are depicted in Figure 6 where the elastic burst-mode data transfer can be seen. One write burst and two read bursts are shown. The write burst is represented by the topmost signal which is the asynchronous request for memory access. A new data word is stored during each pulse. At the right end of the topmost signal the beginning of the next write burst can be seen. The second signal is the request from *Asynctl* to update the asynchronous memory address register. The third and fourth signals are the acknowledgement and negative acknowledgement to *Asynctl*, generated by the nacking arbiter. The next two signals are the synchronous request and acknowledgement signals which are used by *Synctl* to fetch the stored value of *Acount* by communicating with the arbiter. They also separate read bursts, since new data cannot be read before a valid address has been fetched. The last signal, *mod_clk*, is the stoppable clock of the locally synchronous module. One data word is transferred in each clock cycle. The clock is paused when the FIFO is empty in the receiving mode or full in the transmission mode. It is derived from *master_clk* which is the intermediate signal generated by the clock control unit shown in Figure 4.

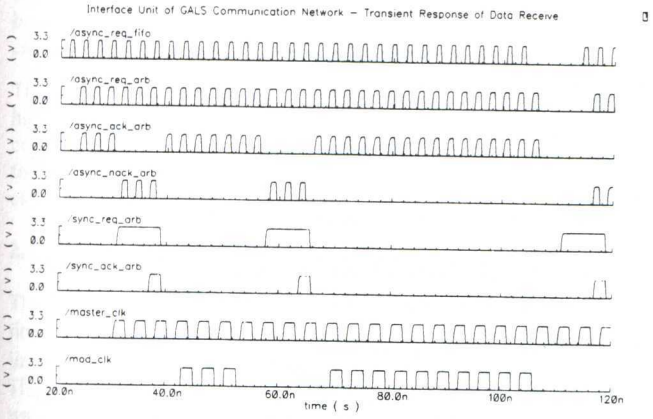



Figure 6: Simulation of elastic burst-mode transfer.

The maximum speed of the FIFO access in the asyncronous domain is 380 MHz at the current Alcatel 0.35 $\mu$m technology. The maximum clock frequency for the synchronous domain of *SAInt* is 420 MHz. The speed is restricted mainly by the relatively slow unoptimized memory. The size of the memory is another significant factor. If a small well-optimized FIFO queue is used, the control logic restricts the clock frequency.

## 6. CONCLUSION

We have presented an asynchronous design approach to interface locally clocked modules in a ULSI system. In this method, data is transferred asynchronously in variable-length packets between concurrently operating synchronous modules. The size of the FIFO queue of the interface units can be easily changed by just replacing the memory and increasing/decreasing the address counter widths, while the control logic can be left untouched.

The presented architecture with server- and master-type interface units allows a feasible way to construct a globally asynchronous locally synchronous system. This enables truly modular design and re-usage of synchronous modules, since no global timing assumptions have to be made. Furthermore, the physical timing problems are made local, and thereby the simulation and verification tasks are simplified. The proposed heterogeneous design method is targeted for systems with large locally synchronous modules each of which has an operation time of several clock cycles. The approach offers a viable method to reduce problems that arise in globally clocked ULSI systems and system-on-chip design.

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# EXHIBIT C

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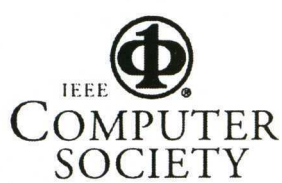
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# Point to Point GALS Interconnect

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## Abstract

*Reliable, low-latency channel communication between independent clock domains may be achieved using a combination of clock pausing techniques, self-calibrating delay lines and an asynchronous interconnect. Such a scheme can be used for point-to-point communication in a globally asynchronous locally synchronous (GALS) system, a possible methodology for managing the predicted increase in clock domains.*

*We present interface wrapper circuits which permit communication between a locally synchronous producer and a locally synchronous consumer via an asynchronous interconnect. Such interfaces can also be used to mix asynchronous and synchronous modules. Clock pausing is used to guarantee that metastability will never result in failure. Arbitration between channel communication and the local clock is performed concurrently so that metastability resolution will rarely delay the clock.*

*Simulation results show that the maximum performance of one data item per consumer clock cycle is achieved when the producer:consumer clock ratio is equal or greater to one. This communication mechanism is suited to other asynchronous interconnect methods which offer low power and high performance.*

## 1. Introduction

The Semiconductor Industry Association (SIA) roadmap and Electronic Design Automation Industry Council predict that the number of clock domains on a silicon chip will grow rapidly. This is due to wire delays becoming harder to predict due to process variation, deep-sub micron effects and dynamic effects such as cross-talk.

An alternative to the challenge of clocking many time zones with controlled skew is a change to more globally asynchronous architecture. From a theoretical standpoint, circuits with delay-insensitive asynchronous interfaces can be composed to produce large systems which are guaranteed to be functionally correct. From a design perspective this composition property eases the worry of timing closure for large systems. Thus, the SIA Roadmap recognises that, by 2007, asynchronous techniques will be used in many designs. However, meeting a performance target may still require multiple design iterations.

We are also entering the systems-on-chip (SoC) era where circuit building blocks from a number of design houses (intellectual property blocks or IP-blocks) are purchased by a systems builder and integrated onto a single chip. In some ways this is similar to building systems by purchasing off the shelf ICs and integrating them via a PCB. However, SoC results in lower cost mass market products with much lower power requirements. Communication between building blocks of a SoC is a complex problem particularly when a range of clocking strategies have to be tailored to each building block in order to obtain the required performance within a power budget.

Clocked circuit design is a mature method with good tool support. Clocked circuits with global synchronisation are becoming impractical for large, deep submicron CMOS designs, where for smaller circuits assumptions about clock distribution are still valid. Given the investment in clocked tools and techniques, clocked design in the small will continue to be an attractive technique in industry. One methodology which builds on this investment is that of globally asynchronous, locally synchronous (GALS) systems where asynchronous communication techniques are used for long distance communication between individually clocked subsystems.

## 2. Globally Asynchronous, Locally Synchronous Systems

Globally Asynchronous, Locally Synchronous (GALS) systems may offer a solution for system on a chip implementors seeking good performance and low power consumption [6]. Clocked building blocks can be integrated onto one chip with independent clocks for each block and an asynchronous interconnect between them.

Synchronising to asynchronous data is a well known problem which can be crudely resolved by latching the data at least twice to allow time for metastability in the latches to resolve. This does not prevent metastability from propagating, though the chance is small [7]. A more pressing concern is the latency that is introduced by this scheme.

An alternative strategy is to stretch the clock when there is a risk of metastability [11, 13, 3, 2, 14, 16, 10]. Such a scheme relies on generating the clock from a delay line because such a clock is simple to stop by gating the clock



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pulse. Self calibrating delay lines may be used to provide an accurate timing reference [5].

In this paper we describe a reliable, low latency and high bandwidth channel communication mechanism which may be positioned between independently clocked synchronous domains. The channel itself relies on asynchronous logic techniques.

To assist explanation, the design is divided into several parts. Section 3 describes our mechanism for reliable data transfer between an asynchronous producer (the output of the asynchronous channel) and a synchronous consumer. Section 4 discusses the synchronous producer which sends data to the asynchronous channel. Section 5 combines these two parts and Section 6 looks at additional decoupling and other techniques required to maximise bandwidth. Section 7 presents a variation in which the producer/consumer can enter 'sleep mode' with the clock stopped. Simulation results are then presented and conclusions drawn.

## 3. Asynchronous producer, synchronous consumer

Figure 1 presents an interface between an asynchronous producer and a synchronous consumer which is based on our earlier work [8, 9]. When no data is being presented, the output clock (`clkB`) is inverted and then fed to a calibrated delay line [5] and to one input of an arbiter. The arbiter then grants in the favour of the clock circuit and is merged with the output from the delay line. This oscillatory process continues and a stable clock signal is produced. Examples of how delay lines may be constructed from standard cells are provided in the Annex.

Data from the asynchronous producer is signalled by a transition in the `req` signal (see Figure 2); the point-to-point channel uses a two-phase signalling scheme. This will result in the arbiter granting in the favour of the asynchronous interface when the clock (`clkB`) is high. If the clock falls and `req` changes around the same time then the arbiter may go metastable. This is safe since the arbiter guarantees that the clock cannot continue and the input `req` signal can not be propagated until the metastability has resolved.

Once the arbiter grants in favour of the input request (`req`), data is latched which in turn releases the hold on the arbiter. Now that the data has been latched, it is safe for the synchronous consumer to be presented with a rising clock edge which latches the incoming data in the final set of latches. The incoming `req` signal is also latched in the final set of latches which is also fed-back as an acknowledge signal.

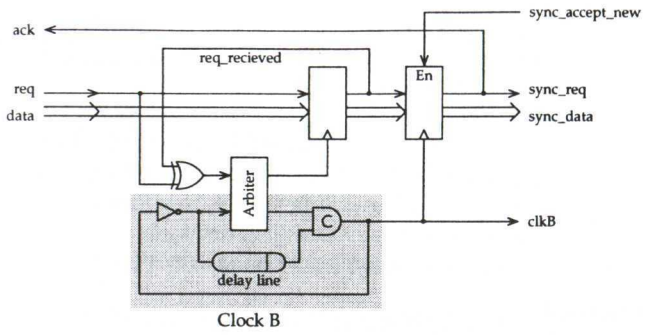



**Figure 1. Interface between an asynchronous producer and a synchronous consumer**

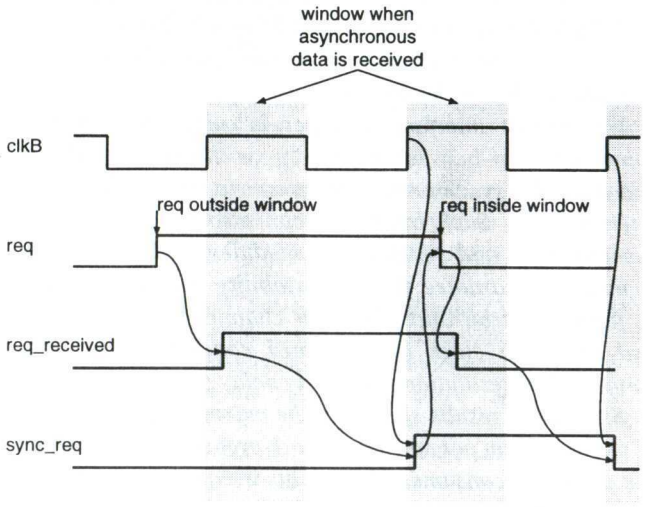



**Figure 2. Request in to request out traces**

## 4. Synchronous producer, asynchronous consumer

Transmitting data from the synchronous domain to the asynchronous domain requires that the synchronous system knows when the asynchronous domain is able to accept data. Thus, the primary difficulty is safe transfer of this control signal from the asynchronous domain to the synchronous one. Therefore, the circuit we require (see Figure 3) is similar to the asynchronous producer, synchronous consumer circuit described in the previous section. The relationship between the incoming asynchronous acknowledge (`ack`) and the outgoing synchronous acknowledge (`sync_ack`) in Figure 4, is identical to the request (`req`) and synchronised request (`sync_req`) presented in Figure 2.

The only difference is the transmission of data from the synchronous world to the asynchronous world. A



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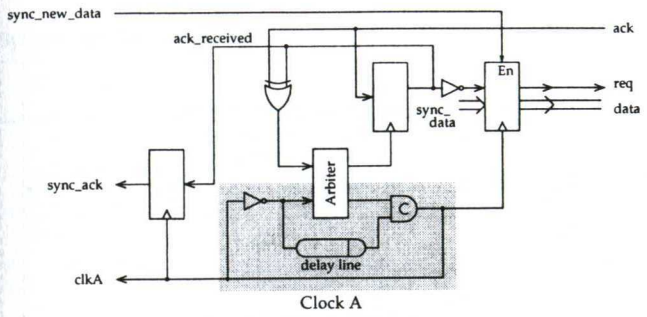



**Figure 3. Interface between an synchronous producer and an asynchronous consumer**

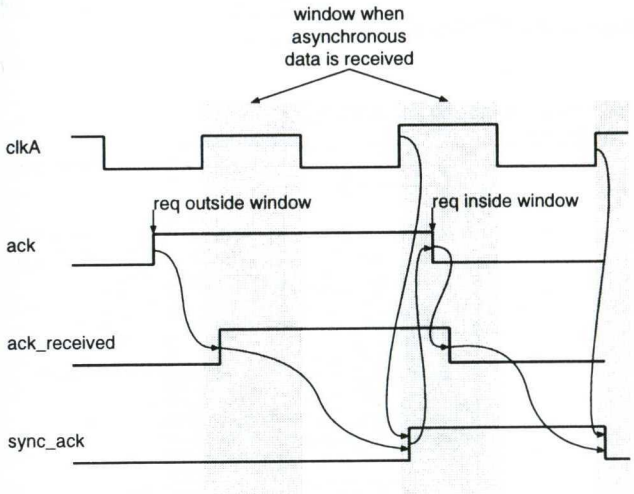



**Figure 4. Acknowledge in to Acknowledge out traces**

2-phase request signal is bundled with the data to indicate to the asynchronous system that new data is available. Provided the synchronous state machine always waits for an `sync_ack` between sending data items, the `req` will always toggle and data will be sent correctly.

## 5. Channel communication with no buffering

The circuits from the previous two sections may be concatenated together to form a simple asynchronous communication channel between two clocked domains. However, as can be seen from Figure 4, the synchronous producer will have to wait at least one clock cycle between sending data and receiving a corresponding `sync_ack` signal. This will limit the bandwidth to a maximum of one data item every second clock cycle. The average bandwidth is typically worse than this because the outgoing `req` has to pass right through the consumer control logic, back out via `ack` and back through control logic in the producer before `sync_ack` is seen.

## 6. Channel communication with buffering

Adding an asynchronous FIFO between the producer and consumer (see Figure 5) decouples the `req`→`sync_ack` path. This allows the producer to reliably send one data item every second clock cycle.

For the producer to be able to transmit a data item every clock cycle we have to make the following assumption: if the first element of the FIFO is empty then any data emitted by the synchronous producer will be safely stored before the next clock cycle. This is a very safe timing assumption. From this assumption it is clear that in place of the `ack` signal from the FIFO we require a *input element of FIFO is empty* signal which we will call `consumed`.

This new scheme is presented in Figure 6, with two-phase to level sensitive conversion of `sync_req` and `sync_consumed` now explicitly shown. The synchronous producer may generate new data every time there is an outgoing transition on `req`. If the FIFO becomes full then no `consumed` will be received from the FIFO which in turn means that no `req` will be produced. Under this condition, data must be held in the output latch by deasserting the enable signal on this latch.

## 7. Variation with sleep mode

For some applications it may be desirable for the synchronous consumer to enter a sleep state with the clock stopped until new data input arrives.

Figure 7 shows an extension of the circuit from Figure 1. A second arbiter is inserted to permit the clock to be stopped; note that both arbitrations are concurrent and that the upper grant output of the additional arbiter is not required. When the synchronous consumer wishes to sleep it raises `sync_sleep` causing the clock to stop. The XOR clears the now set DFF once new data has been latched by the interface. The DFF could be replaced with an SR latch where reset has priority. This circuit extension is also applicable to the high-bandwidth variation from Figure 6.

A similar arrangement applies for the producer, shown in Figure 8. Here the synchronous producer can request to sleep until the previously sent data has been read.

## 8. Multiple interfaces

A GALS block with more than one input/output interface can be constructed by adding additional arbiters in parallel. The single arbiter is replaced with multiple aribters, see Figure 9 and an AND gate, much like the scheme used in



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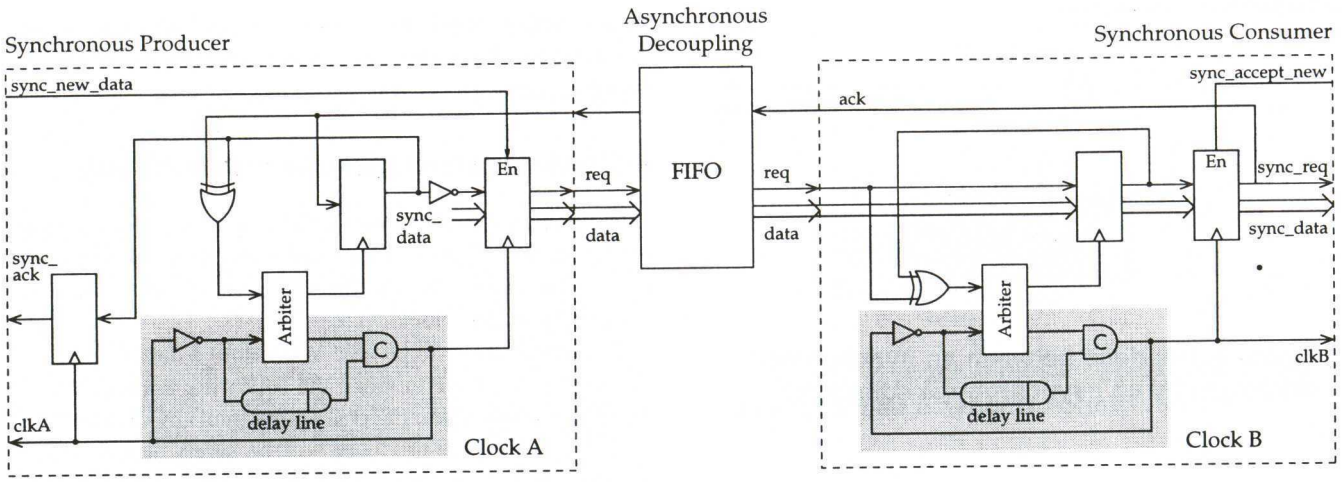



**Figure 5. Channel communication with FIFO buffering**

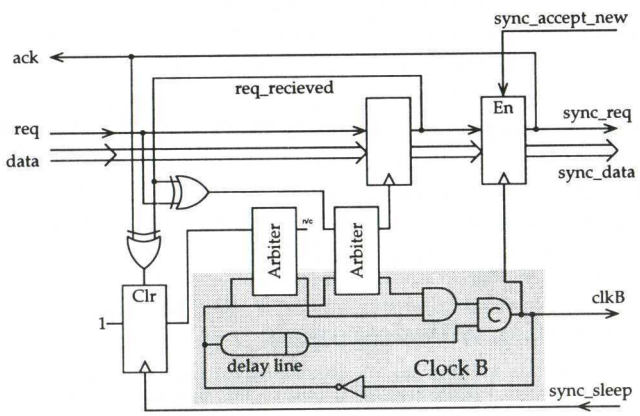



**Figure 7. Synchronous consumer interface with sleep feature**

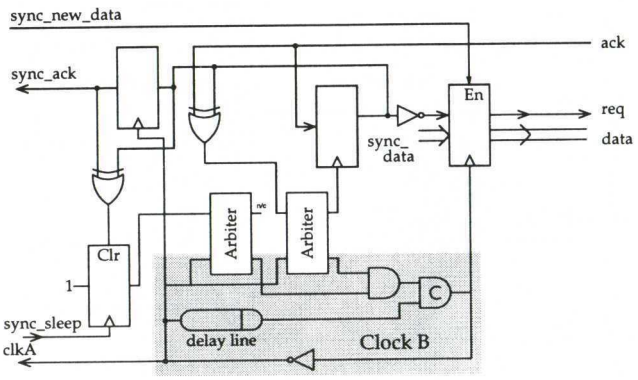



**Figure 8. Synchronous producer interface with sleep feature**

Section 7. Each arbiter arbitrates between a GALS interface and the single clock generator. Such a scheme permits multiple data items to be input or output in each clock cycle, albeit with an increased probability of the clock being paused.

## 9. Results

Simulations were performed using Verilog with SDF annotation using the VST/UMC 0.25$\mu$m timing library with wireload model. The consumer runs at a fixed frequency of 50MHz, the producer at a varying frequency up to 200MHz, obviously higher frequencies are possible depending on the complexity of the producer and consumer.

We tested the simple control scheme (Figure 5) for various FIFO depths. When the FIFO is of size zero, it corresponds to the circuit in Figure 5 with the FIFO removed. The detailed simulations were undertaken and the bandwidth measurements are shown in in Figure 10. Making the FIFO more than two slots long does not improve performance further.

The more complex control scheme (Figure 6) requires a FIFO depth of at least two items. However, making the FIFO deeper does not improve performance further. The bandwidth results are presented in Figure 11.

The calibrated delay line and arbiter to stop and start the clock has been fabricated on a 0.35$\mu$m process. In this test a 25-80MHz clock is produced using a 32kHz watch crystal as a calibration reference, calibration takes place once per second. This clock has been successfully used to clock both a 16 bit microcontroller and a UART serial interface. A revised version with finer adjustment steps has

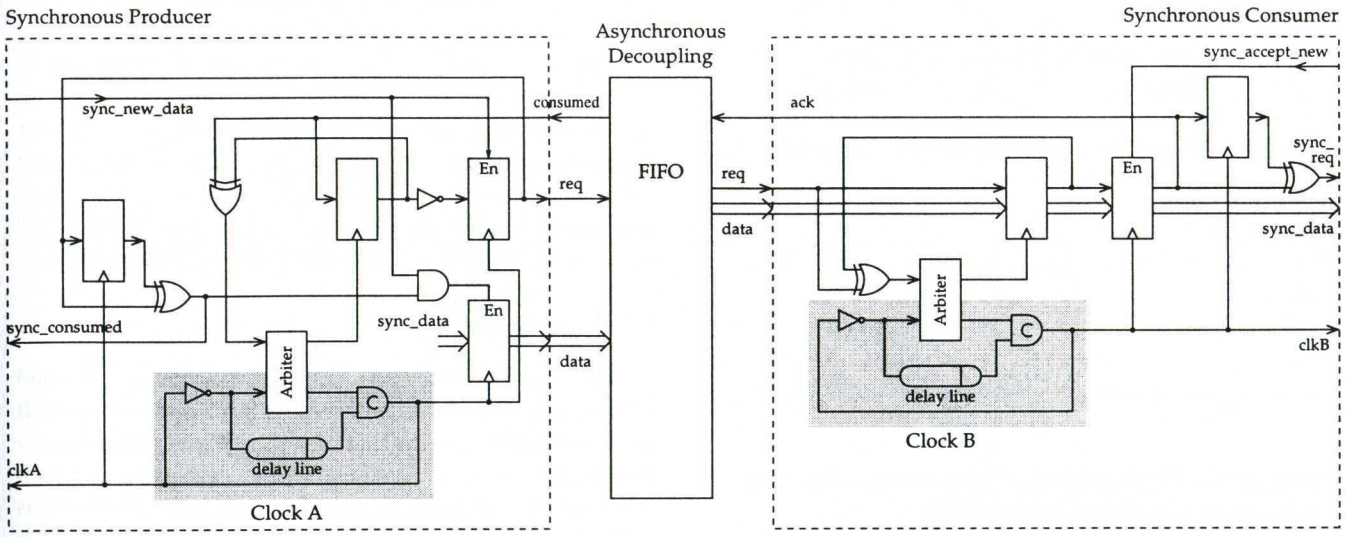



**Figure 6. High bandwidth channel communication scheme**

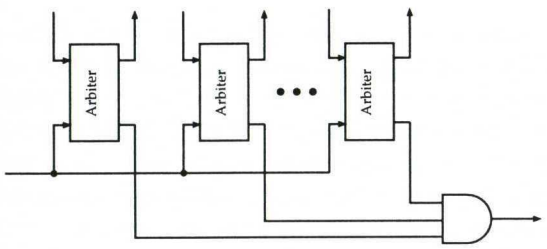



**Figure 9. Concurrent arbiters**

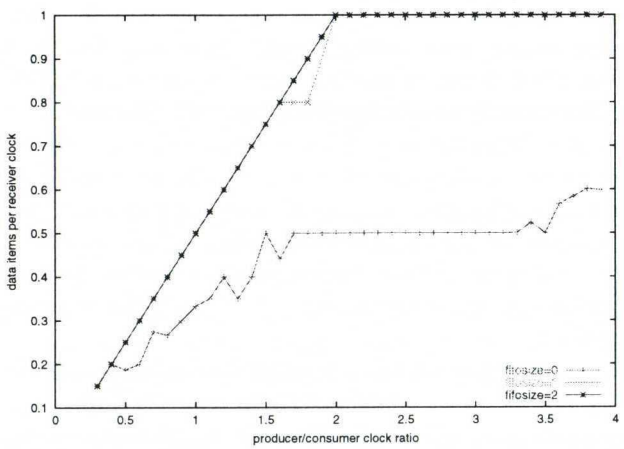



**Figure 10. Throughput of simple channel as FIFO size varies**

been submitted to a 0.18$\mu$m process.

## 10. Review

It is worth noting that some special cases of the GALS interface exist where arbitration is not required.

Case 1—Asynchronous consumer always ready and synchronous producer: Here the synchronous producer simply sends a request and data to the consumer. No acknowledge from the consumer is used. Arbitration and clock pausing are not required. Typically a consumer would always be ready if there was only one input port and it could consume the data within the producer clock cycle. An example of this is a memory device.

Case 2—Asynchronous producer always able to produce data and synchronous consumer: This is the converse of case 1. Arbitration and clock pausing is not required, the consumer clocks data out of the asynchronous FIFO.

Case 3—Synchronous producer and slave consumer. Here the synchronous producer clock pauses until the consumer has acknowledged receipt of the data and returned any response, for example a microcontroller accessing a slow delay-matched memory. Clock pausing is required but not arbitration. A similar principle can be used to embed asynchronous modules inside an otherwise synchronous pipeline [14]. Additionally [14] discusses the impact of the clock buffer insertion delay which we have not addressed here.

So far GALS interfaces with zero probability of failure have been discussed, however, this is at the expense of clock pausing, possibly with arbitration. Additionally failure to meet a timing deadline due to metastability resolution may be considered a failure in some real-time systems.



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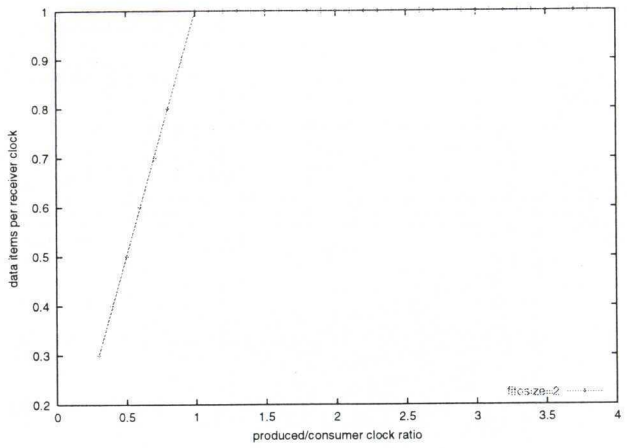



**Figure 11. Throughput of fast channel for the minimum sized (two item) FIFO**

An alternative is to use two cascaded registers for synchronisation but instead of synchronising the data synchronising some control signals indicating the state of the FIFO between producer and consumer [4]. This permits truly free running clocks and the probability of synchronisation failure is linearly reduced by reducing the number of synchronisations without reducing bandwidth. During continuous steady-state data transmission the probability of synchronisation failure is zero, however, such a state may be hard to maintain. This scheme involves extra latency and a startup cost when the FIFO becomes empty.

Each GALS block has a bundled data interface and the delay line for the local clock delay matches the worst case combinational logic path within the synchronous block. This could be viewed as a coarser scale version of standard bundled data design, where a unique delay is used to match the worst case path in each of many small combinational logic blocks. Design styles with even more localised delay assumptions include IPCMOS [12] which uses a pulse generator to strobe latches, and GASP with self-reset [15].

The GALS methodology is well suited to other asynchronous interconnect methods. For simplicity, in this paper bundled data has been used, the request signal is bundled with the data and is assumed to not arrive earlier than the data. Such a scheme is unable to exploit the widely varying data dependent delays for data transmission. At the extreme case, compare one bit going high whilst the others go low with all bits changing in the same direction.

Alternative interconnect could use dual-rail or one-of-four encoding. Such interconnect is truly self-timed, the consumer is able to proceed as soon as data arrives. For large interconnect capacitances the one-of-four encoding scheme offers half the transition power and a lower latency that the bundled and dual-rail schemes [1]. The GALS interface structure would remain the same with the consumers request input supplied from the interconnect completion detection logic. Further bandwidth improvement might be achieved by adding FIFO stages and distributing these between the producer and consumer. Finally it should also be possible to apply the GALS principle to a bus rather than point-to-point link.

## 11. Conclusion

We have presented an asynchronous channel communication mechanism which allows low latency, high bandwidth and reliable data transfer between independently clocked synchronous domains. This mechanism could form the basis of a globally asynchronous, locally synchronous (GALS) chip-level architecture in order to meet the challenges of deep sub-micron CMOS design.

## Annex: Delay line circuits

To achieve a very fine adjustment in the delay our delay lines are composed of two sections, fine and coarse adjustment sections. This is a variation of a previous scheme [8] where fine and coarse adjustment were integrated. The idea is that the fine delay section provides a total delay range of about one delay step in the coarse delay section. This scheme is shown in Figure 12.

The coarse delay line is based upon blocks of inverter delays and a binary scheme, see Figure 13. The fine delay adjustment step requires to be smaller than a normal standard cell gate delay, two possible methods are given here. The first, shown in Figure 14, exploits changing the pull-up resistance in a simple AO gate shown in Figure 15. The second involves having a number of tristate buffers in parallel, the more of which are enabled, the higher the drive strength and thus shorter the delay.

Adjusting the coarse delay should only be performed whilst the clock is stopped and the delay line contains logical zeros, otherwise an extra pulse might be inserted in the feedback ring. Various versions of these delay lines have been included on a 0.18$\mu$m test chip submitted for fabrication.

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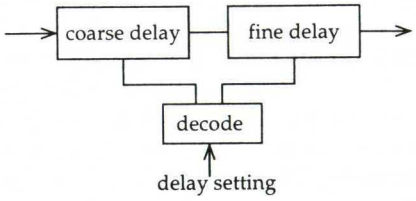



**Figure 12. Block view of delay line**

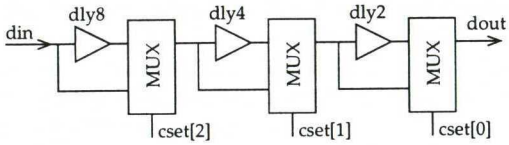



**Figure 13. Coarse section**

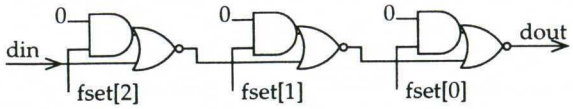



**Figure 14. Fine adjustment: AO gate version**

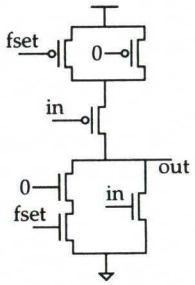



**Figure 15. AO gate**

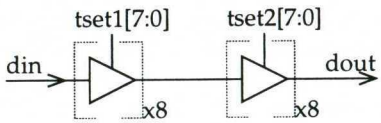



**Figure 16. Fine adjustment: Tristate version**

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# PROCEEDINGS






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# A SOCKET INTERFACE FOR GALS USING LOCALLY DYNAMIC VOLTAGE SCALING FOR RATE-ADAPTIVE ENERGY SAVING

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## ABSTRACT

*A low-power amendment to the globally-asynchronous, locally-synchronous paradigm (GALS) is presented. A proposed socket interface provides locally dynamic voltage scaling (LDVS) adapted to the actual processing rate requirements for each module. Local clock generation by ring oscillators tracks the local device speed at the local supply voltage. Asynchronous I/O handshakes provide the elasticity required to permit the substantial intra-die delay variations present in low voltage, deep sub-micron digital designs to give high yield. By the proposed socket interface, synchronous design methodology can be continued at module level including use of industry standard HDL-based synthesis tools, while module reuse and system design can be substantially simplified.*

## I. INTRODUCTION

*Synchronous* design and test methodology is mandatory in current industrial quality ASICs and SoCs. State-of-the-art HDL-based verification, synthesis, layout and test tools efficiently support the synchronous design flow, while new methodologies and standards emerge for designing reusable cores to increase the design productivity. Synchronous design methodology has several proven qualities and has come to stay. However, as the semiconductor technology scales down and complexity increases, fully synchronous designs will eventually not be feasible on the chip level. For increased design productivity, simplified system design, higher yield, lower energy consumption and higher performance, it is imperative to depart from the *fully* synchronous chip design paradigm, and replace it with a globally-asynchronous locally-synchronous paradigm (GALS). As will be discussed below, the GALS principle and the voltage scaling principle, may join forces to provide the required performance at minimum energy for each module, locally adapted to actual process parameters and temperature. Low-voltage digital deep sub-micron designs suffer from intra-die parameter variations, i.e. substantial delay variations over the chip [6]. The asynchronous handshake mechanisms between the modules in GALS represent the elasticity and the encapsulation required to design and optimize each module separately, in contrast to the fully synchronous design paradigm which ultimately requires chip level timing optimization.

The paper is organized as follows: In the first part, we review the Semiconductor Industry Roadmaps from 1994, 1997 and 1999 regarding their predictions about design methodology, to identify a sudden breakthrough for the GALS concepts in the 1999 Edition. Then, the GALS concept from its origin in the 1960s to more recent contributions is briefly reviewed. Furthermore, various aspects of the application of the voltage scaling principle are discussed, including validation of a performance model at gate and module level, and a discussion concerning intra-die delay variations at low voltage supplies.

In the second part, we present key elements of the Socket Interface concept, proposed and established in the WIRAC research project [7]. The Socket Interface supports GALS and module level local dynamic voltage scaling (LVDS) to provide rate-adaptive energy saving, while continuing to adhere to the established synchronous HDL-based synthesis design flow at module level. Finally, we identify obstacles and future challenges towards the implemention of the proposed Socket Interface.

## II. MOTIVATION FOR GALS

### A. The 1999 Roadmap urges development of GALS methodology.

Four years ahead, in year 2005, the expected on-chip global clock rates are approaching 3 GHz in ASICs and SoCs. The switching time of the fastest buffered global signal will be more than 100 times higher than the gate delay, thus fully synchronous operation on-chip will be very challenging and will imply multi-cycle latencies in the interconnect, according to 1999 ITRS Roadmap [9].


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The previous roadmaps have *not* been discussing such design issues. While concerning several researchers at that time [17], the increasing gap between interconnect delay and gate delay related to scaling was not an issue in the first 1994 SIA Roadmap, even though it was indeed well-known, e.g. by the book of Bakouglu [16] in 1990. Moreover, the 1997 edition just briefly compared interconnect delay and gate delay, only to address the need for interconnect technology improvements without discussing future design obstacles for the fully synchronous design paradigm.

However, the 1999 ITRS edition imperatively expresses both short-term and long-term needs for design methodology and tools to cover asynchronous, multi-cycle paths as well as locally synchronous, high-performance near-neighbor communication. The ITRS editions are based on concensus within the leading industry experts and the research community world-wide. Therefore ITRS' recognition of the globally-asynchronous locally-synchronous (GALS) design paradigm definitely is a strong incentive to further and enforced research on related GALS design methodology and tools.

### B. The renaissance of self-timed locally synchronous regimes with stoppable clocks.

The idea of self-timed locally synchronous modules with stoppable clocks dates back to the 1960s with several design projects conducted by Charles L. Seitz [18]. The GALS concept was the topic of the PhD Thesis of Chapiro in 1984 [10], and several contributions have since then been reported, among them [11][12][13][14][15].

When Seitz back in 1980 [18] discusses local stoppable clocks and stretchable clocks, it is interesting, from a technological and historical point of view, that his motivations are strikingly relevant to the design challenges of *this* decade's complex ASICs and SoCs:

- Global clock distribution with problems related to skew limitations and electromigration. By means of such local clocks, these problems will be significantly reduced.
- Performance spread and yield problems due to variation in process parameters, aging, temperature and supply voltage. Seitz argues for using local ring oscillators as clock sources, since "on the same piece of silicon these variable factors are nearly the same for the clock and for the system".
- Design complexity management. Seitz' self-timed locally synchronous modules with asyncronous communication encapsulate and hide details of the underlying physical implementation, which is not relevant to the system architects. By such design abstraction "free of hidden rules", Seitz introduces a system design domain similar to that of a programmer, called the sequence domain abstraction. This is in many aspects relevant to today's discussion about increasing the design reuse to meet the productivity gap and time-to-market requirements, and the need for new abstraction levels to manage complexity.

### C. Current GALS methodology research.

Today, several research groups work on complete design methodology for globally asynchronous on-chip communication networks [12][13][14][15][23], which may connect both locally-synchronous and entirely asynchronous modules. Muttersbach *et al* [14] give a very clear overview of GALS, present problems to be solved, and propose solutions very instructively.

## III. MOTIVATION FOR GALS-LDVS

Digital design for low power consumption by using low supply voltages was exploited already in the 1970s in digital wrist-watches [21]. In the 1990s, however, design methodology to reduce power consumption was systematically reviewed and enhanced by Chandrakasan and Brodersen [1], among several others. Several researchers argued for utilizing the voltage scaling principle leading to a quadratic reduction in energy per operation, and to treat actual supply voltage as a design variable [1][2]. Use of complete systems with variable supply voltages has been demonstrated in academia, e.g. [8][19][20]. Recently, voltage scaling is introduced in several consumer products for mobile computing based on e.g. Transmeta's Crusoe microprocessor [26].

### A. The performance model for voltage scaling applied at gate level and at module level.

As shown in Figure 1, we have validated by measurements on several test chips [5] that the simple model of delay vs. supply voltage [3] given by $t_{pd} = k \cdot V_{dd}/(V_{dd}-V_t)^{\alpha}$, with $\alpha = 1.55$ for the AMS 0.8 µm process, is quite accurate for simple CMOS inverters. It is also rather accurate for various cells using different circuit techniques, if increased threshold values due to the body effect of stacked devices are used.

Since digital systems are collections of such cells, one may expect that the inverse of the delay model can be applied as a model for performance versus supply voltage. We have demonstrated the validity of this performance model at module level [5] as shown in Figure 2, by scaling and overlaying the performance model to the plot of measurements of maximal sample rate vs. $V_{dd}$ from [22] of complete digital filters functions, implemented in the 0.8 $\mu$m AMS technology, and where we have used $\alpha = 1.55$ as above. Kai Chen and Chenming Hu have reported $\alpha = 1.3$ to be valid for

subhalf-micrometer MOSFET's for a wide range of technologies from $L_{eff}$ = 0.4 $\mu$m down to $L_{eff}$ = 0.1 $\mu$m [4].

**B. The justification of using ring oscillators as local clocks.**

The performance model is strikingly accurate, and is a clear justification of the principle of using a ring oscillator as clock source, since the cells in the ring oscillator follow the same delay model as the complex module itself. Some special functions, like certain sense amplifier topologies used in RAM, do not follow this performance model, and have to be characterized carefully, or must be completely avoided if the performance model is applied at the module level.

**C. Extended voltage scaling for reducing the local speed vs. global speed mismatch.**

Liu and Svensson [2] even suggests more aggressive voltage scaling as a means to alleviate the mismatch between the MOS device speed and the global signal speed, since this

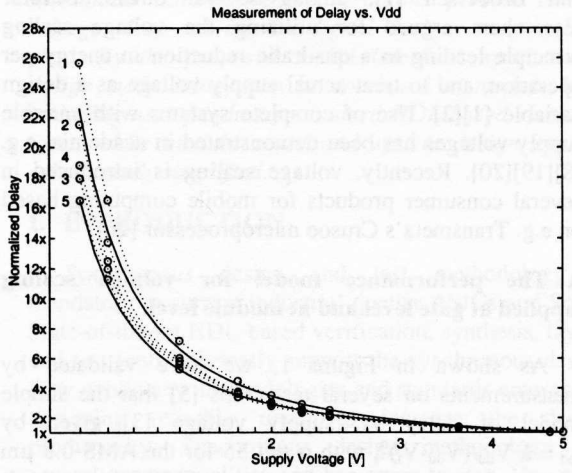



Figure 1: Validation of the delay model at cell level. Dotted line curves: Measured delay vs. supply voltage for different circuit techniques (5 = CMOS inverter chain). Lower solid line curve: delay model with no body effect (inverters). Upper solid line curve: Delay model with increased threshold voltages (due to stacked devices) [5].

mismatch increases dramatically due to the technology scaling.

In this way synchronous design methodology can be utilized further, without need for special high speed interconnect since the clock rate is lower, while parallelism may compensate for degraded performance due to voltage scaling.

**D. Low voltage means increased delay sensitivity and intra-die delay variations.**

By reducing the supply voltage the delay is increased, while the energy per operation is quadratically reduced. However, an unwanted side effect of voltage scaling is that delay sensitivity to process parameter variations, temperature and supply voltage fluctuations increases substantially. The required design margins are dramatically higher, compared to designing at conventional supply voltages [2][6]. Furthermore, intra-die variations can not be ignored. Highly pipelined designs, and designs with a large number of critical paths and with a small logic depth are most sensitive to uncorrelated gate delay variations in state-of-the-art and future technologies [6]. Supply voltage regulation techniques can be used to compensate for process parameter variations for maintaining given throughput performance requirements, but this implies ultimately *local* supply voltage regulation mechanisms to track intra-die variations.

## IV. THE PROPOSED SOCKET INTERFACE

As a part of the Wideband Radio Access project WIRAC [25], supported by the Norwegian Research Council's Basic Telecommunication Research Programme, we have studied implementation issues concerning low-power digital design and digital signal

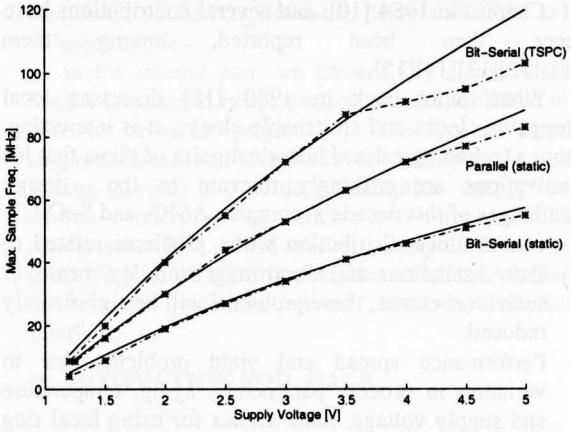



Figure 2: Validation of the performance model at module level. Dotted line curves: Test chip measurements of maximal sample rate of three different wave digital filter architectures [22]. Solid line curves: The performance model, expressed as the inverse of the simple delay model with $\alpha$ = 1.55, (scaled to the measured values at 3 V), see [5].

processing in wireless terminals [27]. Before presenting the Wirac's Socket Interface as a general vehicle for



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implementing rate-adaptive energy-minimal systems by means of state-of-the-art HDL-based synthesis design flow, we will discuss key elements in multiple supply voltage systems and present some results and conclusions from test chip measurements.

### A. A model of an integrated radio access system

An integrated digital tranceiver may be partitioned as in Figure 3, where all the modules with their individual performance and latency requirements are clustered into separate supply voltage regions, thus giving potentially the lowest energy per operation while satisfying the performance requirements. The different regions are communicating through logic level shifters, as presented below.

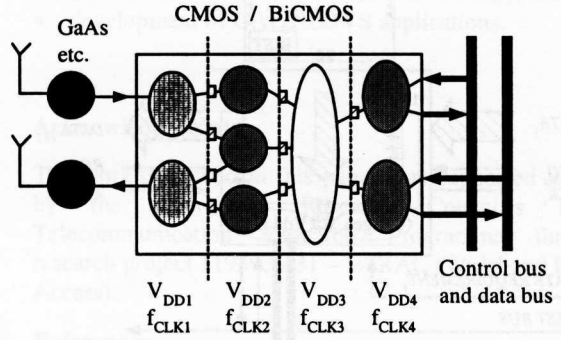



Figure 3: A model of a wideband radio access system using multiple supply voltages and logic level shifters.

### B. Characterization of the level shifter cell.

We have evaluated different logic level shifter topologies. The well-known topology reported by Vittoz in 1977 [21], and utilized in [1], based on cross-coupled PMOS devices, was chosen due to its circuit and conversion symmetry. The cell was characterized by test chip fabrication and measurements in 0.6 µm AMS technology, showing good agreement with simulation results. The topology was also simulated in 0.5 µm and 0.35 µm processes from Alcatel Mietec. Such level shifter translates a logic "1" between two regions of different supply voltages $V_{dd1}$ and $V_{dd2}$.

Table 1: Delay measurements of an inverter (INV) and a level shifter (LS).

| $V_{dd1}$ [V] | 0.9 | 1.0 | 1.1 | 1.3 | 1.5 | 1.7 | 2.2 | 2.7 | 3.3 |
|---|---|---|---|---|---|---|---|---|---|
| $t_{LS}$ [ns] | 83 | 22 | 9.6 | 6.8 | 6.1 | 5.9 | 5.5 | 4.7 | 4.8 |
| $t_{INV}$ [ns] | 252 | 37 | 12 | 3.4 | 1.8 | 1.2 | 0.7 | 0.5 | 0.4 |
| $t_{LS}/t_{INV}$ | 0.3 | 0.6 | 0.8 | 2 | 3.4 | 4.9 | 8.4 | 10 | 12.9 |

Table 1 shows the propagation delay $t_{LS}$ of a level shifter (LS) which translates an input swing of $V_{dd1}$ to output swing $V_{dd2}$ = 3.3 V, compared to the delay of an inverter $t_{INV}$ at $V_{dd1}$. The delay of the LS is 0.3 – 2.0 times the delay of an inverter for low voltages $V_{dd1}$ = 0.9-1.3 V.
Table 2 shows that the energy $W_{LS}$ per level shifting operation (from $V_{dd1}$=1.1V to $V_{dd2}$) is about 2 times that of an inverter $W_{INV}$ supplied by the highest supply voltage $V_{dd2}$. Thus, level shifting from a low voltage $V_{dd1}$ to a high voltage $V_{dd2}$ represent a delay cost (calculated at $V_{dd1}$) and translation energy cost (calculated at $V_{dd2}$) corresponding to about two inverters in series. In contrast, level shifts from high to low voltage do not require level shifters, but can always be performed directly by an inverter or buffer supplied by the low supply voltage.

Table 2: Measurements of energy per operation of an inverter and a level shifter (LS).

| $V_{dd2}$ [V] | 1.3 | 1.5 | 1.7 | 2.2 | 2.5 | 2.8 | 3.1 | 3.3 | 4.0 |
|---|---|---|---|---|---|---|---|---|---|
| $W_{LS}$ [pJ], energy per LS op. | 0.22 | 0.35 | 0.45 | 0.73 | 1.1 | 1.4 | 1.8 | 2.2 | 3.7 |
| $W_{INV}$ [pJ], energy per INV op. | | | | 0.37 | | | | 0.87 | |
| $W_{LS}/W_{INV}$ | | | | 2 | | | | 2.2 | |

### C. Means to generate different local supply voltages

From above, we have concluded that the cost of level shifters is not an obstacle for introducing a multiple-supply voltage methodology. However, regulating and distributing different supply voltages to the different regions in Figure 3 are regarded as more challenging. Different scenarios have been considered:

1. Almost all modules of the chip run at a fixed low supply voltage to minimize power consumption. Parallel processing is utilized to fulfill the performance requirements, as described by [1]. Some very few modules related to the analog front-end, minimum latency DSP functions and fast i/o interfaces require higher supply voltages. The higher supply voltage level may be generated by voltage doublers or triplers. Voltage doublers were already used in commercial wrist-watches in the 1970s [21]. Favrat *et al* [7] have described efficient voltage doublers with external or fully integrated capacitors. We have studied their proposed topologies to specify and design an on-chip dynamically programmable generator to provide local supply voltage of 1x, 2x or 3x of the low input supply. No test design chip has yet been fabricated.
2. Two or more different supply voltages are available


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and distributed on-chip, while the actual supply voltage for each module can be selected by means of DC switches, i.e. large transistors with low $R_{DS(ON)}$. This method is considered to be a viable alternative to the dynamically programmable generator described above, but performance degradation due to IR drop, and other practical aspects of this method, have to be studied further.

3. DC/DC buck converters like in [1][8][20][24] can provide finer regulation of the supply voltage than the two methods above, but require large external components for the low-pass filter [24], so they are not suited for several locally controlled on-chip voltage supply generators.

The candidate methods for local supply voltage generation should be explored further including their suitability for future technologies, because it is only by local supply voltage selection rate-optimal energy saving can be attained.

### D. Data-flow oriented processing

Typically in many signal processing system, e.g. as in Figure 3, many tasks are performed at a fixed rate (or at a temporally fixed rate). Each processing element or complex module, see Figure 4, receives an input data set and produces an output data set at this fixed rate. The input and output data sets may be passed along with handshake signals which implement some given protocol, such that e.g. the processing does not start before the module has input data ready. The fixed rate requirement or the fixed average rate requirement can dynamically be configured, by the special control signal *RATE-REQUIREMENT*$_i$. From a system point of view, faster operation of the processing element than given by the rate requirement does not give any better system performance, while slower operation than the requirement can of course not be tolerated. We have

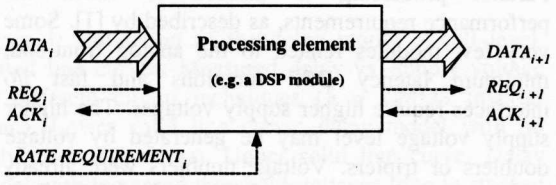



Figure 4: The prosessing element (e.g. a DSP module) executes its calculations fast enough to satisfy the actual performance requirement.

encapsulated all implementation details in the model in Figure 4. In Figure 5 some of the hidden details are revealed. The control signal *RATE-REQUIREMENT*$_i$ can be used to scale down the local supply voltage such that the locally generated clock rate is just high enough to perform the actual processing task and to produce output data at the given rate. The energy per operation will therefore be regulated to the lowest possible value for the actual rate-requirement, the given technology parameters and temperature, since the local clock is generated by a ring oscillator which tracks these local conditions.

Furthermore, the number of clock periods required per processing operation can be predefined, and the local clock can be stopped after the operation is performed. By stopping the clock when no data processing is performed, the power consumption will be further reduced. The clock stopping control circuit will, however, include e.g. counters which represent some contribution to the power consumption.

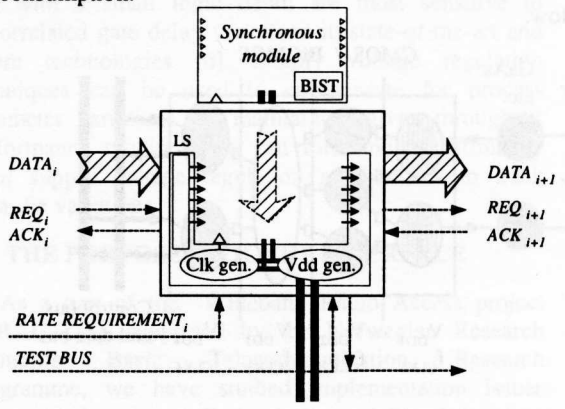



Figure 5: A synchronous version of the actual prosessing element (DSP module) is inserted into the Socket Interface.

The synchronous module in Figure 5 can be generated by state-of-the-art HDL-based synthesis tools including built-in self-test support, and can be "inserted" into the Socket Interface. The socket interface provides level shifting of all data inputs to convert from the low voltage data signals outside the socket, to the module's actual supply voltage level.

A clock signal with the correct frequency given by the logical depth of the synchronous module and by the actual supply voltage level, is active for a predefined number of clock periods for the actual task. The synchronization tasks related to the asynchronous interfaces can be performed as proposed by [14].

## V. CONCLUSION

We have described GALS-LDVS, a low-power amendment to the GALS paradigm where locally rate-adapted dynamic voltage scaling can be provided by means of the proposed Socket Interface. Local clock generation by using local ring oscillator tracks the local device speed. The module's speed is proportional to the



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device speed with the same dependence of local power supply level, process parameters and temperature variations. Asynchronous I/O handshakes support the elasticity required to permit low voltage intra-die delay variations, thereby increasing the performance yield.
By exploiting the proposed methodology, synchronous design and HDL-based synthesis flow support can still be advocated, and design reuse and system design can be substantially simplified.

Further research will focus on

- fail safe synchronization methods [14] when voltage scaling is applied,
- generation and regulation of local supply voltages,
- utilization and enhancements of synthesis tools and layout generator tools to support the proposed Socket Interface for the GALS-LDVS methodology, and
- development of GALS-LDVS applications.

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# EXHIBIT E

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