

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TCL Electronics Holdings Ltd. And TCL Industries Holdings Co., Ltd.,
Petitioner,

v.
Intellectual Ventures I LLC,
Patent Owner.

IPR No. IPR2024-01245

Patent No. 7,089,443
Filing Date: January 23, 2004
Issue Date: August 8, 2006

**DECLARATION OF DR. DAVID KAEI IN SUPPORT OF
PATENT OWNER'S PRELIMINARY RESPONSE**

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I. Introduction And Qualifications

1. I, David Kaeli, submit this declaration on behalf of Intellectual Ventures (“Patent Owner”) to provide my opinions concerning the validity of claims 1, 3, 4, 5, 8, 10 and 12 (the “Challenged Claims”) of U.S. Patent No. 7,098,443 (the “’443 patent,” Ex.1001), in support of Patent Owner’s Preliminary Response to the Petitioner for *Inter Partes* review of the ’443 patent, which I understand was filed by TCL Electronics Holdings Ltd. And TCL Industries Holdings Co., (“TCL”, the “Petitioner”) and accompanied by a Declaration of Dr. Nadar Bagherzadeh (the “Bagherzadeh Declaration”), among other exhibits.

2. I am more than eighteen years of age, and I am a citizen of the United States, currently residing in the Commonwealth of Massachusetts.

3. In formulating my opinions, I have relied upon my knowledge, training, and experience in the relevant art. My qualifications, along with a more detailed summary of my background and publications, are stated more fully in my *curriculum vitae*, which has been provided as Exhibit 2002. Here, I provide a brief summary of my qualifications.

4. I am currently the Director of Northeastern University’s Computer Architecture Research Laboratory and a Distinguished Professor of Electrical and Computer Engineering. I have been a faculty member at Northeastern since September 1993, in the Electrical and Computer Engineering Department.

5. For over thirty years, I have pursued research across a broad range of computer architectures and technologies, including memory systems, storage systems, virtualization, and secure computing systems. I have published over 400 refereed journal and conference papers in the areas of computer architecture and computer security. I also have supervised more than fifty Ph.D. theses in these areas.

6. I am a Fellow of the Institute of Electrical and Electronic Engineers (IEEE) and a Fellow of the Association of Computing Machinery (ACM). I have served two terms as the Chair of the Executive Committee of the IEEE Technical Committee on Computer Architecture. I am serving in my second terms as the Editor-in-Chief of the ACM Transactions on Architecture and Code Optimization. I am also an Associate Editor for Elsevier's Journal of Future Generation Computer Systems.

7. Before I joined Northeastern's faculty in 1993, I spent twelve years working for IBM. From 1981-1986, I worked on the design and delivery of the IBM System/370 3090 mainframe system. From 1986-1993, I worked at the IBM T.J. Watson Research Center, designing, and analyzing IBM Personal Systems 2 computers and associated software. During that time, I also worked on the design of a new Application System/400 multi-processor system.

8. I am an active educator and researcher and have extensive experience in the broader field of computer architecture. I have conducted academic research on, and published multiple papers relating to dynamic voltage and frequency scaling in the context of cybersecurity attacks, as well as energy-efficient microarchitectures. See, e.g., Sabbagh et al., *Overdrive Fault Attacks on GPU*, IEEE/IFIP International Conference on Dependable Systems (2021); Sabbagh et al., *A Novel GPU Overdrive Fault Attack*, ACM/IEEE Design Automation Conference (2020); Tavana et al., *Exploiting Adaptive Data Compression to Improve Performance and Energy-efficiency of Compute Workloads in Multi-GPU Systems*, 33rd IEEE International Parallel and Distributed Processing Symposium (2019); and Ning et al., *Power Aware External Bus Arbitration for System-on-a-Chip Embedded Systems*, *High Performance Embedded Architectures and Compilers* (2005).

9. I have also delivered many tutorials and conducted research in cycle-based simulation methods and technology. See e.g., Sun et al., *MGPUSim: Enabling Multi-GPU Performance Modeling and Options*, *ACM/IEEE 46th International Symposium on Computer Architecture* (2019), Ubal et al., *Multi2Sim: A Simulation Framework for CPU-GPU Computing*, *ACM 21st International Conference on Parallel Architectures and Compilation Techniques* (2012), and Kaeli, *Issues in Trace-driven Simulation*, *IFIP International*

Symposium on Computer Performance Modeling, Measurement and Evaluation (1993).

10. I earned a Bachelor of Science degree in Electrical Engineering from Rutgers University in 1981. I earned a Master of Science degree in Computer Engineering from Syracuse University in 1985. I earned a Ph.D. in Electrical Engineering from Rutgers University in 1992.

II. Summary Of Materials Reviewed And Considered

11. The opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, while drawing on my experience, I reviewed the following documents:

Ex.	Description
1001	United States Patent No. 7,089,443 B2 (“the ’443 patent”)
1003	Declaration of Dr. Nader Bagherzadeh (“Bagherzadeh Decl.”)
1005	Iyer, Anoop, and Diana Marculescu. “Power efficiency of voltage scaling in multiple clock, multiple voltage cores.” Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design (2002).
1006	U.S. Patent App. No. 20030071657 (“Soerensen”)

Ex.	Description
1007	A. Hemani, T. Meincke, S. Kumar, A. Postula, T. Olsson, P. Nilsson, J. Oberg, P. Ellervee, and D. Lundqvist, “Lowering power consumption in clock by using globally asynchronous, locally synchronous design style,” Proc. ACM/IEEE Design Automation Conference, 1999.
1008	Moore, Simon, George Taylor, Bob Mullins, and Peter Robinson. “Channel communication between independent clock domains.” First ACiD-WG Workshop of the European Commission’s Fifth Framework Programme. 2001.
1009	Tormod Njolstad, Odd Tjore, Kjetil Svarstad, Lars Lundheim, Tor O. Vedal, Jukka Typpo, Tor Ramstad, Lars Wanhammar, E. J. Aar, and Helge Danielsen. “A socket interface for GALS using locally dynamic voltage scaling for rate-adaptive energy saving.” Proceedings 14th Annual IEEE International ASIC/SOC Conference (IEEE Cat. No. 01TH8558). IEEE, 2001.
1010	Liljeberg, Pasi, Juha Plosila, and Jouni Isoaho. “Asynchronous interface for locally clocked modules in ULSI systems.” ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems (Cat. No. 01CH37196), IEEE, 2001.
2002	David Kaeli CV
2003	Declaration of David H. Albonesi
2004	Rational Clocking, Sarmenta et al. (“Sarmenta”)
2005	Energy-Efficient Processor Design, Semeraro et al. (“Semeraro”)
2011	SimpleScalar Tutorial

12. My opinions are additionally guided by my appreciation of how a person of ordinary skill in the art would have understood the claims of the '443 patent at the time of the invention, which I have been asked to assume is February 2, 2002. I understand from counsel that this is the publication date for a paper titled "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling" (Semeraro et al., Ex. 2005). I also understand that Column 5, Lines 22-27, of the '443 Patent states: "The following paper describes the invention and is hereby incorporated by reference in its entirety into the present disclosure: Semeraro et al, "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling," High Performance Computer Architecture (HPCA), Feb. 2, 2002." Accordingly, I will use the February 2, 2002 priority date when judging relevant prior art in this discussion.

III. Legal Standards

13. I am not an attorney. However, I have been informed by counsel of certain legal standards and have applied those standards, described below, in formulating my opinions.

14. I understand that the claims of a patent define the limits of a patentee's exclusive rights. I understand that to determine the scope of the claimed invention, courts may construe claim terms, the meaning of which the parties may dispute.

I understand that claim terms should generally be given their ordinary and customary meaning as understood by a person of ordinary skill in the art at the time of filing of the patent application.

15. I understand that claims must be construed in light of and consistent with the intrinsic evidence. In this context, I understand that intrinsic evidence includes the claims themselves, the written disclosure in the specification, and the patent's prosecution history. I understand that the specification is always highly relevant to the claim construction analysis and often is the single best guide to the meaning of a disputed term. I understand that extrinsic evidence may also be considered when construing claims and may include, for example, technical dictionaries, technical publications and books, treatises, and expert testimony, though the intrinsic record will be more persuasive as to the meaning of a particular term.

16. I understand that one or more prior art references can render a patent claim obvious to a person of ordinary skill in the art if the differences between the subject matter set forth in the patent claim and the prior art are such that the subject matter of the claim would have been obvious at the time the claimed invention was made. In analyzing obviousness, I understand that it is important to consider the scope of the claims, the level of skill of a person of ordinary skill in the relevant art, the scope and content of the prior art, the differences between the prior art and the claims, and "secondary considerations" of non-obviousness, which I also

understand can include, for example, evidence of commercial success of the invention, evidence of a long-felt need that was solved by an invention, evidence that others copied an invention, or evidence that an invention achieved an unexpected result.

17.I understand that the claimed subject matter can be obvious when a person of ordinary skill in the art would have been motivated to combine pre-existing elements, and that combination yields no more than what a person of ordinary skill in the art would have expected. I also understand that, in assessing whether a claim is obvious, one must consider whether the claimed improvement is more than the predictable use of prior art elements according to their established functions. I understand that there need not be a precise teaching in the prior art directed to the specific subject matter of a claim because one can take account of the inferences and creative steps that a person of ordinary skill in the art would employ. However, I further understand that obviousness cannot be based on the hindsight combination of components selectively culled from the prior art.

18.I understand that for a reference to qualify as a relevant prior art reference in an obvious analysis, the reference must be “analogous”—meaning it is from the same field of endeavor as the patented technology, and if not, then the reference must be reasonable pertinent to the particular problem facing the inventors of the patent at issue. I also understand that a reference is reasonably pertinent if a person

of ordinary skill in the art would have reasonably consulted those references and applied their teachings in seeking a solution to the problem facing the inventors.

IV. Level Of Skill In The Art And Perspective Applied In This Declaration

19.I understand that certain issues relating to validity must be judged from the perspective of a person of ordinary skill in the art (“POSITA”). I further understand that factors that may be considered in determining the level of skill of a person of ordinary skill in the art include, but are not limited to, (1) the type of problems encountered in the art; (2) prior art solutions to those problems; (3) rapidity with which innovations are made; (4) sophistication of the technology; and (5) the educational level of active workers in the field.

20.I have been informed and understand that a person of ordinary skill in the art is a hypothetical person who is presumed to be aware of all pertinent prior art, thinks along conventional wisdom in the art, and is a person of ordinary creativity. Importantly, this hypothetical person is of ordinary skill in the art to which the claimed subject matter pertains.

21.With respect to the ’443 patent, a person of ordinary skill in the art at the time of the earliest priority date, February 2, 2002, would have been familiar with techniques for techniques that could manage voltage and frequency on a microprocessor, and underlying synchronization technologies used with such techniques.

22. A person of ordinary skill in the art would have had at least a Bachelor's degree in computer science, computer engineering, or a related field, and two years of industry experience or academic research experience on microprocessor design. In my view, more education can supplement relevant experience and vice versa.

23. At the time of the earliest priority date for the '443 patent (February 2, 2002), I met the qualifications to be a person of ordinary skill in the art, and I believe that I also have a sufficient level of knowledge, experience, and education to provide expert opinions in the field of the '443 patent.

24. While my own level of skill exceeded that of the ordinary level of skill as of February 2002, I am well-acquainted with the actual performance and capabilities of a person of ordinary skill in the art as defined above. For example, during the relevant timeframe, I was supervising and evaluating the performance of such individuals, such as my graduate students who were performing research in this area. Furthermore, my participation in professional organizations and in conferences and other events exposes me to the state of the industry and the level of experience of individuals who, like I did, had at least the ordinary level of skill.

25. I have applied the above-defined perspective of a person of ordinary skill in the art, as of February 2002, in forming and expressing my opinions. Unless otherwise stated, my testimony below refers to the knowledge of one of ordinary skill in the art at that relevant time.

26. In the Declaration, Dr. Bagherzadeh sets out the following articulation of the level of ordinary skill:

27. In my opinion, a person of ordinary skill in the art (“POSITA”) at the time of the ‘443 Patent would have at least a Master’s degree in electrical engineering, computer engineering, computer science, or a related field, with at least two or more years of experience in the field of processor design, with more education substituting for work experience and vice versa. I have applied this ordinary level of skill in my analysis, but none of my opinions would change if a somewhat higher or lower level of skill is adopted.

Ex. 1003 (Bagherzadeh Decl.), ¶38. At the time of the earliest priority date for the ‘443 patent (February 2, 2002), I met Dr. Bagherzadeh’s proposed qualifications to be a person of ordinary skill in the art, and my opinions in this Declaration would not change if the Board were to adopt and apply that proposed level of ordinary skill.

V. Claim Construction

28. In my analysis, I have applied the plain and ordinary meanings of the claim terms in the ‘443 patent, as a person of ordinary skill in the art would have understood them in the context of that patent in February 2002. And it is my opinion that the prior art set forth in the Petition fails to disclose or render obvious the subject matter of the challenged claims under any reasonable construction and interpretation of the challenged claims’ terms, including their plain meanings, as well as the constructions Petitioner’s expert, Dr. Bagherzadeh, proposes.

29. Based on the '443 patent's claims and the patent's specification, a person of ordinary skill in the art would understand that the claim language in claims 1 and 8 describe a multiple-clock domain microprocessor, where the multiple clocks are independent of each other, and where the input voltages are independent of each other. Further, the frequency of each clock in a domain can be changed independently of other clocks, and the voltage value for each domain can be changed independently of the voltage values of other domains.

30. Skilled artisans would so understand these limitations because they would immediately recognize that the ability to design a multi-domain microprocessor with independent clock domains and independent voltage domains provides a new degree of flexibility not present in microprocessors in February 2002.

31. I reserve the right to further explain how skilled artisans would understand terms in the '443 patent's claims, including but not limited to the terms discussed above, in the event the Board institutes an *inter partes* review of the '031 patent.

VI. The '443 Patent

32. The '443 patent is titled "Multiple Clock Domain Multiprocessor" and relates to methods for designing a globally synchronous, locally asynchronous (GALS) microprocessor '443 patent, Cover.

33. The '443 patent explains that, around the time of its priority date (February 2002), microprocessor vendors were enjoying the ability to scale frequency, but this scaling had recently impacted by issues related to wire delays '443 patent, 1:29-37. The '443 patent described problems due to clock skew, which raised new questions about whether designers should consider the potential for asynchrony in their designs (Ex. 1001 '443 1:37:45).

34. The '443 patent discusses problems that occur when leveraging asynchronous clocks in a single design. For example, the '443 patent discusses “Two major reasons for this reluctance are the immaturity of asynchronous design tools relative to those in the synchronous domain, and the cost and risk of moving away from the mature design infrastructures that have been successfully used to create many generations of microprocessor products,” '443 patent, 1:50-55. The '443 patent also explains ways the industry had tried to deal with such issues. For example, the '443 patent discusses how “several multiprocessor systems run the memory bus off of a different clock than the processor core,” where “the logic in each of the two clock domains is designed using conventional synchronous design methodologies Ex. 1001 '443 patent, 1:56-1:62.

35. The '443 patent also recognizes that prior methods for supporting a multiple clock domain (MCD) globally-asynchronous locally-synchronous (GALS) clocking did not address issues related supporting synchronization and

communication between domains Ex.1001 '443 patent, 1:62-65. The '443 patent teaches that “[s]ome synchronization schemes restrict the phase relationship and relative frequencies of the clocks, thereby eliminating the need for hardware arbitration [27].” Ex 1001 6:33-35. The '443 patent includes a citation [27] “L. F. G. Sarmenta, G. A. Pratt, and S. A. Ward. Rational Clocking. In Proceedings of the International Conference on Computer Design, Austin, Tex., October 1995.” Ex. 1001 1:54-56. (Ex. 2004) (hereinafter, “Sarmenta”), which provides an example of a GALS design with one exemplar of dependent clocking.

36. Sarmenta describes an “approach maintains [that] a known phase relationship between clocks whose frequencies are related by a rational factor and exploits the predictability of their relative phases to algorithmically time communications without run-time arbitration contests.” Ex. 2004 (Sarmenta) Abstract. The “rational factor” in the paper refers to the relationship between the clock frequencies of two independently clocked digital subsystems. These frequencies are related by the ratio of two integers, (M/N) , where (M) and (N) are small integers. This rational relationship ensures that the clocks align periodically, creating predictable points in time where the active edges of both clocks coincide.

37. As an example, as described by Sarmenta, if a first clock operates at a frequency (f_m) and a second clock at (f_n) , their frequencies satisfy the

relationship the relationship ($f_m/f_n = M/N$). When one clock is a multiple of the other clock, then periodic alignment is possible, described by Sarmenta as a “coincidence cycle” Ex. 2004 (Sarmenta) 271 Section 2. The result is that the clock edges of the two clocks will eventually align periodically. This predictable behavior is key to managing data transfers between different domains, without requiring further synchronization operations.

38. However, as the ‘443 patent discusses when introducing the Sarmenta example, “these schemes impose significant restrictions on the possible choices of frequencies.” Ex 1001 (‘443) 6:35-37. To remedy the limitations of systems such as Sarmenta, the ‘443 patent explains that “[t]he designers of each domain [to be] no longer constrained by the speeds of critical paths in other domains, affording them greater freedom in each domain to optimize the tradeoffs among clock speed, latency, and the exploitation of application parallelism via complex hardware structures.” Ex. 1001 (‘443) 2:34-39. While Sarmenta introduces a synchronization approach leveraging rational frequency relationships, Sarmenta’s scheme imposes significant restrictions on frequency selection, as noted in the ‘443 patent Ex. 1001 (‘443) 6:33-44. The ‘443 invention overcomes these limitations, offering independence in clock frequency generation, allowing each frequency domain to adopt their own independent frequency, offering near infinite resolution in terms of the clock frequency selected for each domain.

39. The '443 patent distinguishes between earlier art that introduced GALS designs, and a multiple clock domain (MCD), where “each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-domain communication,” ‘443 4:17-19. Further, the '443 patent explains “Although the inter-domain synchronization increases the number of clock cycles required to run a given application, an MCD microprocessor affords a number of potential advantages over a singly clocked design” ‘443 patent, 4:21-24. The '443 patent discusses how the use of a local phase lock loop (PLL) can be used to support independence between the clocks used for each domain. This avoids issues of clock skew, that have been a growing issue as design frequencies and chip sizes have increased and allows designers to utilize higher frequency clocks. Further, “Using separate voltage inputs, external voltage regulators, and controllable clock frequency circuits in each clock domain allows for finer-grained dynamic voltage and frequency scaling, than can be achieved with single clock, single-core-voltage systems” ‘443 patent, 4:46-50. Patent ‘443 overcomes earlier limitations of GALS systems by developing novel methods to support using independent clock and independent voltage controls, overcoming issues related to inter-domain synchronization and communication.

40. The inventors of the '443 found that an MCD processor with separate clocks whose frequencies vary from domain to domain not only worked, but

resulted in "a 20% average improvement in energy-delay product." EX1001 , 4:58-59. The scale of the improvement was surprising.

41. Counsel has asked me to discuss the SimpleScalar Tool that is mentioned in the Semeraro paper. In the same timeframe as the Semeraro paper (2002), the computer architecture community, including my own research group, was using the SimpleScalar Tool in our research.

42. In 2002, SimpleScalar was a computer simulator that was commonly used by the computer architecture community to evaluate the performance and correctness of new architectural designs. Among other features, the SimpleScalar tool included a performance simulator that implemented the device at the microarchitecture level, including data paths, memory architecture and control units of the computer device. See, e.g., Paper at 5 (discussing use of SimpleScalar to implement modified "microarchitecture of the Alpha 21264 microprocessor" where the centralized Register Update Unit was split "into separate reorder buffer (ROB), issue queue, and physical register file structures.") The SimpleScalar tool provided for execution-driven simulations, where the device being implemented ran as an instrumented program on a host. See Ex. 2011.

43. Claim 1 of the '443 Patent recites "a plurality of domains' each of which includes "a clock for separately generating a clock signal at a frequency for that domain ... " and "a voltage input for receiving a voltage which is dynamically

changeable ..." When the SimpleScalar tool executed the simulation described in the Paper on a host, the host executing the simulation embodied all of the elements of claim 1 in tangible form. The same can be said for each of the other claims in the '443 Patent, namely, that the host executing the simulation embodied all of the elements of the claim in tangible form. In addition, separate and apart from the host used to implement the device during the simulation, the computer code (standing alone) used to implement the simulation embodied all of the elements of claim 1 (and the other claims of the '443 patent) in tangible form.

44. Industry relies heavily on simulators (such as SimpleScalar) to demonstrate the operation of architectural designs. Similarly, in academia, research papers in the field of computer architecture often include simulation results from simulators, enabling the research community to effectively quantify the benefits a design. In both research and academia, results on a validated simulator (such as SimpleScalar) are typically accepted as evidence that an architectural design has been sufficiently tested to demonstrate that it will work for its intended purpose. In addition, in the context of the Paper, given the details and thoroughness of the simulation as described herein, it is my opinion that others working in the field reading the Paper would have understood that the device implemented in the simulation was shown to work for its intended purpose. At that point, skilled

artisans in the field could have implemented the architectural design in other forms, such as a stand-alone silicon chip, through application of ordinary skills.

VII. The Claims Of The '443 Patent Would Not Have Been Obvious.

45. Petitioner challenges claims 1, 3, 4, 5, 8, 10, and 12, of the '443 patent based on six grounds of purported obviousness, each of which depends on each of which depends on prior art or combinations of prior art.

46. In my opinion, none of the claims of the '443 patent would have been obvious over Petitioner's prior art, for reasons I explain below. I will first review the Petitioner's prior art. Then I will address each of the six grounds.

1. Overview of Iyer

47. Iyer is titled "Power Efficiency of Voltage Scaling in Multiple Clock, Multiple Voltage Cores". Iyer was published in the proceedings of the IEEE/ACM International Conference on Computer Aided Design, November 10, 2022. As this date is after the priority date for the Semeraro paper of February 2, 2002, I will not be addressing Ex. 1005 further in my comments.

2. Overview of Soerensen

48. Soerensen is titled "Dynamic Voltage Control Method and Apparatus" and presents a method for selecting a clock frequency for a microprocessor and determines what voltage is needed to support the targeted clock frequency. More specifically, "a voltage level indicated by the voltage requirement is supplied to

the processor and the frequency distribution indicated by the frequency requirement is provided to the clocks signals of the processor.” Ex.1006 (Soerensen), Cover, Abstract.

49. Figure 2 from Soerensen shows how each domain clock is dependent on the system clock signal 82 Ex. 1006 (Soerensen) Figure 2. Soerensen describes Figure 2 in more detailed, describing how clock signals are changed, stating that “The clock signals in each clock domain are provided by various select, divider, and gating logic and distributed to the components of the processor via a plurality of clock trees 50a-50h.” Ex. 1006 (Soerensen) 0037.

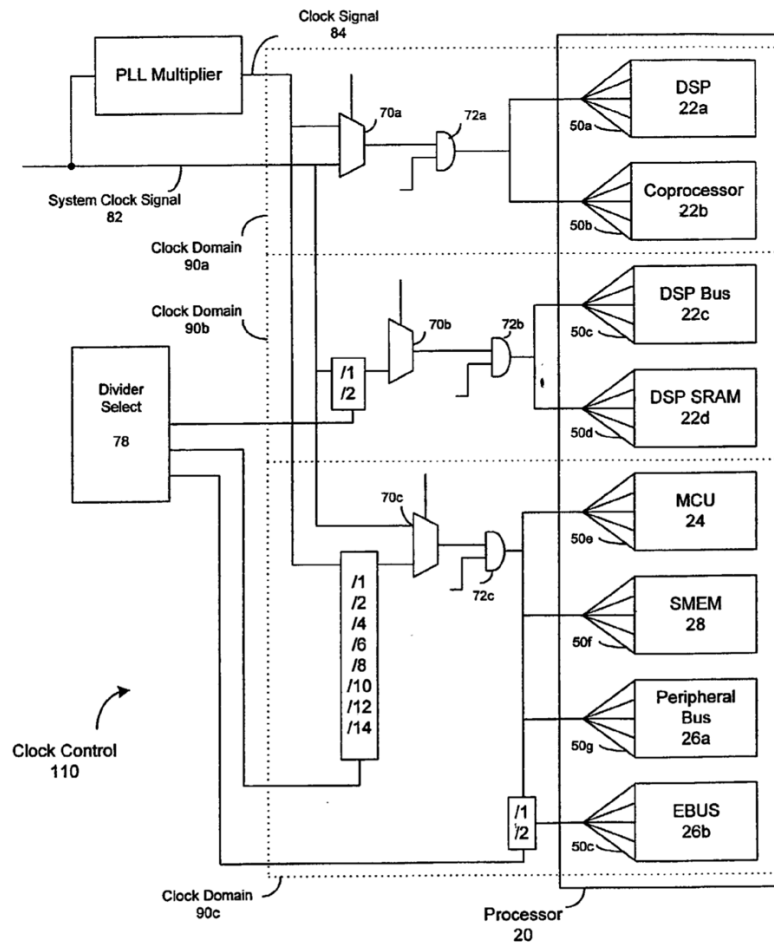


Fig. 2

50. Soerensen further describes clock control as follows “Additionally, clock control 110 may divide the frequency of clock signal 84 in order to provide the components of the processor with clock signals having reduced frequencies in order to meet the clock frequency requirement of the processor..... Similarly, divider 64 may provide the clocked components operating in clock domain 90c with a clock signal having a frequency reduced by factors of 2, 4, 6, 8, 10, 12 and 14.” Ex. 1006 (Soerensen) 0038.

3. Overview of Hemani

51. Hemani is titled “Lowering Power Consumption in Clock by using Globally Asynchronous Locally Synchronous Design Style” and is generally directed toward methods associated determining the best number of clock domains and automation of the synthesis of global asynchronous communication Ex.1007 (Hemani), Cover, Abstract.

52. Hemani discusses design tradeoffs associated with a globally asynchronous locally synchronous design. Hemani teaches “The GALS methodology extends the established synchronous design methodology in two respects.... One is to partition the system into optimal number/size of SBs (synchronous blocks), and the other is to refine the communication among SBs for asynchronous communication” Ex. 1007 (Hemani), page 2. The paper focuses primarily on the first of these challenges.

4. Overview of Moore

53. Moore is titled “Channel Communication Between Independent Clock Domains.” Moore describes methods of achieving reliable and low-latency communication between independent clock domains by combining clock pausing, self-calibrating delay lines and an asynchronous interconnect. Ex. 1008 (Moore) page 1, Abstract. The approach targets a system-on-a-chip design, enabling different system building blocks to be clocked at different rates.

54. Moore describes a “mechanism for reliable data transfer between an asynchronous producer (one end of the asynchronous channel) and a synchronous consumer. Then we will discuss the synchronous producer which sends data to the asynchronous channel. These two parts are then combined and we look at additional decoupling and other techniques required to maximise bandwidth.” Ex. 1008 (Moore) page 1, Intro. Moore does not describe the details of clock control, only how to handle communication between heterogeneous domains.

5. Overview of Njølstad

55. Njølstad is titled “A Socket Interface for GALS Using Locally Dynamic Voltage Scaling for Rate-Adaptive Energy Saving”. Njølstad discusses a low-power implementation of a globally asynchronous locally synchronous design. Ex. 1009 (Njølstad) page 110, Abstract.

56. As shown below in Figure 3 from Njølstad, the paper describes a model for a wideband radio access system that utilizes different clocks and voltages, as well as different device technologies. Ex. 1009 (Njølstad) Figure 3. The structure functions as a sequence of stages or buffers, where the clock rate and voltage are changed so that each stage does not produce results faster than can be processed by the next stage, avoiding overruns. The approach controls each clock frequency to implement flow control, while potentially reducing power usage.

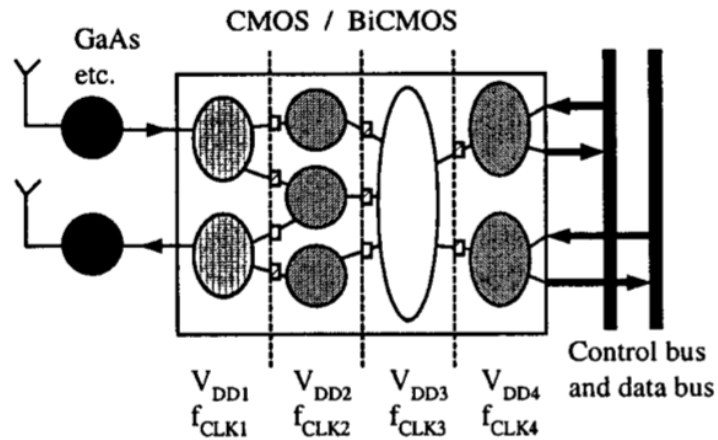


Figure 3: A model of a wideband radio access system using multiple supply voltages and logic level shifters.

57. Njølstad describe the design of this pipelined architecture using multiple clock domains for flow control, much in the same way we would want to balance the stages of an assembly line in a factory. The problem is reminiscent of a well-known sit-com, shown in the figure below¹. Lucille Ball and her friend Ethel Mertz are trying to accommodate an increase in the upstream production rate of chocolates. Lucy and Ethel end up on the production belt covered in chocolate. Clearly, if Lucy had control over the upstream production rate, as Njølstad teaches using a dependent clocking scheme, there would be no assembly line overruns. Though in Njølstad's use of GALS, each clock is interdependent on every other clock in the system.

¹ Available at <https://youtu.be/NkQ58I53mjk?si=853AONLdNJUz3Du1>



6. Overview of Liljeberg

58. Liljeberg is titled “Asynchronous Interface for Locally Clocked Modules in ULSI Systems.” Liljeberg describes an architecture that “employs interface units which communicate asynchronously with each other and synchronously with locally clocked modules.” Ex. 1010 (Liljeberg) Abstract Further, Liljeberg describes an architecture where “Interface units feature elastic burst-mode data transfer to reduce the number of synchronizations.” Ex. 1010 (Liljeberg) Abstract

59. Liljeberg teaches “an interface design which manages asynchronous data transfer and communication between asynchronous modules. To accomplish this, each synchronous module is equipped with an interface unit which transfers data and control signals from asynchronous domain to synchronous domain and vice versa.” Ex. 101 (Liljeberg) Intro. The buffering functions as a FIFO buffer and uses dual-ported memory. Given this design, Liljeberg discusses how to

manage clocks in each domain, and how to support more direct domain-to-domain interaction.

B. Ground 1: Claims 1, 3-5, 8, 9 and 12 Would Not Have Been Obvious By Iyer

60. The ‘443 patent’s priority date is February 2, 2002, which predates the Iyer date of November 10, 2022. Thus, it is my opinion that Iyer has no relevance as prior art in this case. This is also true for all claims and limitations cited by the Petitioner.

C. Ground 2.A: Claims 1, 3, 4, 5, 8, 10 and 12 Would not have been Obvious by Njølstad

61. Claims 1 and 8 of the ‘443 patent are the independent claims of the ‘443 patent. Claims 3, 4, and 5 are dependent on claim 1, and claims 10 and 12 are dependent on claim 8. Njølstad does not teach the independent clocks described in claim 1 and claim 8 of the ‘443 patent, as well as in dependent claims 3, 4, 5, 10 and 12, as we will discuss next.

62. Njølstad describes a low-power implementation of a globally asynchronous locally synchronous design. As described earlier, Njølstad describes how to use multiple clocks for stages of a pipelined system, where clocking is used for flow control. The clocks in Figure 3 (see above) are dependent on each other and are used to maintain a smooth flow of input/output between pipeline stages. If

Njølstad's clocks were not coordinated, we would end up in overruns, as experienced by Lucy and Ethel in the chocolate factory analogy. Therefore, Njølstad does not teach "separately generating a clock signal... the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains," as taught by the independent claims of the '443 patent. Given that claims 3, 4, and 5 depend on claim 1, and claim 12 depends on claim 10, which depends on independent claim 8, it is my opinion that Njølstad does not disclose or make obvious claims 1, 3, 4, 5, 10 and 12 of the '443 patent.

D. Ground 2.B: Claims 5 and 10 Would Not Have Been Obvious Over Njøstad in view of Liljeberg

63. Claim 5 of the '443 patent is dependent on independent claim 1 and claim 10 is dependent on independent claim 8 of the '443 patent. Njøstad does not teach the independent clock control described in claim 1 or claim 8 of the '443 patent, nor does Liljeberg, as we will discuss next.

64. In terms of combining Njøstad and Liljeberg, a POSITA would have recognized that these two exhibits have unrelated goals. Njøstad teaches about a socket interface that can provide locally dynamic voltage scaling Ex. 1009 page 110, Abstract. Njøstad targets a wideband radio access system (see Figure 3 from Njøstad, discussed earlier), while Liljeberg is targeting "an interface design which manages asynchronous data transfer and communication between asynchronous

modules.” Ex. 1010 (Liljeberg) page 1, Abstract, and discusses a FIFO-like system. It appears to me that the Petitioner is working backwards from the ‘443 patent’s claims, looking for disclosures in disparate references, without meaningfully considering whether the reference they cited would, in fact, be combined in the first place. I understand that obviousness arguments based on this type of hindsight are improper.

65. Even assuming that a POSITA would have looked to combine the teachings of Njøstad and Liljeberg, Liljeberg does not make up for the deficiencies of the Njøstad paper. A POSITA would understand that Njøstad teaches a method that uses dependent clocks, versus the independent clocks as taught in the ‘442 patent, and Liljeberg does not provide details on how to manage multiple clock domains. It is my opinion Njøstad, in view of Liljeberg, does not disclose or make obvious claims 5 and 10 of the ‘443 patent.

E. Ground 3.A: Claims 1, 3, 4, 5, 8, 10 and 12 Would Not Have Been Obvious Over Soerensen

66. Claims 1 and 8 are the independent claims of the ‘443 patent. Claims 3, 4, and 5 are dependent on claim 1, and claim 12 is dependent on claim 10, which is dependent on independent claim 8. Soerensen does not teach the independent clocks described in claims 1 or 8 of the ‘443 patent, and does not teach dependent claims 3, 4, 5, and 10 either, as we will discuss next.

67. Soerensen describes methods for selecting a clock frequency for a microprocessor and determines what voltage is needed to support the targeted clock frequency. More specifically, “a voltage level indicated by the voltage requirement is supplied to the processor and the frequency distribution indicated by the frequency requirement is provided to the clocks signals of the processor.” Ex.1006 (Soerensen), Cover, Abstract.

68. In Figure 2 (shown above), Soerensen describes clock control as follows “Additionally, clock control 110 may divide the frequency of clock signal 84 in order to provide the components of the processor with clock signals having reduced frequencies in order to meet the clock frequency requirement of the processor.... Similarly, divider 64 may provide the clocked components operating in clock domain 90c with a clock signal having a frequency reduced by factors of 2, 4, 6, 8, 10, 12, and 14.” Ex. 1006 (Soerensen) 0038.

69. Soerensen suffers from the same issues as Sarmenta, since Soerensen “impose[s] significant restrictions on the possible choices of frequencies.” Ex 1001 (‘443) 6:35-37. Therefore, Soerensen does not teach “separately generating a clock signal... the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains,” as taught by the dependent claims of the ‘443 patent. Given that claims 3, 4, and 5 depend on claim 1, and claim 12 depends on claim 10, which depends on

independent claim 8, it is my opinion that Soerensen does not disclose or make obvious claims 1, 3, 4, 5, 10 and 12 of the ‘443 patent.

F. Ground 3.B: Claims 1, 3, 4, 5, 8, 10, and 12 Would Not Have Been Obvious By Soerensen in View of Hemani

70. Claims 1 and 8 are the independent claims of the ‘443 patent. Claims 3, 4, and 5, are dependent on independent claim 1. Claim 12 is dependent on claim 10 and claim 10 is dependent on independent claim 8. Soerensen does not teach the independent clocks described in claim 1 and claim 8 of the ‘443 patent, as well as the dependent claims 3, 4, 5, 10 and 12, nor does Hemani, as we will describe next.

71. In terms of combining Soerensen and Hemani, a POSITA would have recognized that these two exhibits have unrelated goals. Soerensen teaches about “a voltage level indicated by the voltage requirement is supplied to the processor and the frequency distribution indicated by the frequency requirement is provided to the clocks signals of the processor.” Ex.1006 (Soerensen), Cover, Abstract, while Hemani is focused on identifying the optimal number of clock domains for a globally asynchronous locally synchronous system. While both of these exhibits discuss clocking and power, it appears to me that the Petitioner is working backwards from the ‘443 patent’s claims, looking for disclosures in disparate references, without meaningfully considering whether the reference they site

would, in fact, be combined in the first place. I understand that obviousness arguments based on this type of hindsight are improper.

72. Even assuming that a POSITA would have considered to combine Soerensen with Hemani, the latter does not make up for the deficiencies of the former. Discussed earlier in Figure 2 (shown above), Soerensen describes clock control as follows “Additionally, clock control 110 may divide the frequency of clock signal 84 in order to provide the components of the processor with clock signals having reduced frequencies in order to meet the clock frequency requirement of the processor..... Similarly, divider 64 may provide the clocked components operating in clock domain 90c with a clock signal having a frequency reduced by factors of 2, 4, 6, 8, 10, 12 and 14.” Ex. 1006 (Soerensen) 0038. Therefore, Soerensen does not teach “separately generating a clock signal... the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains.” ‘443 patent.

73. The Hemani paper targets finding the optimal number of clock domains for a design, though does not describe how independent clocks can be managed. The Hemani paper does not address the deficiencies of Soerensen. A POSITA would understand the clocking structure taught by Soerensen would lack the flexibility and precision of the independent clocks that are taught in the ‘443 patent.

For at least the foregoing reasons, it is my opinion that the Petitioner has not shown that claims 1, 3, 4, 5, 8, 10, and 12 would have been obvious.

G. Ground 3.C: Claims 5 and 10 Would Not Have Been Obvious Over Soerensen in view of Moore

74. Claim 5 of the ‘443 patent is dependent on independent claim 1 and claim 10 of the ‘443 patent is dependent on independent claim 8. Soerensen, in view of Moore, does not teach the independent clocks described in claims 1 and 8 of the ‘443 patent, nor dependent claims 5 and 10, as we will describe next.

75. In terms of combining Soerensen and Moore, a POSITA would have recognized that these two exhibits have unrelated goals. Soerensen teaches about “a voltage level indicated by the voltage requirement is supplied to the processor and the frequency distribution indicated by the frequency requirement is provided to the clocks signals of the processor.” Ex.1006 (Soerensen), Cover, Abstract, while Moore is focused on methods of achieving reliable and low-latency communication between independent clock domains by combining clock pausing, self-calibrating delay lines and an asynchronous interconnect. While each exhibit discusses elements of clocking and power, it appears to me that the Petitioner is working backwards from the ‘443 patent’s claims, looking for disclosures in disparate references, without meaningfully considering whether the reference they cite would, in fact, be combined in the first place. I understand that obviousness arguments based on this type of hindsight are improper.

76. Even assuming a POSITA would have considered to combine Soerensen with Moore, the latter does not make up for the deficiencies of the former. Discussed earlier in Figure 2 (shown above), Soerensen describes clock control as follows “Additionally, clock control 110 may divide the frequency of clock signal 84 in order to provide the components of the processor with clock signals having reduced frequencies in order to meet the clock frequency requirement of the processor..... Similarly, divider 64 may provide the clocked components operating in clock domain 90c with a clock signal having a frequency reduced by factors of 2, 4, 6, 8, 10, 12 and 14.” Ex. 1006 (Soerensen) 0038. Therefore, Soerensen does not teach “separately generating a clock signal... the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains.” ‘443 patent.

77. The Moore paper targets a mechanism for reliable data transfer between an asynchronous producer (one end of the asynchronous channel) and a synchronous consumer, in addition to a mechanism that allows a synchronous producer to send data to the asynchronous channel. The Moore paper does not address the deficiencies of Soerensen. A POSITA would understand the “relational clocking” structure taught by Soerensen would lack the flexibility and precision of the independent clocks that are taught in the ‘443 patent. For at least the foregoing

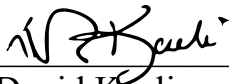
reasons, it is my opinion that the Petitioner has not shown that claims 5 and 10 would have been obvious.

VIII. Conclusion

78. For the foregoing reasons, it is my opinion that claims 1, 3, 4, 5, 8, 10 and 12 of the '443 patent would not have been obvious over the prior art in Petitioner's Petition for *inter partes* review.

All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001.h I declare under penalty of perjury that the foregoing is true and correct.

Executed on November 19, 2024, in Boston, Massachusetts.



Dr. David Kaeli