

In the **PATENT** of:

University of Rochester

Patent No.: 7,089,443

Application No.: 10/762,550

Filed: January 23, 2004

For: MULTIPLE CLOCK DOMAIN
MICROPROCESSOR

INVENTOR DECLARATION

I, David H. Albonesi, make the following declaration based on my own personal knowledge:

1. I am a named inventor of the above-identified patent (hereinafter, '443 Patent) along with my co-inventors Greg Semeraro, Grigorios Magklis, Michael L. Scott, Rajeev Balasubramonian, and Sandhya Dwarkadas. (hereinafter Co-Inventors).

2. I, along with my Co-Inventors, invented the subject matter described and claimed in the '443 Patent.

3. At the time, I worked in the Electrical and Computer Engineering Department of the University of Rochester, and my Co-Inventors worked in the Computer Science Department of the University of Rochester. As set forth in Column 1, Lines 11-16, of the '443 Patent, our work was supported in part by grants from the National Science Foundation and by DARPA.

4. Column 5, Lines 22-27, of the '443 Patent states: "The following paper

describes the invention and is hereby incorporated by reference in its entirety into the present disclosure: Semeraro et al, "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling," High Performance Computer Architecture (HPCA), Feb. 2, 2002."

5. I am a co-author along with my Co-Inventors of "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling" (hereinafter, "Paper"). The Paper was published in *Proceedings Eighth International Symposium on High Performance Computer Architecture*, pp. 29-40 in February, 2002.

6. A copy of the Paper is included in the Appendix to this Declaration.

7. The Paper describes the same invention claimed in the '443 Patent.

8. All of the figures (i.e., 1, 2, 3, 4, 5, 6,7,8A, 8B, 9A, and 9B) contained in the '443 Patent are virtually identical (additional reference numerals were added) to the corresponding figures in the Paper.

9. The Paper was awarded the Technical Committee on Computer Architecture's 2022 Test of Time Award at the 29th IEEE International Symposium on High-Performance Computer Architecture in February 2023 by the Technical Committee on Computer Architecture of the Institute of Electrical and Electronics Engineers Computer Society.

10. As explained by the Institute of Electrical and Electronics Engineers Computer Society, "the HPCA Test of Time (ToT) award recognizes the most influential papers published in prior sessions of the International Symposium of High

Performance Computer Architecture (HPCA) each of whom have had significant impact in the field." (<https://ieeetcca.org/awards/hpca-test-of-time-award/>)

11. The Paper introduced a microarchitecture design for multiple-clock-domain microprocessors that my Co-Inventors and I invented. According to the microarchitecture design, the chip is divided into several clock and frequency domains that can be independently configured to exploit the benefits of frequency and voltage scaling.

12. For example, the Abstract of the Paper describes "We describe an alternative approach, which we call a Multiple Clock Domain (MCD) processor, in which the chip is divided into several (coarse-grained) clock domains, within which independent voltage and frequency scaling can be performed."

13. In addition, the Paper explains that "An approach that allows for aggressive future frequency increases, maintains a synchronous design methodology, and exploits the trend towards making functional blocks more autonomous, is a *multiple clock domain (MCD)* microarchitecture, which uses a *globally-asynchronous, locally-synchronous (GALS)* clocking style. In an MCD microprocessor each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-domain communication."

14. As stated in the Paper, "an MCD microprocessor affords a number of potential advantages over a singly clocked design" including that "[u]sing separate voltage inputs, external voltage regulators, and controllable clock frequency circuits in each clock domain allows for finer grained dynamic voltage and frequency scaling,

and thus lower energy, than can be achieved with single clock, single-core-voltage systems."

15. For example, the Paper described a design that included "four clock domains, corresponding to the front end (including L1 instruction cache), integer units, floating point units, and load-store units (including L1 data cache and L2 cache)."

16. The Paper also described "a simulation infrastructure based on SimpleScalar and Wattch" that we performed to evaluate the design. Paper, Abstract. The simulation described in the Paper was completed before publication of the Paper in February, 2002.

17. The microarchitecture design described in the Paper is the same design implemented by the multiple-clock-domain microprocessor described and claimed in the '443 Patent.

18. The Paper includes a section entitled "3. Simulation Methodology" which details how my Co-Inventors and I simulated and tested our invention to show that it worked as intended by demonstrating that "per-domain dynamic voltage and frequency scaling" resulted in "a 20% average improvement in energy-delay product for a set of benchmarks that includes both compute and memory-bound applications."

19. The same simulation described in "3. Simulation Methodology" of the Paper is described in the '443 Patent. (see Col. 8 Ll. 28 – Col. 13 Ll. 11) The simulation described in the Paper and the '443 Patent are one and the same and, as stated above, was completed before publication of the Paper in February, 2002.

20. The Paper also includes a section entitled “4. Results.” This section contains the results compiled by my Co-inventors and me and shows the results of testing our invention.

21. The same results contained in “4. Results” is also included in the ‘443 Patent. (see Col. 13 Ll. 12- Col. 16 Ll. 14) The results described in the Paper and the ‘443 Patent are one and the same and, as stated above, these results were found before publication of the Paper in February, 2002.

22. The Conclusion of the Paper states:

- a. “We have described and evaluated a multiple clock domain (MCD) microarchitecture, which uses a globally asynchronous, locally-synchronous (GALS) clocking style along with dynamic voltage and frequency scaling in order to maximize performance and energy efficiency for a given application.”
- b. “Our design uses existing queue structures in a superscalar processor core to isolate the different clock domains in a way that minimizes the need for inter-domain synchronization.”
- c. “Performance results for applications drawn from standard benchmark suites suggest that the division of the processor into multiple domains incurs an average baseline performance cost of less than 4%.”
- d. “At the same time, by scaling frequency and voltage in different domains dynamically and independently, we can achieve an average

improvement in energy-delay product of nearly 20%.”

- e. “By contrast, global voltage scaling to achieve comparable performance degradation in a singly clocked microprocessor achieves an average energy-delay improvement of only 3%.”

23. The Paper was published in the Proceedings Eighth International Symposium on High Performance Computer Architecture in February 02-06, 2002.]

24. Accordingly, my Co-Inventors and I had conceived of the invention and actually reduced the invention to practice before the February 2002 publication of the Paper.

25. All statements made herein of my own knowledge are true, all statements made herein on information and belief are believed to be true, and these statements are made with the knowledge that willful false statements are punishable by fine and/or imprisonment under 35 U.S.C. §1001, and may jeopardize the validity of this patent and related applications.

26. I Declare under penalty of perjury that the foregoing is true and correct.

Executed on 11/13/2024.

By: David H. Albonesi
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