

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TCL ELECTRONICS HOLDINGS LTD. and
TCL INDUSTRIES HOLDINGS CO., LTD.,
Petitioner,

v.

UNIVERSITY OF ROCHESTER
(INTELLECTUAL VENTURES I, LLC),
Patent Owner.

IPR2024-01245
Patent 7,089,443 B2

Before JAMESON LEE, THU A. DANG, and HYUN J. JUNG,
Administrative Patent Judges.

DANG, *Administrative Patent Judge.*

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background

TCL Electronics Holdings Ltd. and TCL Industries Holdings Co., Ltd. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1, 3, 4, 5, 8, 10, and 12 (the “challenged claims”) of U.S. Patent No. 7,089,443 B2 (Ex. 1001, “the ’443 patent”). Paper 2 (“Pet.”). University of Rochester (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 9 (“Prelim. Resp.”).¹

Under 37 C.F.R. § 42.4(a), the Board has authority to determine whether to institute an *inter partes* review. Applying the standard set forth in 35 U.S.C. § 314(a), we may not institute an *inter partes* review (also “IPR”) unless the information presented in the petition “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” However, institution of *inter partes* review is discretionary. *See Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“[T]he PTO is permitted, but never compelled, to institute an IPR proceeding.”). For the reasons stated below, we exercise our discretion not to institute an *inter partes* review.

B. Real Parties-in-Interest

Petitioner identifies itself as the real party-in-interest. Pet. 77. Patent Owner identifies itself and Intellectual Venture I LLC, each as the real party-in-interest. Paper 6, 2.

¹ Patent Owner states that University of Rochester owns the patent and Intellectual Ventures I LLC is an exclusive licensee. Paper 6, 2 (Patent Owner’s mandatory notices). Patent Owner represents that Intellectual Ventures I LLC has all substantial rights to the ’443 patent. *Lenovo (United States) Inc. v. University of Rochester*, IPR2024-01225, Paper 5 at 2 (PTAB Nov. 15, 2024) (Patent Owner’s Mandatory Notices).

C. Related Proceedings

The parties identify the following district court matter as involving the '443 patent: *Intellectual Ventures I LLC v. TCL Electronics Holdings Ltd. et al.*, 6:23-cv-00309-ADA (W.D. Tex. April 26, 2023) (the “district court litigation”). Pet. 77; Paper 6, 2. In addition, Patent Owner identifies the following district court matters as involving the '443 patent: (i) *Intellectual Ventures I LLC et al. v. Lenovo Group Limited*, 6:23-cv-00307-ADA (W.D. Tex. April 26, 2023); (ii) *Intellectual Ventures I LLC et al. v. TCL Electronics Holdings Ltd. f/k/a/ TCL Multimedia Technology Holdings, Ltd. et al.*, 6:23-cv-00293-ADA (W.D. Tex. April 20, 2023); and (iii) *Intellectual Ventures II LLC et al. v. Lenovo Group Limited*, 6:23-cv-00068-ADA (W.D. Tex. filed February 2, 2023, terminated on April 20, 2023). Paper 6, 2.

Patent Owner also identifies the following *inter partes* review (with a different petitioner) as involving the '443 patent: *Lenovo (United States) Inc. v. University of Rochester (Intellectual Ventures I LLC)*, IPR2024-01225. Paper 6, 2–3.

D. The '443 Patent

The '443 patent, titled “Multiple Clock Domain Microprocessor,” issued on August 8, 2006, from Application No. 10/762,550, with a filing date of January 23, 2004, and claiming the benefit of Provisional Application No. 60/441,759, filed on January 23, 2003. Ex. 1001, codes (54), (45), (21), (22), (60). The '443 patent observes “that in order to continue the current pace of clock frequency increases, microprocessor designers will eventually be forced to abandon singly-clocked globally synchronous systems in favor of some form of asynchrony.” *Id.* at 1:42–45.

The '443 patent describes a multiple clock domain (MCD) microarchitecture for a microprocessor which uses a globally-asynchronous, locally-synchronous (GALS) clocking style where each functional block operates with a separately generated clock. *Id.* at code (57); *see also id.* at 4:16–19. The '443 patent reports that “by scaling frequency and voltage in different domains dynamically and independently, we can achieve an average improvement in energy-delay product of nearly 20%.” *Id.* at 5:8–11. The '443 patent further describes that “[t]he independence of each local domain clock implies no global clock skew requirement, permitting potentially higher frequencies within each domain and greater scalability in future process generations.” *Id.* at 4:29–32. “Using separate voltage inputs, external voltage regulators, and controllable clock frequency circuits in each clock domain allows for finer grained dynamic voltage and frequency scaling, and thus lower energy, than can be achieved with single clock, single-core-voltage systems.” *Id.* at 4:40–45.

Figure 1 of the '443 patent is a block diagram of an MCD processor, and is reproduced below. *Id.* at 5:32–33.

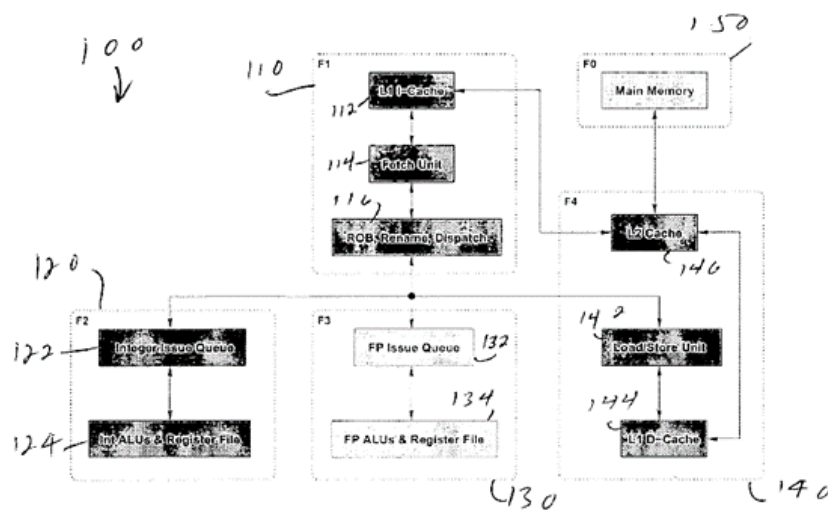


Figure 1

Figure 1 above depicts architecture 100 with four domains consisting of front end 110, integer issue/execute 120, floating point issue/execute 130, and load/store issue/execute 140. *Id.* at 5:52–6:26. Front end 110 includes instruction cache 112, fetch unit 114, and branch prediction, rename, and dispatch 116. *Id.* Integer issue/execute 120 includes integer issue queue 122 and integer arithmetic logic units and register file 124. *Id.* Floating point issue/execute 130 includes floating point issue queue 132 and floating point arithmetic logic units and register file 134. *Id.* Load/store issue/execute 140 includes load/store unit 142, L1 D-cache 144, and L2 cache 146, where L2 cache 146 is in communication with main memory interface 150 as well as with the cache 112 of the front end 110. *Id.*

E. Challenged Claims

Of the challenged claims (1, 3, 4, 5, 8, 10, and 12), claims 1 and 8 are the independent claims. Claims 3, 4, and 5 depend from claim 1, and claims 10 and 12 depend from claim 8. Independent claim 1 is illustrative and is reproduced below:

1. A multiple clock domain microprocessor comprising:
a plurality of domains;
for each of the plurality of domains, a clock for separately
generating a clock signal at a frequency for that domain,
the frequency being dynamically changeable
independently of the frequencies of the clock signals
generated for others of the plurality of domains; and
for each of the plurality of domains, a voltage input for
receiving a voltage which is dynamically changeable
independently of the voltages applied to said others of the
plurality of domains.

Ex. 1001, 17:9–19.²

F. Evidence

Petitioner relies on the references listed below.

Reference	Date	Exhibit No.
Iyer ³	Nov. 10, 2002 ⁴	Ex. 1005
Soerensen ⁵	Apr. 17, 2003 ⁶	Ex. 1006
Hemani ⁷	June 1, 1999 ⁸	Ex. 1007

² The text set forth above reflects corrections made by way of a certificate of correction of June 14, 2011.

³ Iyer, Anoop, and Diana Marculescu, “Power efficiency of Voltage Scaling in Multiple Clock, Multiple Voltage Cores,” *Proceedings of the 2002 IEEE/ACM International Conference on Computer-Aided Design* (2002) (“Iyer”).

⁴ Petitioner contends Iyer is a conference paper from the IEEE/ACM International Conference held on November 10–14, 2002 and was publicly available no later than November 10, 2002. Pet. 3.

⁵ U.S. Patent App. No. 2003/0071657 A1, published April 17, 2003 (“Soerensen”).

⁶ The application from which Soerensen issued was filed August 29, 2002 (Ex. 1006, codes (21), (22)) and claimed the benefit of a provisional application filed August 29, 2001 (Ex. 1006, code (60)). Petitioner contends at least Soerensen’s claim 1 and all of Soerensen’s disclosures relied upon in the Petition find support in the provisional application. Pet. 3 n.2.

⁷ A. Hemani, T. Meincke, S. Kumar, A. Postula, T. Olsson, P. Nilsson, J. Oberg, P. Ellervee, and D. Lundqvist, “Lowering Power Consumption in Clock by Using Globally Asynchronous, Locally Synchronous Design Style,” *Proc. ACM/IEEE Design Automation Conference* (1999) (“Hemani”).

⁸ Petitioner contends Hemani is a conference paper from the 36th Design Automation Conference (DAC ’99) held on June 21–25, 1999 and was publicly available no later than June 1, 1999. Pet. 4.

Moore ⁹	Aug. 16, 2002 ¹⁰	Ex. 1008
Njølstad ¹¹	Sept. 12, 2001 ¹²	Ex. 1009
Liljeberg ¹³	May 1, 2001 ¹⁴	Ex. 1010

Petitioner also relies on the Declaration of Nader Bagherzadeh, Ph.D. (Ex. 1003), Declaration of Sylvia D. Hall-Ellis, Ph.D. (Ex. 1004), and Declaration of Sean O’Bryan (Ex. 1015). Patent Owner relies on the Declaration of David Kaeli, Ph.D. (Ex. 2001) and Declaration of David H. Albonesi (Ex. 2003).

⁹ Moore, Simon, George Taylor, Bob Mullins, and Peter Robinson, “Channel Communication Between Independent Clock Domains,” *First ACiD-WG Workshop of the European Commission’s Fifth Framework Programme*. (2001) (“Moore”).

¹⁰ Petitioner contends Moore is a conference paper from the Fifth ACiD-WG Workshop held in 2001 and was publicly available no later than August 16, 2002. Pet. 4.

¹¹ Tormod Njølstad, Odd Tjore, Kjetil Svarstad, Lars Lundheim, Tor O. Vedal, Jukka Typpo, Tor Ramstad, Lars Wanhammar, E. J. Aar, and Helge Danielsen, “A Socket Interface for GALs Using Locally Dynamic Voltage Scaling for Rate-Adaptive Energy Saving,” *Proceedings 14th Annual IEEE International ASIC/SOC Conference (IEEE Cat. No. 01TH8558)* (2001) (“Njølstad”).

¹² Petitioner contends Njølstad is a conference paper from the 14th Annual IEEE International ASIC/SOC Conference and was publicly available no later than September 12, 2001. Pet. 4.

¹³ Liljeberg, Pasi, Juha Plosila, and Jouni Isoaho, “Asynchronous Interface for Locally Clocked Modules in ULSI Systems,” *The 2001 IEEE International Symposium on Circuits and Systems (Cat. No. 01CH37196)*, (2001) (“Liljeberg”).

¹⁴ Petitioner contends Liljeberg is a conference paper from the IEEE International Symposium on Circuits and Systems held May 6–9, 2001 and was publicly available no later than May 1, 2001. Pet. 4–5.

G. The Asserted Grounds of Unpatentability

Petitioner contends that challenged claims 1, 3, 4, 5, 8, 10, and 12 are unpatentable under the following grounds. Pet. 5.

Claims Challenged	35 U.S.C. § ¹⁵	Reference(s)/Basis
1, 3, 4, 5, 8, 10, 12	103(a)	Iyer
1, 3, 4, 5, 8, 10, 12	103(a)	Njølstad
5, 10	103(a)	Njølstad, Liljeberg
1, 3, 4, 5, 8, 10, 12	103(a)	Soerensen
1, 3, 4, 5, 8, 10, 12	103(a)	Soerensen, Hemani
5, 10	103(a)	Soerensen, Moore

II. ANALYSIS – DISCRETIONARY DENIAL

Institution of an *inter partes* review is discretionary, not mandatory. *See* 35 U.S.C. § 314(a) (authorizing institution of an *inter partes* review under particular circumstances, but not requiring institution under any circumstances); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2140 (2016) (“[T]he agency’s decision to deny a petition is a matter committed to the Patent Office’s discretion.”); *Harmonic*, 815 F.3d at 1367.

Patent Owner argues that “there are strong reasons for exercising discretion to deny institution” in the present IPR proceeding. Prelim. Resp. 62. In particular, Patent Owner asserts that “Petitioner waited until August 2, 2024—1 day shy of a full year after being served with the Complaint [in the district court litigation]—to file the present IPR,” and thus, as a result, the district court litigation “has already reached an

¹⁵ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 285–93 (2011), amended 35 U.S.C. §§ 102, 103. Because the application from which the ’443 patent issued was filed before March 16, 2013, the effective date of the relevant amendment, the pre-AIA versions of §§ 102, 103 apply.

advanced stage.” *Id.* at 61. Patent Owner points out that the district court issued a claim construction order on September 10, 2024, the parties served their final infringement and invalidity contentions on September 23, 2024, fact discovery is scheduled to be closed on February 24, 2025, and the trial is scheduled for July 28, 2025, which Patent Owner contends is “nearly 7 months before the statutory deadline for issuing a Final Written Decision.” *Id.*

When determining whether to exercise discretion to deny institution in view of a parallel proceeding, we consider the following factors:

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board’s exercise of discretion, including the merits.

See Apple Inc. v. Fintiv, Inc., IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv* factors”). “These factors relate to whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel proceeding.” *Id.* In evaluating the *Fintiv* factors, we take “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review,” recognizing that “there is some overlap among these factors” and that “[s]ome facts may be relevant to more than one factor.” *Id.*

On June 21, 2022, the Director of the United States Patent and Trademark Office issued a Memorandum setting forth an “Interim Procedure for Discretionary Denials in AIA Post Grant Proceedings with Parallel District Court Litigation” (“Guidance Memo”).¹⁶ The Guidance Memo states that “to benefit the patent system and the public good, the PTAB will not rely on the *Fintiv* factors to discretionarily deny institution in view of parallel district court litigation where a petition presents compelling evidence of unpatentability.” *Id.* at 2.

In the analysis as set forth below, we first consider whether *Fintiv* factors 1–5 weigh in favor of denying institution, and, if so, we must also determine whether the Petition presents compelling merits. *See CommScope Technologies LLC v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 (PTAB Feb. 27, 2023) (precedential) (“*CommScope*”) (“In circumstances where . . . the Board’s analysis of *Fintiv* factors 1–5 favors denial of institution, the Board shall then assess compelling merits.”). For the reasons stated below, we exercise our discretion to deny institution in view of the parallel district court litigation.

1. *Whether a stay exists or is likely to be granted if a proceeding is instituted*

Patent Owner points out that no stay has been requested in the district court litigation. Prelim. Resp. 62. Further, Patent Owner contends that, “even if this IPR was instituted (which would not occur until on or around February 18, 2025) it is unlikely that the Court (Judge Albright) would grant

¹⁶ Available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf.

a stay, particularly given the very advanced stage of the [district court litigation] at that point and the proximity to the trial date.” *Id.*

Petitioner argues institution would “enable the Board to resolve core issues in, if not completely moot, the [district court litigation]. As such, the District Court likely would stay the case.” Pet. 73–74.

On the present record, neither party has produced evidence that the district court has considered a stay in the district court litigation based on this proceeding. Further, *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 12 (PTAB May 13, 2020) (informative), cautions against speculating whether the district court would grant a stay if one were requested.

Accordingly, this factor is neutral.

2. *The Trial Date in the Related District Court Litigation*

The projected statutory deadline for issuance of a final written decision in this proceeding is in February 2026, one year from the date of this Decision. Here, Patent Owner argues that the trial is scheduled for July 28, 2025, which is nearly 7 months before the statutory deadline. Prelim. Resp. 61–63. Patent Owner further argues the median time from filing to case disposition in the Western District of Texas (where the district court litigation is pending) is 28.3 months and “[g]iven that the [district court litigation] was filed on April 26, 2023, . . . the 28.3 month median time to disposition indicates disposition of the [district court litigation] by the beginning of September, 2025—about six months before the statutory deadline.” Prelim. Resp. 63 (citation and emphasis omitted).

Petitioner acknowledges the scheduled July 28, 2025 trial date, but argues scheduled trial dates are unreliable and often change so a court’s

scheduled trial date is not by itself a good indicator of when the district court trial will occur. Pet. 74 (citing Guidance Memo at 8)).

Given that both the scheduled trial date and the median time-to-trial data suggest trial may occur about at least six months prior to our statutory deadline, this factor weighs in favor of exercising our discretion to deny institution.

3. *Investment in the Parallel Proceeding by the District Court and the Parties*

We consider now the amount and type of work already completed in the district court and by the parties at the time of the institution decision. *See Fintiv*, Paper 11 at 9.

Patent Owner contends that, by the time of the institution decision, the parties and the court have invested significant effort, including claim construction briefing by the parties, a claim construction hearing in August 2024, and issuance of a claim construction order by the court in September 2024. Prelim. Resp. 63–64. Patent Owner further contends Patent Owner served preliminary infringement contentions in February 2024, Petitioner served preliminary invalidity contentions in April 2024, and fact discovery is scheduled to close on February 24, 2025, which is only a few days after the expected date of the institution decision. *Id.* at 64.

Petitioner argues:

The [district court l]itigation is in its early stages, and no discovery has been taken yet beyond initial infringement and invalidity contentions and document productions associated therewith. The parties and the District Court have therefore invested relatively minimal resources to date, such that this factor weighs against discretionary denial.

Pet. 74.

The Board’s precedential *Fintiv* order provides the following guidance:

[I]f, at the time of the institution decision, the district court has issued substantive orders related to the patent at issue in the petition, this fact favors denial.[] Likewise, district court claim construction orders may indicate that the court and parties have invested sufficient time in the parallel proceeding to favor denial.

Fintiv, Paper 11 at 9–10.

Given that both the court and the parties have invested significant effort in connection with claim construction and preliminary infringement and invalidity contentions, we consider this factor weighs in favor of exercising our discretion to deny institution.

4. *Overlap Between Issues Raised in the Petition and in the Parallel Proceeding*

This factor evaluates “concerns of inefficiency and the possibility of conflicting decisions” when substantially identical prior art is submitted in both the district court and the *inter partes* review proceeding. *Fintiv*, Paper 11 at 12.

Petitioner states:

Petitioners stipulate that, if the IPR is instituted, Petitioners will not pursue in the [district court l]itigation the same grounds asserted in this Petition. This “mitigates to some degree the concerns of duplicative efforts.” Moreover, this Petition challenges unasserted Claims 3 and 12, such that their invalidity will not be addressed in that proceeding.

Pet. 75 (citing *Sand Revolution II, LLC v. Continental Intermodal Group—Trucking LLC*, IPR2019-01393, Paper 24 at 12 (PTAB June 16, 2020) (“*Sand Revolution*”)).

Patent Owner argues:

Rather than offer a full *Sotera* stipulation that would have barred Petitioner from pursuing any ground raised *or that could have been reasonably raised in this IPR* if this IPR is instituted, Petitioners offered a much more limited *Sand* stipulation stating that, if this IPR is instituted “Petitioners will not pursue in the [district court l]itigation *the same grounds* asserted in the Petition.” Under the present facts, this stipulation is so narrow as to be meaningless. To gain two bites at the apple, Petitioners have laid the groundwork to advance the identical (or cumulative) prior art and virtually identical arguments in the Parallel Proceedings as advanced in these proceedings, by rearranging the combinations to technically get around the narrow *Sand* stipulation.

Prelim. Resp. 65–67 (citing *Sotera Wireless, Inc. v. Masimo Corporation*, IPR2020-01019, Paper 12, at 18–19 (PTAB Dec. 1, 2020) (“if IPR is instituted, [Petitioner] will not pursue in the District Court Litigation any ground raised or that could have been reasonably raised in an IPR”) (“*Sotera*”); *Sand Revolution*, paper 24 at 11–12).

Here, as Petitioner points out, the Petition challenges claims 3 and 12, of which the issue of validity will not be addressed in the district court litigation. Pet. 75. Further, Petitioner stipulates that it will not pursue in the district court litigation the same grounds asserted in this Petition if this IPR is instituted. *Id.* Although we agree with Patent Owner (Prelim. Resp. 65–67) that Petitioner’s stipulation is narrower than a *Sotera* stipulation, Petitioner’s stipulation does reduce the overlap relating to the challenge presented in the Petition and “mitigates to some degree the concerns of duplicative efforts between the district court and the Board, as well as concerns of potentially conflicting decisions.” *See Sand Revolution*, Paper 24 at 12.

We consider this factor weighs marginally against discretionary denial.

5. *Identity of Petitioner and the Defendant in the Underlying Litigation*

“If a petitioner is unrelated to a defendant in an earlier court proceeding, the Board has weighed this fact against exercising discretion.” *Fintiv*, Paper 11 at 13–14.

TCL Electronics Holdings Ltd. and TCL Industries Holdings Co., Ltd. are the defendants in the district court litigation. Pet. 75; Prelim. Resp. 67–68; *see also* Ex. 2007, 1 (claim construction order identifying parties).

Petitioner contends this factor “weighs slightly in favor of denial” and Patent Owner contends this factor “weighs against institution.” Pet. 75; Prelim. Resp. 67–68.

Because Petitioner here is a defendant in the parallel district court litigation, this factor favors denial of institution under § 314(a). *See also Sotera*, Paper 12 at 19 (citing *Fintiv*, Paper 15 at 15; *Sand Revolution*, Paper 24 at 12–13).

6. *Other Circumstances That Impact the Board’s Exercise of Discretion, Including the Merits*

Under the sixth *Fintiv* factor, we consider “other circumstances that impact the Board’s exercise of discretion, including the merits.” *Fintiv*, Paper 11 at 6.

Petitioner argues this factor “weighs against discretionary denial” because “the Grounds present compelling, meritorious challenges to the ’443 [patent] claims. Each of the references are direct hits on the alleged distinctions between the prior art considered by the examiner and the claimed invention.” Pet. 75. Patent Owner argues that “Petitioners’ challenge is weak. Accordingly, the Petition not only fails to meet the

‘reasonable likelihood’ standard under 35 U.S.C. § 314(a) but fails to meet the higher ‘compelling merits’ standard under Factor 6.” Prelim. Resp. 68.

Under *CommScope*, if we determine that *Fintiv* factors 1–5 favor discretionary denial, we must also consider whether the Petition presents compelling merits. See *CommScope*, Paper 23 at 4–5. That is, we take “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review” when evaluating these factors. *Fintiv*, Paper 11 at 6. As discussed above, factor 1 is neutral, factors 2, 3 and 5 weigh in favor of discretionary denial of institution, and factor 4 weighs marginally against discretionary denial. We, therefore, conclude that the evidence of record on factors 1–5 favors exercising our discretion to deny institution of an *inter partes* review. Accordingly, following *CommScope*, where, as here, our analysis of the first five *Fintiv* factors favors denial of institution, we address the merits of the Petition to determine whether the merits are compelling.

As discussed below, we have further determined that the Petition does not show compelling evidence of unpatentability under factor 6. Therefore, we are persuaded that the interests of efficiency and integrity of the system would be best served by invoking our authority under § 314(a) to deny institution of this Petition.¹⁷

¹⁷ Petitioner also contends the Board should not decline institution pursuant to *General Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 (PTAB Sept. 6, 2017) (precedential) (“*General Plastic*”) and 35 U.S.C. § 325(d). Pet. 76–77. As Patent Owner does not make any arguments in connection with *General Plastic* or § 325(d) (see generally Prelim. Resp.), *General Plastic* and/or § 325(d) is not at issue, and we need not address Petitioner’s contentions in connection with *General Plastic* or § 325(d).

III. ANALYSIS – COMPELLING MERITS

A. Claim Construction

We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art (POSITA) at the time of the invention and in the context of the entire patent disclosure. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc).

Petitioner does not propose any claim construction. *See* Pet. 5–6. Patent Owner also does not propose construction for any claim term. Prelim. Resp. 20–24. However, Patent Owner argues that “[w]hen a patentee describes the features of the ‘present invention,’ it is well-settled that ‘this description limits the scope of the invention.’” *Id.* at 20 (quoting *Pacing Techs., LLC v. Garmin Int’l, Inc.*, 778 F.3d 1021 (Fed. Cir. 2015)). Thus, Patent Owner argues:

the claim language reciting “for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains,” requires that the separate clocks in the plurality of domains be globally-asynchronous.

Id. at 20–21.

According to Patent Owner, “the claims should do [sic] not be read to cover schemes like Sarmenta’s^[18] where frequencies are related by a ‘rational factor’ that significantly restricts the possible choices of frequencies to those related by the ‘rational factor.’” Prelim. Resp. 24; *see also id.* at 21–24.

We do not perceive a need to construe any claim terms of the ’443 patent for purposes of determining whether to institute trial. *See, e.g., Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (holding that “only those terms need to be construed that are in controversy, and only to the extent necessary to resolve the controversy”))); *see also Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (applying *Vivid Techs.* in the context of an *inter partes* review).

B. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, “would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406

¹⁸ “Sarmenta” refers to “L. F. G. Sarmenta, G. A. Pratt, and S. A. Ward. Rational Clocking. *In Proceedings of the International Conference on Computer Design*, Austin, Tex., October 1995,” and is reference 27 in the ’443 patent. Ex. 1001, 3:53–55.

(2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

C. Level of Skill in the Art

The level of skill in the art is a factual determination that provides a primary guarantee of objectivity in an obviousness analysis. *See Al-Site Corp. v. VSI Int’l Inc.*, 174 F.3d 1308, 1324 (Fed. Cir. 1999) (citing *Graham*, 383 U.S. at 17–18 (1966); *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991)). Generally, it is easier to establish obviousness under a higher level of ordinary skill in the art. *See Innovention Toys, LLC v. MGA Entm’t, Inc.*, 637 F.3d 1314, 1323 (Fed. Cir. 2011) (“A less sophisticated level of skill generally favors a determination of nonobviousness . . . while a higher level of skill favors the reverse.”).

Petitioner, relying on the testimony of Dr. Bagherzadeh, contends that a “would have at least a Master’s degree in electrical engineering, computer engineering, computer science, or a related field, with at least two or more years of experience in the field of processor design, with an allowance for additional education or experience that might substitute for those requirements.” Pet. 11 (citing Ex. 1003 ¶ 38). Patent Owner does not contest Petitioner’s proposal or offer an alternative. On this record, we are persuaded that Petitioner’s proposal is consistent with the technology described in the Specification and the cited prior art. For purposes of this Decision, we adopt Petitioner’s proposed level of skill.

D. Claims 1, 3, 4, 5, 8, 10, and 12 as obvious over Njølstad (ground II.A); Claims 5 and 10 as obvious over Njølstad and Liljeberg (ground II.B)

Petitioner contends that Njølstad renders obvious claims 1, 3, 4, 5, 8, 10, and 12 of the '443 patent. Pet. 28–38 (ground II.A). Petitioner further contends that Njølstad and Liljeberg render obvious claims 5 and 10 of the '443 patent. Pet. 39–42 (ground II.B).

In response, Patent Owner contends that ground II.A fails because Njølstad's pipelined architecture relies on synchronized clock rates and does not teach independent clock frequency generation as required by the challenged claims. Prelim. Resp. 28–34. Patent Owner further contends ground II.B fails because Liljeberg does not cure the shortcomings of Njølstad. *Id.* at 34.

We briefly summarize Njølstad and Liljeberg below.

1. Njølstad (Ex. 1009)

Njølstad, titled “A Socket Interface for GALS Using Locally Dynamic Voltage Scaling for Rate-Adaptive Energy Saving,” discloses a low-power amendment to the GALS paradigm where a proposed socket interface provides locally dynamic voltage scaling (LDVS) adapted to actual processing rate requirements. Ex. 1009, Title, Abstract. Local clock generation by ring oscillators tracks local device speed at local supply voltage. *Id.* at Abstract.

Njølstad describes “[a]n integrated digital transceiver may be partitioned as in Figure 3, where all the modules with their individual performance and latency requirements are clustered into separate supply voltage regions.” *Id.* at § IV.A.

Figure 3 is reproduced below.

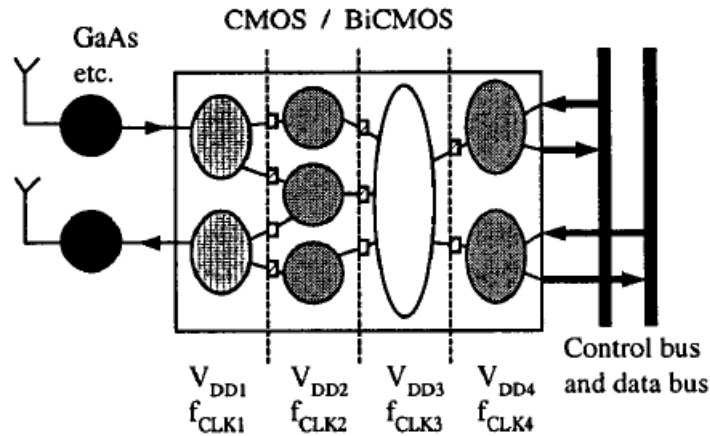


Figure 3: A model of a wideband radio access system using multiple supply voltages and logic level shifters.

Figure 3 above illustrates a model of a radio access system with voltages V_{DD1} , V_{DD2} , V_{DD3} , and V_{DD4} , and parameters f_{CLK1} , f_{CLK2} , f_{CLK3} , and f_{CLK4} . *Id.* at Fig. 3; *see also id.* at § IV.C (“regulating and distributing different supply voltages to the different regions in Figure 3 are regarded as more challenging”).

Njølstad describes “control signal RATE-REQUIREMENT_i” that is used to “scale down the local supply voltage such that the locally generated clock rate is just high enough to perform the actual processing task and to produce output data at the given rate.” *Id.* at § IV.D. Figure 5 is reproduced below.

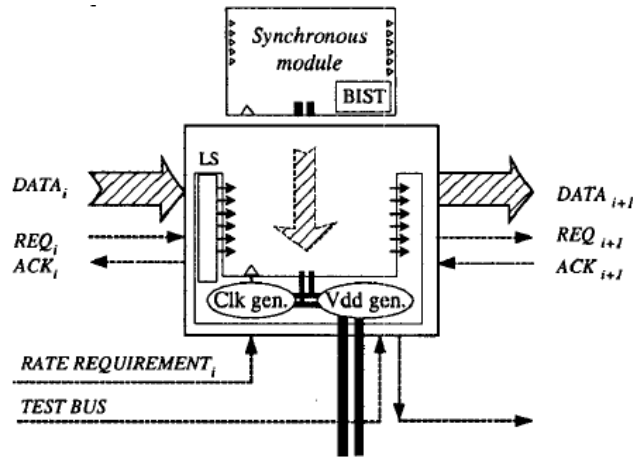


Figure 5: A synchronous version of the actual processing element (DSP module) is inserted into the Socket Interface.

Figure 5 above illustrates $\text{RATE REQUIREMENT}_i$ being input to a “Clk gen.” portion. *Id.* at Fig. 5.

Njølstad summarizes:

We have described GALS-LDVS, a low-power amendment to the GALS paradigm where locally rate-adapted dynamic voltage scaling can be provided by means of the proposed Socket Interface. Local clock generation by using local ring oscillator tracks the local device speed. The module’s speed is proportional to the device speed with the same dependence of local power supply level, process parameters and temperature variations.

Id. at § V.

2. Liljeberg (Ex. 1010)

Liljeberg, titled “Asynchronous Interface for Locally Clocked Modules in ULSI Systems,” describes an approach to construct globally asynchronous, locally synchronous ULSI systems. Ex. 1010, Title, Abstract. Liljeberg describes a [first-in first-out (FIFO)] queue in the form of a dual-port RAM. *Id.* at §§ 3, 6.

Figure 2 is reproduced below.

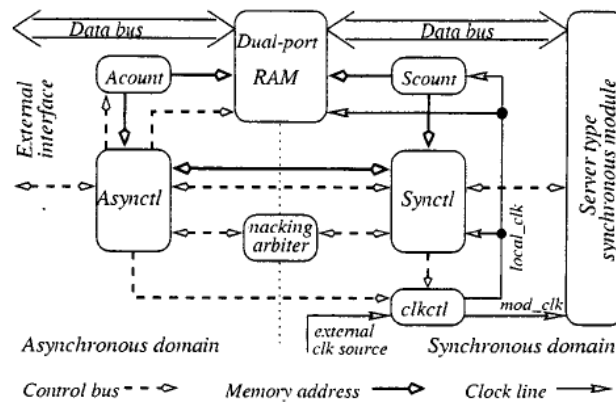


Figure 2: Server-type SAInt architecture

Figure 2 above illustrates the dual-port RAM between a synchronous domain and an asynchronous domain. Ex. 1010 § 3,

3. Claims 1, 3, 4, 5, 8, 10, and 12 as obvious over Njølstad (ground II.A) and Claims 5 and 10 as obvious over Njølstad and Liljeberg (ground II.B)

In grounds II.A and II.B, although Petitioner contends that Njølstad renders obvious the challenged claims of the '443 patent (Pet. 28–38), Patent Owner contends that Njølstad's pipelined architecture relies on synchronized clock rates and does not teach independent clock frequency generation as required by the challenged claims (Prelim. Resp. 28–34). We focus on claim limitations “the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others” recited in independent claim 1 and similarly recited in independent claim 8.

“the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains”

With respect to this limitation, relying on the testimony of Dr. Bagherzadeh for support, Petitioner contends Njølstad teaches that, in a given domain, a local frequency (“Clk gen.”) is based on local processing

demands (“RATE REQUIREMENT_i”) and scaled accordingly. Pet. 30–31 (citing Ex. 1003 ¶ 106; Ex. 1009, § IV.D (“[a] clock signal with the correct frequency [is] given by the logical depth of the synchronous module”)). According to Petitioner, Njølstad implements a dynamically changeable frequency for each domain. *Id.* (citing Ex. 1003 ¶ 107). However, Petitioner does not address the limitation “independently of the frequencies . . . for others of the plurality of domains,” as required by the claims. *See id.* at 29–31.

Here, Patent Owner argues that Njølstad’s pipelined architecture relies on synchronized clock rates and does not teach independent clock frequency generation as required by the challenged claims. Prelim. Resp. 28–34. Patent Owner provides the evidentiary testimony of Dr. Kaeli, to support its contention that, as shown in Figure 3, Njølstad depicts a *pipelined* architecture for a wireless wideband radio access system and, thus, Njølstad relies on synchronized clock rates to maintain system performance. *Id.* at 29 (citing Ex. 2001 ¶ 56). According to Patent Owner, as supported by Dr. Kaeli’s testimony:

in pipelined architecture, input is received, and the input is then serially processed through a series of stages to generate an output that is much like an assembly line in a factory. Accordingly, each respective processing stage receives input from a prior stage, performs processing, and generates an output that is subsequently used by another stage.

Prelim. Resp. 29–30 (citing Ex. 2001 ¶ 57). Patent Owner argues that, “Dr. Kaeli’s explanation of a pipelined architecture is consistent with Njølstad’s description of Fig. 3. For example, Njølstad states, ‘in Figure 3 many tasks are performed at a fixed rate (or at a temporally fixed rate),’ and ‘[e]ach processing element . . . receives an input data set and produces an output

data set at this fixed rate.” *Id.* at 30 (citing Ex. 1009¹⁹ § IV.D; Ex. 2001 ¶ 62). Thus, Njølstad “emphasizes the critical importance of maintaining synchronized rate requirements between processing elements in a pipelined architecture to ensure balanced operation and prevent system failures.” *Id.* (citing Ex. 2001 ¶¶ 55–57). That is, “the rate at which data is generated in one stage cannot be faster than the data consumed in the subsequent stage.” *Id.* at 31–32 (citing Ex. 2001 ¶ 57).

Thus, although Petitioner contends that Njølstad implements a dynamically changeable frequency for each domain wherein a local “rate requirement can dynamically be configured” such that “the locally generated clock rate is just high enough to perform the actual processing task” at that rate (Pet. 31 (citing Ex. 1009 § IV.D)), such teaching merely supports Petitioner’s contention that the frequency is dynamically changeable at the local level (*id.*). However, as Patent Owner points out, such showing is not a compelling disclosure of the frequency generation being independent of the frequencies of the other domains, as required by the challenged claims. Prelim. Resp. 28–34.

For the foregoing reasons, we conclude that Petitioner has not presented compelling merits that Njølstad teaches “the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains” as recited in claim 1 and similarly recited in claim 8.

¹⁹ In several places in this portion of the Preliminary Response, Patent Owner refers to Exhibit 1005 rather than Exhibit 1009. In our summary of Patent Owner’s arguments above, we have corrected these references.

E. Claims 1, 3, 4, 5, 8, 10, and 12 as obvious over Iyer (ground I); Claims 1, 3, 4, 5, 8, 10, and 12 as obvious over Soerensen (ground III.A); Claims 1, 3, 4, 5, 8, 10, and 12 as obvious over Soerensen and Hemani (ground III.B); and Claims 5 and 10 as obvious over Soerensen and Moore (ground III.C)

Petitioner argues that claims 1, 3, 4, 5, 8, 10, and 12 are rendered obvious by Iyer (ground I). Pet. 15–28. Petitioner further contends that claims 1, 3, 4, 5, 8, 10, and 12 are also rendered obvious by Soerensen (ground III.A) (*id.* at 43–54), or by Soerensen in view of Hemani (ground III.B) (*id.* at 55–70), and that claims 5 and 10 are rendered obvious by Soerensen in view of Moore (ground III.C) (*id.* at 70–73). Patent Owner contends that Iyer and Soerensen are not prior art (Prelim. Resp. 1–19). We focus on whether Iyer and Soerensen are prior art.

We briefly summarize Iyer, Soerensen, Hemani, and Moore below.

1. Iyer (Ex. 1005)

Iyer is entitled “Power Efficiency of Voltage Scaling in Multiple Clock, Multiple Voltage Cores.”

Petitioner contends Iyer is a conference paper from the IEEE/ACM International Conference on Computer-Aided Design, held November 10–14, 2002 and was publicly available no later than November 10, 2002.

Pet. 3.

Iyer studies the effect of using a GALS organization and proposes a modeling and simulation environment “for multiple clock cores with static or dynamically variable voltages for each synchronous block.” Ex. 1005, Abstract. Iyer reports the authors were able to assess the power/performance tradeoffs available for “Multiple Clock, Dynamic Voltage (MCDV) cores.” *Id.* Additionally, “[b]y exploiting the flexibility of independent dynamic voltage scaling the various clock domains, the power efficiency of GALS

designs can be improved by 12% on average, and up to 20% more in select cases.” *Id.*

Iyer further describes:

GALS systems contain several independent synchronous blocks which operate with their own local clocks and communicate asynchronously with each other. The main feature of these systems is the absence of a global timing reference and the use of several distinct local clocks (or clock domains), possibly running at different frequencies.

Id. at § 1. Iyer describes a proposal of “a multiple-clock dynamic-voltage core processor where the speed and voltage of each synchronous block are adapted dynamically based on the application profile.” *Id.* at § 3.4.

2. *Soerensen (Ex. 1006)*

Soerensen, titled “Dynamic Voltage Control Method and Apparatus,” discloses “[a] dynamic power controller . . . that identifies a clock frequency requirement of a processor and determines a voltage requirement to support the clock frequency requirement.” Ex. 1006, code (57); *see also* Ex. 1006 ¶ 48, claim 11.

The application from which Soerensen issued was filed on August 29, 2002 (Ex. 1006, codes (21), (22)) and claimed the benefit of a provisional application filed August 29, 2001 (Ex. 1006, code (60) (“Soerensen Provisional Application”). Petitioner contends at least Soerensen’s claim 1 and all of Soerensen’s disclosures relied upon in the Petition find support in the provisional application. Pet. 3 n.2.

Soerensen surmises that “one way to reduce the power consumption of a device is to dynamically adjust the frequency of the clock signals provided to a processor to reflect the clock frequency requirement of the

processor.” Ex. 1006 ¶ 23; *see also* Ex. 1006 ¶¶ 81–83 (describing adjustment of frequency to 45 MHz and 240 MHz).

Soerensen describes:

three major clock domains generated from system clock signal 82 and the PLL clock signal 84; clock domain 90a, clock domain 90b, and clock domain 90c. The components of processor 20 operate within these clock domains. . . . The clock signals in each clock domain are provided by various select, divider, and gating logic and distributed to the components of the processor via a plurality of clock trees 50a-50h. . . . Additionally, clock control 110 may divide the frequency of clock signal 84 in order to provide the components of the processor with clocks signals having reduced frequencies in order to meet the clock frequency requirement of the processor.

Ex. 1006 ¶¶ 36, 37, 38; *see also* Ex. 1006, claim 6, claim 10.

Soerensen additionally describes a “method of dynamically adjusting the power supplied to a processor according to the present invention . . . [where] the clock frequency requirement is evaluated in order to determine a voltage requirement necessary to support the new clock frequency requirement.” Ex. 1006 ¶¶ 57, 58.

3. *Hemani (Ex. 1007)*

Hemani, titled “Lowering power consumption in clock by using Globally Asynchronous Locally Synchronous design style,” discloses “[p]ower consumption in clock of large high performance VLSIs can be reduced by adopting Globally Asynchronous, Locally Synchronous design style (GALS).” Ex. 1007, Title, Abstract. According to Hemani, “GALS architecture is composed of *large* synchronous blocks (SBs) which communicate with each other on an asynchronous basis” and “the frequency at which each SB is clocked can be tailored to the local needs, thus reducing

the average frequency and the overall power consumption.” *Id.* at § 1.

Power consumption in VLSI systems is reduced by reducing voltage. *Id.*

Hemani further describes:

In the GALS architecture local clocks are required for the SBs. There are two possibilities, either to have an independent local clock generator or to use a global reference clock signal with frequency multiplier in SBs to achieve the desired higher frequency.

Id. at § 3.4.

Hemani additionally describes that “[l]ocal clock generators based on ring oscillators have many advantages such as robustness, small size and low power consumption . . . [and t]here are many ways to manipulate the frequency of the ring oscillator.” *Id.* at § 3.4. “[D]ynamic voltage scaling of the power supply voltage at each SB containing a ring oscillator is made.”

Id.

4. *Moore (Ex. 1008)*

Moore, titled “Channel Communication Between Independent Clock Domains,” discloses a low-latency channel communication between independent clock domains may be achieved using a combination of clock pausing techniques, self-calibrating delay lines, and an asynchronous interconnect. Ex. 1008, Title, Abstract. Moore states such a scheme could be used for point-to-point communication in a GALS system. *Id.* at Abstract.

Figure 5 is reproduced below.

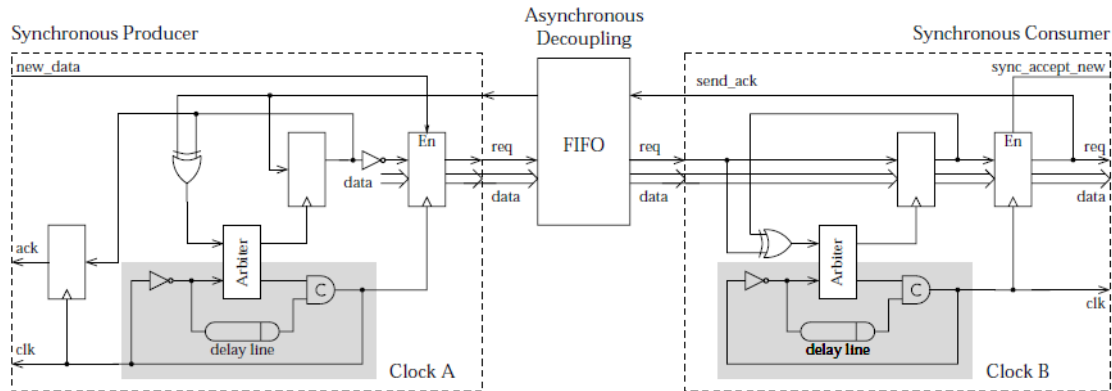


Figure 5: Channel communication with FIFO buffering

Figure 5 illustrates a FIFO asynchronous decoupling between a synchronous producer and synchronous consumer. Ex. 1008, Fig. 5.

5. *Claims 1, 3, 4, 5, 8, 10, and 12 as obvious over Iyer (ground I); Claims 1, 3, 4, 5, 8, 10, and 12 as obvious over Soerensen (ground III.A); Claims 1, 3, 4, 5, 8, 10, and 12 as obvious over Soerensen and Hemani (ground III.B); and Claims 5 and 10 as obvious over Soerensen and Moore (ground III.C)*

Although Petitioner contends that the challenged claims are rendered obvious by Iyer (ground I), Soerensen (ground III.A), or by Soerensen in view of Hemani (ground III.B), and that claims 5 and 10 are rendered obvious by Soerensen in view of Moore (ground III.C) (Pet. at 15–28, 43–73), Patent Owner contends that “the claimed invention was conceived and actually reduced to practice by February 2002, predating at least the Iyer (EX1005) and Soerensen (EX1006) reference” (Prelim. Resp. 1).

Iyer and Soerensen as prior art

Petitioner contends Iyer was publicly available no later than November 10, 2002 and, accordingly, Iyer qualifies as prior art under at least § 102(a)–(b). Pet. 3. Petitioner also contends the application from which Soerensen issued was filed on August 29, 2002, claiming priority to the

Soerensen Provisional Application, filed on August 29, 2001, and therefore Soerensen qualifies as prior art under at least § 102(e). *Id.*

However, Patent Owner argues that Iyer published after the invention to the '443 patent was actually reduced to practice. Prelim. Resp. 27–28. In particular, Patent Owner provides evidentiary testimonies of Dr. Kaeli (Ex. 2001) and Mr. Albonesi (Ex. 2003) to support its contends the '443 patent incorporates by reference a paper authored by the inventors and published in February 2002 (Ex. 2005), which demonstrates conception by providing a full written description of the claimed invention. Prelim. Resp. 6–16. According to Patent Owner, a simulation described in the paper embodied the invention in a tangible form, wherein the simulation described in the paper showed that the invention worked for its intended purpose. *Id.* at 16–19 (citing Exs. 2001, 2003, 2005).

Similarly, Patent Owner contends that the application from which Soerensen issued was filed on August 29, 2002, which is after the invention date of the '443 patent. Prelim. Resp. 35. According to Patent Owner, while Soerensen claims priority to the Soerensen Provisional Application (Ex. 1022), the passages from Soerensen relied on in the Petition are not entitled to the benefit of the filing date of the Soerensen Provisional Application because the subject matter was not disclosed in the manner provided by 35 U.S.C. § 112. *Id.*

We recognize potential merits to Patent Owner's position. That is, we do not find compelling Petitioner's contention that the challenged claims would have been obvious Iyer or Soerensen.

F. Summary

Based on the record before us, Patent Owner has raised substantial issues with Petitioner's analysis of the challenged independent claims, so

that the evidence does not indicate compelling merits in Petitioner’s case. For the reasons given, we determine that Petitioner has not presented a “compelling, meritorious challenge[]” to any claim of the ’443 patent. *Id.* Accordingly, we find that the sixth *Fintiv* factor does not weigh against discretionary denial.

G. Balancing the Fintiv Factors

We have considered the circumstances and facts before us in view of the *Fintiv* factors. As discussed above, we have determined that factors 1–5 weigh in favor of discretionary denial of institution. Moreover, we have further determined that the Petition does not show compelling evidence of unpatentability under factor 6. We therefore conclude that the evidence of record favors exercising our discretion to deny institution of an *inter partes* review.

IV. CONCLUSION

Upon consideration of the Petition, the Preliminary Response, and the evidence presented, we exercise our discretion under 35 U.S.C. § 314(a) to deny institution of an *inter partes* review challenging claims 1, 3, 4, 5, 8, 10, and 12 of the ’443 patent.

V. ORDER

For the reasons given, it is

ORDERED that the Petition is *denied*, and no trial is instituted.

IPR2024-01245
Patent 7,089,443 B2

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