

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Inter Partes Review

Cisco Systems, Inc.,
Petitioner,
v.

Lionra Technologies Limited,
Patent Owner.

IPR2024-01281
U.S. Patent No. 7,738,471

**DECLARATION OF THOMAS BROOKS IN SUPPORT OF
PATENT OWNER'S RESPONSE**

TABLE OF CONTENTS

I.	INTRODUCTION.....	1
II.	QUALIFICATIONS.....	2
III.	SCOPE OF WORK	4
IV.	LEVEL OF ORDINARY SKILL IN THE ART.....	4
V.	OVERVIEW OF THE '471 PATENT	7
A.	Assumed Effective Filing and Invention Dates	7
B.	The '471 Patent	7
C.	Claims and Claim Construction	11
VI.	WHY THE '471 PATENT CLAIMS ARE NOT INVALID.....	13
A.	The Nelson Patent Does Not Disclose “Concurrently Writing ...”.....	13
1.	The Nelson patent	15
2.	The Nelson patent does not disclose “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory”.....	20

I, Thomas Brooks, of Staunton, Virginia, declare that:

I. INTRODUCTION

1. Lionra Technologies Limited has retained me as an independent expert in connection with IPR2024-01281 to provide testimony regarding the technology involved in U.S. Patent No. 7,738,471 (“the ’471 Patent”) and how the inventions described and claimed therein compare with the asserted prior art. I have been asked to provide my technical review, analysis, insights, and opinions regarding the references set forth in the above-referenced IPR by Petitioner Cisco Systems.

2. I am being compensated for my work in this matter at my standard hourly rate for consulting services at \$200 per hour. My compensation is not dependent on the outcome of the case and does not affect the substance of my statements in this Declaration. I have no financial interest in the matter or the Challenged Patent.

3. I have reviewed the specification and the claims of the ’471 Patent, the prosecution history for the ’471 Patent, Cisco’s Petition, the declaration of Cisco’s expert, Dr. Mir, the prior art references, and the Court’s claim construction order in the related District Court Case. I am familiar with the technology involved therein, having practical, hands-on experience in the field for over twenty-five years.

II. QUALIFICATIONS

4. I received a Bachelor of Science degree in computer engineering from the Virginia Polytechnic Institute and State University, commonly referred to as Virginia Tech, in 1998. Since receiving that degree, I have worked extensively in the design of computer networking and computer systems, including both in hardware design and software design.

5. Immediately after graduation from Virginia Tech, I worked for International Business Machines Corp. (“IBM”) as part of an engineering team responsible for the design of a Gigabit Ethernet switch. My specific responsibilities included the design of the Media Access Control (“MAC”) component that could accommodate network traffic at 10 Mbit/s, 100 Mbit/s and 1000 Mbit/s (1 Gbit/s). Over a period of approximately two years, I was involved in designing the MAC architecture from scratch and designing the hardware implementation of the MAC in Hardware Definition Language (“HDL”).

6. After departing IBM, I worked for GE Fanuc, the joint venture between General Electric Corp. (“GE”) and Fanuc Automation Corp. At GE Fanuc, I was part of an engineering team responsible for a microprocessor-based control system for Programmable Logic Controllers (“PLC”). My specific responsibilities included the design of multiple Application Specific Integrated Circuits (“ASIC”) to

interface with industrial automation and the PLC systems as well as the software implementation for Profibus network connectivity for the control system.

7. After GE Fanuc, I worked for Intransa, a start-up focused on providing network-based storage solutions, for several years. I was responsible for the hardware design via HDL of a Field Programmable Gate Array (“FPGA”) to provide an Ethernet-based network interface to ATA-based, including parallel ATA and serial ATA (“SATA”), hard disk storage. This included the complete design, from scratch, of an Ethernet and Internet Protocol (“IP”) based network end-point. I also contributed to the hardware design for the ATA hard disk controller implemented in the FPGA. I was also responsible for the software design for a microprocessor in the FPGA to process ATA commands received via the Internet Protocol.

8. I departed Intransa in 2005 and began consulting work, which I have continued to present, for ADI Engineering, the Barr Group and NOW Solutions. As part of this consulting work, I have designed and implemented network-based solutions in FPGAs for the defense industry, including for General Dynamics. The design and implementation of these network components was done from scratch and involved Ethernet, IP, and Transmission Control Protocol (“TCP”).

9. A copy of my *curriculum vitae* is attached as Ex. 2006.

III. SCOPE OF WORK

10. I have been asked to consider and provide my opinions on the claims of the '471 Patent, including the technical subject matter and the application of various references that allegedly predate the priority date of the '471 Patent. In particular, I have been asked to consider what one of ordinary skill in the art would have understood from the claims and specification of the '471 Patent, and whether certain references would have disclosed or suggested the features recited in the claims of the '471 Patent to a person of ordinary skill in the art at the time of filing of the '471 Patent.

11. My opinions set forth below are based on my education, training, experience, and the content of the references considered.

IV. LEVEL OF ORDINARY SKILL IN THE ART

12. My opinions are provided based on what a person of ordinary skill in the art in the technical field of the inventions of the '471 Patent would have understood at the time of filing of the '471 Patent.

13. I have been informed and understand that the content of a patent and prior art should be interpreted the way a person of ordinary skill in the art would have interpreted those references at the time of filing of the patent. I understand that

the person of ordinary skill is a hypothetical concept referring to one who understands the technology and associated conventional wisdom at the time.

14. I was asked to provide an opinion as to the level of one of ordinary skill in the art pertinent to the subject matter set forth in the '471 Patent at the time of the priority date. Around September 14, 2007 (the filing date of U.S. Application No. 11/855,714 that matured into the '471 Patent), it is my opinion that a person of ordinary skill in the art in the field of the '471 Patent would have, at the time of the respective inventions of the '471 Patent: (1) a Bachelor's degree in computer science, computer engineering, or electrical engineering and at least two years of experience in computer networking, including packet-based networking such as the Internet Protocol, or (2) equivalent work experience in the design and/or implementation of systems involving computer networking. As reflected in the level of ordinary skill, a person of ordinary skill can have equivalent education and work experience. Additional education in the field could be substituted for industry experience, and vice versa. Throughout this declaration, I use the term "POSITA" to refer to a person with these or similar qualifications.

15. The basis for my familiarity with the level of ordinary skill is my interaction with large numbers of workers in the network system and computer security industry who were at this level of skill. In reaching this opinion as to the

hypothetical person of ordinary skill in the art, I have considered the types of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level and professional capabilities of workers in the field. I further note that, based on my extensive experience designing computer networking products prior to September 14, 2007, I was at least at this level of skill.

16. I understand that Dr. Mir, Cisco's expert, contends that a POSITA "would have been someone knowledgeable and familiar with network communications techniques and high speed packet processing technologies available in the mid-2000s. Such a POSITA would have a bachelor's degree in computer science, computer engineering, electrical engineering, or equivalent training, and approximately two years of experience working in the field of network communications. Additional work experience can substitute for specific educational background, and vice versa." Ex. 1003, ¶ 20. As of September 14, 2007, based on my extensive experience designing computer networking products, I was at least at this level of skill.

V. OVERVIEW OF THE '471 PATENT

A. Assumed Effective Filing and Invention Dates

17. The '471 Patent is entitled “High Speed Packet Processing in a Wireless Network” and was filed on September 14, 2007. *See* Ex. 1001. I assume the priority date for the '471 Patent is the filing date of the patent application, September 14, 2007.

B. The '471 Patent

18. The '471 Patent is generally directed to “a method and apparatus for high speed protocol header processing at an intermediate and/or destination node of a packet-based communications network.” *Id.*, 1:8-11. The '471 Patent describes that header processing can have a negative effect on network latency, the time it takes a packet to traverse a network, because “packet transmission often experiences relatively long delays due to protocol header processing at intermediate and/or destination nodes.” *Id.*, 1:63-65. The '471 Patent notes that “[m]any solutions have been proposed for decreasing the protocol header processing time at intermediate and/or destination nodes of a packet-based communications networks.” *Id.*, 1:66-2:1. The '471 Patent describes some of these solutions and their associated drawbacks, including a “sequential processing approach,” *id.*, 2:2-44, and “fixed function applications specific integrated circuits (ASICs) and field programmable

gate arrays (FPGAs),” *id.*, 2:45-56. In the Detailed Description section, the ’471 Patent presents the some of the drawbacks of the prior art approaches, including that “[e]ach of the protocol stack layers use the packet buffer memory 122 to copy its respective header into its own processing memory for receive processing,” *id.*, 5:51-54, and that after “decoder 516 ... performs actions to forward a portion of a decoded packet 300 that is absent of a preamble and physical layer information to a packet buffer memory 520 ... each protocol stack layer processes its respective layer information in a sequential manner,” *id.*, 10:43-48.

19. The ’471 Patent asserts that “[i]n view of the” prior art solutions and their drawbacks, “there is a need for a solution to reduce protocol header processing time in a packet-based communications networks.” Ex. 1001, 2:57-59. The Summary of the Invention section of the ’471 Patent presents the solution:

The invention concerns a method for processing a packet at an egress end user node. The method includes a decoding step and a concurrent writing step. The decoding step involves decoding a packet having a plurality of headers. The concurrent writing step is performed subsequent to the decoding step. The concurrent writing step involves concurrently writing (1) each of the headers to a packet buffer memory and (2) each individual one of the headers to a respective protocol stack layer memory where it is available for immediate processing within a protocol stack layer.

Id., 3:6-15; *see also id.*, claims 1 and 13.

20. Further description is provided in the Detailed Description section, beginning with a discussion of Figure 1:

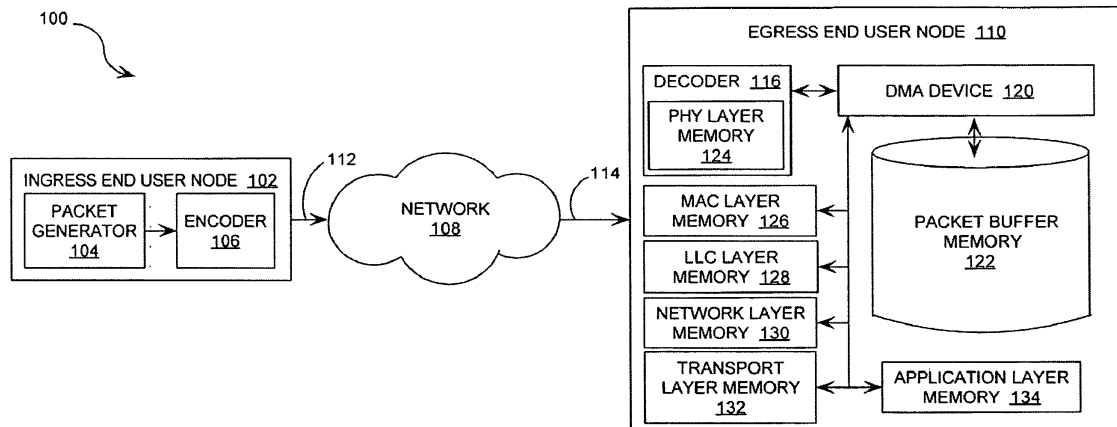


FIG. 1

Ex. 1001, Fig. 1. “FIG. 1 is a block diagram of a packet-based communications system 100. The packet-based communications system 100 is comprised of an ingress end user node (IEUN) 102, a network 108, and an egress end user node (EEUN) 110.” *Id.*, 4:38-41.

21. “The EEUN 110 is an intermediate or destination node.” Ex. 1001, 4:63-64. “The EEUN 110 can be a destination computer system, a routing device, a battery powered wireless communications device, or any other device having a TCP/IP based packet interface.” *Id.*, 4:67-5:2. The ’471 Patent describes that the EEUN is electrically or optically connected to a “packet-based communications

network,” such as “an internet protocol (IP) based communications network and a transmission control protocol/internet protocol (TCP/IP) based communications network,” through a network link. *Id.*, 4:58-63. The ’471 Patent further describes the EEUN and its major structural components, including a decoder, a DMA device, a packet buffer memory and multiple protocol stack layer's internal memory spaces, with respect to Figure 1:

As shown in FIG. 1, the EEUN 110 is comprised of a decoder 116, a direct memory access (DMA) device 120, and a packet buffer memory 122. The EEUN 110 is also comprised of a media access control (MAC) layer memory 126, a logic link control (LLC) layer memory 128, a network layer memory 130, a transport layer memory 132, and an application layer memory 134.

Id., 5:3-9.

22. “The decoder 116 is configured to receive an encoded packet from the network 108” and “[u]pon receipt of the encoded packet, the decoder 116 performs actions involving the decoding of the encoded packet.” Ex. 1001, 5:9-12. “The decoder 116 is also configured to advantageously forward a portion of a decoded packet that is absent of preamble and physical layer information to the DMA device 120.” *Id.*, 5:18-21; *see also id.*, 9:19-23, 9:28-31.

23. As part of the solution of the ’471 Patent to reduce protocol header processing time, “a DMA device is used to concurrently write the specific layer header fields directly into: (a) each protocol stack layer's internal memory spaces

126, . . . , 134 to initiate immediate processing; and (b) the packet buffer memory 122.” *Id.*, 5:64-6:1; *see also id.*, 6:14-21 (“The DMA device 120 is also configured to concurrently communicate data to the packet buffer memory 122” and the protocol stack layer's internal memory spaces, such as the “the media access control (MAC) layer memory 126, the logic link control (LLC) layer memory 128, the network layer memory 130, the transport layer memory 132, and the application layer memory 134,” and “allows the transfer of data to these various memory locations in a single DMA transaction.”); *id.*, 9:41-45 (“Upon receipt of the portion of the decoded packet 300, the DMA device 120 performs write operations to concurrently write the headers 306, 308, 310, 312, 314, and the application data 316 to the packet buffer memory 122 and a respective layer memory 126, 128, 130, 132, 134.”).

C. Claims and Claim Construction

24. Independent claim 1 of the '471 Patent recites:

- [1.0] A method for processing a packet at an egress end user node, comprising:
- [1.1] decoding a packet having a plurality of headers; and
- [1.2] subsequent to said decoding step, ***concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory*** where it is available for immediate processing within a protocol stack layer.

Ex.1001, 11:51-59 (emphasis added).

25. Independent claim 13 of the '471 Patent recites:

[13.0] An egress end user node (EEUN) of a packet based communications system, comprising:

[13.1] a decoder configured for decoding a packet having a plurality of headers; and

[13.2] a direct memory access (DMA) device coupled to said decoder and configured for ***concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory*** where it is available for immediate processing within a protocol stack layer.

Ex.1001, 12:33-43 (emphasis added).

26. For the highlighted phrase “concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory” in the independent claims, I have been asked to apply the following claim construction, as determined by the Court in the related District Court case, in my analysis: Plain meaning, *i.e.*, “concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory.” *See* Ex. 2002, May 13, 2025 *Memorandum Opinion and Order*, at 8.

VI. WHY THE '471 PATENT CLAIMS ARE NOT INVALID.

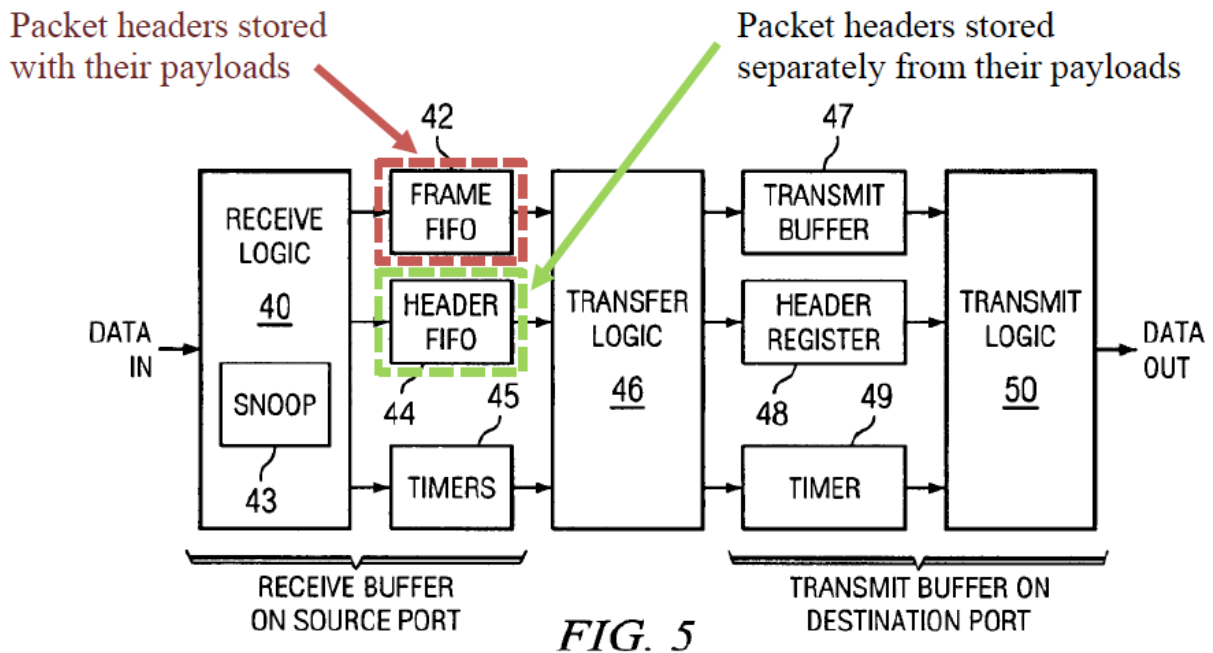
A. The Nelson Patent Does Not Disclose “Concurrently Writing ...”

27. For the limitations of independent claims 1 and 13, the Petition and Dr. Mir rely on a combination of three references. The first reference is U.S. Patent Publ. No. 2006/0072564 to Cornett et al. (Ex. 1005, “the Cornett patent”) and is entitled “Header replication in accelerated TCP (Transport Control Protocol) stack processing.” The second reference is U.S. Patent Publ. No. 2006/0209840 to Paatela et al. (Ex.1007, “the Paatela patent”) and is entitled “System and method for providing transformation of multi-protocol packets in a data stream.” The third reference is U.S. Patent No. 7,333,489 to Nelson et al. (Ex.1006, “the Nelson patent”) and is entitled “System and method for storing frame header data.” *See* Petition at 32-45, 55-56; Ex. 1003, ¶¶ 68-93, 113-116.

28. The Petition and Dr. Mir rely solely on the Nelson patent to satisfy the “concurrently writing” requirement of claims 1 and 13. I disagree that the Petition and Dr. Mir have shown that the Nelson patent satisfies the “concurrently writing” requirement of claims 1 and 13. More specifically, I disagree that the Petition and Dr. Mir have shown that the Nelson patent discloses “concurrently writing ... (2) each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory.”

29. First, the Petition and Dr. Mir only address whether the Nelson patent discloses “concurrently writing” of packet headers to a “packet buffer” and to a “protocol layer memory.” They do not address whether the Nelson patent discloses “concurrently writing ... (2) each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory.” More specifically, the Petition argues:

A POSITA would have understood Nelson to teach that the packet’s header is *written* (1) to a frame FIFO 42 (header and payload) (**red** outline) and (2) to the header FIFO 44 (header only) (**green** outline). This process is performed in parallel, i.e., *concurrently*. This is shown in Fig. 5:



Petition at 42-43; *see also* Ex. 1003, ¶ 89. The Petition and Dr. Mir similarly state that “Nelson teaches writing a packet frame (header and payload) into one buffer

and the packet headers into another buffer, with the two writing operations occurring in parallel.” Petition at 30; *see also* Ex. 1003, ¶ 65 (“In Nelson, a full packet frame is written into one buffer and the packet headers are written into another buffer in parallel.”). This does not address how the Nelson patent can satisfy “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory.”

30. Second, for multiple reasons, the Nelson patent does not disclose “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory” and therefore the Petition does not show that the combination of the Cornett patent, the Paatela patent, and the Nelson patent satisfies all of the limitations of the ’471 Patent. Before I provide those reasons, I will provide some background, from the perspective of a person of ordinary skill in the art, on the disclosure of the Nelson patent.

1. *The Nelson patent*

31. The Nelson patent is generally directed to a system implementation for a Fibre Channel switch. *See* Ex. 1006, 3:49-57. The Nelson patent also describes the serial communication link nature of Fibre Channel: “Each Fibre Channel link consists of a pair of unidirectional fibers. Each fiber is connected to an associated

transmitter and receiver. The link is connected between a pair of data ports. Data is transmitted from a first one of the ports to a second one of the ports over a first one of the fibers (and the corresponding transmitter and receiver.)” *Id.*, 4:4-9; *Cf.* Ex. 2007, *Fibre Channel Framing And Signaling (FC-FS) Specification, Rev. 0.50* (“Fibre Channel Specification”), 46 (“This international standards describes the physical and signaling interface of a high performance serial link for support of the Upper Level Protocols (ULPs) associated with HIPPI, IPI, SCSI, IP and others.”).

32. The Nelson patent, with respect to Fig. 3 and consistent with the Fibre Channel Specification, describes the Fibre Channel frame structure and its applicability to general Fibre Channel switching concepts:

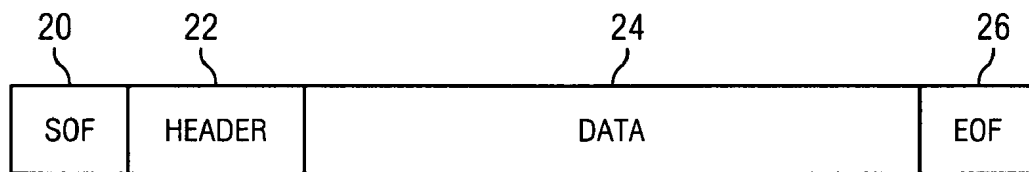


FIG. 3

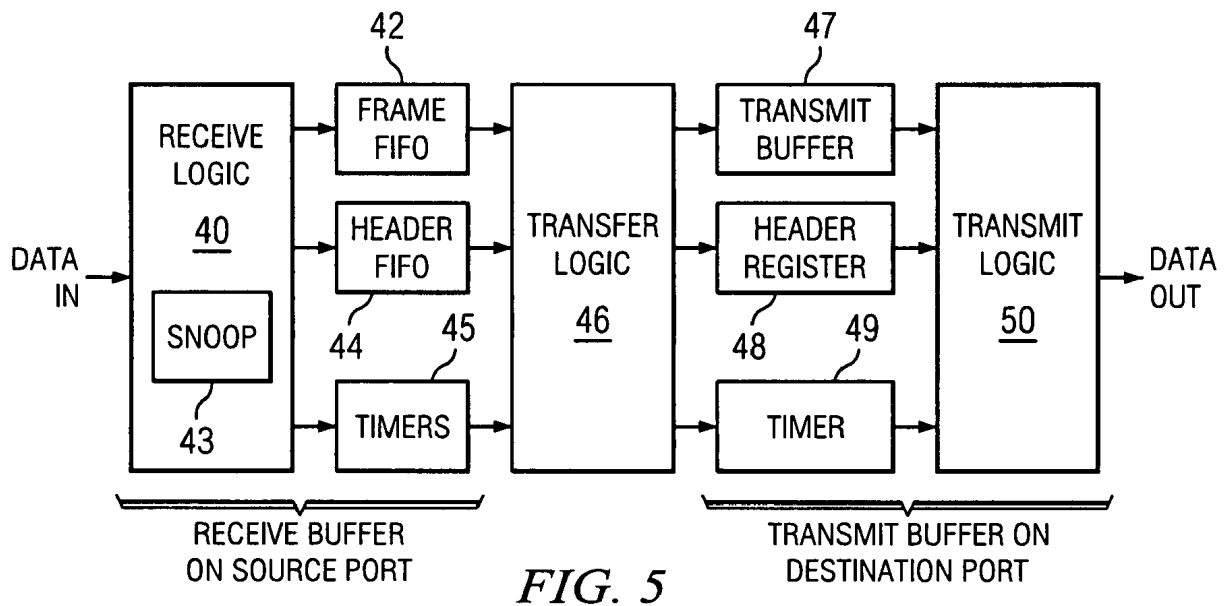
Ex. 1006, Fig. 3; *Cf.* Ex. 2007, *Fibre Channel Specification*, 117 (Figure 21 - FC-2 general frame format).

Referring to FIG. 3, a block diagram illustrating the structure of a frame in one embodiment is shown. In this embodiment, each frame includes a start-of-frame (SOF) primitive 20, a header 22, data 24, and an end-of-frame (EOF) primitive 26. SOF primitive 20 identifies the beginning of a frame. EOF primitive 26 similarly serves to identify the end of the frame. All of the data of a frame, whether useful data or

overhead data, is enclosed between the SOF and EOF primitives. Header 22 comprises overhead data related to the frame. In particular, Header 22 includes information identifying the destination of the frame. The destination information is used by the switches to make the routing decisions necessary to deliver the frame to the target site or device. Data 24 comprises useful data. In other words, data 24 is the data which the was originally intended to be delivered from the source to the destination.

Ex. 1006, 4:34-49; *Cf.* Ex. 2007, Fibre Channel Specification, 121 (“All FC-2 frames follow the general frame format as shown in Figure 21. A FC-2 frame is composed of a Start_of_Frame delimiter, frame content, and an End_of_Frame delimiter. The frame content is composed of a Frame_Header, Data_Field, and CRC. Unless otherwise specified, the term frame refers to a FC-2 frame within FC-FS.”), 117-121 (describing Start_of_Frame (SOF), Frame_Header, Data Field, CRC, and End_of_Frame (EOF)).

33. The Nelson patent describes the structure of the Fibre Channel switch further with respect to Fig. 5:



Ex. 1006, Fig. 5.

Referring to FIG. 5, a block diagram illustrating an embodiment of the present system which includes timers corresponding to the frame and header information is shown. In this figure, data which is transmitted to a port is received by receive logic 40. Receive logic 40 is configured to detect the SOF and EOF primitives which define the boundaries of frames in the received data and to store individual frames to locations in frame FIFO 42. Receive logic 40 includes circuitry to snoop on the received data and to copy the header of each frame to header FIFO 44. The copying of a header to header FIFO 44 occurs in parallel with the storage of the corresponding frame in frame FIFO 42.

Id., 6:59-7:4.

34. The Nelson patent further describes the operation of the Fibre Channel switch when a Fibre Channel frame is received on the switch's port:

Data which is received at a port is examined for the SOF primitive which identifies the beginning of a frame. When the SOF primitive is

detected, the port makes a decision to store the corresponding frame in a frame FIFO 30 of the port. The frame (i.e., all of the data received by the port, from the SOF primitive up to and including the EOF primitive) is stored in one of the storage locations 31 in FIFO 30. Frames are read out of FIFO 30 and transmitted in the order in which they were written to the FIFO.

Id., 4:5-60.

35. The Fibre Channel switch of the Nelson patent further includes “[r]eceive logic in the port [that] stores frames of data in the storage elements of a FIFO buffer and concurrently snoops on the frame data to obtain header information.” *Id.*, 2:13-15. “The header information is stored in a buffer separate from the FIFO that stores the frames.” *Id.*, 2:15-17; *see also id.*, 3:16-18 (“In one embodiment, the invention comprises a buffer system wherein header information is stored in a buffer separate from the FIFO that stores the frame itself.”); 5:4-5 (“In addition to frame buffer 30, the port includes a header buffer 34.”). As the Nelson patent further explains, the “header buffer” “eliminates the need to read part of the frame out of the FIFO and store this data in another buffer while a routing decision is made.” *Id.*, 3:30-22. The “header buffer” may be composed of “register elements” or “dual port RAM” “to store the header information.” *Id.*, 2:26-29, 5:60-63, 6:8-12.

36. The Nelson patent describes the operation of the switch when a frame is received. As noted above, “the SOF primitive signals the beginning of a frame

and is followed by the frame header.” *Id.*, 5:5-6. “[W]hen frames first arrive at a port, the frames are ‘snooped’ (i.e., examined) and the information in the header field is copied to a frame header register.” *Id.*, 2:27-39, 3:26-28. The Nelson patent further describes that “[t]he port snoops on the received data and, as the header is received, the port copies the header to a FIFO which serves as header buffer 34.” *Id.*, 5:7-9. As also noted above, the Nelson patent discloses that the “receive logic” (element 40 in Fig. 5) is responsible for storing frame data “in the storage elements of a FIFO buffer” and “concurrently snoop[ing] on the frame data to obtain header information” that the “receive logic” copies to the “header buffer.” *See id.*, 2:13-15, 6:66-7:4. The Nelson patent does not disclose any memory as part of the “receive logic” circuitry. *See id.*, 6:59-7:4.

2. *The Nelson patent does not disclose “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory”*

37. It is my opinion that a POSITA would recognize that the Nelson patent does not disclose the claimed requirement of “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory” of the independent claims of the ’471 Patent and therefore the Petition does not show that the combination of the Cornett patent,

the Paatela patent, and the Nelson patent satisfies all of the limitations of the '471 Patent.

38. **First**, the Nelson patent discloses only the single Fibre Channel header per frame as the header information that is written to the header buffer, or header FIFO. More specifically, with respect to Fig. 3, reproduced below, the Nelson patent describes that the “Header 22 includes information identifying the destination of the frame. The destination information is used by the switches to make the routing decisions necessary to deliver the frame to the target site or device.” Ex. 1006, 4:43-47.

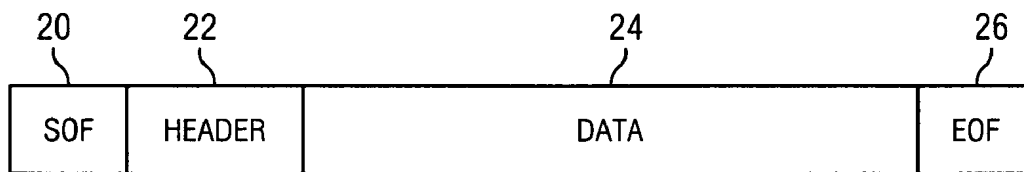


FIG. 3

Id., Fig. 3. The Fibre Channel frame header is 24-Bytes in length and is constituted as follows:

Bits	
Word	3124231615080700
0	R_CTLD_ID
1	CS_CTLS_ID
2	TYPEF_CTL
3	SEQ_IDDF_CTLSEQ_CNT
4	OX_IDRX_ID
5	Parameter

Figure 23 - Frame_Header

Ex. 2007, Fibre Channel Specification, 124. The individual fields of the frame header are described on page 124-145 of the Fibre Channel Specification.

39. The frame header is immediately followed by the data field: “The frame content shall be transmitted sequentially following the SOF delimiter as an ordered byte stream within the definition of the frame as specified in Figure 21, Figure 23, and Figure 24 until the EOF delimiter is transmitted.” Ex. 2007, Fibre Channel Specification, 121.

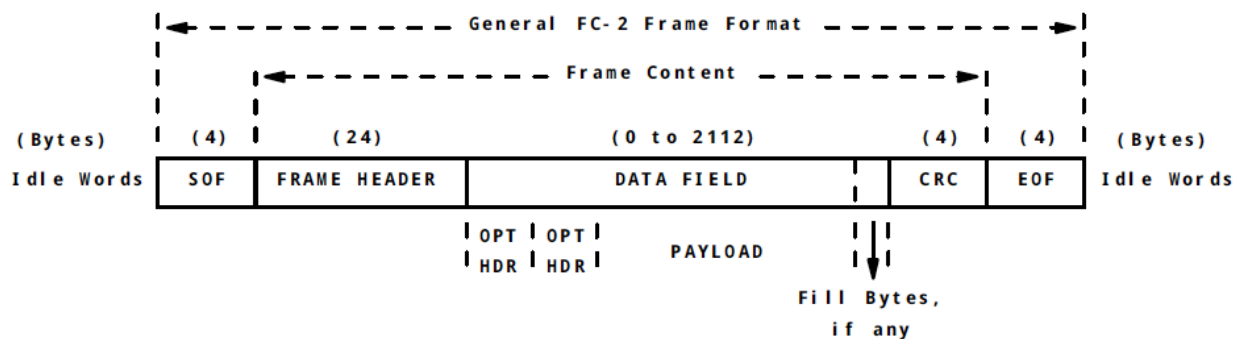


Figure 21 - FC-2 general frame format

Ex. 2007, Fibre Channel Specification, 117; *see also id.*, 121 (Figure 22 - Frame byte order).

40. While the Fibre Channel Specification does provide for optional headers, *see id.*, 117 (Figure 21), 146 (Figure 24), these optional headers would be included as part of the data field. The Nelson patent treats the “data 24,” which it terms “useful data,” as separate from the “header 22,” which it terms “overhead data”: “All of the data of a frame, whether useful data or overhead data, is enclosed between the SOF and EOF primitives. Header 22 comprises overhead data related to the frame. ... Data 24 comprises useful data. In other words, data 24 is the data which the was originally intended to be delivered from the source to the destination.” Ex. 1006, 4:40-49. The Nelson patent discloses that only the header is stored in the header buffer, or header FIFO. *See id.*, 2:13-17 (“Receive logic in the port stores frames of data in the storage elements of a FIFO buffer and concurrently snoops on the frame data to obtain header information. The header information is stored in a buffer separate from the FIFO that stores the frames.”), 6:66-7:1 (“Receive logic 40 includes circuitry to snoop on the received data and to copy the header of each frame to header FIFO 44.”). A POSITA would recognize that the Nelson patent only discloses writing a single header to the header buffer, or header FIFO. A POSITA would therefore recognize that the Nelson patent does not disclose or suggest that

multiple headers are written to the header buffer, or header FIFO. Consequently, a POSITA would recognize that the Nelson patent does not disclose “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory,” as required by the independent claims of the ’471 Patent.

41. **Second**, even if a POSITA thought that the Nelson patent discloses multiple headers per frame as being written to the header buffer (or header FIFO), a POSITA would still recognize that the multiple headers are not “concurrently written” to the header buffer, or header FIFO.

42. The Fibre Channel Specification requires an encoding scheme, termed 8b/10b encoding, for transmission over a serial link. *See* Ex. 2007, Fibre Channel Specification, 84 (“Information to be transmitted over a Fibre shall be encoded eight bits at a time into a 10-bit Transmission Character and then sent serially by bit. Information received over a Fibre shall be collected ten bits at a time, and those Transmission Characters that are used for data, called Data Characters, shall be decoded into the correct eight-bit codes. The 10-bit Transmission Code supports all 256 eight-bit combinations.”); *see also id.*, 84-91. The Fibre Channel Specification also requires that valid transmissions be word aligned at 4-Bytes (with Bytes, after encoding, being termed “characters”). *Id.*, 91 (“A Transmission Word is composed

of four contiguous Transmission Characters treated as a unit. A word prior to transmission and after reception is composed of a combination of four Valid Data Bytes and Special Codes treated as a unit.”). Consequently, all valid contents of a frame, including the SOF, EOF, CRC, Frame Header, and Data, must be divisible in 4 character increments. *See id.*, 91, 92-93.

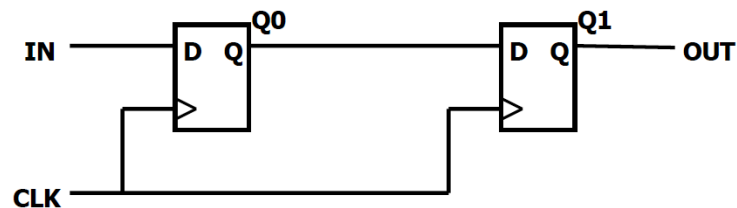
43. The Nelson patent discloses that the “receive logic is [1] configured to detect the SOF and EOF primitives which define the boundaries of frames ... [2] to store individual frames to locations in frame FIFO 42 ... and [3] to snoop on the received data and to copy the header of each frame to header FIFO 44.” Ex. 1006, 6:63-7:1. A POSITA, understanding this disclosure and the Fibre Channel Specification’s Transmission Word requirement, would recognize that the “receive logic” processes an incoming transmission four characters at a time. For example, the “receive logic” can only recognize a SOF based upon several candidate sequences of characters. *See* Ex. 2007, Fibre Channel Specification, 92.

44. Because the Nelson patent does not disclose that the “receive logic” has any storage memory, *see* ¶ 36, Ex. 1006, 6:59-7:4, and based upon the Nelson patent’s disclosure that “[t]he port snoops on the received data and, as the header is received, the port copies the header to a FIFO which serves as header buffer 34,” *id.*, 5:7-9, a POSITA would recognize that the “receive logic” is processing and storing

data in the frame FIFO and the header FIFO in 4 character (4 Bytes after decoding) segments. For the 24-Byte Fibre Channel header, 6 sequential cycles would be required to store the entire header in the “frame FIFO” and the “header FIFO.” This segmented operation is confirmed by the Nelson patent’s disclosure that “[t]he port snoops on the received data and, *as the header is received*, the port copies the header to a FIFO which serves as header buffer 34.” *Id.*, 5:7-9 (emphasis added). This segmented operation is further confirmed by the Nelson patent’s disclosure of “header register elements to store the header information,” and where the “header register elements each comprise a *chain of cascaded flip-flops* ... which is sufficiently large to *hold a frame header*.” *Id.*, 5:60-63 (emphasis added). To a POSITA, “a chain of cascaded flip-flops,” as illustrated below, refers to a chain of flip-flops where the output of one flip-flop feeds the input of another flip-flop with all the flip-flops being clocked at the same time. This is often referred to as a shift register, also illustrated below.

CASCADED FLIP-FLOPS

- Shift register: new value to first stage
while second state obtains current value of first stage
- Outputs change only on clock tick



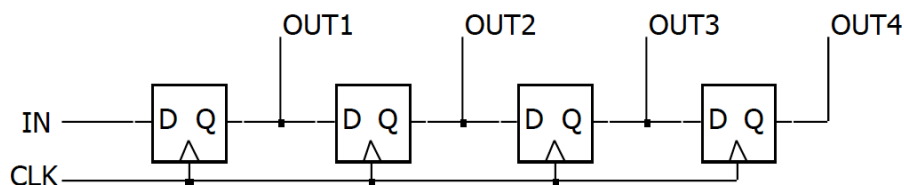
Ex. 2008, University of Washington, Paul G. Allen School of Computer Science and Engineering, CSE467: Advanced Logic Design, Sequential Logic Lecture Notes, at

11 (available at

https://courses.cs.washington.edu/courses/cse467/00wi/lectures/ppt/Sequential_Logic/index.htm, last visited June 18, 2025).

SHIFT REGISTER

- Holds samples of input
 - store last 4 input values in sequence
 - 4-bit shift register:



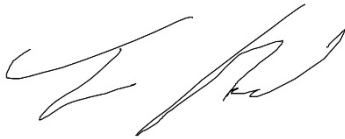
Id., at 14.

45. The use of “a chain of cascaded flip-flops ... sufficiently large to hold a frame header” indicates to a POSITA that multiple clock cycles are required to store a single header. A POSITA would therefore recognize that a single header is stored in the header buffer or header FIFO sequentially. A POSITA would consequently recognize that the Nelson patent does not disclose “concurrently writing” the single header nor does it disclose “concurrently writing” multiple headers to the header buffer or header FIFO. It is therefore my opinion that the Nelson patent does not disclose “concurrently writing ... (2) each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory,” as required by the independent claims of the '471 Patent.

Declaration of Thomas Brooks
Inter Partes Review IPR2024-01281
U.S. Patent No. 7,738,471

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, undersection 1001 of Title 18 of the United States Code.

Date: June 18, 2025

A handwritten signature in black ink, appearing to be 'T. Brooks', written in a cursive style.

Thomas Brooks