

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.

Petitioner,

v.

LIONRA TECHNOLOGIES LIMITED,

Patent Owner.

Case IPR2024-01281
U.S. Patent 7,738,471

PATENT OWNER’S RESPONSE TO THE PETITION

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Exhibit No.	Description
2001	January 2, 2025 <i>Defendant's P.R. 4-2 Disclosure, Lionra Technologies Limited v. Cisco Systems, Inc.</i> , Case No. 2:24-cv-97 (E.D. Tex.)
2002	May 13, 2025 <i>Memorandum Opinion and Order, Lionra Technologies Limited v. Cisco Systems, Inc.</i> , Case No. 2:24-cv-97 (E.D. Tex.)
2003	April 30, 2025 Letter from B. Rosenthal to B. Cooper
2004	March 19, 2025 <i>Defendant Cisco Systems, Inc.'s Responsive Claim Construction Brief, Lionra Technologies Limited v. Cisco Systems, Inc.</i> , Case No. 2:24-cv-97 (E.D. Tex.)
2005	Declaration of Thomas Brooks in Support of Patent Owner's Response
2006	<i>Curriculum Vitae</i> of Thomas Brooks
2007	Fibre Channel Framing and Signaling (FC-FS) Specification, Rev. 0.50 (September 21, 2000)
2008	University of Washington, Paul G. Allen School of Computer Science and Engineering, CSE467: Advanced Logic Design, Sequential Logic Lecture Notes
2009	U.S. Patent No. 8,929,262

I. INTRODUCTION

Patent Owner respectfully requests that the Board find all of Petitioner's challenges to claims 1-3, 5-10, 12-15 and 17-21 ("the Challenged Claims") of U.S. Patent No. 7,738, 471 ("the '471 Patent") without merit. More specifically, the Board should find the claims of the '471 Patent not unpatentable because Petitioner fails to show invalidity for any independent claim. Petitioner asserts that *Cornett* in combination with *Paatela* and *Nelson* disclose the limitations for independent claims 1 and 13. However, neither *Cornett*, *Paatela*, nor *Nelson* disclose a method or system for "concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory." This phrase, as properly construed, requires not only "concurrently writing" of a "plurality of headers to a packet buffer memory ... and ... to a respective protocol stack layer memory," but also "concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory." Neither *Cornett*, *Paatela*, nor *Nelson* disclose the writing of "each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory." Consequently, Petitioner cannot establish that the limitations of the independent

claims are satisfied by the prior art and therefore cannot establish that any of the claims of the '471 Patent are unpatentable.

II. BURDEN OF PROOF

To prevail in an *inter partes* review, Petitioner must show by a preponderance of the evidence that a patent is invalid. 35 U.S.C. § 316(e). “In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); *see also Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (“It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify with particularity the ‘evidence that supports the grounds for the challenge to each claim.’”) (quotations omitted). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review). “Unlike district court litigation—where parties have greater freedom to revise and develop their arguments over time and in response to newly discovered material—the expedited nature of IPRs bring with it an obligation for petitioners to

make their case in their petition to institute. While the Board's requirements are strict ones, they are requirements of which petitioners are aware when they seek to institute an IPR." *Intelligent Bio-Systems*, 821 F.3d at 1369.

Given the importance of particularity, the *inter partes* review rules set out in 37 C.F.R. § 42.104(b) specify the precise requirements for a petition to seek relief. Not only must the challenged claims and the specific statutory grounds for unpatentability be identified, but 37 C.F.R. § 42.104(b)(3) requires the Petition to identify how each "claim is to be construed." Rule 42.104(b)(4) then requires the Petition to identify how each "***construed claim is unpatentable*** under the statutory grounds identified." 37 C.F.R. § 42.104(b)(4)(emphasis added). As the Board has explained, "the construction proposed by the Petitioner" must be "one that Petitioner ***believes is the correct construction*** under applicable law and should apply in the involved proceeding." *Toyota Motor Corp. v. BlitzSafe Texas, LLC*, IPR2016-00422, Paper 12, at 26 (PTAB Jul. 6, 2016) (emphasis added); *see also LG Elecs. Inc. v. Core Wireless Licensing S.A.R.L.*, IPR2016-00986, Paper 12, at 12 (PTAB Aug. 22, 2016) ("Petitioner is responsible to assert in its own petitions before the Board . . . the claim construction that it desires and urges the Board to adopt.").

III. THE '471 PATENT

The '471 Patent is titled “High Speed Packet Processing in a Wireless Network.” *See* Ex. 1001. The '471 Patent is generally directed to “a method and apparatus for high speed protocol header processing at an intermediate and/or destination node of a packet-based communications network.” *Id.*, 1:8-11. The '471 Patent describes that header processing can have a negative effect on network latency, the time it takes a packet to traverse a network, because “packet transmission often experiences relatively long delays due to protocol header processing at intermediate and/or destination nodes.” *Id.*, 1:63-65.

The '471 Patent notes that “[m]any solutions have been proposed for decreasing the protocol header processing time at intermediate and/or destination nodes of a packet-based communications networks.” Ex. 1001, 1:66-2:1. The '471 Patent describes some of these solutions and their associated drawbacks, including a “sequential processing approach,” *id.*, 2:2-44, and “fixed function applications specific integrated circuits (ASICs) and field programmable gate arrays (FPGAs),” *id.*, 2:45-56. In the Detailed Description section, the '471 Patent presents some of the drawbacks of the prior art approaches, including that “[e]ach of the protocol stack layers use the packet buffer memory 122 to copy its respective header into its own processing memory for receive processing,” *id.*, 5:51-54, and that after “decoder 516

... performs actions to forward a portion of a decoded packet 300 that is absent of a preamble and physical layer information to a packet buffer memory 520 ... each protocol stack layer processes its respective layer information in a sequential manner,” *id.*, 10:43-48.

The '471 Patent asserts that “[i]n view of the” prior art solutions and their drawbacks, “there is a need for a solution to reduce protocol header processing time in a packet-based communications networks.” Ex. 1001, 2:57-59. In the Summary of the Invention section, the '471 Patent presents the solution, which is further reflected in the independent claims:

The invention concerns a method for processing a packet at an egress end user node. The method includes a decoding step and a concurrent writing step. The decoding step involves decoding a packet having a plurality of headers. The concurrent writing step is performed subsequent to the decoding step. The concurrent writing step involves concurrently writing (1) each of the headers to a packet buffer memory and (2) each individual one of the headers to a respective protocol stack layer memory where it is available for immediate processing within a protocol stack layer.

Id., 3:6-15; *see also id.*, 11:51-59 (claim 1), 12:33-43 (claim 13).

The '471 Patent provides further description of the solution in the Detailed Description section, where it begins with a discussion of Figure 1:

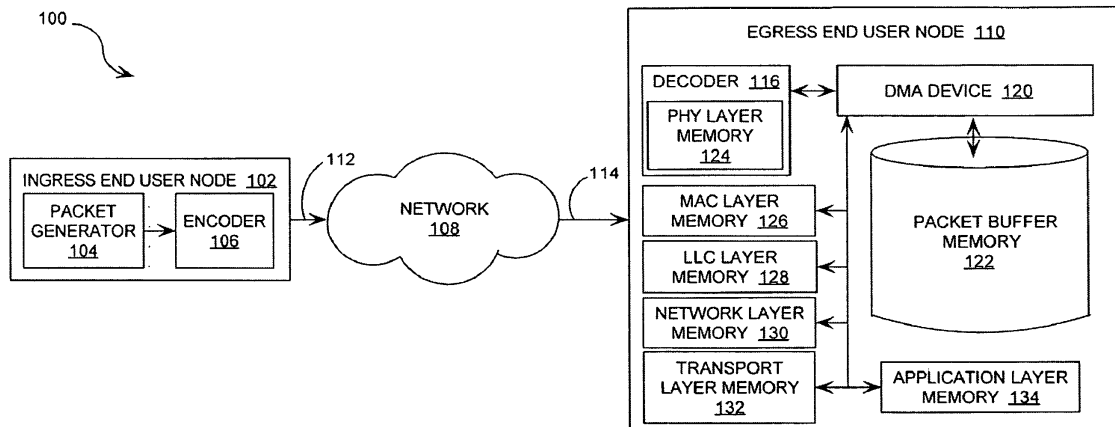


FIG. 1

Ex. 1001, Fig. 1. “Figure 1 is a block diagram of a packet-based communications system 100. The packet-based communications system 100 is comprised of an ingress end user node (IEUN) 102, a network 108, and an egress end user node (EEUN) 110.” *Id.*, 4:38-41.

“The EEUN 110 is an intermediate or destination node.” Ex. 1001, 4:63-64.

“The EEUN 110 can be a destination computer system, a routing device, a battery powered wireless communications device, or any other device having a TCP/IP based packet interface.” *Id.*, 4:67-5:2. The ’471 Patent describes that the EEUN is electrically or optically connected to a “packet-based communications network,” such as “an internet protocol (IP) based communications network and a transmission

control protocol/internet protocol (TCP/IP) based communications network,” through a network link. *Id.*, 4:58-63. The '471 Patent further describes, with respect to Figure 1, the EEUN and its major structural components, including a decoder, a DMA device, a packet buffer memory and multiple protocol stack layer's internal memory spaces:

As shown in FIG. 1, the EEUN 110 is comprised of a decoder 116, a direct memory access (DMA) device 120, and a packet buffer memory 122. The EEUN 110 is also comprised of a media access control (MAC) layer memory 126, a logic link control (LLC) layer memory 128, a network layer memory 130, a transport layer memory 132, and an application layer memory 134.

Id., 5:3-9.

“The decoder 116 is configured to receive an encoded packet from the network 108” and “[u]pon receipt of the encoded packet, the decoder 116 performs actions involving the decoding of the encoded packet.” Ex. 1001, 5:9-12. “The decoder 116 is also configured to advantageously forward a portion of a decoded packet that is absent of preamble and physical layer information to the DMA device 120.” *Id.*, 5:18-21; *see also id.*, 9:19-23, 9:28-31. As part of the solution of the '471 Patent to reduce protocol header processing time, “a DMA device is used to concurrently write the specific layer header fields directly into: (a) *each protocol stack layer's internal memory spaces 126, . . . , 134 to initiate immediate processing*; and (b) the packet buffer memory 122.” *Id.*, 5:64-6:1 (emphasis added);

see also id., 6:14-21 (“The DMA device 120 is also configured to concurrently communicate data to the packet buffer memory 122” and the protocol stack layer's internal memory spaces, such as the “the media access control (MAC) layer memory 126, the logic link control (LLC) layer memory 128, the network layer memory 130, the transport layer memory 132, and the application layer memory 134,” and “allows the transfer of data to these various memory locations in a single DMA transaction.”); *id.*, 9:41-45 (“Upon receipt of the portion of the decoded packet 300, the DMA device 120 performs write operations to concurrently write the headers 306, 308, 310, 312, 314, and the application data 316 to the packet buffer memory 122 and a respective layer memory 126, 128, 130, 132, 134.”).

IV. LEVEL OF ORDINARY SKILL IN THE ART

Patent Owner contends that a POSITA would have, at the time of the respective inventions of the '471 Patent: (1) a Bachelor's degree in computer science, computer engineering, or electrical engineering and at least two years of experience in computer networking, including packet-based networking such as the Internet Protocol, or (2) equivalent work experience in the design and/or implementation of systems involving computer networking. As reflected in the level of ordinary skill, a person of ordinary skill can have equivalent education and work experience. Additional education in the field could be substituted for industry

experience, and vice versa. See Ex. 2005, Brooks Decl., Declaration of Thomas Brooks in Support of Patent Owner's Response ("Brooks Decl."), ¶¶ 14-15. While this level of skill may be slightly different than that proposed by Petitioner, *see* Petition at 13, Patent Owner contends that the differences are immaterial and that the Challenged Claims of the '471 Patent are not unpatentable when applying either proffered level of skill.

V. CLAIM CONSTRUCTION

Claim terms that are in dispute and for which resolution of such dispute is "necessary to resolve the controversy" must be construed. *Realtime, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)); *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997). This threshold for construing claim terms is applicable in *inter partes* review proceedings. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Independent method claim 1 of the '471 Patent recites:

- [1.0] A method for processing a packet at an egress end user node, comprising:
 - [1.1] decoding a packet having a plurality of headers; and
 - [1.2] subsequent to said decoding step, ***concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective***

protocol stack layer memory where it is available for immediate processing within a protocol stack layer.

Ex.1001, 11:51-59 (emphasis added).

Independent apparatus claim 13 of the '471 Patent recites:

[13.0] An egress end user node (EEUN) of a packet based communications system, comprising:

[13.1] a decoder configured for decoding a packet having a plurality of headers; and

[13.2] a direct memory access (DMA) device coupled to said decoder and configured for *concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory* where it is available for immediate processing within a protocol stack layer.

Ex.1001, 12:33-43 (emphasis added).

Consistent with the plain language of the claims, as well as the specification and the prosecution history of the '471 Patent, the phrase “concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory” should be construed to require that the term “concurrently” applies to both the “writing to a packet buffer memory and ... to a respective protocol stack layer memory,” **and** the “writing [of] each individual one of said plurality of headers to a respective protocol stack layer memory.” More specifically: (1) “each of said plurality of headers” must be written “to a packet buffer memory” and “to a respective protocol stack layer

memory” concurrently; **and** (2) “each individual one of said plurality of headers” must be written to each “respective protocol stack layer memory” concurrently.

A. Procedural History

The Petition in the present *inter partes* review was filed on August 26, 2024. *See* Petition at 74-75. The corresponding Notice of Filing Date Accorded was entered and mailed on September 23, 2024. *See* Paper No. 5. Consequently, the deadline for a preliminary response was set for December 23, 2024. *See* 37 CFR § 42.107(b). Patent Owner did not file a preliminary response and review was instituted on March 13, 2025. *See* Paper No. 6.

The Petition asserted that “[f]or the purposes of this proceeding, and the grounds presented herein, Petitioner contends that no claim term requires express construction.” Petition at 13; *see also* Ex. 1003, *Declaration of Nader F. Mir, Ph.D.*, ¶41 (“I have reviewed the entirety of the ’471 patent, as well as its prosecution history. It is my opinion that for purposes of applying the asserted prior art to evaluate the patentability of the Challenged Claims, no terms require express construction.”). However, after the deadline for a preliminary response had passed, Petitioner proposed a construction for the “concurrently writing” phrase and for the “packet buffer” term in the related District Court case, *Lionra Technologies Limited v. Cisco Systems, Inc.*, Case No. 2:24-cv-97 (E.D. Tex.). *See* Ex. 2001, January 2,

2025 *Defendant's P.R. 4-2 Disclosure*, at 4. For “concurrently writing,” Petitioner proposed the construction of: Plain meaning, *i.e.*, “concurrently writing (1) each of said plurality of headers to a CPU main memory space used for the packet transfer and (2) each individual one of said plurality of headers (**each concurrently with each other**) to a respective protocol stack layer memory.” *See id.* (Emphasis added to note the substitution of the proposed construction of “CPU main memory space used for the packet transfer” for “packet buffer memory” and the addition of “(each concurrently with each other).”). Patent Owner subsequently agreed to the construction of “concurrently writing” as “[p]lain meaning, *i.e.*, ‘concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers (**each concurrently with each other**) to a respective protocol stack layer memory,’” and the Court adopted the agreed construction. *See Ex. 2002, May 13, 2025 Memorandum Opinion and Order*, at 8. Patent Owner and Petitioner continued to dispute the construction of “packet buffer memory” and the Court found that the term did not require construction, giving the term its plain and ordinary meaning. *See id.*, at 13.

For the reasons set forth below, Patent Owner contends that the agreed District Court construction of the “concurrently writing” phrase is correct and that the Board should adopt this construction. Moreover, Petitioner contends that this construction,

which is contradictory to the claim construction position proffered in the Petition, is dispositive of the District Court case. *See* Ex. 2003, April 30, 2025 *Letter from B. Rosenthal to B. Cooper*, at 1 (“Lionra’s recent agreement to a claim construction requiring the concurrent writing of a plurality of headers effectively resolves the matter. Cisco’s products, as evidenced by source code for the UADP, Silicon One, and LSE ASICs, do not write the headers concurrently in the manner described.”) (emphasis added).

Petitioner has advocated for a construction in the District Court that it considers dispositive and has provided no explanation of why this construction should not be applicable in this *inter partes* review. Accordingly, the District Court construction should be binding on Petitioner. *See, e.g., Cambridge Mobile Telematics, Inc. v. Sfara, Inc.*, IPR2024-00966, Paper 12 at 8 (PTAB Dec. 13, 2024) (Where a petitioner has proposed a claim term be construed in the District Court proceeding and emphasized the significance and potentially “case dispositive” nature of the proposed construction, “we determine ***the petition is obliged to either apply that construction in this proceeding or explain why that construction is not applicable.***”) (emphasis added); *see also Novartis Pharms. Corp. v. Regents of the University of Michigan*, IPR2023-01346, Paper 8, Dissent at 2 (PTAB Mar. 13, 2024) (Fitzpatrick J.) (Dissenting to institution for failure to meet the requirements of 37

C.F.R. § 42.104(b)(3) and (4), stating that “[a]t the Board, a petitioner should bring a petition for an inter partes review asserting unpatentability based on a construction the petitioner seeks. A petitioner should not seek an *inter partes* review, as was done here, based exclusively on a construction it considers erroneous but ‘adopts’ ‘solely for purposes of this Petition.’”).

B. The Claim Language Dictates the Construction

The independent claims of the '471 Patent recite “concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory.”

Ex.1001, 11:54-57, 12:38-41. As Petitioner has argued with respect to this phrase:

Middle-school grammar rules dictate that a modifier before a numbered list modifies each item in the list. Here, the modifier “concurrently writing” modifies both (1) a plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory. And therefore, the *claims require that the plurality of headers be written concurrently to each of the respective protocol stack layer memories.*

Ex. 2004, March 19, 2025 *Defendant Cisco Systems, Inc.’s Responsive Claim Construction Brief*, at 1 (emphasis added); *see also id.* (identifying claim language as “crystal clear”). Petitioner provided further detail to this argument as follows:

As is readily apparent, the modifier “concurrently writing” applies to both items in the numbered list. As the Federal Circuit has recognized, it is a “general grammatical principle” that a modifier that comes before a series modifies each item in the series. *SIMO Holdings Inc. v. Hong*

Kong uCloudlink Network Tech. Ltd., 983 F.3d 1367, 1377 (Fed. Cir. 2021) (citing Antonin Scalia & Bryan A. Garner, *Reading Law: The Interpretation of Legal Texts* § 19, 147 (2012)). “Th[is] principle has particular force when [like here] the term joining the items in a series is ‘and.’” *Id.* (citing *SuperGuide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 886 (Fed. Cir. 2004)).

Ex. 2004, at 7.

Patent Owner concurs that “a straightforward application of [the] general grammatical principle dictates that ‘concurrently writing’ also modifies the phrase ‘each individual one of said plurality of headers to a respective protocol stack layer memory.’” *Id.* Consequently, the plain and ordinary meaning of the “concurrently writing” phrase requires that the “individual headers” must be written “each concurrently with each other to their respective protocol stack layer memories.”

C. The Specification Confirms the Construction

As set forth above in Section II, the '471 Patent discloses that “a DMA device is used to concurrently write the specific layer header fields directly into: (a) *each protocol stack layer's internal memory spaces 126, . . . , 134 to initiate immediate processing*; and (b) the packet buffer memory 122.” Ex. 1001, 5:64-6:1 (emphasis added); *see also id.*, 6:14-21 (“The DMA device 120 is also configured to concurrently communicate data to the packet buffer memory 122” and the protocol stack layer's internal memory spaces, such as the “the media access control (MAC) layer memory 126, the logic link control (LLC) layer memory 128, the network layer

memory 130, the transport layer memory 132, and the application layer memory 134.”); *see also* Ex. 2004, at 1 (Petitioner identifying specification, in addition to claim language, as “crystal clear”). The specification therefore confirms that the “concurrently writing” phrase requires that the “individual headers” must be written “each concurrently with each other to their respective protocol stack layer memories.”

D. The Prosecution History Confirms the Construction

During the prosecution of the U.S. Application No. 11/855,714 (“the ’714 Application”) that matured into the ’471 Patent, the examiner identified U.S. Pub. No. 2001/0037397 to Boucher et al. (“Boucher”) and rejected all pending claims of the ’714 Application as anticipated by Boucher in an office action dated December 21, 2009. *See* Ex. 1002, at 37-42. In a response dated March 3, 2010, the applicant argued that “Boucher does not teach the combination of steps recited in Applicant’s independent claim 1. For example, Boucher does not teach the step of concurrently writing *“each individual one of said plurality of headers to a respective protocol stack layer memory* where it is available for immediate processing within a protocol stack layer.” Ex. 1002, at 30 (emphasis added)(citing [0029] – [0030] of the specification, Ex. 1002, at 124, which correspond to Ex. 1001 at 5:64-6:21, cited above in Section V.C). The applicant reiterated the distinction by stating that

Boucher “is entirely different from the system recited in Applicant’s claim 1, where *each individual one of a plurality of headers in a packet are written concurrently to a respective protocol stack layer memory location.*” Ex. 1002, at 31 (emphasis added, except for underlining). As Petitioner put it, “the applicant unequivocally explained that the claimed invention requires both: (1) concurrently writing each header to a packet buffer memory and (2) *concurrently writing each individual one of said plurality of headers to a respective protocol stack layer memory.*” Ex. 2004, at 9 (emphasis in original). Based upon the arguments presented in the March 3, 2010 response, the examiner allowed the claims on April 22, 2010, noting that “Applicants have claimed uniquely distinct features in the instant invention, which are not found in the prior art, either singularly or in combination.” Ex. 1002, at 18.

“[W]hen the patentee unequivocally and unambiguously disavows a certain meaning to obtain a patent, the doctrine of prosecution history disclaimer narrows the meaning of the claim consistent with the scope of the claim surrendered.” *Biogen Idec, Inc. v. GlaxoSmithKline LLC*, 713 F.3d 1090, 1095 (Fed. Cir. 2013) (quoting *Omega Eng’g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1323, 1326 (Fed. Cir. 2003)). Applying this standard, Patent Owner concurs with Petitioner’s District Court claim construction argument that there was a “clear and unmistakable prosecution history disclaimer” for the “concurrently writing” phrase because “[t]o distinguish the

claimed invention, the applicant stated that the allegedly anticipatory prior art is 'entirely different' than the claimed invention because the prior art does not teach that 'each individual one of a plurality of headers in a packet are written concurrently to a respective protocol stack layer memory location.'" Ex. 2004, at 1 (emphasis in original).

VI. THE CLAIMS ARE NOT UNPATENTABLE UNDER THE PROPER CONSTRUCTION FOR "CONCURRENTLY WRITING"

Petitioner has failed to meet its burden of establishing that the Challenged Claims are unpatentable and the Petition should be denied for all claims. Petitioner's invalidity challenges are based on alleged obviousness based on a single primary reference in various combinations with either two or three secondary references. The primary reference is Exhibit 1005, U.S. Patent Publ. No. 2006/0072564 ("*Cornett*"). *Cornett* is entitled "Header replication in accelerated TCP (Transport Control Protocol) stack processing," was filed on May 26, 2005 and published on April 6, 2006. The secondary references are:

- (1) Exhibit 1007, U.S. Patent Publ. No. 2006/0209840 ("*Paatela*"): *Paatela* is entitled "System and method for providing transformation of multi-protocol packets in a data stream," was filed on September 12, 2005 and published on September 21, 2006.
- (2) Exhibit 1006, U.S. Patent No. 7,333,489 ("*Nelson*"): *Nelson* is entitled "System and method for storing frame header data," was filed on October 24, 2000 and issued on February 19, 2008.

- (3) Exhibit 1025, U.S. Patent No. 6,678,746 (“*Russell*”): *Russell* is entitled “Processing network packets,” was filed on August 1, 2000 and issued on January 13, 2004.

Petitioner asserts that the Challenged Claims are unpatentable as obvious based on two grounds.

Ground	Claims	Basis	References
1	1-3, 5-7, 9-10, 12-15 and 17-21	§ 103	<i>Cornett</i> in combination with <i>Paatela</i> and <i>Nelson</i>
2	8	§ 103	<i>Cornett</i> in combination with <i>Paatela</i> , <i>Nelson</i> , and <i>Russell</i>

Both of Petitioner's grounds rely upon *Cornett* as the primary reference and *Paatela* and *Nelson* as secondary references. Ground 2 also relies on *Russell* as a secondary reference.

A. The Petition Fails to Show that the Prior Art Discloses “Concurrently Writing”

Independent method claim 1 of the '471 Patent recites “[1.2] subsequent to said decoding step, *concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory* where it is available for immediate processing within a protocol stack layer.” Ex. 1001, 11:54-59. Independent apparatus claim 13 of the '471 Patent similarly recites “[13.2] a direct memory access (DMA) device coupled to said decoder and configured for *concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2)*

each individual one of said plurality of headers to a respective protocol stack layer memory where it is available for immediate processing within a protocol stack layer.” *Id.*, 12:37-43.

The Petition presents its invalidity analysis for claim 13 first, *see* Petition at 32-45, and relies on this analysis for claim 1, *see id.* at 55-56. For limitation [13.2], and consequently for limitation [1.2], tenders its invalidity challenge as follows:

- For “*direct memory access (DMA) device...writing...each of said plurality of headers to a packet buffer memory,*” the Petition relies solely on the disclosure of *Cornett*, *see* Petition at 35-38;
- For “*direct memory access (DMA) device...writing... each individual one of said plurality of headers to a respective protocol stack layer memory,*” the Petition relies solely on the disclosure of *Paatela*, *see* Petition at 38-41;
- For “*direct memory access (DMA) device...concurrently writing,*” the Petition relies solely on the disclosure of *Nelson*, *see* Petition at 41-44; and
- For “*available for immediate processing within a protocol stack layer,*” the Petition relies on the disclosures of *Paatela* and *Nelson*, *see* Petition at 44-45.

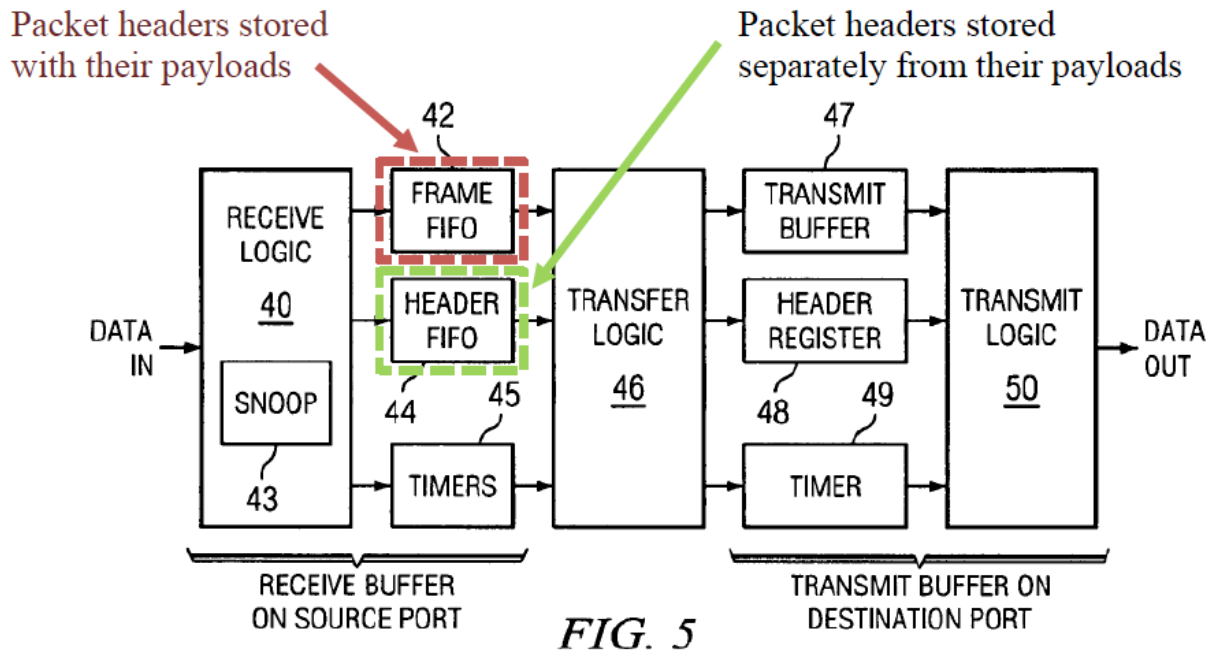
The Petition expressly acknowledges that its challenge to the “concurrently writing” phrase in the claims is limited to the disclosure of *Nelson*. *See, e.g.*, Petition at 42 (“The Cornett-Paatela combination does not explicitly explain the timing of how Cornett’s packet headers are written to Paatela’s respective, separate segments of memory. This timing is explained in Nelson.”); *see also id.* at 29 (“Cornett uses

the DMA engine to store packet headers in one buffer and the entire packet (header and payload) in another, separate buffer. The Cornett-Paatela combination would use Cornett's DMA engine to move each of a packet's individual header into a respective memory segment, per Paatela. *The timing of how packet headers are written to the respective memory segments is not explicit in the combination.*") (citations omitted, emphasis added), 31 ("A POSITA would have appreciated that Paatela stores individual packet headers in respective, separate memory segments to make each packet header available for processing as quickly as possible. Cornett seeks to further accelerate packet processing by using a DMA engine to free up the host processor and move data more efficiently. Nelson similarly seeks to process packets faster by writing headers and frames into separate buffers—in parallel—so that header information is made available for routing decisions without the need (and associated delay) to read the entire frame from the buffer.") (citations omitted).

The Petition's arguments with respect to the "concurrently writing" phrase come up short under the proper construction of the phrase because the Petition only addresses *Nelson's* purported disclosure of "concurrently writing" of packet headers to a "frame FIFO" and to a "header FIFO":

A POSITA would have understood Nelson to teach that the packet's header is *written* (1) to a frame FIFO 42 (header and payload) (**red** outline) and (2) to the header FIFO 44 (header only) (**green** outline).

This process is performed in parallel, i.e., *concurrently*. This is shown in Fig. 5:



Petition at 42-43 (citations omitted, emphasis in original); *see also id.* at 30 (“Nelson teaches writing a packet frame (header and payload) into one buffer and the packet headers into another buffer, with the two writing operations occurring in parallel.”) (citing *Nelson*, Ex.1006, 7:1-4), 31 (“Nelson similarly seeks to process packets faster by writing headers and frames into separate buffers—in parallel—so that header information is made available for routing decisions without the need (and associated delay) to read the entire frame from the buffer.”) (citing *Nelson*, Ex.1006, 2:3-10).

The Petition does not address how *Nelson*, or any of the other references for that matter, disclose “concurrently writing ... each individual one of said plurality

of headers (each concurrently with each other) to a respective protocol stack layer memory.” Ex. 2005, Brooks Decl., ¶¶ 28-29. Consequently, the Petition fails to show how *Nelson*, as part of a combination with *Cornett* and *Paatela*, satisfies the “concurrently writing” phrase of the independent claims of the ’471 Patent, as that phrase is properly construed. The Petition fails to show that the Challenged Claims are unpatentable. Moreover, as explained further below, *Nelson* does not disclose “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory,” and Petitioner cannot show how *Nelson*, as part of a combination with *Cornett* and *Paatela*, satisfies the “concurrently writing” phrase of the independent claims of the ’471 Patent, as that phrase is properly construed.

B. The Disclosure of *Nelson*

U.S. Patent No. 7,333,489 (“*Nelson*”) is the sole reference that the Petition relies on to show that the “concurrently writing” phrase of the independent claims of the ’471 Patent is satisfied. *See* Petition at 41-44. *Nelson* is generally directed to a system implementation for a Fibre Channel switch. *See Nelson*, Ex. 1006, 3:49-57; *see also* Ex. 2005, Brooks Decl., ¶ 31. “Each Fibre Channel link consists of a pair of unidirectional fibers. Each fiber is connected to an associated transmitter and receiver. The link is connected between a pair of data ports. Data is transmitted from

a first one of the ports to a second one of the ports over a first one of the fibers (and the corresponding transmitter and receiver.)” *Nelson*, Ex. 1006, 4:4-9; *see also* Ex. 2005, Brooks Decl., ¶ 31. As Mr. Brooks notes, the disclosure of *Nelson* is consistent with the Fibre Channel Framing and Signaling (FC-FS) Specification (“Fibre Channel Specification”). *See id.* (citing Ex. 2007, Fibre Channel Specification, at 46).

Nelson describes the Fibre Channel frame and general Fibre Channel switching concepts with respect to Fig. 3:



FIG. 3

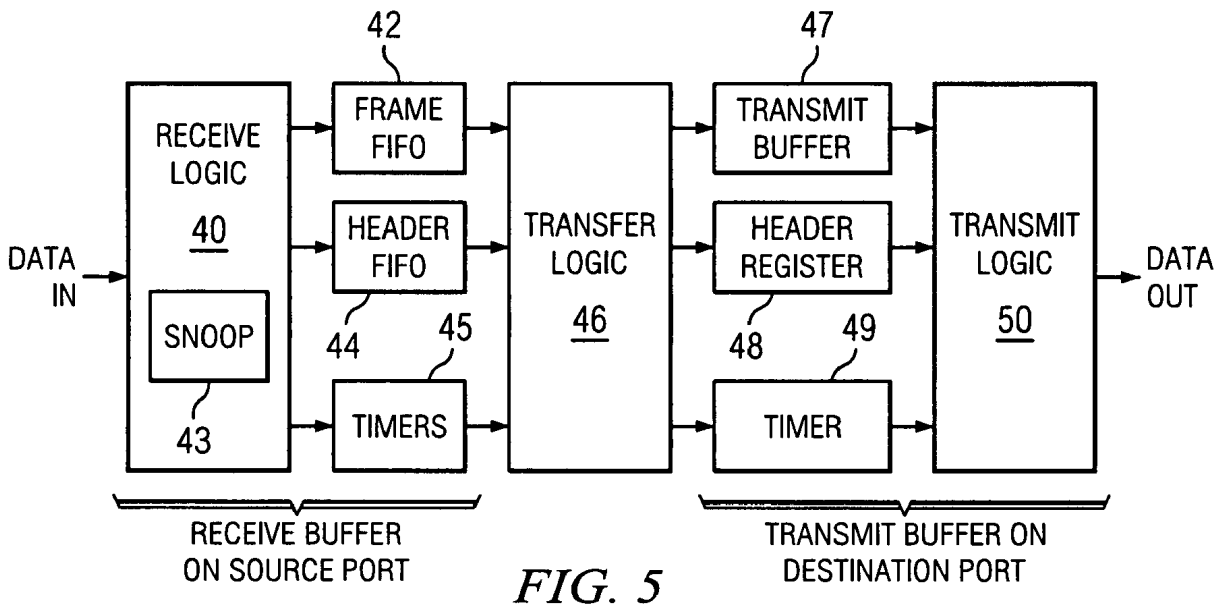
Nelson, Ex. 1006, Fig. 3; *see also* Ex. 2005, Brooks Decl., ¶ 32. Mr. Brooks again notes how closely the disclosure of *Nelson* tracks with the Fibre Channel Specification. *See id.* (citing Ex. 2007, Fibre Channel Specification, at 117 (Figure 21 - FC-2 general frame format)).

Referring to FIG. 3, a block diagram illustrating the structure of a frame in one embodiment is shown. In this embodiment, each frame includes a start-of-frame (SOF) primitive 20, a header 22, data 24, and an end-of-frame (EOF) primitive 26. SOF primitive 20 identifies the beginning of a frame. EOF primitive 26 similarly serves to identify the end of the

frame. All of the data of a frame, whether useful data or overhead data, is enclosed between the SOF and EOF primitives. Header 22 comprises overhead data related to the frame. In particular, Header 22 includes information identifying the destination of the frame. The destination information is used by the switches to make the routing decisions necessary to deliver the frame to the target site or device. Data 24 comprises useful data. In other words, data 24 is the data which the was originally intended to be delivered from the source to the destination.

Nelson, Ex. 1006, 4:34-49; *see also* Ex. 2005, Brooks Decl., ¶ 32. Mr. Brooks notes additional examples of the consistency of the disclosure of *Nelson* with the Fibre Channel Specification. *See id.* (citing Ex. 2007, Fibre Channel Specification, at 121).

Nelson describes the structure and operation of the Fibre Channel switch with respect to Fig. 5:



Nelson, Ex. 1006, Fig. 5; *see also* Ex. 2005, Brooks Decl., ¶ 33.

Referring to FIG. 5, a block diagram illustrating an embodiment of the present system which includes timers corresponding to the frame and header information is shown. In this figure, data which is transmitted to a port is received by receive logic 40. Receive logic 40 is configured to detect the SOF and EOF primitives which define the boundaries of frames in the received data and to store individual frames to locations in frame FIFO 42. Receive logic 40 includes circuitry to snoop on the received data and to copy the header of each frame to header FIFO 44. The copying of a header to header FIFO 44 occurs in parallel with the storage of the corresponding frame in frame FIFO 42.

Nelson, Ex. 1006, 6:59-7:4; *see also* Ex. 2005, Brooks Decl., ¶ 33.

“Data which is received at a port is examined for the SOF primitive which identifies the beginning of a frame. When the SOF primitive is detected, the port makes a decision to store the corresponding frame in a frame FIFO 30 of the port.

The frame (i.e., all of the data received by the port, from the SOF primitive up to and including the EOF primitive) is stored in one of the storage locations 31 in FIFO 30.” *Nelson*, Ex. 1006, 4:52-59; *see also* Ex. 2005, Brooks Decl., ¶ 34. “Frames are read out of FIFO 30 and transmitted in the order in which they were written to the FIFO.” *Nelson*, Ex. 1006, 4:59-60; *see also* Ex. 2005, Brooks Decl., ¶ 34.

Nelson's Fibre Channel switch further includes “[r]eceive logic in the port [that] stores frames of data in the storage elements of a FIFO buffer and concurrently snoops on the frame data to obtain header information.” *Nelson*, Ex. 1006, 2:13-15; *see also* Ex. 2005, Brooks Decl., ¶ 35. “The header information is stored in a buffer separate from the FIFO that stores the frames.” *Nelson*, Ex. 1006, 2:15-17; *see also id.*, 3:16-18 (“In one embodiment, the invention comprises a buffer system wherein header information is stored in a buffer separate from the FIFO that stores the frame itself.”); 5:4-5 (“In addition to frame buffer 30, the port includes a header buffer 34.”); *see also* Ex. 2005, Brooks Decl., ¶ 35. As *Nelson* further explains, the “header buffer” “eliminates the need to read part of the frame out of the FIFO and store this data in another buffer while a routing decision is made.” *Nelson*, Ex. 1006, 3:30-22; *see also* Ex. 2005, Brooks Decl., ¶ 35. The “header buffer” may be composed of “register elements” or “dual port RAM” “to store the header information.” *Nelson*, Ex. 1006, 2:26-29, 5:60-63, 6:8-12; *see also* Ex. 2005, Brooks Decl., ¶ 35.

“[T]he SOF primitive signals the beginning of a frame and is followed by the frame header.” *Nelson*, Ex. 1006, 5:5-6; *see also* Ex. 2005, Brooks Decl., ¶ 36. “[W]hen frames first arrive at a port, the frames are ‘snooped’ (i.e., examined) and the information in the header field is copied to a frame header register.” *Nelson*, Ex. 1006, 2:27-39, 3:26-28; *see also* Ex. 2005, Brooks Decl., ¶ 36. *Nelson* further describes that “[t]he port snoops on the received data and, as the header is received, the port copies the header to a FIFO which serves as header buffer 34.” *Nelson*, Ex. 1006, 5:7-9 (emphasis added); *see also* Ex. 2005, Brooks Decl., ¶ 36. As Mr. Brooks notes, *Nelson* “does not disclose any memory as part of the “receive logic” circuitry.” Ex. 2005, Brooks Decl., ¶ 36 (citing *Nelson*, Ex. 1006, 6:59-7:4).

C. *Nelson* Does Not Disclose “Concurrently Writing”

Nelson does not disclose the claimed requirement of “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory.” Consequently, the Petition, which relies solely on *Nelson* for this limitation, cannot show that the combination of *Cornett*, *Paatela*, and *Nelson* satisfies all of the limitations of the ’471 Patent. Ex. 2005, Brooks Decl., ¶ 37.

First, a POSITA would understand that *Nelson* discloses only a single Fibre Channel header. *See Nelson*, Ex. 1006, 4:43-47 (“Header 22 includes information

identifying the destination of the frame. The destination information is used by the switches to make the routing decisions necessary to deliver the frame to the target site or device.”); *see also* Ex. 2005, Brooks Decl., ¶ 38. A POSITA would further understand that the header is 24-Bytes in length and its fields are defined in the Fibre Channel Specification, including in Figure 23:

Bits	
Word	3124231615080700
0	R_CTLD_ID
1	CS_CTLS_ID
2	TYPEF_CTL
3	SEQ_IDDF_CTLSEQ_CNT
4	OX_IDRX_ID
5	Parameter

Figure 23 - Frame_Header

Ex. 2007, Fibre Channel Specification, 124; *see also id.*, 124-145; *see also* Ex. 2005, Brooks Decl., ¶ 38.

As Mr. Brooks explains, “[t]he frame header is immediately followed by the data field.” Ex. 2005, Brooks Decl., ¶ 39 (citing Ex. 2007, Fibre Channel Specification, 121). This is further illustrated in the Fibre Channel Specification, including in Figure 21:

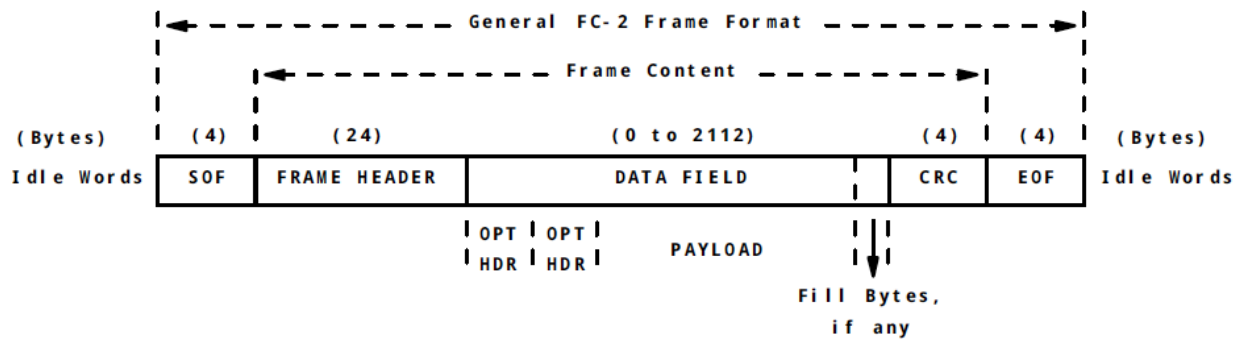


Figure 21 - FC-2 general frame format

Ex. 2007, Fibre Channel Specification, 117; *see also id.*, 121 (Figure 22 - Frame byte order); *see also* Ex. 2005, Brooks Decl., ¶ 39.

While the Fibre Channel Specification does allow for optional headers, *see* Ex. 2007, Fibre Channel Specification, 117 (Figure 21), 146 (Figure 24), these optional headers would be part of the Data Field, what *Nelson* calls “useful data” as opposed to the “overhead data” contained in the Header. *See, e.g.*, Nelson, Ex. 1006, 4:40-49 (“All of the data of a frame, whether useful data or overhead data, is enclosed between the SOF and EOF primitives. Header 22 comprises overhead data related to the frame. ... Data 24 comprises useful data. In other words, data 24 is the data which the was originally intended to be delivered from the source to the destination.”). *Nelson* discloses that its Fibre Channel switch does not store “useful data” in the header buffer (header FIFO) because the header buffer (header FIFO) only stores header information, which *Nelson* distinguishes as “overhead data.” *See*

also Ex. 2005, Brooks Decl., ¶ 40 (citing *Nelson*, Ex. 1006, 2:13-17 (“The header information is stored in a buffer separate from the FIFO that stores the frames.”), 6:66-7:1 (“Receive logic 40 includes circuitry to ... copy the header of each frame to header FIFO 44.”)). Because a “POSITA would recognize that the Nelson patent only discloses writing a single header to the header buffer, or header FIFO,” Ex. 2005, Brooks Decl., ¶ 40, the POSITA would also recognize that *Nelson* does not disclose “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory,” as the Challenged Claims require. *Id.*

Second, even if there was a disclosure in Nelson of multiple headers per frame being written to the header buffer (header FIFO), a POSITA would still recognize that *Nelson* does not disclose “concurrently writing ... (2) each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory.” *See* Ex. 2005, Brooks Decl., ¶ 41.

Fibre Channel uses a specific type of encoding scheme and requires that all valid transmissions be aligned to a 4-byte word. More specifically, “[t]he Fibre Channel Specification requires an encoding scheme, termed 8b/10b encoding, for transmission over a serial link. The Fibre Channel Specification also requires that valid transmissions be word aligned at 4-Bytes (with Bytes, after encoding, being

termed “characters”). Consequently, all valid contents of a frame, including the SOF, EOF, CRC, Frame Header, and Data, must be divisible in 4 character increments.” Ex. 2005, Brooks Decl., ¶ 42 (citations omitted). Because Nelson teaches that the “receive logic” of the Fibre Channel switch is [1] “configured to detect the SOF and EOF primitives which define the boundaries of frames,” and [2] “to store individual frames to locations in frame FIFO 42,” and [3] “to snoop on the received data and to copy the header of each frame to header FIFO 44,” *Nelson*, Ex. 1006, 6:63-7:1, a POSITA would recognize that, consistent with the Fibre Channel Specification’s requirement that valid transmissions be word aligned at 4-Bytes, *Nelson*’s “receive logic” processes an incoming transmission 4-Bytes (or 4 characters) at a time. See Ex. 2005, Brooks Decl., ¶ 43. Mr. Brooks explains the ramifications of this processing:

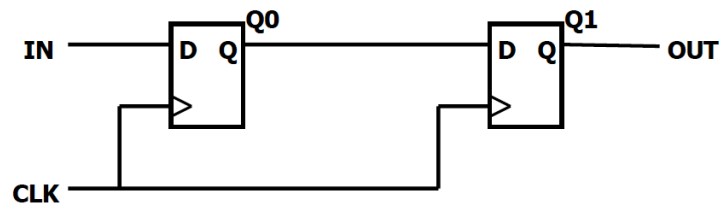
Because the Nelson patent does not disclose that the “receive logic” has any storage memory, see ¶ 36, Ex. 1006, 6:59-7:4, and based upon the Nelson patent’s disclosure that “[t]he port snoops on the received data and, as the header is received, the port copies the header to a FIFO which serves as header buffer 34,” *id.*, 5:7-9, a POSITA would recognize that the “receive logic ” is processing and storing data in the frame FIFO and the header FIFO in 4 character (4 Bytes after decoding) segments. For the 24-Byte Fibre Channel header, 6 sequential cycles would be required to store the entire header in the “frame FIFO” and the “header FIFO.”

Ex. 2005, Brooks Decl., ¶ 44. In other words, *Nelson's* “receive logic” does not “concurrently write” the contents of even a single header, let alone the contents of multiple headers.

Nelson confirms the “segmented” storage of header information to the header buffer (header FIFO) when it describes that “[t]he port snoops on the received data and, **as the header is received**, the port copies the header to a FIFO which serves as header buffer 34.” *Id.*, 5:7-9 (emphasis added); *see also* Ex. 2005, Brooks Decl., ¶ 44. *Nelson* further confirms the “segmented” storage of header information to the header buffer (header FIFO) when it describes the structure of its header buffer (header FIFO) based upon “header register elements to store the header information,” where the “header register elements each comprise a **chain of cascaded flip-flops** ... which is sufficiently large to **hold a frame header**.” *Id.*, 5:60-63 (emphasis added) ; *see also* Ex. 2005, Brooks Decl., ¶ 44. As Mr. Brooks explains: “To a POSITA, ‘a chain of cascaded flip-flops,’ as illustrated below, refers to a chain of flip-flops where the output of one flip-flop feeds the input of another flip-flop with all the flip-flops being clocked at the same time. This is often referred to as a shift register, also illustrated below.” Ex. 2005, Brooks Decl., ¶ 44.

CASCADED FLIP-FLOPS

- Shift register: new value to first stage
while second state obtains current value of first stage
- Outputs change only on clock tick

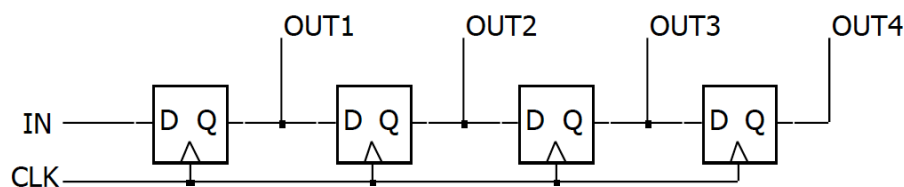


Ex. 2008, University of Washington, Paul G. Allen School of Computer Science and Engineering, CSE467: Advanced Logic Design, Sequential Logic Lecture Notes, at 11 (available at

https://courses.cs.washington.edu/courses/cse467/00wi/lectures/ppt/Sequential_Logic/index.htm, last visited June 18, 2025).

SHIFT REGISTER

- Holds samples of input
 - store last 4 input values in sequence
 - 4-bit shift register:



Id., at 14.

From the foregoing, Mr. Brooks concludes that:

The use of “a chain of cascaded flip-flops ... sufficiently large to hold a frame header” indicates to a POSITA that multiple clock cycles are required to store a single header. A POSITA would therefore recognize that a single header is stored in the header buffer or header FIFO sequentially. A POSITA would consequently recognize that the Nelson patent does not disclose “concurrently writing” the single header nor does it disclose “concurrently writing” multiple headers to the header buffer or header FIFO.

Ex. 2005, Brooks Decl., ¶ 44. A POSITA would therefore recognize that *Nelson* does not disclose “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory,” as the Challenged Claims require.

For the foregoing reasons, the grounds of the Petition fails as to all the independent claims because the *Cornett-Paatela-Nelson* combination does not disclose “concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory,” as claim limitations [1.2] and [13.2], when properly construed, require.

Because a dependent claim cannot be obvious if the independent claim from which it depends is not obvious, Petitioners have not established that any of the challenged dependent claims are unpatentable. *See, e.g., Comaper Corp. v. Antec,*

Inc., 596 F.3d 1343 (Fed. Cir. 2010). If an independent claim is nonobvious, then the dependent claim is also nonobvious. *In re Fine*, 837 F.2d 1071, 1076 (Fed. Cir. 1988) (“A claim that depends from a non-obvious independent claim is non-obvious because it contains all the limitations of the independent claim, plus a further limitation.”). The Board does not need to consider “arguments that certain dependent claim limitations would have been obvious where the base claim has not been proven invalid.” *SynQor, Inc. v. Artesyn Techs., Inc.*, 709 F.3d 1365, 1375 (Fed. Cir. 2013); *see also Zimmer Surgical, Inc. v. Stryker Corp.*, 365 F.Supp. 3d 466, 487-488 (D. Del. 2019) (“As a dependent claim contains at least one more limitation than the independent claim upon which it depends, it cannot be invalid under § 102 . . . if the independent claim upon which it depends is not anticipated.”) (*citing CA, Inc. v. Simple.com, Inc.*, 780 F. Supp. 2d 196, 260 (E.D.N.Y. 2009), *Duhn Oil Tool, Inc. v. Cooper Cameron Corp.*, 2012 U.S. Dist. LEXIS 24088, 2012 WL 604138 (E.D. Cal. Feb. 23, 2012))).

VII. RESPONSE TO STATEMENT OF MATERIAL FACTS

Patent Owner disputes the following statements of material facts set forth in the Petition. Petition at 13-15.

1. The TCP/IP model includes a link layer, a network layer, a transport layer, and an application layer. Ex.1010, [0009]-[0013].

Patent Owner admits that Ex. 1010 references a link layer, a network layer, a transport layer, and an application layer for TCP/IP, but does not reference a TCP/IP model and, on this basis, Patent Owner denies this statement.

2. The TCP/IP model includes a physical layer as its lowest layer, below the link layer. Ex.1003, ¶27.

Patent Owner admits that Dr. Mir states that “[t]he TCP/IP model also includes a physical layer below the link layer” but does not provide any evidentiary support for that statement. Ex. 1010, at [0013] states that “[t]he TCP/IP link layer corresponds to a combination of the data-link and physical layers of the OSI model.” On these bases, Patent Owner denies this statement.

4. The application layer of the TCP/IP model corresponds to the combination of the application, presentation, and session layers of the OSI model. Ex.1010, [0010], [0011].

Patent Owner admits that Ex. 1010 states that [t]he TCP/IP application layer corresponds to a combination of the application, presentation and session layers of the OSI model,” but does not reference a TCP/IP model and, on this basis, Patent Owner denies this statement.

8. Before the priority date of the '471 patent, in IEEE 802.3, use of a logical link control layer header was required. Ex.1014, 8:61-64; Ex.1015, 2:14-18; Ex.1016, Figs. 5A & 5B, 4:20-28.

Patent Owner denies that, in IEEE 802.3, use of a logical link control layer header is required or mandatory.

9. Before the priority date of the '471 patent, in IEEE 802.3, it was known that a packet's preamble sequence consisted of 8 bytes (64 bits) where the first 62 bits consisted of alternating 1's and 0's and the last 2 bits marked the end of the preamble sequence and were known as the start of frame delimiter. Ex.1020, 1:30-44.

Patent Owner denies this statement on the basis that, in IEEE 802.3, a packet's preamble consisted of 7 bytes (56 bits) of a sequence of alternating 1's and 0's and that the preamble was followed by a start of frame delimiter of 1 byte (8 bits) of a 6-bit sequence of alternating 1's and 0's followed by 2 bits of 1's. *See* Ex. 2009, 7:11-17.

VIII. CONCLUSION

Petitioner has failed to meet its burden of establishing that the Challenged Claims are unpatentable and the Petition should be denied for all claims.

Respectfully submitted,

Dated: June 18, 2025

/s/ Brett Cooper
Brett Cooper, Reg. No. 55,085
Lead Counsel for Patent Owner
BC Law Group, P.C.
200 Madison Avenue, 24th Floor
New York, NY 10016
(212) 951-0100

CERTIFICATE OF WORD COUNT (37 C.F.R. § 42.24(d))

The undersigned hereby certifies that the word count in this Patent Owner's Response is 8,069, as counted by the word-processing program Microsoft Word that was used to generate this Patent Owner's Response, where such word count excludes the table of contents, table of authorities, mandatory notices, certificate of service, appendix of exhibits, claim listing, and this certificate of word count. This Patent Owner Response is in compliance with the 14,000-word limit set forth in 37 C.F.R. § 42.24(b)(1).

Date: June 18, 2025

/Brett Cooper/

BC Law Group, P.C.
200 Madison Avenue, 24th Floor
New York, NY 10016
(212) 951-0100

Brett Cooper
Reg. No. 55,085
Attorney for Patent Owner

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the above document and its accompanying exhibits were served on June 18, 2025, by filing this document through the Patent Trial and Appeal Case Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

Theodore M. Foster
David L. McCombs
Calmann J. Clements
HAYNES AND BOONE, LLP
2801 N. Harwood St., Suite 2300
Dallas, TX 75219
ipr.theo.foster@haynesboone.com
david.mccombs.ipr@haynesboone.com
calmann.clements.ipr@haynesboone.com

Date: June 18, 2025

/Brett Cooper/

BC Law Group, P.C.
200 Madison Avenue, 24th Floor
New York, NY 10016
(212) 951-0100

Brett Cooper
Reg. No. 55,089
Attorney for Patent Owner