

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,
Petitioner,

v.

LIONRA TECHNOLOGIES, LTD.,
Patent Owner.

IPR2024-01281
Patent No. 7,738,471 B2

PETITIONER REPLY

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PETITIONER’S EXHIBIT LIST

Ex.1001	U.S. Patent No. 7,738,471 to Kuliner
Ex.1002	File History of U.S. Patent No. 7,738,471
Ex.1003	Declaration of Nader F. Mir, Ph.D.
Ex.1004	<i>Curriculum Vitae</i> of Nader F. Mir, Ph.D.
Ex.1005	U.S. Patent Appl. No. 2006/0072564 to Cornett et al. (“Cornett”)
Ex.1006	U.S. Patent No. 7,333,489 to Nelson et al. (“Nelson”)
Ex.1007	U.S. Patent Appl. No. 2006/0209840 to Paatela et al. (“Paatela”)
Ex.1008	Transmission Control Protocol, RFC 793 (Sept. 1981)
Ex.1009	Andrew S. Tanenbaum, “Computer Networks,” 3rd ed. (1996) (“Tanenbaum”)
Ex.1010	U.S. Patent Appl. No. 2006/0215695 to Olderdissen (“Olderdissen”)
Ex.1011	U.S. Patent No. 7,821,931 to Swenson et al. (“Swenson”)
Ex.1012	U.S. Patent No. 8,396,064 to Giesberts et al. (“Giesberts”)
Ex.1013	U.S. Patent No. 9,307,054 to Boucher et al. (“Boucher”)
Ex.1014	U.S. Patent No. 6,175,571 to Haddock et al. (“Haddock”)
Ex.1015	U.S. Patent No. 6,438,128 to Kashyap (“Kashyap”)
Ex.1016	U.S. Patent No. 6,501,764 to Fudatate et al. (“Fudatate”)
Ex.1017	U.S. Patent No. 7,110,404 to Temoshenko (“Temoshenko”),
Ex.1018	U.S. Patent Appl. No. 2003/0223376 to Elliott et al. (“Elliott”)
Ex.1019	U.S. Patent Appl. No. 2005/0256975 to Kaniz et al. (“Kaniz”)
Ex.1020	U.S. Patent. No. 6,650,654 to Batty et al. (“Batty”)
Ex.1021	Interim procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation (June 21, 2022)

Ex.1022	Complaint filed in <i>Lionra Technologies Ltd. v. Cisco Sys., Inc.</i>
Ex.1023	Radia Perlman, “Interconnections: Bridges, Routers, Switches, and Internetworking Protocols,” 2d ed. (1999) (“Perlman”)
Ex.1024	U.S. Patent Appl. No. 2002/0003795 to Oskouy et al. (“Oskouy”)
Ex.1025	U.S. Patent No. 6,678,746 to Russell et al. (“Russell”)
Ex.1026	WO 00/10302 to Lawton et al. (“Lawton”)
Ex.1027 (NEW)	Deposition transcript of Thomas Brooks
Ex.1028 (NEW)	U.S. Patent No. 6160808 (Maurya)
Ex.1029 (NEW)	U.S. Patent Appl. No. 2002/0110124A1 (Fujita)
Ex.1030 (NEW)	U.S. Patent Appl. No. 2002/0176427A1 (Noda)
Ex.1031 (NEW)	U.S. Patent Appl. No. 2004/0008728A1 (Lee)
Ex.1032 (NEW)	U.S. Patent Appl. No. 2004/0107294 (Chen)
Ex.1033 (NEW)	MPLS Label Stack Encoding, RFC3032 (January 2001).
Ex.1034 (NEW)	U.S. Patent No. 6791985 (Ashwood-Smith)
Ex.1035 (NEW)	U.S. Patent Appl. No. 2003/0053481 (Abiru)
Ex.1036 (NEW)	U.S. Patent Appl. No. 2002/0109878 (Qiao)
Ex.1037 (NEW)	U.S. Patent Appl. No. 2007/0198807 (Rezeanu)

Ex.1038 (NEW)	U.S. Patent Appl. No. 2005/0286527 (Tieu)
Ex.1039 (NEW)	U.S. Patent No. 5940598 (Strauss)
Ex.1040 (NEW)	U.S. Patent No. 6850495 (Baum)
Ex.1041 (NEW)	U.S. Patent No. 6952756B1 (Le)
Ex.1042 (NEW)	IEEE Std. 802.3
Ex.1043 (NEW)	U.S. Patent No. 6330616 (Gioquindo)
Ex.1044 (NEW)	U.S. Patent No. 6438128 (Kashyap)
Ex.1045 (NEW)	U.S. Patent Appl. No. 2003/0053493 (Graham Mobley)
Ex.1046 (NEW)	U.S. Patent No. 7,072,823 (Athanas)
Ex.1047 (NEW)	U.S. Patent No. 6021132 (Muller)
Ex.1048 (NEW)	U.S. Patent No. 5720032 (Picazo, Jr.)
Ex.1049 (NEW)	U.S. Patent No. 5237693 (Kiyohara)

I. Introduction

Patent Owner Lionra Technologies, Ltd. (“Lionra”) fails to distinguish the Challenged Claims from the prior art. Petitioner Cisco Systems, Inc. (“Cisco”) respectfully requests the Board find the Challenged Claims unpatentable for the reasons discussed in the Petition and below.

II. Claim Construction

As Patent Owner notes, the district court issued a claim construction order on May 13, 2025. The court adopted constructions for the following terms:

Claim Term/Phrase	Adopted Construction
“concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory”	Plain meaning, i.e., “concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory.”
“packet buffer memory”	Plain and ordinary meaning.

See Ex.2002 at 8, 13.

Patent Owner advocates for the Board to adopt the court’s construction of “*concurrently writing....*” Patent Owner Response, Paper 12 [POR], 12. Patent Owner also provides the following restatement of the writing steps that must occur “concurrently”:

More specifically: (1) “each of said plurality of headers”

must be written “to a packet buffer memory” and “to a respective protocol stack layer memory” concurrently; **and** (2) “each individual one of said plurality of headers” must be written to each “respective protocol stack layer memory” concurrently.

POR, 10-11 (emphasis by Lionra).

Patent Owner’s restatement appears to be substantively the same as the court’s construction. To the extent that Patent Owner meant for its restatement to have a different meaning or scope than the court’s construction, Patent Owner failed to explain that difference.

If the Board construes the “*concurrently writing*” limitation, Petitioner agrees that the Board should adopt the court’s construction of the “*concurrently writing...*” limitation.

III. Cornett, Paatela, and Nelson render obvious “*concurrently writing...*”

The plain language of the “*concurrently writing*” limitations in claims 1 and 13 unquestionably requires that the writing actions enumerated as “(1)” and “(2)” in the claim occurred *concurrently*. Regarding this concept, the petition’s claim analysis relied on the description in Nelson of simultaneously writing a packet header to a whole-packet memory (i.e., to frame FIFO 42) and to a separate header-only memory (i.e., to header FIFO 44). Pet., 42-43; Ex.1006, 7:1-4 & 2:3-10. This analysis generally corresponds to item (1) in Lionra’s restatement of the

claim construction: that “each of said plurality of headers’ must be written ‘to a packet buffer memory’ and ‘to a respective protocol stack layer memory’ concurrently.” *See* POR, 10-11. Lionra does not identify any shortcoming in the prior art regarding this aspect of the “*concurrently writing*” limitation.

Lionra only disputes whether the prior art renders obvious the portion of claim language that was changed in the district court’s adopted claim construction by the insertion of a clarifying parenthetical: “concurrently writing ... (2) each individual one of said plurality of headers (**each concurrently with each other**) to a respective protocol stack layer memory.” POR, 22-23 (emphasis added).

Lionra and its declarant mistakenly believe that the Petition did not address this concept, and they erroneously allege that the Petition relied solely on Nelson as teaching the entirety of the “*concurrently writing*” limitation. *See, e.g.*, POR, 20 (“For ‘*direct memory access (DMA) device...concurrently writing*,’ the Petition relies solely on the disclosure of *Nelson*”) (emphasis by Lionra); Ex.2005, ¶28 (“The Petition and Dr. Mir rely solely on the Nelson patent to satisfy the “concurrently writing” requirement of claims 1 and 13.”).

The phrase “*concurrently writing*” is part of lengthy limitations in claims 1 and 13, however, for which the Petition (and Dr. Mir’s supporting analysis) also relied upon the other references in the ground, namely Cornett and Paatela. *See* Pet., 36-38 (discussing how Cornett renders obvious writing headers to a *packet*

buffer memory), 38-41 (discussing how Paatela renders obvious writing each header to a respective protocol stack layer memory).

For the reasons discussed in the Petition and further elaborated on below, the prior art identified in the Petition renders the claim obvious.

A. The prior art describes writing multiple headers “currently with each other”

As the Petition noted, Nelson describes implementing its memory using a “dual port” memory. Ex.1006, 6:8-9; Pet., 20, 45. Paatela similarly describes using a “dual-port memory” for separately storing individual protocol layer headers. Ex.1007, [0078]. “A dual-port memory can be **simultaneously** read and/or **written by two different data sources**, or more generally, a shared memory accessible by two processes.” Ex.1007, [0078] (emphasis added); Ex.1027, 90:4-10. Paatela goes on to describe how multiple “words may be simultaneously written”:

In one embodiment, the data stream is a 64-bit data stream, and the memory 716 is a 32-bit wide, 128-word deep, dual-port memory. In this manner, **two 32-bit words may be simultaneously written** to the memory 716 to write the 64-bit data. Alternatively, data can be concurrently written to and read from the memory 716.

Ex.1007, [0078] (emphasis added).

And Paatela explains that the memory may be equipped with more than just two ports. For example, Paatela also contemplates using a “quad-port memory” or

“other multi-port memory.” Ex.1007, [0078]. Given that a dual-port memory supports writing “two 32-bit words... simultaneously,” it would have been obvious to a POSITA that a “quad-port memory” would support writing four 32-bit words simultaneously. Ex.1027, 91:16-17 (“the word ‘quad’ means that there are four”). More generally, it would have been obvious for Paatela’s “multi-port memory” to have any number of ports, and thus, support simultaneously writing any desired number of 32-bit words. Ex.1007, [0078].

It would have been obvious to a POSITA for the simultaneously written 32-bit words to represent multiple different protocol layer headers for multiple reasons. First, many protocol layer headers are 32 bits long or less. Paatela identifies specific exemplary protocol headers, including “a PPP header” and “an MPLS label stack.” Ex.1007, [0077]. A PPP header is typically in the range of 2 to 5 bytes, which corresponds to a length of 16 to 40 bits. Ex.1028, Fig. 5 (showing a two-byte PPP header 503), 10:34-37; Ex.1029, Fig. 17 (showing a 32-bit PPP header for encapsulating a PPP packet in a PPP packet); Ex.1030, Fig. 5A, [0067] (“PPP header constructed by a flag field 201 [1 byte], an address field 202 [1 byte], a control field 203 [1 byte], and a protocol identification field 204 [1 or 2 bytes]”); Ex.1031, Fig. 4, [0058] (“PPP header includes a flag field [1 byte], an address field [1 byte], and a control field [1 byte].”). The variable length of a PPP header is due to the ability of communicating peers to negotiate to compress (e.g., shorten or

omit) some fields. Ex.1032, [0043] (“PPP peers may negotiate to compress address field 904 and control field 906. If compression is enabled, two octets are eliminated. In addition, PPP peers may negotiate to compress protocol field 908 to one byte, e.g., 0x21.”).

An MPLS label stack (protocol header) is 32 bits or less. Ex.1033, §2.1 (“Each label stack entry is represented by 4 octets”), Fig. 1 (showing a 32-bit label stack entry); Ex.1034, 6:21-22 (“the MPLS header has a prefixed length between 0 and 4 bytes”); Ex.1035, Fig.17A (showing a 32-bit MPLS header), [0062]; Ex.1036, [0021] (“a MPLS header (i.e., 32 bits including a 20 bit label)”).

Thus, the dual-port memory for headers described by both Nelson and Paatela would support writing two 32-bit protocol headers associated with two different protocols, such as PPP and MPLS. That alone is sufficient to satisfy the construed claim’s recitation of “*concurrently writing...*” a “plurality of headers (each concurrently with each other) to a respective protocol stack layer memory.” *See* Ex.1027, 56:15-57:4 (Mr. Brooks disputing that writing two headers together would constitute *concurrently writing* only because “Nelson teaches only a single header”).

Paatela’s alternative suggestion of a quad-port protocol layer header memory would support writing four 32-bit protocol headers associated with as many as four different protocols. *See, e.g.,* Ex.1037, [0032] (“Shown are four ports which form a

quad-port RAM.... Ports 0-3 may permit independent, simultaneous access for read/write from/to any location within storage array 22.”). And Paatela’s suggestion of a “multi-port memory,” with an arbitrary number of ports, would allow an arbitrary number of protocol headers to be simultaneously written.

B. The combined prior art renders obvious writing multiple layers’ headers to their respective layer memories “currently with each other”

It would have been obvious to a POSITA for the combined Cornett-Paatela-Nelson device to *concurrently write* multiple packet headers to their respective protocol layer header memories (i.e., each concurrently with each other), because Paatela describes performing simultaneous write operations to the protocol layer-specific header memory 716. Ex.1007, [0078] (“...two 32-bit words may be simultaneously written to the memory 716...”); *see* Pet., 39-40 (explaining how Paatela’s memory 716 renders obvious *respective protocol stack layer memor[ies]*). A POSITA would have been motivated to “move the headers to their respective memory segments in parallel” for reasons discussed in the Petition: namely, Cornett is “dedicated to reducing processing overhead and processing time, Ex.1005, [0097]” while Paatela is “focused on optimizing packet processing in an environment where time is of the essence. Ex.1007, [0076].” Pet., 30. Performing write operations in parallel, as described in Nelson, would facilitate those faster-packet-processing objectives. As Dr. Mir explained in his declaration,

the combination of Cornett, Paatela, and Nelson renders obvious writing the headers to their respective layer memories in parallel with one another:

The combination is premised on the teachings of the references. It permits but does not require physical incorporation of elements from Paatela and Nelson into Cornett. Nevertheless, the physical incorporation of Paatela's and Nelson's teachings for how to process individual encapsulated headers of Cornett's packets, and the timing of writing headers and frames into a buffer, would teach the claim limitations. It would amount to using Paatela's input controller and packet classification engine to "determine[] where one networking layer header ends and the next networking layer header begins." Paatela, [0077]. Then, based on this information, using Cornett's data movement module (e.g., DMA engine) to **move each individual encapsulated header into a respective memory segment**, per Paatela. Cornett, [0074], [0097]. Per Nelson, **the write operations would be performed in parallel to accelerate packet processing**. Nelson, 7:1-4. It would have been obvious to incorporate Paatela's and Nelson's teachings into Cornett's technique.

Ex.1003, ¶67 (some emphasis added).

[T]he combination of Cornett, Paatela, and Nelson processes packets and uses a DMA engine to **save each**

individual encapsulated header of a packet into a respective memory segment, per Paatela, **in parallel**, i.e., concurrently, per Nelson.

Ex.1003, ¶135 (emphasis added).

Writing each of the protocol headers to its respective protocol header memory in parallel would have been obvious because doing so would “accelerate packet processing.” Pet., 32 (citing Ex.1006, 7:1-4); *see also* Ex.1003, ¶¶58, 65-66 (“Nelson writes this data in parallel to accelerate packet processing...”).

In summary, the description in Nelson and Paatela of using a dual-port, quad-port, or multi-port memory to store protocol layer headers renders obvious writing multiple layers’ headers “currently with each other” as required by the claim construction.

C. Patent Owner does not dispute the remaining limitations.

The “concurrently writing” issue discussed above is the only alleged deficiency in the Petitions’ claim analysis identified in the Patent Owner Response. If Patent Owner presents a new argument in its Sur-Reply, the Board should refuse to consider the argument and deem it forfeited. *See* Paper 7 at 9 (“Patent Owner is cautioned that any arguments not raised in the response may be deemed waived.”). Cisco also respectfully requests the Board find in Cisco’s favor on all the uncontested claim limitations and issues for the reasons presented in the Petition.

IV. Material Facts

Lionra denies only a handful of Material Facts. POR, 36-38. Notably, Lionra does not allege that any of its limited denials have any impact whatsoever on the substantive invalidity issues in dispute. Cisco replies to the issues raised by Lionra below. The Board may, and should, consider the undisputed Material Facts (numbers 3, 5-7, 10-11) as admitted. 37 C.F.R. § 42.23(a).

A. Material Fact #1: The TCP/IP model includes a link layer, a network layer, a transport layer, and an application layer.

Lionra denies the statement on the basis that Ex.1010 refers to “TCP/IP” but not to a “TCP/IP model.” POR, 37. Lionra presents no contrary evidence.

Further evidence confirms that Material Fact #1 is true. For example, a prior art patent publication illustrates in its Figure 2 “the TCP/IP model” that “includes four layers.” Ex.1038, Fig. 2, [0006]. Another prior art patent shows in its Figure 2 a “commonly used TCP/IP model” with five layers. Ex.1039, 4:5-24, Fig. 2, 9:47-51 (“FIG. 2 is a comparative diagram of the International Standards Organization (ISO) Open System Interconnection (OSI) model for network architectures and a commonly used TCP/IP model.”).

B. Material Fact #2: The TCP/IP model includes a physical layer as its lowest layer, below the link layer.

Lionra denies this statement, stating that “[t]he TCP/IP link layer corresponds to a combination of the data-link and physical layers of the OSI

model.” POR, 37 (quoting Ex.1010, [0013]). Lionra’s declaration takes yet another position, testifying that (1) there is no such thing as a TCP/IP model and (2) there is neither a “link layer” nor a “physical layer” in TCP/IP. Ex.1027, 15:15-24.

Additional evidence confirms, however, that the physical layer is the lowest layer in the TCP/IP model, irrespective of whether the physical layer is considered part of the link layer (giving a four-layer model) or is considered distinct from the link layer (giving a five-layer model). Ex.1040, Fig. 2, 3:21-30; Ex.1041, Fig. 3, 5:56-60; Ex.1039, Fig. 2, 4:5-24; *cf.* Pet., 54 (citing Material Fact #2 to support that “a frame’s physical layer is the lowest layer in both TCP/IP and OSI models”). Furthermore, Lionra’s declarant agrees that in the only networking model that he was aware of, “the lowest layer... is the physical layer.” Ex.1027, 15:2-12.

C. Material Fact #4: The application layer of the TCP/IP model corresponds to the combination of the application, presentation, and session layers of the OSI model.

Lionra denies this statement on the basis that Ex.1010 refers to “TCP/IP” but not to a “TCP/IP model.” POR, 37. Lionra presents no evidence to contradict or refute the Petition’s three cited references.

Further evidence confirms that Material Fact #4 is true. For example, the prior art figure below shows “a comparison of the standard open system interconnect networking model and the TCP/IP networking model.” Ex.1041, 5:49-51. The figure shows that the TCP/IP model application layer corresponds to the

OSI model application, presentation, and session layers:

OSI	TCP/IP
Application (Layer 7)	Application (HTTP,FTP,SMTP,etc.)
Presentation (Layer 6)	
Session (Layer 5)	
Transport (Layer 4)	Transport (TCP/UDP)
Network (Layer 3)	Internet (IP)
Data link (Layer 2)	MAC
Physical (Layer 1)	PHY

Ex.1041, Fig. 3 (annotated).

A second prior art figure below similarly shows the TCP/IP application layer overlapping with the OSI model application, presentation, and session layers:

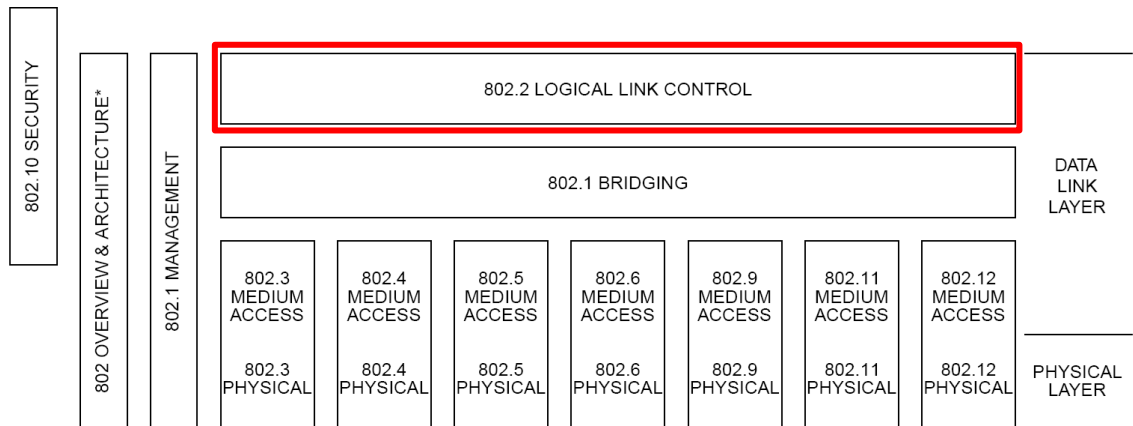
OSI	TCP/IP
Application	Application
Presentation	
Session	
Transport	Transport
Network	Internet
Data Link	Network Interface
Physical	Physical

Ex.1039, Fig. 2 (annotated).

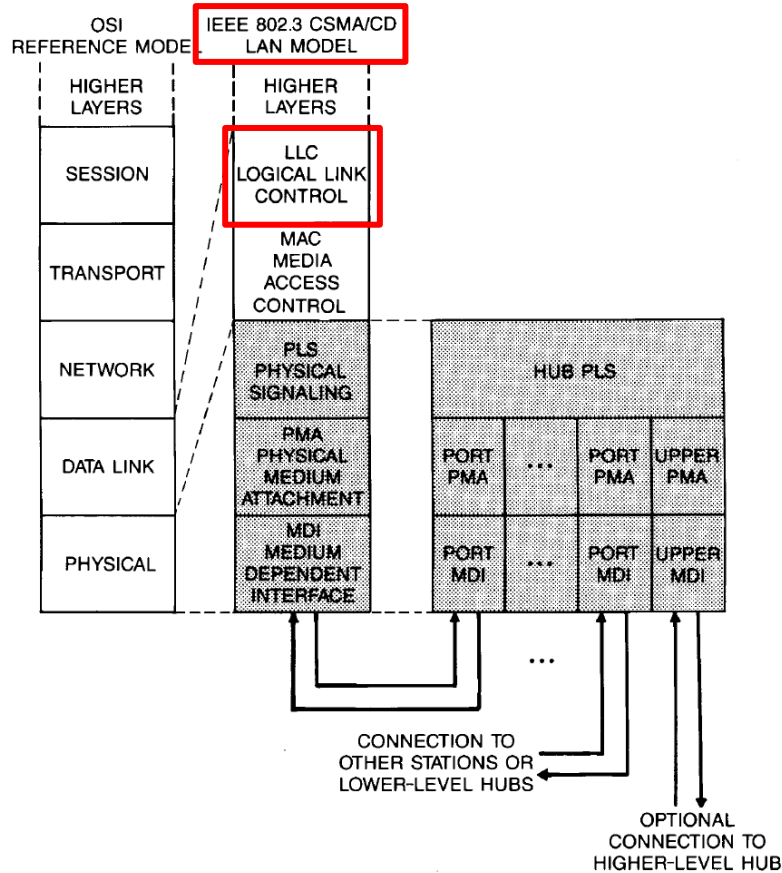
D. Material Fact #8: Before the priority date of the '471 patent, in IEEE 802.3, use of a logical link control layer header was required.

Lionra denies this statement but provides no basis for its denial, nor evidence to support its position.

Cisco's prior art evidence shows that "the 802.3 MAC frame has an IEEE 802.2 logical link control (LLC) header following the MAC header." Ex.1014, 8:61-64; *see also* Ex.1015, 2:14-18. Protocol layer diagrams in the IEEE 802.3 standard itself uniformly show the use of IEEE 802.2 Logical Link Control (LLC):



Ex.1042, iii (annotated).



Ex.1042, 249 (Fig. 12-1, annotated).

See also, e.g., Ex.1042, 3 (Fig. 1-1), 31 (Fig. 2-1a), 42 (Fig. 4-1), 97 (Fig. 6-1).

IEEE 802.3 also defines a “data frame” as including “logical link control (LLC) Data.” Ex.1042, 16 (§1.4.87); *see also id.*, 2 (§1.1.2, “The Logical Link Control (LLC) sublayer and MAC sublayer together encompass the functions intended for the Data Link Layer....”). Since logical link control data is a required part of an IEEE 802.3 data frame, it follows that the use of a logical link control layer header was required in IEEE 802.3.

Those of skill in the art recognized that the logical link control layer header was required in IEEE 802.3 Ethernet. For example, U.S. Patent No. 6,330,616

contrasts the two different Ethernet frame formats that were commonly used in the prior art. Figure 4A shows the IEEE 802.3 Ethernet frame format, including the “LLC” header field:

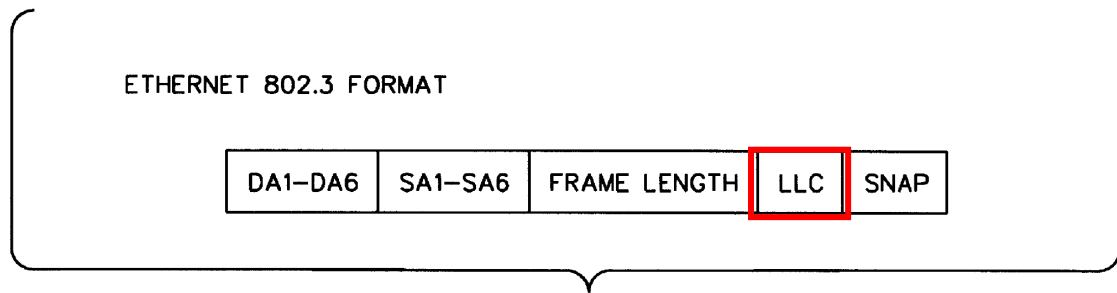


fig. 4A

Ex.1043, Fig. 4A (annotated).

See also Ex.1043, 6:64-7:23.

Although unstated, Lionra may have disputed Material Fact #8 because of its declarant’s unfamiliarity with the fact that there are two frame formats commonly referred to as “Ethernet.” *See infra*, § V.A. The second format—known as “DIX” Ethernet because of its early association with the companies Digital Equipment Corporation (DEC), Intel, and Xerox—does not use an LLC header field:

Layer 2 communication protocols, or media, that are commonly used include **Ethernet, both according to the Dec-Intel-Xerox (DIX) and IEEE 802.3 standards,**...

Some layer 2 protocols further fall under the IEEE 802.2 standard, such as **802.3 Ethernet**, 802.5 Token Ring, and 802.4 Token Bus, which **require use of a logical link control (LLC) header** and a System Network

Architecture Protocol (SNAP) header. The SNAP header includes a field for an Ethertype value. **DIX Ethernet does not use LLC** or SNAP headers, but its header nevertheless includes a field for an Ethertype value.

Ex.1044, 2:14-22 (emphasis added); *see also* Ex.1043, Fig. 4B.

- E. Material Fact #9: Before the priority date of the '471 patent, in IEEE 802.3, it was known that a packet's preamble sequence consisted of 8 bytes (64 bits) where the first 62 bits consisted of alternating 1's and 0's and the last 2 bits marked the end of the preamble sequence and were known as the start of frame delimiter.**

Lionra denies this statement, but its objection is essentially a minor quibble over irrelevant semantics. Lionra argues that the “preamble consisted of 7 bytes (56 bits)... followed by a start of frame delimiter of 1 byte (8 bits).” POR, 38. At the level of individual bits, Lionra agrees that the sequence began with 56 bits of alternating 1's and 0's, following by an additional 6 bits of alternating 1's and 0's – which is indistinguishable from the Material Fact's statement that “the first 62 bits consisted of alternating 1's and 0's.” Lionra also agrees that these 62 bits were then “followed by 2 bits,” which is consistent with the Material Fact's statement that “the last 2 bits marked the end.” In short, Lionra appears only to dispute whether the overall 64-bit sequence is divided into (1) a 62-bit preamble and a 2-bit start of frame delimiter, or (2) a 56-bit preamble and an 8-bit start of frame delimiter. Stated differently, the dispute is whether bit numbers 57 through 62 (out of the entire 64-bit sequence) are classified as part of the preamble or part of the start of

frame delimiter.

The precise dividing line between the preamble and the start of frame delimiter are ultimately of no consequence for this proceeding. Material Fact #9 was relied upon only for claim 21, which recites that the portion of a packet communicated to the DMA device “*is absent of a preamble and a physical layer header.*” Pet., 54. Lionra has not disputed that it would have been obvious for Cornett’s PHY to pass received information without including the preamble and start of frame delimiter. Pet., 55. Lionra also has not disputed that an Ethernet preamble sequence (whether 56 bits or 62 bits) corresponds to the claimed “*preamble*” or that an Ethernet start of frame delimiter (whether 8 bits or 2 bits) corresponds to the claimed “*physical layer header.*” Since the entire 64-bit sequence would be removed (not transmitted for storage), it makes no difference how the 64 bits are divided between a “preamble” portion (*preamble*) and a “start of frame delimiter” portion (*physical layer header*).

V. The testimony of Thomas Brooks is entitled to little or no weight.

The Board should give little or no weight to the direct testimony of Patent Owner’s declarant, Thomas Brooks, for many reasons.

A. Mr. Brooks’ familiarity with the technology of the ’471 patent and prior art is deficient.

While purporting to “know Ethernet well” (Ex.1027, 29:19-20) and to have implemented Ethernet “from scratch” many times (Ex.2005, ¶7; Ex.1027, 29:5-14),

Mr. Brooks is unaware of basic details about Ethernet, such as the fact that there are two commonly used but different standards for formatting Ethernet frames:

Q. Is there more than one standard for the format of an Ethernet frame recognized in the industry?

ATTORNEY AUCHTER: Objection. Form.

A. I don't know.

* * *

Q. Have you ever heard of the DIX standard for Ethernet?

A. No.

Ex.1027, 25:18-26:11.

The existence of two different Ethernet frame formats—and the details of the differences between them—were known to persons of ordinary skill in the art in the prior art timeframe:

In an Ethernet environment, there are two different frame formats in common use, i.e., Ethernet 802.3 and Ethernet DIX, for client platforms which can co-exist on the Ethernet network.

Ex.1043, 6:64-67.

[T]hose skilled in the art will be aware of the relatively minor differences between IEEE 802.3 and the Digital-Intel-Xerox (DIX) 2.0 (or II) specification of ethernet...

Ex.1045, [0113].

Layer 2 communication protocols, or media, that are

commonly used include Ethernet, both according to the
Dec-Intel-Xerox (DIX) and IEEE 802.3 standard,...

Ex.1044, 2:4-6.

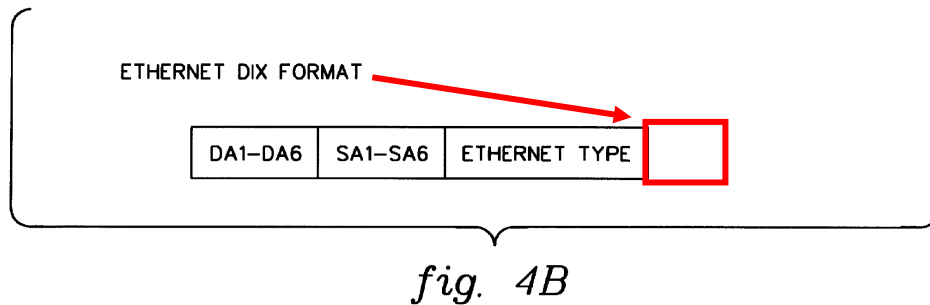
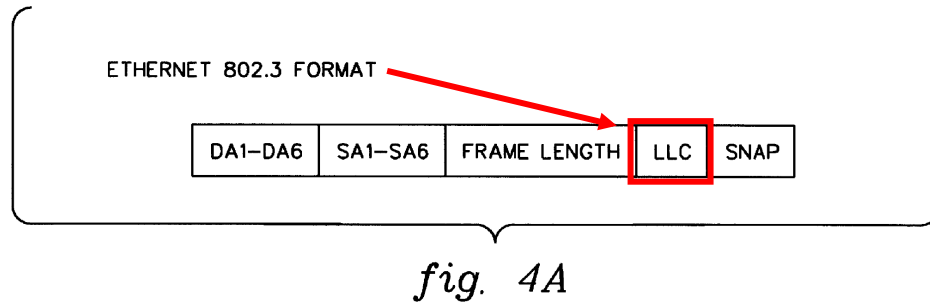
Knowledge of such fundamental Ethernet concepts is not per se required by the ordinary skill level proposed by either party or provisionally adopted by the Board (Pet., 13; POR, 8-9; DI, 6). But Mr. Brooks unfamiliarity with Ethernet is concerning and casts doubt on his credibility, since the '471 Patent, Cornett, and Paatela make their disclosures in the context of Ethernet protocols. *See, e.g.*, Ex.1001, 7:14-15; Ex.1005, [0079]; Ex.1007, [0079], [0113].

Concerns about Mr. Brooks credibility are only exacerbated by the fact that whatever work Mr. Brooks has done implementing Ethernet has apparently related to the DIX variant of Ethernet—the one he's never heard of—since that is the standard which does not use a logical link control (LLC) layer header:

Q. When we were talking about your engineering working where you implemented Ethernet a number of times, have you implemented a logic link control layer?

A. Not to my memory.

Ex.1027, 51:5-9.



Ex.1043, Figs. 4A & 4B (annotated).

Some layer 2 protocols further fall under the IEEE 802.2 standard, such as **802.3 Ethernet**, 802.5 Token Ring, and 802.4 Token Bus, which **require use of a logical link control (LLC) header** and a System Network Architecture Protocol (SNAP) header. The SNAP header includes a field for an Ethertype value. **DIX Ethernet does not use LLC or SNAP headers**, but its header nevertheless includes a field for an Ethertype value.

Ex.1044, 2:14-21 (emphasis added); *see also* Material Fact #8.

B. Mr. Brooks' memory of technology in the relevant timeframe is poor.

Mr. Brooks addressed the purported deficiencies and drawbacks of “prior art” approaches to managing packet headers in memory in his declaration, such as

a supposed need to copy each header into a respective layer's own memory:

In the Detailed Description section, the '471 Patent presents the some of the drawbacks of the prior art approaches, including that “[e]ach of the protocol stack layers use the packet buffer memory 122 to copy its respective header into its own processing memory for receive processing,” *id.* [Ex.1001], 5:51-54, and that after “decoder 516 ... performs actions to forward a portion of a decoded packet 300 that is absent of a preamble and physical layer information to a packet buffer memory 520 ... each protocol stack layer processes its respective layer information in a sequential manner,” *id.*, 10:43-48.

Ex.2005, ¶18 (emphasis added).

Mr. Brooks testified that all the packet processing implementations he developed in the prior art timeframe used this approach:

Q. You were personally involved in developing packet processing implementations using FPGAs and ASICs before the 2007 priority date of the '471 patent. Is that correct?

A. Yes.

Q. Did the packet processing implementations you developed before the 2007 priority date use the approach that you describe in paragraph 18?

ATTORNEY AUCHTER: Objection to form.

A. Yes.

Ex.1027, 31:14-23; *see also id.* 31:5-13 (drawing Mr. Brooks' attention to the header-copying drawback).

A patent assigned to Mr. Brooks' former employer Intransa, Inc. and naming him as a named inventor shows that his memory is incorrect. *See* Ex.2006, 2; Ex.1027, 27:9-20, 59:4-10; Ex.1046, codes 75, 73. Intransa's U.S. Patent No. 7,072,823 describes using a shared memory architecture, where different packet processing layers access packets stored in a commonly accessible "second memory." Rather than copying packets to individualized memory structures for each layer, components on different networking layers transfer packets by sending to one another the packets' storage locations in the memory:

The data storage system may include a second memory 160, according to one embodiment. The second memory 160 may support communication between components within the data storage system, and can support communication between the controller system 80 and memory 90.... Further, the second memory **may support communication between any selected components including: Ethernet interface 60, controller system 80, memory 90, first controller 110, second controller 120, PHY controller 130, MAC controller 140, translation controller 150, and interface 70**, according to the various embodiments. The second memory 160 may advantageously reduce required communication between

any selected components by providing a buffer area.

For example, communication between the first controller 110 and the second controller 120 can use the second memory 160 to buffer Ethernet packets received before the second controller 120 communicates the client system request to the memory 90.... **Instead of communicating each packet individually they may be stored in the shared second memory 160. The corresponding storage location, or buffer location, may be communicated to the second controller 120 instead of transferring the information directly.**

Ex.1046, 6:14-42 (emphasis added).

Thus, contrary to Mr. Brooks' memory that all prior art packet processing systems (including his own) copied packets for processing at each network layer, his own patent describes an alternative (and more advantageous) approach of sharing memory among multiple packet processing layers. Nor was this approach even new with Intransa's 2002 patent application—it had been repeatedly described in earlier patents for at least a decade. *See, e.g.*, Ex.1047 (entitled "Shared memory management in a switched network element"); Ex.1048, Abstract (accelerating packet processing "by only moving pointers to packets around in memory as opposed to the data of the packets itself"), 10:23-30 ("the teachings of the invention are applicable to any network data link layer or physical layer protocol... and any transport layer protocol..."); Ex.1049, Fig.18 (showing

pointers used to exchange information between OSI layers), 17:21-22 (on receiving a packet, “the header portion is cut out from the packet data and is stored in the header storage area for each layer”), 17:41-45 (explaining that passing pointers between layers makes “it possible to reduce the frequency of unnecessary data copying between the layers, thereby allowing the communication to be realized at high speed”). Because Mr. Brooks has a poor memory of the state of technology in the relevant timeframe, his testimony about what a person of skill in the art knew, and what they would have found obvious, is untrustworthy and should not be relied upon.

C. Mr. Brooks felt constrained from offering his opinions freely.

The Board should not rely on Mr. Brooks’ direct testimony because his evaluation of the prior art and the issues of this case was tightly constrained. Rather than consider the entirety of the issues, he apparently ignored any evidence or issues unless he had been specifically asked to provide an opinion on it:

Q. Do you have an understanding of what "concurrent" means?

A. I know what "concurrent" means in the English language. However, I also understand that it is a term in the '471 patent which I have not been asked to offer an opinion on.

Q. And do you have an understanding of what "subsequent" means?

A. I understand that the "subsequent" is a term used in the '471 patent of which I have not been asked to offer an opinion on.

Ex.1027, 34:8-18.

Q. In preparing your declaration, did you review the Cornett prior art patent?

A. I reviewed the Cornett patent. I was not asked to provide an opinion on Cornett.

Ex.1027, 52:15-18.

Q. Is direct memory access a concept that would have been known to a person of ordinary skill in the art?

A. I do not -- I was not asked to offer an opinion on that, so I do not have an opinion on that.

Q. Do you know what a DMA device is?

A. I was not asked to offer an opinion on that, so I have no opinion on what a DMA device is.

Ex.1027, 36:21-37:4.

While it is routine and understandable for a declarant to simply decline to offer an on-the-spot opinion about a matter, Mr. Brooks did not do that. He appeared to believe that he **could not** opine on anything unless Lionra had asked him to do so:

Q. Have you used or designed devices using direct memory access in your work?

A. I would say that DMA devices, or a DMA as described by the '471 patent, I have no – **because I can't offer an opinion on what a DMA device is or DMA is**, I would say that I cannot answer the question of whether or not I have used one in my work.

Ex.1027, 37:8-15 (emphasis added).

Q. Do both of those "each" phrases refer to the same plurality of headers?

A. So -- yeah. **I was not asked to offer an opinion on this, so I have no opinion on that.**

Ex.1027, 44:10-13 (emphasis added).

D. Mr. Brooks' opinions are based on unexplained claim construction positions.

Mr. Brooks' limited direct testimony is also entitled to little or no weight because relied on an unexplained interpretation of the claim language. Mr. Brooks' declaration focuses almost exclusively on the issue of whether Nelson—alone—discloses “*concurrently writing*” headers. *See, e.g.*, Ex.2005, ¶37. Mr. Brooks indicated that he believed “concurrently” had a peculiar meaning in the '471 patent:

Q. Is it your understanding that, in Claim 1, the concurrently writing step occurs after the decoding step?

ATTORNEY AUCHTER: Objection. Form. Calls for a legal conclusion.

A. Yeah, as I stated earlier, **I have no opinion on subsequently and concurrently in their meaning in terms of this patent.** So I do not have an opinion on that.

Ex.1027, 47:22-48:5 (emphasis added).

But Mr. Brooks declined to explain what peculiar meaning he attached to the word “concurrently” in rendering his opinions. He repeatedly stated that claim words like “concurrent” and “subsequent” were outside the scope of what he was asked to opine on:

Q. Is it your understanding that "concurrent" is different than "subsequent"?

ATTORNEY AUCHTER: Objection to form. Calls for a legal conclusion.

A. I've not been offered -- excuse me.

I have not been asked to offer an opinion on the meaning of subsequent and concurrent, and have no opinion on that.

Ex.1027, 34:23-35:5.

Q. In your view, is there a difference between performing one action subsequent to another action and performing those two actions concurrently?

ATTORNEY AUCHTER: Same objection. [Form.]

A. I was not asked to consider that. I do not have an opinion on that.

Ex.1027, 34:1-7.

Mr. Brooks would only explain his understanding of the meaning of such words outside the context of the '471 patent:

Q. Outside the context of the '471 patent, in the English language, how does the meaning of "subsequent" compare to the meaning of "concurrent"?

A. "Concurrent" means at the same time. "Subsequent" means following.

Ex.1027, 36:5-10.

Mr. Brooks knows what the ordinary meaning of claim terms like “concurrently” are, but he did not apply that ordinary meaning in preparing his declaration. He attaches a specialized meaning to the word “concurrently” in the context of the '471 patent claims, but he declined to explain that specialized meaning. Mr. Brooks’ direct testimony is thus unreliable and unhelpful because it is based on an interpretation of the claim language that he steadfastly refused to disclose. *See* F.R.E. 705 (“the expert may be required to disclose those facts or data on cross-examination”).

E. Mr. Brooks’ opinions are based on Nelson alone, not on the combination of references in the grounds of unpatentability.

Mr. Brooks expressly ignored the other references relied upon in the Petition’s analysis and in the grounds at issue:

Q. In preparing your declaration, did you review the Cornett prior art patent?

A. I reviewed the Cornett patent. I was not asked to provide an opinion on Cornett.

Ex.1027, 52:15-18.

Q. In preparing your declaration and the statements in paragraph 40, did you consider the petition's reliance on other references beyond Nelson in combination with Nelson?

ATTORNEY AUCHTER: Objection to form.

A. I considered Nelson. **I did not consider other [references] in combination with Nelson.**

Ex.1027, 62:17-23 (emphasis added).

Both grounds of unpatentability rely on a combination of references—with Nelson being employed as a secondary reference:

No.	Claims	Basis
Ground 1	1-3, 5-10, 12-15, 17-21	35 U.S.C. §103 (Pre-AIA) over Cornett, Paatela, and Nelson
Ground 2	8	35 U.S.C. §103 (Pre-AIA) over Cornett, Paatela, Nelson, and Russell

Pet., 16.

Thus, even ignoring all the other concerns about the reliability of Mr. Brooks' declaration, his direct testimony is of little value because it does not address the proposed grounds.

VI. Conclusion

Cisco respectfully requests the Board issue a Final Written Decision finding all Challenged Claims unpatentable.

Respectfully submitted,

Dated: September 10, 2025
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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Petitioner hereby certifies, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Petitioner Reply, that the number of words in this paper is 5,543.

Pursuant to 37 C.F.R. § 42.24(d), this word count excludes the table of contents, table of authorities, mandatory notices under § 42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing.

Dated: September 10, 2025

/Theodore M. Foster/

Theodore M. Foster
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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), the undersigned certifies that a true and correct copy of the foregoing was served on the Patent Owner as detailed below:

<i>Date of service</i>	September 10, 2025
<i>Manner of service</i>	Electronic Email: bcooper@bc-lawgroup.com ; slindner@bc-lawgroup.com ; robert@auchterlaw.com ; Lionra_Counsel@b-clg.com
<i>Documents served</i>	Petitioner Reply Exhibits Ex.1027- Ex.1049
<i>Persons Served</i>	Brett Cooper Seth Lindner BC Law Group, P.C. 200 Madison Avenue, 24th Floor New York, NY 10016 Robert A. Auchter Auchter PLLC 1629 K Street, NW, Suite 300 Washington, DC 20006

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