

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.

Petitioner,

v.

LIONRA TECHNOLOGIES LIMITED,

Patent Owner.

Case IPR2024-01281
U.S. Patent 7,738,471

PATENT OWNER’S SUR-REPLY TO PETITIONER’S REPLY

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TABLE OF PATENT OWNER'S EXHIBITS

Exhibit No.	Description
2001	January 2, 2025 <i>Defendant's P.R. 4-2 Disclosure, Lionra Technologies Limited v. Cisco Systems, Inc.</i> , Case No. 2:24-cv-97 (E.D. Tex.)
2002	May 13, 2025 <i>Memorandum Opinion and Order, Lionra Technologies Limited v. Cisco Systems, Inc.</i> , Case No. 2:24-cv-97 (E.D. Tex.)
2003	April 30, 2025 Letter from B. Rosenthal to B. Cooper
2004	March 19, 2025 <i>Defendant Cisco Systems, Inc.'s Responsive Claim Construction Brief, Lionra Technologies Limited v. Cisco Systems, Inc.</i> , Case No. 2:24-cv-97 (E.D. Tex.)
2005	Declaration of Thomas Brooks in Support of Patent Owner's Response
2006	<i>Curriculum Vitae</i> of Thomas Brooks
2007	Fibre Channel Framing and Signaling (FC-FS) Specification, Rev. 0.50 (September 21, 2000)
2008	University of Washington, Paul G. Allen School of Computer Science and Engineering, CSE467: Advanced Logic Design, Sequential Logic Lecture Notes
2009	U.S. Patent No. 8,929,262

I. INTRODUCTION

Petitioner's efforts to recast its invalidity challenges with unsupported attorney argument fail. The Board should reject all of Petitioner's arguments and hold that the Challenged Claims of the '471 Patent are not unpatentable.

Petitioner and Patent Owner unsurprisingly agree that the District Court's claim construction, as urged by Petitioner and to which Patent Owner agreed, should be applied. Paper 15, Petitioner's Reply, ("Reply"), 8. Moreover, this construction is not so new that Petitioner could not have anticipated and addressed it in the Petition. *See* Paper 12, Patent Owner Response ("POR"), 11-18. As established in the POR, Petitioner has not shown that the *Cornett-Paatela-Nelson* combination discloses, teaches or suggests "concurrently writing ... each individual one of said plurality of headers to a respective protocol stack layer memory," when this limitation is properly construed. *See, e.g.*, POR, 19-36.

Although Petitioner now attempts to deny it, the Petition did, in fact, rely solely on the disclosure of *Nelson* (U.S. Patent No. 7,333,489, Ex. 1006) for the "*concurrently writing*" requirement of the claims. As Petitioner repeatedly asserted, "[t]he Cornett-Paatela combination does not explicitly explain the **timing** of how packet headers are written to Paatela's respective separate memory segments [and] Nelson provides the expected, yet **missing** detail" Paper 1, ("Petition"), 26

(citing Ex. 1003, “*Mir*,” ¶58).¹ But Petitioner did not show that *Nelson* disclosed “concurrently writing ... each individual one of said plurality of headers to a respective protocol stack layer memory.” The only thing that Petitioner or its expert sought to establish was that “Nelson addresses [the timing of how packet headers are written] by explaining that the full packet frame is written into one buffer and the packet headers into another buffer, **in parallel**.” *Mir*, ¶58 (emphasis in original).

Petitioner now propounds a new theory that relies on a previously undisclosed and uncited discussion of “dual-port memory” in *Paatela* (U.S. Patent Publ. No. 2006/0209840, Ex. 1007). *See* Reply, 10-13. This new theory should be rejected because it is (1) improper new reply argument, (2) unsupported attorney argument, and (3) inconsistent with Petitioner’s other arguments. Moreover, this new theory fails on the merits. *Paatela* does not expressly disclose “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory,” leaving Petitioner to argue that *Paatela*’s “dual-port memory ... would support” the limitation. This argument, substantively one of inherency, fails because inherency requires that a limitation is “necessarily present,” and *Paatela* does not disclose that “concurrently writing” is anything more than a possibility. Petitioner’s new theory also fails with respect to

¹ Emphasis is added unless otherwise so indicated.

at least dependent claims 2, 5, 14 and 17 because the required “media access control layer” and “network layer” headers could not be concurrently written with the other headers (PPP and MPLS) upon which Petitioner now improperly relies.

Petitioner's attempted resuscitation of the challenged “material facts” using new prior art, *see* Reply, 16-23, illustrates the inadequacy of the Petition's cited support. Moreover, Petitioner's new arguments are internally inconsistent, further demonstrating why the Board should not consider any “material fact” as admitted.

Lastly, Petitioner's efforts to discredit Patent Owner's expert, Thomas Brooks, and to convert his cross-examination into direct examination, especially based on the plainly unreasonable memory test to which he was subjected in deposition, should be rejected.

II. CLAIM CONSTRUCTION

Independent claims 1 and 13 of the '471 Patent recite “*concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory.*” Ex.1001, 11:54-57 (Cl. 1), 12:38-41 (Cl. 13). As noted in the POR, the Petition in the present *inter partes* review was filed on August 26, 2024. Petition, 74-75. The corresponding Notice of Filing Date Accorded was entered and mailed on September 23, 2024. *See* Paper 5. Consequently, the deadline for a preliminary

response was set for December 23, 2024. *See* 37 CFR § 42.107(b). After that deadline had passed, Petitioner proposed a construction for the “concurrently writing” limitation in the related District Court case. *See* Ex. 2001, January 2, 2025 *Defendant's P.R. 4-2 Disclosure*, 4.

Specifically, Petitioner proposed the construction of: Plain meaning, *i.e.*, “concurrently writing (1) each of said plurality of headers to a CPU main memory space used for the packet transfer and (2) each individual one of said plurality of headers (**each concurrently with each other**) to a respective protocol stack layer memory.” *See Id.* Patent Owner subsequently agreed to the construction of “concurrently writing” as “[p]lain meaning, *i.e.*, ‘concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers (**each concurrently with each other**) to a respective protocol stack layer memory,’” and the Court adopted the agreed construction. *See* Ex. 2002, May 13, 2025 *Memorandum Opinion and Order*, 8.

Petitioner, having advocated for a construction in the District Court that it considers dispositive² and having provided no explanation of why this construction

² *See* Ex. 2003, April 30, 2025 *Letter from B. Rosenthal to B. Cooper*, 1 (“Lionra’s recent agreement to a claim construction requiring the concurrent writing of a plurality of headers effectively resolves the matter. Cisco’s products, as evidenced by source code for the UADP, Silicon One, and LSE ASICs, do not write the headers concurrently in the manner described.”).

should not be applicable in this *inter partes* review, should be bound by this construction without being rewarded by the admission of new evidence and arguments. See, e.g., *Cambridge Mobile Telematics, Inc. v. Sfara, Inc.*, IPR2024-00966, Paper 12 at 8 (PTAB Dec. 13, 2024) (Where a petitioner has proposed a claim term be construed in the District Court proceeding and emphasized the significance and potentially “case dispositive” nature of the proposed construction, “we determine ***the petition is obliged to either apply that construction in this proceeding or explain why that construction is not applicable.***”); see also *Novartis Pharms. Corp. v. Regents of the University of Michigan*, IPR2023-01346, Paper 8, Dissent at 2 (PTAB Mar. 13, 2024) (Fitzpatrick J.) (Dissenting to institution for failure to meet the requirements of 37 C.F.R. § 42.104(b)(3) and (4), stating that “a petitioner should bring a petition ... asserting unpatentability based on a construction the petitioner seeks. A petitioner should not seek an *inter partes* review ... based exclusively on a construction it considers erroneous but ‘adopts’ ‘solely for purposes of this Petition.’”).

In the District Court, Petitioner argued that:

Middle-school grammar rules dictate that a modifier before a numbered list modifies each item in the list. Here, the modifier “concurrently writing” modifies both (1) a plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory. And therefore, the

claims require that the plurality of headers be written concurrently to each of the respective protocol stack layer memories.

Ex. 2004, March 19, 2025 *Cisco Systems, Inc.'s Responsive Claim Construction Brief*, 1 (further identifying the relevant claim language as “crystal clear”).

Petitioner further emphasized the inevitability of this claim construction:

As is readily apparent, the modifier “concurrently writing” applies to both items in the numbered list. As the Federal Circuit has recognized, it is a “general grammatical principle” that a modifier that comes before a series modifies each item in the series. *SIMO Holdings Inc. v. Hong Kong uCloudlink Network Tech. Ltd.*, 983 F.3d 1367, 1377 (Fed. Cir. 2021) (citing Antonin Scalia & Bryan A. Garner, *Reading Law: The Interpretation of Legal Texts* § 19, 147 (2012)). “Th[is] principle has particular force when [like here] the term joining the items in a series is ‘and.’” *Id.* (citing *SuperGuide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 886 (Fed. Cir. 2004)).

Id., 7.

This construction fully accords with both the '471 Patent specification and prosecution history. *See* POR, 15-18. It is readily apparent that Petitioner, especially as the proponent of the construction in the parallel district court litigation, was fully aware of the claim construction that would ultimately apply here when preparing and filing the Petition.

III. THE CLAIMS ARE NOT UNPATENTABLE BECAUSE THE PRIOR ART DOES NOT DISCLOSE, TEACH OR SUGGEST THE “CONCURRENTLY WRITING” CLAIM LIMITATIONS

Petitioner has failed to meet its burden of establishing that the Challenged Claims are unpatentable, and the Petition should be denied for all claims. In the POR, Patent Owner fully established that the relevant independent claim limitations are not disclosed, taught or suggested in the prior art. In reply, Petitioner presents four contrary arguments, none of which withstands scrutiny, and all of which should be rejected by this Board.

A. The Petition relied solely on the disclosure of *Nelson* to teach “concurrently writing”

Notwithstanding Petitioner's denial, Reply, 9, the Petition did, in fact, rely on the disclosure of *Nelson* for “*concurrently writing* (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory” because, as Petitioner repeatedly asserted, “[t]he Cornett-Paatela combination does not explicitly explain the **timing** of how packet headers are written to Paatela's respective separate memory segments [and] Nelson provides the expected, yet *missing* detail” Petition, 26 (*citing Mir*, ¶58); *see also Mir*, ¶88 ([T]he combination of Cornett and Paatela render obvious a *decoder* that is *configured for writing* (1) *each of said*

plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory.”).

Indeed, the Petition is replete with Petitioner's reliance on *Nelson* for disclosure of “*concurrently writing*”:

- “Nelson teaches writing packets and packet headers into separate memory locations in parallel so that routing decisions can be made more efficiently,” Petition, 7;
- “[W]riting an entire packet frame into one buffer and the packet headers only into another buffer in parallel to accelerate routing decisions, per Nelson,” Petition, 25, 63;
- “A POSITA would have therefore looked to Nelson to provide the missing detail ...,” Petition, 30 (citing *Mir*, ¶65);
- “Nelson teaches writing a packet frame (header and payload) into one buffer and the packet headers into another buffer, with the two writing operations occurring in parallel,” Petition, 30 (citing *Nelson*, 7:1-4);
- “Nelson similarly seeks to process packets faster by writing headers and frames into separate buffers—in parallel—so that header information is made available for routing decisions without the need (and associated delay) to read the entire frame from the buffer,” Petition, 31 (citing *Nelson*, 2:3-10);
- “The move operation would be performed in parallel, per Nelson,” Petition, 32, 66-67 (citing *Nelson*, 7:1-4);
- “The Cornett-Paatela combination does not explicitly explain the timing of how Cornett's packet headers are written to Paatela's respective, separate segments of memory. This timing is explained in Nelson,” Petition, 42 (citing *Mir*, ¶88).
- “Nelson similarly accelerates packet processing by writing an entire packet to one buffer and just the packet headers into another buffer in parallel

because this allows Nelson to make routing decisions without reading the full frame out of the frame buffer,” Petition, 43 (citing *Nelson*, 2:3-10);

- “Cornett’s NIC would cause the DMA engine to perform both storage operations in parallel, i.e., concurrently, per Nelson,” Petition, 44, 69 (citing *Nelson*, 6:66-7:4; *Mir*, ¶¶ 91, 146, respectively); and
- “Nelson seeks to process packets faster by writing headers and frames into separate buffers—in parallel—so that header information is made available for routing decisions without the need (and associated delay) to read the entire frame from the buffer,” Petition, 65 (citing *Nelson*, 2:3-10).

Petitioner’s reliance on *Nelson* is unavailing because Petitioner did not show that *Nelson*, or anything else, disclosed, suggested or taught “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory,” as the claims require. The only thing that Petitioner or Petitioner’s expert sought to establish was that “Nelson addresses [the timing of how headers are written] by explaining that the full packet frame is written into one buffer and the packet headers into another buffer, **in parallel.**” *Mir*, ¶58 (emphasis in original). As explained in the POR, Petitioner’s evidence and argument did not satisfy the entirety of the “concurrently writing” limitation, particularly “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory.” POR, 28-35.

In reply, Petitioner cites Dr. Mir's declaration for the proposition that the *Cornett-Paatela-Nelson* combination "renders obvious writing the headers to their respective layer memories in parallel with one another." Reply, 13-15. But these aspects of the declaration were not cited in either the Petition's, or Dr. Mir's, analysis of the relevant claim limitation. See Petition, 41-44; *Mir*, ¶¶ 88-91. Furthermore, the POR, and the supporting declaration of Mr. Brooks, for which Petitioner provides no substantive refutation, demonstrate that *Nelson* does not disclose "concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory." Petitioner's conclusion that "[w]riting each of the protocol headers to its respective protocol header memory in parallel would have been obvious because doing so would 'accelerate packet processing'" is nothing more than unsupported attorney argument and should be disregarded by the Board. "'Attorney argument is not evidence' and cannot rebut other admitted evidence, ..." *Elbit Systems of America, LLC v. Thales Visionix, Inc.*, 881 F.3d 1354, 1359 (Fed. Cir. 2018) (citing *Icon Health & Fitness, Inc. v. Strava, Inc.*, 849 F.3d 1034, 1043 (Fed. Cir. 2017)).

B. Petitioner's argument that *Paatela's* dual-port memory teaches this limitation is procedurally improper and internally inconsistent with the Petition's contentions

Petitioner attempts to revive its invalidity arguments and rebut Patent Owner's evidence that *Nelson* does not and could not disclose, teach or suggest "concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory" by improperly asserting a new theory that shoehorns in a previously uncited disclosure in *Paatela*. See Reply, 10-11. This new theory, relying on *Paatela's* description of dual-port memory, should be rejected because it is (1) improper new argument first raised in the reply, (2) mere attorney argument, and (3) inconsistent with Petitioner's other arguments in the Petition.

In the Petition, Petitioner relied on *Paatela* for its disclosure of "writing packet headers into individual memory segments to accelerate processing," allegedly "teaching that each individual header is written to a respective, separate memory segment for processing." Petition, 25-26. Petitioner never referenced, let alone cited, *Paatela's* disclosure of dual-port memory. Even if Patent Owner proffered a "new" construction, Petitioner should not be permitted to rely on a new invalidity theory and Petitioner's reply theory crosses the line from the responsive to the new. See *Unified Patents LLC v. VL Collective IP LLC*, IPR2022-01434, Paper No. 49, 5

(P.T.A.B. Mar. 20, 2024). Petitioner's new invalidity theory is improper and should be rejected.

Petitioner's new invalidity should also be rejected because it is not supported by expert testimony. "'Attorney argument is not evidence' and cannot rebut other admitted evidence, ..." *Elbit Systems*, 881 F.3d at 1359. In addition to relying on *Paatel's* disclosure of dual-port memory, Petitioner also relies on *Paatel's* disclosure of quad-port memory. Reply, 10-11. *Paatel*, however, makes only a single reference to quad-port memory, *Paatel*, [0078], without further detail as to how that quad-port memory might be used. Yet Petitioner asserts, without any evidence or explanation, that "it would have been obvious to a POSITA that a 'quad-port memory' would support writing four 32-bit words simultaneously." Reply, 11. In the same vain, Petitioner baldly asserts that "Paatela's suggestion of a 'multi-port memory,' with an arbitrary number of ports, would allow an arbitrary number of protocol headers to be simultaneously written." Reply, 13; *see also id.*, 11. These unsupported arguments should be rejected.

The new invalidity theory should also be rejected because it is contradictory to the positions taken in the Petition, which discussed dual-port memory only with respect to the dual-port RAM described in *Nelson*. *See* Petition, 42 ("According to *Nelson*, '[d]ual port RAM can be used to store the header information' instead of a

FIFO.”)(citing *Nelson*, 6:8-9). The Petition referenced *Nelson*’s dual-port RAM in the context of simultaneous reading from and writing to the dual-port RAM, and not writing to both ports of the dual-port RAM. More specifically, to justify the assertion that it would “have been obvious to a POSITA that packet headers are written to Paatela’s respective, separate segments of memory such that they are available for immediate processing,” Petition, 44, Petitioner argued that “[t]his is consistent with Nelson making header information stored in its header buffer available for immediate routing decision without reading the entire frame out of a frame buffer,” *id.*, 44-45. Petitioner then articulated the basis for this argument, that “Nelson’s use of ‘dual port RAM’ to store headers ... would facilitate immediate processing ***because data written into dual port RAM can be read out of the RAM at the same time.***”) *Id.*, 44-45 (citing *Mir*, ¶92). Petitioner now asserts, in direct contradiction to the evidence and argument set forth in the Petition, that both ports on a dual-port memory can be written simultaneously to satisfy the claims.

Petitioner cannot have it both ways because its Reply arguments and Petition arguments are mutually exclusive. Either there is simultaneous reading from one port and writing to the other port on the dual-port memory to satisfy “available for immediate processing within a protocol stack layer,” **or** there is simultaneous writing to both ports on the dual-port memory to satisfy “concurrently writing ... each

individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory.” Both limitations cannot be satisfied. Consequently, Petitioner fails to show that the Challenged Claims are unpatentable.

Petitioner's citations to a different embodiment in *Paatela* are procedurally improper, unsupported by expert testimony, contradicted by Petitioner's arguments in the Petition regarding the use of dual-port memory, and still do not show that the proposed combination discloses, teaches or suggests “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory.”

C. Petitioner's argument that the use of dual-port memory, to store the PPP and MPLS headers, is procedurally improper and fails on the merits

Petitioner's new theory based on *Paatel's* disclosure of dual-port memory, quad-port memory, multi-port memory, *see* Reply, 10-13, should also be rejected as (1) based on new prior art regarding the PPP and MPLS headers that should have been cited in the Petition, (2) improper new argument first raised in the reply, and (3) attorney argument unsupported by expert testimony. Moreover, Petitioner has still failed to show that that the new theory renders the Challenged Claims unpatentable.

Petitioner cites nine new references, exhibits 1028-1036, for the proposition that the PPP and MPLS headers are 32-bits long or less. *Id.* These references were not cited in the Petition and should be deemed new prior art teaching a claim limitation. As such, they run afoul of the Federal Circuit's holding "that a petitioner may not in reply rely on new prior art to teach a claim limitation." *Axonics Inc. v. Medtronic Inc.*, 75 F.4th 1374, 1383 (Fed. Cir. 2023) (citing *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (holding a reply brief and declaration exceeded the proper scope for a reply because they cited "a number of non-patent literature references which were not relied upon to support unpatentability in the Petition"))).

In addition to being improper, Petitioner's newly raised arguments that the PPP and MPLS headers are small enough to be "concurrently written" by *Paatela's* dual-port memory alternative embodiment,³ Reply, 10-13, fail on the merits. Petitioner does not point to an express disclosure in *Paatela* of "concurrently writing ... each individual one of said plurality of headers (each concurrently with each other)." Rather, Petitioner asserts that, because *Paatela* discloses that "two 32-bit

³ As with Petitioner's arguments regarding *Paatela's* disclosure of "quad-port memory" and "multi-port memory," Petitioner's arguments regarding the PPP and MPLS protocols are not supported by expert testimony. "'Attorney argument is not evidence' and cannot rebut other admitted evidence, ..." *Elbit Systems*, 881 F.3d at 1359.

words may be simultaneously written,” Reply, 10 (citing *Paattela*, [0078]), Petitioner contends that “the simultaneously written 32-bit words ... represent multiple different protocol layer headers ... [if the] headers are 32 bits long or less,” Reply, 11. Petitioner couches this argument as one of obviousness, but is, in reality, substantively one of inherency because there is not an express disclosure of “concurrently writing” a plurality of headers in *Paatela*.

“[T]o rely on inherency to establish the existence of a claim limitation in the prior art in an obviousness analysis,” Petitioner must show that the limitation is “necessarily present” or “the natural result of the combination of elements explicitly disclosed by the prior art.” *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1195-96 (Fed. Cir. 2014). Petitioner’s unsupported attorney argument fails to meet this high standard for inherency. *See id.* at 1195. Petitioner’s argument is nothing more than one of possibilities.⁴ *See* Reply, 12 (“the dual-port memory for headers described by ... *Paatela* **would support** writing two 32-bit protocol headers associated with two different protocols”). “Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing *may*

⁴ Another possibility, with respect to *Paatela*’s disclosure that “two 32-bit words may be simultaneously written,” *Paattela*, [0078], is that the simultaneous writing to both ports of the dual-port memory occurs when writing headers that are longer than 32-bits (4-Bytes), such as the 14-Byte Ethernet, 20-Byte IPv4, or 40-Byte IPv6 headers referenced *infra*.

result from a given set of circumstances is not sufficient.” *PAR*, 773 F.3d at 1195. Petitioner’s additional arguments, that an undisclosed arrangement of “quad-port memory” or ““multi-port memory,’ with an arbitrary number of ports, would allow an arbitrary number of protocol headers to be simultaneously written,” Reply, 13, are little more than pure conjecture and fare the same as the dual-port memory argument.

Petitioner has also failed to show that numerous limitations of the challenged dependent claims are met. First, claims 2 and 14 of the ’471 Patent recite that “at least one of said plurality of headers is a media access control layer protocol header.” Ex. 1001, 11:60-62, 12:44-46. Petitioner identified the Ethernet header as the only example of a “media access control layer protocol header.” Petition at 46-47, 56. The Ethernet header, excluding the Preamble (and Start of Frame delimiter), is 112-bits (14-Bytes) in length. Ex. 1042, IEEE 802.3 (1998), 76-78.⁵ When a PPP header is used within an Ethernet frame, the PPP header is at least 32-bits (4-Bytes) long. Ex. 1029, Figs. 12A, 12B. The combination of the Ethernet and PPP headers is 144-bits (18-Bytes), exceeding the 64-bits (or 128-bits) available in Petitioner’s purported dual-port memory (or quad-port memory) scenarios. The Ethernet header

⁵ The result is the same if older formats of the IEEE 802.3 header or DIX header are considered. See Ex. 1029, Fig. 13, Ex. 1043, Figs. 4A, 4B.

and PPP header cannot be simultaneously written in either scenario. Consequently, *Paatela* cannot satisfy the requirement of “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory” where “at least one of said plurality of headers is a media access control layer protocol header.” The result is the same when a MPLS header (32-bits, *see* RFC1022, 3) is used within an Ethernet frame. Petitioner’s new theory fails to show that claims 2 and 14 of the ’471 Patent are unpatentable.

Second, claims 5 and 17 of the ’471 Patent recite that “at least one of said plurality of headers is a network layer protocol header.” Ex. 1001, 12:5-6, 12:56-57. Petitioner identified the Internet Protocol header as the only example of a “network layer protocol header.” Petition at 49-50, 56. IPv4 has a header with a length of 160-bits (20-Bytes). Ex. 1009, Tanenbaum, 413. IPv6 has a header with a length of 320-bits (40-Bytes). *Id.*, 438-439. The length of each of the IPv4 and IPv6 headers exceeds the 64-bits (or 128-bits) available in Petitioner’s purported dual-port memory (or quad-port memory) scenarios. Neither a IPv4 header nor a IPv6 header can be simultaneously written with another header in either scenario. Consequently, *Paatela* cannot satisfy the requirement of “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory” where “at least one of said plurality of

headers is a network layer protocol header.” Petitioner’s new theory fails to show that claims 5 and 17 of the ’471 Patent are unpatentable.

In summary, Petitioner failed to meet its burden of establishing that “the description in Nelson and Paatela of using a dual-port, quad-port, or multi-port memory to store protocol layer headers renders obvious writing multiple layers’ headers ‘currently [sic] with each other’ as required.” Reply, 15.

IV. PETITIONER’S “MATERIAL FACTS” ARE NOT ADMITTED AND HAVE NOT BEEN ESTABLISHED BY PETITIONER

Petitioner’s attempted resuscitation of the challenged material facts from the Petition using new prior art, *see* Reply, 16-23, illustrates the inadequacy of the cited support in the Petition. Moreover, as detailed below, Petitioner’s new arguments are internally inconsistent, further demonstrating why the Board should not consider any of these “material facts” as admitted.

As to Material Facts #1, #2 and #4, whether Petitioner could eventually find a reference that references a “TCP/IP model” comparable to the OSI model is irrelevant. Even though Ex. 1038 states that “TCP/IP is a protocol system,” Ex. 1038, [0003], it also qualifies any discussion of layers by noting “[i]t is helpful to understand that the TCP/IP protocol defines discrete functions that are to be performed by compliant systems at different ‘layers’ of the TCP/IP model.” *Id.*, [0006]. Furthermore, Petitioner’s references are inconsistent as to exactly what the

purported “TCP/IP model” encompasses. *Compare* Ex. 1010, [0009] (“The TCP/IP protocol stack has four layers ...) *with* Ex. 1039, 4:5-23 (identifying “five layers” for TCP/IP).

As to Material Fact #8, Petitioner’s assertion that “before the priority date of the ’471 patent, in IEEE 802.3, use of a logical link control layer header was required” is contradicted by at least U.S. Patent No. 6,438,128, cited by Dr. Mir, which states that “the IEEE 802.3 standard does not provide for conveyance of SNAP and LLC header information” Ex. 1015, 2:31-33. This comports with the 1998 IEEE 802.3 standard:

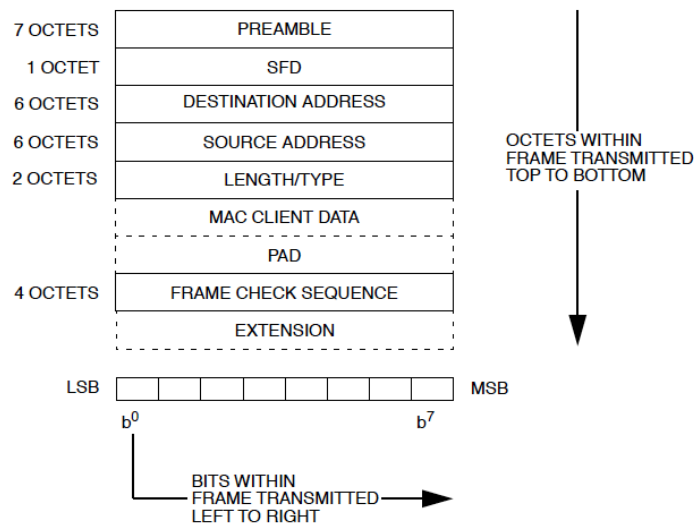


Figure 3-1 – MAC frame format

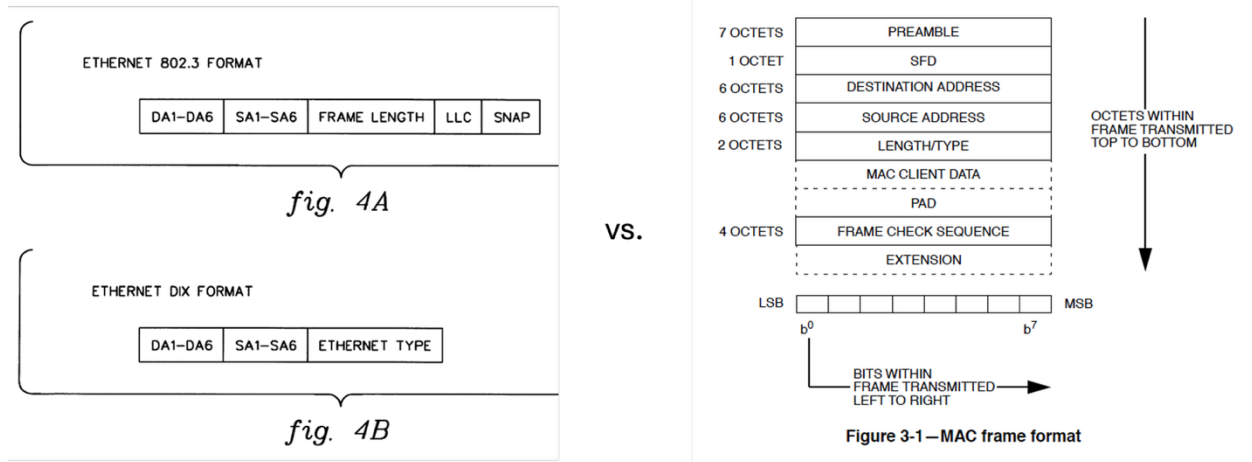
Ex. 1042, 76 (“Figure 3-1 shows the nine fields of a frame: the preamble, Start Frame Delimiter (SFD), the addresses of the frame’s source and destination, a length

or type field to indicate the length of protocol type of the following field that the [sic] contains the MAC Client data, a field that contains padding if required, the frame check sequence field containing a cyclic redundancy check value to detect errors in a received frame, and an extension field if required ...”).

V. PETITIONER’S UNSUCCESSFUL EFFORTS TO ELICIT TESTIMONY BEYOND THE SCOPE OF THE WITNESS’S DECLARATION SHOULD BE DISREGARDED

Petitioner’s efforts to discredit the testimony of Patent Owner’s declarant, Thomas Brooks, are not well-founded and the Board should give weight to Mr. Brooks’ declaration testimony as it is fully supported. Petitioner did not establish any deficiencies in the bases or reasoning for Mr. Brooks’ declaration opinions.

Petitioner’s efforts to cast aspersions upon Mr. Brooks based upon his knowledge of the history of Ethernet must be considered from the proper perspective. While DIX and older versions of the IEEE 802.3 standard had different frame and header formats, by 1998, when Mr. Brooks graduated and started work as a VLSI Design Engineer at IBM on Gigabit Ethernet (as introduced in 1998 IEEE 802.3 standard, *see* Ex. 1042, 12), *see* Ex. 2006, 2, the IEEE 802.3 standard had been modified to bridge the frame format in those older standards. *Compare* Ex. 1043, Figs. 4A, 4B *with* Ex. 1042, Fig. 3-1:



The older IEEE 802.3 header had a Frame Length field. Ex. 1043, Fig. 4A. The DIX header had an Ethernet Type field. *Id.*, Fig. 4B. The 1998 IEEE 802.3 bridged those formats with a Length/Type field. Ex. 1042, 76, 78 (depending on the value of the field, interpreted as Length or Type, with the interpretations being mutually exclusive). Whether Mr. Brooks knew anything about the older formats, including DIX, is irrelevant because those formats were supplanted in the 802.3 standard years before the '471 Patent was filed.⁶ Moreover, as Petitioner recognizes, any differences that may have existed from the older formats were “relatively minor.” Reply, 24. Petitioner’s arguments and purported evidence, proffered in an effort to discredit Mr. Brooks’ testimony, should be disregarded.

⁶ As set forth in Section IV, the 1998 IEEE 802.3 standard did not require a logical link control layer. Compare Ex. 1043, Fig. 4A with Ex. 1042, Fig. 3-1; see also Ex. 1015, 2:19-20 (“DIX Ethernet does not use LLC or SNAP headers”).

The Board should also consider the full context of Petitioner's criticism of Mr. Brooks based on U.S. Patent No. 7,072,823. Mr. Brooks was only one of five named inventors (and not listed at all on the priority provisional application, 60/280,588, entitled "Virtual Storage Network). In addition, the ellipses in Petitioner's quotation, Reply, 28-29, omit an important point regarding transfer of packets between a "first controller" and "second controller", including that "[p]ackets associated with a client system request, such as a [sic] to store a file, may be stored to verify the receipt of all corresponding packets that are associated with the file before the set of packets or corresponding information may then be transferred to the second controller 120." Ex. 1046, 6:33-40. When the entire section is considered, especially 6:29-42, it is apparent that the sentences emphasized by Petitioner refer to collecting and sharing packets associated with a client system request and not to the transfer of packets between "components on different networking layers," as Petitioner urges.

Petitioner's efforts to convert cross-examination into direct examination and fault Mr. Brooks' recollection of events more than two decades in the past should be disregarded by this Board. In an *inter partes* review, "[f]or cross-examination testimony, the scope of the examination is limited to the scope of the direct testimony." 37 C.F.R. § 42.53(d)(5)(ii). The direct testimony is Ex. 2005, Mr.

Brooks' Declaration. Moreover, as Petitioner concedes, "it is routine and understandable for a declarant to simply decline to offer an on-the-spot opinion about a matter." Reply, 31. Those on-the-spot opinions reasonably encompass claim construction, especially where, as here, the claim construction is plain meaning. *See* POR, 12.

Moreover, Mr. Brooks' direct testimony explained the claim construction he applied to the relevant claim limitations. "For the highlighted phrase 'concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory' in the independent claims, I have been asked to apply the following claim construction, as determined by the Court in the related District Court case, in my analysis: Plain meaning, i.e., 'concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory.'" Ex. 2005, ¶ 26.

When a Petitioner seeks to obtain deposition testimony beyond the scope of the direct testimony in an *inter partes* review, presumably for use in a related district court litigation, the Board should not sanction a witness for his or her unwillingness to participate in an unwarranted use of the *inter partes* review discovery process.

VI. CONCLUSION

Petitioner has failed to meet its burden of establishing that the Challenged Claims are unpatentable and the Petition should be denied for all claims.

Respectfully submitted,

Dated: October 22, 2025

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CERTIFICATE OF WORD COUNT (37 C.F.R. § 42.24(d))

The undersigned hereby certifies that the word count in this Patent Owner's Sur-Reply is 5,321, as counted by the word-processing program Microsoft Word that was used to generate this Patent Owner's Sur-Reply, where such word count excludes the table of contents, table of authorities, mandatory notices, certificate of service, appendix of exhibits, claim listing, and this certificate of word count. This Patent Owner's Sur-Reply is in compliance with the 5,600-word limit set forth in 37 C.F.R. § 42.24(c)(4).

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the above document and its accompanying exhibits were served on October 22, 2025, by filing this document through the Patent Trial and Appeal Case Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

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