

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.

Petitioner,

v.

LIONRA TECHNOLOGIES LIMITED,

Patent Owner.

Case IPR2024-01281
U.S. Patent 7,738,471

**PATENT OWNER'S REQUEST FOR DIRECTOR REVIEW
UNDER 37 C.F.R. § 42.75**

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Patent Trial and Appeal Board
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TABLE OF PATENT OWNER’S EXHIBITS

Exhibit No.	Description
2001	January 2, 2025 <i>Defendant’s P.R. 4-2 Disclosure, Lionra Technologies Limited v. Cisco Systems, Inc.</i> , Case No. 2:24-cv-97 (E.D. Tex.)
2002	May 13, 2025 <i>Memorandum Opinion and Order, Lionra Technologies Limited v. Cisco Systems, Inc.</i> , Case No. 2:24-cv-97 (E.D. Tex.)
2003	April 30, 2025 Letter from B. Rosenthal to B. Cooper
2004	March 19, 2025 <i>Defendant Cisco Systems, Inc.’s Responsive Claim Construction Brief, Lionra Technologies Limited v. Cisco Systems, Inc.</i> , Case No. 2:24-cv-97 (E.D. Tex.)
2005	Declaration of Thomas Brooks in Support of Patent Owner’s Response
2006	<i>Curriculum Vitae</i> of Thomas Brooks
2007	Fibre Channel Framing and Signaling (FC-FS) Specification, Rev. 0.50 (September 21, 2000)
2008	University of Washington, Paul G. Allen School of Computer Science and Engineering, CSE467: Advanced Logic Design, Sequential Logic Lecture Notes
2009	U.S. Patent No. 8,929,262
2010	Patent Owner’s Oral Argument Demonstratives

I. Introduction

Pursuant to 37 C.F.R. § 42.75, Patent Owner requests Director Review of the Final Written Decision (Paper 26, “FWD”) that the Challenged Claims of US 7,738,471 (“the ’471 Patent”) are unpatentable over US 2006/0072564 (“Cornett”), US 2006/0209840 (“Paatela”), US 7,333,489 (“Nelson”), and US 6,678,746 (“Russell”). The Board’s decision rests on a theory of unpatentability that Petitioner first introduced in reply to address claim scope that it characterized as “crystal clear” in district court and that contradicted the claim scope presented in the Petition (“Pet.”). The Board abused its discretion in considering the new reply theory.

The Board further made erroneous findings of material fact and erroneous conclusions of law with respect to the new reply theory based on Paatela. It is undisputed that Paatela does not expressly disclose “concurrently writing ... each individual one of said plurality of headers (*each concurrently with each other*).”¹ Petitioner and the Board rely on attorney argument as to what Paatela “would support” to fill this gap in the disclosure, thereby invoking a theory of inherency. In the context of obviousness, inherency places a high burden to prove that the presence of a missing element is not merely probable or possible, but is necessarily the natural result of the operation as taught in the prior art. This burden has not been satisfied and the FWD fails to provide substantial evidence as to unpatentability.

¹ Emphasis is added unless otherwise indicated.

II. Background

A. The Petition

The '471 Patent is titled “High Speed Packet Processing in a Wireless Network.” Ex. 1001. The '471 Patent is generally directed to “a method and apparatus for high speed protocol header processing at an intermediate and/or destination node of a packet-based communications network.” *Id.*, 1:8-11. The '471 Patent was asserted against Petitioner in a case filed on February 13, 2024 in the Eastern District of Texas. *See* Ex. 1022. Petitioner filed a request for *inter partes* review on August 26, 2024. *See* Pet. Patent Owner did not file a preliminary response and review was instituted on March 13, 2025. *See* Paper 6.

Independent claims 1 and 13 of the '471 Patent recite the limitation of “*concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory.*” Ex. 1001, 11:54-58, 12:38-41. With respect to this limitation, the Petition asserted that: (1) Cornett taught “*writing ... each of said plurality of headers to a packet buffer memory,*” Pet., 35-38; (2) Paatela taught “*writing ... each individual one of said plurality of headers to a respective protocol stack layer memory,*” Pet. at 38-41; and (3) Nelson taught “*concurrently writing,*” Pet., 41-44.

B. Claim Scope

The Petition contended “that no claim term requires express construction.” Pet. at 13 (citing Ex. 1003, ¶41 (“I have reviewed the ... patent, as well as its

prosecution history. It is my opinion that ... no terms require express construction.”). However, in the District Court and after the preliminary response deadline, Petitioner proposed the following for “concurrently writing ...”: “Plain meaning, *i.e.*, ‘concurrently writing (1) each of said plurality of headers to a [packet buffer memory] and (2) each individual one of said plurality of headers (**each concurrently with each other**) to a respective protocol stack layer memory.’” Ex. 2001, 4.

In its claim construction brief in the District Court, Petitioner argued that:

Middle-school grammar rules dictate that a modifier before a numbered list modifies each item in the list. Here, the modifier “concurrently writing” modifies both (1) a plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory. And therefore, the *claims require that the plurality of headers be written concurrently to each of the respective protocol stack layer memories.*

Ex. 2004, 1 (characterizing the claim language as “*crystal clear*”), 7 (“As the Federal Circuit has recognized, it is a ‘general grammatical principle’ that a modifier that comes before a series modifies each item in the series... ‘Th[is] principle has particular force when [like here] the term joining the items in a series is ‘and.’”) (citations omitted).² The parties subsequently agreed to, and the court adopted, “[p]lain meaning, *i.e.*, ‘concurrently writing (1) each of said plurality of headers to

² Consistent with the plain language, Petitioner also noted that, in prosecution, “the applicant unequivocally explained that the claimed invention requires both: (1) concurrently writing each header to a packet buffer memory and (2) **concurrently writing each individual one of said plurality of headers to a respective protocol stack layer memory.**” *Id.*, 8-9.

a packet buffer memory and (2) each individual one of said plurality of headers (**each concurrently with each other**) to a respective protocol stack layer memory.” Ex. 2002, 8.

C. Patent Owner’s Response

Patent Owner filed its Response (“POR”) to the Petition on June 18, 2025, setting forth the reasons that the Cornett-Paatela-Nelson combination fails to disclose the limitation of “concurrently writing ...” in the claims of the ’471 Patent. More specifically, the POR demonstrated that neither Cornett, Paatela, nor Nelson disclosed “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) ...” as Petitioner’s “plain language interpretation” requires. POR, 12-19, 23-37 (citing Ex. 2005, ¶¶ 28-44).

The POR demonstrated that the Petition’s challenge to “concurrently writing” was limited to the disclosure of Nelson. *See* POR, 22-23 (citing Pet. at 29 (“Cornett uses the DMA engine to store packet headers in one buffer and the entire packet (header and payload) in another, separate buffer. The Cornett-Paatela combination would use Cornett’s DMA engine to move each of a packet’s individual header into a respective memory segment, per Paatela. *The timing of how packet headers are written to the respective memory segments is not explicit in the combination.*”), 42 (“The Cornett-Paatela combination does not explicitly explain the timing of how Cornett’s packet headers are written to Paatela’s respective, separate segments of memory. This timing is explained in Nelson.”).

D. Petitioner's Reply

Petitioner filed its Reply on September 10, 2025. With respect to claim scope, Petitioner stated that, “[i]f the Board construes the “concurrently writing” limitation, Petitioner agrees that the Board should adopt the court’s construction.” Reply, 8. Petitioner offered no substantive rebuttal to the POR, instead propounding a new theory that relied on a previously uncited discussion of “dual-port memory” in Paatela. *See id.*, 10-13. Petitioner further asserted that “the description in Nelson and Paatela of using a dual-port, quad-port, or multi-port memory to store protocol layer headers renders obvious writing multiple layers’ headers ‘currently with each other’ [sic] as required by the claim construction.” *Id.*, 13-15. The Reply did not address any other limitations or claims and relied exclusively on attorney argument.

E. Patent Owner's Sur-Reply

Patent Owner filed its Sur-Reply on October 22, 2025. Patent Owner demonstrated that Petitioner’s new theory based on Paatela’s “dual-port memory” should be rejected because it (1) was an improper new reply argument, and (2) fails on the merits. On the merits, Patent Owner demonstrated that Paatela does not expressly disclose “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory,” leaving Petitioner to argue that Paatela’s “dual-port memory ... would support” the limitation. Petitioner’s argument as to what Paatela’s “dual-port memory ... would support” is substantively an argument of inherency. This

argument fails because inherency requires that a limitation is “necessarily present” in the prior art, and Paatela does not disclose that “concurrently writing” is anything more than a possibility. Patent Owner also demonstrated that Petitioner’s new theory fails with respect to at least dependent claims 2, 5, 14 and 17, which Petitioner did not address in its Reply, because the required “media access control layer” and “network layer” headers could not be concurrently written with the other headers (PPP and MPLS) upon which Petitioner’s new theory improperly relies.

F. Final Written Decision

The Board issued the FWD on March 4, 2026. As to the “concurrently writing ...” limitation, the Board adopted the construction from the District Court case. FWD, 15-20. With respect to “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory,” the Board, evaluating the circumstances under the standard articulated by the Federal Circuit in *Axonics, Inc. v. Medtronic, Inc.*, 75 F.4th 1374 (Fed. Cir. 2023), concluded that “[b]ecause Patent Owner proposed an express construction for the ‘concurrently writing’ requirement for the first time in the Response, Petitioner ‘must be given the opportunity in its reply to argue and present evidence of anticipation or obviousness under the new construction.’” FWD, 66-69. The Board also rejected Patent Owner’s arguments that Petitioner’s new reply arguments based on Paatela are substantively directed to inherency, instead finding that a person of skill in the art would find them obvious. *See id.*, 76-80.

III. The Board Abused its Discretion in Accepting Petitioner’s New Theory of Invalidity, First Introduced in Reply

The Petition, at most, established that the Cornett-Paatela-Nelson combination taught “concurrently writing ... headers to a packet buffer memory and ... to a respective protocol stack layer memory.” It failed to establish that the combination taught “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory.” *See* POR, 23-37. Only in Reply did Petitioner introduce the theory that Paatela taught “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory.” *See* Reply, 10-13. Relying on *Axonics*, the Board accepted Petitioner’s reply theory “[b]ecause Patent Owner proposed an express construction ... for the first time in the Response.” FWD, 69. The Board erred in doing so.³

The present circumstances are distinguishable from *Axonics*. Patent Owner did not spring a new construction in the POR. Rather, Patent Owner asked that the Board hold Petitioner to what it deems the “plain language interpretation” of the claim. By Petitioner’s arguments and logic, it could not help but be fully aware of

³ The Board also asserted that a petitioner “may introduce new evidence after the petition stage if the evidence is a legitimate reply to evidence introduced by the patent owner.” FWD, 70 (citing *Apple Inc. v. Andrea Elecs. Corp.*, 949 F.3d 697, 706 (Fed. Cir. 2020)). However, the Board cited no POR “evidence” that the Reply was directed to.

the “plain language interpretation” of the claim to be applied when preparing and filing the Petition. Yet, Petitioner ignored that “plain language” in the Petition.

For example, Petitioner’s proposed construction, as ultimately adopted in the District Court and by the Board, is the “plain meaning.” *See* Ex. 2001, 4, 7 (“straightforward application of ... general grammatical principle dictates that ‘concurrently writing’ also modifies the phrase ‘each individual one of said plurality of headers to a respective protocol stack layer memory’ [and] the *plain and ordinary meaning* requires that the headers must be written each concurrently with each other to their respective protocol stack layer memories.”). Yet, as evidenced by the new argument in the reply, the Petition did not apply the plain and ordinary meaning.

The *inter partes* review rules set out in 37 C.F.R. § 42.104(b) specify the precise requirements for a petition to seek relief, requiring the identification of how each “claim is to be construed” and how each “construed claim is unpatentable under the statutory grounds identified.” 37 C.F.R. § 42.104(b)(3)-(4). “[T]he construction proposed by the Petitioner” must be “one *that Petitioner believes is the correct construction under applicable law* and should apply in the involved proceeding.” *Toyota Motor Corp. v. BlitzSafe Texas, LLC*, IPR2016-00422, Paper 12, at 26 (PTAB Jul. 6, 2016). “Although the Board’s trial rules ‘do not necessarily prohibit petitioners from taking inconsistent claim construction positions before the Board and a district court,’ when a petitioner takes alternative positions before the Board and a district court, that petitioner should, at a minimum, explain why alternative

positions are warranted.” *Revvo Techs., Inc. v. Cerebrum Sensor Techs., Inc.*, IPR2025-00632, Paper 20 (Director Nov. 3, 2025) (precedential).

Whether or not Patent Owner proffered an “express construction” in the POR, Petitioner nonetheless took contradictory views of the scope of the claims in the Petition and in the District Court. The Petition took the position that Nelson described “concurrently writing” because it taught “that the packet’s header is written (1) to a frame FIFO 42 (header and payload) ... and (2) to the header FIFO 44 (header only) in parallel, *i.e., concurrently*.” Pet., 42. In the District Court, Petitioner took the opposite position, that “concurrently writing a single header to the packet buffer memory and a single respective protocol stack layer memory” was contrary to the plain meaning of the claims. *See* Ex. 2004, 6-8. Petitioner failed to adequately explain why it took these divergent views.⁴

Petitioner did not comply with its obligations under Rule 42.104(b)(3)-(4). The plain language of the claims requires “the plurality of headers be written concurrently to each of the respective protocol stack layer memories.” Ex. 2004, 7. The Petition failed to establish that any prior art taught this requirement. The Board abused its discretion in allowing Petitioner to correct this failure in a reply theory.

⁴ Not surprisingly, in the District Court, Petitioner emphasized the “case dispositive” nature of its “plain language interpretation.” *See* Ex. 2003, 1 (“Lionra’s recent agreement to a claim construction requiring the concurrent writing of a plurality of headers ***effectively resolves the matter***. Cisco’s products ... do not write the headers concurrently in the manner described.”).

IV. The Board Made Errors of Material Fact and Erroneous Conclusions of Law in the Analysis of Petitioner’s New Theory of Invalidity

In Reply, Petitioner introduced a new invalidity theory, citing 10 new exhibits and relying exclusively on attorney argument, that Paatela taught “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other).” But Petitioner does not point to an express disclosure in Paatela to satisfy the limitation. Rather, Petitioner asserts that, because Paatela discloses that “two 32-bit words may be simultaneously written,” ... “the simultaneously written 32-bit words ... represent multiple different protocol layer headers ... [if the] headers are 32 bits long or less.” Reply, 10-11. Without further explanation, Petitioner conjures up the *mere possibility* of an undisclosed outcome (“simultaneously written headers”) from a given set of circumstances (“simultaneously written 32-bit words”). While Petitioner and the Board assert this as an obviousness argument, *see* FWD, 78-80, it is substantively one of inherency because there is not an express disclosure of “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other)” in Paatela. The Board’s protestations notwithstanding, *see* FWD, 79-80, *LBT IP I LLC v. Apple Inc.*, 2023 WL 3914920 (Fed. Cir. June 9, 2023) is directly on point.

In *LBT*, the Federal Circuit found that an obviousness argument based on a POSITA’s understanding of what may be present for a limitation that is not explicitly disclosed in the prior art must meet the standard for inherency, and anything short of

showing why the limitation is necessarily present does not meet the high bar for inherency. The *LBT* Court, on appeal of several IPRs, dealt with GPS receiver claims reciting, for example, “a battery power monitor configured to selectively activate and deactivate ... transceiver circuitry and location tracking circuitry ...” *LBT*, *2. The primary prior art reference, Sakamoto, disclosed a GPS positioning system that included a portable terminal with a GPS receiver where the GPS signal level is periodically measured to determine system transitions:

1. if GPS signal level is lower than a threshold value, the system transitions to high sensitivity positioning mode;
2. If GPS signal level is higher than a threshold value, the system transitions to normal sensitivity positioning mode; and
3. if positioning cannot be performed when the signal level value is lower than a threshold value, the system transitions into stop-position mode.

LBT, *3. “The Board found Sakamoto discloses activating/reactivating the GPS receiver when it *transitions from stop-position mode into normal sensitivity positioning mode or high sensitivity positioning mode.*” *Id.*, *2. It was undisputed, however, that *Sakamoto* did not expressly disclose such a *transition*. The IPR result hinged on Apple’s expert “to fill in the gap in th[e] disclosure.” *Id.*, *3. The expert testified that a POSITA would have understood that Sakamoto’s GPS receiver would transition out of stop-position mode into normal or high sensitivity positioning mode if the signal level were greater than a predetermined threshold level, and that a receiver that did not do so would “be useless.” *Id.*

While Apple did not “purport to rely on inherency,” based on its concession of Sakamoto’s lack of explicit disclosure and its argument that a POSITA would “understand” the transition out of stop-position mode to be present, the Court concluded that Apple was effectively arguing that the transition “is *inherently disclosed* in Sakamoto.” *Id.* Citing *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1195–96 (Fed. Cir. 2014), the Court further found that, because Apple’s expert did not explain why the transition was ***necessarily present*** in Sakamoto, the standard for inherent disclosure was not met. *LBT*, *3-4.

The present circumstances are analogous. The Petition conceded that the “Cornett-Paatela combination does not explicitly explain the timing of how ... packet headers are written to ... respective, separate segments of memory.” Pet., 31, 29, 42. However, in its new reply theory, Petitioner relied on attorney argument to fill the gap in disclosure by asserting that Paatela’s disclosure “would support” concurrent writing of multiple headers:

- “Nelson and Paatela would support writing two 32-bit protocol headers associated with two different protocols.” Reply, 12.
- “[T]he dual-port memory ... would support writing two 32-bit protocol headers associated with two different protocols, such as PPP and MPLS.” Reply, 12.
- “Paatela’s suggestion of a ‘multi-port memory,’ with an arbitrary number of ports, would allow an arbitrary number of protocol headers to be simultaneously written.” Reply, 13.

Petitioner's new reply theory was directed at how a POSITA would view the possible ways the Paatela dual-port RAM, quad-port RAM or other multi-port memory *could be used* for "simultaneous writing" of multiple headers. As the *LBT* Court recognized, this is substantively an issue of inherency regardless of whether Petitioner couches the argument as one of obviousness. Petitioner must therefore show that "concurrently writing ... each individual one of said plurality of headers (each concurrently with each other)," is "necessarily present" or is "the natural result of the combination of elements explicitly disclosed," *PAR*, 773 F.3d at 1195-96, in Paatela. Petitioner has not done so.

The Board contends that "Patent Owner does not identify a limitation missing from the references like ... in LBT." FWD, 80. This is incorrect. *See* Sur-Reply, 16 ("Petitioner does not point to an express disclosure in Paatela of 'concurrently writing ... each individual one of said plurality of headers (each concurrently with each other).'", 17 ("Petitioner's ... arguments, that an undisclosed arrangement of 'quad-port memory' or 'multi-port memory,' with an arbitrary number of ports ... allow[ing] an arbitrary number of protocol headers to be simultaneously written,' ... are little more than pure conjecture.")). Moreover, as set forth above, the Petition directly acknowledged that Cornett-Paatela does not explicitly disclose the timing of how packet headers are written to separate segments of memory. Pet., 29, 31, 42.

The Board's position is also belied by its own analysis. The Board asserts that Paatela expressly disclosed using a dual-port, quad-port, or multi-port memory to

store headers. FWD, 79. The Board also asserts that “Paatela expressly discloses that ‘two 32-bit words may be simultaneously written to the memory 716’ when implemented as a dual-port memory.” *Id.*, 79-80. The Board then concludes that, “[b]ased on those express disclosures ... it ‘would have been obvious’ to an ordinarily skilled artisan for ‘the simultaneously written 32-bit words to represent multiple different protocol layer headers.’” *Id.*, 80. This conclusion is telling. The Board does not contend that Paatela expressly discloses “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other).” Rather, the Board repeats Petitioner’s assertion that it would be obvious to a POSITA that simultaneously written 32-bit words could “represent multiple different protocol layer headers.” In doing so, the Board tacitly acknowledges that it is relying on the *possible use* of the disclosed memories to satisfy the claims. “In other words, [the Board] argues this [“concurrently writing” of multiple headers] is inherently disclosed in [Paatela].” *LBT*, *3. “Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing *may result* from a given set of circumstances is not sufficient.” *PAR*, 773 F.3d at 1195. The Board erred in distinguishing *LBT* and, by failing to show that “concurrently writing” multiple headers is necessarily present in Paatela, it erred in determining that Paatela satisfies “concurrently writing ... each individual one of said plurality of headers (each concurrently with each other).”

The Board’s analysis of the dependent claims is even more speculative. For example, Claims 2 and 14 recite that “at least one of said plurality of headers is a media access control layer protocol header...” Ex. 1001, 11:60-63, 12:44-47. Claims 5 and 17 recite that “at least one of said plurality of headers is a network layer protocol header ...” *Id.*, 12:5-8, 12:56-59. Petitioner did not address these claims under its new reply theory. Further, Patent Owner pointed out that, for claims 2 and 14, the combination of the Ethernet (“media access control layer protocol header”) and PPP headers, at 144-bits (18-Bytes) in length, and that for claims 5 and 17, the combination of an IPv4 header (“network layer header”) with a length of 160-bits (20-Bytes), or an IPv6 header with a length of 320-bits (40-Bytes), with any other header, exceeded the 64-bits (or 128-bits) available in Petitioner’s purported dual-port memory (or quad-port memory) scenarios” and therefore could not simultaneously be written. Sur-Reply, 18-19. The Board merely concluded that “[a] multi-port memory with a sufficient number of ports supports simultaneously writing an Ethernet header [writing an IPv6 header (or an IPv4 header)] and another header” without citing any evidence or providing any analysis as to what might constitute a “multi-port memory with a sufficient number of ports” that would “support[] [such] simultaneously writing.” FWD, 89 [97]. The Board erred in determining that Paatela satisfies the dependent claims.

Respectfully submitted,

Dated: April 3, 2026

/s/ Brett Cooper

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CERTIFICATE OF SERVICE (37 C.F.R. § 42)

The undersigned hereby certifies that the above document was served on April 3, 2026, by filing this document through the Patent Trial and Appeal Case Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

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