

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,
Petitioner,

v.

LIONRA TECHNOLOGIES, LTD.,
Patent Owner.

IPR2024-01281
Patent No. 7,738,471 B2

**AUTHORIZED RESPONSE TO
DIRECTOR REVIEW REQUEST**

I. INTRODUCTION

Director review is unwarranted here, where the Board rendered a careful 123-page Final Written Decision grounded in precedent and substantial evidence. The Board addressed all arguments raised during the proceeding—including arguments Patent Owner raised for the first time at oral argument—and correctly determined that all challenged claims of U.S. Patent No. 7,738,471 are unpatentable. Paper 26 (“FWD”), 122–123. The Request for Director Review of that decision (Paper 27, “Request”) should be denied. The Board’s decision is well-reasoned, supported by the weight of evidence, and consistent with governing Federal Circuit authority.

Patent Owner raises two principal arguments: (1) that the Board abused its discretion in permitting Petitioner to address the “concurrently writing” limitation in its Reply under the construction Patent Owner proposed for the first time in its Response; and (2) that the Board erred in finding the prior art teaches the “concurrently writing” limitation. Request, 7, 10. Neither argument has merit, and neither warrants Director intervention.

II. THE BOARD CORRECTLY PERMITTED PETITIONER’S REPLY ARGUMENTS UNDER *AXONICS*.

Patent Owner’s principal argument is that the Board abused its discretion in considering Petitioner’s Reply arguments regarding the “concurrently writing”

limitation as applied to the requirement that headers be written “each concurrently with each other” to their respective protocol stack layer memories. Request, 7. This argument fails because the Board’s decision is a straightforward application of the Federal Circuit’s holding in *Axonics, Inc. v. Medtronic, Inc.*, 75 F.4th 1376 (Fed. Cir. 2023).

In *Axonics*, the Federal Circuit held that “where a patent owner in an IPR first proposes a claim construction in a patent owner response, a petitioner must be given the opportunity in its reply to argue and present evidence of anticipation or obviousness under the new construction, at least where it relies on the same embodiments for each invalidity ground as were relied on in the petition.” *Axonics*, 75 F.4th at 1384. Rejecting essentially the same argument that Patent Owner raises here, the Federal Circuit explained that no rule requires “a petition to describe all possible or reasonable claim constructions and to present invalidity theories under those constructions.” *Id.* at 1380–81.

As the Board correctly found, the circumstances here “parallel the circumstances in *Axonics*.” FWD, 66. Neither party identified any claim language for construction pre-institution. Paper 2, 13; Paper 6, 2 (Patent Owner did not file a preliminary response). The Board did not expressly construe any claim term in the Institution Decision. Paper 6, 6. Patent Owner proposed an express construction for the “concurrently writing” requirement for the first time in its Response. Paper 12,

10–11. Petitioner Cisco was entitled to “argue and present evidence of anticipation or obviousness under the new construction” in its Reply. *Axonics*, 75 Fed.4th at 1384.

Cisco’s Reply addressed the new construction by relying on the same embodiments discussed in the Petition, as the Board expressly recognized:

Here, as in *Axonics*, Petitioner relies on the same embodiments for limitation 13.3 in the Petition and the Reply, e.g., Cornett’s Figure 10 embodiment, Paatela’s Figure 7 embodiment, and Nelson’s Figure 5 embodiment. *See* Pet. [Paper 2] 35–45; Reply [Paper 15] 8–15; Ex. 1003 ¶¶ 78–93.

FWD, 69.

The Petition specifically relied on Paatela’s memory 716 in the Figure 7 embodiment in showing the obviousness of limitation [13.3]. Paper 2, 39–41. The Reply’s discussion of Paatela’s dual-port, quad-port, and multi-port memory disclosures pertains to the same memory 716 discussed in the Petition. Ex.1007, [0078]; Paper 15, 8–13; *see also* FWD, 68–69. And the Reply’s discussion of Nelson’s dual-port RAM and Cornett’s network processor likewise pertains to the same disclosures the Petition cited from those references. FWD, 68–69; *compare* Paper 15, 8–12, *with* Paper 2, 38–43. This is precisely the circumstance addressed by *Axonics*, and the Board was correct (both procedurally and on the merits) in considering the Reply argument.

A. Patent Owner’s Attempts to Distinguish *Axonics* Are Unpersuasive.

Patent Owner contends that it did not “spring a new construction” in the Response but merely asked the Board to apply “the ‘plain language interpretation’ of the claim.” Request, 7. In fact, the Patent Owner Response argued that “the phrase ‘concurrently writing...’ **should be construed....**” Paper 12, 10 (emphasis added). But whether characterized as a “construction” or an “interpretation,” there is no ambiguity that the meaning of “concurrently writing” was first introduced as an issue in this proceeding by Patent Owner in the Response. Patent Owner argued for adding the parenthetical “(each concurrently with each other)” to clarify the scope of the claims. Paper 12, 8. Under 37 C.F.R. § 42.23(b) and *Axonics*, that argument triggered Petitioner’s right to respond.

B. Patent Owner’s Reliance on *Revvo* Is Misplaced.

Patent Owner invokes *Revvo Technologies, Inc. v. Cerebrum Sensor Technologies, Inc.*, IPR2025-00632, Paper 20 (Nov. 3, 2025) (precedential), for the proposition that Petitioner was obligated to explain why it took allegedly “contradictory” positions before the Board and the district court. Request, 8–9. *Revvo* does not apply here because Petitioner has maintained a consistent claim-construction position before both the Board and the district court, and there is no unexplained divergence in how Petitioner has applied that construction. There

is nothing to explain.¹

Patent Owner contends that Petitioner took “contradictory” positions by relying in the Petition on Nelson’s disclosure of writing a single header to a frame FIFO and a header FIFO “in parallel” (Pet., 42), while arguing in the district court that the claims require more than writing a single header concurrently to two memories (Ex. 2004, 6–8). Request, 9. These positions are not contradictory. The Petition relied on Nelson to address the aspect of “concurrently writing” that requires simultaneous writing of each header to both the packet buffer memory and the respective protocol stack layer memory—i.e., Parts (1) and (2) of the limitation occurring in parallel. Pet., 41–43; Ex. 1006, 7:1–4. The district court construction subsequently clarified that the limitation additionally requires the individual headers to be written “each concurrently with each other” to their respective protocol stack layer memories. Petitioner advocated for that construction (Ex.

¹ In contrast, Patent Owner has shifted positions during these proceedings. Patent Owner initially argued that the “concurrently writing” limitation “only requires concurrently writing a single header to the packet buffer memory and a single respective protocol stack layer memory.” Ex.2004, 6. Patent Owner subsequently agreed with Petitioner’s district court proposal, then advocated for its adoption by the Board. Ex.2002, 8.

2004, 1, 6–7), the district court adopted it (Ex. 2002, 8), and when Patent Owner proposed it in the Response, Petitioner expressly agreed (Paper 15, 7–8). The Board then adopted it. FWD, 17–20. That Petitioner addressed this clarification of claim scope in its Reply—relying on Paatela’s multi-port memory disclosures already cited in the Petition—is not an inconsistency but a direct response to a newly articulated claim scope requirement, as *Axonics* contemplates. Patent Owner’s citation of Petitioner’s April 2025 correspondence characterizing the construction as favorable to noninfringement (Ex. 2003) underscores rather than undermines this consistency: Petitioner advocated for the same construction in both forums and addressed its implications for the prior art in the Reply. Far from the kind of forum manipulation that *Revvo* addresses, this case presents the opposite: Petitioner has taken the same position everywhere.

Patent Owner also invokes 37 C.F.R. § 42.104(b)(3)–(4) for the proposition that the Petition must identify how claims are to be construed. But the Petition presented its analysis under the plain and ordinary meaning of the claims (Paper 2, 13), which is the default construction standard. The Federal Circuit has squarely held that a petitioner is not required “to describe all possible or reasonable claim constructions and to present invalidity theories under those constructions.” *Axonics*, 75 F.4th at 1380–81. Declining to propose an express construction in the Petition is not the same as adopting a different construction. It is simply declining

to construe—something the Federal Circuit has confirmed is entirely proper. *Id.*

Nor is there any inconsistency in how Petitioner mapped the prior art to the claim limitation across the Petition and Reply. In the Petition, Petitioner relied on Nelson for teaching that packet headers are written to both a frame FIFO (whole packet) and a header FIFO (header only) “in parallel,” addressing the aspect of “concurrently writing” that requires simultaneous writing of each header to both the packet buffer memory and the respective protocol stack layer memory. Paper 2, 41–43; Ex. 1006, 7:1–4. When Patent Owner’s Response raised the additional requirement—that the individual headers also be written “each concurrently with each other” to their respective protocol stack layer memories—Petitioner addressed that additional requirement in its Reply, relying on additional disclosures from the same Paatela embodiment already cited in the Petition. Paper 15, 8–13; Paper 2, 38–41. This is a natural and proper progression of argument in response to a newly raised claim construction, not an inconsistency.

The Board also independently confirmed that Petitioner’s Reply arguments were proper under the standard in *Apple Inc. v. Andrea Electronics Corp.*, 949 F.3d 697, 706 (Fed. Cir. 2020). FWD, 68–70. The Board found that Petitioner’s Reply properly supplemented and expanded on disclosures already cited in the Petition. FWD, 68–69. Specifically, the Petition cited Nelson’s disclosure of using a dual-port memory to store header information, and Paatela’s disclosures about the

Figure 7 embodiment with memory 716. Paper 2, 38–44; Ex. 1007, ¶¶ 74–78; Ex. 1006, 7:1–4. The Reply cited additional disclosures from those same embodiments, pointedly noting that Paatela’s memory 716 is a dual-port, quad-port, or multi-port memory. Paper 15, 8–13; Ex. 1007, ¶ 78. Petitioner showed how the prior art embodiments already of record defeated Patent Owner’s argument; there was no impermissible new theory.

The Director’s well-founded concern about petitioners taking inconsistent positions in parallel proceedings is simply not implicated here. Petitioner advocated for the same construction in district court and before the Board, relied on the same prior art embodiments in the Petition and the Reply, and supplemented its analysis only in direct response to an express claim construction that Patent Owner raised for the first time in its Response. This is the ordinary course of events under *Axonics*, particularly where a petitioner files its IPR challenge quickly (and long before claim construction issues are developed in copending litigation). Patent Owner’s *Revvo* argument is unsupported by the record, which shows consistent advocacy and procedurally proper supplementation at every stage. Nor is there any tension between Petitioner’s position that the prior art satisfies the “concurrently writing” limitation and its district court position that the Accused Products do not. The prior art references at issue—Paatela, Nelson, and Cornett—disclose multi-port memory architectures expressly designed to support

simultaneous write operations to multiple memory destinations.

III. THE BOARD’S ANALYSIS IS SUPPORTED BY SUBSTANTIAL EVIDENCE.

A. Petitioner’s Argument Is One of Obviousness, Not Inherency.

Patent Owner’s second ground for Director Review contends that the Board erred in its analysis of the “concurrently writing” limitation because Petitioner’s argument is “substantively one of inherency” that fails to meet the heightened standard for inherent disclosure. Request, 10. The Board correctly rejected this characterization, and the Director should do the same. FWD, 78–79.

Petitioner’s argument is a classic obviousness theory. Paatela expressly discloses that memory 716 stores “headers of the various protocol layers associated with the incoming packet,” including a PPP header, an MPLS label stack, an IP header, and a TCP header in separate segments of memory 716. Ex.1007, [0077]. Paatela expressly discloses that memory 716 may be implemented as a dual-port memory, and that “two 32-bit words may be simultaneously written to the memory 716” when so implemented. Ex.1007, [0078]. Paatela further discloses that a quad-port memory or multi-port memory may be used as an alternative to produce “analogous results and provide similar advantages.” Ex.1007, [0078]. Given these express disclosures, Petitioner argued that it “would have been obvious” to an ordinarily skilled artisan for “the simultaneously written 32-bit words to represent multiple different protocol layer headers,” particularly where many protocol layer

headers are 32 bits or less, such as PPP headers (16 to 40 bits) and MPLS label stacks (32 bits or less). Paper 15, 11–12.

This is not a case where the petitioner conceded a gap in the prior art’s disclosure and then asked a skilled artisan to fill that gap through inherency. Petitioner does not argue that Paatela’s dual-port memory “always” writes two headers simultaneously or that all headers written are “necessarily” 32 bits or less. Rather, Petitioner argues that given Paatela’s express disclosure of (1) storing different protocol layer headers in memory 716, (2) using a dual-port memory for memory 716, (3) simultaneously writing two 32-bit words to that memory, and (4) handling protocols whose headers are 32 bits or less, it would have been *obvious*—not inherent—for the simultaneously written words to represent different protocol layer headers. Patent Owner emphasizes that the Petition acknowledged that the “Cornett-Paatela combination does not explicitly explain the timing of how ... packet headers are written to ... respective, separate segments of memory.” Pet., 42. But this acknowledgment is precisely why the Petition relied on Nelson for the timing aspect of the limitation, and why the Reply addressed the additional “each concurrently with each other” requirement by pointing to Paatela’s express disclosure of multi-port memory that performs simultaneous writes. Paper 2, 26, 29-32, 42-44; Paper 15, 12-13. There is no gap in disclosure filled by inference; there is a combination of express teachings.

B. The Board Distinguished *LBT*.

Patent Owner relies heavily on *LBT IP I LLC v. Apple Inc.*, 2023 WL 3914920 (Fed. Cir. June 9, 2023), but the Board correctly found that the circumstances in *LBT* “differ materially from the circumstances here.” FWD, 79. In *LBT*, the challenged claim included an activation/reactivation limitation, and Apple conceded that the Sakamoto reference did not expressly disclose that limitation. Apple’s argument rested on a skilled artisan’s understanding that the system would “necessarily” perform the undisclosed function under certain operational conditions—but the evidence did not establish that those conditions necessarily occurred. *LBT*, 2023 WL 3914920 at *3.

Here, by contrast, Paatela expressly discloses every aspect of the claimed “concurrently writing” limitation: (1) storing headers of various protocol layers in separate segments of memory 716; (2) using a dual-port, quad-port, or multi-port memory as memory 716; and (3) simultaneously writing two or more 32-bit words to memory 716. Ex.1007, [0077]-[0079]. The Board further found that Patent Owner “does not identify a limitation missing from the references like the activation/reactivation limitation in *LBT*.” FWD, 80. Unlike in *LBT*, where the prior art simply did not disclose the claimed functionality, here the prior art expressly discloses each component, and Petitioner argues that it would have been *obvious* to combine them to simultaneously write multiple headers. This is standard

obviousness analysis, not inherency. *See* Ex. 3002 (Petitioner’s authorized statement regarding *LBT*); *see also* Ex. 1027, 62:17–23 (Patent Owner’s expert acknowledging that he did not consider the prior art *in combination*).

Moreover, as the Board noted, prior art that “sometimes meet[s] the claim elements” suffices “to show obviousness.” *Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1002 (Fed. Cir. 2016) (holding that prior art satisfying claim elements under some but not all operating conditions suffices for obviousness). That some headers may exceed 32 bits does not defeat obviousness, because the independent claims do not require that *all possible* headers be concurrently written—only that “each individual one of said plurality of headers” is so written. As Petitioner demonstrated (and Patent Owner acknowledged), the protocol headers discussed in Paatela—such as PPP and MPLS—are 32 bits or less and thus fit within the dual-port memory’s simultaneous write capability. FWD, 58–60, 88. The Board therefore correctly rejected Patent Owner’s attempt to analogize this case to *LBT* and properly upheld Petitioner’s obviousness theory.

C. The Board’s Analysis of Dependent Claims 2, 5, 14, and 17 Is Correct.

Patent Owner also challenges the Board’s analysis of dependent claims 2, 5, 14, and 17, arguing that headers exceeding 32 bits (e.g., Ethernet headers at 112 bits, IPv4 headers at 160 bits, or IPv6 headers at 320 bits) could not be simultaneously written using a dual-port or quad-port memory. The Board properly

rejected this argument.

As to claims 2 and 14 (requiring a “media access control layer protocol header”) and claims 5 and 17 (requiring a “network layer protocol header”), the Board correctly found that Paatela discloses using a multi-port memory to store headers of the various protocol layers. FWD, 87–89. The Board concluded that “[a] multi-port memory with a sufficient number of ports supports simultaneously writing an Ethernet header and another header” and similarly supports simultaneously writing an IPv4 or IPv6 header and another header. FWD, 89. This finding is grounded in Paatela’s express disclosure that a “multi-port memory” may be used as an alternative to a dual-port or quad-port memory to produce “analogous results and provide similar advantages.” Ex.1007, ¶78.

Patent Owner’s criticism that the Board cited no evidence for what constitutes a “multi-port memory with a sufficient number of ports” is inconsistent with the record. Paatela itself discloses that multi-port memory is an alternative that provides “similar advantages” to a dual-port memory, including the ability to perform simultaneous write operations. And the Board cited Ex.1037, a 2007 patent application publication, explaining the use of quad-port RAM providing “independent, simultaneous access for read/write from/to any location” within a storage array. Patent Owner offers only unsubstantiated attorney argument to dispute that a multi-port memory with additional ports (beyond four) would

support simultaneously writing correspondingly wider data, including larger headers. The Board’s analysis follows directly from the prior art and is within the understanding of an ordinarily skilled artisan.

D. Petitioner’s Reply Was Supported by Evidence, Not Merely Attorney Argument.

Patent Owner claims that Petitioner’s Reply “relied exclusively on attorney argument.” Request, 5; *see also* Paper 18, *passim*. The Board correctly found this characterization meritless. FWD, 77–78. The Reply cited disclosures in Cornett, Paatela, and Nelson, portions of Dr. Mir’s declaration testimony, portions of Patent Owner’s own expert Mr. Brooks’s testimony, and Exhibits 1028 through 1037. FWD, 77–78. These exhibits were not new prior art used to teach a claim limitation. The evidence was properly relied upon to explain the meaning of the disclosures in Cornett, Paatela, and Nelson, such as explaining that PPP and MPLS headers (discussed in Paatela) are 32 bits or less. FWD, 75–76; Paper 15, 11–12. The Federal Circuit has affirmed the use of such references in this way. *See Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337–38 (Fed. Cir. 2020); *Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1365 (Fed. Cir. 2015).

Furthermore, no rule requires “an expert guiding the Board as to how it should read prior art.” *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1079 (Fed. Cir. 2015). FWD, 78. The Board may “independently assess the strength of a petitioner’s argument and evidence.” *Fanduel, Inc. v. Interactive Games LLC*, 966

F.3d 1334, 1344 (Fed. Cir. 2020). Patent Owner’s assertion of “attorney argument” thus presents no basis for Director review, as the Board’s treatment of the Reply and the cited evidence aligns squarely with established precedent.

IV. CONCLUSION

For the foregoing reasons, Petitioner respectfully requests that the Director deny Patent Owner’s Request for Director Review. The Board’s Final Written Decision is well-reasoned, supported by substantial evidence, and consistent with governing precedent. No error warranting Director intervention occurred.

Respectfully submitted,

Dated: April 13, 2026
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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), the undersigned certifies that a true and correct copy of the foregoing was served on the Patent Owner as detailed below:

<i>Date of service</i>	April 13, 2026
<i>Manner of service</i>	Electronic Email: bcooper@bc-lawgroup.com; slindner@bc-lawgroup.com; robert@auchterlaw.com; Lionra_Counsel@b-clg.com
<i>Documents served</i>	Authorized Response to Director Review Request
<i>Persons Served</i>	Brett Cooper Seth Lindner BC Law Group, P.C. 200 Madison Avenue, 24th Floor New York, NY 10016 Robert A. Auchter Auchter PLLC 1629 K Street, NW, Suite 300 Washington, DC 20006

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