



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application:

Application No.:

Filed:

Title:

Commissioner for patents
Washington, D.C. 20231POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST
(REVOCATION OF PRIOR POWERS)

As assignee of record of each of the patent applications listed in the table of Exhibit A. (and all issued patents listed in the table of Exhibit B),

REVOCATION OF PRIOR POWERS OF ATTORNEY

all powers of attorney previously given in each of the patent applications listed in Exhibit A, and all of the issued patents listed in Exhibit B, are hereby revoked, and

NEW POWER OF ATTORNEY

the attorneys of Thomas, Kayden, Horstemeyer & Risley, LLP, who are listed under the USPTO Customer Number shown below are appointed as the attorneys to prosecute these applications and to transact all business in the United States Patent and Trademark Office connected therewith, recognizing that the specific attorneys listed under that Customer Number may be changed from time to time at the sole discretion of Thomas, Kayden, Horstemeyer & Risley, LLP, and request that all correspondence be addressed to the address filed under the same USPTO Customer Number.

24504

Please direct all correspondence and telephone calls to:

Daniel R. McClure, Reg. No. 38,962
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.
100 Galleria Parkway, Suite 1750
Atlanta, Georgia 30339
770-933-9500

LOCATION:

RX TIME 01/07 '05 03:38

ASSIGNEE OF ENTIRE INTEREST

AU OPTRONICS CORP.
No. 1, Li-Hsin Rd. 2,
Science-Based Industrial Park
Hsinchu 300, Taiwan, R.O.C.

ASSIGNEE CERTIFICATION

The certification under 37 C.F.R. §3.73(b) establishing the right of assignee to take action is attached hereto along with documentation evidencing same. Further, in my official position with AU Optronics Corp., I am authorized to sign documents and otherwise act on its behalf in connection with the management and handling of patent applications and other intellectual property matters.

Date:

12/20/2004



Name Fan LUO
Title V.P. of CTO

Exhibit A
AU Optronics Corp. Patent Applications
Subject to Revocation of Power of Attorney by Assignee

No.	Serial No.	Title	Filing Date	Assignment (Reel/Frame)
1	10/606,860	Power-Saving Circuits and Methods for Driving Active Matrix Display Elements	6/27/03	014253/0773
2	10/727,616	Reflector of Backlight Assembly for Liquid Crystal Display Device	12/5/03	014767/0553
3	10/785,100	Design Methodology of Power Supply Lines in Electroluminescence Display	2/25/04	015020/0318
4	10/747,407	Bendable Light Guide	12/30/03	014855/0158
5	10/785,099	Liquid Crystal Display Device Pixel and Drive Circuit	2/25/04	015020/0662
6	10/747,068	Low Power Driving in a Liquid Crystal Display	12/30/03	014855/0028
7	10/747,406	Mobile Unit with Style Panel Display	12/30/03	014855/0070
8	10/738,040	Dual Display Panel	12/18/03	014810/0353
9	10/865,940	Redundant Storage Capacitor and Method for Repairing OLED Pixels and Driving	6/14/04	015465/0439
10	11/005,648	Storage Capacitor in OLED Pixels and Driving Circuits and Method for Forming the Same	12/7/04	Assignment Provided
11	10/761,211	Analog Buffer for ITPS AMLCD	1/22/04	014914/0888
12	10/833,143	Current-Driven OLED Pixel	4/28/04	015275/0502
13	10/776,177	OLED Pixel	2/12/04	014982/0975
14	10/975,370	Integrated Circuit for Driving Liquid Crystal Display Device	10/29/04	Assignment Provided
15	10/865,941	Integrated Circuit for Liquid Crystal Display Device	6/14/04	015465/0552
16	10/857,860	Driving Method for Dual Panel Display	6/2/04	015426/0311
17	10/911,483	Dual Emitting Method and Device for Active Matrix Organic Electroluminescence	8/5/04	Assignment Provided

A-1

LOCATION:

RX TIME 01/07 '05 03:38



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Sun
Application Serial No.: 11/005,648
Filed: December 7, 2004
For: Storage Capacitor in OLED Pixels and Driving Circuits and Method for Forming the Same
Patent No.:
Issue Date:

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

**CERTIFICATE UNDER 37 C.F.R. §3.73(b)
ESTABLISHING RIGHT OF ASSIGNEE TO TAKE ACTION**

1. The assignee of the entire right, title and interest hereby seeks to take action in the PTO in this matter.

IDENTIFICATION OF ASSIGNEE

2. The assignee of this matter is:

**AU OPTRONICS CORPORATION
NO. 1, LI-HSIN RD. 2
SCIENCE-BSED INDUSTRIAL PARK
HSINCHU, TAIWAN R.O.C.**

PERSON AUTHORIZED TO SIGN

3. Daniel R. McClure
Attorney for Assignee

4. A chain of title from the inventor(s) to the current assignee is shown below:

- a. From:
To:
Recorded in PTO: Reel: Frame:
- b. From:
To:
Recorded in PTO: Reel: Frame:

Recorded in PTO: See Exhibit A evidencing assignment that
has already been filed. No Reel and Frame has been assigned as of yet.

DECLARATIONS

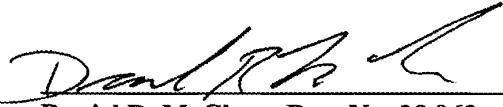
5. I, the undersigned, have reviewed all the documents in the chain of title of the

- ☒ application
☐ patent

matter identified above and, to the best of my knowledge and belief, title is in the assignee identified above.

6. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

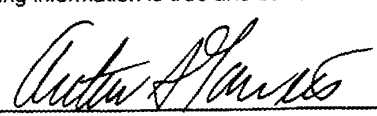
7. I, the person signing below, aver that I am empowered to sign this statement on behalf of the assignee.


Daniel R. McClure, Reg. No. 38,962

Tel. No. 770-933-9500
Customer No.: 24504

**THOMAS, KAYDEN, HORSTEMEYER
& RISLEY, L.L.P.**
100 Galleria Parkway, Suite 1750
Atlanta, Georgia 30339-5948

Docket No. 250142-1170

FORM PTO-1595 1-31-92		ASSIGNMENT RECORDATION FORM COVER SHEET PATENTS ONLY		U.S. Department of Commerce Patent and Trademark Office Attorney Docket No. 8970.0021 Attorney Customer Number: 22,852	
To the Director of the U.S. Patent and Trademark Office: Please record the attached original documents or copy thereof.				Mail Stop Assignment Recordation Services	
1. Name of conveying party(ies): Wein-Town Sun		2. Name and address of receiving party(ies): Name: AU Optronics Corporation			
Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No		Internal Address:			
3. Nature of conveyance:		Street Address: No. 1, Lising 2 nd Road Science-Based Industrial Park Hsinchu, Taiwan Republic of China			
☒ Assignment		☐ Merger		City:	
☐ Security Agreement		☐ Change of Name		State:	Zip Code:
☐ Other:		Additional name(s) & Address(es) attached? ☐ Yes ☒ No			
Execution Date: December 3, 2004					
4. Application number(s) or patent number(s): If this document is being filed together with a new application, the execution date of the application: December 3, 2004					
A. Patent Application Number(s):			B. Patent Number(s):		
Additional numbers attached?			☐ Yes ☒ No		
5. Name and address of party to whom correspondence concerning document should be mailed: Name: Richard V. Burgujian, Esq.			6. Total number of applications and registrations involved: One (1)		
Internal Address: FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.			7. Total fee (37 CFR 3.41): \$40		
Street Address: 1300 I Street, N.W.			☒ Enclosed (Please charge deficiency to deposit account)		
City: Washington, D.C.			☐ Authorized to be charged to deposit account		
State: Zip: 20005-3315			8. Deposit Account No.: 06-0916		
9. Statement and signature. To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.					
Richard V. Burgujian		 Signature		 Date	
Total number of pages including cover sheet, attachments and documents: Two (2)					

ASSIGNMENT

WHEREAS I/We, the below named inventors, [hereinafter referred to as Assignors], have made an invention entitled:

STORAGE CAPACITOR IN OLED PIXELS AND DRIVING CIRCUITS AND METHOD FOR FORMING THE SAME

for which I/We executed an application for United States Letters Patent concurrently herewith; and

WHEREAS, AU Optronics Corporation, a corporation of Hsinchu, Taiwan, R.O.C., whose post office address is No. 1, Lising 2nd Road, Science-Based Industrial Park, Hsinchu, Taiwan (hereinafter referred to as Assignee), is desirous of securing the entire right, title, and interest in and to this invention in all countries throughout the world, and in and to the application for United States Letters Patent on this invention and the Letters Patent to be issued upon this application;

NOW THEREFORE, be it known that, for good and valuable consideration the receipt of which from Assignee is hereby acknowledged, I/We, as Assignor(s), have sold, assigned, transferred, and set over, and do hereby sell, assign, transfer, and set over unto the Assignee, its lawful successors and assigns, my/our entire right, title, and interest in and to this invention, provisional Application No. [Text], filed [Date] (if any), and this application, and all divisions, and continuations thereof, and all Letters Patent of the United States which may be granted thereon, and all reissues thereof, and all rights to claim priority on the basis of the above provisional application (if any), as well as all rights to claim priority on the basis of this application, and all applications for Letters Patent which may hereafter be filed for this invention in any foreign country and all Letters Patent which may be granted on this invention in any foreign country, and all extensions, renewals, and reissues thereof; and I/We hereby authorize and request the Commissioner of Patents and Trademarks of the United States and any official of any foreign country whose duty it is to issue patents on applications as described above, to issue all Letters Patent for this invention to Assignee, its successors and assigns, in accordance with the terms of this Assignment;

AND, I/WE HEREBY covenant that I/We have the full right to convey the interest assigned by this Assignment, and I/We have not executed and will not execute any agreement in conflict with this Assignment;

AND, I/WE HEREBY further covenant and agree that I/We will, without further consideration, communicate with Assignee, its successors and assigns, any facts known to me/us respecting this invention, and testify in any legal proceeding, sign all lawful papers when called upon to do so, execute and deliver any and all papers that may be necessary or desirable to perfect the title to this invention in said Assignee, its successors or assigns, execute all divisional, continuation, and reissue applications, make all rightful oaths and generally do everything possible to aid Assignee, its successors and assigns, to obtain and enforce proper patent protection for this invention in the United States and any foreign country, it being understood that any expense incident to the execution of such papers shall be borne by the Assignee, its successors and assigns.

Wein-Town Sun

FULL NAME OF SOLE INVENTOR

Wein-Town Sun Dec 3, 2004

INVENTOR'S SIGNATURE

DATE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Sun

Serial No. Unassigned

Filing Date: February 22, 2011

Confirmation No.: Unassigned

Examiner: Unassigned

Docket No. 250142-1173

Group Art Unit: Unassigned

For: **Method for Forming a Pixel of an Electroluminescence Device hsing Storage Capacitors**

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

This information disclosure statement is filed in accordance with 37 C.F.R. §§ 1.56, 1.97, and 1.98. Listed on the accompanying form SB_08(a) are documents which may or may not be considered material to the examination of this application. These documents were made of record in a prior application filed December 28, 2006 and having serial no. 11/616,943, to which priority is claimed relative to the present application pursuant to 35 U.S.C. §120. Copies of these documents are not being provided pursuant to 37 C.F.R. § 1.98(d)(1) and (2), which provides:

(d) A copy of any patent, publication, pending U.S. application or other information, as specified in paragraph (a) of this section, listed in an information disclosure statement is required to be provided, even if the patent, publication, pending U.S. application or other information was previously submitted to, or cited by, the Office in an earlier application, unless:

(1) The application is properly identified in the information disclosure statement and is relied on for an earlier effective filing date under 35 U.S.C. §120; and

(2) The information disclosure statement submitted in the earlier application complies with a paragraphs (a) through (c) of this section.

The following rights are reserved by the Applicant(s): the right to establish the patentability of the claimed invention over any of the listed documents should they be applied as reference, the right to prove that some of these documents may not be prior art, and/or the right to prove that some of these documents may not be enabling for the teachings they purport to offer.

This statement should not be construed as a representation that an exhaustive search has been made, or that information more material to the examination of the present application does not exist. The Examiner is specifically requested not to rely solely on the materials submitted herewith. The Examiner is requested to conduct an independent and thorough review of the documents, and to form independent opinions as to their significance.

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449 to indicate the documents have been considered.

Respectfully submitted,

**THOMAS, KAYDEN, HORSTEMEYER
& RISLEY, L.L.P.**

By: /Daniel R. McClure/
Daniel R. McClure, Reg. No. 38,962

Customer No. 24504
Docket: 250142-1173

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		
	Filing Date		2011-02-22
	First Named Inventor	Sun	
	Art Unit		
	Examiner Name		
	Attorney Docket Number		250142-1173

U.S.PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
	1	5459596		1995-10-17	Ueda, et al.			
	2	6610997		2003-08-26	Murade			
If you wish to add additional U.S. Patent citation information please click the Add button.							Add	
U.S.PATENT APPLICATION PUBLICATIONS							Remove	
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
	1	20020104995		2002-08-08	Yamazaki			
	2	20030127652		2003-07-10	Park, et al.			
If you wish to add additional U.S. Published Application citation information please click the Add button.							Add	
FOREIGN PATENT DOCUMENTS							Remove	
Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		
	Filing Date		2011-02-22
	First Named Inventor	Sun	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	250142-1173	

If you wish to add additional Foreign Patent Document citation information please click the Add button				Add
NON-PATENT LITERATURE DOCUMENTS				Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.		T ⁵
	1			☐
If you wish to add additional non-patent literature document citation information please click the Add button				Add
EXAMINER SIGNATURE				
Examiner Signature				Date Considered
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.				
<small> ¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached. </small>				

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	2011-02-22
First Named Inventor	Sun
Art Unit	
Examiner Name	
Attorney Docket Number	250142-1173

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Daniel R. McClure/	Date (YYYY-MM-DD)	2011-02-22
Name/Print	Daniel R. McClure	Registration Number	38962

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Method for Forming a Pixel of an Electroluminescence Device having Storage Capacitors		
First Named Inventor/Applicant Name:		Wein-Town Sun		
Filer:		Daniel R. McClure/Brooke French		
Attorney Docket Number:		250142-1173		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Independent claims in excess of 3	1201	1	220	220
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1310

Electronic Acknowledgement Receipt	
EFS ID:	9488742
Application Number:	13031712
International Application Number:	
Confirmation Number:	5546
Title of Invention:	Method for Forming a Pixel of an Electroluminescence Device having Storage Capacitors
First Named Inventor/Applicant Name:	Wein-Town Sun
Customer Number:	24504
Filer:	Daniel R. McClure/Brooke French
Filer Authorized By:	Daniel R. McClure
Attorney Docket Number:	250142-1173
Receipt Date:	22-FEB-2011
Filing Date:	
Time Stamp:	11:22:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1310
RAM confirmation Number	12804
Deposit Account	200778
Authorized User	MCCLURE,DANIEL R.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	01310718.PDF	1276615	no	4
			d15356e36338ea53de8ada9ede4fbf72ee98171		
Warnings:					
Information:					
2		01310689.PDF	172068	yes	25
			357b6dddb6861338771c151e282fdba5c354a5be		
	Multipart Description/PDF files in .zip description				
	Document Description	Start	End		
	Specification	1	15		
	Claims	16	24		
	Abstract	25	25		
Warnings:					
Information:					
3	Drawings-only black and white line drawings	01310698.PDF	660342	no	11
			eb10ad9a1f2de634c554bed80dd16a94077214af		
Warnings:					
Information:					
4	Oath or Declaration filed	01310680.PDF	427395	no	1
			791a9bafd67e2d39b2c42c20bf0ff17f7083c17		
Warnings:					
Information:					
5		01310685.PDF	2228145	yes	7
			b38ab13bfdedebed7ddc63b643b0ba5ca474cae24		
	Multipart Description/PDF files in .zip description				
	Document Description	Start	End		
	Power of Attorney	1	3		
	Assignee showing of ownership per 37 CFR 3.73(b).	4	7		
Warnings:					
Information:					

6	Transmittal Letter	01311480.PDF	64308 93fae04cd5ac1ece548dd47730185d4f0458a502	no	2
Warnings:					
Information:					
7	Information Disclosure Statement (IDS) Filed (SB/08)	01310736.PDF	767188 7f9399b3444d577a996ab66da98c4392f168c33d	no	4
Warnings:					
Information:					
8	Fee Worksheet (PTO-875)	fee-info.pdf	36118 a559a50e32bb700a1be2aec99e559c42a6243eff	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			5632179		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	250142-1173
		Application Number	
Title of Invention	Method for Forming a Pixel of an Electroluminescence Device having Storage Capacitors		
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Applicant 1					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
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Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
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Application Information:

Title of the Invention	Method for Forming a Pixel of an Electroluminescence Device having Storage Capacitors		
Attorney Docket Number	250142-1173	Small Entity Status Claimed ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	11	Suggested Figure for Publication (if any)	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	250142-1173
		Application Number	
Title of Invention	Method for Forming a Pixel of an Electroluminescence Device having Storage Capacitors		

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Prior Application Status	Pending		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
	Division of	11616943	2006-12-28		
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11616943	Division of	11005648	2004-12-07	7586121	2009-09-08
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	250142-1173
		Application Number	
Title of Invention	Method for Forming a Pixel of an Electroluminescence Device having Storage Capacitors		

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Signature	/Daniel R. McClure/		Date (YYYY-MM-DD)	2011-02-22	
First Name	Daniel	Last Name	McClure	Registration Number	38962

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TITLE

METHOD FOR FORMING A PIXEL OF AN ELECTROLUMINESCENCE

DEVICE HAVING STORAGE CAPACITORS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a division of U.S. patent application serial number 11/616,943, filed December 28, 2006, which is a division of U.S. patent application serial number 11/005,648, filed December 07, 2004.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] This invention relates in general to an electroluminescence device and, more particularly, to a storage capacitor of an electroluminescence device and a method for forming the storage capacitor.

Description of the Related Art

[0003] An electroluminescence ("EL") device is a device which makes use of the phenomenon of electroluminescence to emit light. An EL device generally includes thin film transistors ("TFTs") and light-emitting diodes ("LEDs"). Each LED further includes a light-emitting layer. If the light-emitting layer contains organic light-emitting material, the device is referred to as an organic EL device. When a current passes between a cathode and an anode of the LED device, light is emitted from the light-emitting layer.

[0004] Generally, an active matrix organic light emitting diode ("OLED") device or a polymer light emitting diode ("PLED") device, either voltage-driven or current-driven, includes an array of pixels, where each pixel comprises a set of sub-pixels. Each sub-pixel further includes a switching transistor, a driving transistor and a storage capacitor. If charging conditions permit, it is desirable to design a storage capacitor with a large

capacitance in order to avoid an issue of gray scale fading due to crosstalk or feed-through effect. For bottom-emission pixels, a storage capacitor having a greater capacitance may disadvantageously result in a smaller aperture ratio. In OLED pixels, thin film transistors, scan lines, data lines and power lines included therein may further reduce the aspect ratio. It is thus desirable to have a storage capacitor that includes improved capacitance in a limited area.

BRIEF SUMMARY OF INVENTION

[0005] Consistent with embodiments of the present invention, there is provided a method for forming a pixel of an electroluminescence device that includes providing a substrate; defining at least a first area for capacitors and a second area for a transistor on the substrate; forming a first conductive layer over the first area; forming a first dielectric layer over the first conductive layer over the first area; forming a second conductive layer over the first dielectric layer over the first area; forming a second dielectric layer over the second conductive layer over the first area; forming a third conductive layer over the second dielectric layer over the first area; forming a layer of capping silicon nitride between the second dielectric layer and the third conductive layer over the first area; forming a semiconductor layer over the second area; forming a gate oxide layer over the second area; and forming a fourth conductive layer over the gate oxide layer over the second area; wherein the first conductive layer over the first area is connectable to a power supply voltage, and wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over the first area, and the semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor.

[0006] Consistent with embodiments of the present invention, there is also provided a method for forming a pixel of an electroluminescence device that includes providing a substrate; defining at least a first area for capacitors, a second area for a transistor on the substrate and a third area for an organic light-emitting diode (OLED) on the substrate; forming a first conductive layer over the first area; forming a first dielectric layer over the first conductive layer over the first area; forming a second conductive layer over the first dielectric layer over the first area; forming a second dielectric layer over the second conductive layer over the first area; forming a third conductive layer over the second dielectric layer over the first area; forming a semiconductor layer over the second area; forming a gate oxide layer over the second area; forming a fourth conductive layer over the gate oxide layer over the second area; forming the gate oxide over the first area; forming the first conductive layer over the gate oxide, wherein forming the first conductive layer and forming the fourth conductive layer comprise forming the first conductive layer and the fourth conductive layer using the same material, wherein forming the first dielectric layer comprises forming a layer of interlayer dielectric (ILD), and wherein forming the second dielectric layer comprises forming a layer of passivation silicon nitride; forming a fifth conductive layer over the third area; and forming an organic layer over the fifth conductive layer over the third area, wherein the third conductive layer is over the organic layer over the third area, and wherein the fifth conductive layer, the organic layer, and the third conductive layer over the third area collectively form the OLED, wherein the first conductive layer over the first area is connectable to a power supply voltage, and wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over the first area, and the

semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor, and wherein forming the second conductive layer and forming the fifth conductive layer comprise forming the second conductive layer and the fifth conductive layer using the same material..

[0007] Consistent with embodiments of the present invention, there is also provided a method for forming a pixel of an electroluminescence device that includes providing a substrate; defining at least a first area for capacitors, a second area for a transistor on the substrate and a third area for an organic light-emitting diode (OLED) on the substrate; forming a first conductive layer over the first area; forming a first dielectric layer over the first conductive layer over the first area; forming a second conductive layer over the first dielectric layer over the first area; forming a second dielectric layer over the second conductive layer over the first area; forming a third conductive layer over the second dielectric layer over the first area; forming a layer of capping silicon nitride between the second dielectric layer and the third conductive layer over the first area; forming a semiconductor layer over the second area; forming a gate oxide layer over the first area and the second area, wherein the first conductive layer is both over the gate oxide over the first area and over the second area, the first conductive layer providing contact to the semiconductor layer over the second area; forming a fourth conductive layer over the gate oxide layer over the second area; forming a fifth conductive layer over the third area; and forming an organic layer over the fifth conductive layer over the third area, wherein the third conductive layer over the organic layer over the third area, wherein the first conductive layer over the first area is connectable to a power supply voltage, and wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first

area collectively form a second one of the capacitors over the first area, and the semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor, and wherein forming the first dielectric layer comprises forming a layer of passivation silicon nitride, forming the second conductive layer and forming the fifth conductive layer comprise forming the second conductive layer and the fifth conductive layer using the same material, and forming the second dielectric layer comprises forming a layer of capping silicon nitride, and wherein the fifth conductive layer, the organic layer, and the third conductive layer over the third area collectively form the OLED..

[0008] Consistent with embodiments of the present invention, there is also provided a method for forming a pixel of an electroluminescence device that includes providing a substrate; defining at least a first area for capacitors, a second area for a transistor on the substrate and a third area for an organic light-emitting diode (OLED) on the substrate; forming a first conductive layer over the first area; forming a first dielectric layer over the first conductive layer over the first area; forming a second conductive layer over the first dielectric layer over the first area; forming a second dielectric layer over the second conductive layer over the first area; forming a third conductive layer over the second dielectric layer over the first area; forming a semiconductor layer over the second area; forming a gate oxide layer over the second area and over the first conductive layer over the first area, wherein forming the first dielectric layer comprises forming an interlayer dielectric over the gate oxide; and forming a fourth conductive layer over the gate oxide layer over the second area; forming a fifth conductive layer over the third area; forming an organic layer over the fifth conductive layer over the third area, wherein forming the second dielectric layer comprises forming the organic layer over the second conductive layer, wherein the third conductive layer is over the organic layer over the third area; wherein the

first conductive layer over the first area is connectable to a power supply voltage, and wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over the first area, and the semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor, and wherein forming the first conductive layer and forming the semiconductor layer comprise forming the first conductive layer and the semiconductor layer using the same semiconductor material which is provided as doped polysilicon, and wherein the fifth conductive layer, the organic layer, and the third conductive layer over the third area collectively form the OLED.

[0009] Additional features and advantages of the invention will be set forth in part in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The features and advantages of the invention will be realized and attained by means of the elements and combinations particularly pointed out in the appended claims.

[0010] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed

BRIEF DESCRIPTION OF DRAWINGS

The invention can be more fully understood by reading the subsequent detailed description and examples with references made to the accompanying drawings, wherein:

FIG. 1 is a circuit diagram of a pixel of an electroluminescence device consistent with embodiments of the present invention;

FIG. 2 is a cross-sectional view of a part of the pixel of FIG. 1 and consistent with a

first embodiment of the present invention;

FIG. 3 is a circuit diagram of a pixel of an electroluminescence device consistent with a second embodiment of the present invention;

FIG. 4 is a circuit diagram of a pixel of an electroluminescence device consistent with a third embodiment of the present invention;

FIG. 5 is a circuit diagram of a pixel of an electroluminescence device consistent with a fourth embodiment of the present invention;

FIG. 6 is a circuit diagram of a pixel of an electroluminescence device consistent with a fifth embodiment of the present invention;

FIG. 7 is a circuit diagram of a pixel of an electroluminescence device consistent with a sixth embodiment of the present invention;

FIG. 8 is a circuit diagram of a pixel of an electroluminescence device consistent with a seventh embodiment of the present invention;

FIG. 9 is a circuit diagram of a pixel of an electroluminescence device consistent with an eighth embodiment of the present invention;

FIG. 10 is a circuit diagram of a pixel of an electroluminescence device consistent with embodiments of the present invention; and

FIG. 11 is a circuit diagram of the pixel of FIG. 10, further showing a cross-sectional view of a part of the pixel and consistent with embodiments of the present invention.

DETAILED DESCRIPTION OF INVENTION

[0011] Reference will now be made in detail to embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0012] An electroluminescence (EL) device may include an array of pixels formed on a

substrate such as glass and FIG. 1 shows a circuit diagram of an exemplary pixel 100 consistent with embodiments of the present invention. Pixel 100 includes three MOS transistors 102, 104, and 106, a capacitor 108, and an OLED 110. In one aspect, transistor 102 is a p-type MOS transistor and transistors 104 and 106 are n-type MOS transistors. Each of transistors 102, 104, and 106 has a gate (not numbered), a source (not numbered), and a drain (not numbered). It is to be understood that an MOS structure is generally symmetrical and therefore the source and drain of the MOS transistors in the descriptions herein and in the following may be interchanged without affecting the functions thereof or the scope of the present invention.

[0013] The gate of transistor 102 is coupled to the source of transistor 106. The source of transistor 102 is coupled to a power supply voltage V_{DD} . The drain of transistor 102 is coupled to drive OLED 110. The gates of both transistors 104 and 106 are coupled to a scan line, the drain of transistor 106 is coupled to the source of transistor 104, and the drain of transistor 104 is coupled to a data line to receive data. Capacitor 108 is coupled between the gate and source of transistor 102. OLED 110 has an anode coupled to the drain of transistor 102 and a cathode coupled to a power supply voltage V_{SS} . In one aspect, V_{SS} is ground. In operation, capacitor 108 holds a charge when transistors 104 and 106 are turned off, to maintain a voltage between the gate and source of transistor 102 for driving OLED 110.

[0014] Pixel 100 further includes a capacitor 112 coupled between the gate of transistor 102 and the cathode of OLED 110. Thus, both capacitors 108 and 112 store charge when transistors 104 and 106 are turned off, to maintain the gate voltage of transistor 102. In this sense, capacitors 108 and 112 are coupled to each other in parallel and may be collectively viewed as a storage capacitor of pixel 100 whose capacitance is equal to the sum of the capacitances of both capacitors 108 and 112.

[0015] In one aspect, capacitor 112 is physically formed over the same area of a

substrate where capacitor 108 is formed. Therefore, the storage capacitance of pixel 100 is increased without a chip area thereof being increased. In another aspect, capacitor 112 is formed at the same time OLED 110 and other parts of pixel 100 are formed, without requiring additional masks.

[0016] FIG. 2 shows a cross-sectional view of part of pixel 100 consistent with a first embodiment of the present invention. Only a portion of OLED 110, a portion of transistor 102, and capacitors 108 and 112 are shown. To simplify illustration, transistors 104 and 106 are not shown in FIG. 2.

[0017] Referring to FIG. 2, pixel 100 is formed on a glass substrate 200. Capacitors 108 and 112 are shown to be formed over an area A of substrate 200, transistor 102 is shown to be formed over an area B of substrate 200, and part of OLED 110 is shown to be formed in an area C of substrate 200.

[0018] Referring to FIG. 2, a layer of polysilicon is doped and patterned to form a doped polysilicon 202B and intrinsic polysilicon 202 over area B of substrate 200. A layer of gate oxide 204 is formed over all of areas A, B, and C. A layer of first metal is deposited over gate oxide 204 and patterned to form first metal patterns 206A and 206B over areas A and B, respectively. A layer of interlayer dielectric (ILD) 208 is formed over first metal patterns 206A and 206B. A layer of second metal is deposited over ILD 208 and patterned to form second metal patterns 210A over area A and 210B over both areas B and C, wherein second metal pattern 210B contacts polysilicon pattern 202B through a via hole (not numbered) in ILD 208 and gate oxide 204. A layer of passivation silicon nitride (SiN) 212 is formed over ILD 208 and second metal patterns 210A and 210B. A layer of indium tin oxide (ITO) is formed over passivation SiN 212 and patterned to form an ITO pattern 214C over area C of substrate 200, wherein ITO pattern 214C contacts second metal pattern 210B through a via hole (not numbered) in passivation SiN 212. A layer of capping SiN

216 is deposited to cover passivation SiN 212 and ITO pattern 214C. A layer of organics 218 is deposited over all of areas A, B, and C. Over area A, capping SiN 216 is also patterned to expose a portion of passivation SiN 212. Thus, organic 218 is also formed on passivation SiN 212 over area A. A layer of third metal 220 is formed over organic 218.

[0019] Over area A, first metal pattern 206A, ILD 208, and second metal pattern 210A collectively form capacitor 108; and second metal pattern 210A, passivation SiN 212, organic 218, and third metal 220 collectively form capacitor 112(更正). Over area B, polysilicon pattern 202B provides the source and drain of transistor 102 and first metal pattern 206B serves as the gate of transistor 102. Over area C, ITO pattern 214C, capping SiN 216, organic 218, and third metal 220 collectively form part of OLED 110. Also, first metal pattern 206A is coupled to power supply voltage V_{DD} , second metal pattern 210A is coupled to the gate of transistor 102, i.e., first metal pattern 206B, and third metal 220 is coupled to V_{SS} .

[0020] As shown in FIG. 2, capacitors 108 and 112 are formed over the same area (area A) of substrate 200. Therefore, the storage capacitance of pixel 100 is increased without increasing the area of the storage capacitor and, consequently, without decreasing an aperture ratio. Also, one skilled in the art should now appreciate that no additional masks are required to form capacitors 108 and 112. For example, first metal pattern 206A may be formed using an existing mask that is required for forming first metal pattern 206B and second metal pattern 210A may be formed using an existing mask that is required for forming second metal pattern 210B.

[0021] In FIG. 2, ITO pattern 214C is formed over second metal pattern 210B. However, the layer of ITO may also be deposited and patterned prior to the deposition of the second metal and the formation of second metal patterns 210A and 210B. Similarly, passivation SiN 212 may also be deposited prior to the deposition of the second metal and

the formation of second metal patterns 210A and 210B.

[0022] It is to be understood that the configuration of pixel 100 as shown in FIGS. 1 and 2 is exemplary only. The present invention may be applied to any suitable EL device. For example, a pixel consistent with an aspect of the present invention may include a plurality of capacitors such as capacitors 108 and 112 formed over the same area of a substrate and one or more transistors, but may include no OLED.

[0023] Further, in FIG. 2, capacitor 108 comprises first metal pattern 206A, ILD 208, and second metal pattern 210A, and capacitor 112 comprises second metal pattern 210A, passivation SiN 212, organic 218, and third metal 220. However, it is to be understood that other layers of materials required for forming pixel 100 may also be used to form capacitors 108 and 112.

[0024] For example, consistent with a second embodiment of the present invention, organic 218 may be removed from area A, as shown in FIG. 3, which shows a circuit diagram of pixel 100 and a cross-sectional view of capacitors 108 and 112 consistent with the second embodiment of the present invention. Thus, capacitor 112 comprises second metal pattern 210A, passivation silicon nitride 212, and third metal 220, while capacitor 108 comprises first metal pattern 206A, ILD 208, and second metal pattern 210A. Also, first metal pattern 206A is coupled to power supply voltage V_{DD} , second metal pattern 210A is coupled to the gate of transistor 102, i.e., first metal pattern 206B, and third metal 220 is coupled to V_{SS} .

[0025] As shown in FIG. 4, which shows a circuit diagram of pixel 100 and a cross-sectional view of capacitors 108 and 112 consistent with a third embodiment of the present invention, both capping SiN 216 and organic 218 may be formed over area A and the layer of ITO may be patterned to form an ITO pattern 214A over area A, while first metal pattern 206A is not formed during the deposition and patterning of the layer of first metal. Thus,

capacitor 108 comprises second metal pattern 210A, passivation SiN 212, and ITO pattern 214A; and capacitor 112 comprises ITO pattern 214A, capping SiN 216, organic 218, and third metal 220. Also, second metal pattern 210A is coupled to power supply voltage V_{DD} , ITO pattern 214A is coupled to the gate of transistor 102, i.e., first metal pattern 206B, and third metal 220 is coupled to V_{SS} .

[0026] FIG. 5 shows a circuit diagram of pixel 100 and a cross-sectional view of capacitors 108 and 112 consistent with a fourth embodiment of the present invention. As shown in FIG. 5, capacitor 108 comprises second metal pattern 210A, passivation silicon nitride 212, and ITO pattern 214A; and capacitor 112 comprises ITO pattern 214A, capping SiN 216, and third metal layer 220. Also, second metal pattern 210A is coupled to power supply voltage V_{DD} , ITO pattern 214A is coupled to the gate of transistor 102, i.e., first metal pattern 206B, and third metal 220 is coupled to V_{SS} .

[0027] FIG. 6 shows a circuit diagram of pixel 100 and a cross-sectional view of capacitors 108 and 112 consistent with a fifth embodiment of the present invention, wherein the layer of ITO is deposited prior to the deposition of the layer of second metal. As shown in FIG. 6, capacitor 108 comprises first metal pattern 206A, ILD 208, and ITO pattern 214A; and capacitor 112 comprises ITO pattern 214A, passivation silicon nitride 212, capping silicon nitride 216, organic 218, and third metal layer 220. Also, first metal pattern 206A is coupled to power supply voltage V_{DD} , ITO pattern 214A is coupled to the gate of transistor 102, i.e., first metal pattern 206B, and third metal 220 is coupled to V_{SS} .

[0028] FIG. 7 shows a circuit diagram of pixel 100 and a cross-sectional view of capacitors 108 and 112 consistent with a sixth embodiment of the present invention, wherein the layer of ITO is deposited prior to the deposition of the layer of second metal. As shown in FIG. 7, capacitor 108 comprises first metal 206A, ILD 208, and ITO pattern 214A; and capacitor 112 comprises ITO pattern 214A, passivation silicon nitride 212,

capping silicon nitride 216, and third metal layer 220. Also, first metal pattern 206A is coupled to power supply voltage V_{DD} , ITO pattern 214A is coupled to the gate of transistor 102, i.e., first metal pattern 206B, and third metal 220 is coupled to V_{SS} .

[0029] FIG. 8 shows a circuit diagram of pixel 100 and a cross-sectional view of capacitors 108 and 112 consistent with a seventh embodiment of the present invention. As shown in FIG. 8, the layer of doped polysilicon is also patterned to form a polysilicon pattern 202A over area A of substrate 200. Thus, capacitor 108 comprises polysilicon pattern 202A, oxide 204, ILD 208, and ITO pattern 214A; and capacitor 112 comprises ITO pattern 214A, capping silicon nitride 216, organic 218, and third metal layer 220. Also, polysilicon pattern 202A is coupled to power supply voltage V_{DD} , ITO pattern 214A is coupled to the gate of transistor 102, i.e., first metal pattern 206B, and third metal 220 is coupled to V_{SS} .

[0030] Further, FIG. 9 shows a circuit diagram of pixel 100 and a cross-sectional view of capacitors 108 and 112 consistent with an eighth embodiment of the present invention. As shown in FIG. 9, capacitor 108 comprises doped polysilicon pattern 202A, oxide 204, ILD 208, and second metal pattern 210A; and capacitor 112 comprises second metal pattern 210A, passivation silicon nitride 212, organic 218, and third metal layer 220. Polysilicon pattern 202A is coupled to power supply voltage V_{DD} , second metal pattern 210A is coupled to the gate of transistor 102, i.e., first metal pattern 206B, and third metal 220 is coupled to V_{SS} .

[0031] In FIGS. 3-9, both the cross-sectional views of capacitors 108 and 112 and the circuit diagram of pixel 100 are shown and only the structures of capacitors 108 and 112 are discussed in the above. The rest of the circuit of pixel 100 was previously described with reference to FIG. 1 and is not further described herein.

[0032] Also consistent with embodiments of the present invention, more than two

capacitors may be formed over the same area (area A) of substrate 200 and connected in parallel with one another. An example of four capacitors is shown in FIGS. 10 and 11, wherein FIG. 10 is a circuit schematic of pixel 100 with four capacitors and FIG. 11 further shows a cross-sectional view of those four capacitors formed over area A of substrate 200. As shown in FIG. 10, in addition to capacitors 108 and 112, two more capacitors 114 and 116 are also coupled between the gate and source of transistor 102. The rest of the circuit diagram is the same as that shown in FIG. 1 and therefore is not further described here. Thus, a storage capacitance of pixel 100 is equal to the sum of capacitors 108, 112, 114, and 116. Referring to FIG. 11, capacitor 108 comprises a doped polysilicon pattern 202A, oxide 204, and first metal pattern 206A; capacitor 114 comprises first metal pattern 206A, ILD 208, and ITO pattern 214A; capacitor 116 comprises ITO pattern 214A, passivation silicon nitride 212, and second metal pattern 210A; and capacitor 112 comprises second metal pattern 210A, capping silicon nitride layer 216, organic 218, and third metal layer 220. Polysilicon pattern 202A and ITO pattern 214A are coupled to V_{DD} , first metal pattern 206A and second metal pattern 210A are coupled to the gate of transistor 102, i.e., first metal pattern 206B, and third metal 220 is coupled to V_{SS} .

[0033] One skilled in the art should appreciate that the formation of capacitors 108, 112, 114, and 116 does not require more masks in addition to those already existing for the formation of pixel 100. For example, doped polysilicon pattern 202A may be formed at the same time doped polysilicon pattern 202B is formed, first metal pattern 206A may be formed at the same time first metal pattern 206B is formed, and ITO pattern 214A may be formed at the same time ITO pattern 214C is formed. Additionally, since all of capacitors 108, 112, 114, and 116 are formed over area A of substrate 200, the area of the storage capacitor of pixel 100 is not increased and, therefore, an aperture ratio is not decreased, while the storage capacitance is significantly increased.

[0034] Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

[0035] While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

What is claimed is:

- 1 1. A method for forming a pixel of an electroluminescence device, comprising:
 - 2 providing a substrate;
 - 3 defining at least a first area for capacitors and a second area for a transistor on
 - 4 the substrate;
 - 5 forming a first conductive layer over the first area;
 - 6 forming a first dielectric layer over the first conductive layer over the first
 - 7 area;
 - 8 forming a second conductive layer over the first dielectric layer over the first
 - 9 area;
 - 10 forming a second dielectric layer over the second conductive layer over the
 - 11 first area;
 - 12 forming a third conductive layer over the second dielectric layer over the first
 - 13 area;
 - 14 forming a layer of capping silicon nitride between the second dielectric layer
 - 15 and the third conductive layer over the first area;
 - 16 forming a semiconductor layer over the second area;
 - 17 forming a gate oxide layer over the second area; and
 - 18 forming a fourth conductive layer over the gate oxide layer over the second
 - 19 area;
 - 20 wherein the first conductive layer over the first area is connectable to a power
 - 21 supply voltage, and wherein the first conductive layer, the first dielectric layer, and

22 the second conductive layer over the first area collectively form a first one of the
23 capacitors over the first area, the second conductive layer, the second dielectric layer,
24 and the third conductive layer over the first area collectively form a second one of the
25 capacitors over the first area, and the semiconductor layer, the gate oxide layer, and
26 the fourth conductive layer over the second area collectively form a transistor.

1 2. The method of claim 1, further comprising:

2 forming the gate oxide over the first area;

3 forming the first conductive layer over the gate oxide, wherein forming the
4 first conductive layer and forming the fourth conductive layer comprise forming the
5 first conductive layer and the fourth conductive layer using the same material,
6 wherein forming the first dielectric layer comprises forming a layer of interlayer
7 dielectric (ILD), and wherein forming the second dielectric layer comprises forming a
8 layer of passivation silicon nitride;

9 defining a third area for an organic light-emitting diode (OLED) on the
10 substrate;

11 forming a fifth conductive layer over the third area;

12 forming an organic layer over the fifth conductive layer over the third area,
13 wherein the organic layer is between the layer of capping silicon nitride and the third
14 conductive layer over the first area; and

15 forming the third conductive layer over the organic layer over the third area,
16 wherein the fifth conductive layer, the organic layer, and the third conductive layer
17 over the third area collectively form the OLED.

1 3. A method for forming a pixel of an electroluminescence device, comprising:

2 providing a substrate;

3 defining at least a first area for capacitors, a second area for a transistor on the
4 substrate and a third area for an organic light-emitting diode (OLED) on the substrate;

5 forming a first conductive layer over the first area;

6 forming a first dielectric layer over the first conductive layer over the first
7 area;

8 forming a second conductive layer over the first dielectric layer over the first
9 area;

10 forming a second dielectric layer over the second conductive layer over the
11 first area;

12 forming a third conductive layer over the second dielectric layer over the first
13 area;

14 forming a semiconductor layer over the second area;

15 forming a gate oxide layer over the second area;

16 forming a fourth conductive layer over the gate oxide layer over the second
17 area;

18 forming the gate oxide over the first area;

19 forming the first conductive layer over the gate oxide, wherein forming the
20 first conductive layer and forming the fourth conductive layer comprise forming the
21 first conductive layer and the fourth conductive layer using the same material,
22 wherein forming the first dielectric layer comprises forming a layer of interlayer
23 dielectric (ILD), and wherein forming the second dielectric layer comprises forming a
24 layer of passivation silicon nitride;

25 forming a fifth conductive layer over the third area; and

26 forming an organic layer over the fifth conductive layer over the third area,
27 wherein the third conductive layer is over the organic layer over the third area, and
28 wherein the fifth conductive layer, the organic layer, and the third conductive layer
29 over the third area collectively form the OLED,

30 wherein the first conductive layer over the first area is connectable to a power
31 supply voltage, and wherein the first conductive layer, the first dielectric layer, and
32 the second conductive layer over the first area collectively form a first one of the
33 capacitors over the first area, the second conductive layer, the second dielectric layer,
34 and the third conductive layer over the first area collectively form a second one of the
35 capacitors over the first area, and the semiconductor layer, the gate oxide layer, and
36 the fourth conductive layer over the second area collectively form a transistor, and

37 wherein forming the second conductive layer and forming the fifth conductive
38 layer comprise forming the second conductive layer and the fifth conductive layer
39 using the same material.

1 4. A method for forming a pixel of an electroluminescence device, comprising:

2 providing a substrate;

3 defining at least a first area for capacitors, a second area for a transistor on the
4 substrate and a third area for an organic light-emitting diode (OLED) on the substrate;

5 forming a first conductive layer over the first area;

6 forming a first dielectric layer over the first conductive layer over the first
7 area;

8 forming a second conductive layer over the first dielectric layer over the first
9 area;

10 forming a second dielectric layer over the second conductive layer over the
11 first area;

12 forming a third conductive layer over the second dielectric layer over the first
13 area;

14 forming a layer of capping silicon nitride between the second dielectric layer
15 and the third conductive layer over the first area;

16 forming a semiconductor layer over the second area;

17 forming a gate oxide layer over the first area and the second area, wherein the
18 first conductive layer is both over the gate oxide over the first area and over the
19 second area, the first conductive layer providing contact to the semiconductor layer
20 over the second area;

21 forming a fourth conductive layer over the gate oxide layer over the second
22 area;

23 forming a fifth conductive layer over the third area; and

24 forming an organic layer over the fifth conductive layer over the third area,
25 wherein the third conductive layer over the organic layer over the third area,

26 wherein the first conductive layer over the first area is connectable to a power
27 supply voltage, and wherein the first conductive layer, the first dielectric layer, and
28 the second conductive layer over the first area collectively form a first one of the
29 capacitors over the first area, the second conductive layer, the second dielectric layer,
30 and the third conductive layer over the first area collectively form a second one of the
31 capacitors over the first area, and the semiconductor layer, the gate oxide layer, and
32 the fourth conductive layer over the second area collectively form a transistor, and

33 wherein forming the first dielectric layer comprises forming a layer of
34 passivation silicon nitride, forming the second conductive layer and forming the fifth
35 conductive layer comprise forming the second conductive layer and the fifth
36 conductive layer using the same material, and forming the second dielectric layer
37 comprises forming a layer of capping silicon nitride, and wherein the fifth conductive

38 layer, the organic layer, and the third conductive layer over the third area collectively
39 form the OLED.

1 5. The method of claim 4, further comprising forming an interlayer dielectric
2 layer over the gate oxide layer over the first area and forming the first conductive
3 layer over the third dielectric layer.

1 6. The method of claim 4, further comprising forming the organic layer
2 between the second dielectric and the third conductive layer over the first area.

1 7. A method for forming a pixel of an electroluminescence device, comprising:

2 providing a substrate;

3 defining at least a first area for capacitors, a second area for a transistor on the
4 substrate and a third area for an organic light-emitting diode (OLED) on the substrate;

5 forming a first conductive layer over the first area;

6 forming a first dielectric layer over the first conductive layer over the first
7 area;

8 forming a second conductive layer over the first dielectric layer over the first
9 area;

10 forming a second dielectric layer over the second conductive layer over the
11 first area;

12 forming a third conductive layer over the second dielectric layer over the first
13 area;

14 forming a semiconductor layer over the second area;

15 forming a gate oxide layer over the second area and over the first conductive
16 layer over the first area, wherein forming the first dielectric layer comprises forming
17 an interlayer dielectric over the gate oxide; and

18 forming a fourth conductive layer over the gate oxide layer over the second
19 area;

20 forming a fifth conductive layer over the third area;

21 forming an organic layer over the fifth conductive layer over the third area,
22 wherein forming the second dielectric layer comprises forming the organic layer over
23 the second conductive layer, wherein the third conductive layer is over the organic
24 layer over the third area;

25 wherein the first conductive layer over the first area is connectable to a power
26 supply voltage, and wherein the first conductive layer, the first dielectric layer, and
27 the second conductive layer over the first area collectively form a first one of the
28 capacitors over the first area, the second conductive layer, the second dielectric layer,
29 and the third conductive layer over the first area collectively form a second one of the
30 capacitors over the first area, and the semiconductor layer, the gate oxide layer, and
31 the fourth conductive layer over the second area collectively form a transistor, and

32 wherein forming the first conductive layer and forming the semiconductor
33 layer comprise forming the first conductive layer and the semiconductor layer using
34 the same semiconductor material which is provided as doped polysilicon, and wherein
35 the fifth conductive layer, the organic layer, and the third conductive layer over the
36 third area collectively form the OLED.

1 8. The method of claim 7, further comprising forming the second conductive
2 layer over the second area for providing contact to the semiconductor layer.

1 9. The method of claim 7, wherein forming the second conductive layer and
2 forming the fifth conductive layer comprise forming the second conductive layer and
3 the fifth conductive layer using the same material.

1 10. The method of claim 7, further comprising forming a third dielectric layer
2 between the second conductive layer and the second dielectric layer, wherein the third
3 dielectric layer comprises passivation silicon nitride or capping silicon nitride.

1 11. The method of claim 7, wherein forming the fifth conductive layer
2 comprises forming a layer of indium tin oxide (ITO).

ABSTRACT OF THE DISCLOSURE

[0036] A method for forming a pixel of an electroluminescence device includes providing a substrate; defining at least a first area for capacitors and a second area for a transistor on the substrate; forming a first conductive layer over the first area; forming a first dielectric layer over the first conductive layer; forming a second conductive layer over the first dielectric layer; forming a second dielectric layer over the second conductive layer; forming a third conductive layer over the second dielectric layer; forming a layer of capping silicon nitride between the second dielectric layer and the third conductive layer; forming a semiconductor layer over the second area; forming a gate oxide layer over the second area; and forming a fourth conductive layer over the gate oxide layer.

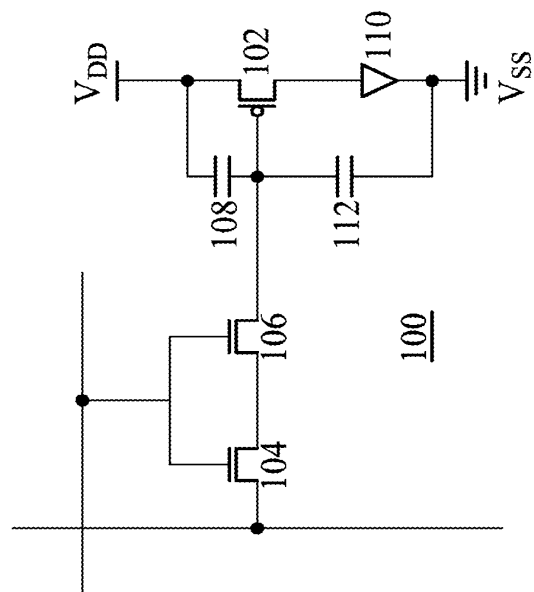


FIG. 1

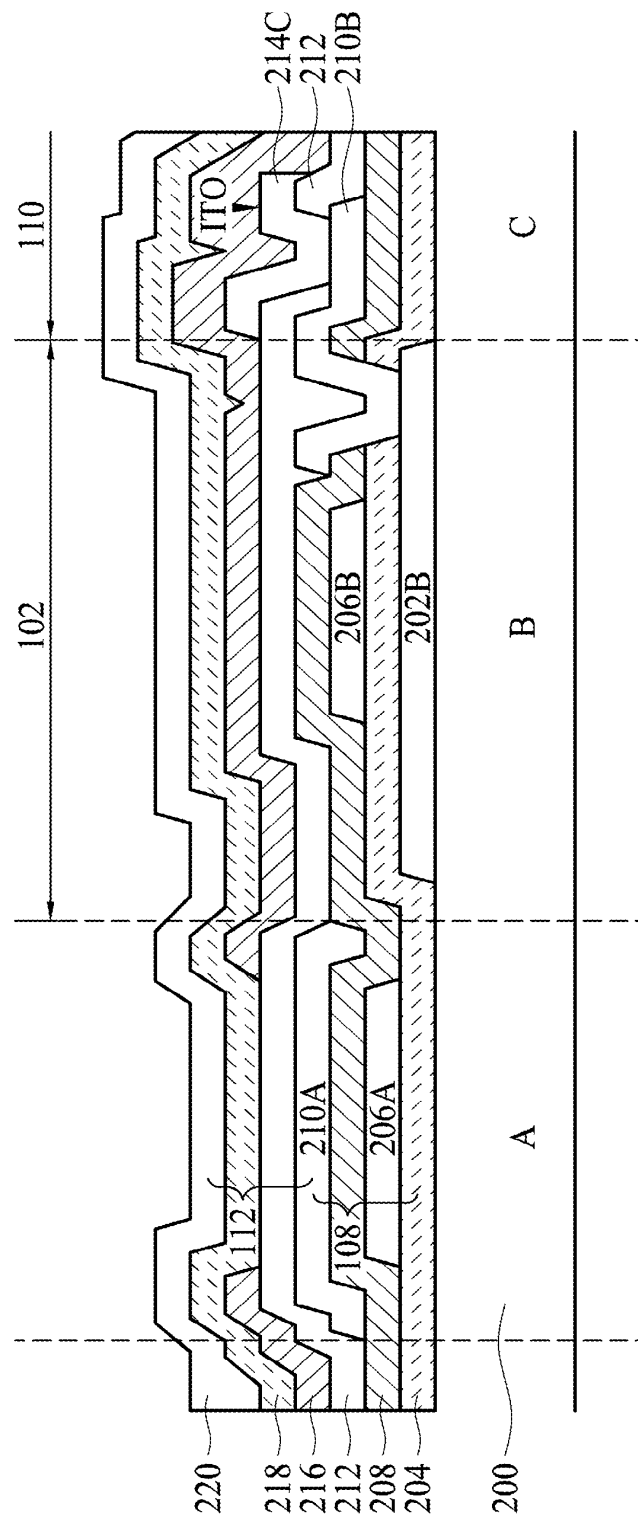


FIG. 2

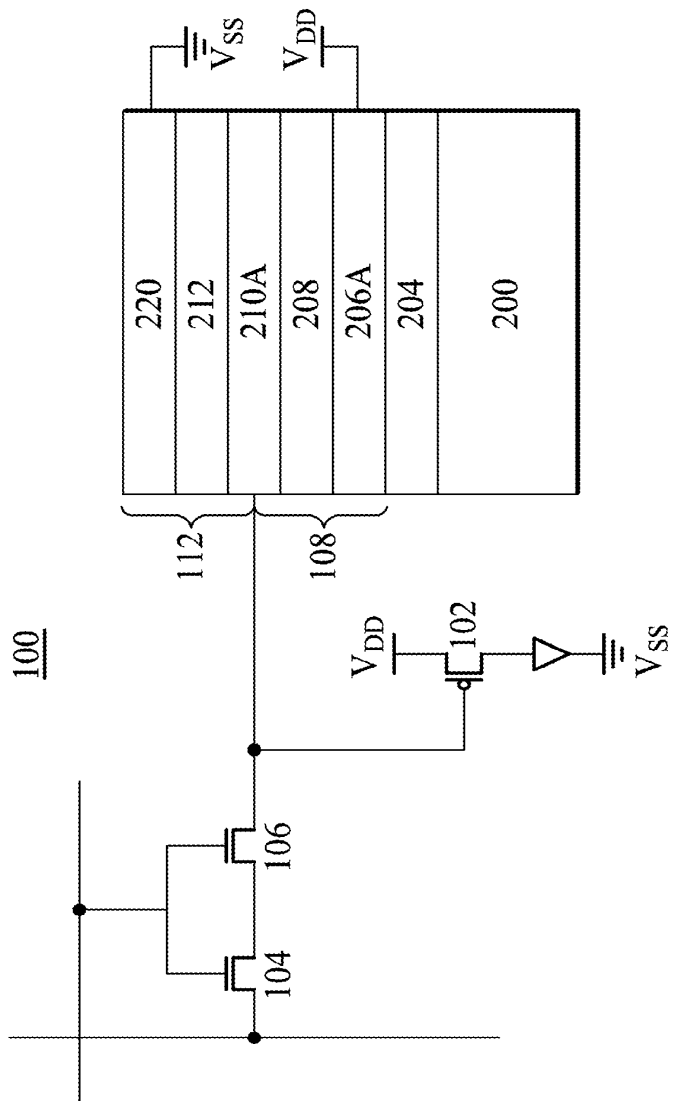


FIG. 3

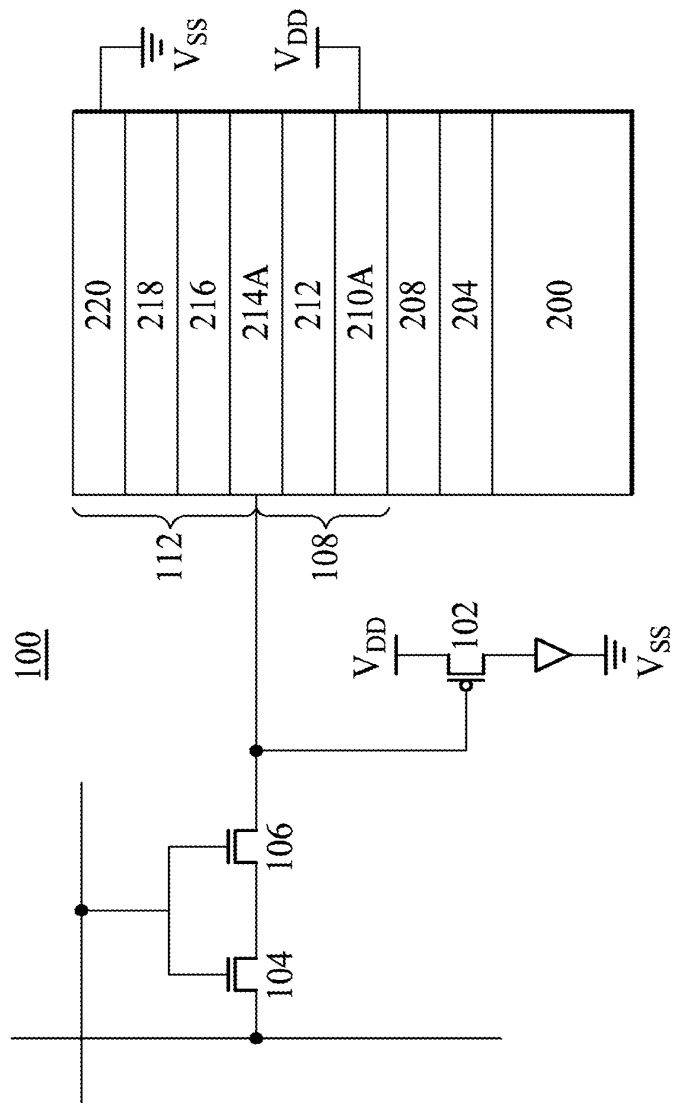


FIG. 4

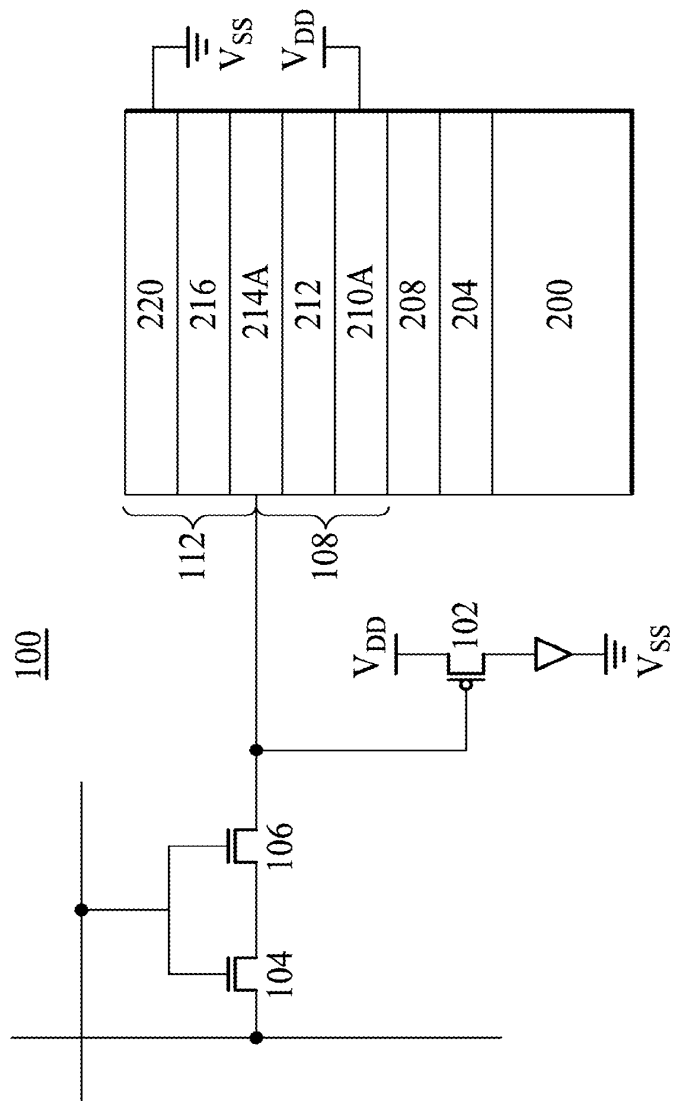


FIG. 5

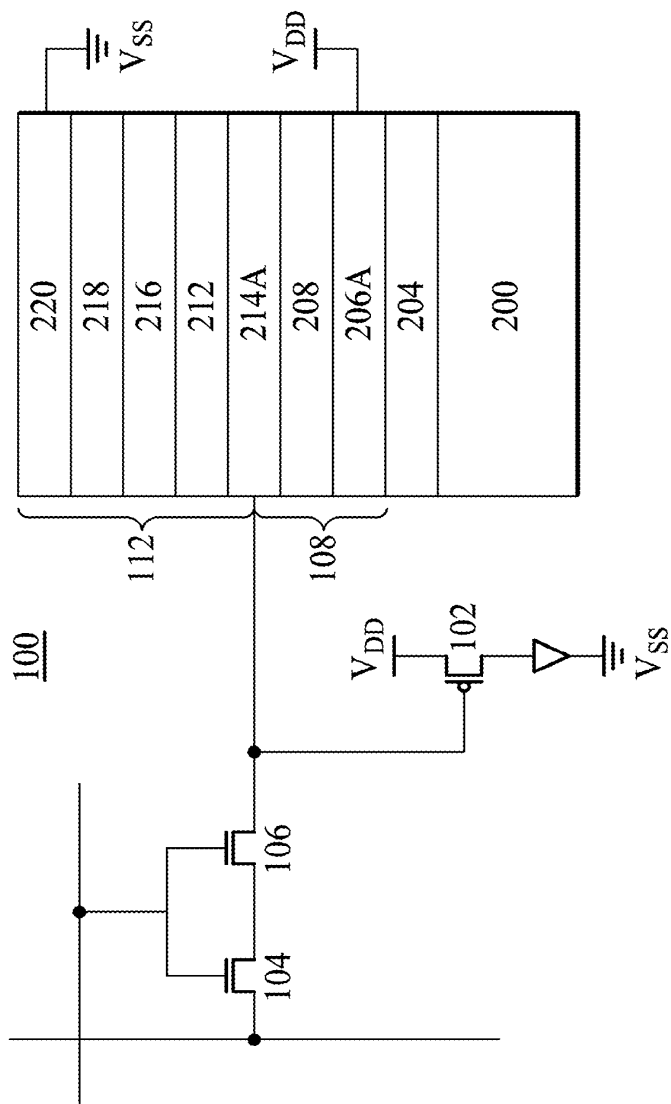


FIG. 6

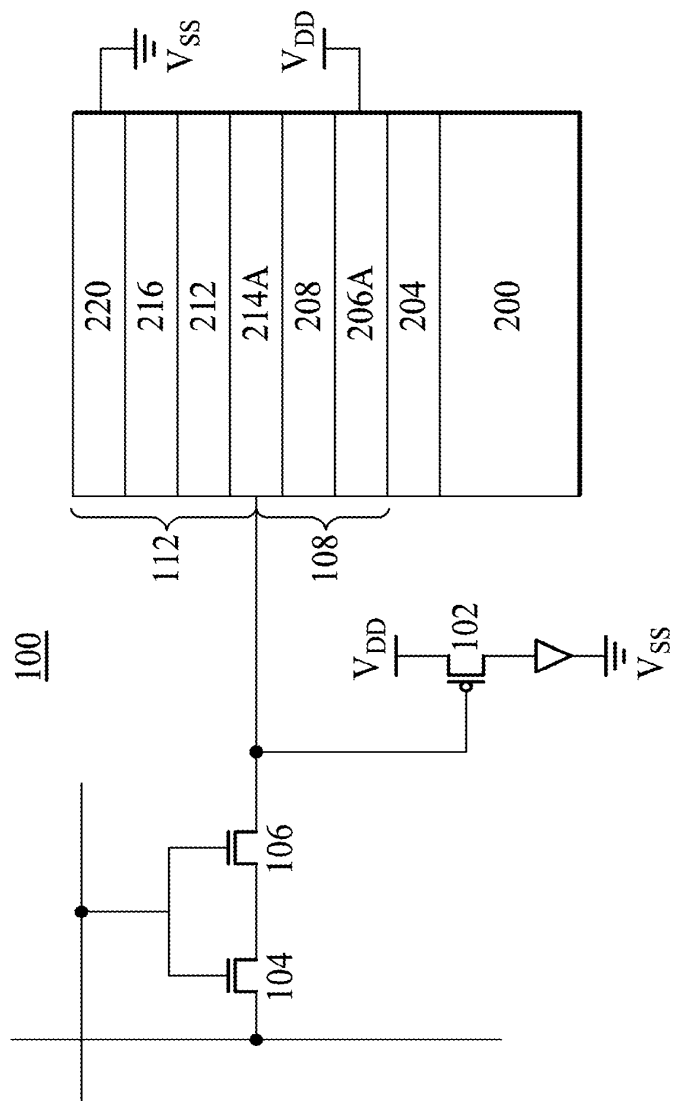


FIG. 7

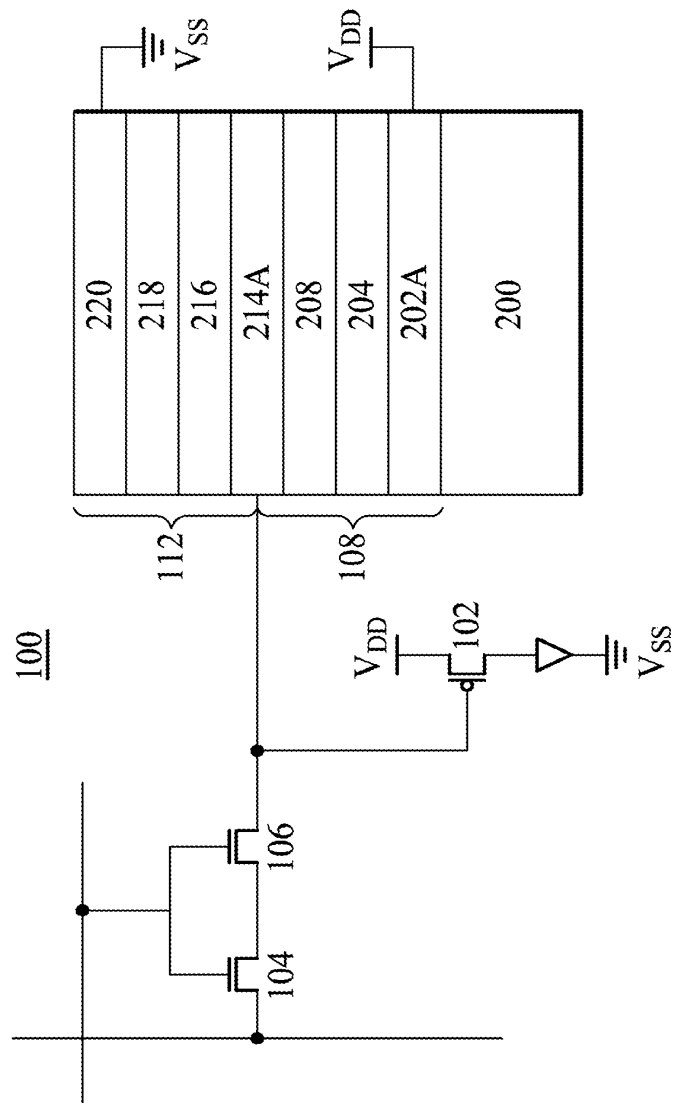


FIG. 8

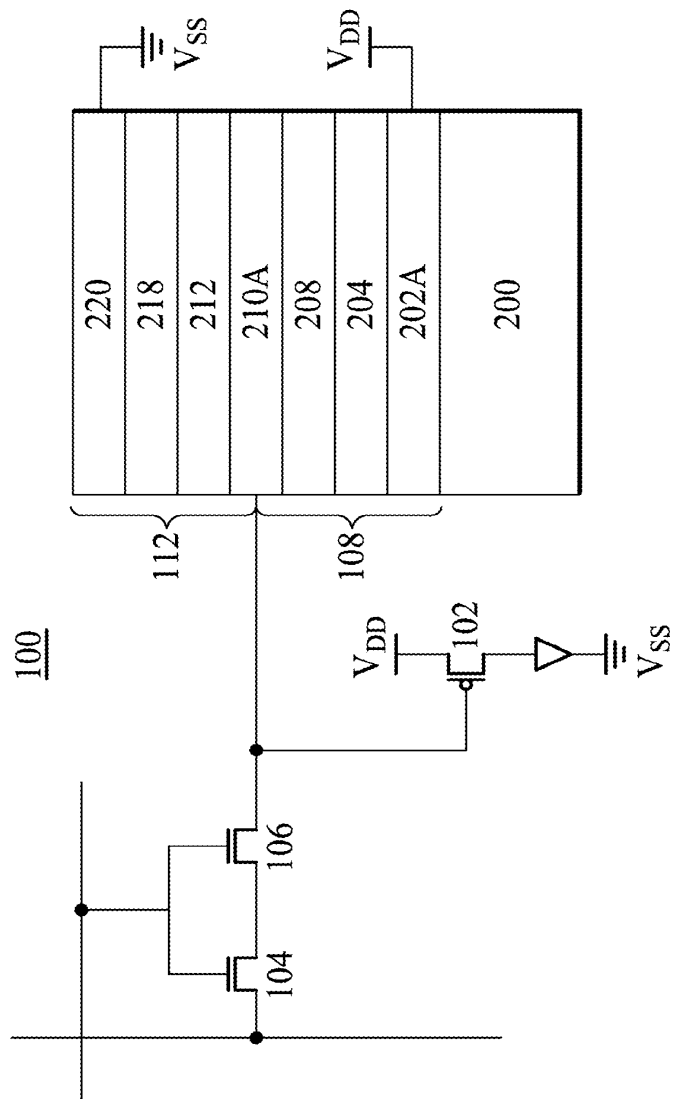


FIG. 9

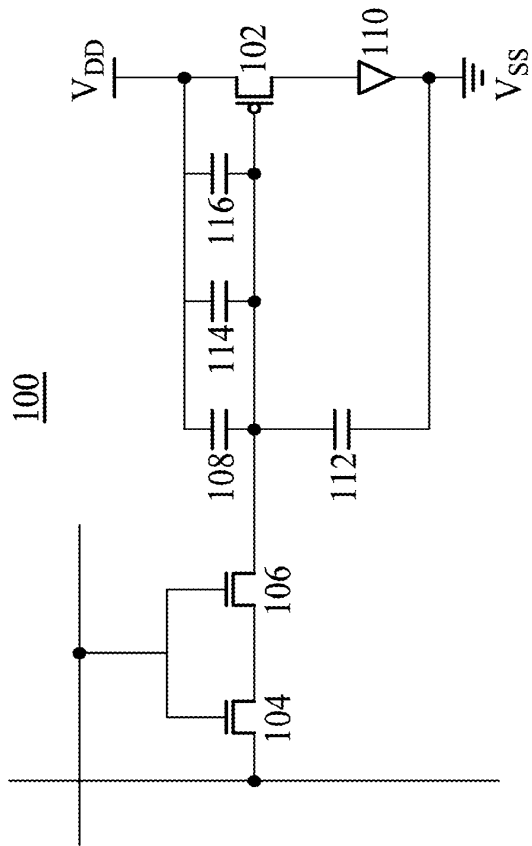


FIG. 10

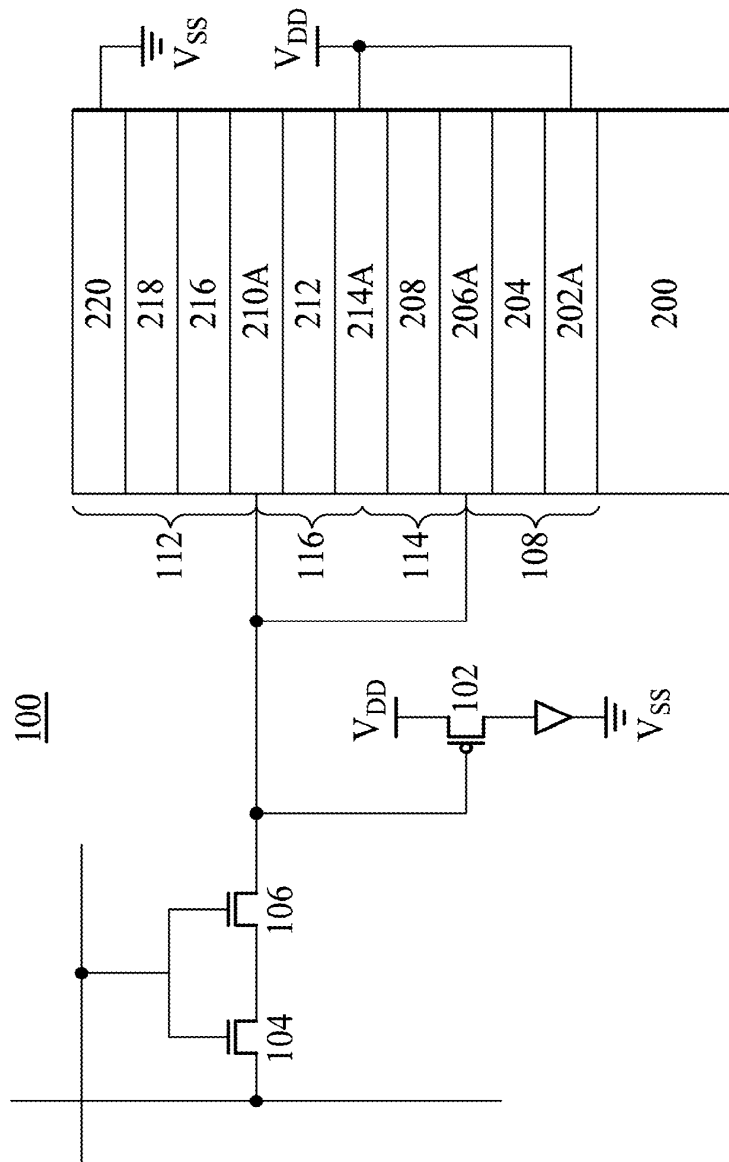


FIG. 11

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: STORAGE CAPACITOR IN OLED PIXELS AND DRIVING CIRCUITS AND METHOD FOR FORMING THE SAME, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT International application(s) designating at least one country other than the United States, listed below and have also identified below, any foreign application(s) for patent or inventor's certificate, or any PCT International application(s) having a filing date before that of the application(s) of which priority is claimed:

Country	Application Number	Date of Filing	Priority Claimed Under 35 U.S.C. 119
			☐ YES ☐ NO
			☐ YES ☐ NO

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

Application Number	Date of Filing

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) or § 365(c) of any PCT International application(s) designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application(s) in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application(s) and the national or PCT International filing date of this application:

Application Number	Date of Filing	Status (Patented, Pending, Abandoned)

I hereby appoint the following attorney and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. **FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P., CUSTOMER NUMBER 22,852.**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Full Name of First Inventor Wein-Town Sun	Inventor's Signature <i>Wein-Town Sun</i>	Date Dec 3, 2004
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Post Office Address c/o AU Optronics Corporation No. 1, Lising 2 nd Road, Science-Based Industrial Park, Hsinchu, Taiwan, R.O.C.		

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/031,712					
APPLICATION AS FILED - PART I											
		(Column 1)	(Column 2)		SMALL ENTITY		OR	OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA		RATE(\$)	FEE(\$)			RATE(\$)	FEE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A				N/A	330		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A		N/A				N/A	540		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A				N/A	220		
TOTAL CLAIMS (37 CFR 1.16(j))	11	minus 20 =	*			OR		x 52 =	0.00		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4	minus 3 =	*	1				x 220 =	220		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								0.00		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									0.00		
				TOTAL				TOTAL	1310		
* If the difference in column 1 is less than zero, enter "0" in column 2.											
APPLICATION AS AMENDED - PART II											
		(Column 1)	(Column 2)		(Column 3)		SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE(\$)	ADDITIONAL FEE(\$)				RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(j))	*	Minus	**	=			OR		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=			OR		x	=
	Application Size Fee (37 CFR 1.16(s))							OR			
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
					TOTAL ADD'L FEE			OR		TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.											
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".											
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
13/031,712	02/22/2011	1788	1310	250142-1173	11	4

CONFIRMATION NO. 5546

FILING RECEIPT



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Date Mailed: 03/04/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Wein-Town Sun, Hsinchu, TAIWAN;

Assignment For Published Patent Application

AU OPTRONICS CORPORATION, Hsinchu, TAIWAN

Power of Attorney: The patent practitioners associated with Customer Number 24504

Domestic Priority data as claimed by applicant

This application is a DIV of 11/616,943 12/28/2006
which is a DIV of 11/005,648 12/07/2004 PAT 7,586,121

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

If Required, Foreign Filing License Granted: 03/03/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/031,712**

Projected Publication Date: 06/16/2011

Non-Publication Request: No

Early Publication Request: No

Title

Method for Forming a Pixel of an Electroluminescence Device having Storage Capacitors

Preliminary Class

428

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

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The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/031,712	02/22/2011	Wein-Town Sun	250142-1173

CONFIRMATION NO. 5546

POA ACCEPTANCE LETTER

24504
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
600 GALLERIA PARKWAY, S.E.
STE 1500
ATLANTA, GA 30339-5994



OC000000046339171

Date Mailed: 03/04/2011

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/22/2011.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/htran/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/031,712	02/22/2011	Wein-Town Sun	250142-1173	5546
24504 7590 05/26/2011 THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP 600 GALLERIA PARKWAY, S.E. STE 1500 ATLANTA, GA 30339-5994			EXAMINER MAI, ANH D	
			ART UNIT 2829	PAPER NUMBER
			NOTIFICATION DATE 05/26/2011	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspatents@tkhr.com
kristen.layton@tkhr.com
ozzie.liggins@tkhr.com

Office Action Summary	Application No.	Applicant(s)	
	13/031,712	SUN, WEIN-TOWN	
	Examiner	Art Unit	
	ANH MAI	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 22 February 2011.

2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☐ Claim(s) _____ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☒ Claim(s) 1-11 are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) ☐ Notice of Informal Patent Application
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____	6) ☐ Other: _____

DETAILED ACTION

1. This application contains claims directed to the following patentably distinct species as shown in Figs. 2, 3, 4, 5, 6, 7, 8, 9, 10 and 11, respectively. The species are independent or distinct because the relative positions of each layer are different from one another. In addition, these species are not obvious variants of each other based on the current record.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species, or a single grouping of patentably indistinct species, for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, there is no generic.

There is a search and/or examination burden for the patentably distinct species as set forth above because at least the following reason(s) apply:

- *the species or groupings of patentably indistinct species have acquired a separate status in the art in view of their different classification*
- *the species or groupings of patentably indistinct species have acquired a separate status in the art due to their recognized divergent subject matter*
- *the species or groupings of patentably indistinct species require a different field of search (e.g., searching different classes /subclasses or electronic resources, or employing different search strategies or search queries).*

Applicant is advised that the reply to this requirement to be complete must include

(i) an election of a species or a grouping of patentably indistinct species to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected species or grouping of patentably indistinct species,** including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out

supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species or grouping of patentably indistinct species.

Should applicant traverse on the ground that the species, or groupings of patentably indistinct species from which election is required, are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing them to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANH MAI whose telephone number is (571)272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Anh D. Mai/
Primary Examiner, Art Unit 2829

<i>Index of Claims</i> 	Application/Control No. 13031712	Applicant(s)/Patent Under Reexamination SUN, WEIN-TOWN
	Examiner ANH MAI	Art Unit 2829

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant										☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM			DATE												
Final	Original	05/20/2011													
	1	÷													
	2	÷													
	3	÷													
	4	÷													
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	9	÷													
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	11	÷													



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/031,712	02/22/2011	Wein-Town Sun	250142-1173

CONFIRMATION NO. 5546

24504

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
600 GALLERIA PARKWAY, S.E.
STE 1500
ATLANTA, GA 30339-5994

PUBLICATION NOTICE



OC000000048242682

Title:Method for Forming a Pixel of an Electroluminescence Device having Storage Capacitors

Publication No.US-2011-0143465-A1

Publication Date:06/16/2011

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of
Sun, Wein-Town

Serial Number: 13/031,712

Filed: February 22, 2011

Title: Method for Forming a Pixel of an
Electroluminescence Device Having
Storage Capacitors

Confirmation No. 5546

Examiner: Mai, Anh D.

Group Art Unit: 2829

TKHR Ref. 250142-1173

Top-Team Ref. 0632-A50404D2-US

RESPONSE TO OFFICE ACTION (ELECTION OF SPECIES)

Mail Stop – Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

The Office Action mailed on May 26, 2011 has been carefully considered. In response thereto, Applicants hereby submit the following amendments and remarks.

Amendments to the Claims:

This listing of claims will replace all prior version, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method for forming a pixel of an electroluminescence device, comprising:

providing a substrate;

defining at least a first area for capacitors and a second area for a transistor on the substrate;

forming a first conductive layer over the first area;

forming a first dielectric layer over the first conductive layer over the first area;

forming a second conductive layer over the first dielectric layer over the first area;

forming a second dielectric layer over the second conductive layer over the first area;

forming a third conductive layer over the second dielectric layer over the first area;

forming a layer of capping silicon nitride between the second dielectric layer and the third conductive layer over the first area;

forming a semiconductor layer over the second area;

forming a gate oxide layer over the second area; and

forming a fourth conductive layer over the gate oxide layer over the second area;

wherein the first conductive layer over the first area is connectable to a power supply voltage, and wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over the first area, and the semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor.

2. (Withdrawn) The method of claim 1, further comprising:

forming the gate oxide over the first area;

forming the first conductive layer over the gate oxide, wherein forming the first conductive layer and forming the fourth conductive layer comprise forming the first conductive layer and the fourth conductive layer using the same material, wherein forming the first dielectric layer comprises forming a layer of interlayer dielectric (ILD), and wherein forming the second dielectric layer comprises forming a layer of passivation silicon nitride;

defining a third area for an organic light-emitting diode (OLED) on the substrate;

forming a fifth conductive layer over the third area;

forming an organic layer over the fifth conductive layer over the third area, wherein the organic layer is between the layer of capping silicon nitride and the third conductive layer over the first area; and

forming the third conductive layer over the organic layer over the third area, wherein the fifth conductive layer, the organic layer, and the third conductive layer over the third area collectively form the OLED.

3. (Withdrawn) A method for forming a pixel of an electroluminescence device, comprising:

providing a substrate;

defining at least a first area for capacitors, a second area for a transistor on the substrate and a third area for an organic light-emitting diode (OLED) on the substrate;

forming a first conductive layer over the first area;

forming a first dielectric layer over the first conductive layer over the first area;

forming a second conductive layer over the first dielectric layer over the first area;

forming a second dielectric layer over the second conductive layer over the first area;

forming a third conductive layer over the second dielectric layer over the first area;

forming a semiconductor layer over the second area;

forming a gate oxide layer over the second area;

forming a fourth conductive layer over the gate oxide layer over the second area;

forming the gate oxide over the first area;

forming the first conductive layer over the gate oxide, wherein forming the first conductive layer and forming the fourth conductive layer comprise forming the first conductive layer and the fourth conductive layer using the same material, wherein

forming the first dielectric layer comprises forming a layer of interlayer dielectric (ILD), and wherein forming the second dielectric layer comprises forming a layer of passivation silicon nitride;

forming a fifth conductive layer over the third area; and

forming an organic layer over the fifth conductive layer over the third area, wherein the third conductive layer is over the organic layer over the third area, and wherein the fifth conductive layer, the organic layer, and the third conductive layer over the third area collectively form the OLED,

wherein the first conductive layer over the first area is connectable to a power supply voltage, and wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over the first area, and the semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor, and

wherein forming the second conductive layer and forming the fifth conductive layer comprise forming the second conductive layer and the fifth conductive layer using the same material.

4. (Withdrawn) A method for forming a pixel of an electroluminescence device, comprising:

providing a substrate;

defining at least a first area for capacitors, a second area for a transistor on the substrate and a third area for an organic light-emitting diode (OLED) on the substrate;

forming a first conductive layer over the first area;

forming a first dielectric layer over the first conductive layer over the first area;

forming a second conductive layer over the first dielectric layer over the first area;

forming a second dielectric layer over the second conductive layer over the first area;

forming a third conductive layer over the second dielectric layer over the first area;

forming a layer of capping silicon nitride between the second dielectric layer and the third conductive layer over the first area;

forming a semiconductor layer over the second area;

forming a gate oxide layer over the first area and the second area, wherein the first conductive layer is both over the gate oxide over the first area and over the second area, the first conductive layer providing contact to the semiconductor layer over the second area;

forming a fourth conductive layer over the gate oxide layer over the second area;

forming a fifth conductive layer over the third area; and

forming an organic layer over the fifth conductive layer over the third area, wherein the third conductive layer over the organic layer over the third area,

wherein the first conductive layer over the first area is connectable to a power supply voltage, and wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors

over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over the first area, and the semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor, and

wherein forming the first dielectric layer comprises forming a layer of passivation silicon nitride, forming the second conductive layer and forming the fifth conductive layer comprise forming the second conductive layer and the fifth conductive layer using the same material, and forming the second dielectric layer comprises forming a layer of capping silicon nitride, and wherein the fifth conductive layer, the organic layer, and the third conductive layer over the third area collectively form the OLED.

5. (Withdrawn) The method of claim 4, further comprising forming an interlayer dielectric layer over the gate oxide layer over the first area and forming the first conductive layer over the third dielectric layer.

6. (Withdrawn) The method of claim 4, further comprising forming the organic layer between the second dielectric and the third conductive layer over the first area.

7. (Original) A method for forming a pixel of an electroluminescence device, comprising:

providing a substrate;

defining at least a first area for capacitors, a second area for a transistor on the substrate and a third area for an organic light-emitting diode (OLED) on the substrate;

forming a first conductive layer over the first area;

forming a first dielectric layer over the first conductive layer over the first area;

forming a second conductive layer over the first dielectric layer over the first area;

forming a second dielectric layer over the second conductive layer over the first area;

forming a third conductive layer over the second dielectric layer over the first area;

forming a semiconductor layer over the second area;

forming a gate oxide layer over the second area and over the first conductive layer over the first area, wherein forming the first dielectric layer comprises forming an interlayer dielectric over the gate oxide; and

forming a fourth conductive layer over the gate oxide layer over the second area;

forming a fifth conductive layer over the third area;

forming an organic layer over the fifth conductive layer over the third area, wherein forming the second dielectric layer comprises forming the organic layer over the second conductive layer, wherein the third conductive layer is over the organic layer over the third area;

wherein the first conductive layer over the first area is connectable to a power supply voltage, and wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over

the first area, and the semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor, and

wherein forming the first conductive layer and forming the semiconductor layer comprise forming the first conductive layer and the semiconductor layer using the same semiconductor material which is provided as doped polysilicon, and wherein the fifth conductive layer, the organic layer, and the third conductive layer over the third area collectively form the OLED.

8. (Original) The method of claim 7, further comprising forming the second conductive layer over the second area for providing contact to the semiconductor layer.

9. (Withdrawn) The method of claim 7, wherein forming the second conductive layer and forming the fifth conductive layer comprise forming the second conductive layer and the fifth conductive layer using the same material.

10. (Original) The method of claim 7, further comprising forming a third dielectric layer between the second conductive layer and the second dielectric layer, wherein the third dielectric layer comprises passivation silicon nitride or capping silicon nitride.

11. (Original) The method of claim 7, wherein forming the fifth conductive layer comprises forming a layer of indium tin oxide (ITO).

REMARKS

This is a full and timely response to the outstanding Office Action mailed May 26, 2011. The Office Action identified the following species of invention: Figs. 2, 3, 4, 5, 6, 7, 8, 9, 10, and 11. Applicant hereby elects the species of figure 11. Claims 1, 7, 8, 10, and 11 read on this elected species.

Applicant understands that if other species are pursued in a divisional application, that the art (if any) used to reject claims of the present application will not similarly be used to reject claims directed to other species. In this regard, the present Office Action has advanced the election requirement on the basis that:

- *the species or groupings of patentably indistinct species have acquired a separate status in the art in view of their different classification;*
- *the species or groupings of patentably indistinct species have acquired a separate status in the art due to their recognized divergent subject matter;*
- *the species or groupings of patentably indistinct species require a different field of search (e.g., searching different classes /subclasses or electronic resources, or employing different search strategies or search queries).*

Consequently, the same prior art should not be applicable to claims of the non-elected species. If it is, then it would appear that the species is improper and should be withdrawn by the Examiner.

Applicant would also like to make of record the apparent inconsistency in the prosecution of the family of applications of the present application. Specifically, the following four applications are in this lineage:

- Application ser. No. 11/005,648, was filed December 7, 2004;
- Application ser. No. 11/616,943, filed Dec. 28, 2006, is a division of 11/005,648;

- Application ser. No. 12/540,517, filed Aug. 13, 2009, is also a division of 11/005,648;
- Application ser. No. 13/031,712, is a division of 11/616,943.

All four of these applications share a common specification. Therefore, it would appear that all four should be subject to the same species requirement (since the species requirement is based on the figures). In both the original application (ser. No. 11/005,648) and application serial number 12/540,517, no species election was advanced. Thus, two of the four applications had no species election requirement, while two of the four have been subject to a 10-way species election. Applicant finds this curious, and notes it for the record.

Applicant respectfully submits that the foregoing is fully responsive to the election requirement and that all presently pending claims be allowed to issue. If the Examiner has any questions or comments regarding Applicant's response, the Examiner is encouraged to telephone the undersigned.

CONCLUSION

Applicant expressly reserves the right to present the non-elected claims, or variants thereof, in continuing applications to be filed subsequent to the present application. Should the Examiner have any questions regarding this response, the Examiner is invited to telephone the undersigned attorney.

No fee is believed to be due in connection with this submission. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

/Daniel R. McClure/

By:

Daniel R. McClure
Registration No. 38,962

Customer No. 24504

Electronic Acknowledgement Receipt	
EFS ID:	10336224
Application Number:	13031712
International Application Number:	
Confirmation Number:	5546
Title of Invention:	Method for Forming a Pixel of an Electroluminescence Device having Storage Capacitors
First Named Inventor/Applicant Name:	Wein-Town Sun
Customer Number:	24504
Filer:	Daniel R. McClure
Filer Authorized By:	
Attorney Docket Number:	250142-1173
Receipt Date:	18-JUN-2011
Filing Date:	22-FEB-2011
Time Stamp:	07:18:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	01388753.PDF	100567	no	12
			4d15ae8402c6f67ba6c9bdcb5b8c15b38a904bbd		

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 13/031,712		Filing Date 02/22/2011		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY ☐ OR			OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))			If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)		(Column 3)			SMALL ENTITY OR OTHER THAN SMALL ENTITY		
AMENDMENT	06/18/2011	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 11	Minus	** 20	= 0	X \$ =		OR	X \$52=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X \$ =		OR	X \$220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/031,712	02/22/2011	Wein-Town Sun	250142-1173	5546
24504 7590 08/31/2011 THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP 400 INTERSTATE NORTH PARKWAY SE SUITE 1500 ATLANTA, GA 30339			EXAMINER MAI, ANH D	
			ART UNIT 2829	PAPER NUMBER
			NOTIFICATION DATE 08/31/2011	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspatents@tkhr.com
kristen.layton@tkhr.com
ozzie.liggins@tkhr.com

Office Action Summary	Application No.		Applicant(s)	
	13/031,712		SUN, WEIN-TOWN	
	Examiner		Art Unit	
	ANH MAI		2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 23 August 2011 (Oral election).

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5) ☒ Claim(s) 1-11 is/are pending in the application.

5a) Of the above claim(s) 4-11 is/are withdrawn from consideration.

6) ☐ Claim(s) ____ is/are allowed.

7) ☒ Claim(s) 1-3 is/are rejected.

8) ☐ Claim(s) ____ is/are objected to.

9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

10) ☒ The specification is objected to by the Examiner.

11) ☒ The drawing(s) filed on 22 February 2011 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date: ____.
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) ☐ Notice of Informal Patent Application
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>February 22, 2011</u> .	6) ☐ Other: ____.

DETAILED ACTION

Status of the Claims

1. Amendment filed June 18, 2011 is acknowledged. Applicant elected Species as shown in Fig. 11; and identified claims 1, 7, 8 10 and 11 are read on the elected Species.

However, reviewing the claims, it is determined that the elected claims 1, 7, 8, 10 and 11 do not read on the elected Species as indicated in the election. In a telephone conversation with Mr. Daniel R. McClure, Reg. No. 38,962 on August 19, 2011, Examiner had requested that the Applicant should review the claims and properly elect a Species and claim(s) that read on that Species.

On August 23, 2011, Applicant elected Species #1, as shown in Fig. 2 and identified claims 1-3 to read on the elected Species. Non-Elected Species, Claims 4-11 have been withdrawn from consideration. Claims 1-11 are pending.

Action on merits of elected Species #1, claims 1-3 follows.

Specification

2. An update of all co-pending applications identified in ¶ [0001] is requested.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103() as being anticipated by Koo et al. (US Pub. No. 2003/0117059) on view of Murade (US Patent No. 6,610,997) of record.

With respect to claim 1, Koo teaches a method for forming a pixel of an electroluminescence device substantially as claimed including:

- providing a substrate (100);
- defining at least a first area for capacitors and a second area for a transistor on the substrate (100);
- forming a first conductive layer (132) over the first area;
- forming a first dielectric layer (135) over the first conductive layer (132) over the first area;
- forming a second conductive layer (143) over the first dielectric layer (135) over the first area;
- forming a second dielectric layer (150) over the second conductive layer (143) over the first area;
- forming a third conductive layer (190) over the second dielectric layer (150) over the first area;
- forming a layer of capping layer (170) between the second dielectric layer (150) and the third conductive layer (190) over the first area;
- forming a semiconductor layer (120) over the second area;
- forming a gate insulating layer (125) over the second area; and
- forming a fourth conductive layer (131) over the gate insulating layer (125) over the second area;

wherein the first conductive layer (132) over the first area is connectable to a power supply voltage, and wherein the first conductive layer (132), the first dielectric layer (135), and the second conductive layer (143) over the first area collectively form a first one of the capacitors over the first area, the second conductive layer (143), the second dielectric layer (150), and the third conductive layer (190) over the first area collectively form a second one of the capacitors over the first area, and the semiconductor layer (120), the gate insulating layer (125), and the fourth conductive layer (131) over the second area collectively form a transistor. (See Fig. 2A).

Thus, Koo is shown to teach all the features of the claim with the exception of explicitly disclosing the materials being used for the capping layer (170) and the gate insulating layer (125).

However, Murade teaches a method for forming a pixel of an electronic device including forming a layer of capping silicon nitride (7) between a second dielectric layer (4) and a third conductive layer (9a) over a first area (70); and forming a gate oxide layer (2) over a second area (30). (See Fig. 3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the capping layer and gate insulation layer of Koo utilizing silicon nitride and gate oxide, respectively, as taught by Murade to increase the capacity of the capacitor and insulating the semiconductor layer.

Moreover, it has been held to be within the general skill of a worker in the art to select a known material, i.e., silicon nitride and oxide, on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416., 125 USPQ 416.

With respect to claim 2, in view of Murade, the method further comprises:

forming the gate oxide (125) over the first area;

forming the first conductive layer (132) over the gate oxide (125), wherein forming the first conductive layer (132) and forming the fourth conductive layer (131) comprise forming the first conductive layer (132) and the fourth conductive layer (131) using the same material, wherein forming the first dielectric layer (135) comprises forming a layer of interlayer dielectric (ILD), and wherein forming the second dielectric layer (150) comprises forming a layer of passivation silicon nitride;

defining a third area for an organic light-emitting diode (OLED) (101) on the substrate (100);

forming a fifth conductive layer (160) over the third area (101);

forming an organic layer (180) over the fifth conductive layer (160) over the third area, wherein the organic layer (180) is between the layer of capping layer (170) and the third conductive layer (190) over the first area (101); and

forming the third conductive layer (190) over the organic layer (180) over the third area (101), wherein the fifth conductive layer (160), the organic layer (180), and the third conductive layer (190) over the third area (101) collectively form the OLED.

With respect to claim 3, Koo teaches a method for forming a pixel of an electroluminescence device substantially as claimed including:

providing a substrate (100);

defining at least a first area for capacitors, a second area for a transistor (102) on the substrate (100) and a third area (101) for an organic light-emitting diode (OLED) on the substrate;

forming a first conductive layer (132) over the first area;

forming a first dielectric layer (135) over the first conductive layer (132) over the first area;

forming a second conductive layer (143) over the first dielectric layer (135) over the first area;

forming a second dielectric layer (150) over the second conductive layer (143) over the first area;

forming a third conductive layer (190) over the second dielectric layer (150) over the first area;

forming a semiconductor layer (120) over the second area;

forming a gate insulating layer (125) over the second area;

forming a fourth conductive layer (131) over the gate insulating layer (125) over the second area;

forming the gate insulating (125) over the first area;

forming the first conductive layer (132) over the gate insulating (125), wherein forming the first conductive layer (132) and forming the fourth conductive layer (131) comprise forming

the first conductive layer (132) and the fourth conductive layer (131) using the same material, wherein forming the first dielectric layer (135) comprises forming a layer of interlayer dielectric (ILD), and wherein forming the second dielectric layer (150) comprises forming a layer of passivation;

forming a fifth conductive layer (142/160) over the third area (101); and

forming an organic layer (180) over the fifth conductive layer (142/160) over the third area (101), wherein the third conductive layer (190) is over the organic layer (180) over the third area, and wherein the fifth conductive layer (142/160), the organic layer (180), and the third conductive layer (190) over the third area (101) collectively form the OLED,

wherein the first conductive layer (132) over the first area is connectable to a power supply voltage, and wherein the first conductive layer (132), the first dielectric layer (135), and the second conductive layer (143) over the first area collectively form a first one of the capacitors over the first area, the second conductive layer (143), the second dielectric layer (150), and the third conductive layer (190) over the first area collectively form a second one of the capacitors over the first area, and the semiconductor layer (120), the gate insulating layer (125), and the fourth conductive layer (131) over the second area collectively form a transistor, and

wherein forming the second conductive layer (143) and forming the fifth conductive layer (142) comprise forming the second conductive layer (143) and the fifth conductive layer (142) using the same material. (See Fig. 2A).

Thus, Koo is shown to teach all the features of the claim with the exception of explicitly disclosing the materials being used for the passivation layer (150) and the gate insulating layer (125).

However, Murade teaches a method for forming a pixel of an electronic device including forming a second dielectric layer (4) comprises forming a layer of passivation silicon nitride (4); and forming a gate oxide layer (2) over a second area (30). (See Fig. 3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the passivation layer and gate insulation layer of Koo utilizing silicon nitride and gate oxide, respectively, as taught by Murade to increase the capacity of the capacitor and insulating the semiconductor layer.

Moreover, it has been held to be within the general skill of a worker in the art to select a known material, i.e., silicon nitride and oxide, on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416., 125 USPQ 416.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANH MAI whose telephone number is (571)272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Anh D. Mai/
Primary Examiner, Art Unit 2829

Notice of References Cited	Application/Control No. 13/031,712	Applicant(s)/Patent Under Reexamination SUN, WEIN-TOWN	
	Examiner ANH MAI	Art Unit 2829	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,196,746	03-2007	Yang, Chien-Sheng	349/39
*	B	US-2003/0117059	06-2003	Koo et al.	313/422
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"7696521"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/08/24 09:36
L2	4	("20040095298" "20050083270" "20060132399" "6521913").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 09:37
L3	36	("5042918" "5208690" "5515187" "5589962" "5686980" "5818550" "5844255" "6147667" "6226059").PN. OR ("6521913").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 09:39
L4	33	"06067201" "08160463" "10020298" "10031235"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/08/24 09:47
L10	1	(10/394637).APP.	US-PGPUB; USOCR	ADJ	ON	2011/08/24 10:43
L15	2	("5824579" "5939760").PN. OR ("6066524").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 11:14
L24	8	("5260818" "5592318" "5734449" "6894735").PN. OR ("7196746").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 11:21
L25	12	("6177970" "6278503" "6400424").PN. OR ("6894735").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 11:24

L26	32	"6610997"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/08/24 11:33
L27	4	("20020104995" "20030127652" "5459596" "6610997").PN. OR ("7915117").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 11:52
L28	1	(10/330128).APP.	USPAT; USOCR	ADJ	ON	2011/08/24 12:16
L29	2	("6489631" "6696105").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 12:16
L30	1	(10/050597).APP.	USPAT; USOCR	ADJ	ON	2011/08/24 12:45
L31	30	("20020070913" "20020195603" "5182620" "5712495" "5747830" "5747930" "5815226" "5856689" "5998841" "6057647" "6118506" "6121652" "6229506" "6278131" "6323918" "6351078" "6414345" "6441829" "6462722" "6490014" "6492778" "6495886" "6521913").PN. OR ("6825496").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 12:45
L32	7	("20030111954" "20030117083" "6724149" "6762564" "6798405" "6825496" "7230591").PN. OR ("7696518").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 12:46

L33	8	("20030189207" "6569717" "6583472" "6610997" "6680488" "6897477" "6906344" "7232702").PN. OR ("7790526").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 13:47
L34	4	("5260818" "5592318" "5734449" "6894735").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 13:57
L35	21	("4759610" "5012274" "5028122" "5182661" "5321535" "5600461" "5657101").PN. OR ("5734449").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 13:58
L36	13	("20030193056" "5734449" "5956103" "6489631" "6542205" "6583472" "6597121" "6597413" "6614174" "6835954" "6921918" "6961111" "7256534").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 13:59
L37	1	(10/288509).APP.	US-PGPUB; USOCR	ADJ	ON	2011/08/24 13:59
L38	14	("20010048490" "20020038998" "20030128311" "5777701" "6002463" "6236063" "6262436" "6300152" "6532050" "6570631" "6583439" "6674495" "6955578").PN. OR ("7256534").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 15:00

L39	6	("4395467").PN. OR ("6955578").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 15:06
L40	7	("6489631" "6696105").PN. OR ("6835954").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 15:09
L41	8	("5260818" "5592318" "5734449" "6894735").PN. OR ("7196746").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 15:22
L53	18	("5672518" "6066860" "6232142").PN. OR ("6358759").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 15:35
L54	12	("20020037600" "5233211" "5637187" "6358759" "6697136").PN. OR ("6900861").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 15:36
L63	2	("20020196213" "6229506").PN. OR ("7443366").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/08/24 15:48

8/ 24/ 2011 5:45:23 PM

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Search Notes 	Application/Control No.		Applicant(s)/Patent under Reexamination	
	13/031,712		SUN, WEIN-TOWN	
	Examiner		Art Unit	
	ANH MAI		2829	

SEARCHED			
Class	Subclass	Date	Examiner
438	22, 23, 29 149, 155 239, 253	8/23/2011	A.M

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST (all) * Inventor * CCLS * See Attached Search History	8/23/2011	A.M

February 22, 2011

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

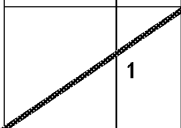
PTO/SB/08a (01-10)

Approved for use through 07/31/2012. OMB 0651-0031

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13/031,712	
	Filing Date		2011-02-22	
	First Named Inventor	Sun		
	Art Unit	2829		
	Examiner Name	Anh D. Mai		
	Attorney Docket Number	250142-1173		

U.S.PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
/A.M./	1	5459596		1995-10-17	Ueda, et al.			
/A.M./	2	6610997		2003-08-26	Murade			
If you wish to add additional U.S. Patent citation information please click the Add button.							Add	
U.S.PATENT APPLICATION PUBLICATIONS							Remove	
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
/A.M./	1	20020104995		2002-08-08	Yamazaki			
/A.M./	2	20030127652		2003-07-10	Park, et al.			
If you wish to add additional U.S. Published Application citation information please click the Add button.							Add	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13/031,712
	Filing Date		2011-02-22
	First Named Inventor	Sun	
	Art Unit		
	Examiner Name		
	Attorney Docket Number		250142-1173

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<small> ¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached. </small>				

<p align="center"><i>Index of Claims</i></p> 	Application/Control No. 13031712	Applicant(s)/Patent Under Reexamination SUN, WEIN-TOWN
	Examiner ANH MAI	Art Unit 2829

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	05/20/2011	08/24/2011						
	1	÷	✓						
	2	÷	✓						
	3	÷	✓						
	4	÷	N						
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	9	÷	N						
	10	÷	N						
	11	÷	N						

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Sun, Wein-Town

Serial No.: 13/031,712

Filed: February 22, 2011

Confirmation No.: 5546

Group Art Unit: 2829

Examiner: Mai, Anh D.

TKHR Ref.: 250142-1173

Client Ref.: 0632-A50404D2-US

For: **Method for Forming a Pixel of an Electroluminescence Device having Storage Capacitors**

AMENDMENT AND RESPONSE TO NON-FINAL OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

The non-final Office Action dated August 31, 2011 has been carefully considered. In response thereto, please enter the following amendments and consider the following remarks.

DEPOSIT ACCOUNT AUTHORIZATION

It is not believed that extensions of time are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor are hereby authorized to be charged to our Deposit Account No. 20-0778.

In the Claims

This listing of claims will replace all prior versions, and listings, of claims.

Listing of Claims

1. (Currently Amended) A method for forming a pixel of an electroluminescence device, comprising:

- providing a substrate;
- defining at least a first area for capacitors and a second area for a transistor on the substrate;
- forming a first conductive layer over the first area;
- forming a first dielectric layer over the first conductive layer over the first area;
- forming a second conductive layer over the first dielectric layer over the first area;
- forming a second dielectric layer over the second conductive layer over the first area;
- forming a third conductive layer over the second dielectric layer over the first area;
- forming a layer of capping silicon nitride between the second dielectric layer and the third conductive layer over the first area;
- forming a semiconductor layer over the second area;
- forming a gate oxide layer over the second area; and
- forming a fourth conductive layer over the gate oxide layer over the second area;

wherein the first conductive layer over the first area is directly connected ~~connectable~~ to a power supply voltage, wherein the second conductive layer is electrically connected to the fourth conductive layer, and wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over the first area, and the semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor.

2. (Original) The method of claim 1, further comprising:

forming the gate oxide over the first area;

forming the first conductive layer over the gate oxide, wherein forming the first conductive layer and forming the fourth conductive layer comprise forming the first conductive layer and the fourth conductive layer using the same material, wherein forming the first dielectric layer comprises forming a layer of interlayer dielectric (ILD), and wherein forming the second dielectric layer comprises forming a layer of passivation silicon nitride;

defining a third area for an organic light-emitting diode (OLED) on the substrate;

forming a fifth conductive layer over the third area;

forming an organic layer over the fifth conductive layer over the third area, wherein the organic layer is between the layer of capping silicon nitride and the third conductive layer over the first area; and

forming the third conductive layer over the organic layer over the third area, wherein the fifth conductive layer, the organic layer, and the third conductive layer over the third area collectively form the OLED.

3. (Currently Amended) A method for forming a pixel of an electroluminescence device, comprising:

providing a substrate;

defining at least a first area for capacitors, a second area for a transistor on the substrate and a third area for an organic light-emitting diode (OLED) on the substrate;

forming a first conductive layer over the first area;

forming a first dielectric layer over the first conductive layer over the first area;

forming a second conductive layer over the first dielectric layer over the first area;

forming a second dielectric layer over the second conductive layer over the first area;

forming a third conductive layer over the second dielectric layer over the first area;

forming a semiconductor layer over the second area;

forming a gate oxide layer over the second area;
forming a fourth conductive layer over the gate oxide layer over the second area;
forming the gate oxide over the first area;
forming the first conductive layer over the gate oxide, wherein forming the first conductive layer and forming the fourth conductive layer comprise forming the first conductive layer and the fourth conductive layer using the same material, wherein forming the first dielectric layer comprises forming a layer of interlayer dielectric (ILD), and wherein forming the second dielectric layer comprises forming a layer of passivation silicon nitride;
forming a fifth conductive layer over the third area; and
forming an organic layer over the fifth conductive layer over the third area, wherein the third conductive layer is over the organic layer over the third area, and wherein the fifth conductive layer, the organic layer, and the third conductive layer over the third area collectively form the OLED,
wherein the first conductive layer over the first area is directly connected ~~connectable~~ to a power supply voltage, wherein the second conductive layer is electrically connected to the fourth conductive layer, and wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over the first area, and the semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor, and
wherein forming the second conductive layer and forming the fifth conductive layer comprise forming the second conductive layer and the fifth conductive layer using the same material.

4. (Withdrawn) A method for forming a pixel of an electroluminescence device, comprising:

- providing a substrate;
- defining at least a first area for capacitors, a second area for a transistor on the substrate and a third area for an organic light-emitting diode (OLED) on the substrate;
- forming a first conductive layer over the first area;
- forming a first dielectric layer over the first conductive layer over the first area;
- forming a second conductive layer over the first dielectric layer over the first area;
- forming a second dielectric layer over the second conductive layer over the first area;
- forming a third conductive layer over the second dielectric layer over the first area;
- forming a layer of capping silicon nitride between the second dielectric layer and the third conductive layer over the first area;
- forming a semiconductor layer over the second area;
- forming a gate oxide layer over the first area and the second area, wherein the first conductive layer is both over the gate oxide over the first area and over the second area, the first conductive layer providing contact to the semiconductor layer over the second area;
- forming a fourth conductive layer over the gate oxide layer over the second area;
- forming a fifth conductive layer over the third area; and
- forming an organic layer over the fifth conductive layer over the third area,

wherein the third conductive layer over the organic layer over the third area,

- wherein the first conductive layer over the first area is connectable to a power supply voltage, and wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over the first area, and the semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor, and

wherein forming the first dielectric layer comprises forming a layer of passivation silicon nitride, forming the second conductive layer and forming the fifth conductive layer comprise forming the second conductive layer and the fifth conductive layer using the same material, and forming the second dielectric layer comprises forming a layer of capping silicon nitride, and wherein the fifth conductive layer, the organic layer, and the third conductive layer over the third area collectively form the OLED.

5. (Withdrawn) The method of claim 4, further comprising forming an interlayer dielectric layer over the gate oxide layer over the first area and forming the first conductive layer over the third dielectric layer.

6. (Withdrawn) The method of claim 4, further comprising forming the organic layer between the second dielectric and the third conductive layer over the first area.

7. (Withdrawn) A method for forming a pixel of an electroluminescence device, comprising:

- providing a substrate;

- defining at least a first area for capacitors, a second area for a transistor on the substrate and a third area for an organic light-emitting diode (OLED) on the substrate;

- forming a first conductive layer over the first area;

- forming a first dielectric layer over the first conductive layer over the first area;

- forming a second conductive layer over the first dielectric layer over the first area;

- forming a second dielectric layer over the second conductive layer over the first area;

- forming a third conductive layer over the second dielectric layer over the first area;

- forming a semiconductor layer over the second area;

- forming a gate oxide layer over the second area and over the first conductive layer over the first area, wherein forming the first dielectric layer comprises forming an interlayer dielectric over the gate oxide; and

- forming a fourth conductive layer over the gate oxide layer over the second area;

forming a fifth conductive layer over the third area;

forming an organic layer over the fifth conductive layer over the third area, wherein forming the second dielectric layer comprises forming the organic layer over the second conductive layer, wherein the third conductive layer is over the organic layer over the third area;

wherein the first conductive layer over the first area is connectable to a power supply voltage, and wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over the first area, and the semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor, and

wherein forming the first conductive layer and forming the semiconductor layer comprise forming the first conductive layer and the semiconductor layer using the same semiconductor material which is provided as doped polysilicon, and wherein the fifth conductive layer, the organic layer, and the third conductive layer over the third area collectively form the OLED.

8. (Withdrawn) The method of claim 7, further comprising forming the second conductive layer over the second area for providing contact to the semiconductor layer.

9. (Withdrawn) The method of claim 7, wherein forming the second conductive layer and forming the fifth conductive layer comprise forming the second conductive layer and the fifth conductive layer using the same material.

10. (Withdrawn) The method of claim 7, further comprising forming a third dielectric layer between the second conductive layer and the second dielectric layer, wherein the third dielectric layer comprises passivation silicon nitride or capping silicon nitride.

11. (Withdrawn) The method of claim 7, wherein forming the fifth conductive layer comprises forming a layer of indium tin oxide (ITO).

REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed August 31, 2011. The Examiner is thanked for the thorough examination of the present application. Upon entry of this response, claims 1-11 are pending in the present application. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

I. Summary of Telephone Interview with Examiner

Applicant wishes to thank Examiner Mai for the time spent with Applicant's representative Jeffrey Hsu (Registration No. 63,063) during a telephone interview conducted on November 29, 2011 regarding the above-identified Office Action. During the telephone interview, various amendments were discussed, including amendments suggested by Examiner Mai for defining over the cited references. Specifically, various amendments were discussed with Examiner Mai regarding structural limitations relating to the various conductive layers defined in the claims. Applicant respectfully submits that the amendments set forth herein are consistent with those discussed during the interview. Applicant requests consideration of the following remarks contained herein.

II. Response to Claim Rejections Under 35 U.S.C. § 103

For a proper rejection of the claim under 35 U.S.C. §103, the cited combination of references must disclose, teach, or suggest all elements / features of the claim at issue. See, e.g., *In re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988) and *In*

re *Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981). Claims 1-3 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over *Koo, et al.* (U.S. Pub. No. 2003/0117059, hereinafter "*Koo*") in view of *Murade, et al.* (U.S. Patent No. 6,610,997 hereinafter "*Murade*").

Applicant respectfully submits that independent claims 1 and 3 are allowable over *Koo* in view of *Murade* for at least the reason that the combination fails to disclose, teach, or suggest the features emphasized below.

Claim 1, as amended, recites:

1. A method for forming a pixel of an electroluminescence device, comprising:
providing a substrate;
defining at least a first area for capacitors and a second area for a transistor on the substrate;
forming a first conductive layer over the first area;
forming a first dielectric layer over the first conductive layer over the first area;
forming a second conductive layer over the first dielectric layer over the first area;
forming a second dielectric layer over the second conductive layer over the first area;
forming a third conductive layer over the second dielectric layer over the first area;
forming a layer of capping silicon nitride between the second dielectric layer and the third conductive layer over the first area;
forming a semiconductor layer over the second area;
forming a gate oxide layer over the second area; and
forming a fourth conductive layer over the gate oxide layer over the second area;
wherein the first conductive layer over the first area is directly connected to a power supply voltage, wherein the second conductive layer is electrically connected to the fourth conductive layer, and wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over the first area, and the semiconductor layer,

the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor.

Claim 3, as amended, recites:

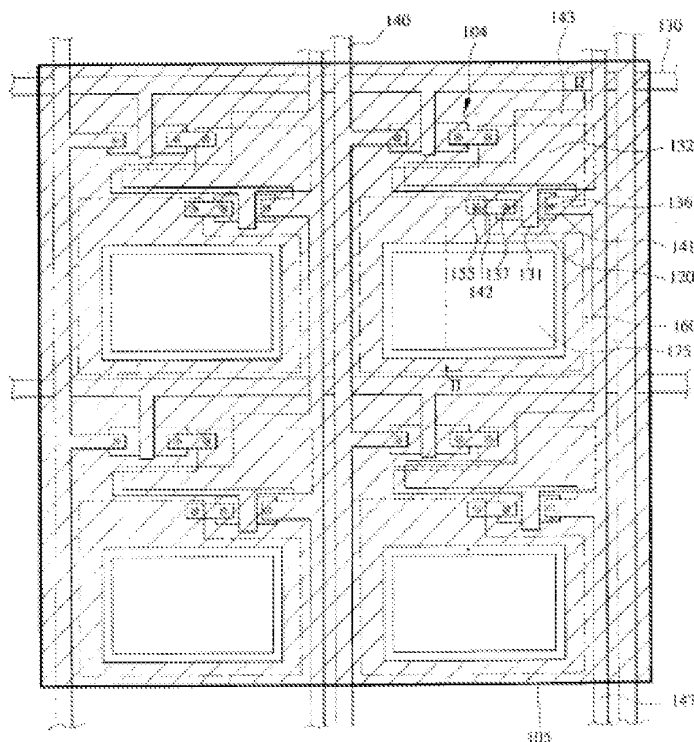
3. A method for forming a pixel of an electroluminescence device, comprising:
providing a substrate;
defining at least a first area for capacitors, a second area for a transistor on the substrate and a third area for an organic light-emitting diode (OLED) on the substrate;
forming a first conductive layer over the first area;
forming a first dielectric layer over the first conductive layer over the first area;
forming a second conductive layer over the first dielectric layer over the first area;
forming a second dielectric layer over the second conductive layer over the first area;
forming a third conductive layer over the second dielectric layer over the first area;
forming a semiconductor layer over the second area;
forming a gate oxide layer over the second area;
forming a fourth conductive layer over the gate oxide layer over the second area;
forming the gate oxide over the first area;
forming the first conductive layer over the gate oxide, wherein forming the first conductive layer and forming the fourth conductive layer comprise forming the first conductive layer and the fourth conductive layer using the same material, wherein forming the first dielectric layer comprises forming a layer of interlayer dielectric (ILD), and wherein forming the second dielectric layer comprises forming a layer of passivation silicon nitride;
forming a fifth conductive layer over the third area; and
forming an organic layer over the fifth conductive layer over the third area, wherein the third conductive layer is over the organic layer over the third area, and wherein the fifth conductive layer, the organic layer, and the third conductive layer over the third area collectively form the OLED,
wherein the first conductive layer over the first area is directly connected to a power supply voltage, wherein the second conductive layer is electrically connected to the fourth conductive layer, and wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over the first area, and the semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor, and

wherein forming the second conductive layer and forming the fifth conductive layer comprise forming the second conductive layer and the fifth conductive layer using the same material.

(Emphasis added). As set forth above, claims 1 and 3 have been amended to recite the features “the first conductive layer over the first area is directly connected to a power supply voltage” and “wherein the second conductive layer is electrically connected to the fourth conductive layer.”

Support for the amendment can be found, for example, in paragraph [0019] and FIG. 2 of the application, which shows that over area A, first metal pattern 206A, ILD 208, and second metal pattern 210A collectively form capacitor 108; second metal pattern 210A, passivation SiN 212, organic 218, and third metal 220 collectively form capacitor 112. Over area B, polysilicon pattern 202B provides the source and drain of transistor 102 and first metal pattern 206B serves as the gate of transistor 102. Over area C, ITO pattern 214C, capping SiN 216, organic 218, and third metal 220 collectively form part of OLED 110. Furthermore, first metal pattern 206A is coupled to power supply voltage V_{DD} , second metal pattern 210A is coupled to the gate of transistor 102, i.e., first metal pattern 206B, and third metal 220 is coupled to V_{SS} . Applicant submits that as discussed during the telephone interview with the Examiner, the cited references fail to disclose or suggest these features.

Koo discloses a flat panel display. The Examiner asserts that the first electrode 132, the second electrode 143, and the gate electrode 131 read on as the first conductive layer, the second conductive layer and the fourth conductive layer in claim 1, respectively.



As shown in FIGS. 2A-B of *Koo* (FIG. 2B is reproduced above), the power supply line 147 is directly connected to the source/drain electrode 141 and the second electrode 143. Also, in paragraph [0039], *Koo* teaches that the first electrode 132 comprises the same material as the gate electrode 131 and the second electrode 143 that is connected to one of the source/drain electrodes, e.g., the source/drain electrode 141. However, the first electrode 132 disclosed by *Koo* is not directly connected to the power supply voltage 147. Further, *Koo*'s second electrode 143 is not electrically connected to the gate electrode 131.

Since the first electrode 132 of *Koo* is not directly connected to the power supply voltage 147, the second electrode 143 of *Koo* is not electrically connected to the gate electrode 131, it is inappropriate to use the first electrode 132 and the second electrode 143 of *Koo* as the first conductive layer and the second conductive layer of the present

invention, respectively. Furthermore, in the Office Action, the Examiner does not mention which features of *Murade* correspond to the first conductive layer, the second conductive layer and the power supply voltage in claim 1, respectively.

Accordingly, Applicant believes that the combination of *Koo* in view of *Murade* fails to disclose or suggest the claimed feature “the first conductive layer over the first area is directly connected to a power supply voltage, wherein the second conductive layer is electrically connected to the fourth conductive layer, and wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over the first area, and the semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor,” as recited in claim 1. Therefore, Applicant believes that the claim 1 is allowable. For reasons similar to those discussed above, claim 3 is also believed to be allowable over the cited art. Dependent claim 2 is allowable for at least the reason that this claim depends from an allowable independent claim. See, e.g., *In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

CONCLUSION

Applicant respectfully submits that all pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a

telephone conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

/Daniel R. McClure/

Daniel R. McClure
Reg. No. 38,962

Customer No. 24504

Under the paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)	Docket Number (Optional) 250142-1173																																
Application Number 13/031,712	Filed February 22, 2011																																
For Method for Forming a Pixel of an Electroluminescence Device having Storage Capacitors																																	
Art Unit 2829	Examiner Mai, Anh D.																																
<p>This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.</p> <p>The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):</p> <table style="width: 100%; border-collapse: collapse;"><thead><tr><th></th><th style="text-align: center;"><u>Fee</u></th><th style="text-align: center;"><u>Small Entity Fee</u></th><th></th></tr></thead><tbody><tr><td>☒ One month (37 CFR 1.17(a)(1))</td><td style="text-align: center;">\$150</td><td style="text-align: center;">\$75</td><td style="text-align: right;">\$ <u>150.00</u></td></tr><tr><td>☐ Two months (37 CFR 1.17(a)(2))</td><td style="text-align: center;">\$560</td><td style="text-align: center;">\$280</td><td style="text-align: right;">\$ _____</td></tr><tr><td>☐ Three months (37 CFR 1.17(a)(3))</td><td style="text-align: center;">\$1270</td><td style="text-align: center;">\$635</td><td style="text-align: right;">\$ _____</td></tr><tr><td>☐ Four months (37 CFR 1.17(a)(4))</td><td style="text-align: center;">\$1980</td><td style="text-align: center;">\$990</td><td style="text-align: right;">\$ _____</td></tr><tr><td>☐ Five months (37 CFR 1.17(a)(5))</td><td style="text-align: center;">\$2690</td><td style="text-align: center;">\$1345</td><td style="text-align: right;">\$ _____</td></tr></tbody></table> <p>☐ Applicant claims small entity status. See 37 CFR 1.27.</p> <p>☐ A check in the amount of the fee is enclosed.</p> <p>☒ Payment by credit card. Form PTO-2038 is attached.</p> <p>☐ The Director has already been authorized to charge fees in this application to a Deposit Account.</p> <p>☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number <u>20-0778</u>.</p> <p>WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.</p> <p>I am the ☐ applicant/inventor.</p> <p style="margin-left: 40px;">☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96).</p> <p style="margin-left: 40px;">☒ attorney or agent of record. Registration Number <u>38,962</u></p> <p style="margin-left: 40px;">☐ attorney or agent under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____</p> <table style="width: 100%; border-collapse: collapse;"><tr><td style="width: 60%; border-bottom: 1px solid black; padding-bottom: 5px;">/Daniel R. McClure/</td><td style="width: 40%; border-bottom: 1px solid black; padding-bottom: 5px;">December 27, 2011</td></tr><tr><td style="text-align: center; padding-top: 5px;">Signature</td><td style="text-align: center; padding-top: 5px;">Date</td></tr><tr><td style="border-bottom: 1px solid black; padding-bottom: 5px;">Daniel R. McClure</td><td style="border-bottom: 1px solid black; padding-bottom: 5px;">770-933-9500</td></tr><tr><td style="text-align: center; padding-top: 5px;">Typed or printed name</td><td style="text-align: center; padding-top: 5px;">Telephone Number</td></tr></table> <p><small>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.</small></p> <p>☒ Total of <u>2</u> forms are submitted.</p>			<u>Fee</u>	<u>Small Entity Fee</u>		☒ One month (37 CFR 1.17(a)(1))	\$150	\$75	\$ <u>150.00</u>	☐ Two months (37 CFR 1.17(a)(2))	\$560	\$280	\$ _____	☐ Three months (37 CFR 1.17(a)(3))	\$1270	\$635	\$ _____	☐ Four months (37 CFR 1.17(a)(4))	\$1980	\$990	\$ _____	☐ Five months (37 CFR 1.17(a)(5))	\$2690	\$1345	\$ _____	/Daniel R. McClure/	December 27, 2011	Signature	Date	Daniel R. McClure	770-933-9500	Typed or printed name	Telephone Number
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This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		13031712		
Filing Date:		22-Feb-2011		
Title of Invention:		Method for Forming a Pixel of an Electroluminescence Device having Storage Capacitors		
First Named Inventor/Applicant Name:		Wein-Town Sun		
Filer:		Daniel R. McClure		
Attorney Docket Number:		250142-1173		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with \$0 paid	1251	1	150	150

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				150

Electronic Acknowledgement Receipt	
EFS ID:	11713308
Application Number:	13031712
International Application Number:	
Confirmation Number:	5546
Title of Invention:	Method for Forming a Pixel of an Electroluminescence Device having Storage Capacitors
First Named Inventor/Applicant Name:	Wein-Town Sun
Customer Number:	24504
Filer:	Daniel R. McClure
Filer Authorized By:	
Attorney Docket Number:	250142-1173
Receipt Date:	27-DEC-2011
Filing Date:	22-FEB-2011
Time Stamp:	17:41:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 150
RAM confirmation Number	3881
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Amendment/Req. Reconsideration-After Non-Final Reject	01515076.PDF	181134 <small>33367f584e369522b1ed9df82fc82c8d01451736</small>	no	15
Warnings:					
Information:					
2	Extension of Time	01515079.PDF	286941 <small>35052b335d59f3695741fe717cafca8e857500e5</small>	no	2
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	29872 <small>8069ddd524af3105d841355d55ea03919bf8fb6e</small>	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			497947		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 13/031,712		Filing Date 02/22/2011		☐ To be Mailed			
APPLICATION AS FILED – PART I												
(Column 1)			(Column 2)		SMALL ENTITY ☐		OR			OTHER THAN SMALL ENTITY		
FOR		NUMBER FILED	NUMBER EXTRA		RATE (\$)	FEE (\$)	OR		RATE (\$)	FEE (\$)		
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A		OR		N/A			
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A	N/A		N/A		OR		N/A			
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A		OR		N/A			
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*		X \$ =		OR		X \$ =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*		X \$ =		OR		X \$ =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).					OR					
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							OR					
					TOTAL		OR		TOTAL			
* If the difference in column 1 is less than zero, enter "0" in column 2.												
APPLICATION AS AMENDED – PART II												
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR		OTHER THAN SMALL ENTITY	
AMENDMENT	12/27/2011	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 10	Minus	** 20	= 0	X \$ =		OR		X \$60=	0	
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X \$ =		OR		X \$250=	0	
	☐ Application Size Fee (37 CFR 1.16(s))							OR				
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR				
					TOTAL ADD'L FEE		OR		TOTAL ADD'L FEE	0		
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR		OTHER THAN SMALL ENTITY	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR		X \$ =		
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR		X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))							OR				
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR				
					TOTAL ADD'L FEE		OR		TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.												

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record

A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews

Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.

All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:

- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

- 1) A brief description of the nature of any exhibit shown or any demonstration conducted,
- 2) an identification of the claims discussed,
- 3) an identification of the specific prior art discussed,
- 4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
- 5) a brief identification of the general thrust of the principal arguments presented to the examiner,
(The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
- 6) a general indication of any other pertinent matters discussed, and
- 7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

24504 7590 02/02/2012
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
400 INTERSTATE NORTH PARKWAY SE
SUITE 1500
ATLANTA, GA 30339

EXAMINER

MAI, ANH D

ART UNIT

PAPER NUMBER

2829

DATE MAILED: 02/02/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/031,712	02/22/2011	Wein-Town Sun	250142-1173	5546

TITLE OF INVENTION: METHOD FOR FORMING A PIXEL OF AN ELECTROLUMINESCENCE DEVICE HAVING STORAGE CAPACITORS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	05/02/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

24504 7590 02/02/2012
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
400 INTERSTATE NORTH PARKWAY SE
SUITE 1500
ATLANTA, GA 30339

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/031,712	02/22/2011	Wein-Town Sun	250142-1173	5546

TITLE OF INVENTION: METHOD FOR FORMING A PIXEL OF AN ELECTROLUMINESCENCE DEVICE HAVING STORAGE CAPACITORS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	05/02/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
MAI, ANH D	2829	438-253000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/031,712	02/22/2011	Wein-Town Sun	250142-1173	5546
24504 7590 02/02/2012 THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP 400 INTERSTATE NORTH PARKWAY SE SUITE 1500 ATLANTA, GA 30339			EXAMINER MAI, ANH D	
			ART UNIT 2829	PAPER NUMBER

DATE MAILED: 02/02/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.		Applicant(s)	
	13/031,712		SUN, WEIN-TOWN	
	Examiner		Art Unit	
	ANH MAI		2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed December 27, 2011.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-3.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☒ Interview Summary (PTO-413), Paper No./Mail Date <u>20111129</u> . 7. ☒ Examiner's Amendment/Comment 8. ☒ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____.
---	--

/Anh D. Mai/ Primary Examiner, Art Unit 2829	
---	--

DETAILED ACTION

Status of the Claims

1. Amendment filed December 27, 2011 is acknowledged. Claims 1 and 3 have been amended. Non-Elected Species, Claims 4-11 have been withdrawn from consideration. Claims are pending.
2. Claims 1-3 are allowable. The restriction requirement among distinct Species, as set forth in the Office action mailed on May 26, 2011, has been reconsidered in view of the allowability of claims to the elected invention pursuant to MPEP § 821.04(a). **The restriction requirement is hereby withdrawn as to any claim that requires all the limitations of an allowable claim.** Claims 4-11, however, directed to other mutually distinct species remain withdrawn from further consideration because they do not all require all the limitations of an allowable generic linking claim as required by 37 CFR 1.141.

In view of the above noted withdrawal of the restriction requirement, applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once a restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

3. This application is in condition for allowance except for the presence of claims 4-11 directed to distinct species non-elected without traverse. Accordingly, claims 4-11 have been cancelled.

EXAMINER'S AMENDMENT

4. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In the Claims:

Cancel claims 4-11.

Allowable Subject Matter

5. Claims 1-3 are allowed.
6. The following is an examiner's statement of reasons for allowance: See the Remarks filed December 27, 2011.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANH MAI whose telephone number is (571)272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Anh D. Mai/
Primary Examiner, Art Unit 2829

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L10	6	"7586121" "7915117"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/01/06 14:40
S185	64	("20010019144" "20020070400" "20020185303" "20040087058" "20040104451" "20040110319" "20040231885" "20050161833" "20050230800" "20060000542" "20060043567" "20060091494" "20060091495" "20060099803" "20060158368" "20060220167" "20060228855" "20060281278" "3585472" "4236046" "4998159" "5126801" "5256597" "5387888" "5612512" "5930639" "5970362" "6005197" "6165814" "6218729" "6252178" "6277436" "6331442" "6346743" "6400576" "6407929" "6477034" "6507496" "6519136" "6524905" "6565730" "6568073" "6582979" "6590227" "6611419" "6677630" "6678144" "6714422" "6724611" "6787902" "6803324" "6818469" "6822170" "6841861" "6847527" "6889431" "6890810" "6900708" "6917259" "6970362" "7290315" "7435675" "7541265" "7588992").PN. OR ("7687366").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2011/12/12 10:32
S186	91	("3938064" "4337446" "4563661" "5204314" "5453494" "5536323" "5635420" "5645634" "5653806" "5711816" "5741363" "5820664" "5850664" "5876503" "5919522" "5980983" "6010969").PN. OR ("6277436").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2011/12/12 10:34
S187	24	("4322736" "4908688" "4966864" "4977105" "5296729" "5373170" "5459688" "5514880" "5589415").PN. OR ("5824579").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2011/12/12 10:42
S188	9	("5726098" "5759914" "5824579" "5859264" "5972788" "6022804" "6180514").PN. OR ("6245664").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2011/12/12 10:43
S189	8	("20030015796" "20050082586" "5442236" "5759914" "6022804" "6245664" "6313029" "6710466").PN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2011/12/12 10:44
S190	11	("5726100" "5741741" "5932928" "5985746" "6008114" "6077769"	US-PGPUB; USPAT;	ADJ	OFF	2011/12/12 10:45

EAST Search History

		"6159845" "6171951" "6174804" "6211063").PN. OR ("6313029").URPN.	USOCR			
S191	16	("4840923" "4872050").PN. OR ("6022804").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2011/12/12 10:48
S192	28	("4619037" "4874719" "4900695" "4948756" "5204286" "5545584").PN. OR ("5726098").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2011/12/12 10:50
S193	43	("3921282" "4290188" "4619037" "4685197" "4717449" "4808261" "4808555" "4874719" "4877483").PN. OR ("4966864").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2011/12/12 10:54
S194	7	("5327003" "5460995" "5536674" "5545584" "5780909").PN. OR ("5926698").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2011/12/12 10:59

1/ 6/ 2012 3:00:25 PM

C:\Users\amail\Documents\EAST\Workspaces\11005648-TFT with two capacitor.wsp

Search Notes 	Application/Control No. 13031712	Applicant(s)/Patent Under Reexamination SUN, WEIN-TOWN
	Examiner ANH MAI	Art Unit 2829

SEARCHED			
Class	Subclass	Date	Examiner
438	23, 155, 239, 253	1/6/2012	A.M

SEARCH NOTES			
Search Notes		Date	Examiner
EAST (all): * Inventor, ** CCLS, *** See Attached Search History		1/6/2012	A.M

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
438	155, 239, 253,	1/6/2012	A.M
257	E51.026, E21.411	1/6/2012	A.M

	/ANH MAI/ Primary Examiner.Art Unit 2829
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 5546

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
13/031,712	02/22/2011	438	2829	250142-1173		
APPLICANTS Wein-Town Sun, Hsinchu, TAIWAN; ** CONTINUING DATA ***** This application is a DIV of 11/616,943 12/28/2006 PAT 7,915,117 which is a DIV of 11/005,648 12/07/2004 PAT 7,586,121 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 03/03/2011						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☐ No Verified and /ANH D MAI/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 11	TOTAL CLAIMS 11	INDEPENDENT CLAIMS 4
ADDRESS THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP 400 INTERSTATE NORTH PARKWAY SE SUITE 1500 ATLANTA, GA 30339 UNITED STATES						
TITLE Method for Forming a Pixel of an Electroluminescence Device having Storage Capacitors						
FILING FEE RECEIVED 1310	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

24504 7590 02/02/2012
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
400 INTERSTATE NORTH PARKWAY SE
SUITE 1500
ATLANTA, GA 30339

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

13/031,712 02/22/2011 Wein-Town Sun 250142-1173 5546

TITLE OF INVENTION: METHOD FOR FORMING A PIXEL OF AN ELECTROLUMINESCENCE DEVICE HAVING STORAGE CAPACITORS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional NO \$1740 \$300 \$0 \$2040 05/02/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
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MAI, ANH D 2829 438-253000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
 1 Thomas|Kayden
 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

AU OPTRONICS CORPORATION

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

HSINCHU, TAIWAN R.O.C.

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

☐ A check is enclosed.
☒ Payment by credit card: XXXXXXXXXXXXXXX
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 20-0778 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Daniel R. McClure/

Date March 14, 2012

Typed or printed name Daniel R. McClure

Registration No. 38,962

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:		13031712		
Filing Date:		22-Feb-2011		
Title of Invention:		METHOD FOR FORMING A PIXEL OF AN ELECTROLUMINESCENCE DEVICE HAVING STORAGE CAPACITORS		
First Named Inventor/Applicant Name:		Wein-Town Sun		
Filer:		Daniel R. McClure/Brooke French		
Attorney Docket Number:		250142-1173		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1740	1740
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2040

Electronic Acknowledgement Receipt	
EFS ID:	12306172
Application Number:	13031712
International Application Number:	
Confirmation Number:	5546
Title of Invention:	METHOD FOR FORMING A PIXEL OF AN ELECTROLUMINESCENCE DEVICE HAVING STORAGE CAPACITORS
First Named Inventor/Applicant Name:	Wein-Town Sun
Customer Number:	24504
Filer:	Daniel R. McClure/Brooke French
Filer Authorized By:	Daniel R. McClure
Attorney Docket Number:	250142-1173
Receipt Date:	14-MAR-2012
Filing Date:	22-FEB-2011
Time Stamp:	17:14:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 2040
RAM confirmation Number	4377
Deposit Account	200778
Authorized User	MCCLURE,DANIEL R.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	01572254.PDF	1020715	no	1
			6a9af88b6d94b6baa8ccc1f96778df78bf993d11		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32099	no	2
			rlb8d3a0418b340a78dabfe8d8608b3a937b0e92		
Warnings:					
Information:					
Total Files Size (in bytes):			1052814		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/031,712	04/17/2012	8158477	250142-1173	5546

24504 7590 03/28/2012
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
400 INTERSTATE NORTH PARKWAY SE
SUITE 1500
ATLANTA, GA 30339

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Wein-Town Sun, Hsinchu, TAIWAN;



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
13/031,712	8158477	2889	9200



Correspondence Address/Fee Address Change

The following fields have been set to Customer Number 109673 on 12/21/2012

- Correspondence Address
- Maintenance Fee Address

The address of record for Customer Number 109673 is:

109673
McClure, Qualey & Rodack, LLP
400 Interstate North Parkway SE
Suite 200
Atlanta, GA 30339