

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE Technology Group Co., Ltd.
Petitioner

v.

Optronic Sciences LLC
Patent Owner

Inter Partes Review No.: IPR2024-01315

**PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO.
8,158,477 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. §§ 42.1-100, ET SEQ**

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1001	U.S. Patent No. 8,158,477 (477 Patent)
1002	Declaration of Dean Neikirk in Support of Petition for Inter Partes Review of U.S. Patent 8,158,477 (477 Patent)
1003	U.S. Patent No. 7,330,168 (“Anzai”)
1004	U.S. Patent No. 6,992,332 (“Yamazaki”)
1005	File History of U.S. Patent No. 8,158,477
1006	Polysilicon TFT Technology for Active Matrix OLED Display by Mark Stewart, et. al., (“Stewart”)
1007	U.S. Patent Publication No. 2003/0067266 (“Kim”)
1008	U.S. Patent Publication No. 2006/0208979 (“Fish”)
1009	PCT Publication No. WO 2003/71511 (“Choi”)
1010	U.S. Patent No. 6,476,419 (“Yasuda”)
1011	U.S. Patent Publication No. 2003/0117059 (“Koo”)
1012	U.S. Patent No. 6,610,997 (“Murade”)
1013	U.S. Patent No. 6,246,179 (“Yamada”)
1014	A Flexible Multilayer Resist System Using Low Temperature Plasma-Deposited Silicon Nitride by B.R. Soller et. Al., (“Soller”)
1015	Room Temperature Deposition of Silicon Nitride Films for Passivation of Organic Electroluminescence Device Using a Sputtering Type Electron Cyclotron Resonance Plasma by Dawei Gao, et. al. (“Gao”)
1016	U.S. Patent No. 7,948,170 (“Strakhilev”)

CHART OF CLAIMS	
[1pre]	A method for forming a pixel of an electroluminescence device, comprising:
[1a]	providing a substrate;
[1b]	defining at least a first area for capacitors and a second area for a transistor on the substrate;
[1c]	forming a first conductive layer over the first area;
[1d]	forming a first dielectric layer over the first conductive layer over the first area;
[1e]	forming a second conductive layer over the first dielectric layer over the first area;
[1f]	forming a second dielectric layer over the second conductive layer over the first area;
[1g]	forming a third conductive layer over the second dielectric layer over the first area;
[1h]	forming a layer of capping silicon nitride between the second dielectric layer and the third conductive layer over the first area;
[1i]	forming a semiconductor layer over the second area;
[1j]	forming a gate oxide layer over the second area; and
[1k]	forming a fourth conductive layer over the gate oxide layer over the second area;
[1l]	wherein the first conductive layer over the first area is directly connected to a power supply voltage,
[1m]	wherein the second conductive layer is electrically connected to the fourth conductive layer, and
[1n]	wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over the first area, and
[1o]	the semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor.
[3pre]	A method for forming a pixel of an electroluminescence device, comprising:
[3a]	providing a substrate;
[3b]	defining at least a first area for capacitors, a second area for a transistor on the substrate and a third area for an organic light-emitting diode (OLED) on the substrate;
[3c]	forming a first conductive layer over the first area;

CHART OF CLAIMS	
[3d]	forming a first dielectric layer over the first conductive layer over the first area;
[3e]	forming a second conductive layer over the first dielectric layer over the first area;
[3f]	forming a second dielectric layer over the second conductive layer over the first area;
[3g]	forming a third conductive layer over the second dielectric layer over the first area;
[3h]	forming a semiconductor layer over the second area;
[3i]	forming a gate oxide layer over the second area;
[3j]	forming a fourth conductive layer over the gate oxide layer over the second area;
[3k]	forming the gate oxide over the first area;
[3l]	forming the first conductive layer over the gate oxide,
[3m]	wherein forming the first conductive layer and forming the fourth conductive layer comprise forming the first conductive layer and the fourth conductive layer using the same material,
[3n]	wherein forming the first dielectric layer comprises forming a layer of interlayer dielectric (ILD), and
[3o]	wherein forming the second dielectric layer comprises forming a layer of passivation silicon nitride;
[3p]	forming a fifth conductive layer over the third area; and
[3q]	forming an organic layer over the fifth conductive layer over the third area, wherein the third conductive layer is over the organic layer over the third area, and wherein the fifth conductive layer, the organic layer, and the third conductive layer over the third area collectively form the OLED,
[3r]	wherein the first conductive layer over the first area is directly connected to a power supply voltage,
[3s]	wherein the second conductive layer is electrically connected to the fourth conductive layer, and
[3t]	wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over the first area,
[3u]	and the semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor, and

CHART OF CLAIMS

[3v] wherein forming the second conductive layer and forming the fifth conductive layer comprise forming the second conductive layer and the fifth conductive layer using the same material.
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I. INTRODUCTION

BOE Technology Group Co. LTD. (“Petitioner”) requests *inter partes* review of claims 1 and 3 (“Challenged Claims”) of U.S. Patent No. 8,158,477 (“477 patent,” EX1001), owned by Optronic Sciences LLC (“PO”).

This petition relies upon the declaration of Dean Neikirk (EX1002) and copies large portions of that declaration herein.

II. STATEMENT OF PRECISE RELIEF REQUESTED

In accordance with 35 U.S.C. § 311, Petitioner requests cancelation of claims 1 and 3 of the 477 patent in view of the following grounds:

Ground	Claims	Stat. Basis	Prior Art
1	1, 3	35 U.S.C. §103	Anzai
2	1, 3	35 U.S.C. §103	Anzai in view of Yamazaki
3	1, 3	35 U.S.C. §103	Anzai in view of Yamada

III. THE 477 PATENT

A. Overview of the Patent

The 477 Patent was filed on February 22, 2011, and issued on April 17, 2012. EX1001, Face of Patent. EX1002, ¶38.

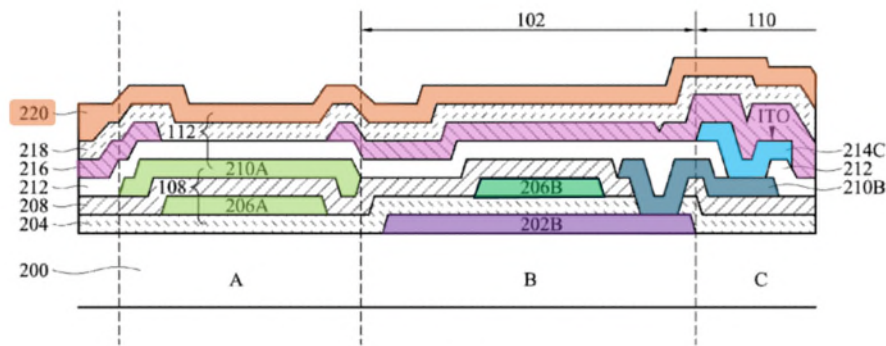


FIG. 2

The 477 Patent, as seen in Figure 2 above (with coloring added), is directed to an OLED device with a plurality of pixels where each pixel (100, as shown in Fig. 1) comprises three areas formed on a substrate 200. EX1001, Abstract. In the first area, area A, a first capacitor 108 and a second capacitor 112 are formed vertically stacked above each other, where the two storage capacitors share the second conductive layer 210A to increase the storage capacitance without increasing chip area or additional masks. *Id.*, Abstract, 5:26-7:3. EX1002, ¶39.

Here, in the first area, area A, the first storage capacitor 108 comprises a first metal pattern 206A (light green), the interlayer dielectric 208, and the second metal pattern 210A (light green). The second storage capacitor 112 comprises the second metal pattern 210A, the passivation SiN layer 212 and the capping SiN layer 216 (pink), organic layer 218, and the third metal layer 220 (orange). *Id.*, 6:1-56. The two storage capacitors 108 and 112 share a common electrode (second metal pattern 210A); this configuration is commonly referred to in the art as a tri-plate capacitor. The 477 Patent discloses that the first metal pattern 206A may be

formed using an existing mask for the first metal pattern 206B (dark green) and the same for second metal patterns 210A and 210B (blue), thus reducing the number of masks needed to form the capacitors. EX1001, 6:1-56. In addition, the 477 Patent states that capacitors 108 and 112 are coupled in parallel to each other and may be collectively viewed as the storage capacitor of pixel 100 "whose capacitance is equal to the sum of the capacitance of both capacitors 108 and 112" such that capacitor 112, is coupled between the gate of transistor 102 and the cathode 220 of the EL element 110. *Id.*, 5:18-32. EX1002, ¶40.

In the second area, area B, the 477 Patent discloses a first metal pattern 206B (dark green), which serves as the gate of the transistor 102, and is formed over a polysilicon pattern 202B (i.e., semiconductor layer) (purple), which with appropriate doping allows the formation of the source and drain, and channel region of transistor 102, with a gate oxide layer 204 in between. EX1001, 5:43-6:12; Fig. 2. The source of transistor 102 is coupled to power supply voltage V_{DD} and the drain is connected to drive the EL element 110. *Id.*, 4:56-5:17. Second metal pattern 210B provides contact between polysilicon pattern 202B to the indium tin oxide ("ITO") pattern 214C of the OLED element 110. *Id.*, Fig. 2. Second metal pattern 210B is formed by depositing a layer of metal over ILD 208 and patterned, where the second metal pattern 210B contacts polysilicon pattern

202B through a via hole in ILD 208 and gate oxide 204. *Id.*, 5:50-55; Fig. 2.

EX1002, ¶41.

In the third area, area C, the 477 Patent discloses an EL element 110 that includes an indium tin oxide ("ITO") pattern 214C (i.e., the anode) (light blue) formed under a capping layer SiN 216 (pink), which is formed under an organic layer 218, which is formed under a third metal layer 220 (i.e., the cathode) (orange). EX1001, 5:11-17;5:43-6:12; EX1002, ¶42.

The 477 Patent includes various embodiments where the first storage capacitor 108 and the second storage capacitor 112 comprise different combinations of insulation and conductive layers. *Id.*, Figs. 3-9, 11; EX1002, ¶43.

B. Overview of the File History

The 477 Patent issued from U.S. Patent Application No. 13/031,712 filed on February 22, 2011, and contains a claim of priority to U.S. patent Application No. 11/005,648, which was filed on December 7, 2004. Ex. 1001, Patent Face.

In an Office Action dated August 31, 2011, original claim one was rejected over Koo (EX1011, 2003/01170591) in view of Murade (EX1012, 6,610,997). *See* EX1005, 89-92. The Examiner found all limitations of original claim 1 disclosed in Koo except for the material composition of two layers, which materials it found would have been obvious design choices. *Id.*

In an Amendment dated December 27, 2011, applicant amended original claim one to include two additional limitations. See EX1005, 114-115. Applicant argued that Koo did not disclose the first limitation “wherein the first conductive layer over the first area is directly connected to a power supply voltage” because Koo’s first electrode 132 “is not directly connected” to Koo’s power supply voltage 147. *Id.*, 118 (emphasis in original). Applicant admitted that electrode 143 “is directly connected” to the power supply line 147 (which carries a power supply voltage). *Id.* Electrodes 132, 143 and 147 are shown in the annotated Figures 2B from Koo below.

FIG. 2B

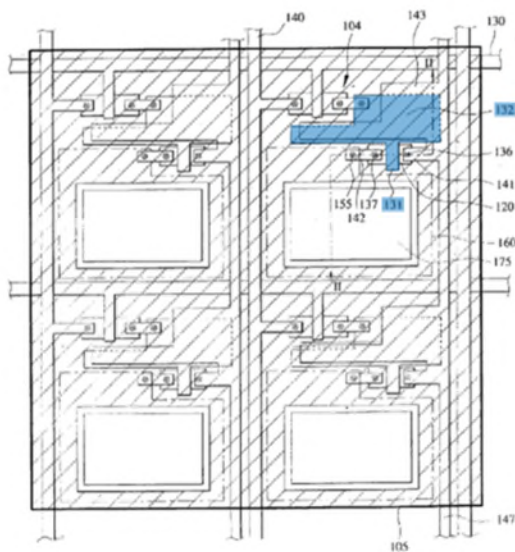
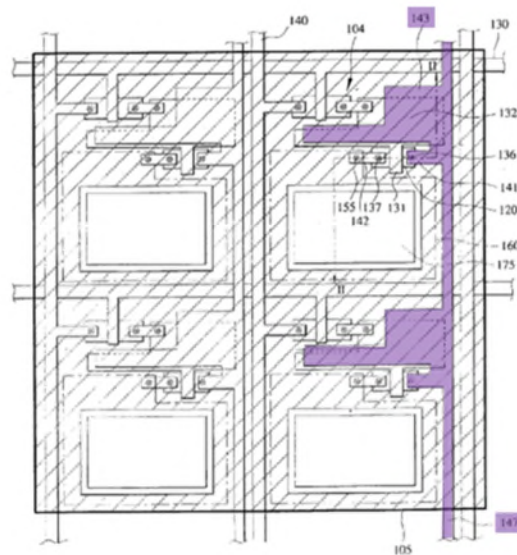


FIG. 2B



Koo's first electrode 132 (not directly connected to 147) and Koo's electrode 143 (admittedly directly connected to 147) are the two electrodes of Koo's storage capacitor. EX1011, Fig 2B, [0039].

Applicant also argued that Koo did not disclose the second limitation "wherein the second conductive layer is electrically connected to the fourth conductive layer" because Koo's second electrode 143 "is not electrically connected" to Koo's gate electrode 131. EX1005, 117-119. Koo's gate electrode 131 is formed of the same metal as Koo's electrode 132 as shown in the annotated Fig 2B above. And as shown above, Koo's electrode 143 is the other electrode of Koo's storage capacitor.

Based on these amendments and remarks, the Examiner allowed the claims. EX1005,136 ("See the Remarks filed December 27, 2011").

C. Person of Ordinary Skill in the Art

A person of ordinary skill in the art ("POSITA") at the time of the alleged invention of the 477 patent (December 7, 2004) would have had a Bachelors' degree in electrical engineering or a comparable field of study, plus approximately two to three years of professional experience with electronic and optoelectronic device design. Additional graduate education could substitute for professional experience, and significant experience in the field could substitute for formal education. EX1002, ¶¶34-37.

D. Claim Construction Under 37 C.F.R. § 42.104(b)(3)

The Challenged Claims are interpreted using the same claim construction standard that is used to construe the claim in a civil action in federal district court. 37 C.F.R. § 42.100(b).

Because the prior art asserted herein discloses the preferred embodiment within the indisputable scope of the claims, the Board need not construe the outer bounds of the claims as part of these proceedings. The district court may have to address other bounds of the claims in addressing infringement. *See, e.g., Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)) (providing that only those terms that are in controversy need be construed, and only to the extent necessary to resolve the controversy).

All the claim terms should be construed according to their plain and ordinary meaning to a POSITA at the time of the 477 patent.

IV. OVERVIEW OF THE PRIOR ART REFERENCES

A. EX1003 – Anzai

U.S. Patent 7,330,168 (“Anzai”) was filed on April 30, 2003, issued February 12, 2008, and claims priority to Japanese Patent Application 2002-128008, filed on April 30, 2002. EX1003, Face of the Patent. Anzai qualifies as prior art to the 477 Patent under at least pre-AIA 35 U.S.C. § 102 (e).

B. EX1004 – Yamazaki

U.S. Patent 6,992,332 (“Yamazaki”) was filed on May 5, 2003, issued on January 31, 2006, and claims priority to Japanese patent application 2002-13994. EX1004, Face of the Patent. Yamazaki qualifies as prior art to the 477 Patent under at least pre-AIA 35 U.S.C. § 102 (e).

C. EX1013 – Yamada

U.S. Patent 6,246,179 (“Yamada”) issued on June 12, 2001. Yamada qualifies as prior art to the 477 Patent under at least pre-AIA 35 U.S.C. § 102 (b).

D. Analogous Art

Anzai, Yamazaki and Yamada are analogous art to the 477 patent because they are in the field of electroluminescence devices that include storage capacitors and methods for forming same. EX1001, 1:15-20; EX1002, ¶¶55-56.

V. GROUND 1: CLAIMS 1 AND 3 ARE RENDERED OBVIOUS BY ANZAI

A. Claim 1

1. [1pre]

To the extent that the preamble is limiting, Anzai teaches “[a] method for forming a pixel (pixel 115) of an electroluminescence device.” Anzai is directed to a method of forming electroluminescent (“EL”) display devices comprising a plurality of pixels 115. EX1003, Fig. 1 (pixel 115), 1:6-17. More particularly, for each pixel, Anzai is directed to reducing the forming area of a storage capacitor for

holding the video signal supplied to a transistor to improve the display quality of an electroluminescent display device. *Id.*, Abstract. Anzai discloses the methods of forming the pixels including depositing the layers of the OLED, transistors, and capacitors. *See, e.g., id.*, 3:56-67, 5:14-33 (forming OLED layers), 4:1-24, 4:52-5:2 (forming transistor layers), 4:25-51, 5:44-6:9 (forming capacitor layers), in accordance with each of the claim limitations as further discussed below. EX1002, ¶58.

2. [1a]

Anzai discloses “providing a substrate (Anzai substrate 10).” Anzai discloses providing “an insulating substrate 10, which is either a substrate made of a glass, a synthetic resin, a conductive material or a semiconductor” on which the other layers or formed during manufacture. EX1003, 3:57-61; Figs. 2A-2B and 3A-3B; EX1002, ¶59.

FIG.2A

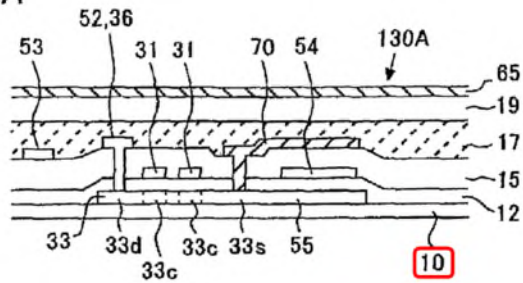
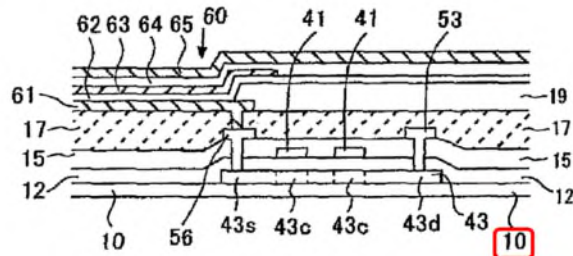
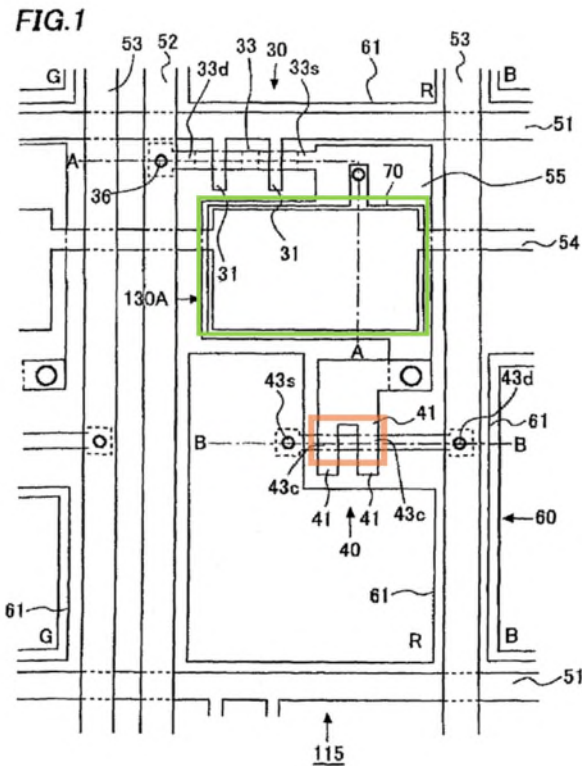


FIG.2B



3. [1b]

Anzai discloses “defining at least a first area (**Capacitor Area**) for capacitors (130A, 130B) and a second area (**Transistor Area**) for a transistor (driving transistor 40) on the substrate (substrate 10) (see [1c]-[1k], [1n]-[1p]).” Anzai discloses a plurality of pixel portions 115, disposed in a matrix configuration forming a display region. EX1003, 3:28-31; Fig. 1; EX1002, ¶60.



Anzai teaches defining at least a first area (Capacitor Area) for multi-layer capacitor 130A and a second area (Transistor Area) for driving transistor 40 on the substrate. *Id.*, 3:32-40; Figs. 2A-2B; EX1002, ¶61.

FIG. 2A

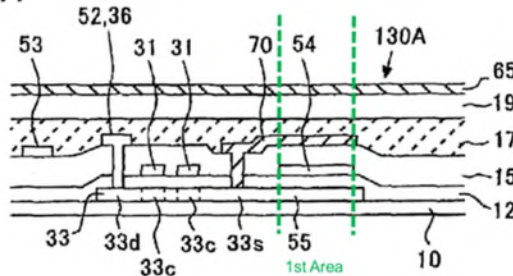
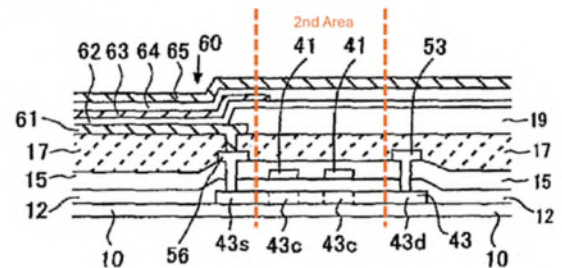


FIG. 2B



Anzai also teaches defining a third (unclaimed in claim 1 but claimed in claim 3) area for “a light emitting device (organic EL element 60), with an anode

layer 61, an emissive layer 63, and a cathode layer 65. EX1003, Fig. 1, 5:3-33; EX1002, ¶62.

Anzai teaches “defining” these areas “for” the circuit elements as claimed because it teaches the **Capacitor Area** of the substrate is used for forming the capacitors exclusive of any transistors or OLED (see [1c]-[1h], [1n]-[1o] (forming both capacitors over the first area without a transistor)), the **Transistor Area** of the substrate is used for forming the transistor, exclusive of any capacitors or OLED. See [1i]-[1k], [1p] (forming transistor 41 over the second area), and the third area of the substrate is used for forming the OLED, exclusive of any transistors or capacitors (see [3p]-[3q]). EX1002, ¶63.

Anzai teaches that defining the areas of the substrate is important for a bottom emission type organic EL display device of the type disclosed in Anzai because the organic element 60 emits light through the substrate. EX1003, 2:19-33, 5:29-33 (explaining light is emitted from EL element 60 through transparent anode 61 and substrate 10). In a bottom emission type device like Anzai, the capacitor serves as a “blind” leading to a decreased “open aperture.” *Id.*, 2:19-33. Thus, Anzai teaches using multi-layer capacitors in a single defined area of the substrate to achieve increased capacitance while minimizing that “blind” area. *Id.*; see also, *id.*, 4:41-47. This is the same reason provided in the 477 patent for defining the areas of the substrate and stacking the capacitors in a single exclusive area. A

POSITA would have understood that common elements of the claimed circuit elements can extend into multiple areas. For example, the cathode layer in Anzai and the 477 patent extends over the entire pixel area and serves in the third defined area as part of the light emitting element and in the first defined area as part of a capacitor, but the light emitting element and the capacitors are exclusively in their respective defined areas. In contrast, Anzai teaches that for top emission devices, the capacitor area need not be so defined. EX1003, 2:14-19; EX1002, ¶64.

A POSITA also would have known that for bottom-type emission devices, it was desirable to define different areas for the OLED and transistors because light from the OLEDs would cause leakage in the transistor. *See, e.g.*, EX1013, Figs. 4, 8, 2:31-35 (discussing known problem), 11:34-40 (discussing solution of shielding layer and offset transistors); EX1002, ¶65.

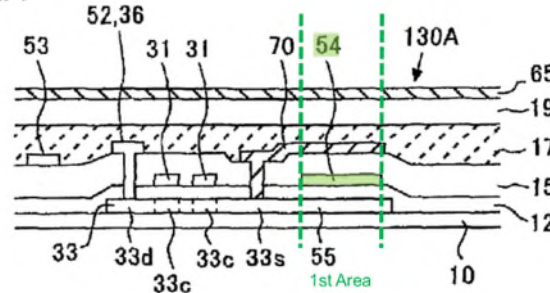
In the alternative, it would have been obvious over Anzai to perform the step of defining a first area (**Capacitor Area**) for the capacitors and a second area (**Transistor Area**) for the driving transistor as claimed. Anzai's stacked capacitors include the lowest layer on top of the substrate (layer 55) and each conductive and dielectric layer up to and including the top layer (cathode 65). Anzai's driving transistor is a TFT that requires a semiconductor layer, gate oxide layer, and gate layer. Accordingly, a POSITA would have had to choose between adding additional layers to overlap these components in the same area or defining different

areas for them. It would have been obvious to a POSITA that Anzai's final design was not the result of mere happenstance or luck, but the result of a conscious design choice to define different areas for the components as claimed in order to avoid the need to add additional layers. EX1002, ¶66.

4. [1c]

Anzai discloses “forming a first conductive layer (electrode layer 54) over the first area (Capacitor Area) (see [1n]).” Anzai discloses forming electrode layer 54 as a first conductive layer for a capacitor made of chromium or molybdenum. EX1003, 4:30-32 (Cr or Mo); EX1002, ¶67.

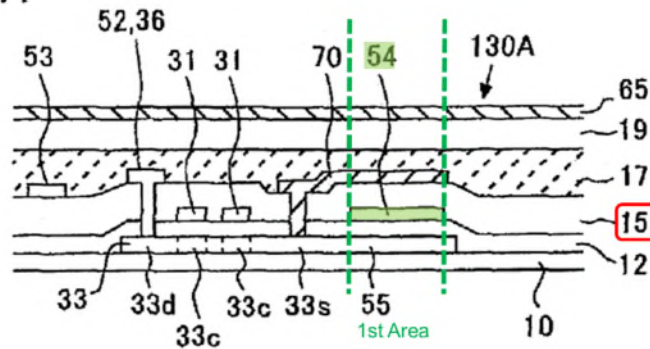
FIG.2A



5. [1d]

Anzai discloses “forming a first dielectric layer (interlayer insulating film 15) over the first conductive layer (electrode layer 54) over the first area (Capacitor Area) (see [1n]).” Anzai discloses forming interlayer insulating film 15 as a dielectric layer formed of a SiO₂ film, a SiN film and a SiO₂ film, sequentially deposited. *Id.*, 4:60-63; EX1002, ¶68.

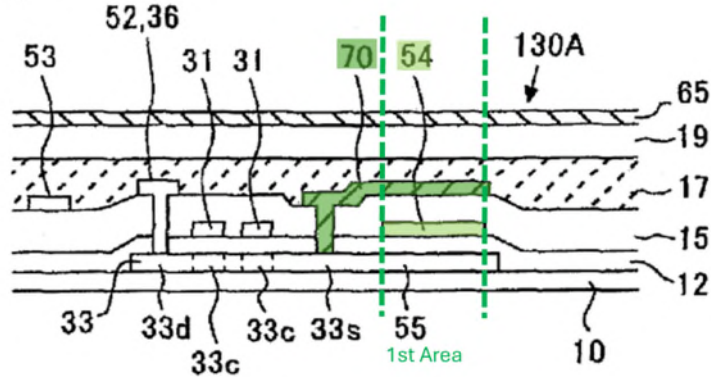
FIG.2A



6. [1e]

Anzai discloses “forming a second conductive layer (electrode layer 70) over the first dielectric layer (interlayer insulating film 15) over the first area (Capacitor Area) (see [1n]).” Anzai discloses forming electrode layer 70 in the same layer and using the same process as drain electrode 36 and drain signal line 52, which are made of conductive aluminum. EX1003, 4:13-14, 4:35-37; 4:44-45. Electrode layer 70 is formed as a capacitive layer extending over interlayer insulating film 15 and electrode layer 54. *Id.*; EX1002, ¶69.

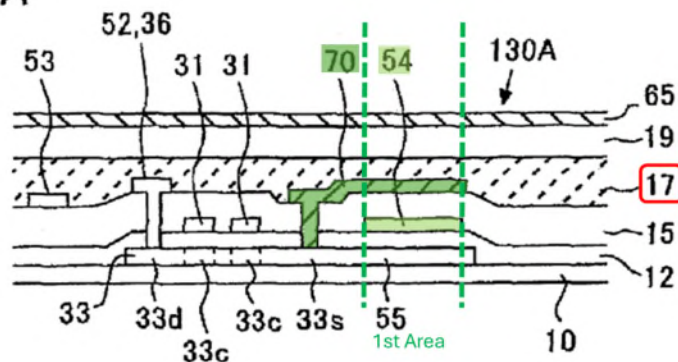
FIG.2A



7. [1f]

Anzai discloses “forming a second dielectric layer (planarization film 17) over the second conductive layer (electrode layer 70) over the first area (Capacitor Area) (see [1n]).” Anzai discloses forming a dielectric insulating layer comprising planarization film 17 over the electrode layer 70. *Id.*, Fig. 2A, 4:48-51, 5:62-67 (“In the first embodiment, a capacitance is formed between the third capacitance electrode layer 70 and the cathode layer 65 when the cathode electrode is used as a fourth capacitance electrode layer. Both the first planarization film 17 and the second planarization film 19 function as the capacitance insulating film in this configuration.”). Anzai discloses film 17 can be an organic resin, which a POSITA would have known is a dielectric. *Id.*, 4:23, 5:3-4. Additionally, Anzai’s teaching that planarization film 17 is a “capacitance insulating film” (*id.*, 5:62-67) discloses to a POSITA that it is a “dielectric layer” as claimed because it is insulating the electrodes of the capacitor so they can hold an electric charge. EX1002, ¶70.

FIG.2A

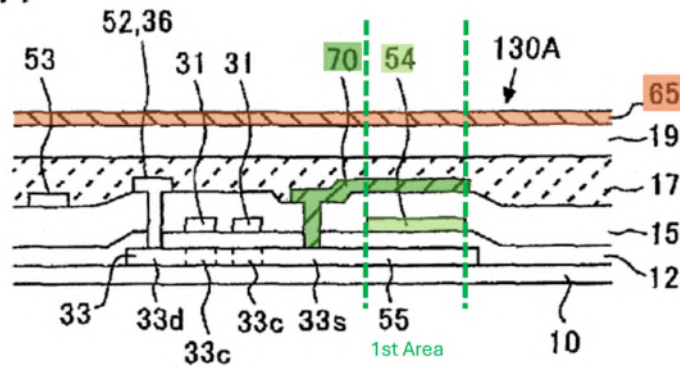


8. [1g]

Anzai discloses “forming a third conductive layer (cathode layer 65) over the second dielectric layer (film 17) over the first area (Capacitor Area) (see [1n]).”

Anzai discloses a cathode layer made of conductive magnesium-indium alloy, aluminum or aluminum alloy is formed over film 17. *Id.*, Fig. 2A, 4:48-51, 5:23-25, 5:62-67; EX1002, ¶71.

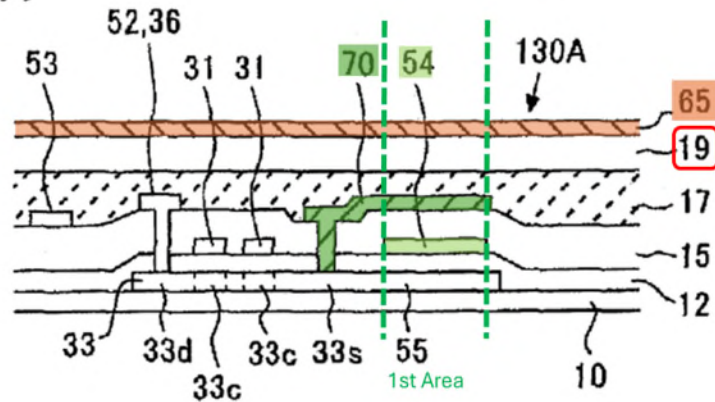
FIG. 2A



9. [1h]

Anzai renders obvious “forming a layer of capping silicon nitride (layer 19) between the second dielectric layer (film 17) and the third conductive layer (cathode layer 65) over the first area (Capacitor Area) (see [1n]).” Anzai discloses forming film 19 between film 17 and cathode 65. EX1003, 5:44-6:9; EX1002, ¶72.

FIG. 2A



A POSITA would have understood that film 19 is “a layer of capping” material relative to film 17. EX1003, 5:44-6:9. The first film 17 is formed over the entire surface for flattening, which will protect the semiconductor surface from the surrounding environment, in addition to being a dielectric layer as shown above. EX1003, 4:17-24, 5:3-13. A POSITA would have further understood that film 19 is then further disposed on film 17, capping film 17. EX1001, Figs. 2A-B, 5:3-13; EX1002, ¶¶73-77.

The Board should reject any attempt by PO to narrowly construe a “layer of capping” material to exclude the relationship between film 19 and film 17. The 477 patent provides no special meaning for a layer of “capping” material. In fact, the 477 patent discloses silicon nitride (SiN) as the sole example for both a layer of “capping” material and the passivation layer that is capped. For the passivation layer of the second dielectric layer, the 477 patent states: “A layer of passivation silicon nitride (SiN) 212 is formed over ILD208 and second metal patterns 210A

and 210B.” EX1001, 5:55-57. The 477 patent then states: “A layer of capping SiN 216 is disposed to cover passivation SiN 212 and ITO pattern 214C.” *Id.*, 5:61-63. A POSITA would have understood from the 477 patent that there is no special meaning ascribed to a layer of “capping” material other than its normal meaning of a layer of material that is on top of, or caps, another. Moreover, given that the sole example in the 477 patent is SiN for both layers, a POSITA would have understood these two layers need not be made of different materials. As such, a POSITA would have understood that Anzai’s film 19 is a layer of capping material for film 17. EX1002, ¶78.

Anzai also teaches layer 19 is “a layer of capping” material for the additional reason that Anzai discloses layer 19 caps film 17 and a portion of anode 61. EX1003, Fig. 2B (showing film 19 over portion of anode 61). Similarly, Anzai teaches layer 19 caps film 17, a portion of anode 61, and electrode 71 in the second embodiment. *Id.*, Figs. 3A-3B. Anzai explains that the second embodiment is a slight modification of the first embodiment, with the only change being the addition of electrode 71. *Id.*, EX1003, 5:34-43; EX1002, ¶79.

Anzai renders obvious that film 19 is “silicon nitride” (SiN). Anzai does not explicitly state what material(s) are used to form layer 19. Thus, a POSITA would have been motivated to investigate an appropriate material, including by reviewing other relevant teachings within Anzai. Anzai discloses that layer 19 functions as a

capacitance insulating film. *Id.*, 5:62-6:9. Anzai expressly discloses that silicon nitride (SiN) can be used as a capacitance insulating film by disclosing that SiN is a material used in the interlayer insulating film 15 that is between second capacitance **electrode layer 54** and third capacitance **electrode layer 70** of storage capacitance element 130, and in the gate insulating film 12 between first and second capacitance electrode layers 55 and 54. *Id.*, 3:49-51, 4:8-10, 4:17-24, 4:26-30, 4:33-36, and 4:40-47. Thus, a POSITA investigating what material to use for capacitance insulating layer 19 would have seen Anzai's express teaching that SiN could be used for a capacitance insulating layer, rendering SiN an obvious choice. A POSITA would have had a reasonable expectation of success in using SiN as an insulating material as taught by Anzai and as known in the art. EX1002, ¶80.

The intrinsic record confirms SiN would have been an obvious material to use such that this claim is obvious over Anzai alone. During prosecution, original claim 1 was rejected over Koo in view of Murade with the Examiner finding Koo disclosed all limitations except for the materials used for Koo's capping layer 170 and gate insulating layer. EX1005, 90-91. What the Examiner found to be "capping layer 170" in Koo is disclosed in Koo as "flattening film 170."¹ EX1011, Fig. 3;

¹ This unchallenged finding in the intrinsic record is also additional evidence that "capping" is not entitled to a special meaning that might distinguish layer 19.

EX1003, Fig. 2A. Moreover, flattening film 170 in Koo, like film 19 in Anzai, is the topmost insulating layer, immediately below the cathode. *Id.* The Examiner found it would have been obvious “to form the capping layer and gate insulation layer of Koo utilizing silicon nitride and gate oxide, respectively, as taught by Murade to increase the capacity of the capacitor and insulating the semiconductor layer.” EX1005, 91. The Examiner went on to hold that “it has been held to be within the general skill of a worker in the art to select a known material, i.e., silicon nitride and oxide, on the basis of [its] suitability for the intended use as a matter of obvious design choice.” *Id.*, 92 (citing *In re Leshin*, 125 USPQ 416.). Applicant did not challenge that finding. Instead, Applicant amended claim 1 to add other, unrelated limitations and argued those new limitations overcame the combination of Koo and Murade. EX1005, 113-119. Thus, the intrinsic record, including the Examiner’s finding, applicant’s acquiescence, and the Murade reference, confirms silicon nitride is an obvious material to use for insulating layer 19 and that a POSITA would have had a reasonable expectation of success in using that material for that type of layer. EX1002, ¶81.

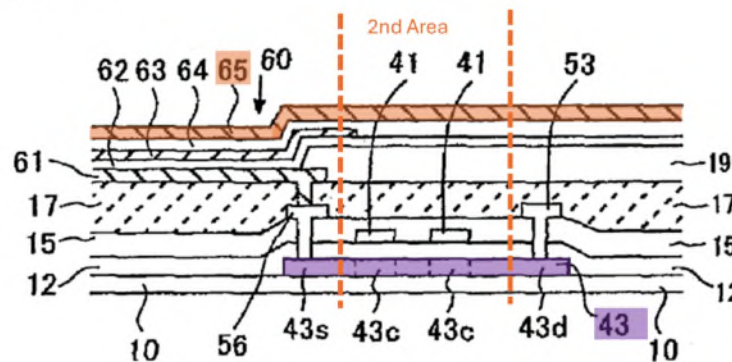
As explained by Dr. Neikirk, it was well known in the art to use a nitride layer as a capping layer. EX1002, ¶¶75-77 (discussing additional analogous examples in the art such as EX1006, EX1007, EX1008, EX1009, EX1014, EX1015).

PO may raise the irrelevant point that it also would have been obvious to use an organic resin for layer 19, since Anzai teaches the use of that material for layer 17. EX1003, 5:3-5. This argument should be rejected for at least two reasons. First, the only relevant question is whether the claimed SiN material would have been obvious—it need not be the only obvious choice or the best of multiple choices. Second, a POSITA would have known that organic materials usually have lower dielectric constants than inorganic materials such as SiN, and a higher dielectric constant is desirable for the insulator in a capacitor since that leads to a higher capacitance per unit area. That then allows a reduced area storage capacitance element, one of the objectives of Anzai. EX1003, Abstract (“The forming area of the storage capacitance element for holding the video signal supplied to the gate of the driving transistor can be thus reduced, improving display quality as well as extending life span of the organic El element.”). This fact is supported by the Examiner’s finding during prosecution that a POSITA would have been motivated to use SiN to “increase the capacity of the capacitor.” EX1005 (8/31/2011), 91. Therefore, a POSITA would have been motivated to use SiN with a higher dielectric constant for film 19, especially if film 17 is an organic resin with a lower dielectric constant. EX1002, ¶82.

10. [1i]

Anzai discloses “forming a semiconductor layer (active layer 43) over the second area (Transistor Area) (see [1o]).” Anzai discloses forming active layer 43 over the substrate 10 using an amorphous silicon film irradiated by a laser beam forming a poly-crystalline silicon film. EX1003, 4:52-56; Fig. 2B. Source 43s and drain 43d are formed at both sides of the channels 43c in active layer 43. *Id.*, 4:58-60. Accordingly, a POSITA would have understood active layer 43 to be a semiconductor layer. EX1002, ¶83.

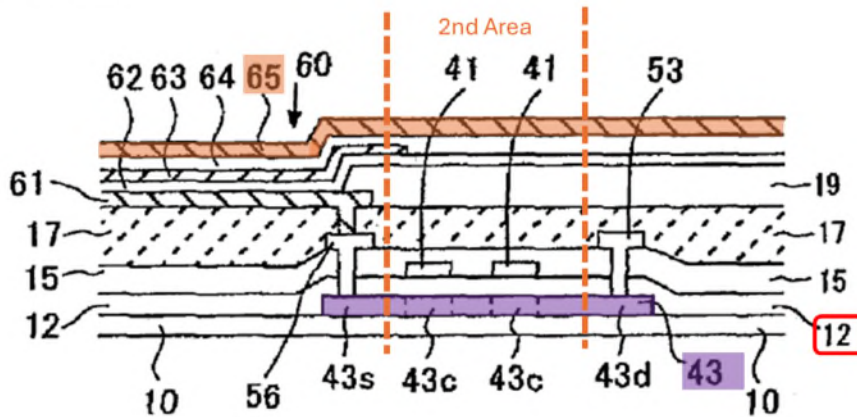
FIG.2B



11. [1j]

Anzai discloses “forming a gate oxide layer (gate insulating film 12) over the second area (Transistor Area) (see [1o]).” Anzai discloses forming gate insulating film 12 over the active layer 43 and the second area using single or multiple layers of SiO₂ (an oxide) and SiN film. EX1003, 4:8-10, 4:56 (gate insulating film 12 deposited on active layer 43); Fig. 2B; EX1002, ¶84.

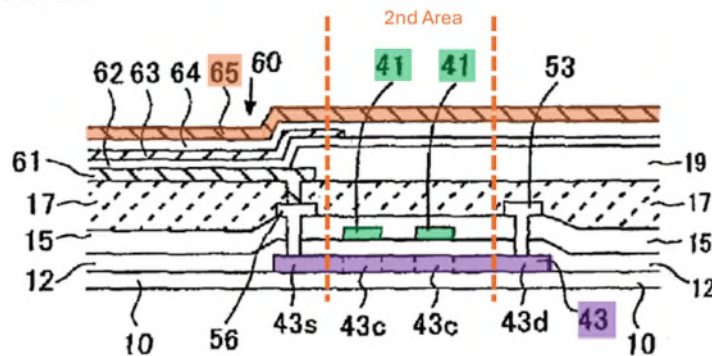
FIG.2B



12. [1k]

Anzai discloses “forming a fourth conductive layer (gate electrode 41) over the gate oxide layer (gate insulating film 12) over the second area (Transistor Area) (see [1o]).” Anzai discloses forming gate electrode 41 out of conductive “metal with a high-melting point such as Cr and Mo” and over the gate insulating film 12 and the second area. EX1003, 4:56-58; Fig. 2B; EX1002, ¶85.

FIG.2B

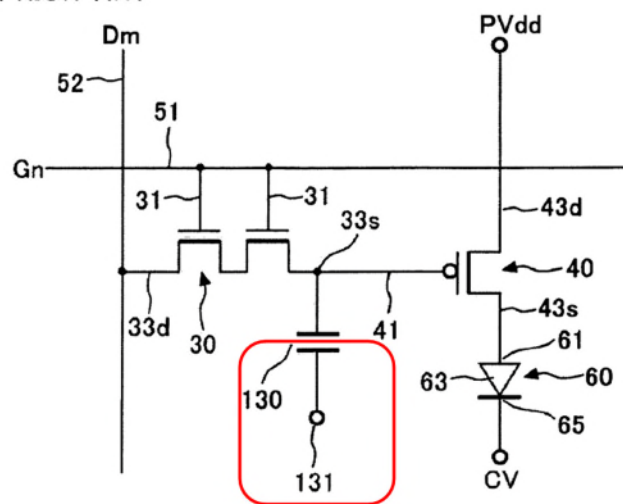


13. [11]

Anzai discloses “wherein the first conductive layer (electrode layer 54) over the first area (Capacitor Area) is directly connected to a power supply voltage (a predetermined stable voltage, PV_{dd} , CV).” Anzai teaches that the first capacitor comprises electrode layer 54 and electrode 70. See [1n]. Anzai also teaches that the invention uses the equivalent circuit diagram of Figure 4. EX1003, 3:26-27; Fig. 4. And with respect to Figure 4, Anzai teaches that the storage capacitor 130 comprises 1) a first electrode that is connected to the gate 41 of the driving transistor 40 and 2) a second “storage capacitance electrode 131,” which is disposed to hold the electric charge for one period. *Id.*, Fig. 4, 1:44-48. Anzai then teaches that storage capacitance electrode 131 is “provided with a predetermined stable voltage.” *Id.*, 2:1-2; EX1002, ¶86.

FIG.4

PRIOR ART



In the context of the first embodiment, capacitor electrode 70/55 is connected to the gate 41 of the driving transistor 40. *See* [1m]. Thus, a POSITA would have understood from Anzai that capacitor electrode 54 is the other electrode of capacitor 131, i.e., the storage capacitance electrode 131 that is “provided with a predetermined stable voltage.” EX1002, ¶87.

A POSITA would have understood Anzai’s teaching that the electrode is “provided with a predetermined stable voltage” to mean that electrode is “directly connected to a voltage power supply.” A storage capacitor in a pixel circuit like Anzai holds a desired charge on the gate of the driving transistor to ensure the desired amount of current flows through the driving transistor and OLED to create the desired amount of light. The desired charge is supplied through the switching transistor to the first electrode (70/55) of the capacitor and Anzai discloses to a POSITA that the desired charge is held by the capacitor because the other electrode (54) of the capacitor is “provided with a predetermined stable voltage.” If the voltage on electrode 54 were changed the charge held by capacitor 130 would change, which would defeat the disclosed function of Anzai’s storage capacitor. Thus, a POSITA would have understood that Anzai’s teaching to provide a “predetermined stable voltage” to electrode 131 to render obvious directly connecting a “voltage power supply” at that electrode. EX1002, ¶88.

In the alternative, it would have been obvious to modify Anzai to connect electrode 54 directly to PVdd or CV. Anzai does not specify which predetermined stable voltage should be supplied to the electrode, so a POSITA would have been motivated to investigate an appropriate predetermined stable voltage and how to apply it to electrode 54. Anzai teaches each pixel already has two voltage power supplies, “plus source voltage PVdd” applied to the drain of the driving transistor and “minus source voltage CV” applied to the cathode 65. EX1003, Figs. 1, 4, 1:27-43. Each of those is a voltage power supply. EX1002, ¶89.

A POSITA would have been motivated to use one of those voltage power supplies to avoid the unnecessary complexity and cost of creating a third voltage power supply and routing that to each pixel. A POSITA would have known how to directly connect electrode 54 to those voltage power supplies. For example, a POSITA would have known that electrode 53 and cathode 65 were directly connected to their voltage power supplies PVdd and CV, respectively, on the periphery of the display and that electrode 54 could have been directly connected to PVdd or CV on the periphery of the display in the same way, since Figure 1 shows electrode 54 extending horizontally across all pixels. As an additional example, as shown in Figures 1 and 4, PVdd is supplied on line 53, which crosses electrode 54, and a POSITA would have known electrode 54 could be directly connected to PVdd where these lines cross. A POSITA would have known how to

form such direct connections. EX1003, 4:63-67 (line 53 connected to driving transistor 40 by creating a contact hole and filling it with aluminum). EX1002, ¶90.

A POSITA would have had a reasonable expectation of success in making the modification as making such direct connections within a pixel is well within a POSITA's knowledge and expertise. EX1002, ¶91.

14. [1m]

Anzai discloses “wherein the second conductive layer (electrode layer 70) is electrically connected to the fourth conductive layer (gate electrode 41).” Anzai discloses that electrode layer 70 is connected to source 33s through a via as shown in Figure 2A-B; EX1002, ¶92.

FIG.2A

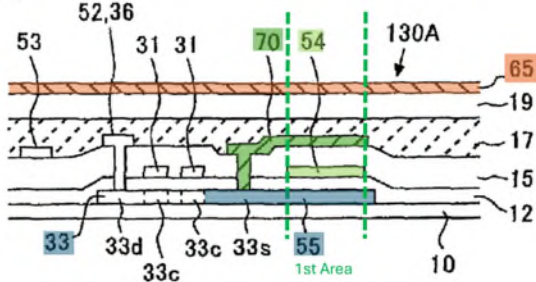
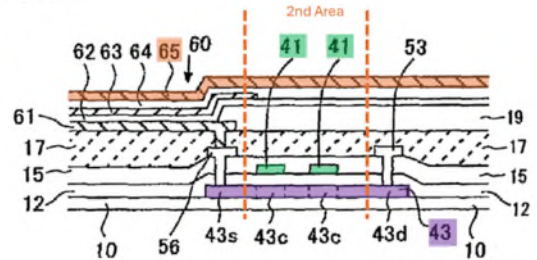


FIG.2B

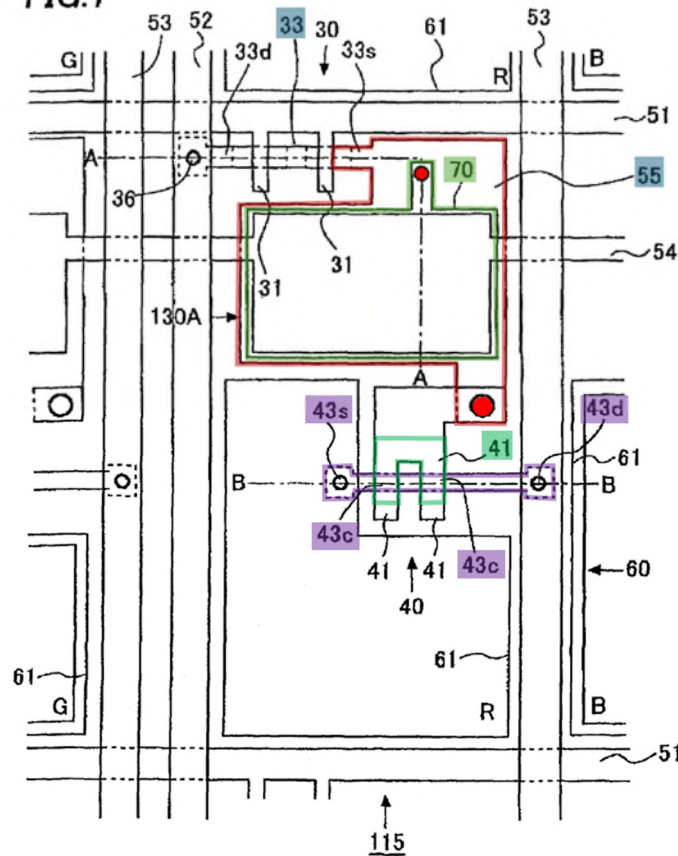


EX1003, Figs. 2A-B, 4:37-39 (“The third capacitance electrode layer 70 is connected to the source 33s of the TFT 30 through a contact hole.”). Anzai also teaches source 33s of the switching transistor is electrode layer 55 and is connected to the gate electrode 41. *Id.*, Fig. 2A-B, 3:42-44 (“A source 33s of the TFT 30 works also as a first capacitance electrode layer 55 and is connected to a gate 41 of the TFT 40”). Anzai also discloses this with respect to Figure 4 where it shows the

[illegible]

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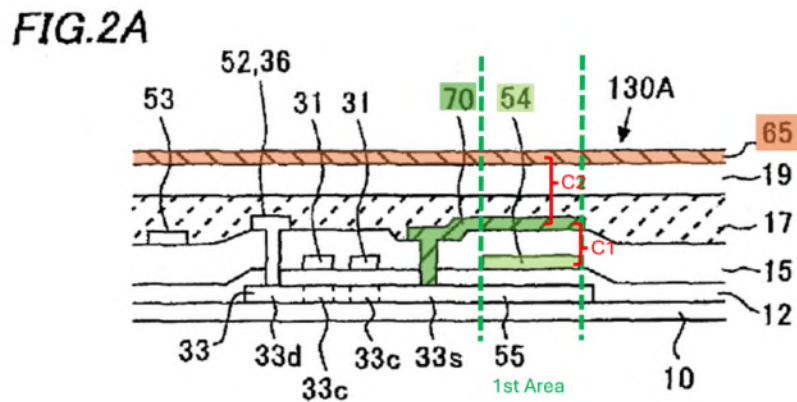
FIG. 1



15. [1n]

Anzai discloses “wherein the first conductive layer (**electrode layer 54**), the first dielectric layer (interlayer insulating film 15), and the second conductive layer (**electrode layer 70**) over the first area (**Capacitor Area**) collectively form a first one of the capacitors (layers 54, 15, 70) over the first area (**Capacitor Area**) the second conductive layer (**electrode layer 70**), the second dielectric layer (planarization film 17), and the third conductive layer (**cathode layer 65**) over the first area (**Capacitor Area**) collectively form a second one of the capacitors (layers 70, 17, 19, 65) over the first area (**Capacitor Area**).” EX1002, ¶95.

As seen in Fig. 2A below, Anzai discloses a first embodiment having the first capacitor within the first area that includes electrode layer 54 and electrode layer 70 with insulating film 15 sandwiched in between. EX1003, Fig. 2A, 4:25-47. Electrode layer 54 is formed over gate insulating film 12, which Anzai discloses can be made from “a SiO₂ film” (i.e., an oxide layer). *Id.*, 3:61-67; Fig. 2A. EX1002, ¶96.



Claim 1 is an open ended “comprising” claim, thus, a device with the claimed capacitors including the claimed layer practices the claims even if the device includes additional capacitors and the capacitor included additional layers. Anzai’s electrode layer 55 providing additional capacitance storage relative to electrode layer 54 is simply such an additional element. EX1002, ¶97.

The second capacitor is formed between electrode layer 70 and cathode layer 65 with an insulating layer comprising first planarization film 17 (and film 19). EX1003, Fig. 2A, 4:48-51, 5:62-67 (“In the first embodiment, a capacitance is

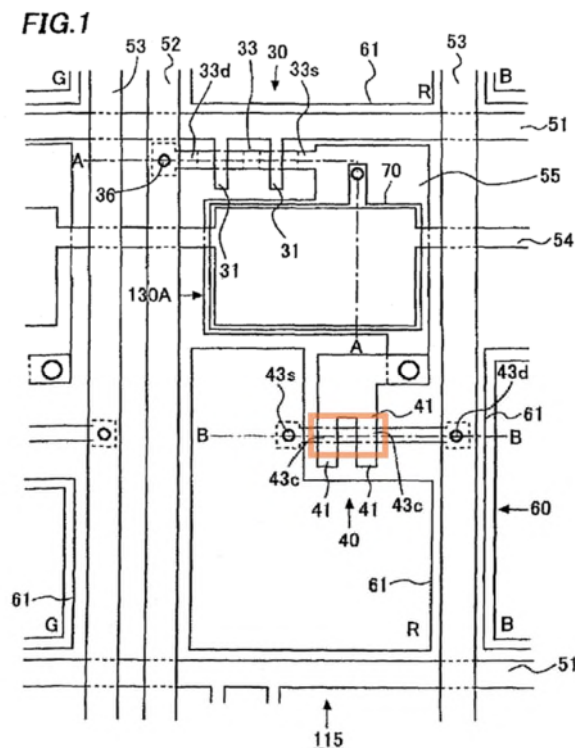
formed between the third capacitance **electrode layer 70** and the **cathode layer 65** when the cathode electrode is used as a fourth capacitance electrode layer. Both the first planarization film 17 and the second planarization film 19 function as the capacitance insulating film in this configuration.”). Again, the fact that Anzai discloses additional intervening capping layer 19 is not relevant to this limitation [1n] and, in fact, the intervening capping layer required by the claim by limitation [1h] (requiring intervening capping layer). EX1002, ¶98.

Anzai discloses that each of the above identified first and second capacitors functions as a capacitor. EX1003, 4:30-47 (first capacitor), 4:48-51 and 5:58-65 (second capacitor). Anzai further discloses that interlayer insulating film 15 is formed of a SiO₂ film, a SiN film and a SiO₂ film, sequentially deposited. *Id.*, 4:60-63. Both the first planarization film 17 and second planarization film 19 “function as the capacitance insulating film.” *Id.*, 5:65-67. A POSITA would have understood the first and second capacitors share a “second conductive layer” as recited in claim 1 since the **electrode layer 70** is common to both capacitors. EX1002, ¶99.

As explained by Dr. Neikirk, these types of two capacitor designs were well known in the prior art. EX1002, ¶¶100-102 (discussing examples in EX1008, EX1009, and EX1010).

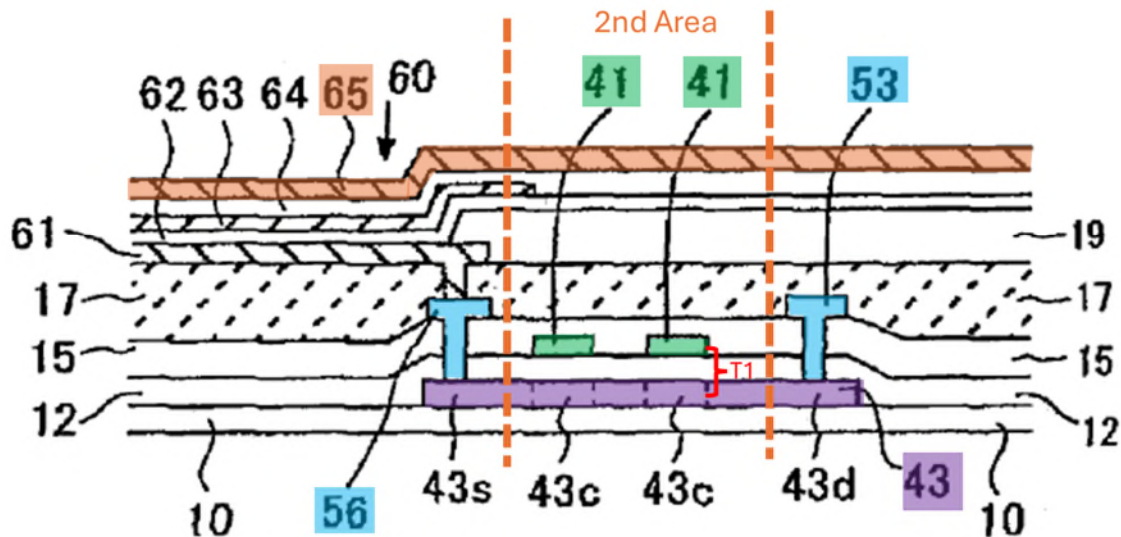
16. [1o]

Anzai discloses “the semiconductor layer (active layer 43), the gate oxide layer (gate insulating film 12), and the fourth conductive layer (gate electrode 41) over the second area (Transistor Area) collectively form a transistor (driving transistor 40).” EX1002, ¶103.



Anzai teaches that in the second, Transistor Area, as seen in Fig. 1 (see [1a]) and in Fig. 2B annotated below (e.g., on the left side of the orange dashed line), driving TFT 40 is formed by gate electrode 41 above active layer 43 with gate insulating film 12 in between. EX1003, Figs. 1 and 2B; 4:1-25 and 37-40. Driving Source Line 53 is connected to the drain 43d, and the anode layer 61 is connected to the source 43s, of the TFT 40. *Id.*; EX1002, ¶104.

FIG.2B



Anzai discloses the TFT is fabricated using sequentially deposited layers. *Id.* Anzai discloses depositing on substrate 10 an amorphous silicon film, which is re-crystallized to form a polycrystalline silicon film that functions as the active layer 43. *Id.*, 3:52-56, 4:52-56, 4:58-60; Figs. 1 and 2A-B. A single or multiple layers of SiO₂ and SiN are formed on layer 43 to serve as the gate insulating film 12. *Id.*, 4:8-10, 4:56. A gate electrode 41 is deposited on gate insulating film 12. *Id.*, 4:56-58; Fig. 2B. A POSITA would have understood the active layer 43 to be the first semiconductor layer, the insulating film 12 to be the gate oxide layer that is deposited over the first semiconductor layer, and the gate electrode 41 to be the fourth conductive layer. EX1002, ¶105.

B. Claim 3

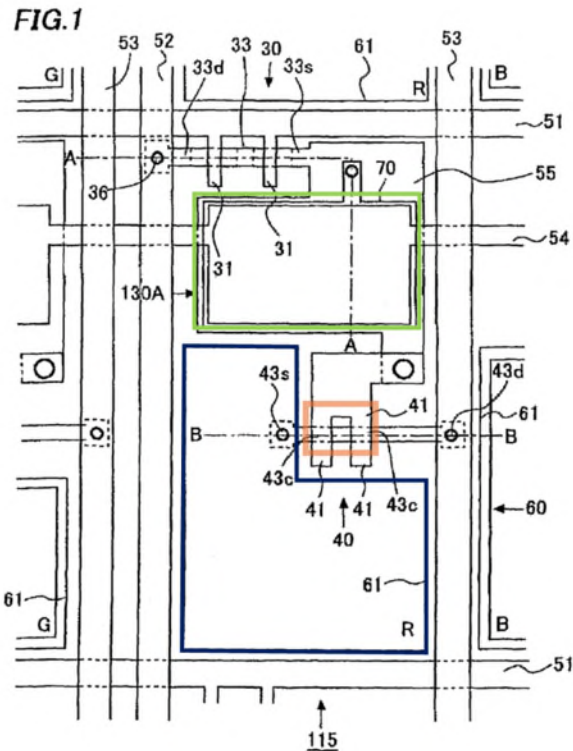
The showing for claim 3 relies primarily on the showing for claim 1, with two main differences. First, claim 3 adds limitations related to the OLED area, which are addressed below. Second, the limitations in claim 3 related to the second conductive layer and second dielectric layer in the second capacitor map to Anzai's layers 71 and 19, respectively, in Anzai's second embodiment. Anzai discloses the second embodiment is identical to the first embodiment in all other respects. EX1003, 5:34-51; EX1002, ¶106.

1. [3pre]-[3a]

See [1pre]-[1a]; EX1002, ¶107.

2. [3b]

Anzia discloses “defining at least a first area for capacitors (*see* [1b]), a second area for a transistor on the substrate (*see* [1b]) and a third area (OLED Area) for an organic light-emitting diode (OLED) on the substrate.” See [1b] (first capacitor and second transistor areas); Anzai discloses third area for an OLED (organic EL element 60) on the substrate as shown in annotated figure 1 below. EX1002, ¶108.



Anzai teaches, or in the alternative renders obvious, defining these areas for these components as shown above for [1b]. EX1002, ¶109.

3. [3c]-[3d]

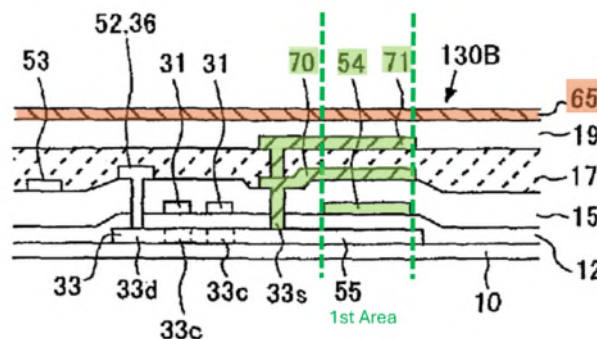
See [1c] (first conductive layer 54)-[1d](first dielectric layer 15); EX1002, ¶110.

4. [3e]

Anzai discloses “forming a second conductive layer (combined **electrode layer 70/71**) over the first dielectric layer (interlayer insulating film 15) over the first area (**Capacitor Area**) (see [3t]).” Anzai discloses the embodiment of Fig. 3A is the same as that of Fig. 2A except for the electrode structure that adds electrode layer 71 to form “storage capacitive element 130B.” EX1003, 5:39-41. A POSITA

would have understood that electrode layer 71 extends over and is electrically connected to electrode layer 70 (i.e., electrode layers 70 and 71 form a U-shaped conductive layer that is shared between the first and second capacitors) in the Capacitor Area. It is appropriate to consider this combined electrode layer 70/71 to be “a second conductive layer” as claimed because the intrinsic record of the 477 patent reflects that one layer can consist of multiple layers. EX1001, 4:8-10 (layer 12 may be formed using “multiple layers” of films), 4:17-18 (layer 15 may be multiple films), U.S. Pat. No. 7,586,121 at claims 1, 3, 6 (parent patent claiming a dielectric layer comprises a passivation silicon nitride layer and an organic layer). Additionally, a POSITA would have understood from Anzai’s disclosures that electrode 70 and 71 a) are at the same potential as set by the switching transistor 30, b) would have covered substantially the same Capacitor Area, c) have only dielectric layer 17 between them, and d) are explicitly taught by Anzai to be part of the same “electrode structure” and “storage capacitive element 130B.” EX1003, Fig., 1, 3A, 5:5:34-6:9; EX1002, ¶111.

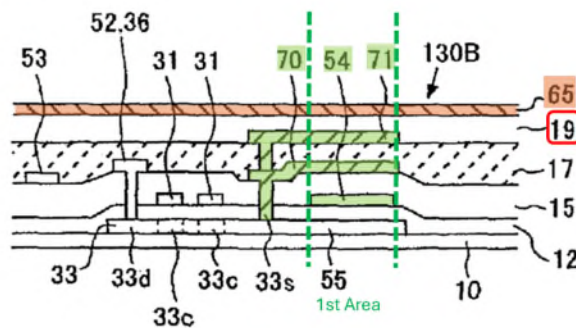
FIG.3A



5. [3f]

Anzai discloses “forming a second dielectric layer (film 19) over the second conductive layer (electrode layer 70/71) over the first area (Capacitor Area) (see [1n]).” Anzai discloses forming film 19 as a capacitor insulating layer over the electrode layer 70/71. *Id.*, Fig. 3A, 5:62-6:9. Anzai’s teaching that film 19 is a “capacitance insulating film” (*id.*, 5:62-6:9) discloses to a POSITA that it is a “dielectric layer” as claimed because it is insulating the electrodes of the capacitor so they can hold an electric charge. EX1002, ¶112.

FIG.3A



6. [3g]

See [1g] (third conductive layer 65); EX1002, ¶113.

7. [3h]

See [1i] (semiconductor layer 43); EX1002, ¶114.

8. [3i]

See [1j] (gate oxide layer 12); EX1002, ¶115.

9. [3j]

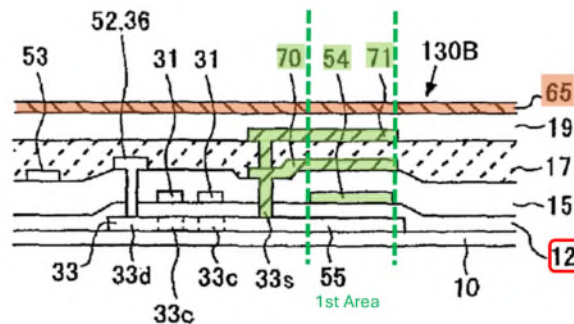
See [1k] (fourth conductive layer 41); EX1002, ¶116.

10. [3k]

Anzai discloses “forming the gate oxide (layer 12) over the first area (Capacitor Area).” Anzai discloses forming layer 12 over the Capacitor Area.

EX1003, Fig. 3A, 4:8-10, 4:17-20, 4:26-27; EX1002, ¶117.

FIG.3A



11. [3l]

Anzai discloses “forming the first conductive layer (electrode layer 54) over the gate oxide (layer 12).” EX1003, Fig. 3A, 4:25-32; EX1002, ¶118.

12. [3m]

Anzai discloses “wherein forming the first conductive layer (electrode layer 54) and forming the fourth conductive layer (gate electrode 41) comprise forming the first conductive layer (electrode layer 54) and the fourth conductive layer (gate electrode 41) using the same material (chromium or molybdenum).” EX1003, 4:30-32 (54 is Cr or Mo), 4:56-58 (41 is Cr or Mo); EX1002, ¶119.

13. [3n]

Anzai discloses “wherein forming the first dielectric layer (interlayer insulating film 15) comprises forming a layer of interlayer dielectric (ILD).” Anzai discloses forming interlayer insulating film 15 as a dielectric layer formed of a SiO₂ film, a SiN film and a SiO₂ film, sequentially deposited. *Id.*, Fig. 3A, 4:40-47 (explaining capacitor formed using insulation); 4:60-63 (disclosing dielectric insulating materials); EX1002, ¶120.

14. [3o]

Anzai renders obvious “wherein forming the second dielectric layer (layer 19) comprises forming a layer of passivation silicon nitride.” Anzai discloses forming a layer of film 19 between electrode 70/71 (and film 17) and cathode 65. EX1003, 5:44-6:9; EX1002, ¶121.

A POSITA would have understood film 19 is a “passivation” layer at least because it is an insulating layer for layer 70/71 and serves as a dielectric between layer 70/71 and cathode 65. The Board should reject any attempt by PO to narrowly construe a “passivation layer” to exclude film 19. The 477 provides no meaning for “passivation layer.” In fact, the 477 patent discloses silicon nitride (SiN) as the sole example for this layer, which is disclosed (or at least rendered obvious) as explained below for film 19. For the passivation layer of the second dielectric layer, the 477 patent states: “A layer of passivation silicon nitride (SiN)

212 is formed over ILD 208 and second metal patterns 210A and 210B.” EX1001, 5:55-57. A POSITA would have understood from the 477 patent that there is no special meaning ascribed to passivation layer other than it is a layer of insulation material. EX1002, ¶122.

While Anzai does not disclose the material for layer 19, it must be made of an insulation material because in the embodiment of Fig. 3A, it is the sole layer between electrode layer 70/71 and cathode layer 65 forming the second capacitor. EX1003, Fig. 3A, 6:3-8. Additionally, Anzai discloses that film 19 functions as a capacitance insulating film. EX1003, 5:65-67; EX1002, ¶123.

Anzai renders obvious that film 19 would have been silicon nitride as shown above. See [1h]; EX1002, ¶124.

15. [3p]

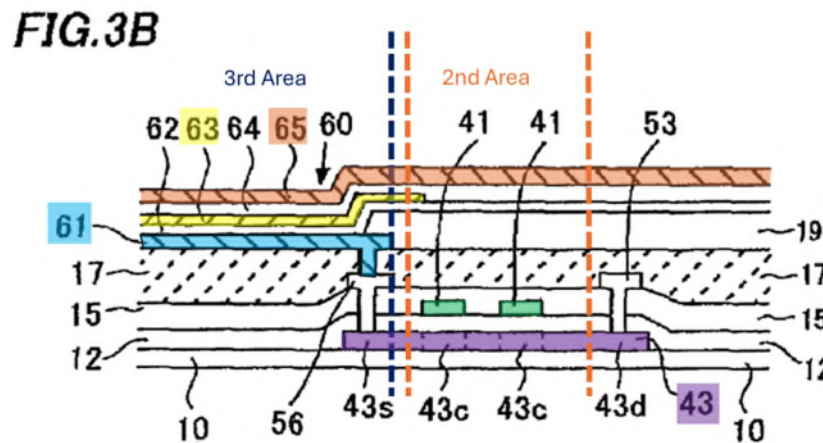
Anzai discloses “forming a fifth conductive layer (anode 61) over the third area (OLED Area). EX1002, ¶125.

16. [3q]

Anzai discloses “forming an organic layer (**emissive layer 63**) over the fifth conductive layer (**anode layer 61**) over the third area (OLED area), wherein the third conductive layer (**cathode layer 65**) is over the organic layer (**emissive layer 63**) over the third area (OLED area), and wherein the fifth conductive layer (**anode layer 61**), the organic layer (**emissive layer 63**), and the third conductive layer

(cathode layer 65) over the third area (OLED area) collectively form the OLED (organic EL element 60).” EX1002, ¶126.

Anzai discloses, in the third area (OLED area) (see [3b]) and as seen in Fig. 3B below (e.g., the left side of the blue dashed line), an EL element is formed with an anode layer 61 (that is connected to the active layer source 43s through source electrode 56), an emissive layer 63 over anode layer 61, and a cathode layer 65 over the emissive layer 63. EX1003, Fig. 3B, 5:3-33. EX1002, ¶127.



Anzai provides the following details of the organic EL element 60:

“The organic EL element 60 includes the anode layer 61 made of the transparent electrode such as ITO (Indium Tin Oxide), a hole transportation layer 62 having a first hole transportation layer made of MTDATA (4,4-bis(3-methylphenylphenylamino)biphenyl) and a second hole transportation layer made of TPD (4,4,4-tris (3-methylphenylphenylamino)triphenylamine), an emissive layer 63 made of Beq2 (bis(10-hydroxybenzohquinolino)beryllium) including quinacridone derivative, an electron transportation layer 64 made of

Bebq2, and the cathode layer 65 made of either magnesium-indium alloy, aluminum or aluminum alloy.” *Id.*, 5:14-25.

A POSITA would have understood that emissive layer 63 is an organic layer because they would have known that Bebq2 is an organic molecule (with chemical composition $C_{26}H_{16}BeN_2O_2$). Additionally, a POSITA would have understood that emissive layer 63 is an organic layer because Anzai explains that during operation, organic molecules in the emissive layer are activated. *Id.*, 5:26-29. A POSITA would also have understood that intervening layers 62 and 64 in the organic EL element 60 do not change the relative positioning of the layers as called for in claim 3, namely, that the emissive layer 63 is over the anode layer 61, and the cathode layer 65 is over the emissive layer 63. EX1002, ¶128.

Anzai discloses that Figs. 3A and 3B show different pixel portions from the same second embodiment. EX1003, 3:10-12; 5:34-36. A POSITA would have therefore understood that the cathode layer 65 in Fig. 3B is the same layer as cathode layer 65 in Fig. 3A (which is the third conductive layer (see [3g])), and therefore Anzai discloses cathode layer 65 (the third conductive layer) is over emissive layer 63 (organic layer) in the OLED area (the third area). Anzai also discloses that anode layer 61 (the fifth conductive layer), the emissive layer 63 (the organic layer), and cathode layer 65 (the third conductive layer) are over the

OLED area (third area) and collectively form the organic EL element 60 (the OLED). EX1003, 5:14-25; EX1002, ¶129.

17. [3r]

Anzai discloses, or at least renders obvious, this limitation. See [1l] (first conductive layer 54 is directly connected to power supply voltage PV_{dd} , CV); EX1002, ¶130.

18. [3s]

Anzai discloses “wherein the second conductive (combined **electrode layer 70/71**) is electrically connected to the fourth conductive layer (**gate electrode 41**).” Anzai discloses layer 70/71 is electrically connected to the common node 55/33s/41 as shown for [1m]. EX1003, Fig. 3A, 5:52-57; see [1m] (explaining how electrode layer 70 is electrically connected to gate electrode 41). EX1002, ¶131.

19. [3t]

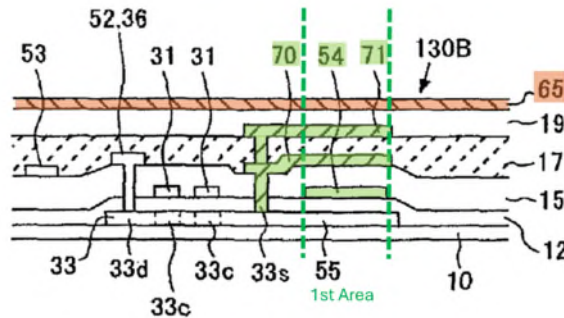
Anzai discloses “wherein the first conductive layer (**electrode layer 54**), the first dielectric layer (interlayer insulating film 15), and the second conductive layer (combined **electrode layer 70/71**) over the first area (Capacitor Area) collectively form a first one of the capacitors (layers 54, 15, 71/70) over the first area (Capacitor Area), the second conductive layer (combined **electrode layer 70/71**), the second dielectric layer (planarization film 19), and the third conductive layer (**cathode layer 65**) over the first area (Capacitor Area) collectively form a second

one of the capacitors (layers 70/71, 19, 65) over the first area (Capacitor Area).”

EX1002, ¶132.

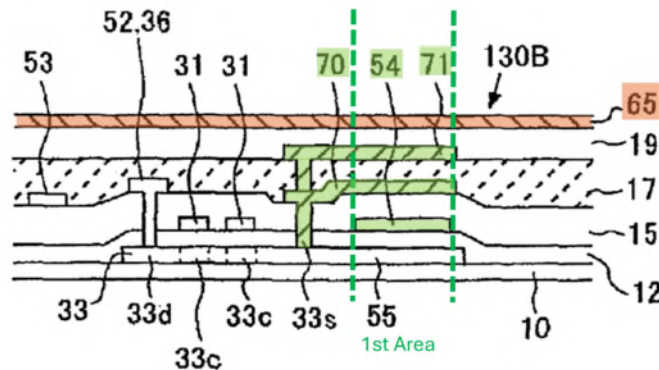
As seen in Fig. 3A below, Anzai discloses a second embodiment having the first capacitor within the first area that includes a first electrode, electrode layer 54, insulating film 15, and a second electrode consisting of the combined **electrode layer 70/71**. EX1003, 5:39-41. A POSITA would have understood that **electrode layer 71** extends over and is electrically connected to **electrode layer 70** (i.e., **electrode layers 70** and **71** form a U-shaped conductive layer that is shared between the first and second capacitors) in the Capacitor Area. It is appropriate to consider this combined **electrode layer 70/71** to be “a second conductive layer. See [3e]. Additionally, a POSITA would have understood from Anzai’s disclosures that **electrode 70** and **71** a) are at the same potential as set by the switching transistor 30, b) would have covered substantially the same Capacitor Area, c) have only dielectric layer 17 between them, and d) are explicitly taught by Anzai to be part of the same “electrode structure” and “storage capacitive element 130B.” EX1003, Fig., 1, 3A, 5:5:34-6:9. Accordingly, a POSITA would have understood combined **electrode layer 70/71** to be part of the first capacitor. *Id.* EX1002, ¶133.

FIG.3A



Claim 3 is an open ended “comprising” claim, thus, a device with the claimed capacitors including the claimed layer practices the claims even if the device includes additional capacitors and a capacitor included additional layers. Anzai’s additional electrode layer 55 is such an additional element. EX1002, ¶134.

FIG.3A



The second capacitor is formed by the common electrode consisting of combined **electrode layer 70/71**, layer 19, and a second electrode **cathode layer 65**. *Id.*, 5:52-61, 5:67-6:3. Here, a POSITA would have understood the first and second capacitors share the common electrode (combined **electrode layer 70/71**) as

recited in claim 3 since combined **electrode layer 70/71** forms a U-shaped conductive layer as explained above. EX1002, ¶135.

Anzai discloses that each of the above identified first and second capacitors functions as a capacitor. EX1003, 5:41 (“electrode structure”), 5:49 (“capacitance element 130B”), 5:44-51 (first capacitor), 5:65-6:3 (second capacitor). EX1002, ¶136.

20. [3u]

See [1o] (driving transistor 40); EX1002, ¶137.

21. [3v]

Anzai discloses “wherein forming the second conductive layer (combined **electrode layer 70/71**) and forming the fifth conductive layer (anode 61) comprise forming the second conductive layer (combined **electrode layer 70/71**) and the fifth conductive layer (anode 61) using the same material (ITO).” EX1003, 5:7-8 (anode 61 is ITO); 5:55-57 (“electrode layer 71 is in the same layer as and formed by the same process as the anode layer 61”); EX1002, ¶138.

VI. GROUND 2: CLAIMS 1 AND 3 ARE RENDERED OBVIOUS BY ANZAI IN VIEW OF YAMAZAKI

To the extent the Board does not find claims 1 and 3 obvious over Anzai, in the alternative, they are obvious over Anzai in view of Yamazaki. EX1002, ¶139.

A. Claim 1

1. [1pre]-[1a]

See Ground 1. EX1002, ¶140.

2. [1b]

See Ground 1. EX1002, ¶141.

To the extent Anzai does not disclose or render obvious the step of defining the areas, it would have been obvious to define them as claimed in view of Yamazaki. Yamazaki discloses an active-matrix type light emitting device with organic compound light emitting element, that includes pixel parts 2. EX1004, Abstract, Fig. 2, 8:56-67. EX1002, ¶142.

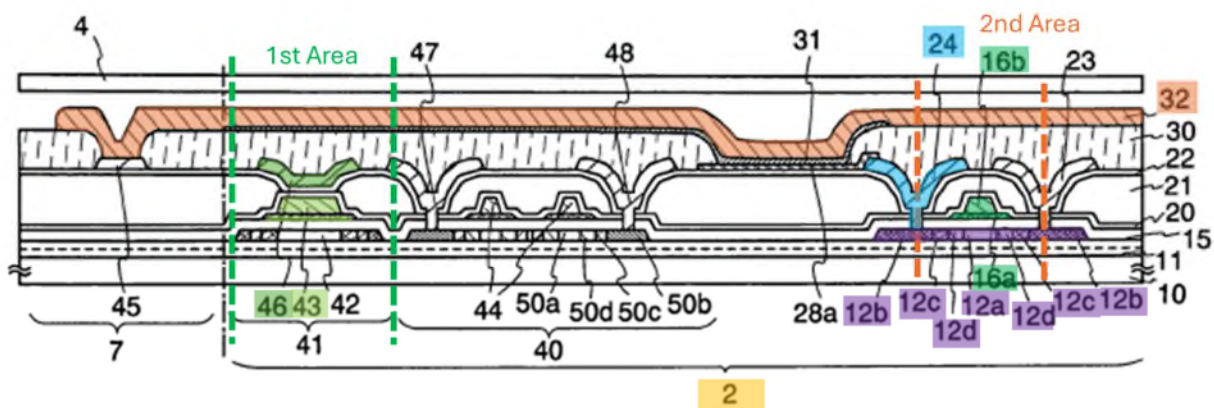


Fig. 2

Each pixel part 2 includes a first area that contains capacitors, a second area that contains a transistor and a third area that contains a light emitting element. *Id.*, Fig. 2, 9:47-12:20. Yamazaki teaches a bottom emission type display and defining

the claimed areas (2 areas for claim 1, 3 areas for claim 3) with additional separation. *Id.*, 11:19-21 (“lower-side radiation type device”). EX1002, ¶143.

A POSITA would have been motivated to define the areas with the additional separation between them as taught by Yamazaki to serve the known goals in the art of ensuring light from the OLED was not blocked by the capacitors, reducing the risk that light from the OLED would cause leakage in the transistor, and avoiding adding layers and potential interference between the capacitors and transistors if they shared the same area. *See* Ground 1, [1b]. While minimizing the area required by the design is also often a design goal, the percentage increase in the total area of the pixel required to further offset the components can be small. The components (e.g., the OLED) have a very large area relative to the small offset at issue. Thus, it would have been obvious to a POSITA to slightly increase the area of the pixel in order to obtain the advantages of increased separation. A POSITA would have had a reasonable expectation of success in creating the additional separation between the areas by using the configuration as illustrated and described in Yamazaki. EX1002, ¶144.

3. [1c]-[1g]

See Ground 1. EX1002, ¶145.

4. [1h]

Anzai in view of Yamazaki renders obvious “forming a layer of capping silicon nitride (silicon nitride layer 19) between the second dielectric layer (planarization film 17) and the third conductive layer (cathode layer 65) over the first area (Capacitor Area) (see [1n]).” Because Anzai does not explicitly disclose the material used for layer 19, (and in the alternative that Anzai alone does not sufficiently teach to use SiN as shown in Ground 1), a POSITA would have been motivated to investigate appropriate materials known in the art for use in layer 19. EX1002, ¶146.

Yamazaki discloses an active-matrix type light emitting device with organic compound light emitting element, that includes pixel parts 2. EX1004, Abstract, Fig. 2, 8:56-67.

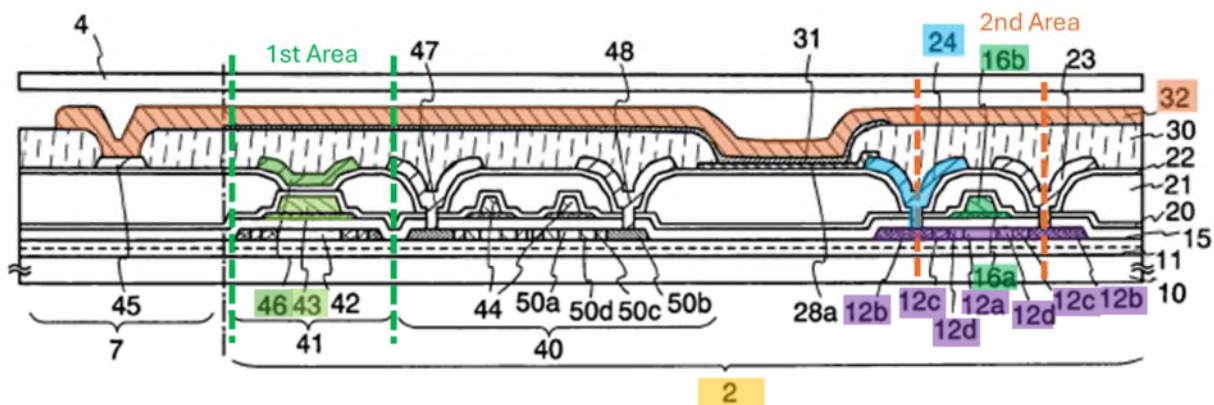


Fig. 2

Each pixel part 2 includes a first area that contains capacitors², a second area that contains a transistor and a third area that contains a light emitting element. *Id.*, Fig. 2, 9:47-12:20. The first area (Capacitor Area) includes a first capacitor formed between electrode 43 and electrode 46 with interlay insulating films 22 and 20 disposed in between, and a second capacitor formed electrode 46 and 2nd electrode 32 (e.g., cathode of the EL device) with an insulating material 30 and EL layer 31 disposed in between. EX1004, Fig. 2, 9:65-12:20. The second area (TFT Area) includes a transistor (e.g., current-controlling TFT) formed by gate electrodes 16a/16b disposed on top of regions 12a-12d on top of substrate 10. *Id.*, Fig. 2, 9:47-64. The third area includes a light emitting element formed by a 2nd electrode 32 disposed above an EL layer 31 which is disposed above 1st electrode 28a (e.g., anode of the EL device). *Id.*, Fig. 2, 11:22-12:20; EX1002, ¶¶147-148.

Insulation layer 30 is disposed between cathode electrode layer 32 and the electrodes 46, 47, 48, 24, 23 underneath (similar to Anzai's layers 17, 19 disposed

² Yamazaki refers to “a capacity 41”, and “a holding capacity is formed using an electrode 46 and an electrode 43,” and “a holding capacity is also formed using the electrode 43 and a semiconductor film 42.” EX1004, 9:65-10:15. A POSITA would have understood that “capacity” refers to a “capacitor” given the structure at issue (two electrodes separated by insulation). EX1002, ¶148; n. 11.

between cathode 65 and electrodes 53, 52, 70). EX1004, Fig. 2. The top surface of insulation layer 30 is flattened relative to the topology underneath that includes electrodes 46, 47, 48, 24, 23 and insulation film 21 (similar to Anzai's layers 17, 19). *Id.* Yamazaki teaches that silicon nitride is a suitable material for insulation layer 30. *Id.*, 11:45-50. Yamazaki also teaches that the flat top surface of insulation layer 30 can be achieved by CMP (chemical mechanical polish), which can be performed after the formation of insulating material 30. *Id.*, 20:17-24; EX1002, ¶149.

Yamazaki teaches that silicon nitride is a suitable material for insulation layer 30. EX1004, 11:45-50 (“The insulating material 30 may be a photosensitive or non-photosensitive organic material (such as polyimide, acrylate, polyamide, polyimide amide, resist, or benzocyclobutene), an inorganic material (such as silicon oxide, silicon nitride, or silicon oxynitride) with a CVD method, a sputtering method, or coating method, or a laminate thereof.” Therefore, Yamazaki discloses that at least this layer (insulating material 30 of Yamazaki) comprises silicon nitride. EX1002, ¶150.

It would have been obvious to a POSITA to combine the teachings of Anzai and Yamazaki to use silicon nitride as the material for film 19 of Anzai. EX1002, ¶151.

A POSITA would have understood the issue involved, namely what material(s) should be used to form layer 19 for the second capacitor of Anzai. To address this issue, a POSITA would have investigated what insulator material(s) would be appropriate. A POSITA would have been motivated to use silicon nitride to form layer 19 of Anzai because (1) Yamazaki teaches using silicon nitride as the insulating layer 30 under its cathode layer (EX1004, 11:45-50), (2) Yamazaki teaches using silicon nitride for use as a planarization film for flattening the surface (compare upper and lower surfaces of insulation layer 30 (*Id.*, 11:22-12:20), and (3) Anzai teaches using silicon nitride in the interlayer insulating film 15 between second and third capacitance electrode layers 54 and 70, and in the gate insulating film 12 between first and second capacitance electrode layers 55 and 54. EX1003, Fig. 2A, 4:8-10 and 17-24; EX1004, Fig. 2, 11:22-12:52, 20:17-39; EX1002, ¶152.

Additionally, Anzai discloses that film 19 is used as a capacitance insulating film. EX1003, 5:65-67. A POSITA would have known that organic materials usually have lower dielectric constants than inorganic materials such as SiN, and a higher dielectric constant is desirable for the insulator in a capacitor since that leads to a higher capacitance per unit area. That then allows a reduced area storage capacitance element, one of the objectives of Anzai. EX1003, Abstract (“The forming area of the storage capacitance element for holding the video signal supplied to the gate of the driving transistor can be thus reduced, improving

display quality as well as extending life span of the organic El element.”). This is supported by the Examiner’s finding during prosecution that a POSITA would have been motivated to use SiN to “increase the capacity of the capacitor.”

EX1005, 91. Therefore, a POSITA would have been motivated to use SiN for film 19, particularly if film 17 were made of material with a lower dielectric constant like organic resin. EX1002, ¶153.

The modification to Anzai would simply involve selecting an appropriate insulation material for layer 19. A POSITA would have had a reasonable expectation of success in combining Anzai and Yamazaki, as both references disclose forming capacitors for use with organic electroluminescent devices, and both references teach insulator films for such capacitors that comprise silicon nitride. Anzai itself confirms that SiN can be used for insulation layers as noted above. And because combining the teachings of Anzai and Yamazaki would involve known methods, it would have yielded predictable results. EX1002, ¶154.

5. [1i]-[1k]

See Ground 1. EX1002, ¶155.

6. [1l]

Anzai in view of Yamazaki renders obvious “wherein the first conductive layer (electrode layer 54) over the first area (Capacitor Area) is directly connected to a power supply voltage (a predetermined stable voltage, PVdd, CV).” As shown

for Ground 1, Anzai discloses that electrode layer 54 is provided with “a predetermined stable voltage” but does not explicitly disclose what would provide that voltage. Accordingly, a POSITA would have been motivated to investigate known solutions in the art and be led to Yamazaki. As discussed above for limitation [1h] it would have been obvious to combine the teachings of Anzai and Yamazaki. EX1002, ¶156.

Yamazaki discloses storage capacitor 1859 with one electrode electrically connected to the gate of driving transistor 1858 and the other electrode directly connected to power supply line 1854. EX1004, Fig. 18B, 39:18-21. Just like in Anzai, the voltage of one electrode of the storage capacitor 1859 is set to a desired voltage through select transistor 1851, and the voltage of the other electrode is provided with a stable predetermined voltage in order to store the charge for use on the gate of the driving transistor. While Anzai teaches electrode 131/54 is provided with an unidentified “predetermined stable voltage,” Yamazaki teaches that a “predetermined stable voltage” can be provided to that electrode by directly connecting it to power supply line 1854. Yamazaki expressly teaches this embodiment may be used with Example 1 and Figure 2 which were discussed with respect to limitation [1h]. *Id.*, 39:43-60; EX1002, ¶157.

A POSITA would have been motivated to modify Anzai to directly connect electrode layer 54 to the Anzai’s power supply voltage 53 based on the teaching of

Yamazaki to directly connect that electrode of the storage capacitor to the power supply line. A POSITA would have recognized this direct connection in Yamazaki as a known and efficient way to provide a predefined stable voltage as required by Anzai. A POSITA would have had a reasonable expectation of success in making the combination using a simple via connecting 54 and 53 for all the reasons provided above for this limitation in Ground 1, which are incorporated herein by reference. EX1002, ¶158.

7. [1m]-[1o]

See Ground 1. EX1002, ¶159.

B. Claim 3

1. [3pre]-[3n]

See Ground 1. EX1002, ¶160.

For step [3b], *see also*, Ground 2, [1b] (explaining additional bases for obviousness of this step in view of Yamazaki's increased separation between the areas). EX1002, ¶161.

2. [3o]

See Ground 1, [3o] (Anzai renders obviousness layer 19 is SiN); Ground 2, [1h] (Anzai in view of Yamazaki renders obvious layer 19 is SiN); EX1002, ¶162.

3. [3p]-[3q]

See Ground 1. EX1002, ¶163.

4. [3r]

See Ground 1, [3r] (Anzai renders obvious layer 54 is directly connected to power supply voltage); Ground 2, [1l] (Anzai in view of Yamazaki renders obvious layer 54 is directly connected to power supply voltage); EX1002, ¶164.

5. [3s]-[3v]

See Ground 1. EX1002, ¶165.

VII. GROUND 3: CLAIMS 1 AND 3 ARE RENDERED OBVIOUS BY ANZAI IN VIEW OF YAMADA

To the extent the Board does not find claims 1 and 3 obvious over Anzai, in the alternative, they are obvious over Anzai in view of Yamada. EX1002, ¶166.

A. Claim 1

1. [1pre]-[1a]

See Ground 1. EX1002, ¶167.

2. [1b]

See Ground 1. EX1002, ¶168.

To the extent Anzai does not disclose or render obvious the step of defining the areas, it would have been obvious to define them as claimed in view of Yamada. It would have been obvious to combine Anzai and Yamada as shown below for [1h]. Yamada explicitly teaches the desire to prevent light from an OLED from causing leakage current in the transistor by defining different areas for these components and including a light shielding layer 19. See, e.g., EX1013, Figs.

4, 8, 2:31-35 (discussing known problem), 11:34-40 (discussing solution of shielding layer and offset transistors); EX1002, ¶169.

A POSITA would have been motivated to define the areas with the additional separation between them as taught by Yamada to serve the known goals in the art of ensuring light from the OLED was not blocked by the capacitors, reducing the risk that light from the OLED would cause leakage in the transistor, and avoiding adding layers and potential interference between the capacitors and transistors if they shared the same area. *See* Ground 1, [1b]. While minimizing the area required by the design is also often a design goal, the percentage increase in the total area of the pixel required to further offset the components can be extremely small. The components (e.g., the OLED) have a large area relative to the small offset at issue. Thus, it would have been obvious to a POSITA to slightly increase the area of the pixel in order to obtain the advantages of increased separation. A POSITA would have had a reasonable expectation of success in creating the additional separation between the areas by using the configuration as illustrated and described in Yamada. EX1002, ¶170.

3. [1c]-[1g]

See Ground 1. EX1002, ¶171.

4. [1h]

Anzai in view of Yamada renders obvious “forming a layer of capping silicon nitride (silicon nitride layer 19) between the second dielectric layer (planarization film 17) and the third conductive layer (cathode layer 65) over the first area (Capacitor Area) (see [1n]).” Because Anzai does not explicitly disclose the material used for layer 19, (and in the alternative that Anzai alone does not sufficiently teach to use SiN as shown in Ground 1), a POSITA would have been motivated to investigate appropriate materials known in the art for use in layer 19. EX1002, ¶172.

Yamada is assigned to the same assignee as Anzai, discloses a nearly identical pixel structure, and includes many similar figures and accompanying text. In relevant part, Figure 3 of Yamada is nearly identical to Figure 1 of Anzai, Figure 4B of Yamada is nearly identical to Figure 2B of Anzai, and the schematic in Figure 5 of Yamada shows an obvious modification to the schematic of Figure 4 of Anzai. EX1013, Figs. 3, 4B, 5; EX1003, Figs. 1, 2B, 4. Thus, a POSITA would have recognized the similarities in the references and found the teachings of Yamada particularly relevant to Anzai. EX1002, ¶173.

Yamada teaches the same layers as Anzai, including layers 17 and 19. EX1013, Fig. 4B. Much of the text in Yamada disclosing the layers is identical to Anzai. *Id.*, 4:65-6:30. Like Anzai, Yamada discloses planarizing insulting film 17

may consist of organic resin. *Id.*, 6:2-4. Yamada differs from Anzai by expressly teaching that layer 19 “may be composed of a single layer of SiO₂ film or SiN film, or a lamination of those films.” *Id.*, 6:48-50, 11:16-17. Yamada also teaches that layer 19 could be made of other materials like a resin, but those additional teachings do not detract from the teaching that SiN would have been an obvious design choice. This is particularly true in the context of Anzai, where the higher dielectric constant of SiN would make it preferable to organic resins to enhance the capacitance of Anzai’s second capacitor as explained for Ground 1. EX1002, ¶174.

It would have been an obvious design choice to use SiN for layer 19 and a POSITA would have had a reasonable expectation of success in using that material as taught by Yamada and for all the reasons provided above for Grounds 1 and 2, which are incorporated by reference herein. EX1002, ¶175.

5. [1i]-[1k]

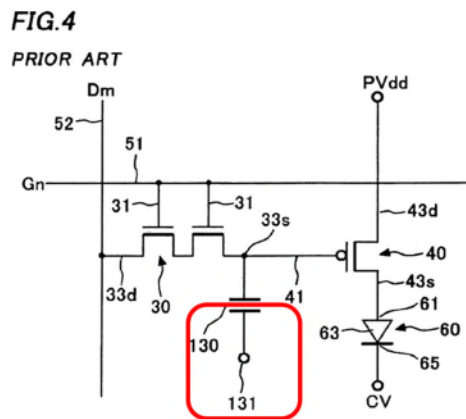
See Ground 1. EX1002, ¶176.

6. [1l]

Anzai in view of Yamada renders obvious “wherein the first conductive layer (electrode layer 54) over the first area (Capacitor Area) is directly connected to a power supply voltage (PVdd).” As shown for Ground 1, Anzai discloses that electrode 54 is provided with “a predetermined stable voltage” but does not explicitly disclose what would provide that voltage. Accordingly, a POSITA would

have been motivated to investigate known solutions in the art and would have been led to Yamada. As discussed above for limitation [1h] it would have been obvious to combine the teachings of Anzai and Yamada because they disclose nearly identical pixel circuits and are assigned to the same assignee. EX1002, ¶177.

Yamada discloses storage capacitor 90 with one electrode electrically connected to the gate electrode 41 of driving transistor 40 and the other electrode directly connected to power line 53. EX1013, Fig. 5, 7:49-61. Figure 5 of Yamada and Figure 4 of Anzai are shown below with the relevant electrodes of the capacitors highlighted. EX1002, ¶178.



Anzai Figure 4

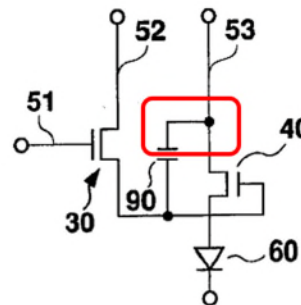


Fig. 5

Yamada Figure 5

As explained in Ground 1, electrode 131 in Figure 4 of Anzai corresponds with electrode 54 of Anzai. While Anzai teaches electrode 131/54 is provided with an unidentified “predetermined stable voltage,” Yamada teaches that a “predetermined stable voltage” can be provided to that electrode by directly connecting it to voltage power supply 53. EX1002, ¶178.

A POSITA would have been motivated to modify Anzai to directly connect electrode layer 54 to the Anzai's own power supply voltage 53 based on the teaching of Yamada to directly connect that electrode of the storage capacitor to Yamada's power supply line 53. A POSITA would have recognized this direct connection in Yamada as a known and efficient way to provide a predefined stable voltage as required by Anzai. A POSITA would have had a reasonable expectation of success in making the combination using a simple via connecting 54 and 53 for all the reasons provided above for this limitation in Grounds 1 and 2, which are incorporated herein by reference. EX1002, ¶179.

7. [1m]-[1o]

See Ground 1. EX1002, ¶180.

B. Claim 3

1. [3pre]-[3n]

See Ground 1. EX1002, ¶181.

For step [3b], *see also*, Ground 3, [1b] (explaining additional bases for obviousness of this step in view of Yamada's increased separation between the areas). EX1002, ¶182.

2. [3o]

See Ground 1, [3o] (Anzai renders obviousness layer 19 is SiN); Ground 3, [1h] (Anzai in view of Yamada renders obvious layer 19 is SiN); EX1002, ¶183.

3. [3p]-[3q]

See Ground 1. EX1002, ¶184.

4. [3r]

See Ground 1, [3r] (Anzai renders obvious layer 54 is directly connected to power supply voltage); Ground 3, [1l] (Anzai in view of Yamada renders obvious layer 54 is directly connected to power supply voltage); EX1002, ¶185.

5. [3s]-[3v]

See Ground 1. EX1002, ¶186.

VIII. DISCRETIONARY DENIAL IS NOT WARRANTED

A. 35 U.S.C. § 314(a) Analysis

The *Fintiv* factors (enumerated below) weigh against discretionary denial. IPR2020-00019, Paper 11, 5-6 (PTAB Mar. 20, 2020) (precedential).

1. Stay

This factor is neutral because no party has requested a stay. *Sand Revolution II, LLC. v. Continental Intermodal Group-Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020).

2. Trial Date

Trial has been set for January 5, 2026 and any IPR instituted on this Petition should complete within approximately two months of that date. Thus, this factor weighs against a discretionary denial.

3. Parallel Proceeding

As of the filing of this Petition, neither party has initiated any discovery of the other. A Markman hearing is not scheduled until July 15, 2025.

4. Issue Overlap

This Petition includes independent claims 1 and 3, and the litigation only involves claim 1. Claim 3 is an independent claim substantively different from claim 1 because it includes limitations directed to a third OLED region and the respective layers in that region. PO chose not to assert claim 3 against Petitioner even though PO chose to assert similar claim 1 of the parent 121 patent, which has similar claims drawn to the third OLED region. Thus, this factor weighs strongly against exercising the Board's discretion to deny institution.

5. Same Party

Because Petitioner and the PO are the parties in the Litigation, and because this Board is likely to reach the merits around the same time as the district court, this factor weighs slightly against discretionary denial. *See NVIDIA Corp. v. Invensas Corp.*, IPR2020-00603, Paper 11, at 23.

6. Other Considerations

Other considerations weigh strongly against a discretionary denial. The Challenged Claims are clearly invalid, Petitioners have not previously challenged this patent based on the references relied upon in this petition, and the patent has

never been challenged in a post-issuance proceeding. Thus, this factor weighs against a discretionary denial.

The Board should not exercise its discretion under *Fintiv* to deny this Petition because to do so would encourage gamesmanship by patent owners. PO filed the underlying litigation on November 22, 2023 when it asserted several patents including the 121 patent, which contains claims very similar to the 477 patent and to which the 477 patent claims priority. However, PO did not assert the 477 patent until it filed an amended complaint on July 19, 2024—on the last possible day it could do so under the local rules without a requirement to show good cause. PO asserts the 121 and 477 patents against the same product with substantially identical theories using the same purported reverse engineered evidence. PO has not offered any explanation for the timing of its assertions.

Regardless of whether this particular patent owner had a good reason for the timing of its assertions in this particular instance, if the Board were to exercise its discretion under *Fintiv* to deny this Petition, other patent owners might feel compelled to zealously represent their clients by initiating a litigation on a subset of patents and delaying the assertion of additional patents until the last possible moment. Here, Petitioner was able to quickly file this Petition (less than two months after the first assertion of the 477 patent). Thus, the Board should not exercise its discretion under *Fintiv* to deny this Petition because Petitioner reacted

promptly to the first assertion of the 477 patent and because denying this Petition under these circumstances could invite gamesmanship by other patent owners.

Finally, even if the Board were to determine that *Fintiv* factors on balance weigh in favor of denial, institution should nonetheless be granted because this Petition satisfies the compelling merits standards. Interim Guidance at 4; *Vizio, Inc. v. Maxell, Ltd.*, IPR2022-01458, Paper 8, at 62.

B. 35 U.S.C. § 325(b) Analysis

Applying the two-part framework discussed in *Advanced Bionics, LLC v. Med-El Elektromedizinische Gerate GMBH*, IPR2019-01469, Pap. 6, *8-9, the Board should not exercise its §325(d) discretion to deny institution.

None of the challenges are substantially the same as those considered during prosecution. In the event that the challenges herein are found to be based on prior art that is the same as or cumulative to prior art considered by the examiner during prosecution, the examiner has made a clear error in allowing the claims over such prior art.

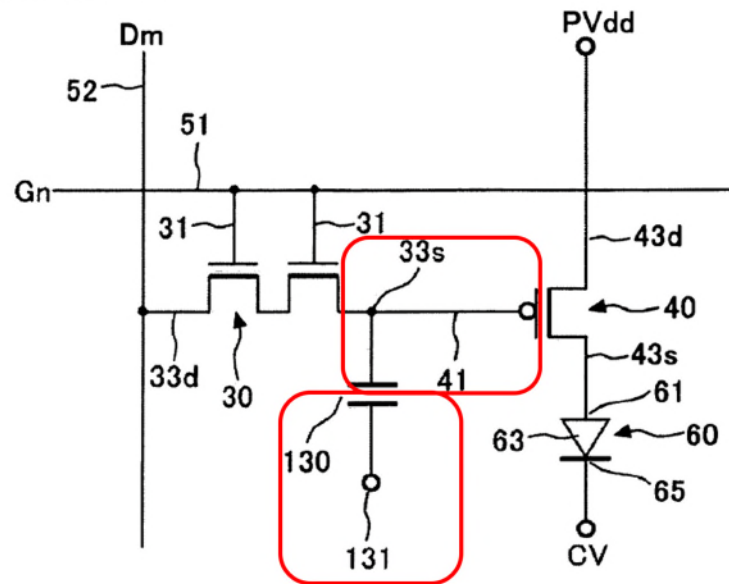
In addition to all the other limitations, the two limitations added during prosecution ([11] and [1m]) to secure allowance (see Section III.B Overview of the File History) are clearly disclosed in the prior art as shown in the above Grounds. As shown in annotated Figure 4 of Anzai below, for [11] the relevant electrode (capacitor electrode 54 illustrated on the bottom of capacitor 130 in Figure 4) is

directly connected to a power voltage supply (predetermined stable voltage 131).

And for [1m] the relevant electrode (capacitor electrode 70/55 illustrated on the top of capacitor 130 in Figure 4) is electrically connected to a gate electrode (gate electrode 41). EX1002, ¶¶55-56.

FIG.4

PRIOR ART



Accordingly, the Board should not exercise its discretion to deny institution.

IX. COMPLIANCE WITH FORMAL REQUIREMENTS

A. Mandatory Notices Under 37 C.F.R. §§ 42.8(b)(1)-(4)

1. Real Party-In-Interest

BOE Technology Group Co., LTD is the real party-in-interest.

2. Related Matters

The 477 patent is subject to the following actions: *Optronic Sciences LLC v.*

BOE Technology Group Co., LTD, 2:23-cv-00549 (EDTX).

IPR2024-01132 asserts grounds similar to those asserted in this Petition
against U.S. Pat. No. 7,586,121, to which the 477 patent claims priority.

3. Lead and Backup Counsel

Lead Counsel	Backup Counsel
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4. Service Information

Please address correspondence to counsel at the addresses above. Petitioner consents to electronic service to: dla-boe-optronicsciences-IPR@us.dlapiper.com and the email addresses listed above.

B. Proof of Service on the Patent Owner

In accordance with 37 C.F.R. §§42.6(e) and 42.105, as identified in the attached Certificate of Service, a copy of this Petition in its entirety is being served

electronically (by agreement) on counsel for Patent Owner in the District Court
Litigation.

C. Power of Attorney

Powers of attorney are being filed with designation of counsel in accordance
with 37 C.F.R. § 41.10(b).

D. Standing

In accordance with 37 C.F.R. §42.104(a), Petitioner certifies that the 477
patent is available for *inter partes* review and that Petitioner is not barred or
estopped from requesting an *inter partes* review challenging the patent claims on
the grounds identified in this Petition.

E. Fees

The undersigned authorizes the Director to charge the fee specified by 37
C.F.R. § 42.15(a) and any additional fees that might be due in connection with this
Petition to Deposit Account No. 503266.

X. CONCLUSION

All Challenged Claims of the 477 patent should be found unpatentable for
the reasons discussed in this Petition.

Respectfully submitted,

/Brian Erickson/
Brian Erickson
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DLA Piper LLP (US)

U.S. Patent No. 8,158,477
Petition for *Inter Partes* Review
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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Petitioner certifies that this petition includes 11,848 words, as measured by Microsoft Word, exclusive of the table of contents, mandatory notices under § 42.8, certificates of service, word count, claim listing, and exhibits.

Date: August 28, 2024

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CERTIFICATE OF SERVICE

The undersigned certifies pursuant to 37 C.F.R. §§ 42.6(e) and 42.105 that on August 28, 2024, a true and correct copy of the Petition for Inter Partes Review of U.S. Patent No. 8,158,477 was served by emailing a copy of same (by agreement) to the following attorneys for the Patent Owner:

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