

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner,

v.

OPTRONIC SCIENCES LLC,
Patent Owner.

IPR2024-01315
Patent 8,158,477 B2

Before BENJAMIN D. M. WOOD, BRIAN J. McNAMARA, and
ROBERT J. WEINSCHENK, *Administrative Patent Judges*.

WEINSCHENK, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

BOE Technology Group Co., Ltd. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1 and 3 (“the challenged claims”) of U.S. Patent No. 8,158,477 B2 (Ex. 1001, “the ’477 patent”). Optronic Sciences LLC (“Patent Owner”) filed a Preliminary Response (Paper 13, “Prelim. Resp.”) to the Petition.

An *inter partes* review may not be instituted unless “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). Further, when instituting an *inter partes* review, we “will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.” 37 C.F.R. § 42.108(a). Here, Petitioner demonstrates a reasonable likelihood of prevailing in showing that at least one of the challenged claims is unpatentable. Thus, we institute an *inter partes* review of the challenged claims on all the grounds of unpatentability in the Petition.

B. *Real Parties in Interest*

The parties identify themselves as the only real parties in interest. Pet. 67; Paper 4, 1.

C. *Related Matters*

The parties indicate that the ’477 patent is the subject of the following district court case: *Optronic Sciences LLC v. BOE Technology Group Co., Ltd.*, No. 2:23-cv-00549 (E.D. Tex.). Pet. 67; Paper 4, 1. The parties also

identify IPR2024-01130, IPR2024-01131, IPR2024-01132, IPR2024-01133, and IPR2024-01134, as related matters. Pet. 68; Paper 4, 1.

D. The '477 Patent

The '477 patent relates to “a storage capacitor of an electroluminescence device.” Ex. 1001, 1:16–19. The '477 patent states that “an active matrix organic light emitting diode (‘OLED’) device or a polymer light emitting diode (‘PLED’) device . . . includes an array of pixels, where each pixel comprises a set of sub-pixels.” *Id.* at 1:30–34. “Each sub-pixel further includes a switching transistor, a driving transistor and a storage capacitor.” *Id.* at 1:34–35. According to the '477 patent, “it is desirable to design a storage capacitor with a large capacitance in order to avoid an issue of gray scale fading due to crosstalk or feed-through effect.” *Id.* at 1:35–38. However, “a storage capacitor having greater capacitance may disadvantageously result in a smaller aperture ratio.” *Id.* at 1:38–41. To address this deficiency, the '477 patent describes “a storage capacitor that includes improved capacitance in a limited area.” *Id.* at 1:43–45.

E. Illustrative Claim

Both challenged claims, claims 1 and 3, are independent. Claim 1 is reproduced below.¹

1. A method for forming a pixel of an electroluminescence device, comprising:
 - [1a] providing a substrate;
 - [1b] defining at least a first area for capacitors and a second area for a transistor on the substrate;
 - [1c] forming a first conductive layer over the first area;

¹ We use Petitioner’s designations for the limitations of claim 1. Pet. vi.

[1d] forming a first dielectric layer over the first conductive layer over the first area;

[1e] forming a second conductive layer over the first dielectric layer over the first area;

[1f] forming a second dielectric layer over the second conductive layer over the first area;

[1g] forming a third conductive layer over the second dielectric layer over the first area;

[1h] forming a layer of capping silicon nitride between the second dielectric layer and the third conductive layer over the first area;

[1i] forming a semiconductor layer over the second area;

[1j] forming a gate oxide layer over the second area; and

[1k] forming a fourth conductive layer over the gate oxide layer over the second area;

[1l] wherein the first conductive layer over the first area is directly connected to a power supply voltage, [1m] wherein the second conductive layer is electrically connected to the fourth conductive layer, and [1n] wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area, the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over the first area, and [1o] the semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor.

Ex. 1001, 8:54–9:20.

F. Evidence

Petitioner submits the following evidence:

Evidence	Exhibit No.
Declaration of Dr. Dean Neikirk (“Neikirk Declaration”)	1002
Anzai, US 7,330,168 B2, issued Feb. 12, 2008 (“Anzai”)	1003

Evidence	Exhibit No.
Yamazaki, US 6,992,332 B2, issued Jan. 31, 2006 (“Yamazaki”)	1004
Yamada, US 6,246,179 B1, issued June 12, 2001 (“Yamada”)	1013

G. Asserted Grounds

Petitioner asserts that the challenged claims are unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 3	103(a) ²	Anzai
1, 3	103(a)	Anzai, Yamazaki
1, 3	103(a)	Anzai, Yamada

II. ANALYSIS

A. Legal Standards

A claim is unpatentable as obvious under if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including 1) the scope and content of the prior art; 2) any differences between the claimed subject matter and the prior art; 3) the level of ordinary skill in the art; and 4) any objective indicia of non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. Based on the effective filing date of the ’477 patent, we apply the pre-AIA version of § 103.

B. Level of Ordinary Skill in the Art

Petitioner argues that a person of ordinary skill in the art “would have had a Bachelors’ degree in electrical engineering or a comparable field of study, plus approximately two to three years of professional experience with electronic and optoelectronic device design.” Pet. 6 (citing Ex. 1002 ¶¶ 34–37). Petitioner’s description of the level of ordinary skill in the art is supported by the testimony of Petitioner’s declarant, Dr. Dean Neikirk. Ex. 1002 ¶¶ 34–37. Patent Owner does not dispute Petitioner’s description at this stage of the proceeding. *See* Prelim. Resp. 1. We adopt Petitioner’s description for the purposes of this Decision.

C. Claim Construction

In an *inter partes* review proceeding, a patent claim is construed using the same standard used in a civil action under 35 U.S.C. § 282(b), including construing the claim in accordance with the ordinary and customary meaning of the claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. 37 C.F.R. § 42.100(b). Neither party proposes an express construction for any claim terms. Pet. 7; *see* Prelim. Resp. 1. We determine that no claim terms require express construction for purposes of this Decision.

D. Asserted Obviousness of Claims 1 and 3 over Anzai

Petitioner argues that claims 1 and 3 would have been obvious over Anzai. Pet. 8–47. Patent Owner does not present any substantive arguments regarding this asserted ground. *See* Prelim. Resp. 1. For the reasons discussed below, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claims 1 and 3 would have been obvious over Anzai.

1. Claim 1

Claim 1 recites “[a] method for forming a pixel of an electroluminescence device.” Ex. 1001, 8:54–55. Petitioner presents evidence that Anzai teaches forming an electroluminescent (“EL”) device comprising a plurality of pixels. Pet. 8–9 (citing Ex. 1003, 1:6–17, Fig. 1). On this record, Petitioner shows sufficiently that Anzai teaches the recitations in the preamble of claim 1.³

Claim limitation [1a] recites “providing a substrate.” Ex. 1001, 8:56. Petitioner presents evidence that Anzai teaches providing a substrate. Pet. 9–10 (citing Ex. 1003, 3:57–61, Figs. 2A, 2B). On this record, Petitioner shows sufficiently that Anzai teaches limitation [1a].

Claim limitation [1b] recites “defining at least a first area for capacitors and a second area for a transistor on the substrate.” Ex. 1001, 8:57–58. Petitioner presents evidence that Anzai teaches defining a first area for capacitors on the substrate and a second area for a transistor on the substrate. Pet. 10–14 (citing Ex. 1003, 3:28–40, Figs. 1, 2A, 2B). Petitioner’s annotated versions of Anzai’s Figures 2A and 2B are reproduced below. Pet. 11.

FIG.2A

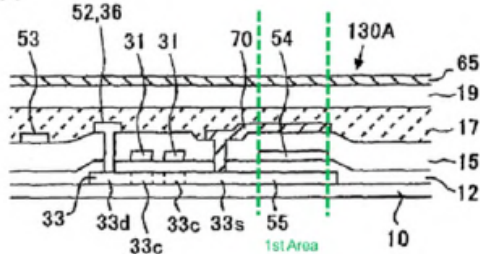
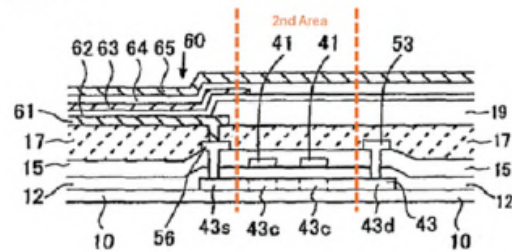


FIG.2B



³ We need not decide whether the preamble of claim 1 is limiting because Petitioner shows sufficiently that the prior art teaches the recitations in the preamble.

Figures 2A and 2B show cross-sectional views of a pixel portion of an electroluminescent device. Ex. 1003, 3:21–26. Petitioner’s annotation to Figure 2A shows a first area for capacitor 130A on substrate 10. Pet. 10–12 (citing Ex. 1003, 3:28–40, Figs. 2A, 2B). Petitioner’s annotation to Figure 2B shows a second area for a transistor comprising gate electrode 41 on substrate 10. *Id.* (citing Ex. 1003, 3:28–40, Figs. 2A, 2B). On this record, Petitioner shows sufficiently that Anzai teaches limitation [1b].

Claim limitation [1c] recites “forming a first conductive layer over the first area.” Ex. 1001, 8:59. Petitioner presents evidence that Anzai teaches forming electrode layer 54 over the first area. Pet. 14 (citing Ex. 1003, 4:30–32, Fig. 2A). On this record, Petitioner shows sufficiently that Anzai teaches limitation [1c].

Claim limitation [1d] recites “forming a first dielectric layer over the first conductive layer over the first area.” Ex. 1001, 8:60–61. Petitioner presents evidence that Anzai teaches forming interlayer insulating film 15 over electrode layer 54 and the first area. Pet. 14–15 (citing Ex. 1003, 4:60–63, Fig. 2A). On this record, Petitioner shows sufficiently that Anzai teaches limitation [1d].

Claim limitation [1e] recites “forming a second conductive layer over the first dielectric layer over the first area.” Ex. 1001, 8:62–63. Petitioner presents evidence that Anzai teaches forming electrode layer 70 over interlayer insulating film 15 and the first area. Pet. 15 (citing Ex. 1003, 4:13–14, 4:35–37, 4:44–45, Fig. 2A). On this record, Petitioner shows sufficiently that Anzai teaches limitation [1e].

Claim limitation [1f] recites “forming a second dielectric layer over the second conductive layer over the first area.” Ex. 1001, 8:64–65.

Petitioner presents evidence that Anzai teaches forming planarization film 17 over electrode layer 70 and the first area. Pet. 16 (citing Ex. 1003, 4:23, 4:48–51, 5:3–4, 5:62–67, Fig. 2A). On this record, Petitioner shows sufficiently that Anzai teaches limitation [1f].

Claim limitation [1g] recites “forming a third conductive layer over the second dielectric layer over the first area.” Ex. 1001, 8:66–67. Petitioner presents evidence that Anzai teaches forming cathode layer 65 over planarization film 17 and the first area. Pet. 17 (citing Ex. 1003, 4:48–51, 5:23–25, 5:62–67, Fig. 2A). On this record, Petitioner shows sufficiently that Anzai teaches limitation [1g].

Claim limitation [1h] recites “forming a layer of capping silicon nitride between the second dielectric layer and the third conductive layer over the first area.” Ex. 1001, 9:1–3. Petitioner presents evidence that Anzai teaches forming planarization film 19 between planarization film 17 and cathode layer 65 and over the first area. Pet. 17–18 (citing Ex. 1003, 5:44–6:9, Fig. 2A). Petitioner also presents evidence that a person of ordinary skill in the art would have: 1) known that Anzai’s planarization film 19 is a capping layer; and 2) found it obvious to form planarization film 19 of silicon nitride. *Id.* at 18–22 (citing Ex. 1002 ¶¶ 73–77, 80; Ex. 1003, 3:49–51, 4:17–24, 5:3–13, 5:44–6:9). On this record, Petitioner shows sufficiently that Anzai teaches limitation [1h].

Claim limitation [1i] recites “forming a semiconductor layer over the second area.” Ex. 1001, 9:4. Petitioner presents evidence that Anzai teaches forming active layer 43 over the second area. Pet. 23 (citing Ex. 1003, 4:52–60, Fig. 2B). On this record, Petitioner shows sufficiently that Anzai teaches limitation [1i].

Claim limitation [1j] recites “forming a gate oxide layer over the second area.” Ex. 1001, 9:5. Petitioner presents evidence that Anzai teaches forming gate insulating film 12 over the second area. Pet. 23–24 (citing Ex. 1003, 4:8–10, 4:56, Fig. 2B). On this record, Petitioner shows sufficiently that Anzai teaches limitation [1j].

Claim limitation [1k] recites “forming a fourth conductive layer over the gate oxide layer over the second area.” Ex. 1001, 9:6–7. Petitioner presents evidence that Anzai teaches forming gate electrode 41 over gate insulating film 12 and the second area. Pet. 24 (citing Ex. 1003, 4:56–58, Fig. 2B). On this record, Petitioner shows sufficiently that Anzai teaches limitation [1k].

Claim limitation [1l] recites “wherein the first conductive layer over the first area is directly connected to a power supply voltage.” Ex. 1001, 9:8–9. Petitioner presents evidence that Anzai teaches providing capacitor 130 with a “predetermined stable voltage.” Pet. 25–26 (citing Ex. 1003, 1:44–48, 2:1–2, 3:26–27, Fig. 4). Petitioner also presents evidence that a person of ordinary skill in the art would have found it obvious to directly connect capacitor 130’s electrode layer 54 to the “predetermined stable voltage.” *Id.* at 26–28 (citing Ex. 1002 ¶¶ 88–91). On this record, Petitioner shows sufficiently that Anzai teaches limitation [1l].

Claim limitation [1m] recites “wherein the second conductive layer is electrically connected to the fourth conductive layer.” Ex. 1001, 9:9–11. Petitioner presents evidence that Anzai teaches electrically connecting electrode layer 70 to gate electrode 41 through source 33s. Pet. 28–30 (citing Ex. 1003, 1:18–2:8, 3:26–27, 3:42–44, 4:37–39, Figs. 2A, 2B, 4). On this record, Petitioner shows sufficiently that Anzai teaches limitation [1m].

Claim limitation [1n] recites “wherein the first conductive layer, the first dielectric layer, and the second conductive layer over the first area collectively form a first one of the capacitors over the first area,” and “the second conductive layer, the second dielectric layer, and the third conductive layer over the first area collectively form a second one of the capacitors over the first area.” Ex. 1001, 9:11–17. Petitioner presents evidence that Anzai’s electrode layer 54, interlayer insulating film 15, and electrode layer 70 form a first capacitor. Pet. 30–32 (citing Ex. 1002 ¶¶ 95–97; Ex. 1003, 3:61–67, 4:25–47, Fig. 2A). Petitioner also presents evidence that Anzai’s electrode layer 70, planarization film 17, and cathode layer 65 form a second capacitor. *Id.* (citing Ex. 1002 ¶¶ 95, 98; Ex. 1003, 4:48–51, 5:62–67, Fig. 2A). On this record, Petitioner shows sufficiently that Anzai teaches limitation [1n].

Claim limitation [1o] recites wherein “the semiconductor layer, the gate oxide layer, and the fourth conductive layer over the second area collectively form a transistor.” Ex. 1001, 9:18–20. Petitioner presents evidence that Anzai’s active layer 43, gate insulating film 12, and gate electrode 41 form a transistor. Pet. 33–34 (citing Ex. 1002 ¶¶ 103–105; Ex. 1003, 3:52–56, 4:1–25, 4:37–40, 4:52–60, Figs. 1, 2B). On this record, Petitioner shows sufficiently that Anzai teaches limitation [1o].

2. Claim 3

Petitioner presents evidence that teaches Anzai also teaches the limitations of claim 3. Pet. 35–47. On this record, Petitioner shows sufficiently that Anzai teaches the limitations of claim 3.

3. Summary

For the foregoing reasons, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claims 1 and 3 would have been obvious over Anzai.

E. Asserted Obviousness of Claims 1 and 3 over Anzai and Yamazaki

Petitioner argues that claims 1 and 3 would have been obvious over Anzai and Yamazaki. Pet. 47–57. Petitioner presents evidence indicating that the Anzai and Yamazaki combination teaches the limitations of claims 1 and 3, and that a person of ordinary skill in the art would have had reason to combine these references. *Id.* Patent Owner does not present any substantive arguments regarding this asserted ground. *See* Prelim. Resp. 1. On this record, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claims 1 and 3 would have been obvious over Anzai and Yamazaki.

F. Asserted Obviousness of Claims 1 and 3 over Anzai and Yamada

Petitioner argues that claims 1 and 3 would have been obvious over Anzai and Yamada. Pet. 57–63. Petitioner presents evidence indicating that the Anzai and Yamada combination teaches the limitations of claims 1 and 3, and that a person of ordinary skill in the art would have had reason to combine these references. *Id.* Patent Owner does not present any substantive arguments regarding this asserted ground. *See* Prelim. Resp. 1. On this record, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claims 1 and 3 would have been obvious over Anzai and Yamada.

G. Patent Owner's Preliminary Response

Patent Owner's Preliminary Response does not present any substantive arguments regarding the asserted grounds. *See* Prelim. Resp. 1. Patent Owner, though, requests that we “articulate which ground . . . has the highest likelihood of success so that Patent Owner can focus on addressing that ground.” *Id.* As discussed above, we determine that each asserted ground has a reasonable likelihood of prevailing. *See* Sections II.C, II.D, II.E. We do not determine on the current limited record which asserted ground would be most likely to prevail on a full record. We remind Patent Owner that “any arguments for patentability not raised in the response [after institution] may be deemed waived.” Consolidated Trial Practice Guide, 94 (Nov. 2019), *available at* <https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf>.

III. CONCLUSION

Petitioner demonstrates a reasonable likelihood of prevailing in showing that at least one of the challenged claims is unpatentable. Accordingly, we institute an *inter partes* review on all grounds of unpatentability in the Petition. At this stage of the proceeding, we have not made a final determination with respect to the patentability of any of the challenged claims.

IV. ORDER

It is hereby

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1 and 3 of the '477 patent is instituted with respect to all grounds of unpatentability set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '477 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

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