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(54) FREQUENCY INTERLEAVING METHOD FOR WIDEBAND SIGNAL GENERATION

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(57) **ABSTRACT**

Wideband signal generation systems and methods are provided which employ frequency interleaving for generating wideband signals. A general method increases a digitally synthesized signal's bandwidth by frequency interleaving multiple digitally synthesized signal sources of narrower bandwidth. Frequency interleaving creates a continuous wideband signal by summing multiple narrower band signals that overlap in frequency. According to certain embodiments, digital signal processing (DSP) and analog mixing are used to create the multiple narrower band signals such that a high fidelity, continuous wideband signal is produced when the multiple narrower band signals are summed.

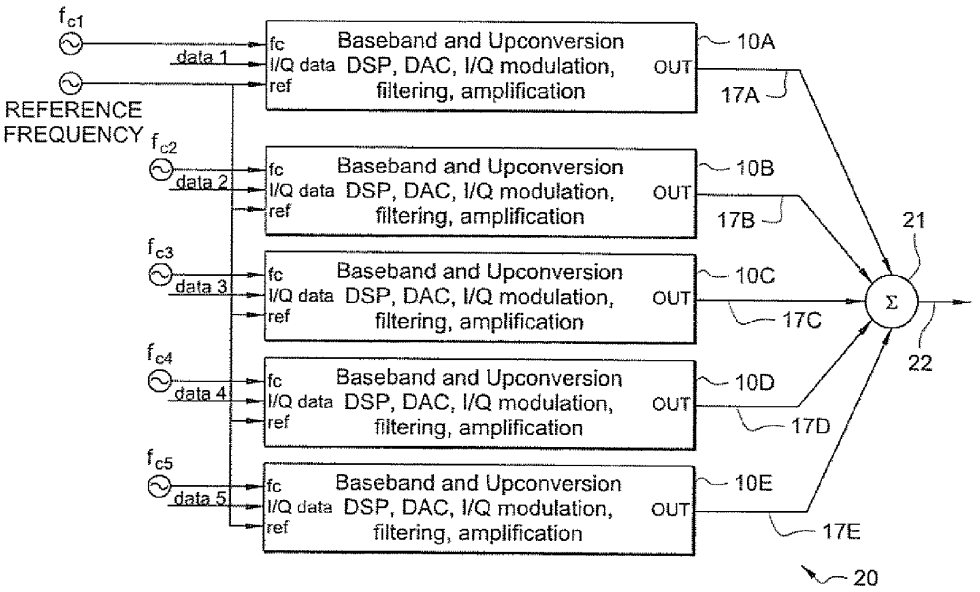


FIG. 1

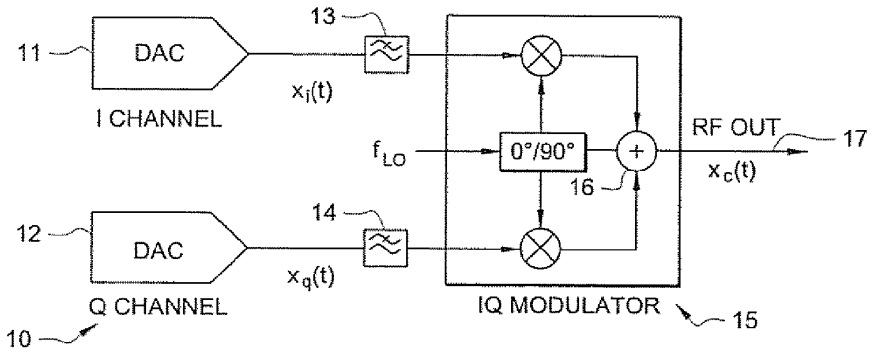



FIG. 2A

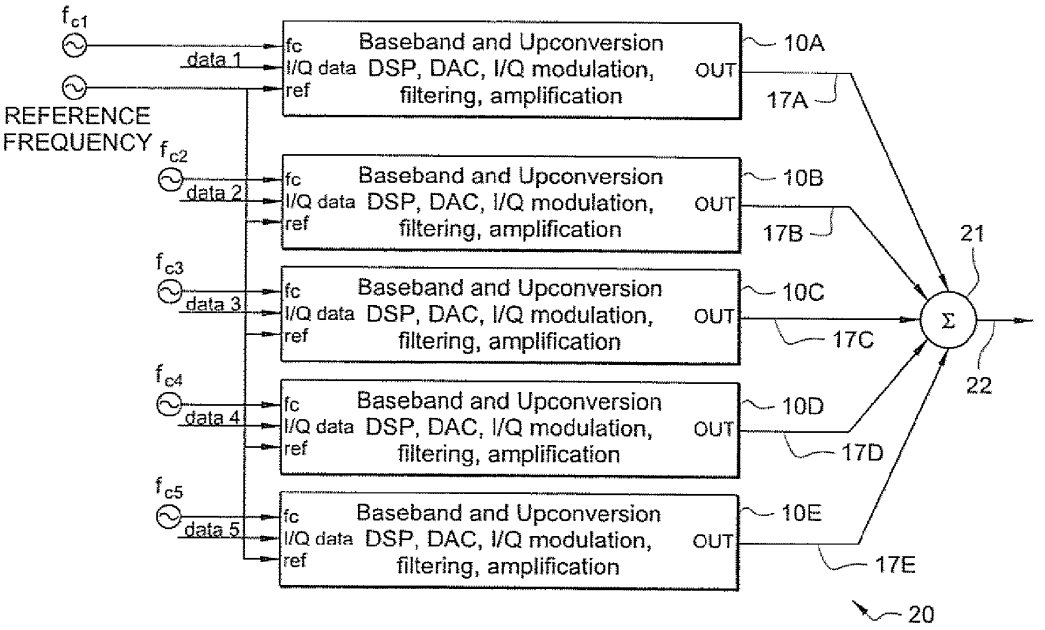



FIG. 2B

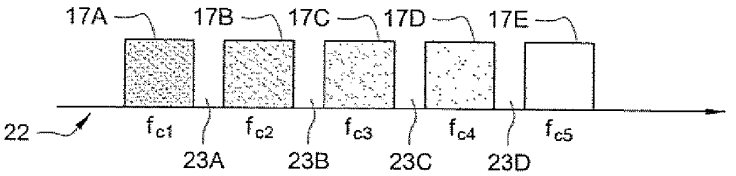


*FIG. 3*

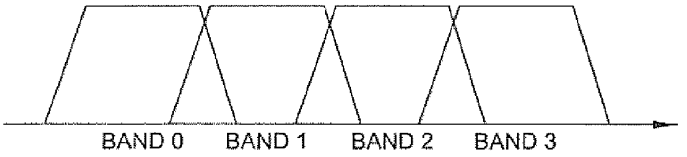



*FIG. 4*

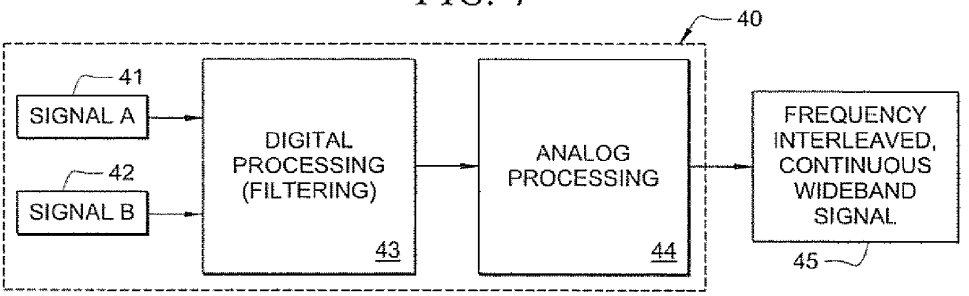



*FIG. 5*

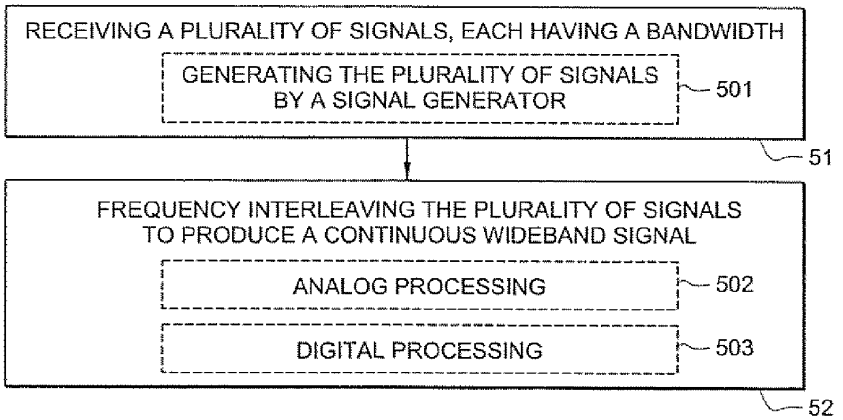


*FIG. 6*

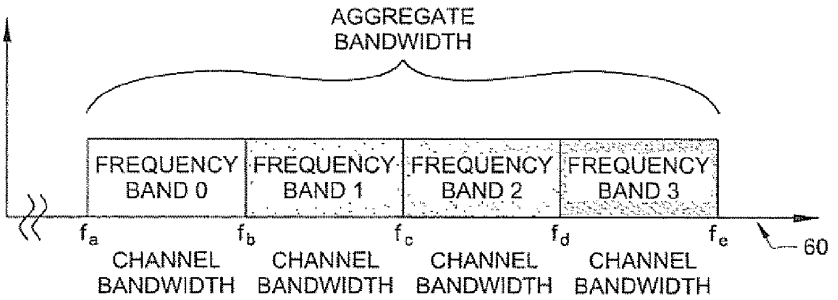

AGGREGATE BANDWIDTH
FREQUENCY BAND 0
FREQUENCY BAND 1
FREQUENCY BAND 2
FREQUENCY BAND 3
$f_a$
$f_b$
$f_c$
$f_d$
$f_e$
60
CHANNEL BANDWIDTH
CHANNEL BANDWIDTH
CHANNEL BANDWIDTH
CHANNEL BANDWIDTH

*FIG. 7*

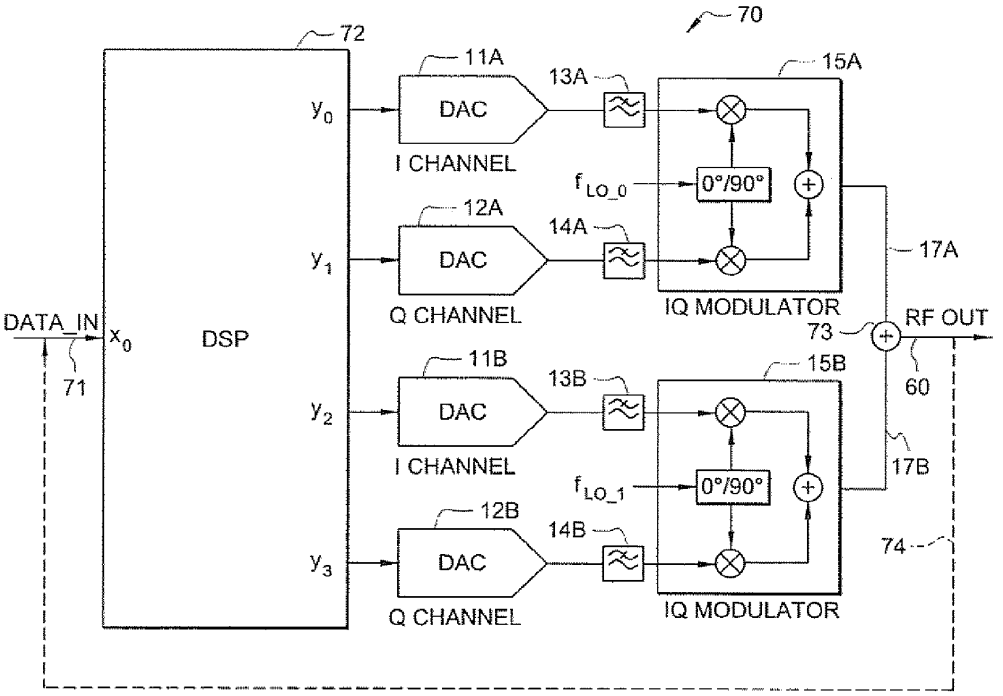

70
72
DATA_IN
$x_0$
71
DSP
$y_0$
$y_1$
$y_2$
$y_3$
11A
DAC
I CHANNEL
12A
DAC
Q CHANNEL
11B
DAC
I CHANNEL
12B
DAC
Q CHANNEL
13A
14A
13B
14B
$f_{LO_0}$
$f_{LO_1}$
0°/90°
0°/90°
15A
IQ MODULATOR
15B
IQ MODULATOR
17A
17B
73
RF OUT
60
74

FIG. 8

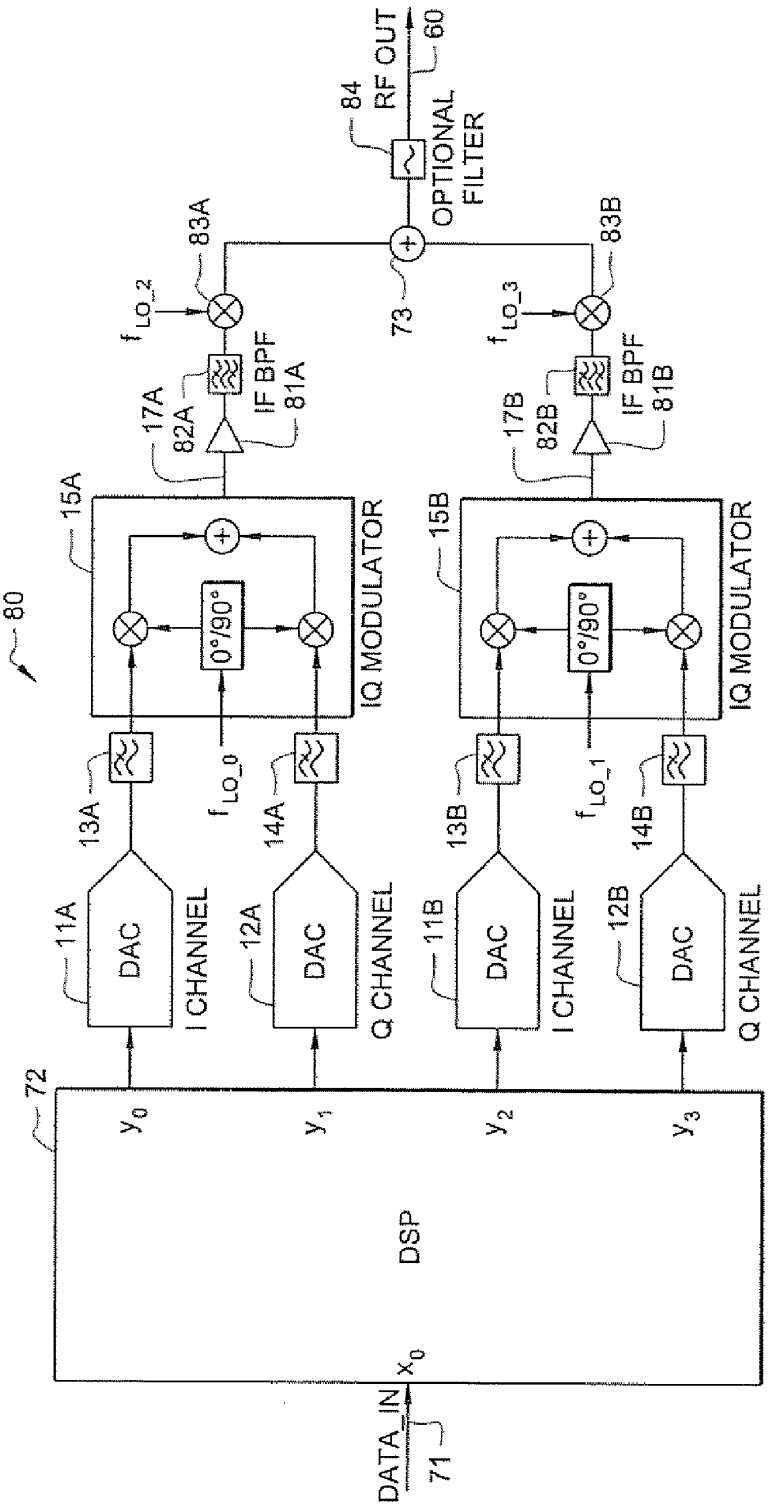

80
72
DSP
$x_0$
DATA_IN
71
$y_0$
$y_1$
$y_2$
$y_3$
11A
DAC
I CHANNEL
12A
DAC
Q CHANNEL
11B
DAC
I CHANNEL
12B
DAC
Q CHANNEL
13A
14A
13B
14B
$f_{LO_0}$
$f_{LO_1}$
15A
IQ MODULATOR
0°/90°
15B
IQ MODULATOR
0°/90°
17A
82A
17B
82B
IF BPF
81A
IF BPF
81B
$f_{LO_2}$
$f_{LO_3}$
83A
83B
73
84
OPTIONAL FILTER
RF OUT
60

*FIG. 9*

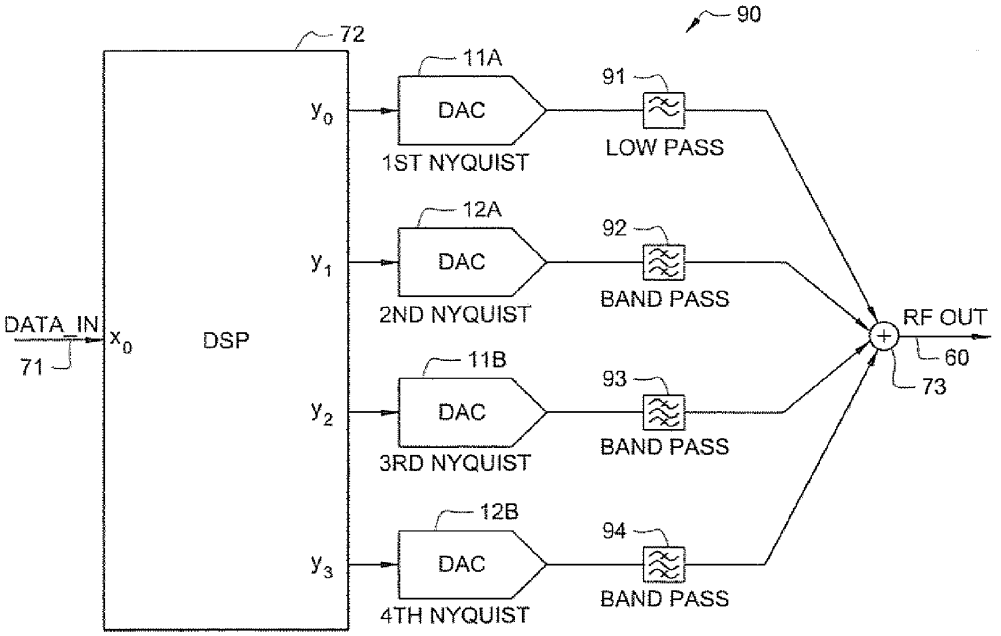
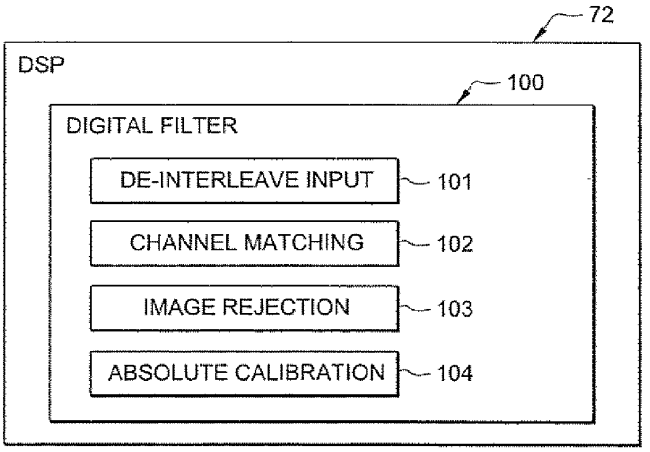

90
72
11A
91
DAC
$y_0$
1ST NYQUIST
LOW PASS
12A
92
DAC
$y_1$
2ND NYQUIST
BAND PASS
DATA_IN
$x_0$
DSP
RF OUT
71
60
73
11B
93
DAC
$y_2$
3RD NYQUIST
BAND PASS
12B
94
DAC
$y_3$
4TH NYQUIST
BAND PASS

*FIG. 10*


72
DSP
100
DIGITAL FILTER
DE-INTERLEAVE INPUT
101
CHANNEL MATCHING
102
IMAGE REJECTION
103
ABSOLUTE CALIBRATION
104

# FREQUENCY INTERLEAVING METHOD FOR WIDEBAND SIGNAL GENERATION

## TECHNICAL FIELD

**[0001]** The following description relates generally to wideband sign generation, and more specifically to systems and methods for using frequency interleaving for wideband signal generation.

## BACKGROUND OF THE INVENTION

**[0002]** Current communications systems exhibit a trend toward higher transmit and receive signal bandwidths. Such bandwidths afford greater data rates (as in WiMAX, discussed below) or allow the communication to appear as background noise that does not interfere with pre-existing wireless systems (as in UWB, discussed below). These bandwidth requirements often exceed the capabilities of state of the art signal generation and digitization solutions. Not surprisingly, test and measurement instruments follow the same trend toward generating and digitizing increasingly wider bandwidth signals, often with the additional requirement of improved dynamic range over that of commercial systems.

**[0003]** WiMAX (Worldwide Interoperability for Microwave Access) is a telecommunications technology aimed at providing wireless data over long distances in a variety of ways, from point-to-point links to full mobile cellular type access. WiMAX is based on the IEEE 802.16 standard, which is also called WirelessMAN. WiMAX allows a user to, for example, browse the Internet on a laptop computer without physically connecting the laptop to a wall jack.

**[0004]** Ultra-Wideband (UWB) is a technology for transmitting information spread over a large bandwidth (>500 MHz) that should, in theory and under the right circumstances, be able to share spectrum with other users. The FCC has authorized the unlicensed use of USE in 3.1-10.6 GHz, which is intended to provide an efficient use of scarce radio bandwidth while enabling both high data rate personal-area network (PAN) wireless connectivity and longer-range, low data rate applications, as well as radar and imaging systems. High data rate UWB can enable wireless monitors, the efficient transfer of data from digital camcorders, wireless printing of digital pictures from a camera without the need for an intervening personal computer, and the transfer of files among cell phone handsets and other handheld devices like personal digital audio and video players, as examples.

**[0005]** A desire often arises for generating a wideband digital signal. In state of the art signal generators, signal bandwidth is limited by the digital-to-analog converter (DAC) sample rate, I/Q modulator bandwidth, and the bandwidth of other analog components in the signal path. Typically, the sample rate of the DAC is the primary limitation to the generated signal bandwidth. For example, FIG. **1** shows a block diagram of a prior art signal generating system **10** that is commonly employed for generating radio frequency (RF) signals **17**. System **10** comprises an in-phase (I) DAC **11** and a quadrature (Q) DAC **12** for I and Q channels, respectively. To attempt to generate wideband signals, a DAC having as wide a band as possible may be implemented. So, a system such as that of FIG. **1** typically uses an I DAC **11** and a Q DAC **12**, which are clocked at the maximum sample rate possible. Each channel may be fed through reconstruction filters **13**, **14**, which remove higher order spectral images of the converted signal. Typically, these images are unwanted and "distort" the desired DAC output Each channel is then modulated by an IQ modulator **15**, wherein the outputs of the I and Q channel are summed by summation circuit **16** to generate an upconverted wideband signal output **17** centered at frequency $f_{LO}$ (where "LO" refers to local oscillator). That is, IQ modulator **15** receives the I and Q channels and modulates the I and Q channels by sinusoids 90 degrees out of phase. Modulation with orthogonal carriers in this manner is spectrally efficient and is prevalent in communications systems today.

**[0006]** Standard notation for complex baseband and passband signals is as follows. The baseband signal is designated $x_c(t)$ and is referred to as the complex envelope. A passband signal is designated $x_z(t)$ and is the upconverted baseband signal.

$x_z(t)=x_1(t)+jx_Q(t)$, where $x_1(t)$ and $x_Q(t)$ are real signals.

$$x_c(t)=\sqrt{2}\cdot Re[x_z(t)\cdot e^{j2\pi f_c t}]$$

$$x_c(t)=\sqrt{2}\cdot[x_1(t)\cos(2\pi f_c t)-x_Q(t)\sin(2\pi f_c t)]$$

**[0007]** DAC sample rate is the primary factor that limits signal generator bandwidth in the technique employed by the exemplary system **10** of FIG. **1**. The well-known Nyquist criterion specifies that the bandwidth of the converted analog signal can be no greater than one half (½) the DAC sample rate. Thus, when two DACs **11**, **12** feed an I/Q modulator **15** (as in the case of FIG. **1**), the upconverted output **17** has a signal bandwidth of no greater than twice (2×) that of each of the input paths. Thus, the exemplary signal generation technique of FIG. **1** is limited to R signal synthesis of signals **17** that have a bandwidth no greater than 2× the bandwidth of I DAC **11** or Q DAC **12**.

**[0008]** Additionally, as shown in the example of FIGS. **2**A and **2**B, summing the output of multiple signal generators is a common technique to create multi-carrier wireless signals. For instance, multiple signal generators, such as the exemplary signal generator **10** described with FIG. **1**, may be employed in a signal generation system **20** of FIG. **2**A, which shows such signal generators **10**A, **10**B, **10**C, **10**D, and **10**E that generate RE signals **17**A, **17**B, **17**C, **17**D, and **17**E, respectively. Such signals **17**A-**17**E are summed by summing circuit **21** to generate a multi-carrier wireless signal **22**. However, as illustrated in FIG. **2**B, such a multi-carrier wireless signal **22** is not truly wideband, as it contains "holes" in the spectrum, and the sub-carriers do not necessarily share a fixed magnitude and phase relationship. For instance, as shown in FIG. **2**B, the generated signal **22** contains the plurality of summed signals **17**A-**17**E with holes **23**A, **23**B, **23**C, and **23**D interspersed between. Thus, the exemplary summing technique of FIGS. **2**A-**2**B does not allow wideband signal generation that is free of in-band spectral discontinuities. Frequencies that lie within spectral holes **23**A, **23**B, **23**C, and **23**D cannot be synthesized with the aforementioned technique.

**[0009]** While the multi-carrier technique of FIGS. **2**A-**2**B can generate signals **22** with energy at many places in a given bandwidth, these signals have frequency "holes" (e.g., holes **23**A-**23**D). These holes exist by design so that the information content at one carrier frequency does not interfere with adjacent carriers. This approach to subdividing a larger band into sub-bands works well for a given multi-channel communication format. However, this approach is inflexible and impractical for general-purpose wideband, such as is desired for "software radio" signal generation. In the communica-

tions area, the general-purpose transceiver is often referred to as a "software radio". Other signals, such as high fidelity wideband radar chirps, are impossible to re-create using the exemplary multi-carrier technique described above.

**[0010]** Thus, a desire exists for an improved system and method for generating wideband signals.

## BRIEF SUMMARY OF THE INVENTION

**[0011]** The present invention is directed to systems and methods which employ frequency interleaving for generating wideband signals. According to embodiments of the present invention, a general method is provided to increase a digitally synthesized signal's bandwidth by frequency interleaving multiple (i.e., at least 2) digitally synthesized signal sources of narrower bandwidth. Frequency interleaving creates a continuous wideband signal (i.e., one without holes, such as holes **23**A-**23**D in the exemplary multi-carrier signal **22** of FIG. **2**B) by summing multiple narrower band signals that overlap in frequency. According to certain embodiments, digital signal processing (DSP) and analog mixing are used to create the multiple narrower band signals such that a high fidelity, continuous wideband signal is produced when the multiple narrower band signals are summed.

**[0012]** According to one embodiment, signal generation techniques are employed to generate multiple narrower bandwidth signals. For instance, a plurality of signal generators, such as the exemplary signal generator of FIG. **1**, may be employed to each generate a signal. Thus, each of the multiple signals may be generated with the maximum bandwidth possible (e.g., using the state of the art techniques). This embodiment of the present invention then employs frequency interleaving of the multiple signals to generate a wideband signal. Nat is, the signal generation system interleaves the multiple signals, each with a frequency offset, such that the signals overlap in the frequency domain.

**[0013]** Thus, according to this embodiment, the multiple signals are each generated with the same signal generation technique (e.g., the exemplary signal generation technique of FIG. **1**), and such signals are then frequency interleaved. Thus, the exemplary signal generation system of this embodiment is not limited by the sample rate of the available DACs that might be employed for generating each of the multiple signals.

**[0014]** Normally, summing frequency overlapped bands would be thought by those of ordinary skill in the art to be disastrous, since each signal channel would overlap with the adjacent channel and cause interference. However, by careful system design, it is possible to sum frequency overlapped bands, compensate for any interference, and generate the desired wideband signal. One way to mitigate this interference problem is to filter each band to remove unwanted spectral leakage. According to certain embodiments of the present invention, the burden of filtering the signals is split between analog and digital domains to allow channels to be combined and overlapped.

**[0015]** Analog filters are often used to remove unwanted spectral components (these filters include the reconstruction filters that typically follow DACs, as well as RF filters that remove unwanted components following mixing). In addition, analog filters may be used to "shape" the response of the generated signal such that signals within the passband are not attenuated and signals within the stopband are attenuated. Often, digital filtering used in conjunction with analog filters improves the desired filter response and compensates for imperfections typical of analog filters. These imperfections include non-linear phase, unflatness in the passband, slow roll of, and insufficient stopband attenuation.

**[0016]** According to one embodiment, the following actions may be performed in the analog domain:

**[0017]** a) two or more signals are synthesized using separate signal generation circuits;

**[0018]** b) these signals may be upconverted (using a device known as a mixer) to the desired center frequency;

**[0019]** c) the signals are filtered to remove unwanted spectral components;

**[0020]** d) a frequency reference is distributed between signal generation circuits to ensure a fixed frequency and phase relationship; and

**[0021]** e) a calibration procedure determines the frequency response of each signal generation circuit, as well as the phase offset (and possibly frequency offset, if it is not precisely known).

**[0022]** According to one embodiment, the following actions may be performed in the digital domain:

**[0023]** a) the input digital representation of the desired wideband signal is filtered to separate the desired aggregate wideband signal to multiple narrower band component signals;

**[0024]** b) each component signal is filtered to compensate for imperfections in the signal generation circuit (for example, sine rolloff in the DAC);

**[0025]** c) each component signal is digitally rotated to compensate for the upconverter (or I/Q modulator) frequency and phase mismatch between the multiple signal generation circuits;

**[0026]** d) each component signal is filtered to compensate for I/Q modulator imperfections; and

**[0027]** e) each component signal is filtered to compensate for frequency response mismatch between the multiple signal generation circuits.

**[0028]** The order of operations identified above is intended as only an example. In addition, multiple cascaded digital filters may be folded into a single filter for a more compact implementation according to an embodiment of the present invention. In addition it may be desirable to apply nonlinear transformations in the digital domain to compensate for nonlinear imperfections of any analog component used for signal generation or upconversion.

**[0029]** According to certain embodiments of the present invention, the multiple, narrower band signals are each generated via a respective generation path, and the paths are tied together such that each one knows about the other. So, for example, when a baseband signal is frequency translated to an intermediate or R frequency signal there is a local oscillator that is employed, wherein such local oscillator has a frequency and a phase. So, in the multiple generation paths, if the relative frequencies and phases are locked together (i.e., they may be "locked together" in this manner by reference to a common local oscillator that is used for setting their respective frequencies and phases), the multiple signals will not drift in frequency or phase relative to each other.

**[0030]** Further, according to certain embodiments of the present invention, the signal generation system accounts for the fact that oftentimes, in practice, there are delays in each signal generation path. For instance, there may exist gain imbalances or magnitude response differences between the multiple, narrower band generation paths. The signal generation system of certain embodiments removes those differ-

ences between the signal generation paths using DSP before the signal generation portion such that after the signals go through the various impairments in each path, the output is identical at each site. The output is referred to as being "identical" in this regard in that each of the multiple, narrower band signals maintain relative frequencies and phases that are locked together, and not that the output signals are duplicates of each other. The digital signal processing (DSP) is intended to equalize the magnitude, phase, I/Q imbalances, nonlinearities, and other mismatches between paths. So, the outputs from the multiple signal generation paths can be summed together to produce a high fidelity, continuous wideband signal.

**[0031]** Thus, the wideband signal generation systems and methods of certain embodiments of the present invention enable signals to be generated with a bandwidth greater than that possible with traditional, state of the art signal generation techniques. Additionally, the frequency interleaving method employed by certain embodiments of the present invention generates continuous wideband signals, thus avoiding "spectral holes" that appear in certain multi-cattier signal generation techniques, such as those discussed with FIGS. **2**A-**2**B above.

**[0032]** Additionally, for improved signal fidelity (improved interleaving image suppression), a digital approach to frequency interleaving is employed in certain embodiments of the present invention, which digitally matches channels with more accuracy than is achievable with traditional approaches. While similar filtering techniques may be employed in certain prior art systems, they have not been employed in the context of frequency interleaving.

**[0033]** The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims. The novel features which are believed to be characteristic of the invention, both as to its organization and method of operation, together with further objects and advantages will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present invention.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0034]** For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

**[0035]** FIG. **1** shows an exemplary prior art system for generating signals, wherein the bandwidth of the generated signal is limited to no greater than twice the bandwidth of a digital-to-analog converter (DAC) employed in the system;

**[0036]** FIGS. **2**A-**2**B show another exemplary prior art system for generating signals, which sums the output of multiple signal generators to create multi-carrier wireless signals that contain "holes" in the spectrum;

**[0037]** FIG. **3** shows an exemplary graph illustrating frequency overlapped bands in which each signal channel overlaps with the adjacent channel;

**[0038]** FIG. **4** shows an exemplary block diagram of a wideband signal generator according to one embodiment of the present invention;

**[0039]** FIG. **5** shows an exemplary operational flow diagram of a wideband signal generator according to an embodiment of the present invention;

**[0040]** FIG. **6** shows a graph illustrating multiple sources stitched together in the frequency domain to result in a continuous wideband signal that comprises multiple adjacent channels with no spectral "holes" therebetween according to one embodiment of the present invention;

**[0041]** FIG. **7** shows an exemplary signal generation architecture that may be employed according to embodiments of the present invention, wherein the signal generator uses I/Q modulation for frequency interleaved RF signal generation;

**[0042]** FIG. **8** shows another exemplary signal generation architecture that may be employed according to embodiments of the present invention, wherein the signal generator provides frequency interleaved RE signal generation with heterodyne upconversion;

**[0043]** FIG. **9** shows another exemplary signal generation architecture that may be employed according to embodiments of the present invention, wherein the signal generator provides frequency interleaved RE signal generation using multiple DACs operating in different Nyquist bands; and

**[0044]** FIG. **10** shows an exemplary block diagram of the digital signal processing (DSP) flow that may be implemented within a wideband signal generator of embodiments of the present invention for providing digital filtering (frequency response equalization), I/Q mismatch correction, local oscillator frequency and phase mismatch correction, and nonlinear corrections.

## DETAILED DESCRIPTION OF THE INVENTION

**[0045]** Frequency interleaving, according to embodiments of the present invention, creates a continuous wideband signal by summing multiple narrower band signals which overlap in frequency. According to certain embodiments, the frequency interleaving technique uses digital signal processing (DSP) and analog mixing to create these narrower band signals such that they create a high fidelity, continuous wideband signal when summed.

**[0046]** As the example of FIG. **3** shows, information content from multiple bands may be combined to create a continuous wideband signal with arbitrary spectral content. Practically, there will be some redundant information in each generated signal. The overlap eliminates the redundant information. According to certain embodiments of the present invention, a filtering operation equalizes the magnitude and phase variation between the summed paths. The filtering operation also allocates frequency content to each signal generator.

**[0047]** Normally, summing frequency overlapped bands would be considered disastrous by those of ordinary skill in the art, since each signal channel would overlap with the adjacent channel and cause interference, such as illustrated in FIG. **3**. One way to avoid this problem is to filter the signal. A

perfect filter with no transition band ("brick wall") is needed to place frequency content from one DAC immediately adjacent to that of another without interference. Unfortunately, such analog filters are impossible to achieve in practice.

**[0048]** Embodiments of the present invention thus split the burden between the analog and digital domains to allow channels to be combined and overlapped. According to one embodiment, the signal is partitioned between multiple upconversion channels, the channels' frequency responses are matched, and the upconverters' local oscillator phases are matched using digital filtering. The outputs of the DACs are upconverted and optionally filtered using standard analog techniques. In certain embodiments, a digital block of the system may perform absolute calibration (calibrating the output signal to a known level and phase) as well.

**[0049]** Turning to FIG. **4**, an exemplary block diagram of a wideband signal generator **40** according to an embodiment of the present invention is shown. As shown, wideband signal generator **40** comprises digital processing block **43** and analog processing block **44**. A plurality of narrower bandwidth signals, such as signals **41** and **42**, are processed by the digital processing block **43** and analog processing block **44** to perform frequency interleaving of the multiple signals **41**, **42** to generate a wideband signal **45**. As discussed further herein, the generated wideband signal **45** is referred to as being "continuous" because it does not have "holes" in between the signals contained therein, such as the holes **23**A-**23**D shown in FIG. **2**B.

**[0050]** According to certain embodiments, signal generation techniques are employed to generate the multiple narrower bandwidth signals **41**, **42** within signal generator **40**. For instance, a plurality of signal generators, such as the exemplary signal generator of FIG. **1**, may be employed to each generate one of the signals **41** and **42**. Thus, each of the multiple signals may be generated with the maximum bandwidth possible (e.g., using the state of the art techniques). The signal generator **40** then employs frequency interleaving of the multiple signals **41**, **42** to generate a wideband signal **45**. That is, the signal generator **40** interleaves the multiple signals **41**, **42** with the signals being offset in frequency such that the signals overlap in the frequency domain. Accordingly, the exemplary signal generator **40** of this embodiment is not limited by the sample rate of the available DACs that might be employed for generating each of the multiple signals **41**, **42**.

**[0051]** As discussed above, typically signal generators generate arbitrary waveforms with a bandwidth of $W_1$, where $W_1$ is less than Fs/2 in a single DAC system, where Fs is the sample rate. A signal generator with an I/Q modulator may generate signals with a bandwidth of $W_2$, where $W_2$ is less than twice Fs/2 (in other words, $W_2$ is less than Fs). This is because the bandwidth of two DACs is combined using the I/Q modulator, such as in the exemplary system of FIG. **1**.

**[0052]** However, according to an embodiment of the present invention, a frequency interleaving method is employed by a signal generator (such as signal generator **40** of FIG. **4**) which uses M DACs to generate a wideband signal having a bandwidth of $W_3$. The bandwidth $W_3$ is less than M*Fs/2, but since the number, M, of DACs employed in the signal generator can potentially be greater than 2, wider band signals can be created than is achievable with previous state of the art signal generators. For instance, according to certain embodiments, at least 3 DACs are employed.

**[0053]** As mentioned above, summing frequency overlapped bands would normally be thought by those of ordinary skill in the art to be disastrous, since each signal channel would overlap with the adjacent channel and cause interference. However, by careful system design, it is possible to sum frequency overlapped bands, compensate for any interference, and generate the desired wideband signal. One way to mitigate this interference problem is for signal generator **40** to filter each band to remove unwanted spectral leakage. According to certain embodiments of the present invention, the burden of filtering the signals is split between analog domain **44** and digital domain **43** to allow channels to be combined and overlapped.

**[0054]** Analog filters are often used to remove unwanted spectral components (these filters include the reconstruction filters that typically follow DACs, as well as R filters that remove unwanted components following mixing). In addition, analog filters may be used to "shape" the response of the generated signal such that signals within the passband are not attenuated and signals within the stopband are attenuated. Often, digital filtering used in conjunction with analog filters improves the desired filter response and compensates for imperfections typical of analog filters. These imperfections include non-linear phase, unflatness in the passband, slow roll off, and insufficient stopband attenuation.

**[0055]** In this exemplary embodiment, various operations may be performed in the digital processing block **43** and analog processing block **44**. For instance, in digital processing block **43**, such operations as filtering (FIR or IIR), phase rotation, frequency translation, and optionally nonlinear corrections may be performed, while in analog processing block **44** such operations as digital to analog conversion, image rejection filtering, mixing, upconversion, I/Q nodulation, amplification, and any further filtering may be performed.

**[0056]** FIG. **5** shows an exemplary operational flow diagram of a wideband signal generator of one embodiment of the present invention. In operational block **51**, the wideband signal generator receives a plurality of signals, each having a bandwidth. For instance, as shown in FIG. **4**, signals **41** and **42** may be received. In certain embodiments, as indicated by sub-operational block **501**, the signal generator generates such signals, thereby receiving them as a result of its generation of them. Each of the signals **41** and **42** have a narrower bandwidth than the wideband signal **45** that is generated by the wideband signal generator **40**.

**[0057]** In operational block **52**, the wideband signal generator **40** performs frequency interleaving of the plurality of signals **41**, **42** to produce a continuous wideband signal **45**. As shown in sub-operational blocks **502** and **503**, digital and analog processing of the plurality of signals may be performed to produce a high fidelity, continuous wideband signal **45**. As described above with FIG. **4**, various operations may be performed in the digital processing block **43** and analog processing block **44**. For instance, in digital processing block **43**, such operations as filtering (FIR or IIR), phase rotation, frequency translation, and optionally nonlinear corrections may be performed, while in analog processing block **44** such operations as digital to analog conversion, image rejection filtering, mixing, upconversion, I/Q modulation, amplification, and any further filtering may be performed.

**[0058]** According to one embodiment, in the analog processing sub-operational block **502**, wideband signal generator **40** may perform the following exemplary operations (by analog processing block **44** of FIG. **4**):

**[0059]** a) two or more signals are synthesized using separate signal generation circuits;

**[0060]** b) these signals may be upconverted (using a device known as a mixer) to the desired center frequency;

**[0061]** c) the signals are filtered to remove unwanted spectral components;

**[0062]** d) a frequency reference is distributed between signal generation circuits to ensure a fixed frequency and phase relationship; and

**[0063]** e) a calibration procedure determines the frequency response of each signal generation circuit, as well as the phase offset (and possibly frequency offset, if it is not precisely known).

**[0064]** According to one embodiment, in the digital processing sub-operational block **503**, wideband signal generator **40** may perform the following exemplary operations (by digital processing block **4**) of FIG. **4**):

**[0065]** a) the input digital representation of the desired wideband signal is filtered to separate the desired aggregate wideband signal to multiple narrower band component signals;

**[0066]** b) each component signal is filtered to compensate for imperfections in the signal generation circuit (for example, sine rolloff in the DAC);

**[0067]** c) each component signal is digitally rotated to compensate for the upconverter (or I/Q modulator) frequency and phase mismatch between the multiple signal generation circuits;

**[0068]** d) each component signal is filtered to compensate for I/Q modulator imperfections;

**[0069]** e) each component signal is filtered to compensate for frequency response mismatch between the multiple signal generation circuits; and

**[0070]** f) optionally, apply nonlinear transformations in the digital domain to compensate for nonlinear imperfections of any analog component used for signal generation or upconversion.

**[0071]** The order of operations described above for the analog and processing sub-blocks **502-503** is intended as only an example only. In addition multiple cascaded digital filters may be folded into a single filter in certain embodiments for a more compact implementation.

**[0072]** According to one embodiment, each channel comprises one or more DACs and an upconversion circuit. For instance, in one exemplary implementation of the signal generation system, each channel comprises an I and Q DAC, followed by reconstruction filters, followed by an I/Q modulator. Thus, each channel may be implemented as system **10** of FIG. **1** discussed above, where each channel comprises I DAC **11**, Q DAC **12**, reconstructions filters **13** and **14**, and I/Q modulator **15** for producing a signal **17**. Alternately, in certain embodiments each channel may have a single DAC, followed by a reconstruction filter, then followed by a mixer with an optional filter.

**[0073]** Alternately, in certain embodiments each channel may have a DAC and a reconstruction filter. In this case, the DAC mode provides the frequency translation by operating in the 1st, 2nd, 3rd, . . . , Nyquist zones. Note that the $2^{nd}$, $3^{rd}$, etc. Nyquist zones describe a DAC that can provide significant frequency content at a multiple of the Nyquist rate (Fs/2). For example, a DAC with energy in $2^{nd}$ Nyquist is able to generate frequency content between Fs/2 and Fs, where Fs is the sample rate. Each module is driven by one DSP block which provides the following functions: channelization, channel matching and the necessary calibration. The DSP block may contain FIR, IIR, and frequency translation components.

**[0074]** The outputs of each channel are summed using well-known techniques. One commonly used summation circuit is a resistive power combiner. Note that even the resistive combiner will not be perfectly balanced, or have a flat frequency response. Hence, calibration across the various paths (through each channel of the system, and through the power combiner itself) is preferably employed to allow N channels, each with a bandwidth of M, to operate as a single channel with a bandwidth approaching N*M.

**[0075]** According to one embodiment of the signal generator, the DAC sample clocks and mixer LOs are phase locked and low jitter to create a high signal-to-noise ratio (SNR) signal. The phase of the LOs is thus preferably known and stable Calibration may utilize a pilot tone on each of the parallel signal paths to extract the LO phase relative to the sample clock.

**[0076]** According to embodiments of the present invention, two or more baseband signals (usually generated with DACs) are frequency interleaved. FIGS. **6-9** discussed hereafter illustrate an exemplary technique employing 4 frequency interleaved DACs using a variety of frequency translation techniques. While 4 frequency interleaved DACs are employed for illustrative purposes in these techniques, it should be recognized that the concepts described herein are not limited to 4 such frequency interleavings, but may likewise be extended to any number of frequency interleavings that may be desired. FIG. **6** illustrates a concept of "stitching together" multiple sources in the frequency domain. As can be seen, FIG. **6** illustrates an exemplary continuous wideband signal **60** that comprises multiple adjacent channels with no spectral "holes" therebetween. As such, the aggregate bandwidth is a continuous wideband comprising a plurality of narrower band signals that are frequency interleaved.

**[0077]** FIGS. **7-9** show exemplary block diagrams of different signal generation architectures that may be utilized for employing the frequency interleaving concept for generating continuous wideband signals, such as signal **60** of FIG. **6**. These exemplary architectures include I/Q modulator upconversion (FIG. **7**), heterodyne/homodyne upconversion (FIG. **8**), and interleaving DACs operating in different Nyquist zones (FIG. **9**).

**[0078]** Although not explicitly shown, it should be evident that all clocks and local oscillators are phase locked in the exemplary signal generation systems now described with FIGS. **7-9**. This ensures that the frequency relationship (and consequent sampling relationship) between channels remains fixed. In addition, the digital signal processing (DSP) block in the exemplary architectures of FIGS. **7-9** allows each channel to be more perfectly matched. This step is not essential to the method of frequency interleaving. However, it improves signal fidelity by reducing unwanted interference from adjacent channels. For some applications, the signal created by frequency interleaving may be unusable (low fidelity) without DSP-assisted channel matching.

**[0079]** FIG. **7** shows one exemplary signal generation architecture that may be employed according to embodiments of the present invention. The exemplary signal generator **70** of FIG. **7** uses I/Q modulation for frequency interleaved W signal generation. In this example, signal generator **70** comprises two channels, where each channel comprises two DACs and an upconversion circuit. For instance, in this example, each channel comprises an I and Q DAC, followed by reconstruction filters, followed by an I/Q modulator. For instance, the first channel of signal generator **70** comprises I DAC **11**A, Q DAC **12**A, reconstruction filters **13**A and **14**A, and I/Q modulator **15**A; while a second channel of signal generator **70** comprises I DAC **11**B, Q DAC **12**B, reconstruction filters **13**B and **14**B, and I/Q modulator **15**B. Signal generator **70** further comprises a DSP **72**, and summation logic (e.g., a resistive power combiner) **73**. As discussed further hereafter, signal generator **70** is operable to produce a continuous wideband signal **60**, such as that of FIG. **6** discussed above.

**[0080]** In operation, DSP **71** receives a Data_In signal **71**. Digital signal processing (DSP) block **71** may be implemented using digital signal processors that are known in the art (such as those available from Texas Instruments or Analog Devices), reconfigurable logic devices known as field-programmable gate arrays (FPGAs), or custom logic known as application specific integrated circuits (ASICs), as examples. Each implementation platform has its strengths and weaknesses. The choice of one platform depends on such factors as performance, power, budget.

**[0081]** The Data_In signal **71** in this example refers to the digital representation of the desired wideband signal at the output. The DSP **72** block in this example refers to all subsequent processing of that signal in the digital domain before conversion to analog form. The processing includes in this exemplary embodiment:

**[0082]** a) the input digital representation of the desired wideband signal is filtered to separate the desired aggregate wideband signal to multiple narrower band component signals;

**[0083]** b) each component signal is filtered to compensate for imperfections in the signal generation circuit (for example, sinc rolloff in the DAC);

**[0084]** c) each component signal is digitally rotated to compensate for the upconverter (or I/Q modulator) frequency and phase mismatch between the multiple signal generation circuits;

**[0085]** d) each component signal is filtered to compensate for I/Q modulator imperfections;

**[0086]** e) each component signal is filtered to compensate for frequency response mismatch between the multiple signal generation circuits; and

**[0087]** f) optionally, apply nonlinear transformations in the digital domain to compensate for nonlinear imperfections of any analog component used for signal generation or upconversion.

**[0088]** Again, the order of operations described above for DSP block **72** is intended as an example only. In addition, multiple cascaded digital filters may be folded into a single filter in certain embodiments for a more compact implementation.

**[0089]** DSP **72** outputs the 4 separate signals (via the outputs $y_0$, $y_1$, $y_2$, and $y_3$ shown in the example of FIG. **7**). The outputs from $y_0$ and $y_1$ are received by I DAC **11**A and Q DAC **12**A, and are processed through such DACs **11**A and **12**A, reconstruction filters **13**A and **14**A, and I/Q modulator **15**A in the traditional manner as discussed above with the example of FIG. **1** to produce signal **17**A. Similarly, the outputs from $y_2$ and $y_3$ of DSP **72** are received by I DAC **11**B and Q DAC **12**B, and are processed through such DACs **11**B and **12**B, reconstruction filters **13**B and **143**, and I/Q modulator **15**B in the traditional manner as discussed above with the example of FIG. **1** to produce signal **17**B.

**[0090]** Signals **17**A and **17**B are then summed by summation circuit **73** to produce the continuous, frequency interleaved wideband signal **60**. In certain embodiments, a calibration path **74** may be provided from the output **60** to the input **71** in order to perform calibration for determining the mismatch between each path (**11**A and **12**A, **11**B and **12**B, and so on, up to **17**A and **17**B).

**[0091]** FIG. **8** shows another exemplary signal generation architecture that may be employed according to embodiments of the present invention. The exemplary signal generator **80** of FIG. **8** provides frequency interleaved M signal generation with heterodyne upconversion. As with the example of FIG. **7** discussed above, signal generator **80** comprises two channels, where each channel comprises two DACs and an upconversion circuit. For instance, in this example, each channel comprises an I and Q DAC, followed by reconstruction filters, followed by an IQ modulator. For instance, the first channel of signal generator **80** comprises I DAC **11**A, Q DAC **12**A, reconstruction filters **13**A and **14**A, and I/Q modulator **15**A; while a second channel of signal generator **80** comprises I DAC **11**B, Q DAC **12**B, reconstruction filters **13**B and **14**B, and I/Q modulator **15**B. Also like signal generator **70** of FIG. **7** discussed above, signal generator **80** further comprises a DSP **72**, and summation logic (e.g., a resistive power combiner) **73**.

**[0092]** In operation, DSP **71** receives a Data_In signal **71**. DSP **71** processes the received signal as discussed above with FIG. **7**. Further, the outputs of each channel from the DSP **71** are processed by DACs **11**A, **12**A, **18**, **12**B, reconstruction filters **13**A, **14**A, **13**B, **14**B, and I/Q modulators **15**A and **15**B to produce signals **17**A and **17**B in the manner discussed above with FIG. **7**.

**[0093]** In this exemplary embodiment, $f_{LO_0}=f_{LO_1}$. That is, the center frequency for I/Q modulator **15**A and I/Q modulator **15**B are identical. In this case, respective signals **17**A and **17**B are at the same center frequency. Amplifiers **81**A and **81**B amplify the signal and intermediate frequency (IF) bandpass filter **82**A and **82**B remove any unwanted spurs and images that are a byproduct of the I/Q modulator. Mixer **83**A and **83**B mix the signals from intermediate frequency $f_{LO}$ to the final RF frequency. With appropriate choice of $t_{LO_2}$ and $f_{LO_3}$, these two signals overlap in the frequency domain. They are summed with summing circuit **73**. Again, any unwanted spectral images or spurs generated by the mixing process are filtered out using optional bandpass filter **84**. The need for this filter depends on the mixer chosen as well as the application requirements.

**[0094]** In an implementation in which $f_{LO_0}$ does not equal $f_{LO_1}$, then the exemplary embodiment of FIG. **8** can be simplified by choosing these initial carrier frequencies for I/Q modulator **15**A and I/Q modulator **15**B such that their output signals appropriately overlap with each other in frequency. This is identical to the exemplary embodiment of FIG. **7**. Then, summing circuit **73** would follow directly after IF bandpass filter **82**A and **82**B. A mixer (such as mixer **83**A or **83**B) would then be placed following the summing circuit **73** to allow the wideband signal to be translated to a higher frequency. Again, any unwanted spectral images or spurs generated by the mixing process are filtered out using optional bandpass filter **84**. This second scenario is simply frequency translation of FIG. **7** described above.

**[0095]** FIG. **9** shows another exemplary signal generation architecture that may be employed according to embodiments of the present invention. The exemplary signal generator **90** of FIG. **9** provides frequency interleaved RF signal generation using multiple DACs operating in different Nyquist bands. As with the example of FIG. **7** discussed above, signal generator **90** comprises two channels, where each channel comprises two DACs. For instance, in this example, each channel comprises an I and Q DAC. For instance, the first channel of signal generator **90** comprises I DAC **11**A and Q DAC **12**A; while a second channel of signal generator **90** comprises I DAC **11**B and Q DAC **12**B. Also like signal generator **70** of FIG. **7**

discussed above, signal generator **90** further comprises a DSP **72**, and summation logic (e.g., a resistive power combiner) **73**.

**[0096]** In operation, DSP **71** receives a Data_In signal **71**. DSP **71** processes the received signal as discussed above with FIG. **7**. Further, the outputs of each channel from the DSP **71** are processed by DACs **11**A, **12**A, **11**B, **12**B. In this example, DACs **11**A, **12**A, **11**B, and **12**B are operating in different Nyquist bands. For instance, DAC **11**A is operating in a first Nyquist zone, DAC **12**A is operating in a second Nyquist zone, DAC **11**B is operating in a third Nyquist zone, and DAC **12**B is operating in a fourth Nyquist zone. Therefore, FIG. **9** illustrates an example of interleaving multiple DACs operating in the 1st, 2nd, 3rd, and $4^{th}$ Nyquist zones. Note, it is possible for a DAC to generate significant spectral energy centered on a frequency other than between DC and Fs/2. Various commercially available DACs operate in multiple Nyquist zones, such as the MAX19692 DAC.

**[0097]** This is typically referred to as the 1st Nyquist zone. As an example, if a doublet generating circuit at the DAC output is used instead of the typical zero order hold, significant energy is placed in the 2nd Nyquist zone. This output pulse shape modulates the DAC output with a signal at 2× the sample rate, upconverting the output signal to be centered at Fs. For practical considerations, it may be desirable in certain embodiments to modify the sampling frequencies of the component DACs such that their outputs overlap in the frequency domain.

**[0098]** The analog filters **91**-**94** included in the exemplary embodiment of FIG. **9** are used to remove extraneous spectral images in the multi-Nyquist DACs before their outputs are summed. For example, the lowpass filter **91** attenuates all images above Fs/2 (above the $1^{st}$ Nyquist zone). The band-pass filter **92** attenuates all images not between Fs/2 and Fs (the $2^{nd}$ Nyquist zone). The band-pass filter **93** attenuates all images not between Fs and 3*Fs/2 (the $3^{rd}$ Nyquist zone). The band-pass filter **94** attenuates all images not between 3*Fs/2 and 2*Fs (the $4^{th}$ Nyquist zone). In certain embodiments, frequency interleaving may be performed without the use of these filters. With appropriate choice of the phase of the DAC sample clock, these filters may become redundant. Thus, such an analogous frequency interleaving approach may be implemented without employing filters **91**-**94**, but use of the analog filters **91**-**94** may simplify the digital filters applied in block **72**.

**[0099]** As discussed above, DSP **72** may implement a digital filter. An exemplary block diagram of such a DSP **72** according to one embodiment is shown in FIG. **10**. As shown, DSP **72** may be configured to implement a digital filter **100**. Such digital filter **100** may, for example, include (but is not limited to) de-interleave input logic **101**, channel matching logic **102**, image rejection logic **103**, and absolute calibration logic **104**. The de-interleave (channelization) filter **101** partitions the input signal into sub-bands. This is accomplished by low-pass, band-pass, or high-pass filtering the input signal. Each sub-band has a narrower bandwidth than the original signal. Each sub-band shares some frequency content (overlaps) its adjacent bands. Each sub-band is synthesized as an analog waveform in separate signal generation channels.

**[0100]** The channel matching function provided by channel matching logic **102** serves to equalize the magnitude and phase across each of the digital-to-analog and upconversion paths in the system (such as the paths output by $y_0$, $y_1$, $y_2$ and $y_3$ of DSP **72** in FIGS. **7**-**9**). Such channel matching may be a desirable precursor to removing artifacts, such as signal aliases, in the output signal. Typically, this is implemented as a digital filter. One approach to remove mismatch between the measured frequency responses ($H_0$, $H_1$, $H_2$, $H_3$) of multiple channels is to calculate the average frequency response ($H_{avg}=(H_0+H_1+H_2+H_3)/4$), then calculate the channel matching filter that transforms the measured frequency response to the average. For example: the channel matching filter for Channel **0** would be $G_0=H_{avg}/H_0$.

**[0101]** The image rejection function provided by image rejection logic **103** serves as a hybrid digital/analog filter to cleanly stitch together information in each output channel, although the raw analog signals may have overlapping frequencies.

**[0102]** The absolute calibration step **104** is optional, and may be used to calibrate the signal output power (for example) to an externally referenced level. This step typically requires an external signal reference for calibration purposes.

**[0103]** The digital block (i.e., DSP **72**) may also include the functions of removing I/Q mismatch. These mismatches may be created by imbalances between the analog quadrature signals. There may be analog filtering, amplification, or PCB layout related differences between I and Q paths. Pre-correcting the I/Q data before DAC conversion can ensure frequency response mismatches are minimal and return I and Q channels to a 90-degree (orthogonal) relationship.

**[0104]** According to one embodiment, the digital filter **100** is designed using the following procedure:

**[0105]** 1.) Measure frequency response function of each channel;

**[0106]** 2.) Calculate correction filter (FIR/IIR);

**[0107]** 3.) [optional] merge with desired response;

**[0108]** 4.) [optional] calculate lower order correction filter; and

**[0109]** 5.) [optional] Iterate

**[0110]** In the above procedure, the frequency response function of each channel is first measured. The correction filter (e.g., FIR/IIR) is then calculated. In certain embodiments, the "merge" step combines the correction filter with an optional desired channel response. This optional desired channel response may be a correction to match an external reference power level (for example). The "calculate lower order correction filter" step refers to the fact that oftentimes the algorithm to determine the filter taps for the filters of steps 2 or 3 may yield filters with too many taps. Reducing the filter taps often reduces the cost and complexity of the implementation. Step 4 reduces the number of filter taps by using a lower order approximation to the "ideal" filters calculated previously.

**[0111]** Alternately, in certain embodiments, adaptive filtering is employed within the signal generator, as equalization coefficients may change over time and/or temperature.

**[0112]** Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later

to be developed that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

**1**. A method comprising:

receiving, by a wideband signal generator, a plurality of signals; and

frequency interleaving, by the wideband signal generator, the plurality of signals to produce a continuous wideband signal.

**2**. The method of claim **1** wherein said receiving comprises:

generating said plurality of signals by said wideband signal generator.

**3**. The method of claim **1** wherein said plurality of signals each have a bandwidth that is less than said continuous wideband signal.

**4**. The method of claim **1** wherein said frequency interleaving comprises:

overlapping frequencies of said plurality of signals.

**5**. The method of claim **1** wherein said frequency interleaving comprises:

aligning frequencies of said plurality of signals immediately adjacent each other.

**6**. The method of claim **1** wherein said frequency interleaving comprises digital signal processing and analog processing of the received plurality of signals.

**7**. The method of claim **6** wherein said analog processing comprises:

synthesizing the plurality of signals using separate signal generation circuits;

upconverting the plurality of signals to a desired center frequency;

filtering the plurality of signals to remove unwanted spectral components;

employing a frequency reference by the separate signal generation circuits to ensure a fixed frequency and phase relationship between the plurality of signals; and

employing calibration to determine a frequency response of each of the signal generation circuits.

**8**. The method of claim **6** wherein said digital processing comprises:

filtering an input digital representation of a desired wideband signal to separate the desired wideband signal to multiple narrower band component signals;

filtering each component signal; and

digitally rotating each component signal.

**9**. The method of claim **8** wherein said filtering each component signal comprises at least one of:

filtering each component signal to compensate for imperfections in a signal generation circuit that generated the component signal;

filtering each component signal to compensate for I/Q modulator imperfections; and

filtering each component signal to compensate for frequency response mismatch between multiple signal generation circuits that are employed for generating the plurality of received signals.

**10**. The method of claim $ wherein the digitally rotating comprises:

digitally rotating each component signal to compensate for frequency and phase mismatch between multiple signal generation circuits that are employed for generating the plurality of received signals.

**11**. The method of claim **8** wherein the digital processing further comprises:

applying a nonlinear transformation to compensate for nonlinear imperfections of any analog component used for signal generation or upconversion.

**12**. A wideband signal generator comprising:

means for receiving a plurality of signals; and

means for frequency interleaving the plurality of signals to produce a continuous wideband signal.

**13**. The wideband signal generator of claim **12** wherein said means for receiving comprises:

means for generating said plurality of signals.

**14**. The wideband signal generator of claim **12** wherein said plurality of signals each have a bandwidth that is less than said continuous wideband signal.

**15**. The wideband signal generator of claim **12** wherein said means for frequency interleaving comprises:

means for overlapping frequencies of said plurality of signals.

**16**. The wideband signal generator of claim **12** wherein said means for frequency interleaving comprises:

digital processing means; and

analog processing means.

**17**. The wideband signal generator of claim **12** comprising:

an analog processing block for generating the plurality of signals, said plurality of signals having overlapping frequencies;

a digital processing block for digitally filtering said plurality of signals; and

summation logic for combining the plurality of signals having overlapping frequencies into said continuous wideband signal.

**18**. A system comprising:

at least three digital-to-analog converters (DACs) each having a sample rate (Fs) for generating a plurality of signals; and

a wideband signal generator for receiving the plurality of signals and frequency interleaving the plurality of signals to form a continuous wideband signal having a bandwidth that is greater than the sample rate (Fs) of the DACs.

**19**. The system of claim **18** wherein the plurality of DACs comprise M DACs, where M is at least 3. and wherein the continuous wideband signal has a bandwidth $W_3$ of M*Fs/2.

**20**. The system of claim **18** wherein the wideband signal generator comprises,

a digital processing block for performing at least one of filtering, phase rotation, frequency translation, and nonlinear corrections; and

an analog processing block for performing at least one of digital-to-analog conversion, image rejection filtering, mixing, upconversion, I/Q modulation, and amplification.

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