

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BMW OF NORTH AMERICA, LLC,

Petitioner,

v.

FORAS TECHNOLOGIES LTD.,

Patent Owner.

Case IPR2024-01347
U.S. Patent 7,624,302

PATENT OWNER’S SUR-REPLY TO PETITIONER’S REPLY

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Patent Trial and Appeal Board
U.S. Patent and Trademark Office
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Alexandria, VA 22313-1450

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TABLE OF PATENT OWNER'S EXHIBITS

Exhibit No.	Description
2001	U.S. Patent No. 7,251,746 ("Fox"), dated July 31, 2007
2002	U.S. Patent No. 7,085,959 ("Safford"), dated August 1, 2006
2003	U.S. Patent No. 6,438,687 ("Klein"), dated August 20, 2002
2004	Declaration of Nigel A. Jones
2005	Curriculum Vitae of Nigel A. Jones
2006	Published Patent Application US 2006/0107112 A1
2007	Deposition Transcript of Dr. Michael Brogioli

LISTING OF CLAIMS OF U.S. PATENT NO. 7,624,302

Claim 1	
[1pre]	A method, comprising:
[1a]	detecting loss of lockstep (LOL) for a processor in a multi-processor system;
[1b]	determining that the processor for which said LOL is detected is assigned a role of boot processor;
[1c]	changing a system identifier, used by the system's operating system to recognize the boot processor, of said boot processor for which said LOL is detected, to a different value, which causes the system's operating system to not recognize the processor for which said LOL is detected as the boot processor; and
[1d]	changing a system identifier of the spare processor to that of the boot processor, thereby switching the role of boot processor to a spare processor without shutting down the system's operating system.
Claim 2	
2	The method of claim 1 wherein the spare processor is a hot spare that is held in idle until switched the role of boot processor.
Claim 3	
3	The method of claim 1 wherein the spare processor is an active spare.
Claim 4	
4	The method of claim 3 wherein said switching further comprises: causing the system's operating system to idle the active spare.
Claim 5	
5	The method of claim 1 wherein the spare processor is a processor module that includes a master and slave processors that operate in lockstep.
Claim 6	
6	The method of claim 1 wherein said determining that the processor for

	which said LOL is detected is assigned the role of boot processor comprises: accessing information stored to non-volatile data storage that identifies one of the processors in said multi-processor system that is assigned the role of boot processor.
Claim 7	
7	The method of claim 1 further comprising: determining the processor that is assigned the role of spare processor.
Claim 8	
8	The method of claim 7 wherein said determining the processor that is assigned the role of spare processor comprises: accessing information stored to non-volatile data storage that identifies one of the processors in said multi-processor system that is assigned the role of spare processor.
Claim 9	
9	The method of claim 1 wherein said determining step is performed by system firmware.
Claim 10	
10	The method of claim 1 wherein said switching step is performed by system firmware.
Claim 11	
11	The method of claim 1 wherein the processor for which said LOL is detected includes a lockstep pair of processors, and wherein said switching comprises: determining one of the lockstep pair of processors that is not the cause of said LOL; and copying the state of the determined one of said lockstep pair of processors that is not the cause of said LOL to said spare processor.
Claim 12	
12	The method of claim 11 wherein said spare processor includes a lockstep pair of processors, and wherein said copying comprises: copying the state of the determined one of said lockstep pair of processors that is not the cause of said LOL to each of said lockstep pair of processors of said spare processor.

Claim 13	
[13pre]	A method comprising:
[13a]	system firmware determining that loss of lockstep (LOL) is detected for a lockstep pair of processors that are assigned the role of boot processor in a system;
[13b]	determining one of said lockstep pair of processors that is not the cause of said LOL;
[13c]	copying the state of the determined one of said lockstep pair of processors that is not the cause of said LOL to a spare processor;
[13d]	changing a system identifier, used by the system's operating system to recognize the boot processor, of said lockstep pair of processors that are assigned the role of boot processor, to a different value, which causes the system's operating system to not recognize the lock step pair of processors for which said LOL is detected as the boot processor; and
[13e]	changing a system identifier of the spare processor to that of the boot processor, thereby switching the role of boot processor to said spare processor.
Claim 14	
14	The method of claim 13 wherein the spare processor is a hot spare that is held in idle until switched the role of boot processor.
Claim 15	
15	The method of claim 13 wherein the spare processor is an active spare.
Claim 16	
16	The method of claim 15 further comprising: causing the system's operating system to idle the active spare.
Claim 17	
17	The method of claim 13 wherein said switching causes the system's operating system to recognize said spare processor as said boot processor without shutting down said operating system.
Claim 18	

18	The method of claim 13 wherein said determining step is performed by system firmware.
Claim 19	
19	The method of claim 13 wherein said copying step is performed by system firmware.
Claim 20	
20	The method of claim 13 wherein said switching step is performed by system firmware.
Claim 21	
[21pre]	A system comprising:
[21a]	a plurality of processor modules that each include a master processor and a slave processor that operate in lockstep;
[21b]	an operating system;
[21c]	error detection logic operable to detect loss of lockstep (LOL) for at least one of said processor modules; and
[21d]	system firmware operable, responsive to the detection of LOL for a first of said processor modules, to determine whether said first processor module is assigned a role of system boot processor;
[21e]	wherein if determined that said first processor module is assigned the role of system boot processor, said system firmware is further operable to cause said operating system to recognize another processor module as system boot processor without shutting down said operating system.
Claim 22	
22	The system of claim 21 wherein the another processor module is a processor module assigned a role of spare processor.
Claim 23	
23	The system of claim 21 wherein the another processor module is held in idle until said system firmware causes said operating system to recognize said another processor module as said system boot processor.
Claim 24	

24	The system of claim 21 wherein the system firmware causes the operating system to idle the another processor module before causing said operating system to recognize said another processor module as said system boot processor.
Claim 25	
25	The system of claim 21 further comprising: non-volatile data storage storing information that assigns the role of system boot processor to one of said plurality of processor modules.
Claim 26	
[26pre]	A system comprising:
[26a]	system firmware means for detecting loss of lockstep (LOL) for a processor in a multi-processor system;
[26b]	system firmware means for determining whether the processor for which said LOL is detected is assigned the role of boot processor; and
[26c]	system firmware means for switching the role of boot processor to a spare processor without shutting down the system's operating system if determined that the processor for which said LOL is detected is assigned the role of boot processor.
Claim 27	
27	The system of claim 26 wherein said processor in said multi-processor system is an Itanium Processor Family (IPF) processor.

I. Introduction

Patent Owner's arguments were not rebutted by Petitioner's Reply and this Board should reject all of Petitioner's challenges to the claims of U.S. Patent No. 7,624,302 ("the '302 patent") and hold that the challenged claims are not unpatentable. *See, e.g.*, Paper 11, Patent Owner's Response, ("POR"), *and* Paper 14, Petitioner's Reply ("Reply").

First, Petitioner's assertion that the statement of fact remains undisputed (Paper 14, Reply, 1) is facially incorrect. Petitioner admits that Patent Owner denied Nos. 2, 3, 6, and 8 and asserted that Nos. 4, 7, and 9 cannot be admitted or denied. *Id.* Petitioner ignores Patent Owner's citations to the record evidence and fails to rebut Patent Owner's assertions that the prior art does not support Petitioner's alleged facts. *See* Paper 11, POR, 8-11.

Second, Petitioner's assertion that Patent Owner misconstrues switching the role of boot processor to the spare processor, (Paper 14, Reply, 2-6), is inherently flawed because it disassociates the role of the boot processor from the boot process. Switching identification of the boot processor without reference to booting seems to miss the point. And to be sure, Patent Owner did not confuse a boot device with a boot processor as Petitioner contends. *Id.*, 6. Patent Owner simply noted that the '302 Patent teaches how boot information, such as the boot device path, can be

persistently stored for the next time the system reboots, Paper 11, POR, 27. Neither Patent Owner nor Mr. Jones conflated a boot device and a boot processor.

Third, Petitioner's reiteration of its Ground 1 arguments, (Paper 14, Reply, 7-10), continues to rest upon the flawed premise that the boot processor does not need to be involved with the boot process and neither the Petition nor the Reply explain how copying the context or state of a processor would affect the role of boot processor while booting or rebooting.

Fourth, Petitioner's reiteration of its Ground 2 arguments, *id.*, 10-12, rests upon the same flawed premise as Ground 1, that the boot processor does not need to be involved with the boot process, and neither the Petition nor the Reply explain how designating a logical CPU0 would have the effect of switching the role of boot processor. Nor does Petitioner address Patent Owner's observation that Petitioner's arguments are defective because the additional prior art identified by Petitioner in Ground 2, Ex. 1011, U.S. Patent No. 5,408,647 ("Landry"), teaches processor selection during system initialization, which is irrelevant to the challenged claims of the '302 Patent that recite "without shutting down the operating system." Paper 11, POR, 35.

Fifth, Petitioner does not rebut Patent Owner's challenges regarding the evidentiary deficiencies and glaring inconsistencies of the unsubstantiated hearsay

documents Petitioner attempts to rely on to fill in the gaps in the prior art Petitioner cites as grounds for its invalidity challenges. *See* Paper 11, POR, 16-17, 20-24; Paper 14, Reply, 12-16. Petitioner does not credibly explain why a document (IA-32) purportedly available in 2002 has a 2003 copyright date, nor does Petitioner explain why a marked-up document with unaccepted tracked changes (MP Specification) would have been publicly distributed. Paper 14, Reply, 15-16.

Sixth, Petitioner asks this Board to construe a single sentence description of an alternative embodiment in isolation and without reference to the entirety of the rest of the specification in Ex. 1005, Patent Application Publication US 2005/0172164 A1 (“Fox”). *See* Paper 14, Reply, 16-19. Petitioner does not address Petitioner’s declarant’s conflation of a hot-spare processor and an active spare processor, Paper 11, POR, 42, or that Fox only discloses idling a failing processor, but not a functioning active processor. *Id.*, 44.

Seventh, Petitioner does not refute that neither claim 24 nor claims 11, 12 or 17 were specifically addressed in the Petition. Petitioner instead argues that Patent Owner and the Board should have somehow inferred Petitioner’s arguments for claim limitation [21e]. Paper 14, Reply, 18. Somewhat astonishingly, Petitioner also argues that Patent Owner should have exceeded the proper scope of cross examination by questioning Dr. Brogioli about matters outside of his declaration –

claim 24 and whether Fox discloses idling an active processor. *Id.*, 18-19. As Patent Owner noted, neither the Board nor the Patent Owner are obliged to decode the petition to locate additional arguments beyond the ones clearly made. Paper 11, POR, 49. Both the Petition and Dr. Brogioli's declaration are silent as to why claim 24 and claims 11, 12 or 17 are allegedly unpatentable, and Petitioner's post-hoc efforts to cobble together an invalidity challenge that was not presented in the Petition should be rejected. *Id.*, 48-50.

Eighth, Petitioner's arguments that a POSITA would understand that multi-processor system main memory would be non-volatile memory or that RAM is non-volatile (Paper 14, Reply, 19-20) are simply incorrect for the reasons stated in Patent Owner's Response. Paper 11, POR, 45-48.

Ninth, Petitioner concedes that the Petition is silent with respect to claims 11, 12 and 17 by asserting, without justification, that the limitations were discussed with reference to [1a], [13b], and [13c], or [1d], [13e], and [21e]. Paper 14, Reply 21-22. Petitioner's argument is the antithesis of identifying with particularity the evidence that supports the grounds for the challenge to each claim. *See Intelligent Bio-Systems, Inc. v. Illumina Cambridge, Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (quoting 35 U.S.C. § 312(a)(3) (2012)). This Board should reject Petitioner's efforts to cobble together an invalidity challenge that was not made in the petition.

Tenth, this Board should reject Petitioner's contentions that Mr. Jones's testimony lacks sufficient factual basis and does not reflect the knowledge and skill of a POSITA. Paper 14, Reply, 22-24. As discussed below, Petitioner's contentions are contrary to Mr. Jones's sworn deposition testimony and declaration and are further premised, at least in part, on Petitioner's erroneous understanding of what the role of a boot processor is and Petitioner's efforts to somehow identify the role of a boot processor as separate and distinct from the boot process itself.

II. Petitioner's Material Facts Were and Are Disputed and Should not be Deemed Admitted.

As noted above, Petitioner's assertion that the statement of fact remains undisputed (Paper 14, Reply, 1) is facially incorrect. Petitioner admits that Patent Owner denied Nos. 2, 3, 6, and 8 and asserted that Nos. 4, 7, and 9 cannot be admitted or denied. *Id.* Petitioner's complaints ignore Patent Owner's citations to contrary record evidence and Patent Owner's still undisputed particularized assertions where the prior art cited by Petitioner does not support Petitioner's alleged fact. *See* Paper 11, POR, 8-11.

III. Petitioner erroneously separates the "role of the boot processor" from the boot process.

Petitioner's assertion that Patent Owner misconstrues switching the role of boot processor to the spare processor, (Paper 14, Reply, 2-6), is inherently flawed

because Petitioner seeks to disassociate the role of the boot processor from the boot process itself. Petitioner admits that the boot processor “perform[s] system initialization and booting the operating system during the boot process,” *id.*, 3 (emphasis added), but apparently denies that these are part of the role of the boot processor. It is only by so doing that Petitioner is able to argue that the system identifier used to identify the boot processor does not need to persist.

Petitioner's argument that “requiring the spare processor to perform initialization after system reboots” is contrary to “without shutting down the system's operating system” (*id.*, 4) is just wrong. Changing a persistent system identifier will allow the spare processor to perform all of the boot processor responsibilities, and not just the limited subset (controlling various system functions after the boot process) Petitioner identifies.

Petitioner, apparently not understanding “for example,” wrongly contends that Patent Owner confused a boot device with a boot processor. *Id.*, 6. Patent Owner simply noted that the '302 Patent teaches how boot information, such as the boot device path, can be persistently stored for the next time the system reboots, Paper 11, POR, 27. Neither Patent Owner nor Mr. Jones conflated a boot device and a boot processor. Rather, what was pointed out was that the '302 Patent specification describes a specific approach by which a persistent identifier used during the boot

process is changed without shutting down the operating system.

IV. Ground 1 does not render obvious switching the role of the boot processor and the spare processor.

Petitioner's reiteration of its Ground 1 arguments, (Paper 14, Reply, 7-10), continues to rest upon the flawed premise that the boot processor does not need to be a boot processor. It is only by ignoring the primary responsibility of the role of boot processor (*i.e.*, booting) that Petitioner can argue that switching the logical APIC IDs of the boot processor and a spare processor would switch the roles. *Id.*, 8. However, as explained in the POR, switching an identifier in non-volatile memory would not switch the role of the boot processor during the boot process – a role that plainly encompasses performing system initialization after the system reboots. Paper 11, POR, 24-30.

Neither the Petition nor the Reply explain how copying the context or state of a processor would affect the role of boot processor, especially with respect to booting or rebooting the system. *Id.*, 28. Copying the context or state of a failing processor to a spare processor applies to any processor, and that alone, even in combination with switching a non-volatile ID that would not persist through a system reset, would not switch the role of boot processor. *Id.*, 28-30.

V. Ground 2 does not render obvious switching the role of the boot processor and the spare processor.

Petitioner's reiteration of its Ground 2 arguments, *id.*, 10-12, rests upon the same flawed premise as Ground 1, that the boot processor does not need to be involved with the boot process, and neither the Petition nor the Reply explain how designating a logical CPU0 would have the effect of switching the role of boot processor.

Significantly, Petitioner does not address Patent Owner's observation that Petitioner's arguments are defective because the additional prior art identified by Petitioner in Ground 2, Ex. 1011, U.S. Patent No. 5,408,647 ("Landry"), teaches processor selection during system initialization, which is irrelevant to the challenged claims of the '302 Patent that recite "without shutting down the operating system." Paper 11, POR, 35.

VI. Petitioner's invalidity challenges should be limited to the patents and published patent applications cited by Petitioner without resort to unsubstantiated documents that have not been established as prior art.

Petitioner does not rebut Patent Owner's challenges regarding the evidentiary deficiencies and the glaring inconsistencies of the unsubstantiated hearsay documents that Petitioner attempts to rely on to fill in the gaps in the prior art Petitioner cites as grounds for its invalidity challenges. *See* Paper 11, POR, 16-17, 20-24; Paper 14, Reply, 12-16. The Petition relies extensively on IA-32 Intel® Architecture Software Developer's Manual, Vol. 3: System Programming Guide,

(“IA-32”) with approximately thirty (30) separate multi-page citations. *See* Paper 1, Petition, *passim*. Petitioner plainly felt it was necessary to do so because the Fox prior art does not disclose, teach or suggest what Petitioner contends it does, such as, for example, a boot processor or a BSP flag. Paper 11, POR, 16, 20.

Petitioner apparently believes that Ex. 1009, an Internet Archive declaration and webpages from 2002 are evidence of the public availability of Ex. 1008, IA-32, but fails to explain why a 2002 web page is relevant to a documentary exhibit that, on its face, is from 2003. There is no way that a document from 2003 would be available to a POSITA in 2002 using a webpage in 2002.

Petitioner's efforts to establish the public availability of Ex. 1028, MP Specification are equally deficient. As explained in the POR, Ex.1028 is a marked-up version that includes unaccepted tracked changes which plainly indicate that Petitioner's version was an ongoing draft that presumably never left Intel (irrespective of whether a previous finalized version could be obtained from Intel). Paper 11, POR, 23.

VII. Grounds 1 and 2 do not render obvious the “active spare” dependent claims 3, 4, 15, and 16 because there is no teaching in the prior art of idling an active processor and Dr. Brogioli's deposition testimony demonstrates that he did not appreciate the distinction between active and hot spare processors.

Petitioner asks this Board to construe a single sentence description of an alternative embodiment in Fox in isolation. *See* Paper 14, Reply, 16-19. However, as detailed in the POR, Petitioner's reading is both unfounded and contrary to Fox's teachings. Paper 11, POR, 38-44. And, as also detailed in the POR, but unrebutted by Petitioner, Fox is silent regarding the steps necessary to make an active spare a hot spare. *Id.*, 39-41.

Petitioner also does not address Petitioner's declarant's conflation of a hot-spare processor and an active spare processor shown below. Paper 11, POR, 42.

Petitioner is apparently arguing that a hot-spare processor and an active spare processor are the same as Dr. Brogioli testified.

- 4 Q. So are you saying that that
5 processor is **still** a hot-spare processor and
6 now that it's been added to the active list
7 is **also** an active spare?
8 A. That seems to me the language
9 that Fox is using.
10 Q. Is that your understanding of
11 Fox?
12 A. Yeah. That's what he is saying
13 and that is why these sequences of
14 paragraphs are what show both -- taking us
15 back to my declaration -- what is both

16 dependent claim 13 and dependent claim 14.
Ex. 2007, Brogioli Dep. Tr., 78:4-16 (emphasis added).

Petitioner also does not dispute that Fox only discloses idling a failing processor but is silent regarding idling a functioning active processor. Paper 11, POR, 44.

Petitioner relies on the same disclosure in Fox for claims 3, 4, 15 and 16, but, as explained above and in the POR, a POSITA would not understand that Fox discloses, teaches, or suggests using an active spare instead of a hot-spare. Accordingly, Petitioner has not met its burden to establish that claims 3, 4, 15 and 16 are unpatentable.

VIII. Grounds 1 and 2 do not render obvious the “active spare” dependent claim 24 because the Petition is devoid of any arguments applying the prior art to claim 24 .

Petitioner does not refute that neither claim 24 nor claims 11, 12 or 17 were specifically addressed in the Petition. Petitioner instead argues that Patent Owner and the Board should have somehow inferred Petitioner's arguments for claim limitation [21e] applied to claim 24. Paper 14, Reply, 18. Petitioner's flawed attempt to shift Petitioner's burden to Patent Owner must be rejected. It is the Petitioner, not the Patent Owner, who bears the burden of persuasion in an *inter partes* review. “In an [*inter partes* review], the petitioner has the burden from the

onset to show with particularity why the patent it challenges is unpatentable.”
Harmonic Inc. v. Avid Tech., Inc., 815 F.3d 1356, 1363 (Fed. Cir. 2016).

This Board should reject Petitioner's assertion that Patent Owner should have exceeded the proper scope of cross examination by questioning Dr. Brogioli about matters outside of his declaration – claim 24 and whether Fox discloses idling an active processor. *Id.*, 18-19. Neither the Board nor the Patent Owner are obliged to decode the petition or accompanying declaration to locate additional arguments beyond the ones clearly made. Paper 11, POR, 49. Because the Petition and Dr. Brogioli's declaration and deposition testimony are devoid of any application of the prior art to claim 24 (and claims 11, 12 or 17), Petitioner's post-hoc efforts to cobble together any invalidity challenges that were not presented in the Petition should be rejected. *Id.*, 48-50.

IX. Petitioner has not established that claims 6, 8 and 25 are rendered obvious because a POSITA would not have understood that multi-processor system main memory would be non-volatile or that RAM is non-volatile memory.

As discussed in the POR, Petitioner's arguments regarding the non-volatile data storage limitations of claims 6, 8, and 25 are unavailing.

Petitioner does not dispute that Fox does not disclose storing the information Petitioner alleges corresponds to the claimed information identifying “one of the processors” (e.g., processor register or table) in system memory or that Arai

discloses storing similar information (*e.g.*, ACPI or MP table) in main memory. Petitioner attempts to remedy these deficiencies by arguing that main memory in a multi-processor system would be non-volatile memory such as ROM (per Dr. Brogioli) and that, despite the absence of any disclosure or teaching to that effect, that Fox's register or table would have been stored in Fox's system memory and that the multiprocessor system memory would be non-volatile. Paper 1, Petition, 59-62, 65. Petitioner did not provide any teachings of a multiprocessor system with non-volatile system memory, and a POSITA would not have understood that multiprocessor system memory was non-volatile in the absence of such teachings.

Petitioner also apparently argues that a POSITA would understand that RAM is nonvolatile. Paper 14, Reply, 20. Petitioner's assertion is an unwarranted logical leap premised on the existence of non-volatile RAM (NVRAM), a logical step which ignores the straightforward fact that NVRAM is distinguished from RAM because RAM is volatile. And data stored in volatile memory such as RAM would not persist through a reset. Ex. 2005, Jones Dec., ¶ 36.

Accordingly, Petitioner has not met its burden to establish claims 6, 8, or 25 would have been obvious over the asserted prior art.

X. This Board should reject Petitioner's attempts to assert invalidity challenges to claims 11, 12, 17 and 24 because the Petition is devoid of any arguments applying the prior art to claims 11, 12, 17 or 24.

Petitioner's efforts to cobble together an invalidity challenge to claims 11, 12, 17, and 24 in the Reply should be rejected by this Board. The Federal Circuit has "rejected, many times, post-hoc attempts on appeal to include additional, new arguments not contained in the petition." *Netflix, Inc. v. DivX, LLC*, 84 F.4th 1371, 1377 (Fed. Cir. 2023) (citing *Microsoft Corp. v. Biscotti, Inc.*, 878 F.3d 1052, 1074 (Fed. Cir. 2017)).

"[T]he Board should ... not have to decode a petition to locate additional arguments beyond the ones clearly made." *Netflix, Inc. v. DivX, LLC*, 84 F.4th 1371, 1377 (Fed. Cir. 2023). "It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify 'with particularity' the 'evidence that supports the grounds for the challenge to each claim.'" *Intelligent Bio-Systems, Inc. v. Illumina Cambridge, Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016). The Federal Circuit has further "held that the Board erred when it relied on a prior art reference that was unasserted for meeting a particular limitation, even though the passage from the reference that the Board relied on for disclosing the limitation had been block quoted in the petition and institution decision, in a different context." *Oren Techs., LLC v. Proppant Express Invs. LLC*, 2021 U.S. App. LEXIS 21859, *14 (Fed. Cir. July 23, 2021) (citing *Emera-Chem*

Holdings, LLC v. Volkswagen Grp. of Am., Inc., 859 F.3d 1341, 1350 (Fed. Cir. 2017).

There is no basis for finding claims 11, 12, 17, or 24 are unpatentable in the absence of any arguments linking the prior art to the claims in the Petition (with or without particularity) in this *inter partes* review proceeding.

XI. This Board should consider Mr. Jones's testimony dispositive.

Petitioner's contentions that Mr. Jones's testimony lacks sufficient factual basis and does not reflect the knowledge and skill of a POSITA, (Paper 14, Reply, 22-24), are contrary to Mr. Jones's sworn deposition testimony and declaration.

Petitioner's first objection, that Mr. Jones improperly interprets a boot processor as the processor used to "boot," (*Id.*, 23), simply reflects Petitioner's efforts to nonsensically separate a "boot processor" from the process of booting. Petitioner's second objection, that Mr. Jones assumed that a "boot device" is a "boot processor," *id.*, reflects Petitioner's failure to understand that "for example" refers to the approach of persistent storage of configuration data in non-volatile memory as shown in the citations to the '302 patent in paragraph 32 of Mr. Jones's Declaration.

Petitioner's second objection, that Mr. Jones's testimony does not reflect a POSITA, cannot be reconciled with Mr. Jones's extensive deposition testimony of

forty (40) years of experience designing complex electronic systems, including strip chart recorders, PID controllers, electromechanical systems, life-support systems, control systems, smart batteries, microwave telecommunication links, a networking card, an encrypted circuit board manufacturing line, a near-infrared moisture gauge, electromagnetic and radiofrequency-based cable system detectors, etc. Ex. 1007, Jones Dep. Tr., 21:20-23:21.

Petitioner's third objection, that Mr. Jones considered the documents cited in his declaration and the Petition itself, (Paper 14, Reply, 24) is not an indictment against Mr. Jones as he fully explained the bases for his opinions in his declaration. *See, e.g.*, Ex. 2004, ¶¶ 31-39; 42-44; 48-51; 55.

Petitioner's fourth objection, that Petitioner disagrees with Mr. Jones's testimony, (Paper 14, Reply, 24), appears premised on incomplete citations to Mr. Jones's testimony. For example, Mr. Jones testified that:

17 The word 'processor'
18 appears over 350 times in Fox. Not once is it
19 qualified with the word 'boot.' In fact, booting
20 isn't even really mentioned in Fox. And so I
21 think someone reading Fox would conclude that how
22 the system is booted is irrelevant to what Fox is
1 claiming is his invention.

Ex. 1007, Jones Dep. Tr., 81:17-82:2. Mr. Jones also testified that:

13 A person of ordinary skill in the art
14 wouldn't have to know what a boot processor is,
15 because the specification for the '302 lays out
16. what a boot processor is. And so whether there's
17. a person of ordinary skill in the art that has a
18. different definition, a narrower or broader, I
19 obviously cannot comment. But the '302
20 specification, as I cite here in my declaration at
21 Paragraph 33, does give a description on what a
22 boot processor is.

Ex. 1007, Jones Dep. Tr., 69:13-22. Mr. Jones also testified that, because the specification of the '302 Patent spells out what a boot processor is at column 12, lines 1 through 21, what is relevant to the patentability of the '302 Patent claims is that definition in the '302 Patent. *Id.*, 74:13-75:1.

Accordingly, Mr. Jones's sworn testimony is not based on only a small subset of the record and is, as apparent from his declaration, based on cited admissible facts from the perspective of a POSITA and Petitioner's contrary assertions are belied by the sworn testimony on the record and should be disregarded.

XII. Conclusion

Petitioner has failed to meet its burden of establishing that the Challenged Claims are unpatentable and the Petition should be denied for all claims.

Dated: October 24, 2025

Respectfully submitted,

/s/ Brett Cooper

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CERTIFICATE OF WORD COUNT (37 C.F.R. § 42.24(d))

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