

RF Circuits Technique of Dual-band Transceiver IC for GSM and DCS1800 applications

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Abstract

This paper describes a dual band transceiver IC for small and low cost handsets applied to GSM and DCS 1800 applications. The IC fabricated in a $0.35\mu\text{m}$ SOI BiCMOS process includes a dual band receiver, transmitter, and synthesizers. The receiver contains on-chip LNAs, and low distortion mixers. The evaluation results of the LNA of GSM and DCS1800 show gain of 18.8dB, 13.5dB, NF of 1.7dB, 1.8dB, and ICP of -8.8dBm, -8.8dBm, respectively. The mixer results for GSM are gain of 9.2dB, NF of 8.9 dB and ICP of -4.5 dBm. The mixer results for DCS1800 are gain of 10.8 dB, NF of 8.7 dB and ICP of -3.8 dBm. The reference sensitivity of -107.8 dBm for GSM and -108.3 dBm for DCS 1800 were obtained.

1. Introduction

Transceiver IC for mobile communication is required to implement small, low cost, and low power handsets. Lately, an IC applied to dual band applications has been developed [1,2]. Some of the authors have already developed and reported a dual band transceiver IC that utilizes a transmitter using an offset phase locked loop (OPLL) technique [3]. This paper describes an enhanced RF analog receiver of the dual band transceiver IC designed to GSM and DCS1800 applications. This

receiver contains two on-chip low noise amplifiers (LNAs) and two low distortion 1st mixers for the dual band applications. The LNA ensured high gain and linearity by using emitter degeneration technique and low noise figure (NF) by optimizing elements of the circuit. The mixer improved linearity by applying emitter-decoupling scheme. Those two circuit techniques are discussed in detail in the later section.

2. Architecture

Figure 1 shows a block diagram of a whole transceiver, where this IC is drawn inside the large, thick polygon. The IC contains the dual-IF receiver that consists of two LNAs, two 1st mixers (1st MIX), a 2nd mixer (2nd MIX), a programmable gain amplifier (PGA), and a quadrature demodulator (QDEM), and in the transmitting path, a quadrature modulator (QMOD) and an OPLL. The decoder controls the gain of the 1st MIX, 2nd MIX and PGA using serial data from a baseband LSI. The IC also contains the dual-RF synthesizer, a frequency divider (DIV) with on-chip VHF-voltage controlled oscillator (VCO), a band-selection circuit which selects the GSM or DCS1800 mode, and the power-control circuit which selects the transmitting, receiving, and idle mode.

The decoder and switches for the band selection are implemented with CMOS transistors, whereas the others

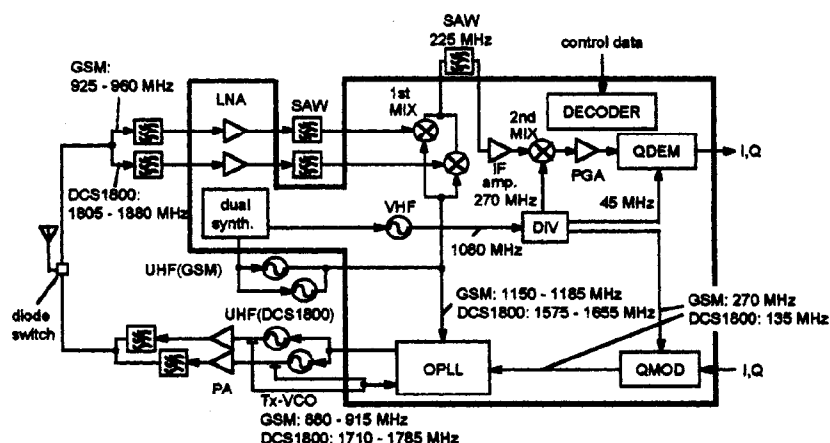


Figure 1. Block diagram of RF section

with bipolar transistors. Except for the decoder and the VHF-VCO, all circuits are designed as a differential type to eliminate common mode noise.

2.1. 0.35 μm SOI BiCMOS technology

The IC was fabricated in a 0.35 μm SOI BiCMOS process. By applying the trench isolation technology and the silicon on insulator (SOI) substrate technology, the capacitance between the collector of the transistor and the substrate is reduced. Figure 2 shows the relationship of capacitance of the substrate (C_{sub}) and f_T . As C_{sub} of this process is half of the conventional bipolar processes, and the f_T of a minimum size transistor was improved. This process enables RF circuits to obtain high gain and speed.

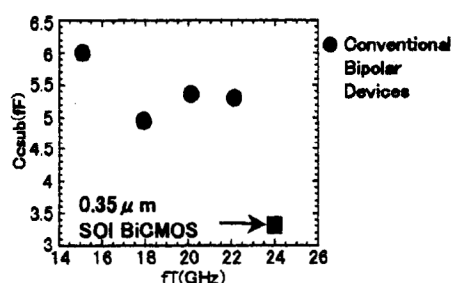


Figure 2. C_{sub} depend on f_T

2.2. LNA

Figure 3 shows a circuit schematic of the on-chip LNA in figure 1. The bias circuit of LNA is based on the current mirror circuit scheme. With circuit scheme employed for the both applications, the LNA for GSM has one ground pin and the LNA for DCS1800 has two ground pins. The band gap reference circuit (BGR) provides the stable bias current level to bias transistor Q2 regardless of deviation of power supply voltage and the temperature. Transistor size was compromised to reduce the base resistance and the capacitance of the transistors, i.e. C_{be} and C_{μ} . The resistor R1 intercepts the noise from Q2 and BGR. It also supplies the bias voltage to the base of Q1. It was also optimized to obtain good NF and to avoid large voltage drop at the base of Q1. The ground pins were separated between Q1 and Q2 to avoid resonance caused by parasitic capacitance included in such as transistor Q2, BGR and the inductance of bonding wires. The inductance of the bonding wire on the emitter of Q1 produces negative feedback called emitter degeneration. It improves linearity, however, decreases gain. As the LNA for DCS1800 has two parallel connected ground pins, the inductance is reduced in half and the LNA ensures high gain. To meet the requirement of high linearity, the LNA for GSM has off-chip additional 1nH inductor between the emitter of Q1 and the ground. The input 1dB compression point (ICP) was improved by 5dB because of the additional inductance described above. The LNA

circuit includes protection circuit against electrostatic discharge (ESD). The components of 50 Ω matching circuits are off-chip.

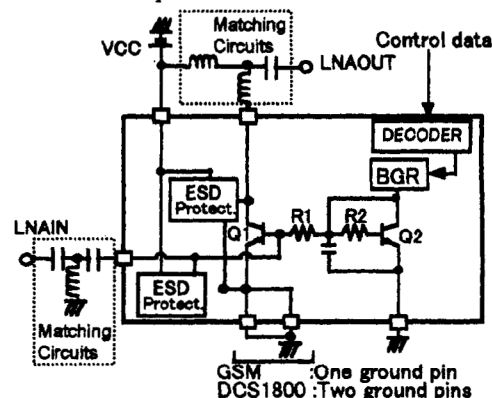


Figure 3. The LNA circuit

The evaluation results of the LNA for GSM and DCS1800 are shown in figures 4 and 5. At 3.0V power supply, gain of 18.8dB and NF of 1.7dB for GSM at the center frequency 940MHz were achieved. For DCS1800 gain of 13.5dB and NF of 1.8dB at the center frequency 1840MHz were achieved. Both input and output VSWRs were less than 2 in these applications. The current level of LNAs was 4.5mA each. The ICP was -8.8dBm for GSM and -8.8dBm for DCS1800.

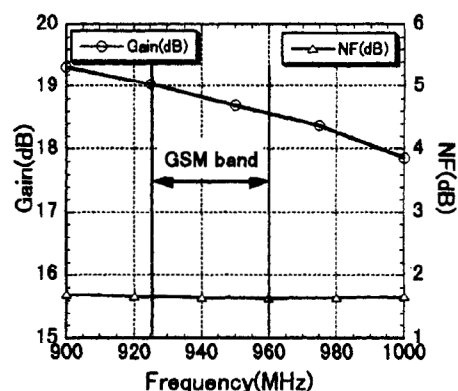


Figure 4. Gain and NF for GSM

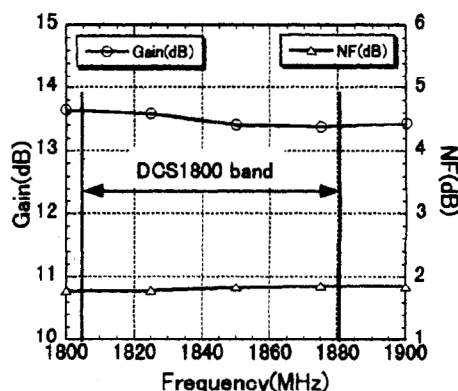


Figure 5. Gain and NF for DCS1800

2.3. MIX for GSM

Linearity of the 1st MIX for GSM was improved by an emitter-decoupled circuit configuration. A source-decoupled technique for linear CMOS RF circuits has been reported [4]. However, the advantages of the source-decoupled circuit are not completely clarified. Here, the advantages of the emitter-decoupled circuit is discussed in detail and clarified by comparing with emitter-coupled circuit.

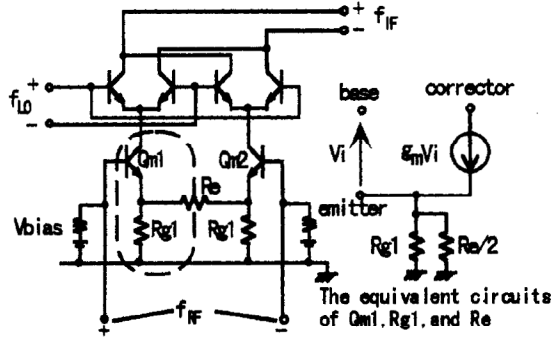


Figure 6. GSM 1stMIX
Emitter-coupled circuit (MIX-C)

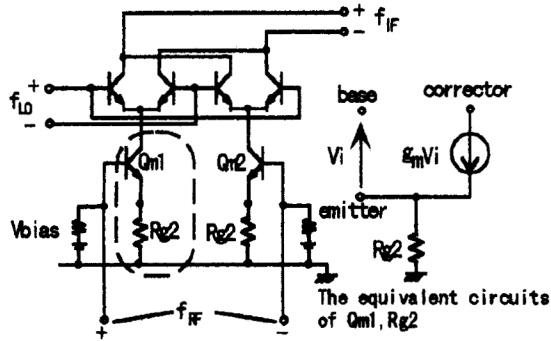


Figure 7. GSM 1stMIX
Emitter-decoupled circuit (MIX-D)

Figure 6 and 7 show 1st MIX circuit with the emitter-coupled circuit (MIX-C), the emitter-decoupled circuit (MIX-D) and corresponding equivalent circuits. An equivalent circuit of the input stage that is surrounded by a broken oval in each figure is drawn on the right side. G_m of each equivalent circuit in MIX-C and MIX-D are given by eq. (1) and eq. (2), respectively.

$$G_{m1} = 1/(1/g_m + R_{g1}/(1 + R_{g1}/(R_e/2))) \quad (1)$$

$$G_{m2} = 1/(1/g_m + R_{g2}) \quad (2)$$

For comparing two types of mixers with the same conversion gain and current level, the resistors are chosen as follows;

$$R_{g1} = 200\Omega, R_e = 400\Omega, R_{g2} = 100\Omega.$$

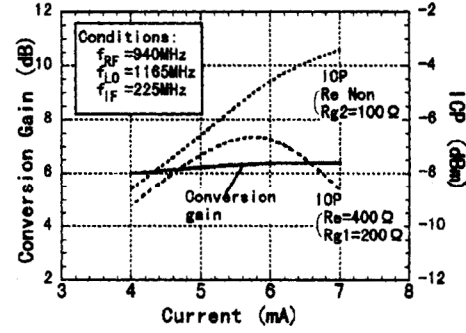


Figure 8. Simulated performance

The simulated comparison of two types of mixer on conversion gain and ICP with varying biasing current level is shown in figure 8. The frequency of RF input signal, RF local signal, IF output signal and supply voltage were 940MHz, 1165MHz, 225MHz and 2.7 V, respectively. Both mixers achieved the same conversion gain with the same current level. However, the emitter-decoupled mixer achieved higher ICP. At lower current level of 4-5.5 mA, the advantage was about 1dB. Over 5.5mA, the advantage becomes much more significant. For clarifying the difference of two types of mixer, transient waveforms at the emitter of Qm1 are compared as shown in figure 9.

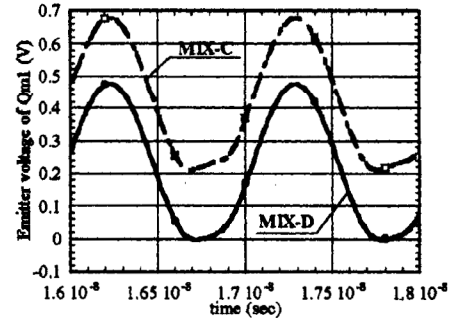


Figure 9. Waveform at the emitter of Qm1

Both input voltages at the base of Qm1 and Qm2 are 0.6 Vpp that is equivalent with -9dBm@50Ω input at 4mA biasing level. The waveform of MIX-C was clipped at the bottom of the waveform. When the emitter voltage of Qm1 is decreased, that of Qm2 is increased. If emitter-coupling resistor R_e exists, the current flows from Qm2 side to Qm1 side and push up the emitter voltage of Qm1. As the result, Qm1 is forced to enter cutoff state and the waveform is clipped as shown in figure 9. The emitter-decoupled circuit eliminates this effect. When the biasing current is increased, the headroom of Qm1 and Qm2 limits linearity. The emitter-biasing resistor R_{g2} of MIX-D is half of R_{g1} of MIX-C. Therefore, MIX-D has larger headroom than MIX-C, which makes a larger difference on ICP performance. In the small current level, the existence of the emitter-coupling resistor R_e is dominant for degradation of linearity, and in the large current level, the headroom of Qm1 and Qm2 is

dominant. The emitter-decoupled scheme has the advantage on linearity and headroom of the differential pair.

The disadvantage of the scheme is degradation of common-mode rejection ratio (CMRR). To find the impact of low CMRR, unbalanced input signal, which was generated by 20% deviation of off-chip matching circuit components, was applied to MIX-D. The gain and ICP degraded 0.8dB and 0.4dB. These results were acceptable for the mixer.

Measured results of the emitter-decoupled mixer are shown in figure 10. The conversion gain of 9.2dB and ICP of -4.5dBm were achieved with 8mA. The ICP was improved by 4dB as compared with our conventional type mixer.

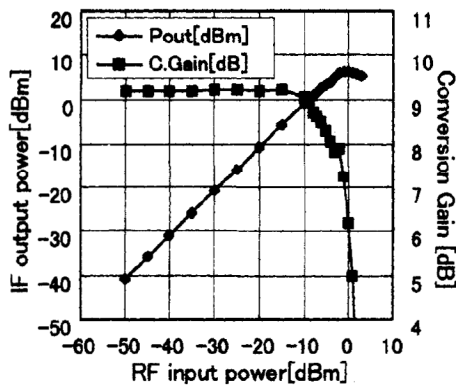


Figure 10. Mixer evaluation results

3. Overall experimental performance

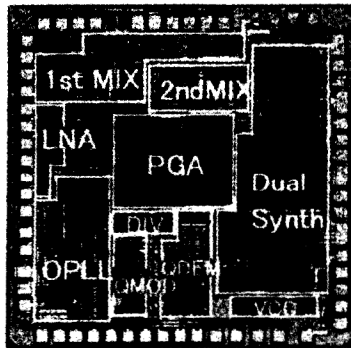


Figure 11. Chip photograph

A microphotograph of the IC is shown in figure 11. The IC fabricated in a 0.35μm SOI BiCMOS process occupies 2.9 mm² chip area. The chip is bonded in package QFP-56. The system performance has been tested including this IC. The required reference sensitivity of a receiver, which is defined by a residual bit error rate (RBER), should be less than 2% at -102dBm for both applications. The measured RBER is shown in figure 12. The reference sensitivities were -107.8 dBm for GSM and -108.3 dBm for DCS1800. Figure 13 shows the RBER against 3MHz blocker level for

GSM, which should be larger than -23dBm at RBER of 2%. The blocker level was -18dBm at RBER of 2%. High sensitivity and low distortion characteristics of the receiver were achieved. Table 1 summarizes the receiver characteristics of the IC.

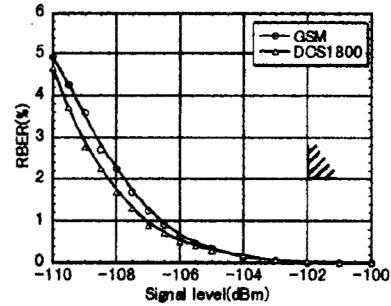


Figure 12. RBER of the receiver

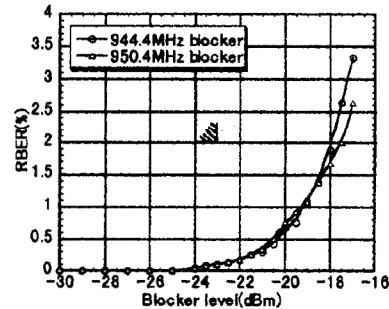


Figure 13. RBER against 3MHz blocker

Table 1. Receiver characteristics of the IC

elements	Evaluation items	GSM	DCS1800
Receiver tota	reference sensitivity	-107.8 dBm	-108.3 dBm
LNA	Gain	18.8 dB	13.5 dB
	NF	1.7 dB	1.8 dB
	ICP	-8.8 dBm	-8.8 dBm
1st MIX	Conversion gain	9.2 dB	10.8 dB
	NF	8.9 dB	8.7 dB
	ICP	-4.5 dBm	-3.8 dBm
2nd MIX	Conversion gain	12.3 dB	
	NF	6.8 dB	
PGA	Gain control range	93 dB	
	ICP(when Gain = -30dB)	-3.2 dBm	
QDEM	DC-offset	17 mV	

4. References

- [1] B. Razavi, "A 900MHz / 1.8GHz CMOS Transmitter for Dual Band Applications," 1998 Symposium on VLSI circuits, pp. 128-131, 1998
- [2] K.L.Fong "Dual-Band High-linearity Variable-Gain Low-Noise Amplifiers for Wireless Applications," 1999 IEEE Int. Solid-State Circuits Conf., pp. 224-225, 1999
- [3] T. Yamawaki, et. al. "A Dual-band Transceiver for GSM and DCS1800 applications" 24th European Solid-State Circuits Conf., pp. 84-87, 1998
- [4] A. Rofougaran et. al., "A 1GHz CMOS RF Front-end IC for a Direct-Conversion Wireless Receiver", IEEE J. of SC, Vol. 31No. 7, July 1996