AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the Eastern District of Texas, Marshall Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:24-cv-00140	2/28/2024	for the Eastern District of Texas, Marshall Division

PLAINTIFF	DEFENDANT
Harbor Island Dynamic, LLC	SamsungElectronics Co., Ltd. and Samsung Electronics America, Inc.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 9,245,826	1/26/2016	Harbor Island Dynamic, LLC
2 7,772,673	8/10/2010	Harbor Island Dynamic, LLC
3 9,147,609	9/29/2015	Harbor Island Dynamic, LLC
4 7,745,886	6/29/2010	Harbor Island Dynamic, LLC
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/286,472	09/29/2008	Robert L. Zwingman	TSJ-0150165

CONFIRMATION NO. 5453

POA ACCEPTANCE LETTER

22888
BEVER HOFFMAN & HARMS, LLP
39500 Stevenson Place
Suite 209
Fremont, CA 94539

OC000000097363539

Date Mailed: 02/13/2018

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/06/2018.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/agizaw/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/286,472	09/29/2008	Robert L. Zwingman	0150165

CONFIRMATION NO. 5453

POWER OF ATTORNEY NOTICE

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

OC000000097363513

Date Mailed: 02/13/2018

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/06/2018.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/agizaw/

PTO/AIA/80 (07-12)
Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office; U.S DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

[■] Practitioners associated with Customer Number: 22888

OR

[ ] Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

[■] The address associated with Customer Number: 22888

OR

[ ] Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address: Newport Fab LLC dba Jazz Semiconductor
4320 Jamboree Road
Newport Beach, CA 92660

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record
The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	Ronit Vardi	Date	May 9, 2016
Name	Ronit Vardi	Telephone	949 435 8827
Title	Chief Financial Officer		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Robert L. Zwingman, et al.

Application No./Patent No.: 7,745,886 Filed/Issue Date: June 20, 2010

Titled: SEMICONDUCTOR ON INSULATOR (SOI) SWITCHING CIRCUIT

Newport Fab LLC dba Jazz Semiconductor, a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. [X] The assignee of the entire right, title, and interest.

2. [ ] An assignee of less than the entire right, title, and interest (check applicable box):

[ ] The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

[ ] There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. [ ] The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. [ ] The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

A. [X] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 021681, Frame 0527, or for which a copy thereof is attached.

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/E. Eric Hoffman/	February 6, 2018
Signature	Date
E. ERIC HOFFMAN	38,186
Printed or Typed Name	Title or Registration Number

PTO/SB/123 (04-15)
Approved for use through 01/31/2018. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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CHANGE OF CORRESPONDENCE ADDRESS
Patent

Address to:
Mail Stop Post Issue
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Patent Number	7,745,886
Issue Date	06/29/2010
Application Number	12/286,472
Filing Date	09/29/2008
First Named Inventor	Robert L. Zwingman
Attorney Docket Number	TSJ-0150165

Please change the Correspondence Address for the above-identified patent to:

☒ The address associated with Customer Number: 22888

OR

☐ **Firm *or* Individual Name**

Address

City	**State**	**ZIP**

Country

Telephone	**Email**

This form cannot be used to change the data associated with a Customer Number. To change the data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB/124).

This form will not affect any "fee address" provided for the above-identified patent. To change a "fee address" use the "Fee Address Indication Form" (PTO/SB/47).

I am the:

☐ Patentee.

☐ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☒ Attorney or agent of record. Registration Number 38,186.

Signature	/E. Eric Hoffman/		
Typed or Printed Name	E. Eric Hoffman		
Date	February 6, 2018	Telephone	(925) 895-3545

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Post Issue, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/47 (03-09)
Approved for use through 05/31/2015. OMB 0651-0016
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
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"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

- OR -

Fax to:
571-273-6500

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below**: If you have a Customer Number to represent the fee address. **When to check the second box below**: If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☑ Customer Number: 22888

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
7,745,886	12/286,472

Completed by (check one):

☐ Applicant/Inventor

/E. Eric Hoffman/
Signature

☑ Attorney or Agent of record 38,186 (Reg. No.)

E. Eric Hoffman
Typed or printed name

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

(925) 895-3545
Requester's telephone number

☐ Assignee recorded at Reel _____ Frame_____

February 6, 2018
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

☑ *** Total of** 1 **forms are submitted.**

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	31720583
Application Number:	12286472
International Application Number:	
Confirmation Number:	5453
Title of Invention:	SEMICONDUCTOR ON INSULATOR (SOI) SWITCHING CIRCUIT
First Named Inventor/Applicant Name:	Robert L. Zwingman
Customer Number:	25700
Filer:	Edward Eric Hoffman/Carrie Reddick
Filer Authorized By:	Edward Eric Hoffman
Attorney Docket Number:	0150165
Receipt Date:	06-FEB-2018
Filing Date:	29-SEP-2008
Time Stamp:	20:38:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		TSJ-0150165-PTO-POA2-Filed.pdf	657955 f5414ba8ff267209fa68b6b229d13a5a49700054e	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Power of Attorney	1	1
	Assignee showing of ownership per 37 CFR 3.73	2	3
	Change of Address	4	4
	Maintenance Fee Address Change	5	5
Warnings:			
Information:			
	Total Files Size (in bytes):	657955	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/286,472	09/29/2008	Robert L. Zwingman	0150165

CONFIRMATION NO. 5453

MISCELLANEOUS NOTICE

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

OC000000086749906

Date Mailed: 10/27/2016

A communication which cannot be delivered in electronic form has been mailed to the applicant.

Doc Code: N572

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/286,472	09/29/2008	Robert L. Zwingman	0150165

CONFIRMATION NO. 5453

OC000000086749906

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

Cc:- BEVER HOFFMAN & HARMS, LLP
39500 STEVENSON PLACE
SUITE 209
FREMONT, CA 94539

Date Mailed:10/26/2016

DENIAL OF REQUEST FOR POWER OF ATTORNEY

The request for Power of Attorney 10/18/2016 is acknowledged. However, the request cannot be granted at this time for the reason stated below.

- ☐ The Power of Attorney you provided did not comply with the new Power of Attorney rules that became effective on June 25, 2004. See 37 CFR 1.32.
- ☐ The revocation is not signed by the applicant, the assignee of the entire interest, or one particular principal attorney having the authority to revoke.
- ☒ The Power of Attorney is from an assignee and the Certificate required by 37 CFR 3.73(c) has not been received.
- ☐ The person signing for the assignee has omitted their empowerment to sign on behalf of the assignee.
- ☐ The inventor(s) is without authority to appoint attorneys since the assignee has intervened as provided by 37 CFR 3.71.
- ☐ The signature(s) of _____co-inventor in this application, has been omitted. The Power of Attorney will be entered upon receipt of confirmation signed by said co-inventor(s).
- ☐ The person(s) appointed in the Power of Attorney is not registered to practice before the U.S. Patent and Trademark Office.

Doc Code: N572

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

- ☐ Only one Customer Number can be designated for the Power of Attorney in an application. The Customer Number that was captured is the first Customer Number provided on the Power of Attorney document.

- ☐ A request under 37 CFR 1.48 to add an inventor was granted in this application, however, no power of attorney consistent with the power of attorney granted by the originally named inventive entity has been received. Thus, the addition of the inventor has resulted in the loss of power of attorney in the application. See 37 CFR 1.32(e).

- ☐ The power of attorney has not been accepted because the party who is giving power of attorney has not been identified. Power of attorney may only be signed by the applicant for patent (37 CFR 1.42) or the patent owner. A patent owner who was not the applicant must appoint any power of attorney in compliance with 37 CFR 3.71 and 3.73. See 37 CFR 1.32(b)(4).

- ☐ The power of attorney from the inventors has not been accepted because it is a copy from a prior national application for which benefit is claimed and the continuing application names an inventor who was not named as an inventor in the prior application.

- ☐ The power of attorney from the inventors has not been accepted because the power of attorney must be signed by the applicant for patent. See 37 CFR 1.32(b)(4).

- ☐ Any request to correct or update the name of the applicant must include an application data sheet (ADS) in compliance with 37 CFR 1.76 specifying the correct or updated name of the applicant in the applicant information section. Any request to change the applicant after an original applicant has been specified under 37 CFR 1.46(b) must include a new ADS in compliance with 37 CFR 1.76 specifying the applicant in the applicant information section and comply with 37 CFR 3.71 and 3.73. See 37 CFR 1.46(c).

Any inquiries regarding this notice should be directed to the Application Assistance Unit at 571-272-4200.

Application Assistance Unit
571-272-4200

PTO/SB/47 (03-09)
Approved for use through 05/31/2015. OMB 0651-0016
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

- OR -

Fax to:
571-273-6500

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below**: If you have a Customer Number to represent the fee address. **When to check the second box below**: If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☑ Customer Number: 22888

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
7,745,886	12/286,472

Completed by (check one):

☐ Applicant/Inventor

/E. Eric Hoffman/
Signature

☑ Attorney or Agent of record 38,186
(Reg. No.)

E. Eric Hoffman
Typed or printed name

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

(925) 895-3545
Requester's telephone number

☐ Assignee recorded at Reel _____ Frame_____

October 18, 2016
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

☑ *** Total of** 1 **forms are submitted.**

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1. 11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313- 1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA.,
Document Description: Power of Attorney

PTO/SB/81 (07-13)
Approved for use through 11/30/2014. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

22898

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I are the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Newport Fab, LLC dba Jazz Semiconductor

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	2/17/15
Name	Ronit Vardi		
Title	Chief Financial Officer		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of ONE forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/123 (04-15)
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CHANGE OF CORRESPONDENCE ADDRESS
Patent

Address to:
Mail Stop Post Issue
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Patent Number	7,745,886
Issue Date	06/29/2010
Application Number	12/286,472
Filing Date	09/29/2008
First Named Inventor	Robert L. Zwingman
Attorney Docket Number	TSJ-0150165

Please change the Correspondence Address for the above-identified patent to:

☒ The address associated with Customer Number: 22888

OR

☐ **Firm *or* Individual Name**

Address

City | **State** | **ZIP**

Country

Telephone | **Email**

This form cannot be used to change the data associated with a Customer Number. To change the data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB/124).

This form will not affect any "fee address" provided for the above-identified patent. To change a "fee address" use the "Fee Address Indication Form" (PTO/SB/47).

I am the:

☐ Patentee.

☐ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☒ Attorney or agent of record. Registration Number 38,186.

Signature /E. Eric Hoffman/

Typed or Printed Name E. Eric Hoffman

Date October 18, 2016 | Telephone (925) 895-3545

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Post Issue, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	27253603
Application Number:	12286472
International Application Number:	
Confirmation Number:	5453
Title of Invention:	SEMICONDUCTOR ON INSULATOR (SOI) SWITCHING CIRCUIT
First Named Inventor/Applicant Name:	Robert L. Zwingman
Customer Number:	25700
Filer:	Edward Eric Hoffman/Carrie Reddick
Filer Authorized By:	Edward Eric Hoffman
Attorney Docket Number:	0150165
Receipt Date:	18-OCT-2016
Filing Date:	29-SEP-2008
Time Stamp:	18:39:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		TSJ-0150165-PTO-CHG-Adrs-POA-MF-CHG-Adrs-FILED.pdf	634056 f11ba3dab16f1ba1ed8884e29d2b8e2dca8a4e2c	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Maintenance Fee Address Change	1	1
	Power of Attorney	2	2
	Change of Address	3	3
Warnings:			
Information:			
	Total Files Size (in bytes):	634056	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/286,472	09/29/2008	Robert L. Zwingman	0150165

CONFIRMATION NO. 5453

MISCELLANEOUS NOTICE

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

OC000000085968130

Date Mailed: 09/23/2016

A communication which cannot be delivered in electronic form has been mailed to the applicant.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/286,472	09/29/2008	Robert L. Zwingman	0150165

CONFIRMATION NO. 5453

IMPROPER CPOA LETTER

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

OC000000085988949

Date Mailed: 09/23/2016

NOTICE REGARDING POWER OF ATTORNEY

This is in response to the power of attorney filed 09/14/2016. The power of attorney in this application is not accepted for the reason(s) listed below:

- The power of attorney is from an assignee and the statement required by 37 CFR 3.73(c) has not been received.

/dtvernon/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Doc Code: N572

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/286,472	09/29/2008	Robert L. Zwingman	0150165

CONFIRMATION NO. 5453

OC000000085968130

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

Cc BEVER HOFFMAN & HARMS, LLP
39500 STEVENSON PLACE
SUITE 209
FREMONT, CA 94539

Date: 09/22/2016

DENIAL OF REQUEST FOR POWER OF ATTORNEY

The request for Power of Attorney filed 09/14/2016 is acknowledged. However, the request cannot be granted at this time for the reason stated below.

- ☐ The Power of Attorney you provided did not comply with the new Power of Attorney rules that became effective on June 25, 2004. See 37 CFR 1.32.
- ☐ The revocation is not signed by the applicant, the assignee of the entire interest, or one particular principal attorney having the authority to revoke.
- ☑ The Power of Attorney is from an assignee and the Certificate required by 37 CFR 3.73(c) has not been received.
- ☐ The person signing for the assignee has omitted their empowerment to sign on behalf of the assignee.
- ☐ The inventor(s) is without authority to appoint attorneys since the assignee has intervened as provided by 37 CFR 3.71.
- ☐ The signature(s) of _____ a co-inventor in this application, has been omitted. The Power of Attorney will be entered upon receipt of confirmation signed by said co-inventor(s).
- ☐ The person(s) appointed in the Power of Attorney is not registered to practice before the U.S. Patent and Trademark Office.
- ☐ Only one Customer Number can be designated for the Power of Attorney in an application. The Customer Number that was captured is the first Customer Number provided on the Power of Attorney document.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
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- ☐ A request under 37 CFR 1.48 to add an inventor was granted in this application, however, no power of attorney consistent with the power of attorney granted by the originally named inventive entity has been received. Thus, the addition of the inventor has resulted in the loss of power of attorney in the application. See 37 CFR 1.32(e).

- ☐ The power of attorney has not been accepted because the party who is giving power of attorney has not been identified. Power of attorney may only be signed by the applicant for patent (37 CFR 1.42) or the patent owner. A patent owner who was not the applicant must appoint any power of attorney in compliance with 37 CFR 3.71 and 3.73. See 37 CFR 1.32(b)(4).

- ☐ The power of attorney from the inventors has not been accepted because it is a copy from a prior national application for which benefit is claimed and the continuing application names an inventor who was not named as an inventor in the prior application.

- ☐ The power of attorney from the inventors has not been accepted because the power of attorney must be signed by the applicant for patent. See 37 CFR 1.32(b)(4).

- ☐ Any request to correct or update the name of the applicant must include an application data sheet (ADS) in compliance with 37 CFR 1.76 specifying the correct or updated name of the applicant in the applicant information section. Any request to change the applicant after an original applicant has been specified under 37 CFR 1.46(b) must include a new ADS in compliance with 37 CFR 1.76 specifying the applicant in the applicant information section and comply with 37 CFR 3.71 and 3.73. See 37 CFR 1.46(c).

Any inquiries regarding this notice should be directed to the Application Assistance Unit at 571-272-4200.

Application Assistance Unit
571-272-4200

PTO/SB/123 (04-15)
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CHANGE OF CORRESPONDENCE ADDRESS
Patent

Address to:
Mail Stop Post Issue
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Patent Number	7,745,886
Issue Date	06/29/2010
Application Number	12/286,472
Filing Date	09/29/2008
First Named Inventor	Robert L. Zwingman
Attorney Docket Number	TSJ-0150165

Please change the Correspondence Address for the above-identified patent to:

☒ The address associated with Customer Number: 22888

OR

☐ **Firm *or* Individual Name**

Address

City | **State** | **ZIP**

Country

Telephone | **Email**

This form cannot be used to change the data associated with a Customer Number. To change the data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB/124).

This form will not affect any "fee address" provided for the above-identified patent. To change a "fee address" use the "Fee Address Indication Form" (PTO/SB/47).

I am the:

☐ Patentee.

☐ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☒ Attorney or agent of record. Registration Number 38,186.

Signature /E. Eric Hoffman/

Typed or Printed Name E. Eric Hoffman

Date September 14, 2016 | Telephone (925) 895-3545

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Post Issue, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/47 (03-09)
Approved for use through 05/31/2015. OMB 0651-0016
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
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"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

- OR -

Fax to:
571-273-6500

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below**: If you have a Customer Number to represent the fee address. **When to check the second box below**: If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☑ Customer Number: 22888

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
7,745,886	12/286,472

Completed by (check one):

☐ Applicant/Inventor

/E. Eric Hoffman/
Signature

☑ Attorney or Agent of record 38,186 (Reg. No.)

E. Eric Hoffman
Typed or printed name

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

(925) 895-3545
Requester's telephone number

☐ Assignee recorded at Reel _____ Frame_____

September 14, 2016
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

☐ *** Total of _____forms are submitted.**

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1. 11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313- 1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	26922452
Application Number:	12286472
International Application Number:	
Confirmation Number:	5453
Title of Invention:	SEMICONDUCTOR ON INSULATOR (SOI) SWITCHING CIRCUIT
First Named Inventor/Applicant Name:	Robert L. Zwingman
Customer Number:	25700
Filer:	Edward Eric Hoffman/Carrie Reddick
Filer Authorized By:	Edward Eric Hoffman
Attorney Docket Number:	0150165
Receipt Date:	14-SEP-2016
Filing Date:	29-SEP-2008
Time Stamp:	14:01:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		TSJ-0150165-PTO-CHG-Adrs-POA-MF-CHG-Adrs-FILED.pdf	555600 d5ae8f3cd259cd0abedd831015a126a1be716757	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Change of Address	1	1
	Power of Attorney	2	2
	Maintenance Fee Address Change	3	3
Warnings:			
Information:			
	Total Files Size (in bytes):	555600	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 22888

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Newport Fab, LLC

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Ronit Vardi	Date (Optional)	1/11/2016
Name	Ronit Vardi		
Title	Chief Financial Officer		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of ONE forms are submitted.

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If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/286,472	06/29/2010	7745886	0150165	5453

25700 7590 06/09/2010
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 87 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Robert L. Zwingman, Walnut, CA;
Marco Racanelli, Santa Ana, CA;

IR103 (Rev. 10/09)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25700 7590 02/24/2010

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

OPAP IAP5 MAY 17 2010 PATENT & TRADEMARK OFFICE

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Jembier Davalos (Depositor's name)
Jembier Davalos (Signature)
May 17, 2010 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/286,472	09/29/2008	Robert L. Zwingman	0150165	5453

TITLE OF INVENTION: SEMICONDUCTOR ON INSULATOR (SOI) SWITCHING CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	05/24/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
LEE, CALVIN	2892	257-401000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Farjami & Farjami LLP
2

05/18/2010 MBLANCO1 00000044 12286472
01 FC:1501 1510.00 OP
02 FC:1504 300.00 OP
03 FC:1801 6.00 OP

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE (CITY and STATE OR COUNTRY)

Newport Fab, LLC dba Jazz Semiconductor — Newport Beach, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☒ Advance Order - # of Copies 2

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)
☐ A check is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-0731 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date May 17, 2010

Typed or printed name Michael Farjami Registration No. 38,135

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PAGE 5/5 * RCVD AT 5/17/2010 7:52:38 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/31 * DNIS:2732885 * CSID:949 282 1002 * DURATION (mm-ss):01-56

FARJAMI & FARJAMI LLP

AN INTELLECTUAL PROPERTY LAW FIRM

www.farjami.com

26522 La Alameda Avenue, Suite 360
Mission Viejo, California 92691
tel: (949) 282-1000
fax: (949) 282-1002

FACSIMILE TRANSMISSION COVER SHEET

Date: May 17, 2010

To: United States Patent and Trademark Office
Examiner: Lee, Calvin; Art Unit: 2892

Fax: (571) 273-2885

Re: **Application Serial No.: 12/286,472**
Filing Date: 9/29/2008; First-Named Inventor: Zwingman
Attorney Docket No.: 0150165

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 5

Message:

Enclosed please find the Issue Fee, Publication Fee, and Fee for Two Copies of the Issued Patent.

Payment for Issue Fee, Publication Fee, and Fee for Two Copies of the Issued Patent in the Amount of $1,816.00 is hereby enclosed on Form PTO-2038.

Thank you.

The documents accompanying this facsimile contain PRIVILEGED AND CONFIDENTIAL information intended only for use of the individual or entity named above. If you are not the intended recipient, disclosure, copying, distribution or use of the contents of this facsimile information is prohibited. If you have received this facsimile in error, please immediately notify us by telephone and return the original facsimile to us at the above address via U.S. Postal Service. We will reimburse you for all expenses incurred.

OPAP IAP5 MAY 17 2010 PATENT & TRADEMARK OFFICE

Attorney Docket No.: 0150165

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): **Zwingman, et al.**	Group Art Unit: **2892**
Application Serial No.: **12/286,472**	Examiner: **Lee, Calvin**
Filed: **September 29, 2008**	Notice of Allowance: **February 24, 2010**
Title: **Semiconductor on Insulator (SOI) Switching Circuit**	

ISSUE FEE, PUBLICATION FEE, AND FEE FOR TWO COPIES OF THE ISSUED PATENT

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

Enclosed, please find the completed "Issue Fee Transmittal" form and a "Payment by Credit Card" form (PTO-2038) in the amount of $1,816.00 to cover the issue fee, publication fee, and fee for two (2) copies of the issued patent. The Director is hereby authorized to charge any deficiency, or credit any overpayment, to Deposit Account 50-0731. The drawings filed in the present application have been accepted as formal drawings by the Examiner.

PAGE 2/5 * RCVD AT 5/17/2010 7:52:38 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/31 * DNIS:2732885 * CSID:949 282 1002 * DURATION (mm-ss):01-56

Attorney Docket No.: 0150165

An early issuance of the present application is respectfully requested.

Respectfully Submitted;
FARJAMI & FARJAMI LLP

Dated: 5/17/10

Michael Farjami, Esq.
Reg. No. 38,135
FARJAMI & FARJAMI LLP
Attorneys for Applicant

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Tel: (949) 282-1000
Fax: (949) 282-1002

CERTIFICATE OF MAILING OR TRANSMISSION
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed: Mail Stop Issue Fee, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450, or being facsimile transmitted to the USPTO at (571) 273-2885, on the date indicated below.

Date: 5/17/2010

Jembier Davalos
Name of Person Mailing or Transmitting Paper and/or Fee

Jembier Davalos
Signature

PAGE 3/5 * RCVD AT 5/17/2010 7:52:38 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/31 * DNIS:2732885 * CSID:949 282 1002 * DURATION (mm-ss):01-56

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NOTICE OF ALLOWANCE AND FEE(S) DUE

25700 7590 02/24/2010

FARJAMI & FARJAMI LLP
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MISSION VIEJO, CA 92691

EXAMINER	
LEE, CALVIN	
ART UNIT	PAPER NUMBER
2892	

DATE MAILED: 02/24/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/286,472	09/29/2008	Robert L. Zwingman	0150165	5453

TITLE OF INVENTION: SEMICONDUCTOR ON INSULATOR (SOI) SWITCHING CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	05/24/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

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B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25700 7590 02/24/2010

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(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/286,472	09/29/2008	Robert L. Zwingman	0150165	5453

TITLE OF INVENTION: SEMICONDUCTOR ON INSULATOR (SOI) SWITCHING CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	05/24/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
LEE, CALVIN	2892	257-401000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____

2_____

3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

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❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/286,472	09/29/2008	Robert L. Zwingman	0150165	5453

25700 7590 02/24/2010

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER
LEE, CALVIN

ART UNIT	PAPER NUMBER
2892	

DATE MAILED: 02/24/2010

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 87 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 87 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	12/286,472	ZWINGMAN, et al	
	Examiner	Art Unit	
	Calvin Lee	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are *1-19*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Calvin Lee/
Primary Examiner
Art Unit: 2892

OFFICE ACTION

Allowable Subject Matter

1. Claims 1-19 are allowed. Following is the Examiner's statement reason for allowance:

The prior arts of record: *Kohno* (US 5,789,800) discloses a collector plug **21** contacting the surface of a buried oxide layer **20** [Fig. 7 and col. 10], and *Zheng et al* (US 6,867,477) discloses a trench **220** extending beyond a top surface of a buried oxide layer **214** [Fig. 3 and col. 5]. None of the cited arts anticipates or fairly suggests such limitation as: "one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit," of the pending claims in a manner which would warrant a rejection under 35 USC § 102 and/or 35 USC § 103. There was no other prior art that suggested modification or combination with the cited prior art so as to satisfy the combination of claims 1, 12 & 16 and their dependent claims.

2. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

3. Any inquiry concerning this communication from the Examiner should be directed to *Calvin Lee* at (571) 272-1896 on Mondays thru Thursdays 7AM-5PM (EST). If attempts to reach the examiner by telephone are unsuccessful, Art Unit 2818's Supervisory Patent Examiner *Thao Xuan Le* can be reached at (571) 272-1708. The central fax number for the organization is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system at http://pair-direct.uspto.gov Should you have questions on access to the PAIR system, contact the Electronic Business Center at (866) 217-9197.

/Calvin Lee/

Dated: February 22, 2010 Primary Examiner, Art Unit 2892

Notice of References Cited	Application/Control No. 12/286,472	Applicant(s)/Patent Under Reexamination ZWINGMAN, et al	
	Examiner Calvin Lee	Art Unit 2892	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,867,477	03-2005	Zheng et al.	257/557
*	B	US-5,789,800	08-1998	Kohno, Hiroshi	257/588
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12286472	ZWINGMAN, ET AL.
	Examiner	**Art Unit**
	Calvin Lee	2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/22/2010								
	1	=								
	2	=								
	3	=								
	4	=								
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	17	=								
	18	=								
	19	=								

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12286472	ZWINGMAN, ET AL.
	Examiner	**Art Unit**
	Calvin Lee	2892

ORIGINAL		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
257	401	H	0	1	L	31 / 113 (2006.01.01)						
CROSS REFERENCE(S)		H	0	1	L	21 / 336 (2006.01.01)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											
438	284											

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 19	
/Calvin Lee/ Primary Examiner.Art Unit 2892 (Primary Examiner)	Feb 22-"10 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3, 4, & 5

U.S. Patent and Trademark Office

Part of Paper No. 2

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	12/286,472	ZWINGMAN, et al	
	Examiner	Art Unit	
	Calvin Lee	2892	0150165

SEARCHED			
Class	Subclass	Date	Examiner
257	393-401 501-504	02/20/2010	CL
438	279-286	#	#
257E29.	.32	#	#

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
257	**401**	**02/22/2010**	**CL**
438	284	#	#

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
Keyword Search EAST and cls/scl 257/401 & 438/284	02/22/2010	CL

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BIB DATA SHEET

CONFIRMATION NO. 5453

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/286,472	09/29/2008 **RULE**	438	2892	0150165

APPLICANTS
Robert L. Zwingman, Walnut, CA;
Marco Racanelli, Santa Ana, CA;

** **CONTINUING DATA** ************************** CL
This appln claims benefit of 61/007,035 12/10/2007

** **FOREIGN APPLICATIONS** ************************* NONE

** **IF REQUIRED, FOREIGN FILING LICENSE GRANTED** **
10/21/2008

		STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed ❑ Yes ☑ No 35 USC 119(a-d) conditions met ❑ Yes ☑ No Verified and Acknowledged /CALVIN LEE/ Examiner's Signature	❑ Met after Allowance CL Initials	CA	7	19	3

ADDRESS

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691
UNITED STATES

TITLE

Semiconductor on insulator (SOI) switching circuit

FILING FEE RECEIVED 1030	FEES: Authority has been given in Paper No.____________ to charge/credit DEPOSIT ACCOUNT No.____________ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other ________________ ❑ Credit

BIB (Rev. 05/07).

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/286,472	09/29/2008	Robert L. Zwingman	0150165

CONFIRMATION NO. 5453

PUBLICATION NOTICE

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

OC000000036421055

Title: Semiconductor on insulator (SOI) switching circuit

Publication No.US-2009-0149213-A1
Publication Date:06/11/2009

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The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/286,472	09/29/2008	2812	1030	0150165	19	3

CONFIRMATION NO. 5453

FILING RECEIPT

25700
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26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

OC000000032719577

Date Mailed: 10/27/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Robert L. Zwingman, Walnut, CA;
Marco Racanelli, Santa Ana, CA;

Assignment For Published Patent Application

NEWPORT FAB, LLC DBA JAZZ SEMICONDUCTOR, Newport Beach, CA

Power of Attorney:
Michael Farjami--38135
Farshad Farjami--41014

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/007,035 12/10/2007

Foreign Applications

If Required, Foreign Filing License Granted: 10/21/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/286,472**

Projected Publication Date: 06/11/2009

Non-Publication Request: No

Early Publication Request: No

Title

Semiconductor on insulator (SOI) switching circuit

Preliminary Class

438

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/286,472	09/29/2008	Robert L. Zwingman	0150165

CONFIRMATION NO. 5453

25700
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NOTICE

OC000000032719578

Date Mailed: 10/27/2008

NOTICE OF INFORMAL APPLICATION

This application is considered to be informal since it does not comply with the regulations for the reason(s) indicated below. The period within to correct the informalities noted below and avoid abandonment is set in the accompanying Office action.

Items Required To Avoid Processing Delays:

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

A new oath or declaration, identifying this application number, or, if appropriate, an application data sheet (37 CFR 1.76), is required. The oath or declaration does not comply with 37 CFR 1.63 in that it:

- does not identify the complete mailing or post office address of each inventor.

14230 U.S. PTO

092908

Attorney Docket No.: 0150165

U.S. PTO
12/286472
09/29/2008

PATENT APPLICATION COVER SHEET

MAIL STOP PATENT APPLICATION
COMMISSIONER FOR PATENTS
P.O. BOX 1450; ALEXANDRIA, VA 22313-1450

CUSTOMER NUMBER
25700
PATENT TRADEMARK OFFICE

Transmitted herewith is the patent application of:

ASSIGNEE: NEWPORT FAB, LLC DBA JAZZ SEMICONDUCTOR (NEWPORT BEACH, CA)

Inventor(s): Robert L. Zwingman and Marco Racanelli

For: "Semiconductor on Insulator (SOI) Switching Circuit"

This application is a ☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____.

Enclosed are:

☒ Seven (7) Sheets of drawings

☐ Request for Non-Publication (Form PTO/SB/35 (11-00))

☒ Separate Payment Form PTO-2038 for $40.00 is Attached for Assignment of the invention to: **Newport Fab, LLC dba Jazz Semiconductor**

☐ The enclosed payment includes $____for the recording of the assignment

☐ Applicant(s) claim(s) small entity status

☐ Information Disclosure Statement

☐ Preliminary Amendment

☒ Declaration and Power of Attorney

☒ The filing fee has been calculated as shown below:

	(Col. 1)	(Col. 2)	SMALL ENTITY		OTHER THAN A SMALL ENTITY	
FOR:	No. Filed	No. Extra	RATE	FEE	RATE	FEE
BASIC FEE				$155.00		$310.00
SEARCH FEE				$255.00		$510.00
EXAMINATION FEE				$105.00		$210.00
APPLICATION SIZE FEE (Total Number of Sheets)	(33 -100)/50=	0	x $130.00=	$	x $260.00=	$
TOTAL CLAIMS	19 -20 =	0	x $25.00=	$	x $50.00=	$
INDEPENDENT CLAIMS	3 -3 =	0	x $105.00=	$	x $210.00 =	$
MULTIPLE DEPENDENT CLAIMS PRESENTED			+$185.00=	$	+$370.00 =	$
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07JAZ0005J-2

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MICHAEL FARJAMI, ESQ.

Date: 9/29/08

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14230 U.S. PTO

092908

Attorney Docket No.: 0150165

PATENT APPLICATION COVER SHEET

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COMMISSIONER FOR PATENTS
P.O. BOX 1450; ALEXANDRIA, VA 22313-1450

CUSTOMER NUMBER
25700
PATENT TRADEMARK OFFICE

Transmitted herewith is the patent application of:

ASSIGNEE: NEWPORT FAB, LLC DBA JAZZ SEMICONDUCTOR (NEWPORT BEACH, CA)

Inventor(s): Robert L. Zwingman and Marco Racanelli

For: "Semiconductor on Insulator (SOI) Switching Circuit"

This application is a ☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____.

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☐ Applicant(s) claim(s) small entity status

☐ Information Disclosure Statement

☐ Preliminary Amendment

☒ Declaration and Power of Attorney

☒ The filing fee has been calculated as shown below:

	(Col. 1)	(Col. 2)	SMALL ENTITY		OTHER THAN A SMALL ENTITY	
FOR:	No. Filed	No. Extra	RATE	FEE	RATE	FEE
BASIC FEE				$155.00		$310.00
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INDEPENDENT CLAIMS	3 -3 =	0	x $105.00=	$	x $210.00 =	$
MULTIPLE DEPENDENT CLAIMS PRESENTED			+$185.00=	$	+$370.00 =	$
If the difference in Col. 1 is less than zero, enter "0" in Col. 2			TOTAL	$	TOTAL	$1,030.00

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(949) 282-1000

Attorney Docket No.: 0150165

UNITED STATES PATENT APPLICATION

FOR

SEMICONDUCTOR ON INSULATOR (SOI) SWITCHING CIRCUIT

INVENTORS:

ROBERT L. ZWINGMAN
MARCO RACANELLI

CUSTOMER NUMBER

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Christina Carter Ellis — Christina Carter Ellis

Name — Signature

PREPARED BY:

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Customer No.: 25700

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BACKGROUND OF THE INVENTION

The present application claims the benefit of and priority to a pending provisional patent application entitled "Semiconductor on Insulator (SOI) Structure, Method for Fabrication, and Circuits Using Same," Serial Number 61/007,035 filed on December 10, 2007. The disclosure in that pending provisional application is hereby incorporated fully by reference into the present application.

1. FIELD OF THE INVENTION

The present invention is generally in the field of fabrication of semiconductor structures and circuits. More particularly, the invention is in the field of fabrication of semiconductor on insulator (SOI) structures and circuits.

2. BACKGROUND ART

Semiconductor structures such as transistors and isolating trenches are conventionally fabricated on several types of silicon wafers. For example, such structures can be fabricated on bulk silicon wafers or silicon on insulator wafers. Bulk silicon wafers typically have a substantially uniform composition, while semiconductor on insulator wafers typically have a layered composition. Once fabricated on a particular silicon wafer, such semiconductor structures are typically used in a wide variety of circuits, including switching circuits.

Each type of silicon wafer utilized for fabricating such semiconductor structures suffers from attendant drawbacks. For example, it is difficult to electrically isolate semiconductor structures fabricated on a conventional bulk silicon wafer, because

although such semiconductor structures can be partially electrically isolated by virtue of, for example, their isolating trenches, electric current can still flow under such trenches, leading to, for example, voltage and current fluctuations. Neighboring semiconductor devices, e.g. neighboring cascaded transistors, in such structures thus tend to interfere with one another when fabricated on bulk silicon wafers. In contrast, it is easier to electrically isolate semiconductor structures or circuits implemented on a conventional silicon on insulator wafer, in which a buried oxide layer provides additional isolation. Unfortunately, circuits designed for fabrication in a bulk silicon wafer must be redesigned for fabrication in a conventional silicon on insulator wafer, which significantly increases manufacturing and integration complexity and cost.

Thus, there is a need in the art for semiconductor structures and circuits that overcome disadvantages associated with utilizing conventional bulk silicon and silicon on insulator wafers.

SUMMARY OF THE INVENTION

A semiconductor on insulator (SOI) switching circuit, substantially as shown in and/or described in connection with at least one of the figures, and as set forth more completely in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows an example of a conventional semiconductor on insulator (SOI) structure.

Figure 2 shows an exemplary SOI structure according to one embodiment of the present invention.

Figure 3 shows an exemplary SOI structure according to one embodiment of the present invention.

Figure 4 shows an exemplary SOI switching circuit according to one embodiment of the present invention.

Figure 5 shows an exemplary wireless communications device according to one embodiment of the present invention.

Figure 6 shows an exemplary front end circuit according to one embodiment of the present invention.

Figure 7 shows an exemplary front end circuit according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is directed to a semiconductor on insulator (SOI) switching circuit. Although the invention is described with respect to specific embodiments, the principles of the invention, as defined by the claims appended herein, can obviously be applied beyond the specific embodiments of the invention described herein. Moreover, in the description of the present invention, certain details have been left out in order to not obscure the inventive aspects of the invention. The details left out are within the knowledge of a person of ordinary skill in the art.

The drawings in the present application and their accompanying detailed description are directed to merely exemplary embodiments of the invention. To maintain brevity, other embodiments of the invention which use the principles of the present invention are not specifically described in the present application and are not specifically illustrated by the present drawings.

In Figure 1, a conventional semiconductor on insulator ("SOI") wafer cross section is shown as structure 100. Structure 100 comprises exemplary device layer 102, buried oxide layer 104, and bulk semiconductor layer 106. Device layer 102 comprises a semiconductor such as, for example, silicon, and has thickness 142, which might be about 800 Angstroms in one embodiment. Buried oxide layer 104, which is situated below device layer 102, is an insulator such as, for example, silicon oxide, and has thickness 144, which might be about 1200 Angstroms in one embodiment. Bulk semiconductor layer 106, which is situated below buried oxide layer 104, has, in one embodiment, a

typical resistivity of about 3 to 20 ohms-centimeter, and thickness 146 which might be about 725 microns, and forms the bottom of structure 100.

Device layer 102, buried oxide layer 104, and bulk semiconductor layer 106 of structure 100 can be produced by several methods as known in the art. For example, one method involves growing oxide layers on two silicon wafers, placing the oxide layers in contact with each other, annealing the oxide layers together, and grinding the reverse side of one of the silicon wafers to produce a SOI wafer having a device layer of the desired thickness. Another exemplary method utilizing two silicon wafers involves growing an oxide on one silicon wafer (typically 80% of the resulting buried oxide layer), growing an oxide on the other silicon wafer (typically 20% of the resulting buried oxide layer), implanting hydrogen, placing the two silicon wafers together, and thermally shocking the resulting assembly. The shock cracks one of the silicon wafers, producing a new top surface (e.g., top surface 102a of structure 100) resulting in a SOI wafer of the desired thickness.

Structure 100 also comprises trench 108 and trench 110. To form trenches 108 and 110, the material of device layer 102 situated where trenches 108 and 110 will be formed is removed, e.g. etched away, and LOCOS or STI oxidation processes, for example, are used to fill both trenches with an insulative oxide. Trenches 108 and 110 typically extend through device layer 102 and contact the top surface of buried oxide layer 104, as shown in Figure 1. In the region, or island, of device layer 102 between trenches 108 and 110 transistor 112 can be fabricated. Transistor 112 (an example of a "semiconductor device" in the present application), is electrically isolated from

neighboring islands 120 and 122 by trenches 108 and 110, respectively, and buried oxide layer 104. This isolation is one conventional advantage of building semiconductor structures, such as transistor 112, on a SOI wafer, because the isolation allows such semiconductor structures to experience positive and negative voltage excursions without affecting neighboring devices and without shorting to ground.

Transistor 112 of structure 100 could be, for example, an NFET or a PFET transistor, and comprises source 114, gate 116, and drain 118. Source 114 and drain 118 typically extend all the way through device layer 102 and contact the top surface of buried oxide layer 104. Because there is thus no, or almost no, semiconductor material, e.g. silicon, between source 114 or drain 118 and the top surface of buried oxide layer 104, there is no, or almost no, semiconductor junction to create a capacitive load. Such low capacitance allows for, for example, higher speed operation or lower power consumption. However, such low or non-existent junction capacitance also prevents the utilization of well understood bulk silicon wafer design methodology, device models, and well developed design kits that take into account existence of certain amount of junction capacitance based on, for example, transistor sizes, device geometries and other factors. In other words, conventional SOI structure 100 must be designed and fabricated using only new, less developed, and less prevalent design methodologies, device models and design kits that are not as well developed, tested or understood, and which also introduce additional development costs and inefficiencies in the design and fabrication of SOI devices using conventional SOI structure 100 in Figure 1.

Conventional structure 100 thus illustrates several advantages and disadvantages of utilizing a conventional SOI wafer instead of a conventional bulk silicon wafer when fabricating certain semiconductor structures, such as transistor 112 and trenches 108 and 110. Building trenches similar to trenches 108 and 110 in a conventional bulk silicon wafer, instead of a conventional SOI wafer as shown in Figure 1, would not produce effective isolation because semiconductor devices, such as transistor 112, could short out to other devices or electrically communicate under the trenches. However, as discussed above, utilizing a conventional SOI wafer imposes significant design challenges and costs.

Figure 2 shows a semiconductor on insulator ("SOI") wafer cross section, according to one embodiment of the present invention, as structure 200. Structure 200 shares certain features with structure 100, and comprises device layer 202, buried oxide layer 204, and bulk semiconductor layer 206. In this embodiment, and by way of examples only, device layer 202 has a thickness 242 of about 1.4 microns. Buried oxide layer 204 is situated below device layer 202, is an insulator such as, for example, silicon oxide, and has a thickness 244 of, for example, about 1 micron. Bulk semiconductor layer 206 is situated below buried oxide layer 204, has a thickness 246 of, for example, about 725 microns, has a resistivity of, for example, about 1000 ohms-centimeter, and forms the bottom of structure 200. Thus, in this embodiment, while the invention's bulk semiconductor layer 206 may have a thickness similar, for example, to conventional bulk semiconductor layer 106, the invention's buried oxide layer 204 and device layer 202 are significantly thicker than respective conventional buried oxide layer 104 and device layer

102. Additionally, the invention's bulk semiconductor layer 206 has a significantly greater resistivity than conventional bulk semiconductor layer 106.

Structure 200 comprises semiconductor devices, such as for example transistor 212, which in one embodiment could be, for example, an NFET or a PFET transistor. Continuing with this example, transistor 212 comprises source 214, gate 216, and drain 218. Because of the increased thickness of device layer 202, source 214 and drain 218 do not extend all the way through device layer 202 to contact the top surface of buried oxide layer 204. Instead, a layer with intervening thickness 248 remains between the bottom surfaces of source 214 and drain 218 and the top surface of buried oxide layer 204. Consequently, a semiconductor junction is formed by source 214 and drain 218 within device layer 202. Each such semiconductor junction will have an associated junction capacitance, e.g. the source/drain junctions of transistor 212 have corresponding source/drain junction capacitances.

The source/drain junction capacitances of transistor 212 behave similarly to the junction capacitances of a transistor implemented in a conventional bulk silicon wafer, instead of a conventional SOI wafer, in part because of the greater thickness of device layer 202 compared to the thickness of conventional device layer 102. The better understood and more predictable junction capacitances in structure 200 result in more predictable behavior of transistor 212 such that, for example, computer simulation programs and bulk silicon wafer design kits that are well understood and widely used for conventional bulk silicon fabrication can be utilized to design and implement transistor 212 in the invention's SOI wafer. Significantly, the behavior of transistor 212 is better

understood and more predictable than the behavior of transistor 112 in Figure 1 which, for example, practically lacks any source or drain junction capacitance because source 114 and drain 118 of transistor 112 extend all the way to the top surface of buried oxide layer 104.

Transistor 212 is electrically isolated from neighboring islands 220 and 222 by adjacent trenches 208 and 210, respectively, and by buried oxide layer 204. In order to achieve this isolation, in one embodiment of the invention trenches 208 and 210 are etched to extend all the way, or almost all the way, through device layer 202 and contact, or almost contact, the top surface of buried oxide layer 204. According to the present invention, a novel process is used to form trenches 208 and 210 after the fabrication of transistor 212, instead of forming the trenches prior to fabrication of transistor 212, as is the case in the fabrication of conventional structure 100. More specifically, to fabricate structure 100, trenches 108 and 110 are etched early in the fabrication process, a thin layer of oxide is grown in each trench, the trenches are coated and lined with more oxide, and then the trenches are filled with polysilicon, as known in the art. In contrast, trenches 208 and 210 are etched during a "backend" process after fabrication of transistor 212 and are filled with a dielectric, which in one embodiment is silicon oxide, and/or some additive, instead of polysilicon.

According to one embodiment of the invention, islands 220 and 222 may have well 224 and well 226, respectively, which cannot be formed in the process used to create SOI structure 100. Wells 224 and 226 may or may not extend all the way through device layer 202, and may or may not contact the top of buried oxide layer 204. The wells, if

they exist, can be P-wells or N-wells, depending on the type of semiconductor devices to be placed in island 220 and island 222, if any.

Figure 3 shows a semiconductor on insulator ("SOI") wafer cross section, according to one embodiment of the present invention, as structure 300. Structure 300 comprises device layer 302, buried oxide layer 304, and bulk semiconductor layer 306, which correspond to device layer 202, buried oxide layer 204, and bulk semiconductor layer 206 of structure 200. Structure 300 also comprises trench 308, trench 309, and trench 310, which correspond to trenches 208 and 210 in structure 200. Additionally, structure 300 comprises transistor 312 and transistor 322, each of which is a semiconductor device corresponding to transistor 212 in structure 200. In one embodiment of the invention, transistors 312 and 322 can exist in neighboring islands 330 and 340 in device layer 302, separated by trench 309 and isolated from other semiconductor devices by trenches 308 and 310 and by buried oxide layer 304.

Figure 3 illustrates how the combination of the isolation provided by buried oxide layer 304 and by trenches 308, 309, and 310, the greater thickness of device layer 302, and the high resistivity of bulk silicon layer 306 allows for the enhancement and advantages in the design of transistors or other semiconductor devices. Notably, in this configuration transistors 312 and 322 can be "stacked" together, i.e. closely spaced, while remaining electrically isolated to make advantageous circuits, such as various high voltage switching circuits, an embodiment of which is described below.

It is noted that in the configuration of structure 300 in Figure 3, transistors 312 and 322 each consists of two gates (which might be implemented as a gate with two

"fingers," "branches," i.e. as a "partitioned gate"). For example, transistor 312 consists of two gates 316 and 317 (or a gate with two fingers or two branches 316 and 317) that are shorted to each other by a metal interconnect or other interconnect, not shown in any of the Figures. Similarly, transistor 322 consists of two gates 326 and 327 (or a gate with two fingers or two branches 326 and 327) that are shorted to each other by a metal interconnect or other interconnect, not shown in any of the Figures. In some embodiments of the present invention, each transistor may consist of many more gates shorted to each other to represent a single electrical gate.

Each transistor may also consist of one or more drains (or one or more sources), interconnected to result in a single drain (or a single source). For example, transistor 312 is shown as having sources 314 and 315, which are shorted by a low resistivity interconnect not shown. Drain 318 is common between the shorted gates 316, 317, and the shorted sources 314 and 315 of transistor 312. However, in some embodiments more than one drain can be used (i.e. a drain with branches and fingers that are shorted to represent a single electrical drain). Similarly, transistor 322 is shown as having sources 324 and 325, which are shorted by a low resistivity interconnect not shown. Drain 328 is common between the shorted gates 326, 327, and the shorted sources 324 and 325 of transistor 322. However, in some embodiments more than one drain can be used (i.e. a drain with branches and fingers that are shorted to represent a single electrical drain). Various embodiments of the invention's transistors can be used in high voltage circuits, such as high voltage switching circuits, an embodiment of which is described below.

Because of the significantly greater thickness of device layer 302, semiconductor material, e.g. silicon, remains between the bottom surfaces of the sources and drains of transistors 312 and 322 and the top surface of buried oxide layer 304 (such remaining semiconductor corresponds to the semiconductor remaining in thickness 248 in structure 200) in islands 330 and 340. This remaining semiconductor would result in source/drain junction capacitance, similar to the junction capacitance of structure 200 as discussed above.

It should be noted that the effect of the resulting capacitive load from source/drain junction capacitances in structure 200 or structure 300 is advantageously reduced by taking advantage of the thick buried oxide layer 204 or 304 and the high resistivity of bulk silicon layer 206 or 306. For example, the greater thickness of buried oxide layer 304 can reduce the effect of junction capacitances in transistors 312 and 322, and the higher resistivity of bulk semiconductor layer 306 can further reduce such capacitances by facilitating the formation of thick depletion regions 350 and 352, thereby reducing the effect of source/drain junction capacitances loading transistors 312 and 322. Moreover, preserving the advantages of SOI structures, during operation of transistors 312 and 322, islands 330 and 340 can withstand large positive and negative voltage excursions because of the electrical isolation provided by adjacent trenches 308, 309, and 310, and buried oxide layer 304.

Depth 354 of depletion regions 350 and 352 (not drawn to scale), extending from the bottom surface of buried oxide layer 304, might be in one embodiment about 20 microns into bulk semiconductor layer 306, and is much greater than the depth of a

corresponding depletion region in conventional bulk semiconductor layer 106 in Figure 1, which may be, for example, as little as 2 microns or even a tenth of a micron, because conventional structure 100 has a much lower resistivity bulk semiconductor.

Some further advantages of using the invention's SOI structures, such as transistors 312 and 322, are for example, improved noise isolation and lower power consumption. Also, insertion loss can be reduced, and the "ON" resistance of transistors 312 and 322 is reduced, and in this way intended signals can pass through transistors 312 and 322 and/or can be amplified without being subjected to too much noise and without losing signal strength, thus maintaining a high signal to noise ratio. Moreover, because the entire islands 330 and 340 can experience voltage excursions, the reduced capacitance between islands 330 and 340 and bulk semiconductor layer 306 also reduces the time constant required to charge islands 330 and 340. According to these and other various advantages of the invention, transistors 312, 322, and additional transistors according to various embodiments can be used to design advantageous high voltage circuits, such as high voltage switching circuits, that exhibit reduced voltage and current fluctuations in device layer 302.

Figure 4 shows exemplary switching circuit 410, according to one embodiment of the present invention. Switching circuit 410 comprises a plurality of cascaded transistors 411, 412, 413, 414, 415, and 416 ("transistors 411 through 416"), and resistors 431, 432, 433, 434, 435, and 436 ("resistors 431 through 436"). Transistors 411 through 416 are fabricated in islands 421, 422, 423, 424, 425, and 426 ("islands 421 through 426") respectively, and coupled in series, or cascaded, as shown in Figure 4. Transistors 411

through 416 are fabricated according to one embodiment of the present invention. For example, each transistor might have a structure corresponding to exemplary transistor 312 in Figure 3 or to exemplary transistor 212 in Figure 2. While in the present embodiment of switching circuit 410, transistors 411 through 416 are NFET transistors, in another embodiment transistors 411 through 416 might be PFET transistors. In one embodiment, each island 421 through 426 might have a structure corresponding to exemplary island 330 in Figure 3. While Figure 3 depicts exemplary island 330 in cross-section, islands 421 through 426 in Figure 4 are shown conceptually and comprise regions in a device layer surrounded by isolating trenches extending down to a buried oxide layer, as previously shown and described in relation to exemplary island 330 in Figure 3. The unique fabrication of the previously described embodiment of the invention's exemplary transistor 312 (or transistor 212) results in advantageous operation of high voltage circuits such as switching circuit 410. For example, various advantages of SOI structures are maintained, while circuit design is greatly simplified and enhanced.

In one embodiment of the present invention, one transistor is situated in each island, e.g. transistor 411 is fabricated in island 421, but in another embodiment more than one transistor can be situated in an island and/or wired in parallel, for greater total current carrying capacity of switching circuit 410. In other embodiments, switching circuit 410 may comprise fewer than six islands (e.g. one island) or greater than six. With six islands and six cascaded transistors, as shown in Figure 4, signals as high as 30 volts can be controlled and applied between nodes 4A and 4B, while each transistor 411 through 416 experiences only about five volts of potential across its drain and source

terminals within each respective island 421 through 426. Nodes 4A, 4B, and 4C can be coupled to, for example, an input, an output, and a switch control signal, respectively; the latter driving the gates of transistors 411 through 416 via resistors 431 through 436. Figures 5, 6, and 7 show an exemplary wireless communications device and "front end circuits" comprising a high voltage switching circuit such as switching circuit 410, as discussed further below.

Figure 5 shows an exemplary wireless communications device 502, which can utilize circuits fabricated according to the present invention, such as switching circuit 410. Wireless communications device 502 can be, for example, a cellular telephone, a wireless personal computer, a wireless audio or video player, a wireless personal assistance device, or any other device configured for wireless communication. Exemplary wireless communications device 502 comprises display screen 504 and keypad 506, which in one embodiment may be an LCD screen and an alphanumeric keypad, for example. Wireless communications device 502 additionally comprises "front end circuit" (also referred to as "front end module") 512 coupled to antenna 508. While antenna 508 is depicted as an external antenna of wireless communications device 502, in one embodiment antenna 508 is an internal, i.e. integrated, antenna. Antenna 508 and front end circuit 512 may correspond to antenna 608 and front end circuit 612, shown in Figure 6, or to antenna 708 and front end circuit 712, shown in Figure 7.

As stated above, in one embodiment of wireless communications device 502, antenna 508 and front end circuit 512 correspond to antenna 608 and front end circuit 612, shown in Figure 6. Front end circuit 612 comprises switching circuit 610 and low

noise amplifier 614. Switching circuit 610 corresponds to switching circuit 410 in Figure 4, i.e. it comprises a number of cascaded transistors and respective resistors coupled to nodes 6A, 6B, and 6C corresponding to nodes 4A, 4B, and 4C. Switching circuit 610 is coupled via node 6A to antenna 608, via node 6B to the input of low noise amplifier 614, and via node 6C to a switch control signal. Switching circuit 610 can be utilized, for example, to couple low noise amplifier 614 to antenna 608, under control of a switch control signal applied to node 6C, and to shield low noise amplifier 614 from high voltages experienced by antenna 608.

In another embodiment of wireless communications device 502, antenna 508 and front end circuit 512 correspond to antenna 708 and front end circuit 712, shown in Figure 7. Front end circuit 712 comprises switching circuit 710 and power amplifier 716. In a manner similar to switching circuit 610, switching circuit 710 also corresponds to switching circuit 410 in Figure 4, i.e. it can comprise a number of cascaded transistors and respective resistors coupled to nodes 7A, 7B, and 7C corresponding to nodes 4A, 4B, and 4C. Switching circuit 710 is coupled via node 7A to antenna 708, via node 7B to the output of power amplifier 716, and via node 7C to a switch control signal. Thus configured, the output of power amplifier 716 can switchably drive antenna 708 to transmit desired wireless signals, under control of a switch control signal coupled to node 7C. Node 7A could thus oscillate, for example, at 900 MHz, or 1.8 GHz, or other desired frequencies, especially at frequencies that are considered high frequencies suitable for wireless communications.

Switching circuit 410 can thus be utilized in front end circuit 512 of wireless communications device 502, configured in a manner corresponding to front end circuits 612 or 712. Notably, in one embodiment of the invention, wireless communications device 502 can comprise two front end circuits, configured respectively like front end circuits 612 and 712, coupled to a single antenna and individually controllable by respective switch control signals. Figures 5, 6, and 7 demonstrate merely examples of how an embodiment of the present invention's transistors and structures can be used in high voltage circuits, for example in switching circuit 410 in Figure 4, and employed in actual devices.

The invention's advantages of, for example, a high resistivity bulk semiconductor layer, and thick device and buried oxide layers, each aid in implementing high performance circuits, such as switching circuit 410. An engineer using design methodologies suitable for conventional bulk semiconductor devices and circuits, without using specialized design techniques or device models required for conventional SOI technology, can readily design and implement high performance circuits utilizing various embodiments of the invention's SOI transistors and other SOI structures. One reason is that the invention's thick device layer semiconductor behaves substantially like a conventional bulk semiconductor, and conventional device models and computer simulation applications can be employed to design advantageous circuits utilizing the invention's SOI structures.

In addition to enabling use of bulk semiconductor device models and design methodologies, another advantage of the thick device layer in the invention's SOI

structures is that the invention's wafer fabrication processes can be run and implemented in a bulk semiconductor factory, i.e. at the same time as bulk semiconductor wafers are processed and even in the same wafer lots. In contrast, using conventional SOI structure 100 in Figure 1 to fabricate circuits would require more complex fabrication processes since the conventional SOI wafers typically cannot be fabricated using bulk semiconductor wafer processes or in the same wafer lots.

From the above description of the invention it is manifest that various techniques can be used for implementing the concepts of the present invention without departing from its scope. Moreover, while the invention has been described with specific reference to certain embodiments, a person of ordinary skill in the art would recognize that changes can be made in form and detail without departing from the spirit and the scope of the invention. The described embodiments are to be considered in all respects as illustrative and not restrictive. It should also be understood that the invention is not limited to the particular embodiments described herein, but is capable of many rearrangements, modifications, and substitutions without departing from the scope of the invention.

CLAIMS

1. A switching circuit comprising:

a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;

each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;

at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.

2. The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer.

3. The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer.

4. The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is an NFET with a gate driven by a switch control signal in a wireless communications device.

5. The switching circuit of claim 4, wherein said switch control signal drives said gate of said NFET through at least one resistor.

6. The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is a PFET with a gate driven by a switch control signal in a wireless communications device.

7. The switching circuit of claim 6, wherein said switch control signal drives said gate of said PFET through at least one resistor.

8. The switching circuit of claim 1, wherein a power amplifier in a wireless communications device provides an input to said switching circuit, and wherein an output of said switching circuit drives an antenna in said wireless communications device, and said switching circuit is controlled by a switch control signal in said wireless communications device.

9. The switching circuit of claim 8, wherein said wireless communications device is selected from the group consisting of a cellular telephone, a wireless personal computer, a wireless audio player, a wireless video player, and a wireless personal assistance device.

10. The switching circuit of claim 1, wherein an antenna in a wireless communications device provides an input to said switching circuit, and wherein an output of said switching circuit drives a low noise amplifier in said wireless communications device, and wherein said switching circuit is controlled by a switch control signal in said wireless communications device.

11. The switching circuit of claim 10, wherein said wireless communications device is selected from the group consisting of a cellular telephone, a wireless personal computer, a wireless audio player, a wireless video player, and a wireless personal assistance device.

12. A wireless communications device comprising a power amplifier and an antenna, said wireless communications device further comprising:

a switching circuit controlled by a switch control signal and interposed between said power amplifier and said antenna, said switching circuit including:

a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer, each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;

at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said

plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.

13. The wireless communications device of claim 12, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer.

14. The wireless communications device of claim 12, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer.

15. The wireless communications device of claim 12, wherein said wireless communications device is selected from the group consisting of a cellular telephone, a wireless personal computer, a wireless audio player, a wireless video player, and a wireless personal assistance device.

16. A wireless communications device comprising an antenna and a low noise amplifier, said wireless communications device further comprising:

a switching circuit controlled by a switch control signal and interposed between said antenna and said low noise amplifier, said switching circuit including:

a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer, each of said plurality of cascaded

transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;

at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.

17. The wireless communications device of claim 16, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer.

18. The wireless communications device of claim 16, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer.

19. The wireless communications device of claim 16, wherein said wireless communications device is selected from the group consisting of a cellular telephone, a wireless personal computer, a wireless audio player, a wireless video player, and a wireless personal assistance device.

ABSTRACT

A disclosed embodiment is a switching circuit including a number of transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer. Each transistor has a source/drain junction that does not contact the buried oxide layer, thus forming a source/drain junction capacitance. The disclosed switching circuit also includes at least one trench extending through the device layer and contacting a top surface of the buried oxide layer, thus electrically isolating at least one of the transistors in the switching circuit so as to reduce voltage and current fluctuations in the device layer. The disclosed switching circuit may be coupled to a power amplifier or a low noise amplifier and an antenna in a wireless communications device, and be controlled by a switch control signal in the wireless communications device.

Fig. 1

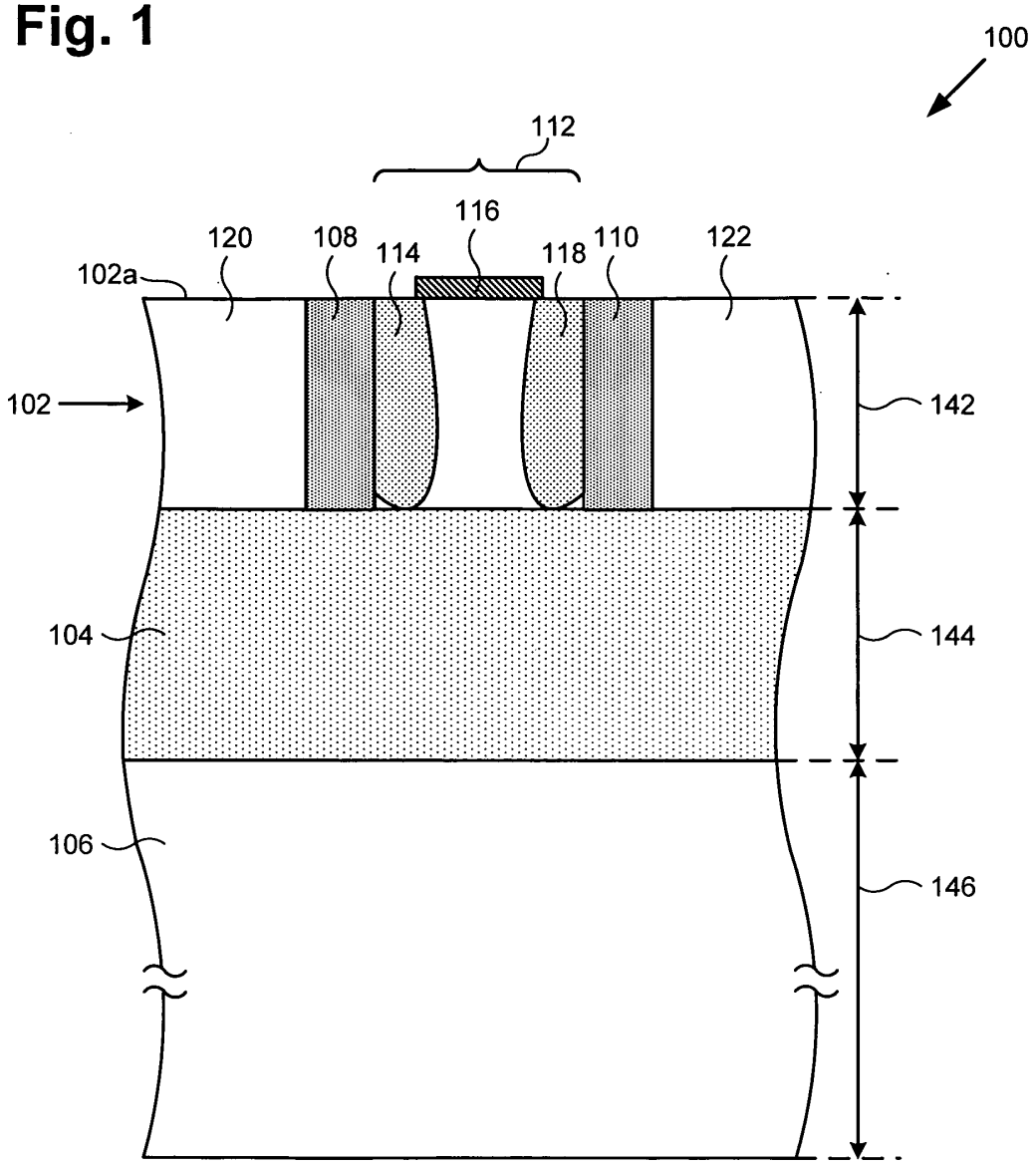

Fig. 2

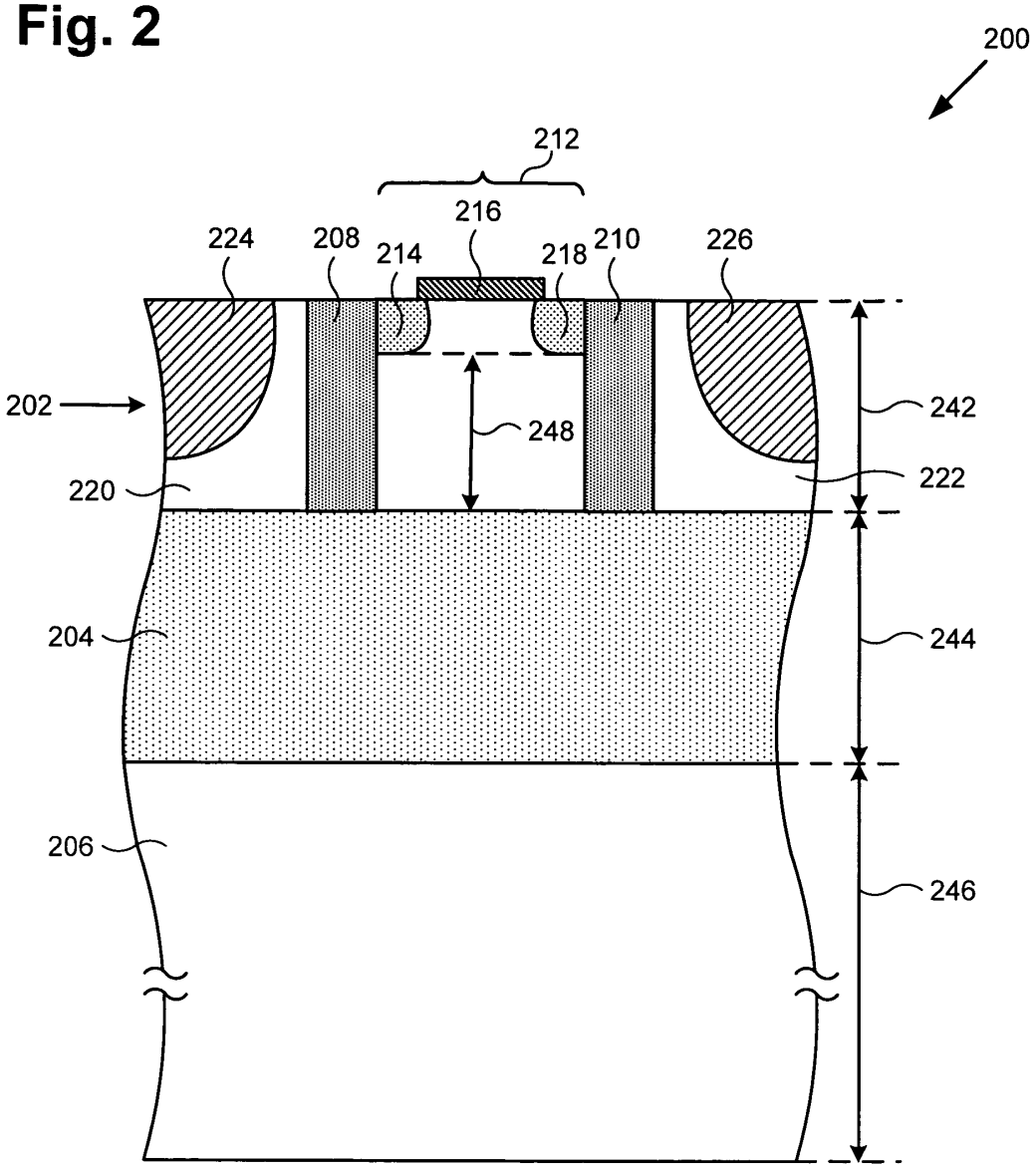
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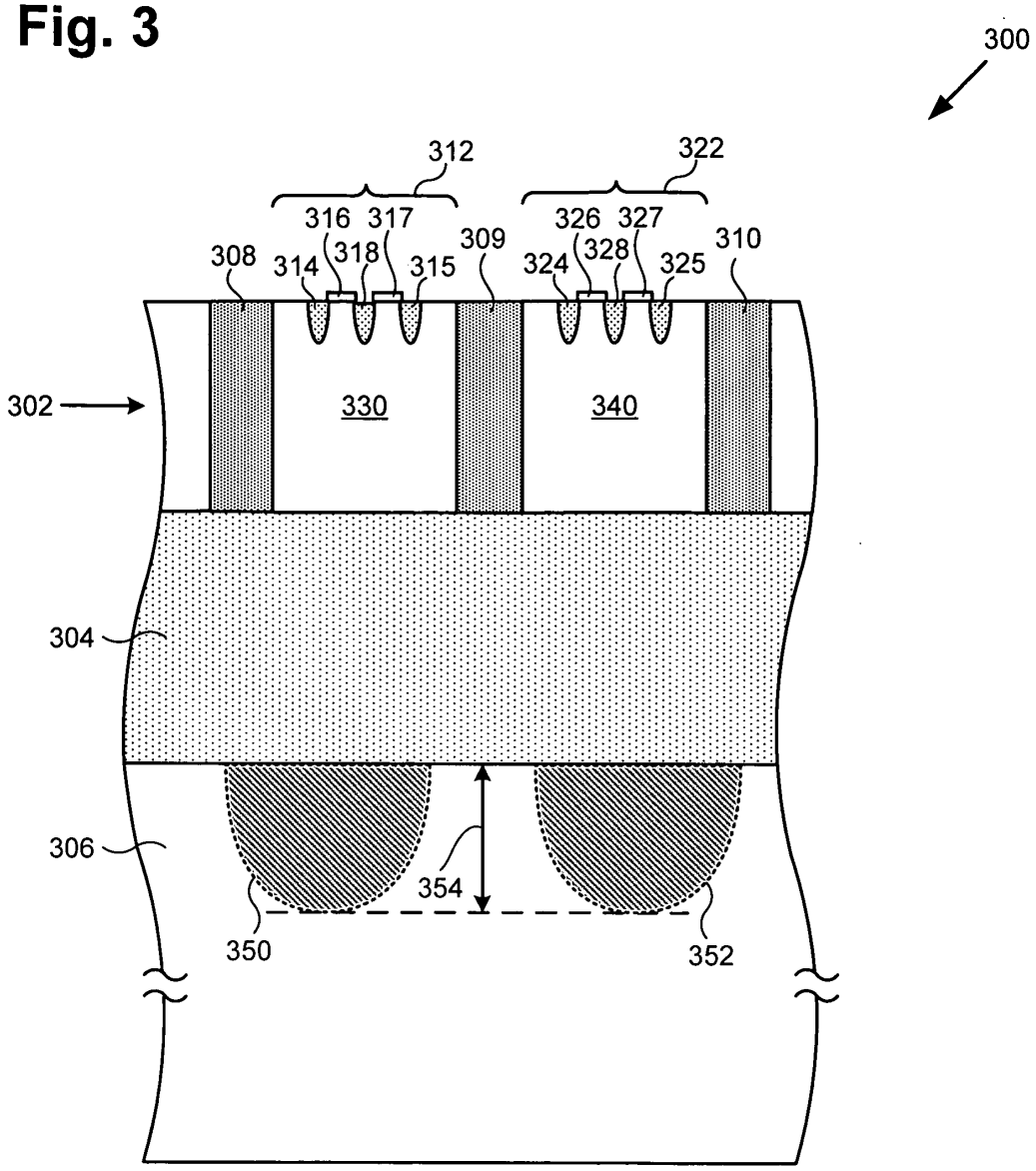
Fig. 3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322
316
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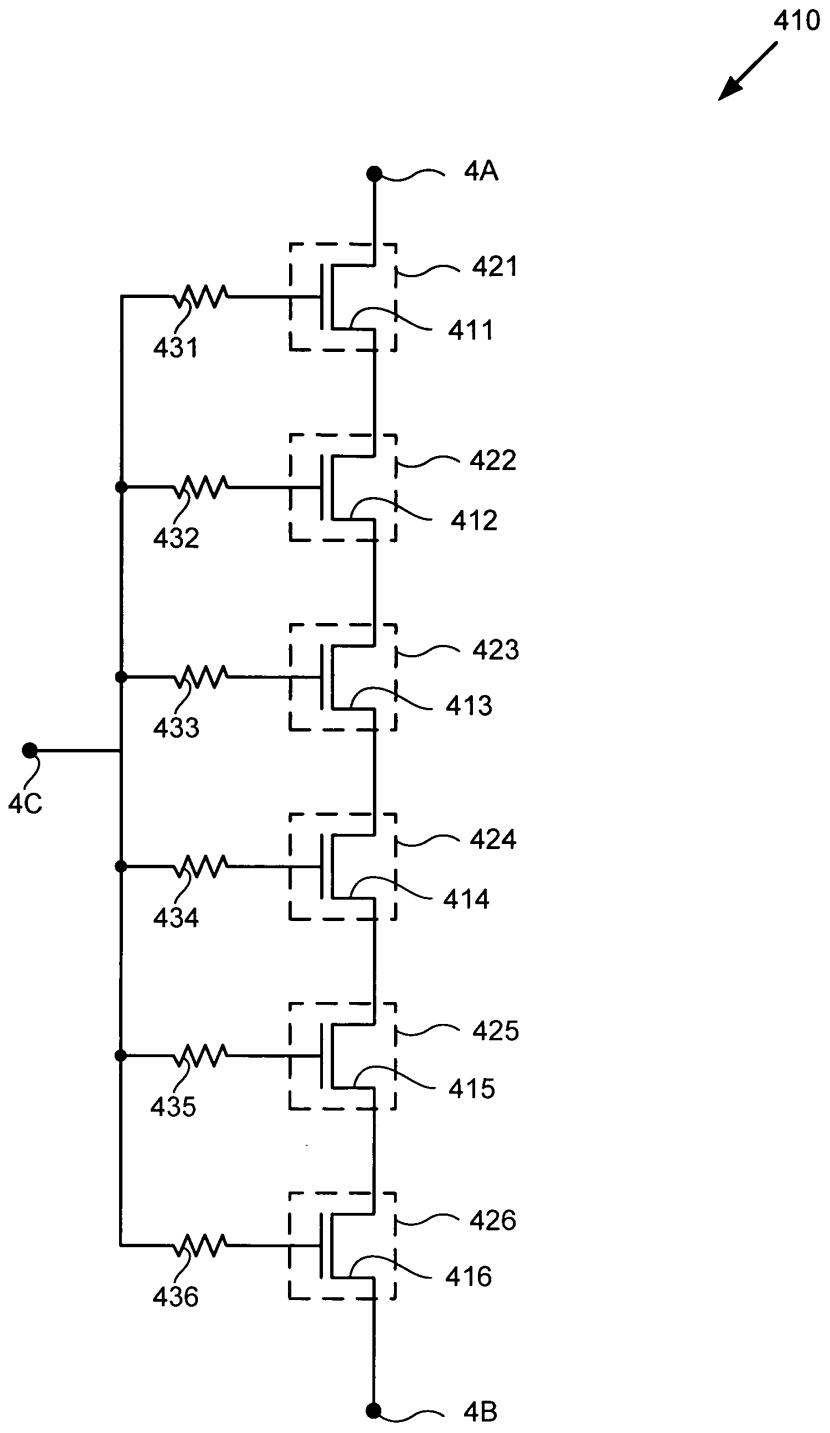
Fig. 4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4A
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431
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4C
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416
436
4B

Fig. 5

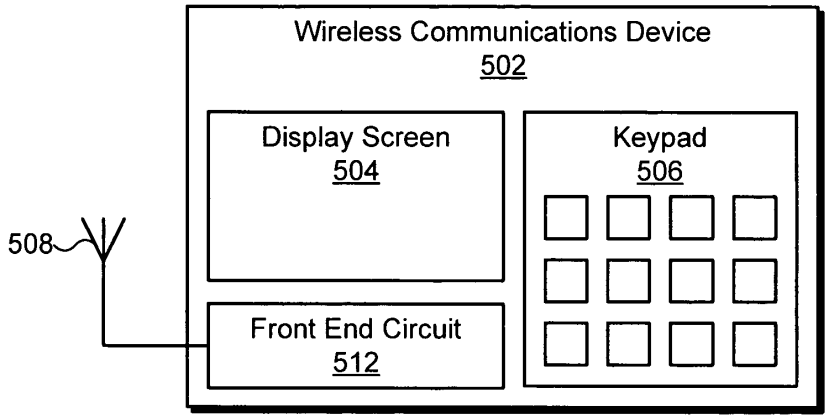

Wireless Communications Device
502
Display Screen
504
Keypad
506
508
Front End Circuit
512

Fig. 6

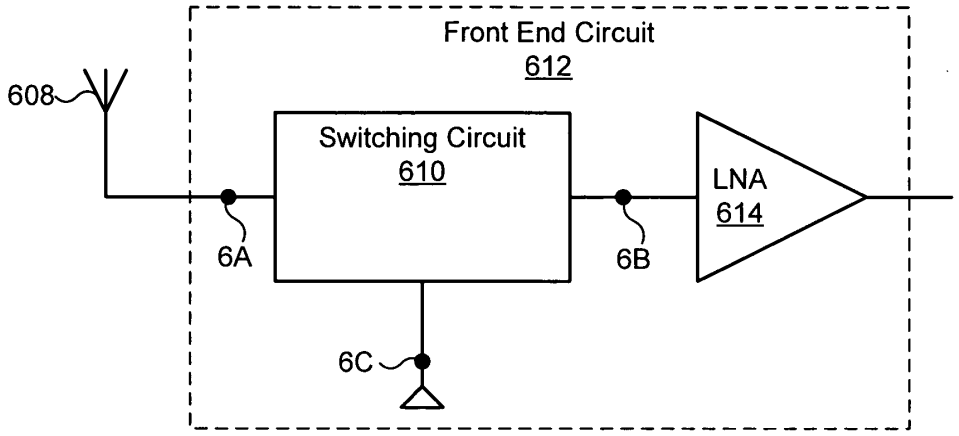
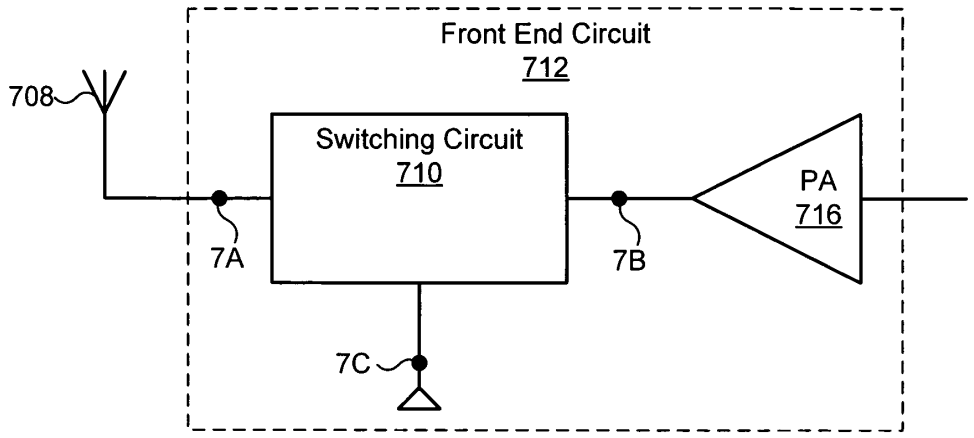

Front End Circuit
612
608
Switching Circuit
610
LNA
614
6A
6B
6C

Fig. 7


Front End Circuit
712
708
Switching Circuit
710
PA
716
7A
7B
7C

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: SEMICONDUCTOR ON INSULATOR (SOI) SWITCHING CIRCUIT.

The specification of which
a. ☒ is attached hereto
b. ☐ was filed on _____ as application serial no. _____ and was amended on _____ (if applicable) (in the case of a PCT-filed application) described and claimed in international no. filed _____ and as amended on _____ (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability of this application as defined in Section 1.56 of Title 37, Code of Federal Regulations (see the last page attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, Sections 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

a. ☒ no such applications has been filed.
b. ☐ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC Section 119

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

ALL FOREIGN APPLICATIONS, IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

I hereby claim the benefit under Title 35, United States Code, Sections 119 and 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose information material to patentability, as defined in Section 1.56 of Title 37, Code of Federal Regulations, which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. APPLICATION NUMBER	DATE OF FILING	STATUS
61/007,035	12/10/2007	Pending

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

MICHAEL FARJAMI, Reg. No. 38,135
FARSHAD FARJAMI, Reg. No. 41,014

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/firm/organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct them to the contrary.

Please direct all correspondence in this case to FARJAMI & FARJAMI LLP at the address indicated below:

FARJAMI & FARJAMI LLP
26522 La Alameda Avenue, Suite 360
Mission Viejo, CA 92691
Telephone: (949) 282-1000
Customer No. 25700

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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CITIZENSHIP OF INVENTOR: U.S.A.

SIGNATURE OF INVENTOR: Robert L Zwingman DATE: Sept 12, 2008

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CITIZENSHIP OF INVENTOR: U.S.A.

SIGNATURE OF INVENTOR: _____ DATE: Sept 12, 2008

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a *prima facie* case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A *prima facie* case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

(e) In any continuation-in-part application, the duty under this section includes the duty to disclose to the Office all information known to the person to be material to patentability, as defined in paragraph (b) of this section, which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

PATENT APPLICATION SERIAL NO._____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

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10/02/2008 WASFAW1  00000049 12286472

01 FC:1011                    310.00 OP
02 FC:1111                    510.00 OP
03 FC:1311                    210.00 OP
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PTO-1556
(5/87)

*U.S. Government Printing Office: 2002- 489-267/69033

PTO/SB/06 (10-07)
Approved for use through 06/30/2010. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 12286472

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	$155		N/A	$310
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	$255		N/A	$510
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	$105		N/A	$210
TOTAL CLAIMS (37 CFR 1.16(i))	19 minus 20 =	* —	X $25 =		OR	X $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	* —	X $105 =			X $210 =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $260 ($130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).		$130			$260	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			$185			$370	
			TOTAL			TOTAL	1030

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDI-TIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDI-TIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	X $25 =		OR	X $50 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $105 =		OR	X $210 =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					$185		OR	$370	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDI-TIONAL FEE ($)	OR	RATE ($)	ADDI-TIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	X $25 =		OR	X $50 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $105 =		OR	X $210 =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					$185		OR	$370	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.