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(54) INTEGRATED RF FRONT END WITH STACKED TRANSISTOR SWITCH

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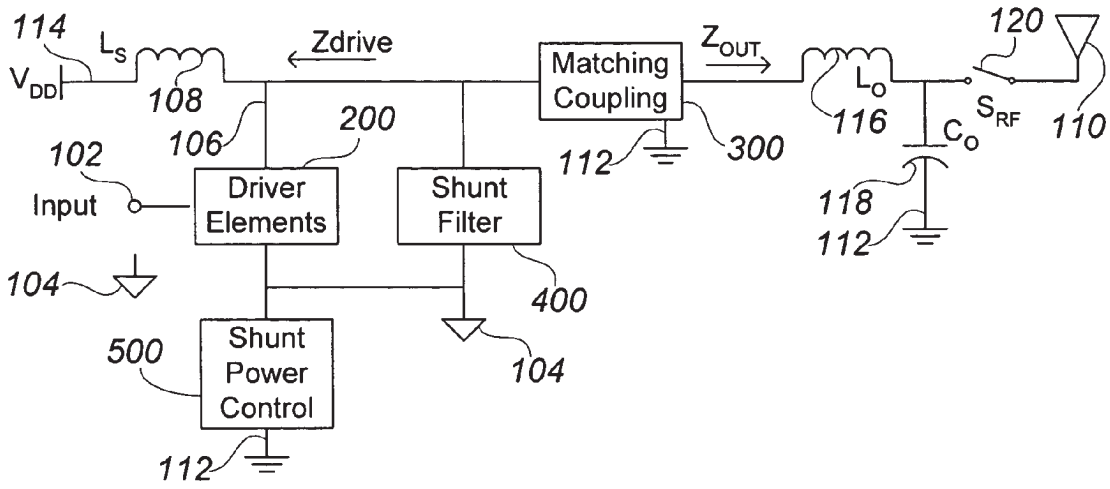
(57) **ABSTRACT**

A monolithic integrated circuit (IC), and method of manufacturing same, that includes all RF front end or transceiver elements for a portable communication device, including a power amplifier (PA), a matching, coupling and filtering network, and an antenna switch to couple the conditioned PA signal to an antenna. An output signal sensor senses at least a voltage amplitude of the signal switched by the antenna switch, and signals a PA control circuit to limit PA output power in response to excessive values of sensed output. Stacks of multiple FETs in series to operate as a switching device may be used for implementation of the RF front end, and the method and apparatus of such stacks are claimed as subcombinations. An iClass PA architecture is described that dissipatively terminates unwanted harmonics of the PA output signal. A preferred embodiment of the RF transceiver IC includes two distinct PA circuits, two distinct receive signal amplifier circuits, and a four-way antenna switch to selectably couple a single antenna connection to any one of the four circuits.



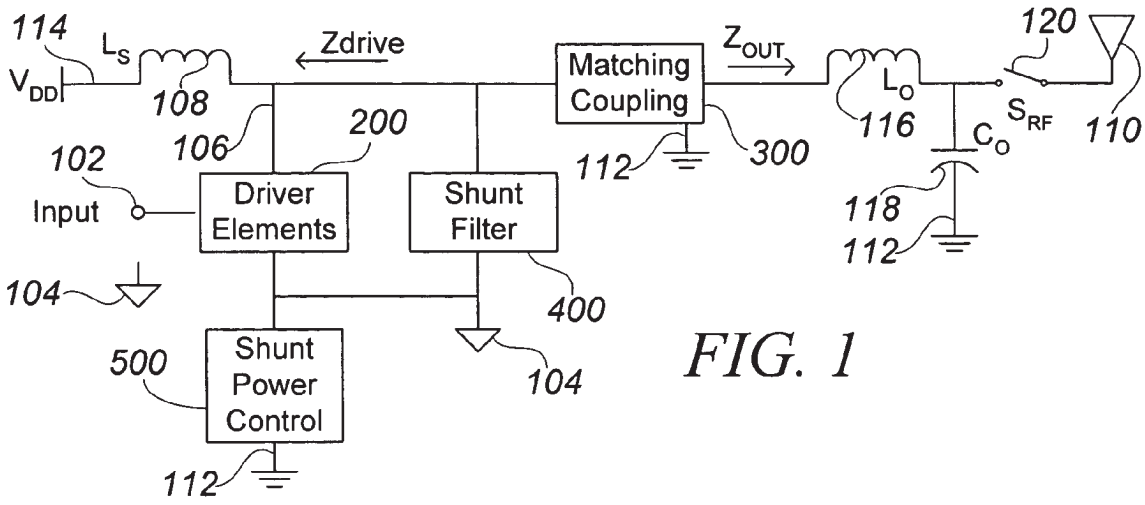

114
L_S
V_{DD}
108
Zdrive
106
200
102
Input
Driver Elements
Shunt Filter
104
400
500
Shunt Power Control
112
104
Matching Coupling
Z_{OUT}
112
300
L_O
116
C_O
118
112
S_{RF}
120
110

FIG. 1

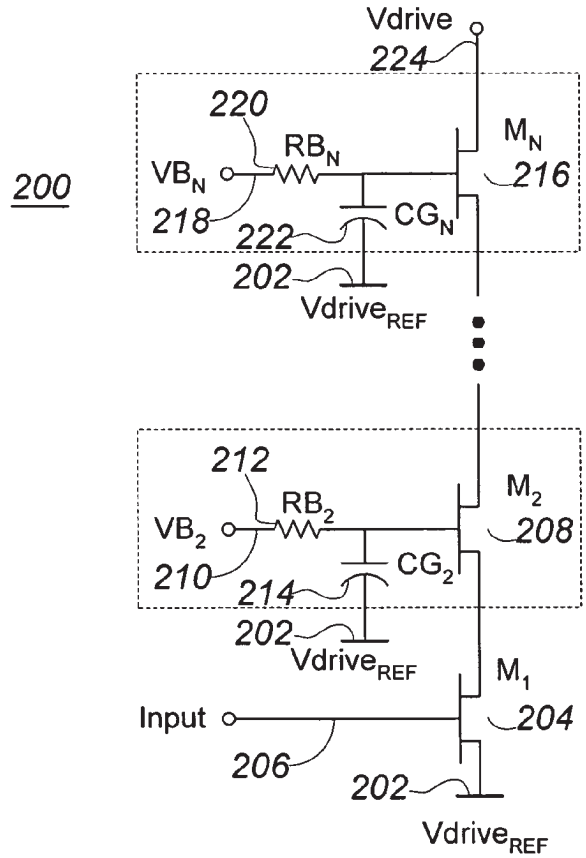

Vdrive
224
200
220
RB_N
M_N
VB_N
216
218
CG_N
222
202
$Vdrive_{REF}$
212
RB_2
M_2
VB_2
208
210
CG_2
214
202
$Vdrive_{REF}$
M_1
Input
204
206
202
$Vdrive_{REF}$

FIG. 2

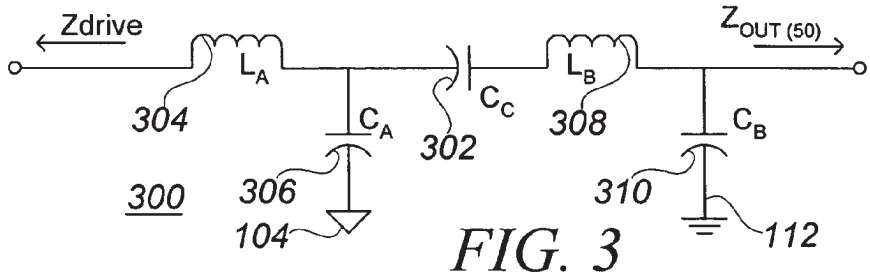


FIG. 3

FIG. 4

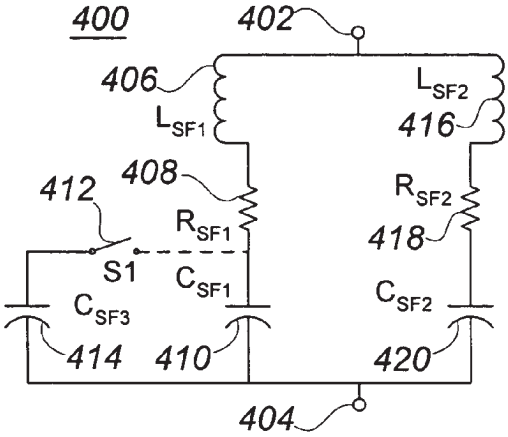


FIG. 5

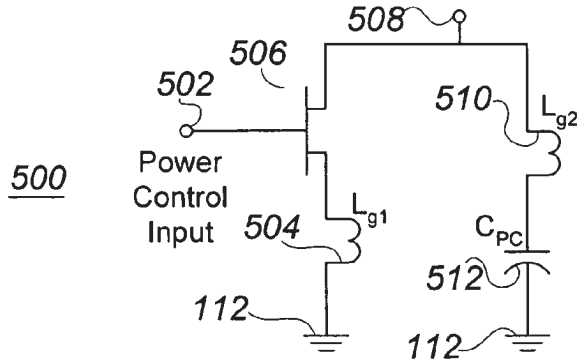
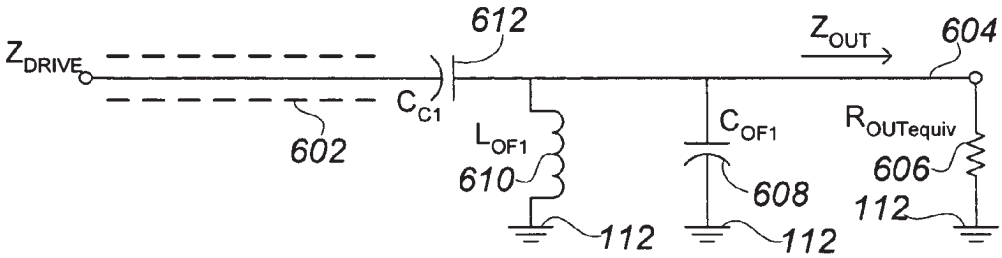


FIG. 6



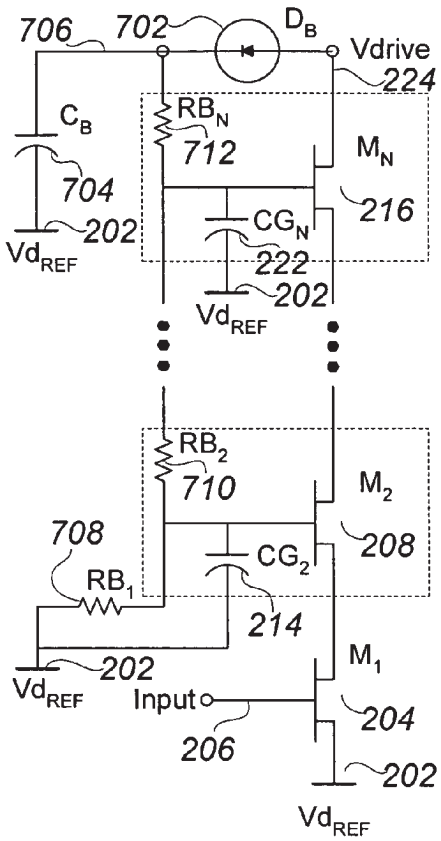

706
702
D_B
Vdrive
224
C_B
RB_N
712
M_N
704
216
202
CG_N
Vd_{REF}
222
202
Vd_{REF}
RB_2
710
M_2
708
208
CG_2
RB_1
214
202
M_1
Vd_{REF}
Input
204
206
202
Vd_{REF}

FIG. 7

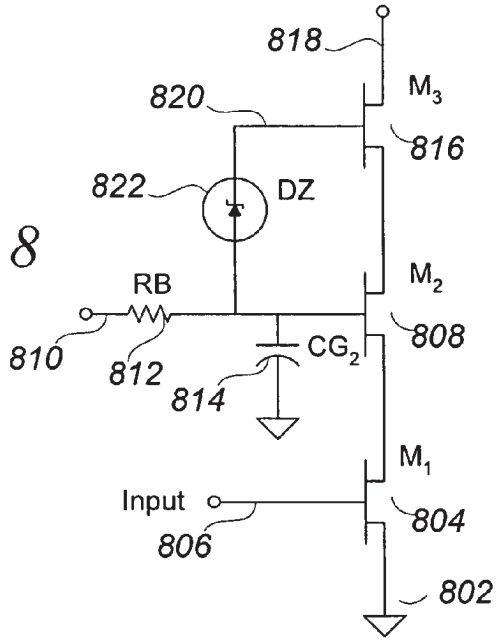

818
M_3
820
816
822
DZ
RB
M_2
810
812
CG_2
808
814
M_1
Input
804
806
802

FIG. 8

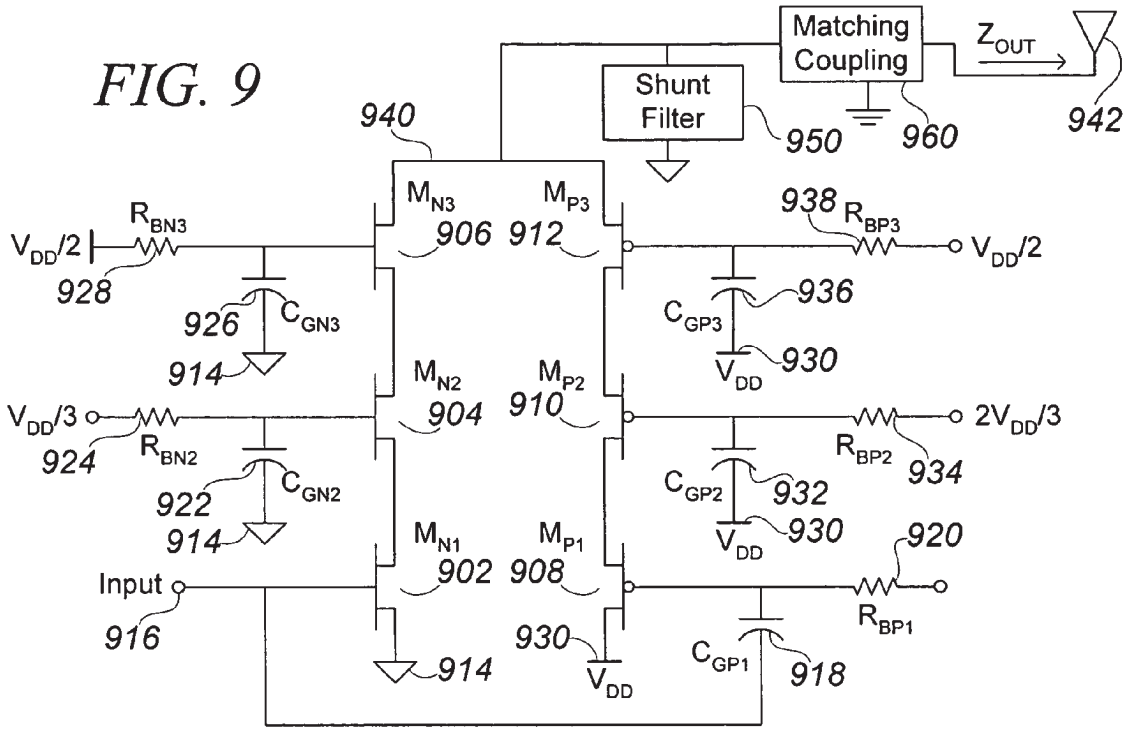


FIG. 9
Matching Coupling
Z_{OUT}
Shunt Filter
940
950
960
942
M_{N3}
M_{P3}
906
912
938
R_{BP3}
$V_{DD}/2$
R_{BN3}
928
926
C_{GN3}
914
C_{GP3}
936
V_{DD}
930
M_{N2}
M_{P2}
904
910
$V_{DD}/3$
924
R_{BN2}
922
C_{GN2}
$2V_{DD}/3$
R_{BP2}
934
C_{GP2}
932
M_{N1}
M_{P1}
902
908
920
Input
916
R_{BP1}
C_{GP1}
918

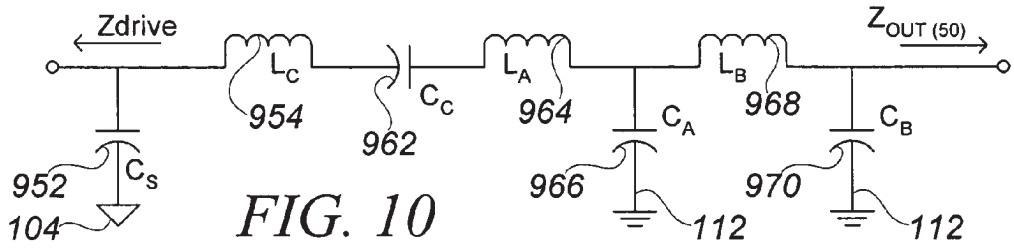

Zdrive
L_C
954
C_C
962
L_A
964
C_A
966
L_B
968
C_B
970
$Z_{OUT\ (50)}$
C_S
952
104
112
112

FIG. 10

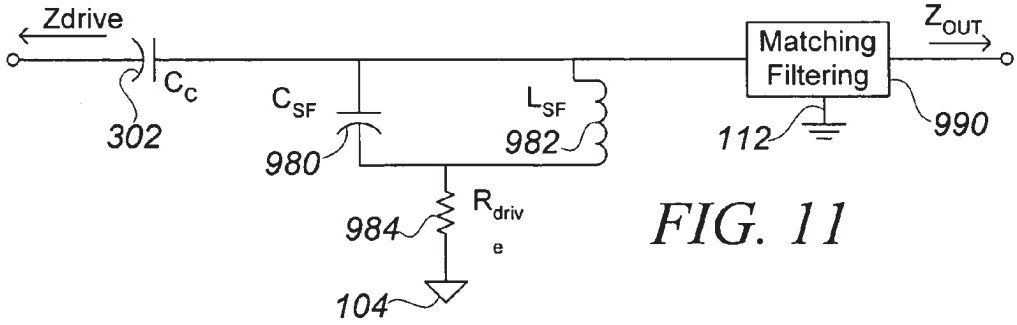

Zdrive
C_C
302
C_{SF}
980
L_{SF}
982
Matching Filtering
Z_{OUT}
112
990
984
R_{driv}
e
104

FIG. 11

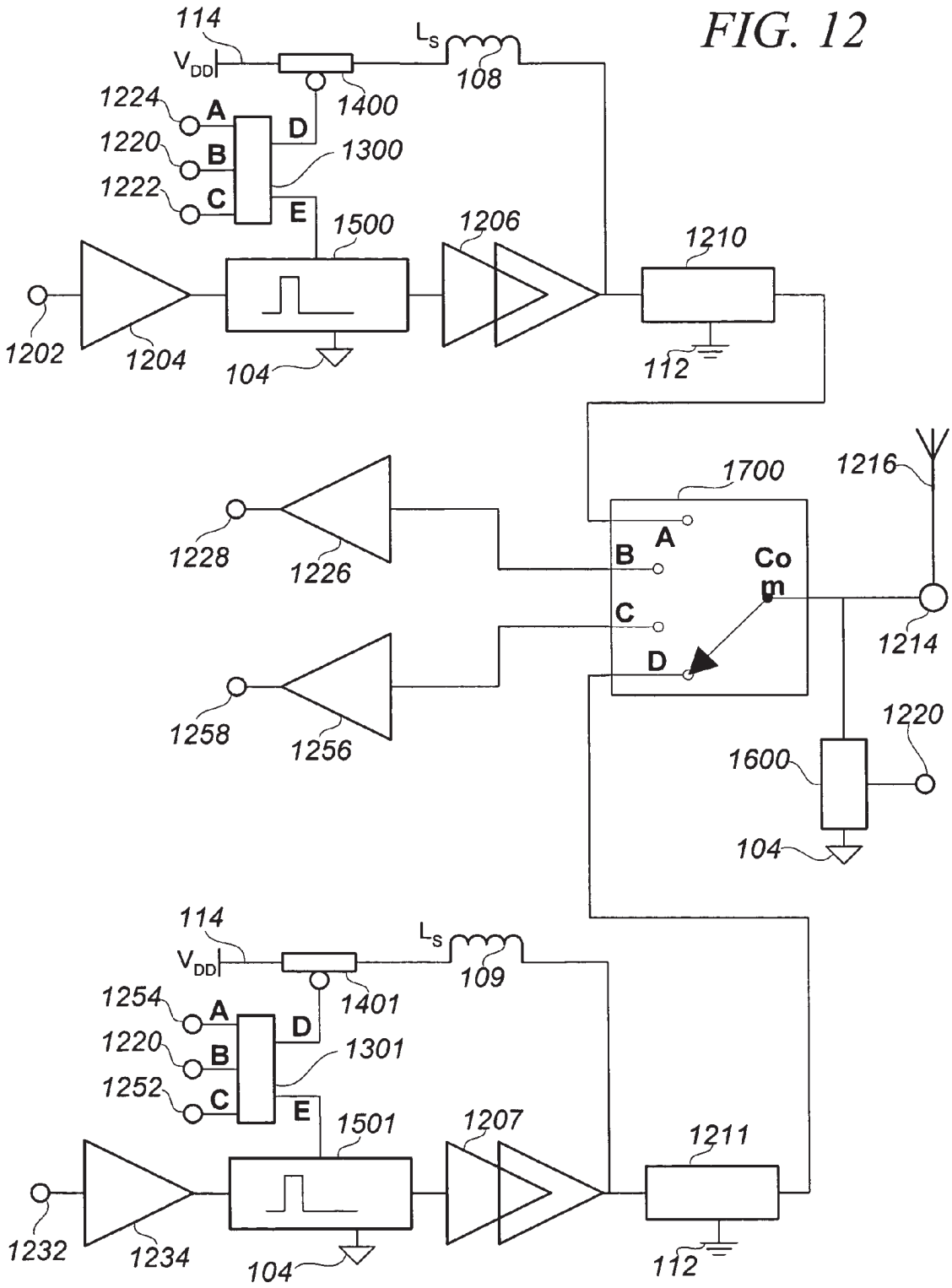


FIG. 12
114
V_{DD}
L_S
108
1400
1224
A
D
1220
B
1300
1222
C
E
1500
1206
1210
1202
1204
104
112
1700
1216
1228
1226
A
B
Com
C
D
1214
1258
1256
1220
1600
104
114
V_{DD}
L_S
109
1401
1254
A
D
1220
B
1301
1252
C
E
1501
1207
1211
1232
1234
104
112

FIG. 13

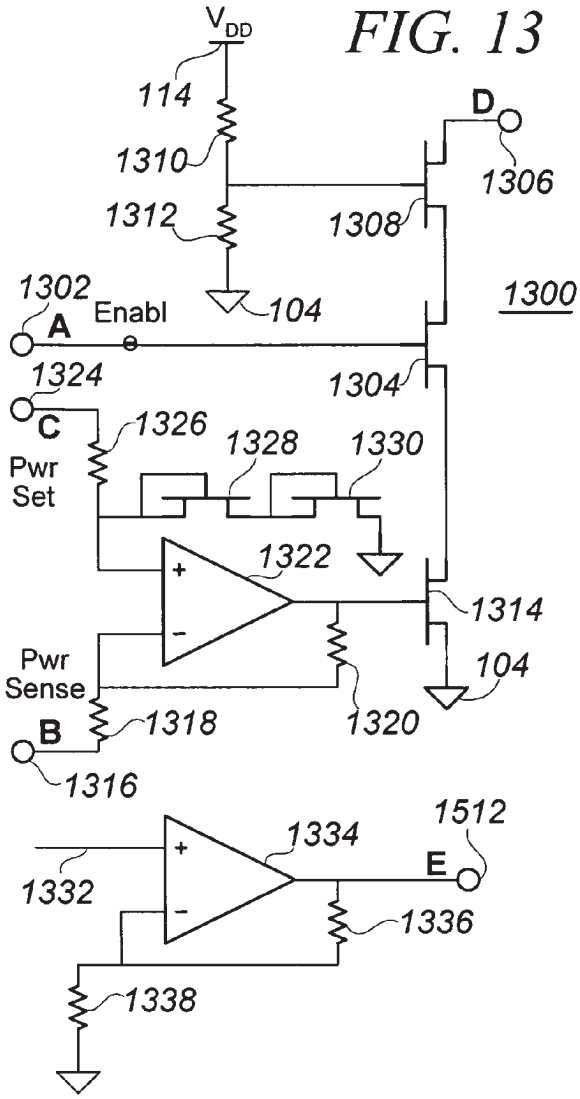


FIG. 14

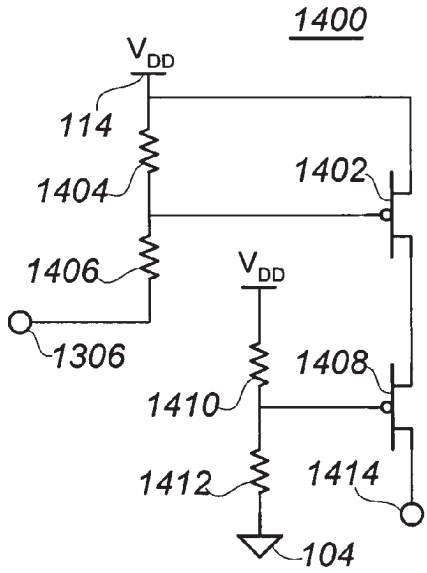


FIG. 15

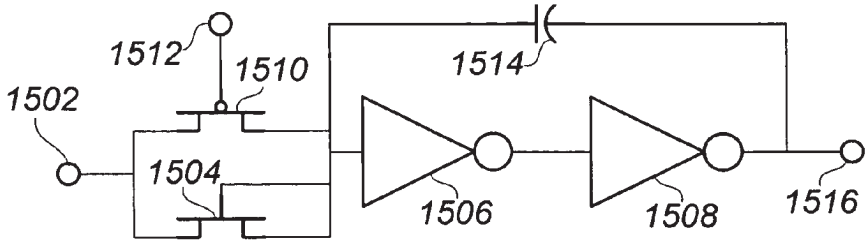
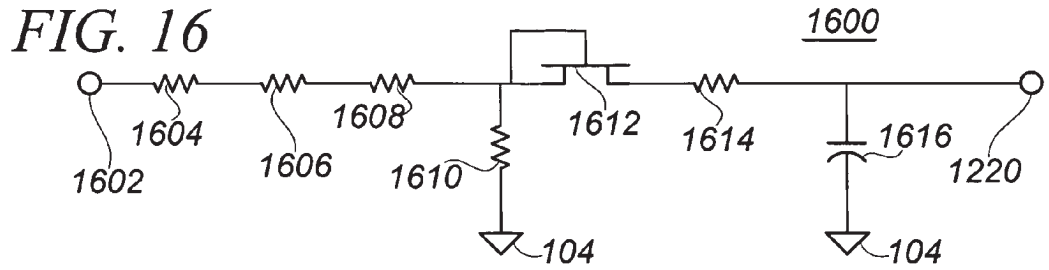


FIG. 16


1600
1602
1604
1606
1608
1610
1612
1614
1616
1220
104
104

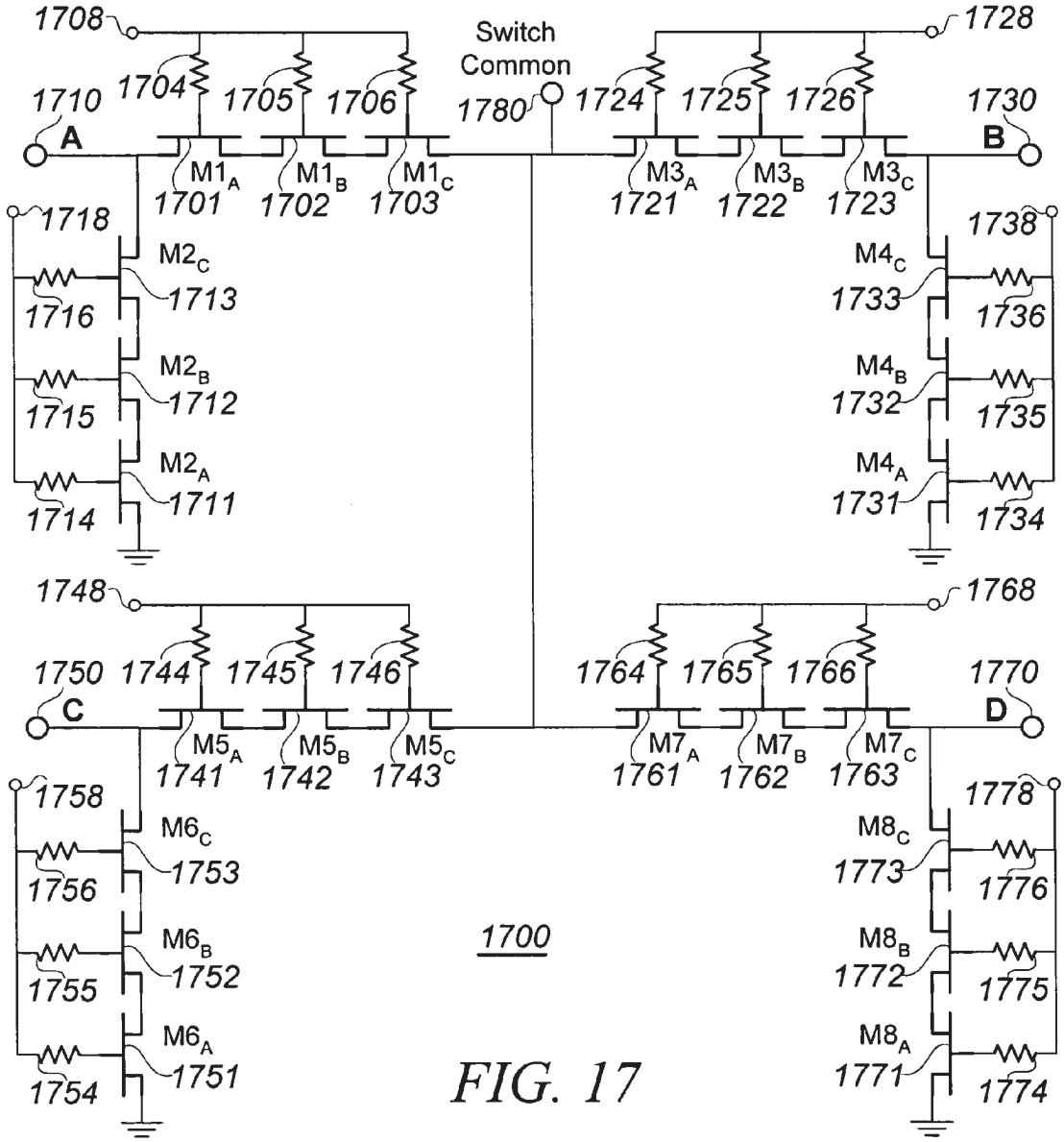

1708
Switch
Common
1728
1710
1704
1705
1706
1780
1724
1725
1726
1730
A
B
M1A
M1B
M1C
M3A
M3B
M3C
1701
1702
1703
1721
1722
1723
1718
1738
M2C
M4C
1713
1733
1716
1736
M2B
M4B
1712
1732
1715
1735
M2A
M4A
1711
1731
1714
1734
1748
1768
1750
1744
1745
1746
1764
1765
1766
1770
C
D
M5A
M5B
M5C
M7A
M7B
M7C
1741
1742
1743
1761
1762
1763
1758
1778
M6C
M8C
1753
1773
1756
1776
M6B
M8B
1752
1772
1755
1775
1700
M6A
M8A
1751
1771
1754
1774

FIG. 17

INTEGRATED RF FRONT END WITH STACKED TRANSISTOR SWITCH

[0001] This application is a continuation of copending and commonly assigned U.S. patent application Ser. No. 11/158,597 filed Jun. 22, 2005 and entitled "Integrated RF Front End," which is a continuation-in-part of co-pending and commonly assigned U.S. patent application Ser. No. 10/875,405 filed Jun. 23, 2004 and entitled "Stacked Transistor Method and Apparatus," and is related to the following commonly owned U.S. patent documents: U.S. Pat. No. 5,663,570, issued Sep. 2, 1997 and entitled "High-Frequency Wireless Communication System on a Single Ultrathin Silicon On Sapphire Chip," U.S. Pat. No. 6,804,502, issued Oct. 12, 2004 and entitled "Switch Circuit and Method of Switching Radio Frequency Signals," and copending, published U.S. patent application Ser. No. 10/658,154, filed Sep. 8, 2003 and entitled "Low Noise Charge Pump Method and Apparatus;" and the entire contents of each of these six U.S. patent documents are hereby incorporated herein in their entireties by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention relates broadly to integrated electronic circuits, and more specifically to RF transceiver circuitry.

[0004] 2. Related Art

[0005] Wireless communications devices, especially handheld devices, are undergoing sustained development. Perhaps more than any other factor, the extreme popularity of cellular mobile telephones has motivated improvements in efficiency, speed, size and cost-effectiveness for RF transmission circuits in handheld devices. Enhancing the efficiency of such circuits is highly desirable so that the size of the required batteries may be reduced, while their life is extended. Cost-effectiveness is clearly always desirable for consumer products, particularly when such products require periodic replacement to stay abreast of changes in the technology. The steady advance of functionality in cellular telephones, combined with consumer preferences for light and small devices, puts a premium on reducing the volume required for RF transmission circuits. Additionally, transmitters must meet stringent emission limits, which have been established in order to facilitate high communication density at minimal power levels.

[0006] Most wireless communication units, such as cellular telephones, comprise at least one RF transceiver. A communication device, such as a cellular telephone, may comprise a multiplicity of RF (radio frequency) front end circuits, which are of primary interest herein. RF front end circuits (or subcircuits) typically include an RF transmit signal amplifier, a Power Amplifier (PA), a matching and filtering section, an antenna switch, and may include a received signal amplifier. A complete transceiver generally also includes a low-noise amplifier for the received signal. Of these circuits, the PA subcircuit is typically the most power-consuming portion of such transmitters, and, also typically, is the source of the most significant unintended or "spurious" emissions. In order to extend battery life, to meet stringent spurious emissions standards, and to minimize the cost of these high-volume consumer items, there is a need to improve the speed and efficiency, while reducing spurious emissions and manufacturing costs, for such PA subcircuits. Due to their need to handle high power, the PA and antenna switch subcircuits consume the most integrated circuit area. Manufacturing costs for integrated circuits are strongly dependent on the amount of device area required for each circuit. Consequently, substantial reductions in the area required for the various RF transceiver subsections will generally lead to commensurate reductions in manufacturing costs for transceiver circuits.

[0007] A range of PA topologies have been developed, each having different advantages. For example, PAs of class A, B, C, D, E and F are well known in the art. The primary amplifying devices in PAs of classes A-C are designed to operate in an "active" region of their operating range, thus intentionally conducting current while voltage is present across the device.

[0008] PAs of classes D, E and F attempt to reduce the power loss caused by such linear operation by employing amplifier devices as switches that minimize operation in active regions, rather than as linear amplifiers. However, the pulse-type outputs from such amplifiers generally require extensive filtering in order to establish a narrow-band sinusoidal output, as is typically required. While normal operation of PAs in classes D-F does not intentionally cause drive element devices to conduct while voltage is present across the devices, even switched devices consume real power due to current flowing while voltage is present during finite switching periods. Moreover, compared to drive devices in analog PAs operating at the same transmission center frequency, drive devices in class D-F switching circuits must often operate at much higher frequencies. The higher frequency signals include significant energy at undesired frequencies, and such undesired signal energies not only consume circuit power, but also require filtering to meet emission limits.

[0009] Integration of devices is generally desirable in order to improve various features of the resulting product, such as operating frequency and reliability, and may also reduce overall manufacturing costs, as well as likely reducing the volume occupied by the circuits. Field Effect Transistors (FETs) are extremely popular for both linear amplification and switching purposes in integrated circuits. However, integrated circuit (IC) FETs have a limited capability to withstand voltage between any two nodes, including gate-source, gate-drain, and drain-source node pairs. Such voltage withstand limitations may particularly impair the usefulness of IC FETs in high power switching circuits, in which inductive voltages may greatly exceed the supply voltage. As a particular example, the transmission output power capability of an RF PA is highly dependent upon the amplitude of the output voltage. One of the difficulties with existing PA technologies is that many otherwise desirably high-speed devices are fabricated using processes that tend to yield FETs having relatively low breakdown voltages. It is very desirable to solve this problem ant thereby provide a wider voltage range while retaining other desirable integrated device features. Such a solution enables integration on monolithic integrated circuits of power and control features that previously required separate processing, such as PA features and RF switch features. Integration of interacting circuits that were previously discrete will enhance

yield and predictability, due to the process matching that is inherent in monolithic integration.

[0010] Methods and circuits are described herein that facilitate the fabrication of all of the transceiver RF circuits of a dual-band transceiver onto a single integrated circuit, thereby solving the problems and gaining the benefits noted above. Many of the benefits are achieved by integrating even the front-end portions of transceivers that do not necessarily include dual-band operation. One or more alternatives are described for each of numerous subcircuits (or corresponding methods), and a fully integrated RF front end, or an integrated RF transceiver, may be fabricated by using any compatible one of such alternatives for each section of the transceiver. Moreover, several of the subcircuits (or corresponding methods) that permit an integrated RF transceiver to be realized are also useful in other contexts, often independently of other RF transceiver subcircuits. Thus, various subcombinations of features described herein constitute useful inventions in their own right. Combined, various aspects of these subcombinations together achieve an integrated dual-band RF transceiver having all of the benefits noted above. Particularly notable among the independently useful subcircuits are stacked-FET RF switches and particular PA circuit topologies. Finally, the integration of certain RF transceiver subsections permits efficiencies in manufacturing without compromising safety and reliability of the final product.

SUMMARY

[0011] A combination of methods and/or circuits is described that enables the fabrication of a self-protected monolithic integrated circuit including all of the RF front-end sections of a communications transceiver. Such self-protected RF front-end circuits particularly include those sections, from a Power Amplifier (PA) through an antenna connection, that permit efficient internal protection from overload due to an improper, missing or damaged antenna.

[0012] Several subcombinations of the self-protected monolithic integrated RF front-end circuits have independent importance. One such subcombination is an integrated stacked-FET switch. One embodiment of this subcombination is a circuit including a multiplicity of FETs in a stack having drain-source channels coupled in series to control conductivity between nodes in a circuit. A control signal is coupled to a first FET to cause changes in conductivity of the first FET, and conductivity of the remaining FETs is enslaved to the conductivity of the first FET. A voltage withstand capability across the series combination of the FET stack may be substantially equal to a sum of drain-source voltage withstand capabilities of the individual FETs of the stack. A gate of each FET other than the first FET may be capacitively coupled to a common voltage.

[0013] Another subcombination is an RF Power Amplifier (PA) that may be referred to as an integrated iClass PA. One embodiment of this subcombination includes an input controlling an RF switch whose output is coupled to a supply source via an RF choke, and which operates with a characteristic drive output impedance at an operating frequency f_0. The drive output is coupled to an antenna connection having an expected antenna impedance via a coupling circuit that matches the drive output impedance to the expected antenna impedance, and also includes a circuit that dissipatively terminates signals at one or more harmonics of the operating frequency f_0. The iClass RF PA may further include a shunt filter configured to provide local minimum impedances between the drive output and the reference at a plurality of frequencies, including an even harmonic of f_0 and a non-unity odd harmonic of f_0. These minimum impedances may be approximately equal to the characteristic drive impedance.

[0014] One embodiment of the self-protected front-end circuit is an integrated circuit that includes a PA having an output amplitude regulator circuit that is controlled by an output limiting controller. The embodiment further includes an antenna switch that selectably couples an antenna connection to either the PA, via a matching and coupling circuit, or to a receive signal amplifier. The embodiment also includes an antenna connection sensor configured to sense current through, and/or voltage at, the antenna connection, and circuitry coupling an output of the antenna connection sensor to the output limiting controller, which is configured to affect the output amplitude regulator circuit to prevent the existence of currents or voltages in excess of design limits at the antenna connection.

[0015] A related embodiment is a method of making a monolithically integrated PA with protection from excessive output values caused by high Voltage Standing Wave Ratios (VSWRs) that are due to improper antenna impedance. The embodiment includes fabricating an RF PA on an integrated circuit chip to receive a transmit signal, and providing an output power limiting circuit for the PA. It also includes fabricating coupling, matching and filtering circuits on the same integrated circuit to condition a PA output signal having a PA output impedance to a different impedance desired for a connecting element that is connected to the integrated circuit to couple the conditioned signal to an antenna. The embodiment further includes disposing an antenna switch on the integrated circuit between the PA and the connecting element whereby the connecting element may be controllably coupled to either the conditioned signal from the PA, or to a receive amplifying circuit disposed on the integrated circuit. The embodiment includes providing a sensing circuit to sense a parameter of the signal delivered to the connecting element, and a PA control circuit to reduce power of the PA output signal in response to a value of the sensed parameter that is deemed excessive.

[0016] An embodiment of a further subcombination is a method of amplifying RF signals, and includes providing a plural-FET stack to control conduction between an output drive node and a reference node to effect a characteristic impedance at an operating frequency f_0. The embodiment further includes disposing, between the output drive node and the reference node, a shunt filter configured to dissipatively terminate a harmonic frequency of f_0. The shunt filter may include local minimum impedances at an even harmonic of f_0 and at a non-unity odd harmonic of f_0, and the local minimum impedances may be approximately equal to the characteristic impedance of the FET stack.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Embodiments of the present invention will be more readily understood by reference to the following figures, in which like reference numbers and designations indicate like elements.

[0018] **FIG. 1** is a block schematic diagram representative of some types of RF power amplifier (PA) circuitry.

[0019] **FIG. 2** is a generalized schematic diagram of a stacked-FET control circuit useable with a PA such as shown in **FIG. 1**.

[0020] **FIG. 3** is a simplified schematic diagram of an impedance matching and coupling bandpass filter useable in a PA such as shown in **FIG. 1**.

[0021] **FIG. 4** is a simplified schematic diagram of a shunt filter useable in a PA such as shown in **FIG. 1**.

[0022] **FIG. 5** is a simplified schematic diagram of a shunt power control circuit useable in a PA such as shown in **FIG. 1**.

[0023] **FIG. 6** is a simplified schematic diagram of an output filter for Class F operation of a PA such as shown in **FIG. 1**.

[0024] **FIG. 7** is a schematic diagram illustrating alternative biasing features for a stacked-FET amplifying circuit.

[0025] **FIG. 8** is a simplified schematic diagram illustrating an alternative method of biasing FETs of a FET stack.

[0026] **FIG. 9** is a simplified schematic diagram of a Class D PA employing complementary stacked-FET drive elements.

[0027] **FIG. 10** is a schematic diagram of exemplary output filtering for a Class D PA such as represented in **FIG. 9**.

[0028] **FIG. 11** is a simplified schematic diagram of a harmonic termination shunt filter useable in a PA such as shown in **FIG. 1**.

[0029] **FIG. 12** is a simplified schematic diagram of an integrated dual-band RF transceiver.

[0030] **FIG. 13** is a schematic diagram of an exemplary PA output power supervisor for directing output power levels in the transceiver of **FIG. 12**.

[0031] **FIG. 14** is a schematic diagram of an exemplary series output regulator for the transceiver of **FIG. 12**.

[0032] **FIG. 15** is a schematic diagram of an exemplary pulse width controller for the transceiver of **FIG. 12**.

[0033] **FIG. 16** is a schematic diagram of an exemplary output voltage detector for the transceiver of **FIG. 12**.

[0034] **FIG. 17** is a schematic diagram of an exemplary dual-band antenna switch for the transceiver of **FIG. 12**.

DETAILED DESCRIPTION

I. Power Amplifier Overview

[0035] **FIG. 1** is a block diagram of an RF power amplifier (PA). The illustrated RF PA is quite general, in that varying the biasing of devices in a driver elements block **200**, and/or varying details of the other blocks, will permit the RF PA illustrated in **FIG. 1** to operate in any of amplifier classes A, B, C, E, F, or, as described further herein, as an iClass amplifier. **FIGS. 2-5** each show an exemplary circuit to implement one of the blocks shown in **FIG. 1**.

[0036] An input **102** is provided to the PA with respect to a circuit reference, or common, **104**. The input **102** generally comprises a properly biased signal at a center drive frequency, f_0. In response to the input **102**, the driver elements block **200** controls conduction between a drive output node **106** and the circuit common **104**. The driver elements block **200**, in conjunction with current from V_{DD} via an RF choke (RFC) L_S **108**, provides a signal having a particular impedance Zdrive. Zdrive may vary with frequency, but will refer to the drive impedance at the center operating frequency f_0, unless otherwise indicated. A shunt filter **400** may be coupled between the drive output node **106** and the circuit common **104**. Numerous different filtering arrangements may be used, some examples of which are described subsequently herein.

[0037] An antenna **110** has a characteristic impedance Z_{OUT}, generally 50Ω (at the center frequency f_0 unless otherwise indicated). A block **300** is typically required to provide matching and coupling between the drive node **106** (at Zdrive) and the output at Z_{OUT}. Following the matching and coupling, an output filter section such as the combination of L_O **116** and C_O **118** may typically be disposed in the signal path before an RF switch, S_{RF} **120**, which appropriately couples the output to the antenna **110**. Because the PA circuit is integrated on a semiconductor device, and the antenna **110** is typically external to the IC comprising the PA, the antenna **110** often operates with a different reference voltage, for example a chassis ground **112**, which has a non-zero impedance to the circuit common **104**. Accordingly, the matching-coupling block **300**, as well as the filter section **116-118**, has an output that is referenced to chassis ground **112**.

[0038] Power control may optionally be provided. One example employs a shunt power control block **500**, which may provide a voltage offset between chassis ground **112** and circuit common **104** to reduce the amplitude of signals received by the antenna **110**. A series regulator circuit, such as items **1400-1401** in **FIG. 12**, is probably used more commonly.

[0039] The monolithically integrated RF PAs, RF front ends, and RF transceivers described herein may be fabricated to operate at relatively high frequencies of at least 900 MHz and/or 2.4 GHz, and at moderate power levels. These designs are useful for transceivers having transmit power maximums of at least 0.5 W, 1 W, or 1.5 W RMS of RF output power delivered to the antenna connection when it is properly coupled to a matched antenna.

II. Stacked-FET Drivers

[0040] **FIG. 2** is a simplified schematic diagram of a stacked-FET circuit that may be used for the driver elements block **200** in the RF PA of **FIG. 1**, for controlling conduction between the drive output node **106** and the circuit common **104**. The stack includes two or more FETs of the same polarity, i.e., all FETs in a stack are N-channel FETs, or all are P-channel FETs, or at least all FETs in a stack operate substantially similarly as each other.

[0041] The FET stack **200** of **FIG. 2** is configured to control conduction between two nodes of an integrated circuit. A terminal $Vdrive_{REF}$ **202** is connected to one of the two nodes (e.g., circuit common **104** in **FIG. 1**), while a terminal Vdrive **224** is connected to the other node (e.g., Vdrive **106** in **FIG. 1**). For N-channel FETs (N-FETs) as illustrated in **FIG. 2**, $Vdrive_{REF}$ **202** will be connected to the

more negative of the two nodes, for example to circuit common **104** in **FIG. 1**. The terminal $Vdrive_{REF}$ **202** is coupled to the source of a first FET of the stack **200**, M_1 **204**.

[**0042**] The FET stack **200** is controlled by means of an input signal, relative to terminal $Vdrive_{REF}$ **202**, that is coupled to the gate of the signal-input FET M_1 **204** via an input terminal **206**. The drain of M_1 **204** is coupled to the source of a second FET M_2 **208**. The gate of M_2 **208** is provided with a bias voltage VB_2 **210** via a bias resistor RB_2 **212**, and is decoupled to $Vdrive_{REF}$ **202** via CG_2 **214**. In some embodiments, these two FETs are sufficient, when properly configured to divide applied voltages so as to avoid exceeding breakdown limits of either device, to serve as a conduction controlling circuit to handle increased voltages in a circuit such as a PA or a quad mixer.

[**0043**] In other embodiments, however, one or more additional FETs of the same polarity are connected in series with M_1 **204** and M_2 **208**. Such additional FETs are represented in **FIG. 2** by an Nth FET, M_N **216**. As for each additional FET of the stack, the source of M_N **216** is coupled to the drain of the preceding FET of the stack, i.e., to the drain of FET M_{N-1} (not shown, though if N=3 then M_{N-1} is M_2 **208**). The drain of the last FET of the stack, M_N **216**, is coupled to the output terminal Vdrive **224**. Associated with each additional FET is a biasing voltage VB_N **218**, which is coupled to the gate of the FET via a bias impedance such as RB_N **220**, and a capacitor CG_N **222** for coupling the gate to a voltage such that the FET is enslaved to conduction by the signal-input FET (here, M_1 **204**). As shown, enslaving may be effected by coupling the gate of each additional FET to $Vdrive_{REF}$ **202**.

[**0044**] FET stacks with at least nine FETs in series have been fabricated or simulated, and stacks of even more series FETs are certainly possible. Note that physical circuit couplings generally include finite capacitance, inductance, and resistance. For many purposes it is preferred that the FETs of the FET stack **200** be coupled with minimal impedance in series, drain to source. However, impedance may be intentionally added to such couplings. For example, it may be desirable to more closely control a drive impedance, and to dissipate heat in specific resistive series coupling elements rather than within the FETs themselves. It may also be desirable to add impedance between the FETs of the FET stack **200** so as to tune the conductance of the drive circuit.

II.A. FET Stack Biasing

[**0045**] In some embodiments, the FETs of a FET stack may all have substantially similar voltage withstand capabilities, such as breakdown voltages $V_{GS(br)}$, $V_{DS(br)}$, and $V_{DG(br)}$. For some integrated circuit fabrication processes, these values will be similar from FET to FET. Moreover, for some integrated circuit fabrication processes, the breakdown voltages $V_{GS(br)}$, $V_{DS(br)}$, and $V_{DG(br)}$ may be approximately equal to each other. Proper biasing will usefully ensure that none of these breakdown voltages is exceeded during normal operation of the circuit. In some embodiments, with proper biasing, voltage excursions between $Vdrive_{REF}$ **202** and Vdrive **224** may be permitted to approach a sum of V_{DS} breakdown voltages for each constituent FET of the stack.

[**0046**] Biasing and coupling the FETs of a FET stack as described below may prevent voltages from exceeding any maximum allowable node to node voltage for any FET of the stack, even when the total voltage impressed from Vdrive **224** to $Vdrive_{REF}$ **202** is nearly equal to the sum of the maximum allowable V_{DS} for the individual FETs of the stack. Unless otherwise noted, the maximum allowable voltage between any two nodes of the FETs (i.e., V_{GS}, V_{DS}, and V_{DG}) are generally assumed to be substantially equal, both for the various nodes of each FET, and from FET to FET, which accords with an exemplary semiconductor fabrication processes. However, the skilled person may readily extend the principles set forth below to encompass situations in which these maximum allowable voltages are not equal. Also, the calculations set forth below for N-channel FET stacks may be applied to P-channel FET stacks with appropriate inversions of polarities and references.

[**0047**] The impedance of the gate drive of M_1 may be selected according to ordinary transistor driving principles. In this exemplary embodiment, V_{DS}(max) is the same for all FETs of the stack. V_{DS} for M_1 will therefore approximate (Vdrive-$Vdrive_{REF}$)/N. For each FET $M_{\cdot X}$", for X values from 2 to N, the effective value of each biasing resistor RB_X is selected to control a time constant, τ_{GX}, of the gate coupling. τ_{GX} is, approximately, the sum of effective capacitances of the gate coupling capacitor CG_X plus the parasitic gate capacitances C_{GPX}, multiplied by the series impedance to a biasing voltage. Such series impedance is typically resistive, and will be designated $RB_{X(equiv)}$. It may be desirable for τ_{GX} to be much longer than the period $1/f_0$ of the center drive frequency, preferably 5-20 times as long. Thus, a good design center goal is:

$$RB_{X(equiv)}(C_{GX}+C_{GPX})=10/f_0 \quad \text{(Eqn. 1).}$$

[**0048**] With respect to $Vdrive_{REF}$, and for Vpeak that is the maximum expected value of Vdrive, one proper bias voltage value is simply a proportional portion of ½ of Vpeak:

$$VB_X=X(V\text{peak})/2N \quad \text{(Eqn. 2)}$$

Thus, an example in which N=4 yields: VB_2=Vpeak/4, VB_3=3(Vpeak)/8, and VB_4=Vpeak/2.

II.B. FET Stack Gate Signal Coupling

[**0049**] In **FIGS. 2 and 7**, each gate node (V_{GX}) is coupled via the capacitor C_{GX} to the reference voltage $Vdrive_{REF}$. Each gate node is also coupled to a DC bias voltage via a bias resistor. In this configuration, the effective drive voltage V_{GSX} for each FET M_X of the FET stack depends upon the voltage excursion of its source, V_{SX}, in conjunction with the impedance from the source to the gate node, and from the gate node to AC ground. These impedances are dominated by the gate-source capacitance and the coupling capacitor CG_X. Appropriate values for CG_X may be determined as follows.

[**0050**] In the exemplary embodiment, the maximum voltage between each node pair of each FET is the same. The voltage excursions of the source of FET M_2 must therefore not exceed the maximum V_{DS} for M_1. As such, the value of CG_2 is unlimited, and desirably large, for effecting AC grounding of the gate of M_2 and thereby providing the largest common-gate drive signal to M_2. V_{GS} (max) will not be exceeded for M2 if the (DC) voltage on the gate is maintained within the range of the source voltage excursions. However, if (contrary to the assumptions above) the maximum V_{DS1} exceeds the maximum V_{GS2}, then CG_2

values may need to be limited in a manner analogous to that described below for CG_X for X from 2 to N.

[0051] The voltage excursion of the source of each FET M_X with respect to $Vdrive_{REF}$, ΔV_{SX}, will be equal to the drain voltage excursion for $M_{(X-1)}$, $\Delta V_{D(X-1)}$. This voltage, presuming equal division between the various FETs, is X(Vpeak−Vmin)/N. For Vmin=0, this is simply X(Vpeak)/N, and ΔV_{SX}=(X−1)(Vpeak)/N.

[0052] The parasitic gate-source capacitance C_{GS} of a FET increases, when $V_{GS}=V_{GS}(on)$, to C_{OX}, the oxide capacitance. C_{OX} for a particular FET M_X is designated C_{OXX}. Because C_{GX} is coupled to the reference voltage $Vdrive_{REF}$, the net V_{GSX} will be capacitively divided between CG_X and C_{OXX}. Thus, the gate-source excursion $\Delta V_{GSX}=(\Delta V_{SX})/(1+C_{OXX}/C_{GSX})$. Presuming equal maximums for V_{GS} and V_{DS}, it is desired to limit $\Delta V_{GSX} \leqq Vpeak/N$. Thus, substituting for ΔV_{GSX} and ΔV_{SX}, $Vpeak/N \geqq [(X-1)(Vpeak)/N]/[1+C_{OXX}/C_{GSX}]$. Appropriate consolidation yields:

$$C_{GX} \leqq C_{OXX}/(X-2) \quad \text{(Eqn. 3)}$$

For X=2, $C_{GX} \leqq$ infinity, as expected. Also as expected, excessive values for C_{GX} will tend to cause excessive gate-source voltage excursions (ΔV_{GSX}). The inequality of Eqn. 3 may prevent excessive voltages between nodes of the devices. However, C_{GX} may desirably be as large as is allowable so as to provide the largest allowable drive levels without exceeding breakdown voltages. Accordingly, the inequality of equation 3 may be treated as an approximate equality.

[0053] The result set forth above may not apply when it is desired to divide voltage differently between different FETs of the stack, or when maximum gate-source voltages differ from maximum drain-source voltages. However, the skilled person will have no difficulty determining desirable values for C_{GX} for such various circumstances by calculations corresponding to those set forth above, with appropriately modified assumptions. Because the capacitors C_{GX} must sustain voltages exceeding the bias voltage of the corresponding FET M_X, a metal-insulator-metal (MIM) capacitor is a good choice. Moreover, the capacitance of both (parasitic) oxide capacitors and MIM capacitors is a direct function of geometry. Certain fabrication variables, such as lithographic variables, therefore tend to have similar effects on both types of capacitances, leaving the ratio of such capacitances relatively immune to such variables.

[0054] **FIG. 3** shows an exemplary matching, coupling and filtering block **300**, which, as shown in **FIG. 1**, may be disposed between the drive output node **106** and the antenna **110**. The matching function transforms the typically 50Ω characteristic impedance of the antenna, Z_{OUT}, to the characteristic impedance of the drive output node **106** (both at the operating frequency f_0) in a manner well known to those of skill in the art. The coupling capacitor C_C **302** blocks DC from the drive output node **106**, and may be selected to have an impedance at f_0 that is less, and desirably much less, than the impedance to chassis ground **112**, or to circuit common **104**, from either side of the capacitor **302**. The matching circuit **300** includes an "A" filter element comprising an inductor L_A **304** and a capacitor C_A **306**, which may be fabricated as part of the integrated circuit. The matching circuit **300** also includes a "B" filter element comprising an inductor L_B **308** and a capacitor C_B **310** to chassis ground **112** (to which the antenna **110** of **FIG. 1** is referenced). The coupling capacitor C_C **302**, as well as the inductor L_B **308** and the capacitor C_B **310** may be fabricated on an integrated circuit with the PA, but some of these devices are typically external to the integrated circuit.

III. Shunt Filtering

[0055] **FIG. 4** illustrates a shunt filter **400** that may be employed in an iClass PA such as illustrated in **FIG. 1**. A node **402** of shunt filter **400** may be connected to the drive output node **106** of **FIG. 1**, and an opposite node **404** may be connected to circuit common **104** of **FIG. 1**. The shunt filter **400** may provide local minimum impedances at each of one or more particular frequencies. The minimum impedances may be matched to the drive circuit impedance (as established, for example, by the drive elements **200** and the RF choke L_S **108**). The shunt filter elements may be fabricated as part of the integrated circuit that includes the drive elements **200**, thus reducing loop areas of currents passing through the elements of the shunt filter **400**.

[0056] A shunt filter **400** for **FIG. 1** may be a "transmission line filter" fabricated of reactive elements that are substantially distributed over an appropriate length, for example ¼ wavelength at f_0. Such a transmission line may be coupled to circuit common via a resonant circuit having a maximum impedance at f_0, such as a filter **600** as illustrated in **FIG. 6** and described in more detail hereinbelow. Such a configuration for the shunt filter **400** provides local impedance minimums (approximately zero) at each even harmonic of f_0, and local maximum impedances at each odd harmonic of f_0. Stated more concisely, such a configuration may typically be said to reflect all odd harmonics, and to short all even harmonics, thus permitting operation as a Class F PA.

[0057] However, the shunt filter **400** illustrated in **FIG. 4** for use in an iClass PA generally differs from such a transmission line filter. First, the shunt filter **400** may employ lumped, rather than distributed, elements. Consequently, local minimum impedances may occur at selected frequencies rather than at all odd, or at all even, harmonics of a resonant frequency (e.g., f_0). Second, the filter may employ series resistive elements to intentionally establish a non-zero value of local minimum impedance. It may be useful, for example, to control the local impedance minimum values so as to match an impedance of the drive circuit at the corresponding frequency (or, alternatively, at f_0). As a result of such differences between the circuit illustrated in **FIG. 4** and a conventional transmission line filter, the magnitudes of currents in current loops may be reduced. Moreover, drive element power dissipation may be reduced at the frequencies corresponding to the selected minimum impedances.

[0058] In **FIG. 4**, a first shunt filter element includes L_{SF1} **406**, R_{SF1} **408**, and C_{SF1} **410**. These components establish a local minimum impedance at a particular frequency, with the impedance increasing for both higher and lower frequencies. A switch S**1412**, in conjunction with an additional capacitor C_{SF3} **414**, represents an optional circuit for adjusting the frequency of the minimum impedance of the first filter element. As shown, the effective value of the series capacitor of the first filter element is increased when S**1** is closed and C_{SF3} is disposed in parallel with C_{SF1} **410**.

[0059] Of course, such frequency adjustability may be effected in numerous different manners. For example, S**1412**

may be a FET for electronically switching the frequency. Additionally or alternatively, C_{SF1} **410**, as well as optional C_{SF3} **414**, may be varactors (with the corresponding addition of an appropriate control circuit for the DC voltages on such varactors). Moreover, the capacitor C_{SF3} **414** may be disposed in series connection, rather than parallel connection, with C_{SF1} **410**, in which event the switch **S1** may be configured to bypass the capacitor C_{SF3} **414**. Yet further, analogous techniques may be employed to vary inductance, rather than capacitance. For example, the switch **S1412** may selectably bypass a second inductive element, so as to vary the effective inductance of the first shunt filter element.

[**0060**] The second shunt filter element comprises an inductor L_{SF2} **416**, a resistive element R_{SF2} **418**, and a capacitor C_{SF2} **420**. The resonant frequency of the second filter element (or, indeed, of any further filter element) of the shunt filter **400** may be varied by similar techniques as outlined above with respect to the first filter element. It may be useful to have a minimum impedance that is substantially resistive, and/or that is non-zero. In one embodiment, the first and second filter elements are designed to provide local minimum impedances, at a second harmonic and a third harmonic of the operating frequency f_0 respectively, which are approximately equal to the drive circuit impedance. Though only two filter elements are illustrated, additional harmonics may desirably be treated with additional filter elements (not shown).

[**0061**] **FIG. 11** is a schematic diagram of a circuit alternative for shunt filter **400** together with matching and coupling circuit **300**. Zdrive and Z_{OUT} of **FIG. 11** are connected as shown in **FIG. 1**. C_C **302** is substantially the same as in **FIG. 3**, providing DC isolation of the PA from the antenna output. The shunt filter includes a parallel resonant circuit primarily consisting of C_{SF} **980** and L_{SF} **982**, which together function as a tank circuit that is resonant at f_0. All integer harmonic frequencies of f_0 are coupled through Rdrive **984**, which is preferably selected to be approximately equal to the characteristic drive impedance of the PA switching circuit. Thereby, all harmonic frequencies of f_0 are terminated at the drive impedance. In some embodiments, alternative filtering, such as two parallel tank circuits each resonant near f_0, may be disposed in series above Rdrive **984**. Dual tank circuits may be configured either to resonate at substantially identical frequencies, thereby increasing the impedance at f_0 and reducing power loss at f_0, or to resonate at slightly different frequencies, thereby broadening the range of frequencies at which the circuit has high impedance to ease manufacturing tolerances. Following the shunt filter, a matching and filtering network **990** may be as illustrated in **FIG. 3**, except for two differences: first, coupling capacitor C_C **302** is omitted, and second, C_A **306**, being on the antenna side of coupling capacitor C_C **302**, is coupled to earth ground **112** rather than circuit common **104**. The two common references may be made effectively identical in some integrated circuit layouts.

IV. PA Output Power Control

[**0062**] **FIG. 5** illustrates elements of one possible shunt power control circuit **500** for the PA of **FIG. 1**. A power control input **502** may establish a bias with respect to chassis ground **112**. An inductive impedance Lg**1504** (which may reflect, for example, the inductance of a bond wire) is illustrated between chassis ground and the source of a power control FET M_{PC} **506**. A connection **508** may be coupled to circuit common **104** in **FIG. 1**. An inductance Lg**2510** typically exists in series with a bypass capacitor for the power control circuit, C_{PC} **512**. Assuming that the DC voltage V_{DD} is with respect to chassis ground **112**, the substantially DC voltage established across C_{PC} **512** will reduce the effective supply voltage with respect to circuit common **104**.

[**0063**] Other techniques may also be used to control the output power for a circuit as shown in **FIG. 1**, particularly when operated in a Class F configuration (rectangular wave input control). Such other techniques may be used either in addition to, or instead of, shunt power control as described above with respect to **FIG. 5**.

[**0064**] As a first example, referring also to **FIG. 2**, the bias voltages on the FETs M_2 **208** . . . M_N **216** may be adjusted. Efficiency will decrease, but power output will decrease more rapidly. As noted above, bias may generally be set such that VB_X=X(Vpeak)/2N. However, if VB**2** is decreased well below the calculated value, the output voltage Vdrive (in iClass operation with harmonic termination) will also decline. Thus, for example, a circuit may be configured as shown in **FIG. 7**, except that the effective average voltage at the gate of M_2 **208** may be controllably reduced. This may be accomplished by making the value of RB_1 **708** variable (e.g., by means of a parallel FET). Alternatively, the value of RB_1 **708** may be reduced, and RB_1 **708** may be coupled to a variable voltage source rather than to reference **202**. Reducing the bias voltage will cause corresponding reductions in drive output voltages. As described below in more detail, the self adjusting bias supply circuit of **FIG. 7** will permit the bias on RB_N to gradually follow the reductions in Vdrive(peak) that are caused by varying the bias voltage on the gate of M_2.

[**0065**] PA output power may also be controlled by varying the amplitude of the drive signal. The conduction impedance of the drive elements will be higher when driven with a lower amplitude rectangular wave, resulting in a smaller effective drive voltage. The efficiency of this technique is typically comparable to the efficiency of varying bias voltages.

[**0066**] As discussed below with respect to **FIGS. 12 and 14**, a series regulator circuit may be used to control PA output power either alone, or in conjunction with one or more other power control techniques.

V. ALTERNATIVE PA EMBODIMENTS

[**0067**] **FIG. 6** is a simplified schematic diagram of a filter circuit **600** that may be employed in a manner similar to the shunt filter **400** in **FIG. 1** to form a versatile PA architecture. The drive output node **106** of **FIG. 1** may be coupled to a Zdrive node as an input to **600**. The Zdrive node may be coupled via a ¼ wavelength transmission line **602** and a coupling capacitor C_C, **612** to an output filter section. The output filter section may comprise a parallel combination of L_{OF1} **610** and C_{OF1} **608**, resonant at the operating frequency f_0. Unlike some embodiments of shunt filters **400**, the output filter section of **FIG. 6** is typically not part of the PA integrated circuit, and thus is referenced to chassis ground **112** rather than to circuit common. The impedance of this bandpass filter to ground **112** falls rapidly as the frequency deviates from f_0, and, therefore, the harmonics of the oper-

ating frequency are effectively shorted to ground at the output filter end of the transmission line **602**. The standing waves of the properly tuned ¼ wavelength transmission line therefore provide a high impedance at each odd harmonic, and a low impedance at each even harmonic, as seen at the Zdrive node. A Z_{OUT} node **604** may be coupled to a further output filter section **116-118**, an RF switch **120**, and antenna **110** as shown in **FIG. 1**. A matching network (not shown) may also be required, similar to that illustrated in **FIG. 3** with the coupling capacitor C_C **302** omitted. Such further filtering and matching circuits, or a transmission line coupled thereto, will ideally appear to the filter circuit **600** as a resistive impedance $R_{OUTequiv}$ **606** at the operating frequency f_0.

[**0068**] Modified as described above, the circuit of **FIG. 1** may be operated as an RF PA of Class A, Class B, Class C, Class E or Class F. For Class A operation, the input signal **102** is sinusoidal and does not cause the current through M_1 **202** of **FIG. 2** to go to zero. For Class B operation, the input signal **102** is sinusoidal but M_1 **202** conducts only 50% of the time (conduction angle 180 degrees). Operation may be Class C, with a conduction angle less than 180 degrees, which yields some efficiency improvement as compared to the Class B operation. In each case the FETs M_2 to M_N are enslaved to M_1, and the FET stack of **FIG. 2** functions substantially as a single device. The circuit of **FIG. 1** may also be operated as an iClass PA in a configuration related to Class F but having dissipative termination for harmonics of the operating frequency.

[**0069**] The circuit of **FIG. 1**, configured as described immediately above, may also be operated as a Class F RF PA. For Class F operation the input signal is preferably a square wave having a duty cycle that causes the circuit **200** to conduct at precisely a 50% duty cycle. The output voltages resulting from Class F operation generally increase substantially when the conduction duty cycle deviates from 50%. Unfortunately, ordinary manufacturing component variations tend to cause the duty cycle to deviate from 50%, and consequently the circuit may not readily be able to safely and reliably utilize the full voltage withstand capability of the drive element(s).

VI. Alternative Bias and Slaving

[**0070**] Embodiments of a FET stack, as described herein, may include a signal-input FET that receives a drive signal coupled to its gate with respect to a reference voltage that is coupled to its source. The remaining FETs of the stack may be enslaved to the signal-input FET, such that they conduct under the control of conduction in the signal-input FET. The method by which the other FETs of a FET stack are enslaved to the signal-input FET must cooperate with the method employed to properly bias the FETs. Accordingly, enslavement and biasing are addressed together.

[**0071**] In RF PAs generally according to **FIG. 1**, the peak voltage of drive output node **106** (with respect to circuit common **104**) will often exceed twice the available supply voltage V_{DD} **114**. As such, bias voltages as required for the driver elements of **FIG. 2** may not be readily available. This lack may be remedied by recourse, for example, to a charge pump. A charge pump that is preferred from the standpoint of minimal noise generation is described in commonly owned and copending U.S. patent application Ser. No. 10/658,154, "Low-Noise Charge Pump Method and Apparatus," which is hereby incorporated in its entirety by reference. As described therein in detail, a low-current voltage source may be readily established at any desired voltage. Such voltage source may be provided, as needed, to any of the bias voltage inputs VB_2 **210** to VB_N **218** in **FIG. 2**.

[**0072**] **FIG. 7** illustrates a self-adjusting bias supply that may be employed to bias the FETs of a FET stack. As in **FIG. 2**, a signal input **206** is coupled to the gate of a signal-input FET M_1 **204**. The source of the FET M_1 **204** is coupled to Vd_{REF} **202**, while its drain is coupled in series with each subsequent FET of the stack, including M_2 **208** . . . M_N **216**. The drain of the last FET of the stack, M_N **216**, is coupled to Vdrive **224**. To provide a bias voltage that reflects Vdrive **224**, a diode (or equivalent) D_B **702** charges a bias supply capacitor C_B **704** to Vbias **706**. Vbias will charge to approximately Vpeak, the peak value of Vdrive **224** with respect to Vd_{REF} **202**. If a time constant associated with C_B **704** is sufficiently long, then Vbias will remain substantially at this value. The time constant is the product of the capacitance of C_B **704** multiplied by the resistance, to Vd_{REF} **202**, of the resistive voltage divider having N resistors including RB_1 **708**, RB_2 **710**, . . . , and RB_N **712**. The total resistance of this voltage divider may be designated $R_B$sum.

[**0073**] With respect to Equations 1, 2 and 3 that are set forth above, "X" represents the position of the particular FET in a stack, and N represents the total number of FETs in such stack. Assuming that all FETs are approximately identical, it may be seen that:

$$RB_1=RB_2=\ldots=RB_{(N-1)} \quad \text{(Eqn. 4), and, accordingly,}$$

$$RB_N=(N-1)RB_1 \quad \text{(Eqn. 5).}$$

[**0074**] In view of equations 1-5, it may be seen that, for the last FET of the stack (X=N),

$$(C_{GX}+C_{OXX})=C_{OX}(N-1)/(N-2) \quad \text{(Eqn. 6),}$$

$$RB_{X(equiv)}=RB_1(N-1)/2 \quad \text{(Eqn. 7), and}$$

$$RB_1 \geqq 20(N-2)/[C_{OX}(N-1)^2 f_0] \quad \text{(Eqn. 8).}$$

Thus, for N=3, $RB_1 \geqq 5/C_{OX}/f_o$, and RB_1 declines monotonically as N increases (for given values of C_{OX} & f_0).

[**0075**] The total resistance $R_B$sum of the resistive divider described above, in which the lower (N−1) resistors are RB_1 and the top (or Nth) resistor is the sum of the lower resistors, is simply $2(N-1)RB_1$. The ripple on Vbias **706** may be acceptably low if the time constant $C_B(R_B\text{sum}) \geqq 10/f_0$. Coupling that criteria with Eqn. 8 yields

$$C_B \geqq C_{OX}(N-1)/(N-2)/4 \quad \text{(Eqn. 9).}$$

Thus, for N=3, $C_B \geqq C_{OX}/2$. As N increases, smaller values of C_B (with respect to Cox) will be required to achieve the same ripple voltage.

[**0076**] A significant ripple voltage is not necessarily a problem, and CB may desirably assume even smaller values if rapid self-adjustment response is required. Indeed, in view of the filtering effected by each gate bypass capacitor CG_X in conjunction with $RB_{X(equiv)}$, an average value is the main consideration for Vbias. However, if the average value of Vbias is permitted to decline significantly below Vpeak for any reason, including the presence of substantial ripple on C_B, the skilled person will understand that the resistive divider values should be adjusted accordingly.

[0077] **FIG. 8** illustrates an alternative for providing both bias and gate coupling for FETs M_3 and above ($X \geqq 3$). A reference **802** is coupled to the source of a signal-input FET M_1 **804**, the gate of which is coupled to an input signal **806**. The drain of M_1 **804** is coupled to the source of a second FET M_2 **808**. A bias voltage is applied to a bias input **810**, which is coupled via a bias resistance RB **812** to the gate of M_2 **808**, and to a relatively large capacitance CG_2 **814**. The drain of M_2 **808** is coupled to the source of a third FET of the stack, M_3 **816**. The drain of M_3 **816** may be coupled to a further FET stage, if present. However, the drain of the FET of the last stage, M_3 **816** as shown in **FIG. 8**, is coupled to an output node Vdrive **818**.

[0078] The gate **820** of FET M_3 **816** may be coupled to the base of the preceding stage FET M_2 **808** via a zener diode DZ **822**. DZ **822** may have a conduction threshold knee at approximately the maximum desired value for V_{DS} of M_3 **816**. (A circuit operating similarly to a zener diode may be used instead of DZ **822**.) Additional FET stages designated by subscripts "Y" may be added. For such additional stages, corresponding additional zener diodes may be employed in like manner as DZ **822**, i.e., anode to the gate of additional FET M_Y, and cathode to the gate of $M_{(Y-1)}$.

VI.A. Alternative Stacked FET Switch Configurations and Extensions

[0079] The FET stacks described above with respect to **FIGS. 1-8** employ N-channel FETs (N-FETs). P-channel FET (P-FET) stacks may be fabricated analogously, by reversing the polarity of each voltage and polarized component associated with the stack. The P-FET stack reference voltage will generally be coupled to the source of a first, signal-input FET M_{P1}. Such inverted circuits will operate according to substantially the same principles as the N-FET stack circuits described above. For example, Vdrive **818** may be negative with respect to reference **802** in **FIG. 8** if all FETs are P-channel, and the zener DZ **822** connection is reversed (anode and cathode exchanged).

[0080] **FIG. 9** is an exemplary circuit that employs both an N-channel FET stack comprising N-channel FETs M_{N1} **902**, M_{N2} **904** and M_{N3} **906**, plus a P-channel FET stack comprising P-channel FETs M_{P1} **908**, M_{P2} **910** and M_{P3} **912**. For Class D operation, an input square wave may be provided with respect to common **914** at the input **916** to the N-FET stack, and coupled to an input for the P-FET stack on the gate of M_{P3} **912** via a capacitor C_{GP1} **918**. A bias voltage, set for example to one half of V_{GS}(on) below the P-FET stack reference V_{DD} **930**, may be provided for M_{P1} **908** via a bias resistor R_{BP1} **920**. Alternatively, the capacitor C_{GP1} **918** and the bias resistor R_{BP1} **920** may be deleted, and the input **916** and the gate of M_{P1} **908** may each be driven, instead, by means of an appropriate non-overlap clock generator (not shown).

[0081] Control of the N-FETs M_{N2} **904** and M_{N3} **906** is substantially as described with respect to **FIG. 2** (for N=3). The gate of M_{N2} **904** is coupled to common (i.e., decoupled) via a capacitor C_{GN2} **922** having a relatively large value, and may be biased to about ($V_{DD}/3$) volts via a bias resistor R_{BN2} **924**. The gate of M_{N3} **906** is decoupled to common via a capacitor C_{GN3} **926** having a value calculated as described with respect to **FIG. 2**, and may be biased to ($V_{DD}/2$) volts via a bias resistor R_{BN3} **928**.

[0082] The P-FET stack is controlled analogously as the N-FET stack. The polarities of the bias voltages are inverted, and referenced to the "reference voltage" of the P-FET stack, which in this case is V_{DD} **930**. For purposes of capacitively decoupling the P-FET gates, the fact that the P-FET reference voltage is V_{DD} **930** is likely to make little difference, because V_{DD} is typically closely coupled to the circuit common **914** that is the reference for the N-FETs. Therefore, decoupling capacitors **932** and **936** may alternatively be connected to circuit common **914**. As shown, however, the gate of M_{P2} **910** is decoupled to V_{DD} via a relatively large capacitor C_{GP2} **932**, and biased to about $\frac{2}{3}$ V_{DD} via a bias resistor R_{BP2} **934**. The gate of M_{P3} **912** is decoupled to V_{DD} via a capacitor C_{GP3} **936**. The value of C_{GP3} **936** may be calculated as described with respect to **FIG. 2** for X=3 and N=3. The gate of M_{P3} **912** is biased to about $V_{DD}/2$ via a bias resistor R_{BP3} **938**.

[0083] An output voltage Vdrive **940** will be driven between common and V_{DD}, according to whether the N-FET stack is conducting or the P-FET stack is conducting. The output Vdrive **940** may be shunt filtered by a shunt filter **950**, and may be processed by a matching and coupling circuit **960**, as described below in more detail with respect to **FIG. 10**. From the matching and coupling circuit **960** the signal may proceed to an antenna **942**, typically via a transmission line, one or more further filter sections, and an RF switch (not shown).

[0084] The shunt filter **950** of **FIG. 9** may be similar to that shown in **FIG. 4**, or that shown in **FIG. 6**. The matching and coupling circuit **960** of **FIG. 9** may, for example, be similar to that shown in **FIG. 3**. However, **FIG. 10** illustrates filtering that may be employed for both blocks **950** and **960** in the circuit of **FIG. 9**. The capacitor C_S **952** may serve as the shunt filter **950**. The remainder of **FIG. 10** may function as the matching and coupling circuit **960** of **FIG. 9**. An inductor L_C **954** may comprise a physical coupling connection. A coupling capacitor C_C **962** serves to block DC. L_A **964**, C_A **966**, L_B **968** and C_B **970** may be configured for matching to the output impedance Z_{OUT}, which is typically 50 ohms.

VII. Monolithically Integrated, Medium Power Dual-Band RF Transceiver

[0085] An RF transceiver, such as the dual-band RF transceiver represented in **FIG. 12**, typically includes a received-signal amplifier such as items **1226** or **1256** of **FIG. 12**. Such a received-signal amplifier is typically a low noise amplifier (LNA), and is employed to condition signals received from the antenna. An RF front end may be considered to be an RF transceiver circuit that does not necessarily include an LNA.

[0086] In most RF transceivers, discrete integrated circuits must be combined in a module to fabricate a complete RF front-end section. Typically, at least the antenna switch will be fabricated on a different, separate integrated circuit (IC) from the PA, and often many more discrete integrated circuits must be connected via off-chip wiring to fabricate an RF front end module. Each such discrete integrated circuit must be defined by particular performance requirements which ensure that the module functions properly even when the discrete integrated circuits which it comprises are from different lots, or have been designed and manufactured differently from other integrated circuits that perform the same tasks. Such performance requirements, which are thus

developed to achieve mix-and-match flexibility and reliability, may well exact a cost for the discrete ICs that are combined in these devices.

[0087] PAs in multiple-IC transceiver modules typically produce a signal of substantial power on demand. An antenna switch unit couples an antenna (more precisely, an antenna connection) to either a transmit signal matched to the expected antenna impedance (e.g., 50 ohms), or to a receive signal input. However, damage to the antenna connection or the antenna may cause the impedance reflected to the antenna connection point from the antenna connecting line to vary drastically from its expected value. In such event, a large voltage standing wave (VSW) may be caused by the resulting mismatch between that reflected impedance, and the expected value to which the transmit signal has been matched. Voltage excursions much larger than those expected during normal operation may be generated as a consequence of such mismatch-induced VSWs. Voltage withstand requirements for antenna switches are typically set much higher than normal peak operating voltages to avoid damage under such mismatch conditions.

[0088] The IC area occupied by switching devices (such as FETs) in a power-switching circuit, such as an antenna switch, may increase as the square of the voltage they are capable of withstanding. Thus, halving the required withstand voltage may reduce the switch device area to one fourth. Moreover, because these devices dominate the IC area used by an antenna switching circuit, a very substantial saving in IC area (and thus in manufacturing cost) may be realized by reducing their required withstand voltage. Such reduction may not be practical when discrete ICs must be coupled to fabricate an entire transceiver. However, a single IC that includes all devices from a PA, through an antenna switch, and to an antenna connection, may take advantage of reliable internal coupling and close device matching to protect against high mismatch-induced VSWs. Due to these advantages of integration, substantial savings in device area can be realized as compared to combining discrete ICs to fabricate a comparably-performing transceiver.

[0089] **FIG. 12** is a simplified block schematic diagram of the primary RF sections of a dual-band transceiver that is configured to benefit from such internal protection. A low-level signal at a first operating frequency f_{O1} is coupled to an input node **1202** from a source which may (but need not) be on the same IC chip. The signal is amplified through any suitable amplifier, as indicated by amplifier **1204**. The signal produced by the amplifier **1204** may deviate considerably from a preferred rectangular shape if a pulse adjustment circuit **1500** is provided to improve rectangularity, and preferably to also adjust the duty cycle, of the waveform that is ultimately coupled into a power amplifier (PA) **1206**.

[0090] The output of the pulse adjustment circuit **1500** is the input to the PA **1206**, which draws power from a supply V_{DD} **114** via supply conditioning elements, including a series regulator **1400** and an RF choke (RFC) L_S **108**, to generate a PA output signal. The PA output signal has a characteristic impedance resulting from the input signal, the PA circuit elements, and the supply conditioning elements, and generally differs from the impedance expected at the antenna node **1214**. A coupling, matching and filtering network may be needed, for example as represented by a block **1210**. Such a network may couple the PA output signal to the antenna switch while blocking DC current, and may transform the PA output impedance to the desired antenna node impedance (e.g., 50 ohms). It may also filter undesirable signal components, such as harmonics of f_{O1}, from the PA output signal before coupling it to an "A" input of an antenna switch **1700**. If separate grounds are maintained as a matter of design preference, then the output of the coupling, matching and filtering block **1210** may be referenced to a ground reference **112**, which may be distinguishable from a circuit common reference **104** used elsewhere in the circuit. The antenna switch **1700** selectably couples the signal to the antenna node **1214**, from whence it may be coupled, for example by transmission line, to an antenna that may be separated from the IC chip.

[0091] Availability of the antenna connection of the antenna switch on the same IC chip as the PA (and all intervening circuitry) provides an opportunity to reliably limit the maximum electrical stress that must be endured by the antenna switch circuitry, by the PA, or by coupling, matching or filtering elements. An output sensor **1600** may be coupled to the antenna node **1214**, sensing the electrical stress and providing a signal that will cause the PA to reduce its output if the electrical stresses are excessive. To this end, the output **1220** of output sensor **1600** is coupled to an input "B" of a PA control block **1300**. An "A" input **1224** to the PA control block **1300** may receive an amplitude control signal to adjust the envelope amplitude of the PA output signal. This input may also be used to restrict, or even to terminate, output from the PA. Both the "A" and "B" inputs may affect an output "D" that is coupled from the PA control block **1300** to the series regulator block **1400**. A "C" input **1222** to the PA control block **1300** may be provided with information, or a signal, that controls an "E" output from the block **1300**. The "E" output may be coupled to the pulse adjustment circuit **1500** to control the duty cycle of the rectangular wave that is input to the PA **1206**. Duty cycle control may, for example, provide another means to reduce the power level of the PA output signal. The signal path from **1202** may be tuned for a first band of operating frequencies, which include f_{O1}.

[0092] The antenna switch **1700** may selectably decouple the antenna node **1214** from the first-band transmit signal on input "A," and couple the antenna node instead to output "B" so as to deliver a signal received from the antenna to a receive preamplifier **1226** for a first receive band. The receive preamplifier **1226** (as well as **1256**) is preferably a low noise amplifier (LNA). LNAs are not necessarily included in integrated front ends as described herein, though they typically are included in complete transceiver circuits. The output from receive preamplifier **1226**, if present, may be delivered to further first receive band circuitry either on or off the same IC chip. The antenna switch **1700** may similarly selectably couple the antenna node **1214** to a second receive band preamplifier **1256** to amplify a signal from the antenna to a second receive band output node **1258**. That output may be delivered to further second receive band circuitry either on or off the IC chip.

[0093] Similarly as described above with respect to the first transmit band circuitry, a transmit signal at a second operating frequency f_{O2} in a second operating frequency band may be provided to an input **1232**, and amplified by an amplifier **1234**. The duty cycle and waveform of the signal output from the amplifier **1234** may be conditioned by a

pulse adjustment **1501** under control of a PA control block **1301**, and then delivered as an input to a second band PA **1207**. The second band PA **1207** will generate a second-band PA output signal using power that is provided from V_{DD} **114**, as limited by a series regulator **1401** under control of the PA control block **1301**, via an RF choke **109**. The second-band PA output will have a characteristic impedance, and will be coupled to the "D" input of the antenna switch **1700** via a block **1211** that couples the signal, matches the PA output and antenna node impedances, and filters the output signal. The antenna switch **1700** may be controlled to couple the "D" input to the antenna node **1214**, from whence the signal will be delivered to the antenna **1216**. The output **1220** of the output sensor **1600** may be coupled also to a "B" input to the second-band PA control block **1301**, whereby excess output voltage will cause the second-band PA output signal to be reduced to safe levels. The second-band PA control block **1301** may also accept an envelope-control signal at an "A" input **1254**, as well as a duty-cycle control signal at a "C" input **1252**.

[**0094**] Though not shown, control circuitry is preferably enabled only when the associated PA is active. Exemplary circuitry for a PA control block, such as **1300** or **1301**, is shown in **FIG. 13**. Exemplary circuitry for a series regulator, such as **1400** or **1401**, is shown in **FIG. 14**. Exemplary circuitry for a pulse adjustment circuit, such as **1500** or **1501**, is shown in **FIG. 15**. The PAs **1206** or **1207** may be fabricated as described for Driver Elements **200** of **FIG. 1**, together with a shunt filter, such as block **400** of **FIG. 1** or the appropriate elements of **FIG. 11**. Coupling, matching and filtering circuits **1210** and **1211** may be fabricated as described above for **FIG. 3**, or **FIG. 10**, or in any other manner to obtain similar coupling, matching and filtering effects. Note that if a circuit as shown in **FIG. 11** is to be employed, the coupling capacitor **302** will be disposed before the shunt filter, and the matching and filtering will be provided subsequently, as in block **990**.

[**0095**] **FIG. 13** illustrates exemplary circuitry for a PA control block **1300**. An enable input "A"**1302** may be coupled directly to a FET **1304**, such that if input **1302** is approximately ground potential, an output "D"**1306** can draw no current. Conduction into the output "D"**1306** may control the PA output power via a series regulator, such as shown in **FIG. 14**, such that when output **1306** conducts no current, no current will be provided to the PA, reducing output power to zero as discussed below with respect to **FIG. 14**. FET **1308** is biased by resistors **1310** and **1312**, which may have equal values, a nominal value such as 30-50 kΩ being selected for engineering convenience. This configuration protects low-voltage FETs, ensuring that V_{GD}, V_{GS}, and V_{DS} for all of FETs **1304**, **1308** and **1314** do not significantly exceed $V_{DD}/2$.

[**0096**] A power sense input "B"**1316** may be coupled to resistor **1318**. Resistor **1318** may be about 30-50 kΩ, and reasonably equal to a resistor **1320** to establish unity gain for op amp **1322**. A power set input "C"**1324** may be set, in one embodiment, from 0V to 2*Vth (FET threshold voltage), where Vth may be 0.4 to 0.7V, nominally about 0.5V, and is consistent within the circuit. The noninverting input of op amp **1322** is prevented from exceeding this voltage range by means of a resistor **1326** (e.g., 30-50 kΩ) together with diode-connected FETs **1328** and **1330**, thus limiting the maximum power that may be selected. The skilled person may adjust circuit values, and circuit design, so as to achieve a selectable output power up to a fixed circuit design maximum. In particular, one or both diode-connected FETs **1328** and **1330** may be replaced by a network that includes a bandgap reference, for example to increase accuracy of power settings and output voltage limits. Many other techniques may be employed to achieve similar effects. When power sense input "B"**1316** exceeds a value established by the power set input voltage, FET **1314** will cease conducting, precluding conduction into output "D"**1306**.

[**0097**] The PA control block **1300** also provides an output "E"**1512** to control the duty cycle adjustment effected by the pulse adjustment circuit **1500** of **FIG. 12**. A reference voltage, which may be adjustable according to factors such as fabrication process parameters, is provided at an input **1332**. This voltage is doubled by an op amp **1334** under control of equal-valued resistors **1316** and **1318**. Of course, in other embodiments the gain of circuitry such as shown in **FIG. 13** will likely be different, and resistors setting such gains, for example **1316** and **1318**, will accordingly differ in value. By reducing the duty cycle somewhat, the PA output power may be correspondingly reduced, and by reducing it to zero the PA output may be suppressed entirely. A reference voltage provided to an input **1322** of an amplifier **1320**, the gain of which may be controlled in the usual manner by resistors **1324** and **1326**, may serve to establish the voltage at output "E"**1512** to control duty cycle of the output of block **1500**.

[**0098**] **FIG. 14** illustrates an exemplary series regulator circuit **1400** for limiting the effective voltage provided to the PA, and thus limiting the PA output amplitude. The voltage provided to input **1306**, as compared to V_{DD}, is divided via resistors **1406** and **1404** to control a P-channel FET **1402** and also protect FET **1402** from excessive voltage between any two nodes. A P-channel FET **1408** is biased by resistors **1410** and **1412** so as to divide maximum voltages that are generated between V_{DD} and an output **1414**, somewhat equally between FETs **1402** and **1408**. The output **1414** provides power to the PA via an RF choke. The FETs **1402** and **1408** may, for example, have V_{GS} threshold voltages of between −0.4V and −0.7V. Resistors **1404**, **1406**, **1410** and **1412** may all be substantially equal, with a magnitude selected for engineering convenience to be, for example, 30-50 kΩ. These exemplary values and relative values may be varied for engineering convenience.

[**0099**] **FIG. 15** is a schematic representation of an exemplary signal conditioning circuit **1500**. An input signal may be provided on an input node **1502**, and coupled via a diode-connected FET **1504** to the input of an inverter **1506**. When the input signal voltage, plus the V_{DS} threshold of FET **1504**, is less than the threshold of the inverter **1506**, the output of inverter **1508** will be low. However, when the voltage of the input signal rises above this value, the FET **1504** will cease conducting. Thereafter, even if the voltage of input **1502** is quite high (e.g., V_{DD}), current from the input will be limited by P-channel FET **1510** under control of an input voltage **1512**. Such current through the FET **1510** must charge a capacitor **1514** (which may be a metal-insulator-metal or "MIM" capacitor of about 0.25 to 0.05 pF) until the input to inverter **1506** rises above its switching threshold. At that point the inverters **1506** and **1508** will change state rapidly due to positive feedback via the capacitor **1514**, providing square edges at an output node **1516**, rise

and fall times being limited primarily by delays through the inverters **1506** and **1508**. If the signal at the input **1502** is a roughly rectangular wave of about 50% duty cycle, as in a preferred embodiment, the voltage at the control input **1512** may be adjusted such that the output duty cycle is reduced from 50% to an arbitrarily lower value that may reach zero. The input signal may be configured to have a duty cycle exceeding 50% if a wider range of output duty cycle is desired.

[0100] **FIG. 16** is a schematic of exemplary circuitry **1600** for sensing peak voltage at a sense node **1602**, which may for example be connected directly to antenna node **1214** of **FIG. 12**. An input divider may be used as shown to sense relatively high voltages. Four roughly equal resistors **1604**, **1606**, **1608** and **1610** having a relatively low resistance, such as 1 kΩ, may be used. Diode-connected FET **1612** conducts when this voltage is high, providing current through a resistor **1614** of about 24 kΩ to a capacitor **1616** of about 1 pF. Many other values may be used, so long as the time constant established by resistor **1614** and capacitor **1616** is much smaller than the duration of any event that could cause the output voltage to rise (for a given level of PA output signal). For example, an antenna mechanical event that caused the antenna impedance to vary drastically from the design value, thereby causing a high voltage standing wave to appear, will take at least milliseconds to occur. The time constant of approximately 24 nS of the exemplary circuit **1600** is well below such an event duration. However, the corner frequency due to these components should generally be well below both the first and second band operating frequencies f_{O1} and f_{O2}, in order to avoid circuit oscillations. If event durations may approach $1/f_O$, then other common circuit design considerations may require a more complicated circuit to avoid oscillation while ensuring that the response is sufficiently fast to prevent excessive voltages.

[0101] **FIG. 17** is a simplified schematic of exemplary circuitry **1700** for an antenna switch. Further details regarding design and fabrication of such an RF switch may be found in U.S. Pat. No. 6,804,502, issued Oct. 12, 2004 and entitled "Switch Circuit and Method of Switching Radio Frequency Signals." Circuitry to provide control signals is not shown. Moreover, the control voltages should preferably be either "high," nearly V_{DD}, or "low" at nearly $-V_{DD}$. To generate $-V_{DD}$ control voltages, a negative voltage generator will be helpful, preferably a low-noise circuit such as described in copending, published U.S. patent application Ser. No. 10/658,154, filed Sep. 8, 2003 and entitled "Low Noise Charge Pump Method and Apparatus." Such a low-noise charge pump is important for avoiding unintended emissions from the antenna.

[0102] A port node **1780** is the common connection of the switch **1700**. In **FIG. 12**, the common connection of the switch **1700** is coupled to the antenna node **1214**. The common connection is generally coupled to only one RF port (port A **1710**, port B **1730**, port C **1750**, or port D **1770**) at a time. Each RF port has a corresponding "+" control node and a corresponding "−" control node. For ports A, B, C and D, the "+" control nodes are nodes **1708**, **1728**, **1748** and **1768**, respectively, while the "−" control nodes are nodes **1718**, **1738**, **1758** and **1778**, respectively.

[0103] To couple an RF port to the common connection, a "high" voltage ($\sim V_{DD}$) is applied to the port's corresponding "+" control node, while a "low" voltage ($\sim -V_{DD}$) is applied to the port's corresponding "−" control node. Meanwhile, a "low" voltage is applied to each "+" control node corresponding to another RF port, and a "high" voltage is applied to each "−" control node corresponding to another RF port. Thereby, a selected RF port will be coupled to the common connection, while every other RF port will be coupled to ground. Thus, to couple RF port A **1710** to common connection **1780**, a "high" voltage is applied to control nodes **1708**, **1738**, **1758**, and **1778**, while a "low" voltage is applied to all other control nodes (**1718**, **1728**, **1748** and **1768**).

[0104] Every resistor will typically have the same value. In some embodiments, the value will be roughly 30-50 kΩ. The resistor is selected such that the time constant of the parasitic gate capacitance of a FET (e.g. $M1_A$ **1701**), in conjunction with the value of its corresponding gate resistor (e.g. **1704**) is much greater than $1/f_O$, where f_O is the lowest significant frequency of the RF signal being controlled. The illustrated configuration serves to divide the voltage appearing across FET stacks (such as the stack consisting of FETs $M1_A$, **1701**, $M1_B$ **1702** and $M1_C$ **1703**, the stack consisting of FETs $M2_A$, **1704**, $M2_B$ **1705** and $M2_C$ **1706**, and so on) uniformly, reducing compression effects. The FET stacks (such as FETs **1701**, **1702** and **1703**) that provide the switching functions may include more or less than the three devices that are shown for illustration; stacks of at least nine devices have been successfully fabricated. Due to the voltage stress distribution uniformity, a wide range of signal voltages and fabrication process parameters may be accommodated.

Integrated Circuit Fabrication and Design

[0105] Integrated circuit fabrication details are not provided in the above description. In some preferred embodiments, including some which have output powers in excess of 1 W at around 2.4 GHz, the integrated circuits may be fabricated in accordance with ultrathin silicon on sapphire processing as described in U.S. Pat. No. 5,663,570, issued Sep. 2, 1997 and entitled "High-Frequency Wireless Communication System on a Single Ultrathin Silicon On Sapphire Chip." Other semiconductor-on-insulator (SOI) techniques may be used to fabricate a dual-band transceiver integrated circuit as described above, for at least some frequency bands and power levels.

[0106] The preferred integrated circuit fabrication techniques described above readily produce FETs having a rather low maximum V_{DS}. Accordingly, various techniques are described for stacking FETs to achieve control of higher voltages while maintaining consistent processing. Using other manufacturing techniques, or lower voltages and impedances, a need for cascode or multiply-stacked FETs may be avoidable.

CONCLUSION

[0107] The foregoing description illustrates exemplary implementations, and novel features, of a method and apparatus that employs stacked transistors to control conduction between a pair of nodes in an integrated circuit. The skilled person will understand that various omissions, substitutions, and changes in the form and details of the methods and apparatus illustrated may be made without departing from the scope of the invention. Numerous alternative implemen-

tations have been described, but it is impractical to list all embodiments explicitly. As such, each practical combination of the apparatus or method alternatives that are set forth above, and/or are shown in the attached figures, constitutes a distinct alternative embodiment of the subject apparatus or methods. Each practical combination of equivalents of such apparatus or method alternatives also constitutes a distinct alternative embodiment of the subject apparatus or methods. Therefore, the scope of the presented invention should be determined only by reference to the appended claims, and is not to be limited by features illustrated in the foregoing description except insofar as such limitation is recited, or intentionally implicated, in an appended claim.

[**0108**] It will be understood that similar advantages of integration will accrue to circuits having other functional blocks. For example, mixers may be incorporated on such a device, enabling integration of more portions of transmission signal processing. Phase locked loops may further enhance the ability to generate the transmission signal on the same monolithic IC as the RF front end or transceiver. Additional types of filters may be useful, for either or both of receive and transmission processing.

[**0109**] All variations coming within the meaning and range of equivalency of the various claim elements are embraced within the scope of the corresponding claim. Each claim set forth below is intended to encompass any system or method that differs only insubstantially from the literal language of such claim, if such system or method is not an embodiment of the prior art. To this end, each described element in each claim should be construed as broadly as possible, and moreover should be understood to encompass any equivalent to such element insofar as possible without also encompassing the prior art.

What is claimed is:

1. An integrated RF Power Amplifier (PA) circuit, comprising:

a) an input node to accept an input signal with respect to a reference voltage Vref, coupled to a gate G**1** of a first insulated-gate FET M**1**;

b) a plurality of additional insulated-gate FETs M**2** to Mn having a same polarity as M**1** and coupled in series with M**1** to form a control circuit configured to control conduction between the reference voltage and an output drive node, wherein FETs M**2** to Mn are each enslaved to M**1**; and

c) an output coupling capacitor coupling the output drive node to an output load node.

2. The integrated circuit of claim 1, further comprising (d) an output power control input node coupled to a power controlling insulated-gate FET that is coupled in series connection with M**1**.

3. The integrated circuit of claim 2, wherein the power controlling FET is disposed between the reference voltage and a power supply voltage external to the PA.

4. The integrated circuit of claim 2, wherein the power controlling FET is one of the FETs M**2** to Mn.

5. The integrated circuit of claim 1, further comprising a low-pass filter disposed in series with the output coupling capacitor between the output drive node and the output load node.

6. An integrated circuit including a multiple-FET stack circuit for controlling conduction between a drive output node Vdrive and a reference voltage node Vref under control of an input signal applied between an input signal node and Vref, the integrated circuit comprising:

a) a series stack of J same-polarity FETs M_N, N an integer between 1 and J and J an integer 3 or greater, each FET M_N having a source S_N, a gate G_N and a drain D_N,

b) an input signal node coupled to the gate G_1 of a signal-input FET M_1 of the FET stack;

c) for 0<N<J, a series coupling between each drain D_N and the source $S_{(N+1)}$ of a next higher FET $M_{(N+1)}$ of the FET stack;

d) for 1<N≦J, a gate coupling between each gate G_N and at least one lower FET $_{M(N-K)}$, K an integer between 1 and (N−1), in a configuration enslaving each FET $M_{(N+1)}$ to M_1 so as to conduct substantially concurrently with, and under control of, conduction in M_1;

e) a source coupling for the FET stack between S_1 and Vref; and

f) a drain coupling for the FET stack between D_1 and Vdrive.

7. The integrated circuit of claim 6, wherein a peak value of voltage on Vdrive with respect to Vref, Vdrive(peak), is divided approximately uniformly across all J FETS such that each drain-source voltage $Vds_{(N)}$ is approximately Vdrive-(peak)/J.

8. The integrated circuit of claim 6, wherein each gate coupling comprises a capacitive coupling between G_N and S_1 for each N, 1<N≦J.

9. The integrated circuit of claim 6, further comprising a resistive divider for biasing a FET M_N, N>1, of the FET stack.

10. A Class A, B or C RF PA comprising an integrated circuit according to claim 6, wherein the multiple-FET stack is configured as a primary amplifying device of the Class A, B or C RF PA.

11. A quad mixer comprising an integrated circuit according to claim 6.

12. A Class F RF PA comprising an integrated circuit according to claim 6, wherein the multiple-FET stack is configured as a primary amplifying device of the Class F RF PA.

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