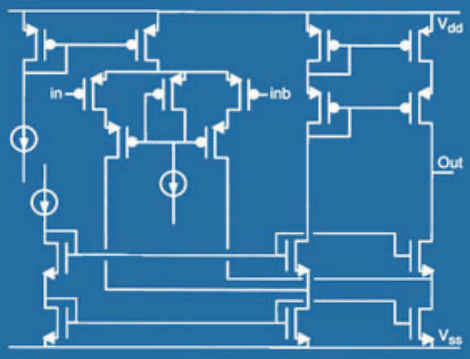
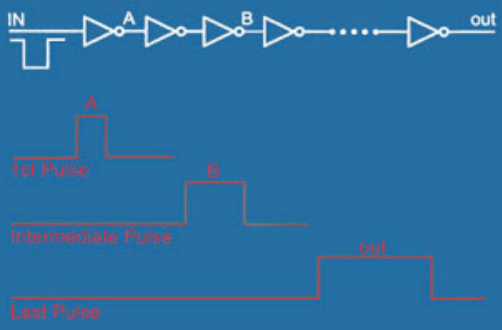
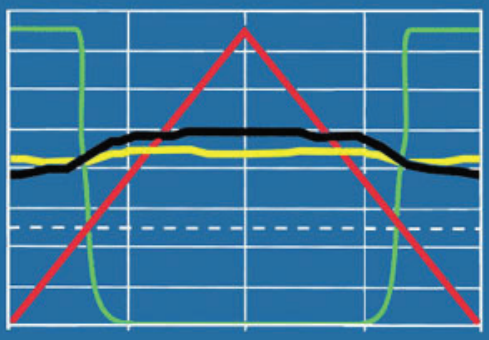
SOI Design:

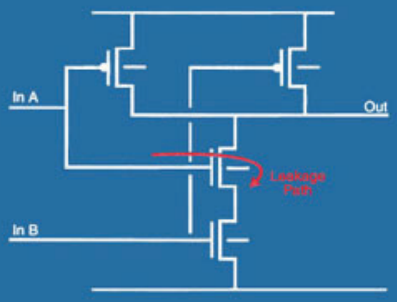
Analog, Memory and Digital Techniques

Andrew Marshall
Sreedhar Natarajan









Kluwer Academic Publishers

SOI DESIGN

ANALOG, MEMORY AND DIGITAL TECHNIQUES

This page intentionally left blank

SOI DESIGN

ANALOG, MEMORY AND DIGITAL TECHNIQUES

by

Andrew Marshall
&
Sreedhar Natarajan

Texas Instruments Incorporated

KLUWER ACADEMIC PUBLISHERS
NEW YORK, BOSTON, DORDRECHT, LONDON, MOSCOW

eBook ISBN: 0-306-48161-8
Print ISBN: 0-7923-7640-4

©2003 Kluwer Academic Publishers
New York, Boston, Dordrecht, London, Moscow

Print ©2002 Kluwer Academic Publishers
Dordrecht

All rights reserved

No part of this eBook may be reproduced or transmitted in any form or by any means, electronic, mechanical, recording, or otherwise, without written consent from the Publisher

Created in the United States of America

Visit Kluwer Online at: http://kluweronline.com
and Kluwer's eBookstore at: http://ebooks.kluweronline.com

To Judith, Amy and Elise for their enduring patience and encouragement.

-- Andrew Marshall

To my wife Chandra for her patience and support, my Parents, my brother Sriram and his family, my wife's family, and friends for their continued encouragement.

-- Sreedhar Natarajan

Samsung Exhibit 1010, Page 6 of 204

This page intentionally left blank

Table of Contents

Preface	xix
Acknowledgements	xxi
Chapter 1: Overview	1
1.1 Silicon on Insulator – a brief Introduction	1
1.2 Circuits and SOI	2
1.3 Technology and SOI	3
Chapter 2: SOI Materials	5
2.1 Silicon on Heteroepitaxial Substrate	5
2.2 Silicon-Oxide-Silicon SOI substrates	6
2.2.1 Separation by Implantation of Oxygen	6
2.2.2 Wafer-Bonding methods for preparing SOI	8
2.2.3 SOI Materials Summary	11
2.3 Comparison of SOI and Bulk	11
2.3.1 Isolation Techniques	11
2.4 SOI Technology Advantages	16
2.4.1 Capacitance Reduction	16
2.4.2 Reduced Short Channel Effect	16
2.4.3 Lower Device Threshold	16
2.4.4 Soft Error Rate (SER) Effects	17
2.5 Performance	17
2.6 Partially and Fully Depleted-SOI	18
2.7 Technology Scaling	21
2.8 SOI Device Properties	22
2.8.1 Source/Drain-to-Substrate Capacitance	22
2.8.2 Gate Leakage	22
2.9 Body Effects	23
2.9.1 Bipolar Effect	23

2.9.2 Kink Effect 24
2.9.3 Capacitive Body Effects 26

2.10 Body Ties 29
2.10.1 Body Tied to Substrate 31
2.10.2 Body-tied to gate Configurations 32
2.10.3 Resistive Body Tie 33

2.11 Device Noise 34

2.12 Self Heating 36
2.12.1 Self Heating from elsewhere on the same chip 38
2.12.2 Self Heating from within a sub-circuit 39

Chapter 3: Components 47

3.1 MOS devices 47

3.2 Diodes 49

3.3 Bipolar Transistors 49

3.4 Lateral DMOS 51

3.5 Drain Extended Devices 53
3.5.1 Design of an SOI high voltage DEMOS device. 55

3.6 Compound High Voltage SOI Structures 56

3.7 Passive Components 57
3.7.1 Resistors 57
3.7.2 Capacitors 58
3.7.3 Inductors 59

Chapter 4: SOI Modeling 63

4.1 Modeling Introduction 63

4.2 Example SOI spice deck 66

4.3 Models 68
4.3.1 BSIM 68

Samsung Exhibit 1010, Page 9 of 204

4.4 Alternative Model Options 70

Chapter 5: Layout for SOI 75

5.1 Introduction to Layout for SOI components 75

5.2 Converting designs from Bulk to SOI 77
5.2.1 Diodes 77
5.2.2 Bipolar Transistors 79

5.3 Layout for Minimization of Thermal Self Heating Effects 80
5.3.1 Cross coupling with thermal coupling 81

5.4 Output Stages 83

Chapter 6: Static SOI Design

6.1 Introduction 85
6.1.1 Lower Fan Out Capacitance 87

6.2 Decreased Body Effect 87

6.3 Gate Leakage 88

6.4 Static Inverter Characteristics 89

6.5 Body Voltages in SOI Inverters 92

6.6 Body Voltage Convergence 94
6.6.1 Delay vs. effective gate length 94

6.7 Noise Margin In Inverters 95

6.8 Nand Gate Response 96
6.8.1 Body Voltage Response in Nand Gates 101

6.9 Nor Gate response 103

6.10 Static OR-AND SOICMOS Circuit 104

6.11 XOR Gate response in SOI 107

Samsung Exhibit 1010, Page 10 of 204

6.12 Ring Oscillator Performance 108
6.12.1 Nand Fan-out of 3 ring-Performance vs. V_{DD} 109
6.12.2 Nand fanout of three - Performance vs supply 110
6.12.3 Nand fan-out of one 110

6.13 Pass Gate Response 112
6.13.1 Pass transistor based circuits 114
6.13.2 Pass transistors based Multiplexers 115

6.14 History Dependence 117

6.15 SOI vs BULK : Performance benefits in Digital Circuits 118

6.16 Floating body and hysteresis effect 119

6.17 Non Ideal diode characteristics 120

Chapter 7: Dynamic SOI Design

7.1 Introduction 125

7.2 Dynamic Circuit Response 125
7.2.1 Dynamic History Effect 125
7.2.2 Dynamic Charge Sharing 126
7.2.3 Capacitive Coupling Effects 126
7.2.4 Keeper Devices or Bleeders 127

7.3 Dynamic Circuit Design Considerations 129

7.4 Re-ordering and Remapping 130

7.5 Logical Remapping 130

7.6 Complex Domino 132
7.6.1 Three-input Domino OR Gate 132
7.6.2 Dynamic AND-OR Domino Gate 133

7.7 No-Race Logic (NORA) 136

7.8 Dynamic Noise Suppression 141

7.9 Design Issues in Dynamic 2-way NAND Logic 142

7.10 Dynamic 2-Way OR Circuit 145

7.11 Dynamic Cascade Switch Logic 147

7.12 Clocked CMOS 149

7.13 Pulse Stretching in Dynamic Circuits 153

7.14 Dynamic Wide-OR 157

7.15 Non Overlapping Clocks 158

7.16 Pass transistor based Non-Overlapping Clocks 159

7.17 Low Power SOI Techniques 161
7.17.1 Dynamic Threshold SOI CMOS 161
7.17.2 Dynamic Threshold Multithreshold CMOS Logic 162
7.17.3 Dynamic Threshold Pass Transistor Logic 164
7.17.4 Dynamic threshold voltage Full Adder 165
7.17.5 Dynamically Body Bias SOI CMOS Inverter 174

Chapter 8: SOI SRAMs

8.1 Introduction 181

8.2 SRAM Cell structures 182

8.3 Design considerations and specifications for SRAM Cells 185
8.3.1 4T-2R Polysilicon resistor load SRAM 186
8.3.2 SRAM cell with 2 thin-film transistor loads 186
8.3.3 6T-PMOS Load SRAM cells 186

8.4 Four Transistor SRAM using Self-body biased MOSFET 187

8.5 Basic SOI SRAM Cell operation 189
8.5.1 READ Operation in a SRAM Cell 189
8.5.2 Write operation in SRAM Cell 193

8.6 Cell Stability 197

8.7 SRAM Junction & Bit line capacitance 201

Samsung Exhibit 1010, Page 12 of 204

8.8 Decoders 201

8.9 SRAM Architecture 203

8.10 Bit Line Related Architecture 205

8.11 Sense Amplifiers 206
8.11.1 Differential Amplifier 207
8.11.2 Clocked Dual Slope Sense Amplifiers 211
8.11.3 Dynamic Body Charge Controlled Sense Amplifier 213
8.11.4 Sense Amplifier Techniques 218

8.12 Mismatches in Sense Amplifiers 220
8.12.1 Offset Considerations for High Speed Sensing 223

8.13 Mismatch in SRAM Cells 225
8.13.1 Body Bias 225
8.13.2 Supply Rail Droop 225
8.13.3 Body-to-Body Coupling 226
8.13.4 Common Mode Supply Rail 226
8.13.5 MOS Junction capacitance 226
8.13.6 Self Heating 226

8.14 SER Issues in SRAMs 227

8.15 SOI CMOS Memory Challenges 228

8.16 Destructive read-out characteristics of SRAM 229

Chapter 9: SOI DRAMs

9.1 Introduction 235

9.2 DRAM structure and Operation 237

9.3 Memory Array 238

9.4 DRAM cell storage 241
9.4.1 Storage to Bit Line Capacitance 243

9.5 SOI DRAM Process 244
9.5.1 Smart-cut for DRAM 246

9.5.2 Quasi- SOI technology 246

9.6 Influence Of SER on SOI DRAMs 246

9.7 Cosmic Ray induced Soft Errors in SOI DRAMs 247

9.8 DRAM Refresh and Data Retention 249
9.8.1 Static Data Retention 249
9.8.2 Dynamic Data Retention 250
9.8.3 Parasitic Leakage in DRAMs 254

9.9 High Density DRAMs with Body Contacts 258

9.10 Operating Voltage Reduction 259
9.10.1 Half-Vdd Data Line Pre-charge 259
9.10.2 Signal To Noise Ratio 260

9.11 Sense Amplifier Operation 260
9.11.1 Sensing with Dummy Cell Structure 263
9.11.2 Sensing with Body Contacts 264
9.11.3 Body-Pulse Sense Amplifier (BPS) 265

9.12 Word Line Boosting 267
9.12.1 Boosted Word Line with body contacts 268
9.12.2 Boot-strapped Word line Driver 268

9.13 Charge pumps and generators 269

9.14 Embedded DRAMS in SOI 274

9.15 DRAM operation problems 274

9.16 SOI DRAM READ Critical Path Body Contacts 275

9.17 Synchronous Interface on DRAMs 276

9.18 High Speed Modes for Synchronous DRAMs 277

9.19 Prefetch Architecture 279

9.20 Other Architectures 280

Samsung Exhibit 1010, Page 14 of 204

9.21 Destructive read out characteristics of DRAM 281

Chapter 10: SOI Analog Design

10.1 Introduction 289
10.1.1 Benefits of SOI for Analog Design 289
10.1.2 Drawbacks of Analog Design on SOI 289

10.2 Body Voltage Regulation 292
10.2.1 Dynamic Body 292

10.3 Circuit Thermal Coupling Effects 294
10.3.1 DC Thermal Coupling in Current Mirrors 294
10.3.2 Transient Thermal Coupling in Current Mirrors 294

10.4 Band-gap Designs 295
10.4.1 β helper circuitry 298
10.4.2 "Threshold Voltage Difference" Voltage Reference 300

10.5 Charge Pump Circuitry 301

10.6 Amplifiers 302
10.6.1 Sense Amplifier 302
10.6.2 Operational Amplifiers 303
10.6.3 Operational Transconductance Amplifier Design 309

10.7 Matching 310

10.8 Output Stages / Buffers 311

10.9 High Voltage and Power Applications 312

10.10 Sample and Hold Circuitry 312

10.11 Circuits for RF/Wireless Applications 313
10.11.1 Radio Frequency Low Noise Amplifier (LNA) 314
10.11.2 Mixers and Analog Multipliers 316
10.11.3 Delay Locked Loop 317
10.11.4 Phase Locked Loop 319
10.11.5 Phase Detector 319
10.11.6 Loop Filter 320
10.11.7 Oscillators 320

Samsung Exhibit 1010, Page 15 of 204

10.12 Microwave Applications 324

10.13 Voltage Regulation 325
10.13.1 Series Regulator 325
10.13.2 LDO Regulator 325

10.14 Analog to Digital Converters (ADC) 326
10.14.1 Successive Approximation ADC 326
10.14.2 Flash Converters 327
10.14.3 Pipelined ADCs 329

10.15 Digital-to-Analog Converters (DAC) 330

10.16 Sigma Delta Modulator 331

10.17 Interface between Digital and Analog Circuitry 332

10.18 Power Amplifiers 333

10.19 Sensors and Actuators 333

Chapter 11: Global Design Issues

11.1 Introduction to Global Design Issues 339
11.1.1 Cell Libraries 339
11.1.2 Clock Distribution 339
11.1.3 Decoupling Capacitance and Series Resistance 340
11.1.4 High Temperature Operation 340
11.1.5 Gate Leakage 341

11.2 Noise Immunity 341
11.2.1 Circuit Noise 341
11.2.2 Capacitive Coupling Noise 342
11.2.3 Delay Noise 343
11.2.4 Logic Noise 343
11.2.5 Decoupling Capacitors 343

11.3 Latchup Immunity 343

11.4 Self Heating 346

11.5 Electrostatic Discharge (ESD) 347

11.5.1 ESD Protection in Output Structures 348

11.6 Radiation Hard (Rad-Hard) Circuits 349

11.7 Reliability 350
11.7.1 IDDQ (Quiescent I_{DD}) 351
11.7.2 Delay Fault Testing 354

11.8 Package and Bond wire 355

Chapter 12: Low Power Design

12.1 Introduction 359

12.2 Clocking 360
12.2.1 Clock Generation 360
12.2.2 Clock Distribution 360
12.2.3 Clock Gating 361

12.3 Options for Low Power 361
12.3.1 Static vs. Dynamic Logic 362
12.3.2 Gate Sizing 362
12.3.3 Minimizing Switching 363
12.3.4 Interconnect 363
12.3.5 Low Voltage Swing 363

12.4 Analog Low Voltage Operation 364

12.5 Floating Voltage Schemes 364
12.5.1 Low Voltage Output Operation 365

12.6 System Performance 366

12.7 System Power Management 367
12.7.1 Low Power Standby Modes 367
12.7.2 Supply Voltage during Standby 367
12.7.3 Trade-Off for Power 368

12.8 Instruction Set Architecture 368
12.8.1 Instruction Complexity: RISC or CISC 368

12.9 Reduction of Voltage below 3.3V 368

Samsung Exhibit 1010, Page 17 of 204

Chapter 13: SOI in Development

13.1 SOI Technology Roadmap 371

13.2 Device Enhancements 371
13.2.1 Enhanced-gate SOI MOSFET 371
13.2.2 FinFET 373

13.3 Quantum Devices 373

13.4 Stacked SOI 373

13.5 Reduced Temperature Operation 374

13.6 High Temperature Operation 374

13.7 New Circuit Designs for SOI 375
13.7.1 Merged Bipolar / MOS 375
13.7.2 Body Driven Operational Amplifier 375
13.7.3 Body-input D-Flip-Flop 377
13.7.4 SOI Transistor as a DRAM 377

Appendix 1: Internet Sites (issue 1.0) 381

Appendix 2: Trade Mark / Technology Information (issue 1.0) 382

Index 383

About the Authors 393

Samsung Exhibit 1010, Page 18 of 204

This page intentionally left blank

Preface

In the 1850's my wife's great-great grandfather wrote a medical textbook. In the year and a half that it has taken to complete this work I have grown to appreciate not only how difficult it is to write a book, but also how much more difficult it must have been back then. One hundred and fifty years ago Dr. Julius Jeffreys had to write his entire tome by hand, without the aid of error correcting word processing software or even electric light. More obviously in electronics than in many other fields, the pace of technology development since that time has been astounding. Even in just the past fifty years semiconductor technology has progressed from little more than a laboratory curiosity to an integral part of our daily lives.

Now silicon on insulator technology is becoming the process of choice for high performance consumer electronics, it is appropriate that memory systems and analog circuitry are considered in a single volume with the SOI process and logic implementation. Such an overview helps put SOI into perspective. What we see is a very impressive technology, which holds a great deal of promise. There are applications where SOI does not appear to be a good fit, but generally it appears that SOI has a bright future.

We have compiled this book, based on available literature and SOI circuit development work at Texas Instruments.

Chapter 1 introduces the reader to silicon on insulator, with a very brief review of the history of SOI technology and circuits.

Chapter 2 briefly reviews the materials of SOI, and methods used to generate the most common forms of SOI material used commercially. Manufacturing considerations and materials properties are highlighted in this section.

In chapter 3 we review silicon on insulator devices, with discussion of how they differ from devices available to the designer of bulk silicon integrated circuits. Electrical properties associated with SOI devices are introduced in the discussion of MOS devices, diodes, bipolar transistors and passives.

Chapter 4 explores the challenges of modeling SOI material and devices, with particular emphasis on circuit simulation. The chapter will be of particular interest to the designer of analog circuits, as an introduction to circuit simulation of SOI components.

Chapter 5 introduces some concepts for successful SOI circuit layout. We review various options for the reduction of thermal self-heating effects and

Samsung Exhibit 1010, Page 20 of 204

consider the conversion of designs from bulk to SOI from a layout perspective.

Chapters 6 and 7 provide a review of static and dynamic logic circuits by way of introduction into the memory sections. While this has been covered in detail elsewhere (notably Kerry Bernstein and Norman Rohrer' SOI Circuit Design Concepts), the summary here permits a full understanding of the possibilities and challenges of SOI essential to a good cognition of more complex circuitry.

Chapters 8 and 9 are devoted to the dominant memory structures in current use, the SRAM and DRAM. Methods to improve memory performance at the memory cell and sense amplifier level are discussed.

Chapter 10 addresses techniques to permit the integration of analog circuitry into SOI designs. This is an inevitable requirement as SOI use transfers from just microprocessors to DSP and mixed signal applications.

Chapters 11 and 12 examine global design issues, those issues that affect both digital and analog circuit design, and are more easily discussed in a general setting. Low power and low voltage circuit design is of particular importance to the industry, and is thus considered in a chapter by itself.

Chapter 13 takes a look at some of the possibilities for SOI in development, both from the material and circuit viewpoints.

For updates, corrections etc., the web site associated with this publication is given in appendix 1. This site also has contact information where you the reader may communicate suggestions, errata etc. We hope this will prove to be a valuable source of data in this rapidly evolving field.

In summary, we echo the words of Kerry Bernstein and Norman Rohrer, when in the final words of their preface to "SOI Circuit Design Concepts" they state, "Rather than designing to avoid SOI's idiosyncrasies, the true benefit of the technology may be realized when these features are exploited".

Andrew Marshall
Sreedhar Natarajan

October 2001

Samsung Exhibit 1010, Page 21 of 204

Acknowledgements

It is inevitable with a work of this length and scope that a huge number of individuals have had a hand in enhancing the content. We thank everyone involved in the work, but would especially like to thank the following:

We extend a special thanks to the reviewers, for their very helpful suggestions: Brock Barton, Charvaka Duvvury, John Fattaruso, David Scott, Howard Tigelaar, Tom Vrotsos.

For discussions and insight: Terry Blake, James Burns, Xiaowei Deng, Olivier Faynot, Jim Gallia, Keith Green, Ted Houston, Keith Joyner, Weideng Liu, Homi Mogul, Betty Prince.

For drafting, simulation, and silicon evaluation: Erich Caulfield, Andres Diaz, Imran Hossain, Rick Little, Gary Mathews, Brian Neal, Michelle Nguyen, Mouli Vaidyanathan.

For enabling the work: Randy McKee, Yoshio Nishi, David Spratt, Tom Thorpe and especially Wah Kit Loh.

Samsung Exhibit 1010, Page 22 of 204

This page intentionally left blank

Chapter 1: Overview

1.1 Silicon on Insulator – a brief Introduction

Silicon on insulator (SOI) is a very attractive technology for large volume integrated circuit production and is particularly good for low-voltage, low-power and high-speed digital systems. SOI has also proved to be effective in various niche and growing markets. IC processes based on SOI are known to reduce susceptibility to radiation, and have been used for many years in high radiation environments. SOI is also used for power integrated circuits, micro-electromechanical systems (MEMS), integrated optics and high temperature applications.

Devices built on SOI have lower capacitances to substrate than comparable devices on bulk silicon. MOS transistors on SOI are also, in most cases, capable of higher current density than obtained with equivalent devices on bulk. These improvements are achieved without reductions in process geometries, and thus have the benefit of delaying the introduction of higher precision production equipment, resulting in significant capital equipment cost deferral. The performance advantages associated with SOI have led to consideration of the technology for high performance applications, such as microprocessors, DSPs and wireless applications.

Since being introduced into limited production in the early 1990s the variety of SOI explained by the term "active silicon, separated from a silicon substrate by a silicon oxide insulator" has been developed into a mainstream technology, especially for digital applications [1.1 – 1.4]. Market predictions suggest that SOI will receive a growing proportion of the total integrated circuit market, particularly for high performance requirements.

1.2 Circuits and SOI

SOI offers numerous opportunities and challenges in the design of low-voltage and low-power CMOS circuits for both analog and digital applications. The benefits of this technology for digital applications have been clear for many years. The exploitation of SOI for analog and memory subsystems, meanwhile, has lagged behind digital developments, but is now beginning to attain a level of parity, with circuits that are in some cases improved over their bulk counterparts. SOI is suitable for digital, memory and analog designs, although it is not necessarily straightforward to convert circuits developed for bulk processes into SOI. Device operation is affected by SOI specific factors, including resistive body ties and localized self-heating.

The circuit design examples covered in this book have, for the most part, been developed specifically for use with partially depleted (PD) SOI rather than fully depleted SOI. This is because:

(a) The current lack of availability of good quality fully-depleted (FD) SOI material in abundance, and;

(b) Once PD-SOI analog and digital circuit designs are available the conversion of these circuits to FD-SOI is expected to be straightforward.

Memory and most analog circuits either interface to, or are incorporated within, a digital environment. The design of analog circuits on SOI, in a mixed signal environment, and memory design in an embedded memory application are discussed. Various processes are examined and comparison is made between bulk and SOI circuit design concepts. SOI is the process of choice in various RF applications, particularly when digital circuitry is required. In addition to known and well understood advances in digital circuit operation, the use of SOI can directly lead to improved passive component capability (particularly inductors) and active RF component frequency response.

The potential to integrate high power and high voltage components is a significant benefit of SOI processes. In addition SOI permits simpler higher temperature circuit design (potentially negating some of the detrimental consequences of increased temperature circuit elements due to local heating). As is well known, SOI also gives improved immunity to radiation effects (so-called rad-hard circuit design). SOI CMOS allows fabrication, design and operation at low supply voltages for analog, digital and microwave components with properties significantly superior to those obtained using bulk silicon CMOS.

Samsung Exhibit 1010, Page 25 of 204

1.3 Technology and SOI

There are a number of books on SOI technology [1.5 – 1.7]. This work examines some of the basics, but is primarily concerned with circuit related issues. Static and dynamic logic circuit design has previously been studied in some detail [1.5], however, memory design for SOI and analog circuit designs have hitherto been examined only in a piecemeal manner.

SOI material is considered here in terms of implementations that are promising or have been used elsewhere in circuit development, with historical perspective where appropriate. The two basic methods for producing SOI substrates are SIMOX and bonded silicon technologies. In most cases these are interchangeable in terms of circuit design.

Samsung Exhibit 1010, Page 26 of 204

References

[1.1] F. Assaderaghi, et. al., "Transient Pass-Transistor Leakage Current in SOI MOSFET's", IEEE Electron Device Letters, June 1997, pp. 241-3.

[1.2] G. Shahidi, et. al., "Mainstreaming of the SOI Technology", IEEE International SOI Conference, Oct 1999, pp. 1-4.

[1.3] F. Assaderaghi, et. al., "History-Dependence of Non-Fully Depleted Digital SOI Circuits", VLSI Tech. Digest, 1996, pp. 122-3.

[1.4] M. Canada, et. al., "A 580MHz RISC Microprocessor in SOI", ISSCC 1999, pp. 430-431.

[1.5] K. Bernstein & N. J. Rohrer, "SOI Circuit Design Concepts", Kluwer Academic Publishers, January 2000, ISBN 0-7923-7762-1

[1.6] J-P. Colinge, "Silicon-on-Insulator Technology Materials to VLSI, 2nd Edition" Kluwer Academic Press, September 1997, ISBN 0-7923-8007-X

[1.7] S. Cristoloveanu & S. S. Li, "Electrical Characterization of Silicon-on-Insulator Materials and Devices" Kluwer Academic Press, June 1995, ISBN 0-7923-9548-4

Chapter 2: SOI Materials

2.1 Silicon on Heteroepitaxial Substrate

SOI has been created by both epitaxial growth and by transfer of an active layer onto various types of substrate. Some of the most common heteroepitaxial substrates for silicon include diamond, sapphire, cubic zirconia, calcium fluoride, quartz and glass. Among these processes silicon on sapphire (SOS) and silicon on glass or quartz are the only ones that have seen a level of commercial success.

Historically, SOS material has been available since the 1970s and has led to specialized commercial products. SOS technology requires a silicon epitaxial layer to be grown on sapphire. Defect density of the silicon is relatively high due to lattice mismatch, but decreases with silicon thickness. Electron mobility is significantly lower in SOS than bulk, due to the high defect density and compressive stress in the silicon caused by the lattice mismatch [2.1]. Silicon on sapphire has been used principally for defense and space (rad-hard) applications, where insensitivity to circuit latch-up due to radiation is important. The process is relatively expensive.

Silicon on quartz and silicon on glass are important areas of current development. Most modern processes for heteroepitaxial SOI are similar, and use bonding techniques similar to the majority of the silicon-insulator-silicon processes. This approach produces an active silicon region that is monocrystaline, so is electrically superior to polysilicon films grown directly on quartz or glass. Applications for silicon on glass include liquid crystal displays (LCDs), charge coupled device (CCD) detectors and high definition television (HDTV) projection systems.

One type of silicon-on-glass is termed "silicon on anything" (SOA) [2.2]. If a high resistivity substrate is chosen, SOA is particularly good for integrated inductors. A transparent substrate may be useful for opto-electronic devices. However, these do suffer from inferior thermal characteristics compared to bulk substrates. SOA starts as a fully processed SOI wafer. Additional processing is then required as follows: A glass plate is bonded on top of the fully processed circuits, then the original silicon substrate is etched back to the buried oxide layer. Bondpads are contacted by creating openings in the buried oxide. With this technology it is possible to fabricate low-power transistors. It is also possible to produce integrated inductors that have a quality factor greater than 25 at 1GHz [2.2, 2.3].

2.2 Silicon-Oxide-Silicon SOI substrates

While not exhaustive, this section considers most commercially viable and some experimental techniques for creating SOI. These are separable into two basic methods: (1) separation by implantation, and (2) wafer bonding.

2.2.1 Separation by Implantation of Oxygen

The Separation by Implantation of Oxygen (SIMOX) process is a technique to create SOI through the use of implantation. Most versions of this process use oxygen implantation. Implantation is performed before CMOS processing. High-energy implantation forces oxygen deep below the wafer surface (figure 2.1). The implanted dose to form a buried oxide layer is usually over 200 times higher than required for ion implantation doping [2.1]. After implantation, a 1300°C anneal of around 6 hours is performed, which forms a silicon dioxide layer and recrystalizes the epitaxial layer of any damage sustained from the high-energy implant. The oxygen typically forms an oxide region of thickness from about 50 to 500nm, with a thickness uniformity of +/- 2.5nm. The oxide region normally starts below a 40-70nm silicon region (for fully depleted material), and approximately 100-200nm for partially depleted material. In general terms the oxide thickness produced is categorized as; full dose, where the buried oxide (BOX) layer is about 380nm; medium dose, where the BOX layer is about 150nm; and low dose (approximately 100nmBOX thickness) [2.4].

Implant dose with O_2 ions is usually between 4.0 and 4.5el7 cm^2 at 200 keV. Several companies manufacture implanters aimed at the SOI market, including Hitachi [2.5] and Ibis [2.6], and numerous manufacturers produce SIMOX wafers.

Patterned Insulators

Secective patterning of the buried oxide of SIMOX permits mixed bulk and SOI on the same wafer. The body of a SOI device may be contacted from the

Samsung Exhibit 1010, Page 29 of 204

substrate, providing not only true SOI devices, but also structures that are bulk in nature. Selective patterning does leave a stress region within a few microns from the edge of the buried silicon dioxide layer. This must be taken into account in the layout for selectively patterned designs. Patterned insulators permit various combination structures that may otherwise not be practical. These include DRAM chips combined with SOI logic [2.7], and vertical bulk power devices combined with SOI circuitry. High performance logic may be fabricated in SOI, while the DRAM is fabricated on bulk areas. Selective patterning is shown pictorially in Figure 2.2.

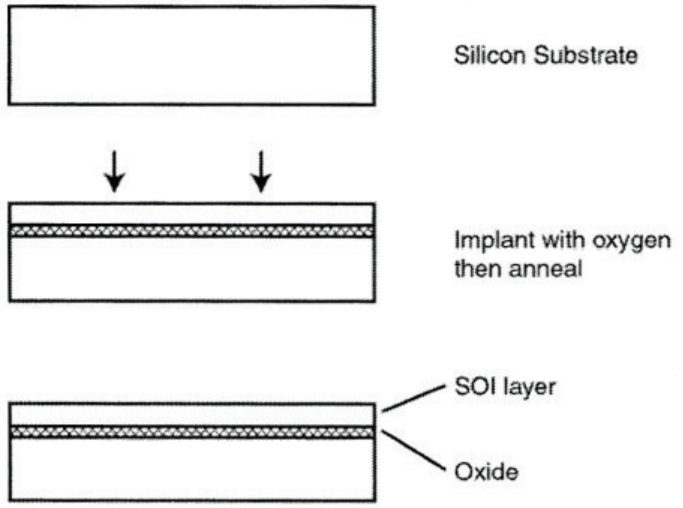


Figure 2.1: Representation of the preparation of SOI using SIMOX process. The starting material is a conventional silicon substrate. This is implanted with oxygen and annealed, to form an SOI layer over oxide, on a silicon support.

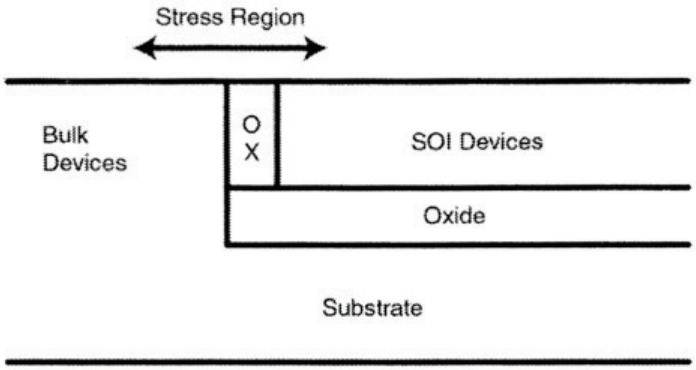


Figure 2.2: Selective SIMOX pattern, showing the possibility of combining bulk and SOI devices on a single substrate. The damage area around the edge of the buried oxide should be avoided for the purposes of building electrically active components.

Samsung Exhibit 1010, Page 30 of 204

2.2.2 Wafer-Bonding methods for preparing SOI

Silicon-oxide-silicon wafer technologies, with the exception of SIMOX and its variants, are based on wafer bonding. The basic process sequence for the fabrication of bonded SOI wafer is as follows: The active wafer (also called the donor wafer) is bonded to the support wafer (also called the substrate or handle wafer). In most cases both active and support wafers have been oxidized, although some processes do not require the support to be oxidized. The bonded pair is annealed to increase bond strength. Processing differs depending on the techniques employed, but in all cases the active wafer is reduced to the desired thickness after bonding. Several alternatives are possible to perform thinning, including grinding and chemical etching, plasma assisted chemical etching, bond and selective etch of porous silicon and implant-enhanced wafer splitting.

Physical Thinning and Etchback

The grind and etchback method of creating SOI is the most mature of the practical forms of wafer bonding based SOI techniques, but is least economical in terms of raw material. Two wafers are required, a support wafer and a wafer to contain the circuitry (the active wafer). Both support and active wafers are oxidized. The two wafers are bonded together (oxide to oxide), and the wafer designated the active wafer is ground, annealed and polished.

For the basic grind-back method the active wafer is ground and thinned down to the thickness required for the active layer. SOI quality is usually very good with this process technique [2.8], but thickness uniformity is poor. Uniformity of the active region depends on flatness of the substrate wafer. This is usually inadequate for use except in thick film SOI.

To bypass uniformity problems of grinding, etch-stop methods have been developed. In etch-stop processes a high concentration of an impurity is implanted into the active wafer, prior to bonding. The active wafer is ground and chemically etched using a selective etch. Boron [2.9] and nitrogen-implanted layers [2.10] are common impurities used as etch-stops to improve SOI layer uniformity. Nonetheless, uniformity remains limited since the concentration profile of the etch-stop dopant blurs during annealing. The crystalline quality of this type of material may also be degraded due the high dose implantation.

Figure 2.3 shows the method of preparation of ground and etch-back silicon on insulator. Bonding has the advantage over SIMOX SOI that the substrate can have a wide range of resistivity. Typically the substrate is moderately doped P-type, but there is no fundamental restriction. Higher resistivity

Samsung Exhibit 1010, Page 31 of 204

substrates may have beneficial properties in some applications, especially when the circuitry contains inductors, where higher resistivity substrates can lead to higher Q devices. Typically for bonded wafers, the oxide between substrate and active region is 400-500nm.

SmartCut®

SmartCut Technology from SOITEC [2.11] is a variant of the bonded technique. Here, however, the wafer to be used for the active silicon is implanted with hydrogen (protons) at approximately 1μm depth. Annealing creates a stress fracture. The active and support wafers are bonded, and the active wafer is split along the stress fracture to generate a Unibond® wafer. The unused portion of the active wafer can be reused (either as the support wafer or active wafer), resulting in a cost saving over the traditional ground-back method (described above). The bonded combination is the SOI wafer. It is annealed and polished in readiness for use. Figure 2.4 shows the method of preparation for SmartCut wafers.

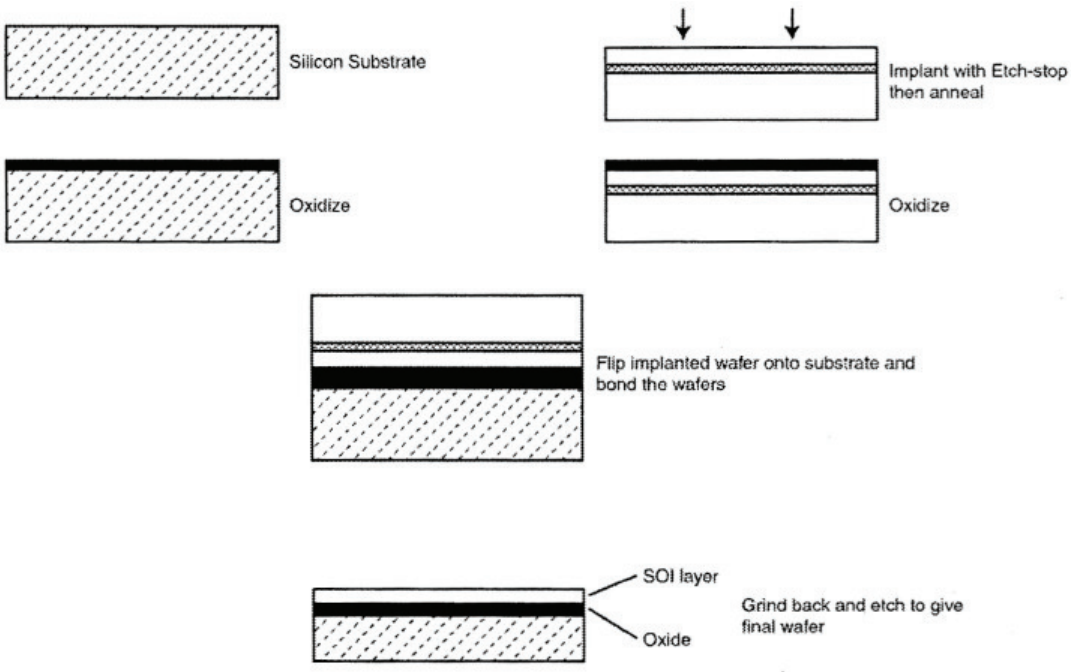


Figure 2.3: Process steps for the grind and etch-back processes for creating SOI material.

Eltran(tm)

Eltran (Epitaxial Layer TRANsfer) is another method of creating SOI wafers [2.12]. This process uses porous silicon to obtain a uniform SOI thickness. A region of about 12μm of porous silicon is formed by anodizing the surface of a boron- doped silicon wafer. An epitaxial silicon layer is grown on the

porous silicon. The layer is bonded to the oxidized substrate wafer. The porous silicon is split from the epitaxial material, using a water jet, and results in a re-usable split wafer. The porous silicon remaining on the epitaxial silicon is selectively etched away [2.13]. The quality of epitaxial silicon grown on porous silicon is poor due to stacking faults. However, stacking faults can be significantly reduced with a pre-bake in hydrogen before the epitaxy process. The material can be produced with an active layer thickness range between 50nm and 5μm, although the standard thickness ranges between 100nm and 200nm. The oxide thickness range available is also of the order of the same range. Surface roughness is comparable to bulk.

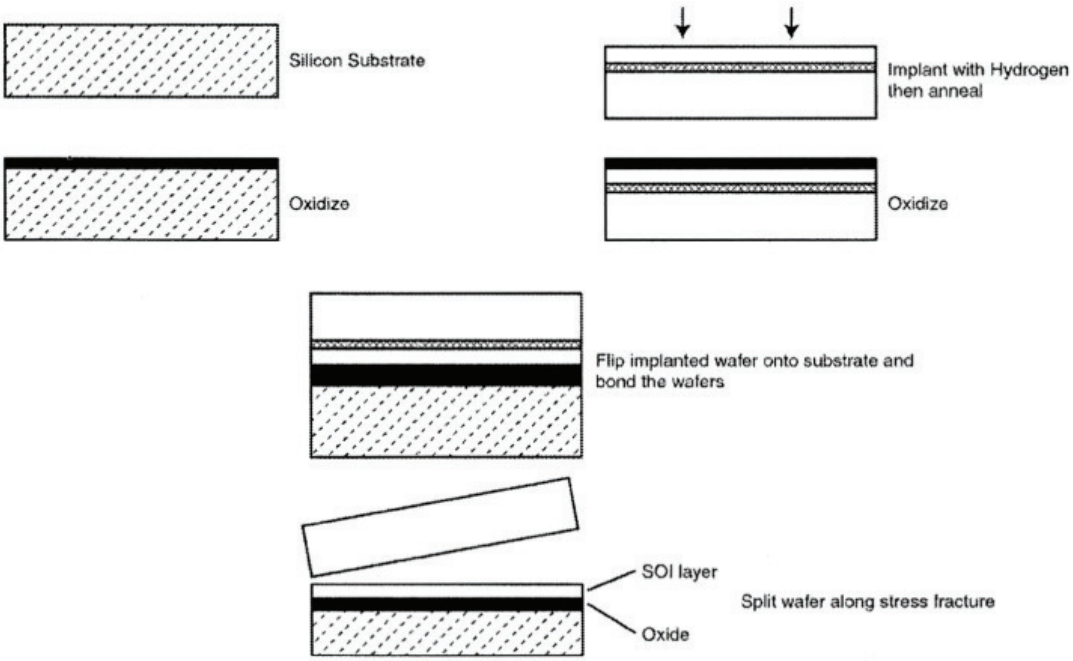


Figure 2.4: SOI wafer produced using the SmartCut® process. This process has the advantage of not wasting an entire wafer, as the split wafer can be re-used.

AcuThin

The AcuThin process uses a local dry etch process, using plasma assisted chemical etching (PACE) to obtain a uniform SOI layer. Measurements are made as etching proceeds, and non-uniformity is reduced through feedback of the local etch rates. With this technology better than 1% SOI thickness uniformity can be obtained [2.14].

The processing proceeds by bonding the substrate and active wafer. During processing the buried oxide thickness is determined by reflectance

Samsung Exhibit 1010, Page 33 of 204

measurement. Uniformity of the silicon on insulator layer is determined by the plasma characteristics and number of etching cycles. As the plasma area is reduced, and etching rate slowed, uniformity can be improved, at the expense of throughput.

Nanocleave

Nanocleave is an atomic layer cleaving process for bonded SOI [2.15], with a local surface roughness of less than the lattice constant of silicon (0.54nM). This SOI fabrication process is based on forming a cleave plane on an active wafer, using ion implantation. A bonded wafer pair is created with the active wafer. The bond strength of the donor-handle interface is higher than the cleave plane. The cleaving is done at room temperature using the force of a nitrogen jet. The resultant SOI wafer has an active silicon thickness within ±1% [2.16]. In this process the handle wafer can be silicon, glass or quartz, and the active wafer can have a layer of SiO_2, or be just silicon. The donor wafer is re-usable.

2.2.3 SOI Materials Summary

Various methods of producing SOI material have been presented. Some are more applicable to particular requirements than others. For example bonded techniques have the option of tailored resistivity for the support wafer, while the processing of SIMOX may provide a simple method to obtain mixed bulk, PD-SOI and FDSOI on the same wafer. For all methods there appear to be no fundamental restrictions on producing material up to or beyond 300mm wafers, and 200mm SOI is readily available. With several manufacturers now producing the material, it is becoming more readily available. As material costs reduce designers are considering SOI as a means to improve performance, without upgrading photolithographic equipment.

2.3 Comparison of SOI and Bulk

Designs in SOI benefit from reduced junction capacitance, reduced threshold voltage and improved I-drive. Threshold voltage reduction however is often at the expense of leakage. Process design usually accounts for this by matching worst-case leakage. This is usually considered to be at the strong process corner, high temperature and nominal supply voltage. Using this process corner for matching of the IDDQ leakage leads to I-drive gains throughout the operating range, while maintaining the maximum specification of leakage. It should be noted, however, that this method of device design normally results in a higher average leakage (figure 2.5).

2.3.1 Isolation Techniques

Bulk silicon processes use either junction isolation, or dielectric isolation. While both techniques are effective, junction isolation has the advantage of

low cost. However, it has the disadvantage of requiring a relatively large silicon area to isolate structures, since lateral diffusion of an isolation tank is about 70% of the vertical diffusion (figure 2.6). Sufficient vertical diffusion of a tank for a pMOS structure requires the tank to be diffused well below the deepest possible junction of the source and drain. For speciality MOS devices such as high voltage components diffusions may become substantial. With the reduction of feature sizes adding to the cost per square millimeter of silicon, the area lost to isolation becomes more significant with successive process nodes.

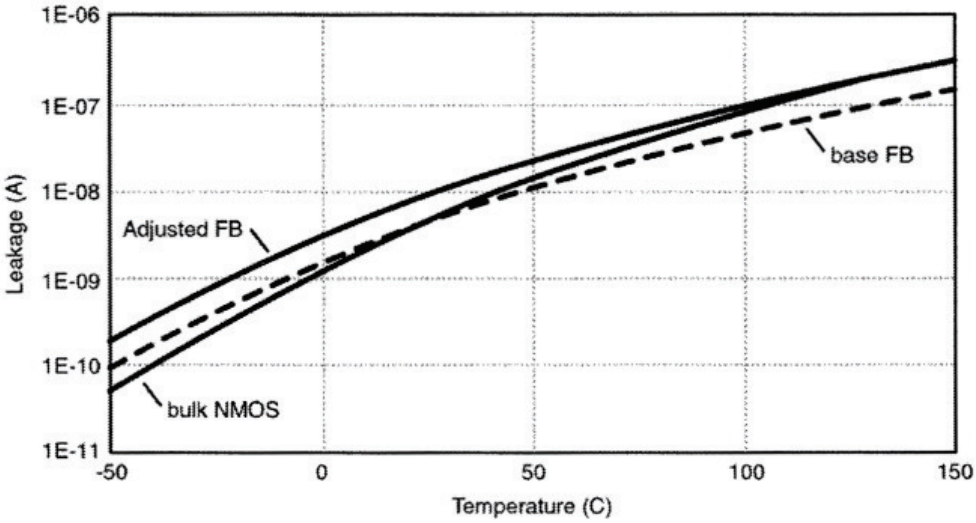


Figure 2.5: Drain-source leakage characteristics of SOI vs. Bulk. The bulk has a steeper leakage slope, so is normally lower leakage at room temperature and higher leakage at high temperature than its SOI counterpart. To maximize the performance enhancement of SOI it is common for the leakage of the SOI process to be adjusted, so it matches that of bulk at the high temperature limit.

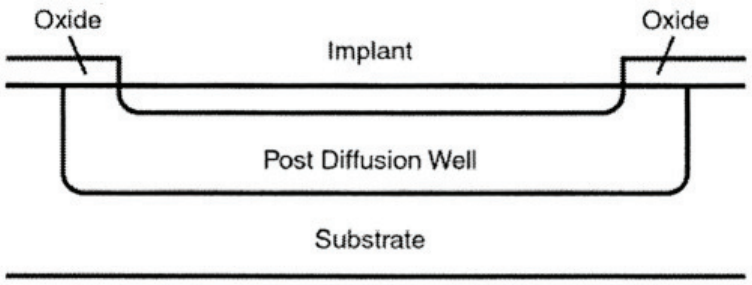


Figure 2.6: Diffusion of the Nwell or Pwell into which the MOS source and drain diffusions are made. For junction isolated schemes, the sideways diffusion of the dopant can add significantly to chip area.

Samsung Exhibit 1010, Page 35 of 204

In SOI, individual devices can be dielectrically isolated from each other using a trench-type isolation, resulting in isolation that is not susceptible to electrical latchup, and can be significantly more area efficient than junction isolation.

Figure 2.7 shows conventional bulk nMOS and pMOS structures in a junction isolated process. Figure 2.8 shows these structures in a dielectric isolated process, on a bulk substrate.

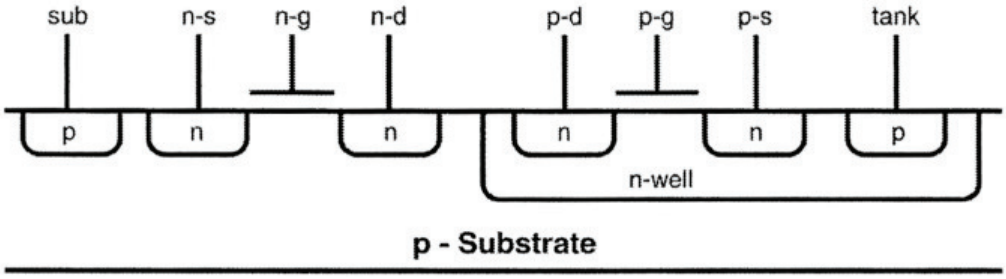


Figure 2.7: Simplified junction-isolated cMOS processed cross-section: The nMOS structure is generally constructed directly into the substrate or epitaxial material, and the pMOS normally is fabricated into an N-well diffused into the p-type silicon. The sources and drains are more heavily doped, shallower diffusions.

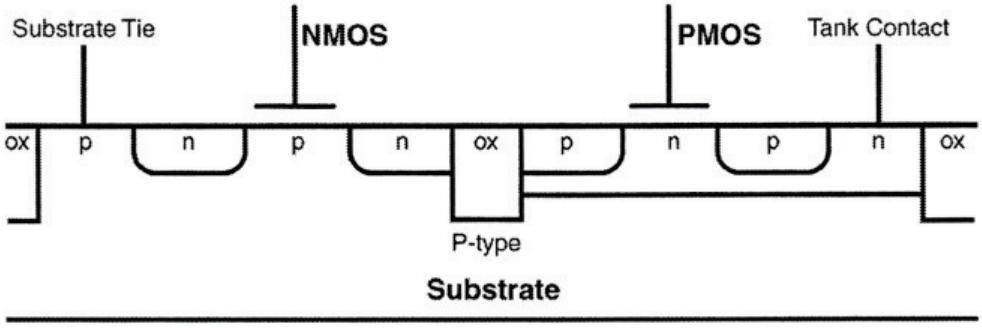


Figure 2.8: Simplified dielectric isolated CMOS process cross-section. Here the nMOS source/drains are diffused into a lightly doped P-type region, while the pMOS source drains are diffused into a lightly doped N-type region. Electrical isolation between structures is achieved with dielectrics, but the devices are electrically connected to the substrate either directly, or via a N-P junction diode.

The use of oxide isolation can result in a reduction of interconnect, source and drain capacitance, but body and local substrate contacts are still required. Figure 2.9 shows the basic SOI structure. This is similar to the oxide isolated bulk process, figure 2.8, except for the buried oxide or BOX

layer. The basic transistor changes from body tied (to ground for the nMOS, and usually to supply or source for the pMOS), to one where the body floats. This allows the parasitic bipolar device, which is in parallel with the MOS device, to be affected by switching conditions, allowing both the MOS and bipolar characteristics to modify device performance.

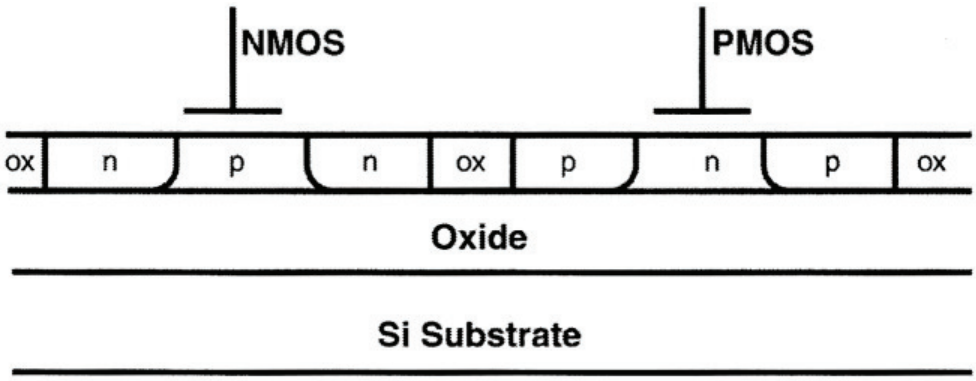


Figure 2.9: Simplified PD-SOI process cross-section: The nMOS source/drains are diffused into a lightly doped P-type region, and the pMOS source/drains are diffused into a lightly doped N-type region. Electrical isolation between structures is achieved with an oxide dielectric.

Source and Drain Doping Profiles.

The sources and drains of SOI devices have shallow junction depths compared to junctions in bulk material. The use of SOI results in a well-defined source/drain, which is relatively easy to maintain with technology scaling. This is not the case with bulk material, where junction scaling becomes more difficult as geometries reduce. Reduction in volume of the SOI source/drain does, however, tend to lead to higher resistance transistors than their bulk counterparts due to their shallower diffusions.

Partial Trench / Shallow Trench

There are several configurations that permit body ties through silicon. These are more area efficient than their metal connected counterparts, and may have advantages in reducing the effective body resistance, but normally require partial trench isolation and extra processing steps. A shallow, or partial, trench is achieved by adding an extra processing step that creates a trench in the active silicon which does not reach down to the buried oxide region. Their drawback is that the silicon under a shallow trench is usually fairly high impedance, thus not recommended for connections where low-resistance contacts are required. Partial trench may also be used to maintain thermal coupling between devices. The shallow or partial trench concept is shown in figure 2.10.

A degradation of the electrical characteristics of SOI devices with shallow trench isolation (STI), which depends on device size, is due to mobility decrease caused by interface roughness. The degradation is the result of plasma damage and can possibly be removed with a thermal oxidation [2.17].

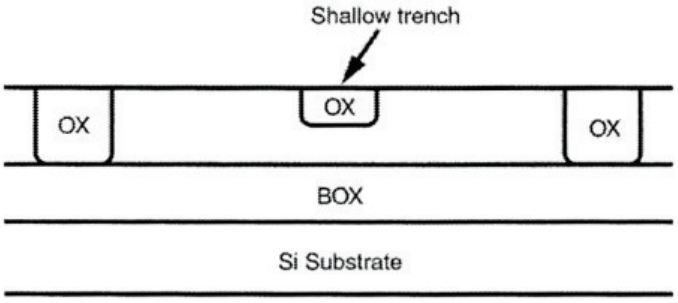


Figure 2.10: A shallow trench is created by etching part way through the active silicon and stopping before the buried oxide region is reached. This provides a resistive electrical contact between areas separated by the shallow trench, and a relatively good thermal contact between the regions.

Substrate Ties

Despite the active silicon being only capacitively coupled to substrate it remains normal practice to ground the substrate. This precaution prevents charge build-up on the substrate, which can affect transistor performance through the creation of a channel region in the body region, just above the buried oxide. A scheme to achieve a substrate tie in PD-SOI is shown in figure 2.11. In addition to connection to ground within the die, it is easy to connect the entire substrate to ground around the scribe line seal. This is area efficient since it is common practice to use a grounded metal ring at the outer periphery of many ICs.

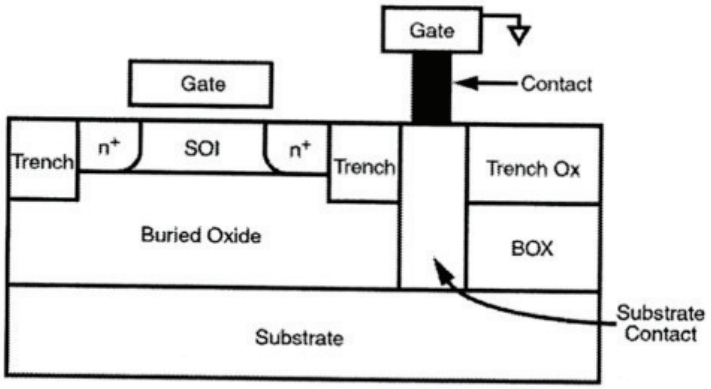


Figure 2.11: Method to tie the substrate to ground. This is achieved by etching through the active region and buried oxide. A substrate contact is included that extends from the substrate to the top of the active region.

Samsung Exhibit 1010, Page 38 of 204

2.4 SOI Technology Advantages

2.4.1 Capacitance Reduction

SOI devices have low drain / source to substrate capacitances, due to the buried oxide region, which replaces the junction capacitance of bulk material with oxide capacitance to substrate. Compared to some IC processes which use junction isolation, sidewall capacitance is also reduced. Mostly, reduction in source capacitance does not confer significant device performance improvement, although operating frequency improvements are observed in circuits where the source voltage varies, such as the upper nMOS device of a NAND gate, or when a source follower configuration is used.

Reduced capacitance of drain to substrate (or drain to tank in a pMOS) provides performance enhancement, although it does not provide a benefit in certain source-follower configurations. The reduction in source/drain capacitance usually provides incremental speed improvement, or conversely power reduction. However, reduced capacitance can also be a disadvantage. Supply noise is reduced in bulk material as a result of the large pMOS tank to substrate. This capacitance is not present in SOI material.

2.4.2 Reduced Short Channel Effect

Short channel effect increases as channel lengths are reduced. This compromises the threshold voltage and leads to increased device leakage. The threshold voltage roll-off decreases as substrate bias increases. Since the bodies of PD-SOI devices float, this tends to negate the short channel roll-off effect [2.18]. However, threshold voltage may be degraded in short channel floating body devices due to impact ionization [2.19]. The dominant mechanism depends on process, layout and operating conditions. PD-SOI can utilize many techniques used in bulk CMOS for controlling short channel effect, such as retrograde wells and pocket or halo implants. Controlling short-channel effects is a challenge as device channel lengths are scaled below 100nm. For bulk silicon, the method used to contain short channel effects is through careful design of the dopant profiles [2.20 - 2.22].

2.4.3 Lower Vt Device Threshold

Unless adjustments to processing are made, SOI features lower threshold voltage (Vt) compared to bulk. It is therefore normal practice for threshold adjust ion implants to be modified to achieve a similar threshold voltage for PD-SOI and bulk, to maintain similar drain-source leakage levels. Without threshold voltage correction drain-source leakage may become excessive, especially at high temperatures.

Samsung Exhibit 1010, Page 39 of 204

2.4.4 Soft Error Rate (SER) Effects

One benefit recognized early in the development of SOI has been reduction in memory soft-error rate resulting from cosmic rays and background radiation. SER is a greater concern in small area memory cells, where there is less charge to disrupt. With the sizes of all types of memory cells reducing at a rate close to that of process feature size reductions, any advantage that can be gained from reduced SER is significant. In addition, soft error immunity (radiation hardness) of SOI devices is important for high data rate network servers and global data transfer links [2.23]. SER is discussed in more detail in chapters 8 and 9.

2.5 Performance

There continues to be considerable debate surrounding the benefits of SOI, and questions of scalability. This is largely due to difficulty in obtaining direct comparisons between SOI and bulk. The floating body gives different levels of benefit depending on the circuit being tested, operating conditions such as supply voltage and temperature, and history of the signals to the circuitry being compared. In addition, performance also varies depends on the comparison point of device leakage. If circuit leakage is normalized to nominal operating conditions the result is very different to circuit leakage being normalized to the high temperature, high leakage corner. However, SOI appears to provide better performance than bulk material in virtually all cases, so additional processing costs aside, SOI appears to have a future.

When compared to bulk, MOS devices fabricated on SOI have lower capacitances from source to substrate and drain to substrate, but with many devices, interconnect capacitance contributes significantly to total capacitance. Therefore reductions in drain and source capacitance observed in the move to SOI are not as significant as initial appearances might suggest. Circuits exploiting the reduced reverse body effect in SOI obtain approximately 15% performance enhancement compared to bulk, but added design margin required due to history effect may take away much of the advantage, unless care is exercised in design. Differences between SOI and bulk are given in table 2.1. Metal and poly-silicon etches may need re-tuning between bulk and SOI processes due to different etch rates on SOI and bulk. The yield of bulk silicon is the same as that of bonded wafer SOI and SIMOX material.

Gate lengths of planar CMOS transistors on bulk silicon are not expected to reduce much beyond 50nm [2.16]. According to some reports a 20-50% increase in transistor speed can be achieved by switching from bulk material to SOI [2.24, 2.25]. This improvement represents one to two generations of scaling, without the cost of higher resolution lithography [2.16].

Circuits built on SOI are more versatile than those on bulk because the buried oxide can be used to optimize scaling [2.26]. As devices are scaled source/drain capacitances begin to dominate gate capacitance. However, as this occurs interconnect capacitance becomes more significant in defining overall chip speed, moving the focus towards improved drive currents and a combination of reduced interconnect capacitance and resistance as the most important performance drivers. Library cell layout can be between 10 and 30% more compact with SOI because nMOS and pMOS devices may be randomly placed, since there are no dielectric isolation requirements for SOI.

Table 2.1: Principal benefits and disadvantages of SOI vs. bulk material

Principal Benefits of SOI:

- Reduced drain and source capacitance, resulting from oxide isolation rather than junction isolation techniques.
- Reduction in the "MOS reverse body effect" in stacked transistor devices.
- Performance enhancement due to floating body effects, particularly in stacked components such as the upper nMOS devices in NAND gates, where a floating body replaces a body biased at lower than the source voltage.
- Marginally reduced device area may lead to a reduction in metalization capacitance, and slightly reduced die area, and layout of library cells are more compact with SOI because nMOS and pMOS devices can be randomly placed.
- Improved latchup, noise and current immunity through the substrate
- Improved high temperature performance (lower device and parasitic leakage)
- Improvements to passive components – Inductor Q improvement, parasitic capacitance reduction
- Reduced capacitance from substrate to metal interconnect.

The primary disadvantages of SOI are:

- Self heating
- Reduced supply to ground capacitance for noise reduction on the supply rail.
- Undesirable kink effect (chapter 10) in analog applications
- Floating body can lead to increased drain-source leakage (transient and DC)
- Floating body can lead to high or excessive gate to body voltages, with potential reliability issues
- History effect complicates design, and requires greater design margin in many cases.

2.6 Partially and Fully Depleted-SOI

The depletion region of partially Depleted (PD) SOI does not reach through the entire silicon channel/body region. PD material usually has a silicon thickness greater than 0.15μm. Claimed performance benefits of using PD-SOI compared to bulk range from 7-11% to 20-35% over similar bulk

material [2.27]. Actual comparison is difficult due to the non-exact equivalence of bulk to SOI in terms of optimum transistor design.

In the early 1990's SOI was hampered by poor material quality. SOI still has to be measured against the continuing scaling achieved in bulk. Over the last few years SOI material quality has improved and bulk scaling appears to be reaching a point where improvements can only be made at greater costs. This makes the improvements gained from the use of SOI relatively more cost effective. PD-SOI is easier to manufacture than fully Depleted (FD) SOI due to its relatively thicker substrate [2.28].

PD SOI devices display the 'kink effect', a circuit behavior not present in bulk technology, which also reduces further as the active region reduces, to the extent that it can be eliminated in FD-SOI. The kink effect is caused as a result of the floating body. It has the beneficial effect of higher drive current for digital designs (chapter 3). The floating body also gives rise to "history dependence", causing different switching rates on subsequent switching edges. In PD silicon, "pass-gate leakage" can occur, and is a result of the body voltage floating to a point where the parallel, parasitic bipolar transistor associated with most PD MOS devices, can turn on.

Partially Depleted SOI is often considered to be an evolutionary advance in process development, as the topology is essentially the same as bulk, with the exception that bulk does not have the oxide layer. In many analog and transmission-gate logic applications floating body effects are unacceptable. In these cases a body contact can be added to PD-SOI, although body contacts are resistive, and may not be very efficient at high frequencies. It is not realistic to add a body contact to FD-SOI, since there is no guarantee of a body region being available under most operating conditions.

The body potential of a floating body PD-SOI device depends on switching history, circuit topology, component, chip temperature and supply voltage [2.29]. This may vary typically by approximately 8% faster or slower than a nominal state. As a minimum, test routines are required to force the body voltages to the extreme delays. This approach however, can cause over-compensation, resulting in excessive margin. Minimization of design margin is discussed in chapter 6.

Variations in the floating body voltage of PD-SOI MOS transistors causes an uncertainty in the gate-source threshold voltage. This in turn reduces the noise margins for dynamic and memory circuits [2.29]. As noise margin is reduced, additional attention must be paid to dynamic circuit and memory design. Predischarging can be used to force floating nodes into a known

state, to improve noise margin. This discharges body nodes of indeterminate voltage (chapter 10).

The use of fully depleted silicon on insulator material has been proposed as a way to minimize floating body effects. For FD devices, the SOI film is far thinner than the device depletion width (a few nanometers to a few tens of nanometers). Thus there is no body region of the MOS device that can be charged. With no floating body, FD does not exhibit significant kink or history effects.

It may be assumed that fully depleted MOS transistors lend themselves more readily to analog implementations, as they do not have the kink and history effects of their PD-SOI counterparts. However, PD-SOI is more difficult to manufacture, and threshold voltage control, together with matching difficulties may occur due to 2-D field fringing. Devices on FD-SOI display a steep sub-threshold slope, with low parasitic capacitances, making them appropriate for low-voltage, low-power applications. A significant advantage of FD circuits is that for the same bandwidth they typically consume only about half the power of their bulk counterparts, alternatively, bandwidth may be improved a given power dissipation. Table 2.2 shows differences in PD and FD-SOI characteristics.

Table 2.2: Comparison of the component differences between Partially Depleted-SOI and Fully Depleted-SOI

	PD-SOI	**FD-SOI**
Floating body	yes	no *
Active Silicon Thickness	>0.15μm	<0.1μm
Kink effect	yes**	no
History effect	yes	no
Source/Drain resistance	moderate	high
Manufacturing	reasonable	difficult
Power	low	very low

*Floating body is not present in the saturation region of operation
**Kink effect is suppressed in some operational states

Many device and circuit performance related limitations are postponed or eliminated for CMOS fabricated on very thin SOI. In bulk material the control of very shallow MOS source/drain junctions is difficult due to limited thermal budgets [2.30], but with SOI material junctions are determined by the thickness of the active silicon [2.16].

Samsung Exhibit 1010, Page 43 of 204

The term 'Ultra-thin' film SOI is usually used to refer to material with an active silicon thickness in the range of 20-50nm, although functional transistors on an active silicon thickness of just 1nm have been demonstrated [2.26]. In such devices, thickness-related effects on carrier mobility and threshold voltage become important. At thicknesses of 1nm, devices are quantum mechanical in nature, and the structures behave as quantum wells (chapter 13).

Here we consider mostly PD-SOI circuits, rather than FD-SOI, due to the clearer applicability of PD-SOI at this time, and also the particular challenges of designing with PD-SOI. PD-SOI will likely dominate through the 50 to 70nm gate length generation, and will therefore be used by mixed signal designers for a number of years. FD-SOI may follow with two different gate electrodes. This is because the mobility of double gate devices is close to 4x that of single gate structures as a result of electric field effects. Although mostly described with an emphasis on PD-SOI, many of the process effects, thermal effects and some of the circuit techniques, are applicable to FD-SOI. FD-SOI gives more improvement in circuit speed and soft-error immunity than PD-SOI [2.16], and also permits a reduction in power requirement.

Thick film SOI (SOI material that has an active region that is thicker than about one micron) is used mostly for power integrated circuit applications, RF bipolar applications, MEMS and opto-electronic devices. Floating body CMOS devices designed for thick film SOI exhibit similar floating body effects to PD-SOI devices, although due to the additional thickness, the parasitic bipolar is less affected by depletion caused by the source/gate/drain of the MOS structure.

2.7 Technology Scaling

Scaling device dimensions has been used as a fallback method to improve device performance. It has proved highly successful as patterning technology has improved ahead of the processing requirements. However, as simple scaling has proved more difficult to achieve, additional process improvements have been required to maintain the trend of matching the Moore's Law curve. This includes combinations of the best improvements from all areas of IC production [2.31].

SOI processes also make use of the process improvements that have occurred during the last few years, including high-performance CMOS logic technology where gate lengths are measured in the tens of nanometers, together with multi-level copper [2.32] and dual-damascene interconnects with low dielectric constant (low-k) intermetallic material [2.33].

Samsung Exhibit 1010, Page 44 of 204

When high velocity carriers flow from source to drain, impact ionization induced electron-hole pairs are generated. The threshold that impact ionization occurs depends on many device characteristics, including gate oxide thickness, doping profile and supply voltage. Impact ionization causes hole charging of the body, which reduces with gate length scaling. However, while impact ionization reduces, gate leakage increases due to the thinner gate oxides, which are required for the shorter channel lengths. One solution to reduce gate leakage is to use high dielectric constant (high-K) gate dielectrics, though this has limitations. Parasitic bipolars can be tuned to minimize device gain. This is achieved through a combination of source doping and channel doping to reduce emitter efficiency and gain. There is general agreement that SOI provides an improvement in terms of operating frequency for digital applications over bulk at technologies down to gate lengths of between 50 and 100nm. However, there has been some debate on the level of scalability of PD-SOI with future technology generations [2.34 - 2.36]. This stems from the reduced role of junction capacitance in the obtainable improvements, and the possibility of increased history effect with device scaling. (Increased history effect leads to the possibility of over-designing to guarantee circuit functionality and hence a loss of much of the expected SOI performance improvement).

2.8 SOI Device Properties

2.8.1 Source/Drain-to-Substrate Capacitance

Devices built on SOI have lower source-to-substrate and drain-to-substrate capacitances than bulk silicon [2.37], due to the oxide layer between source/drain and substrate. These junctions are not diode-like in behavior in SOI, which eliminates the possibility of forward biasing the node to substrate or to the tank (in the case of the pMOS device). High-resistivity SOI substrates, used for high frequency applications, further reduces these capacitances. At low to moderate frequencies capacitances to substrate may not need to be included in simulations, but at higher frequencies, above 500MHz to 1GHz, specific substrate capacitance modeling is usually required [2.38].

2.8.2 Gate Leakage

Along with shorter gate lengths there is a trend to reduced gate oxide thickness. This results in increased gate leakage, due to tunneling. When thin gate oxides are combined with SOI the body voltage is affected in some conditions. Leakage may not cause significant effects in simple inverter circuits, since when a large potential is present across the gate and body of a device, the device is usually in the 'on' state. However, there may be some effects on stacked stages, such as the upper MOS of a stacked scheme, as

Samsung Exhibit 1010, Page 45 of 204

found in NAND or NOR gates, and also in transmission gates (chapters 6 and 7).

The gate leakage mechanism is described by tunneling [2.39], providing a leakage that is not greatly affected by temperature. Thus there may be little noticeable effect on circuit operation of relatively gate-leakage-tolerant circuits at room temperature or higher. The impact at lower temperatures, however, becomes significant, when gate leakage may dominate other sources of leakage that do scale with temperature. This is of particular concern in such circuits as loadless four-transistor (4T) SRAM cells, where gate leakage contributes to a significant proportion of the overall leakage. Gate leakage is an important consideration in analog designs where charge storage is required (chapter 10). Gate leakage is usually low enough that static logic operation is unaffected for bulk designs, but in many other circuits gate leakage may be problematic, and requires consideration when transferring a bulk design to SOI.

Gate leakage depends on the voltage gradient across the oxide. For nMOS devices gate leakage reduces the body potential if Vgb is below zero, and increases it if the Vgb is above zero. In terms of switching sequence for a nMOS device in an inverter, the starting condition can be with the gate at either zero volts or the supply voltage. If the starting condition is zero volts on the input, then the body of the nMOS will drift to a few tenths of a volt, as a result of the drain-to-body and body-to-source leakage. Under these conditions tunneling between gate and body is very low, and has a minimal effect on the starting condition.

If the starting condition is an input state of Vdd, the effect of gate leakage is to increase body voltage from the expected value of 0V, to a value that can be several tenths of a volt above ground [2.40]. As switching occurs, drain capacitance tends to dominate the switching effects on the body, raising the voltage still further. The overall effect is an increase in history effect, together with a marginal increase in frequency.

2.9 Body Effects

2.9.1 Bipolar Effect

Figure 2.12 shows the bipolar structure of a PD-nMOS. The base of the parasitic NPN is not connected, but capacitive switching and leakage effects can combine to increase the base voltage sufficiently that the structure could turn on. An example of NPN turn-on is readily seen when the nMOS source and drain are high (e.g. in a transmission gate), the body drifts high (neglecting gate leakage), until source, drain and body are at the same

Samsung Exhibit 1010, Page 46 of 204

potential. Assuming that the gate remains low during this time the circuit configuration is in the 'off' state, and does not draw current. If the source is then pulled low, the base is pulled down due to the base-emitter (body-source) diode turning on. The body voltage will initially be at about 0.7V higher than the source. The result is that the parasitic NPN will turn on for a transient period, until carriers are swept from the base region. This can take many picoseconds, during which time current is being drawn from the drain (collector) region. It is important to consider this effect in several circuit configurations, and circuit designs have been proposed to address this effect (chapters 6 and 7).

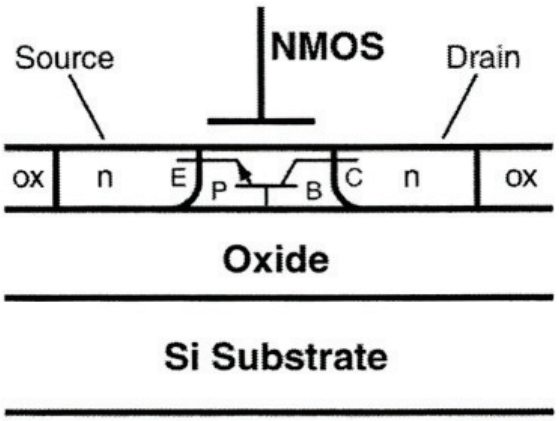


Figure 2.12: The parasitic bipolar device of a PD-nMOS. Unlike in bulk silicon, the body of the bipolar is floating, and can be turned on through capacitive coupling.

When power is supplied, or when there is either input or output state change to a PD-SOI component, the body voltage can be perturbed by capacitive coupling. The time taken for the body to settle back to its steady state value ranges from a few microseconds, to a few milliseconds. During this time Vt and Idrive can change. This can seriously impact digital and analog circuits, and can also significantly increase the initial parasitic leakage current (although once steady state body bias is reached, leakage current will settle to the expected value). This is discussed further in chapters 6 and 10.

2.9.2 Kink Effect

The "Kink Effect" is observed once impact ionization begins. This effect is the result of an abrupt saturation current increase in the strong inversion condition. It is mainly caused by an increase in body potential due to carrier generation caused by impact ionization. The rise of body potential is accentuated in thin depletion layers because the lateral field is stronger and the recombination region is restricted [2.41]. The effects of this phenomenon can be used to advantage in digital designs to improve performance. The

Samsung Exhibit 1010, Page 47 of 204

kink in the output current curve (figure 2.13) shows where the drain to source leakage current is boosted, and is observed in PD-SOI, but not in bulk devices. It is detrimental to the design of analog circuits, and most analog designs avoid operation of SOI devices in the region where the kink effect occurs.



Figure 2.13: Graph showing the kink effect. As source-drain voltage is increased, the output current passes through the impact ionization threshold region, and output current is boosted.

As operating frequency increases the kink effect is suppressed [2.42]. It has been suggested that this may be beneficial when designing RF circuits for SOI applications [2.43]. Other work suggests that for optimum PD-SOI device performance in RF applications the use of body-source tied devices is necessary for lowest noise [2.44], and that parasitic bipolar contributions should be minimized.

The large output swings and matching requirements of high speed operational amplifiers, analog-to-digital converters, and a variety of other analog circuits still necessitate the removal of the I-V kink. In some cases body contact structures are used, but body contacts are not ideal due to the high resistance of the body region and resistance variability with body bias. Other circuits make use of circuit biasing to operate outside the kink region. The low-frequency noise overshoot has been correlated to frequency dependence of the kink-related noise in SOI FETs, even when the devices are body-tied [2.45].

The kink effect observed in PD-SOI can be minimized through process optimization (minimizing the bipolar gain and leakage), and/or by layout design (such as adding body ties). Body ties can be source or ground (or supply) connected. Body to source ties have specific layout requirements, to maintain low resistance, for example 5μm maximum between body ties. For

Samsung Exhibit 1010, Page 48 of 204

body tied structures it is normal, though not universal, practice to contact both ends of the body region (figure 2.14). This is because the double contact effectively reduces the body resistance by a factor of four compared to a single resistive contact at one end of the body.

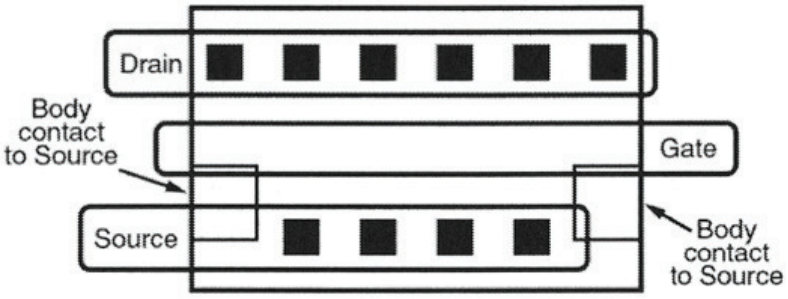


Figure 2.14: Body contacted nMOS device, showing typical body contacting sites. Maximum spacing between body contacts is determined from the body characteristics and MOS transistor leakages.

At drain voltages, a secondary kink can occur, attributable to the lateral parasitic bipolar device turn-on. This occurs at the point when the body is sufficiently forward biased to allow the bipolar device to turn on. At this point the parasitic and MOS devices are conducting in parallel. This becomes less significant as supply voltages reduce below 1.5V.

2.9.3 Capacitive Body Effects

Perhaps the single most significant feature of MOS devices on SOI, compared to bulk, is that the SOI body is connected electrically to the substrate through a capacitance (insulator of the silicon-on-insulator). The junction in bulk material is capacitive in negative bias, and behaves as a diode with positive bias. Studies have compared circuits and devices on bulk to fully and partially depleted SOI [2.46-2.48]. In bulk silicon the nMOS body is typically substrate, and therefore directly connected to ground. The pMOS is normally built in an N-type well, which makes a PN junction to substrate. The construction of MOS devices in bulk silicon can lead to the production of a highly efficient PNP structure to substrate, consisting of the pMOS source or drain, N-type tank and P-substrate. This PNP must be maintained in the 'off' state to prevent excessive supply-to-substrate leakage. Figure 2.15 shows the parasitic transistor of bulk integrated circuits. The floating body in SOI is capacitively coupled to the substrate. The body voltage of a SOI device is determined by rapid transient switching of the source, drain and gate, and their associated leakages. Capacitive coupling between gate and drain to the floating body leads to the so-called 'history' effect, where the response to device switching is dependent upon earlier switching events.

Samsung Exhibit 1010, Page 49 of 204

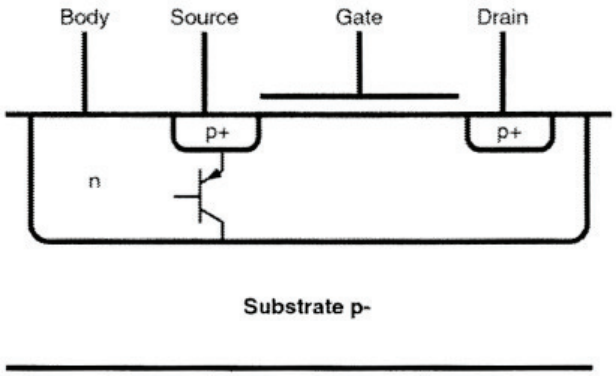


Figure 2.15: A parasitic transistor is created in bulk ICs by a pMOS source or drain, the N type diffusion for the pMOS well acts as the PNP base and the substrate is the collector.

With any type of circuitry converted from one technology to another, even when it is merely from one bulk process node to the next, the most challenging aspect of the transfer is a complete understanding and characterization of the new circuit behavior. This is generally achieved through modeling and silicon analysis. With conventional redesign, process adjustment is largely limited to the various advances made resulting from shorter channel length devices, such as Idrive improvements, changes to parasitics, and supply voltage reduction. The technology transfer from bulk to SOI is vastly more challenging, largely due to the floating body behavior of SOI.

Figure 2.16 shows the circuit elements that contribute to the body voltage of a device built in SOI. The DC component of body voltage is determined by the p-n diode leakages of body to source and body to drain. The body to drain current includes impact ionization current and gate induced drain leakage. In addition, there is the possibility of gate leakage current resulting from tunneling through gate oxide. The AC component of body voltage is determined by capacitive coupling during switching, in particular the gate to body coupling (Cgd) and drain to body coupling (Cdb). The Source to body capacitance (Csb) attenuates some of the body coupling in most circuits. Time constants for the leakage currents can be in the order of milliseconds, whereas response time of capacitive coupling is instantaneous.

Gate thickness continues to be scaled with technology generations. Thin gate dielectric is important in maintaining performance at reduced supply voltages and in controlling short-channel effects. With very thin dielectrics, especially at reduced temperatures, gate tunneling current dominates over other leakage mechanisms. Part of the tunneling current is between body and gate, affecting body voltage [2.40].

Samsung Exhibit 1010, Page 50 of 204

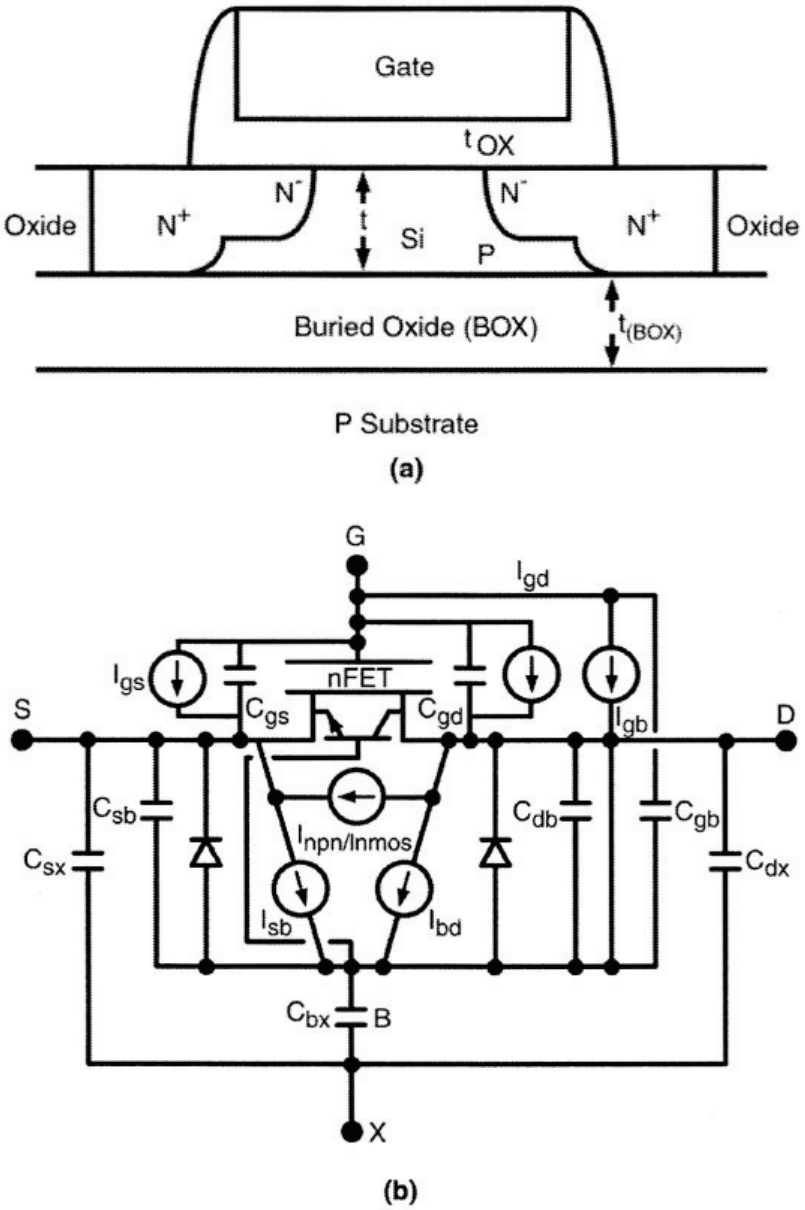


Figure 2.16: Cross section and equivalent parasitic components associated with the nMOS structure in PD-SOI. Note the body voltage is determined from DC leakage to drain, source and gate, and AC coupling to gate, source, drain and substrate.

Floating-body effects depend strongly on supply voltage. The baseline (DC) body voltage depends on leakage and the AC perturbation of the DC value is capacitance driven. Thus as supply voltage is reduced, floating body effects are also reduced. The kink effect gives rise to reduced MOS resistance at high Vds conditions, improving the efficiency of the structure.

A significant 'floating body' effect is the MOS device's dependence on past switching events. History dependence (or history effect) is the effect of switching history on gate delay [2.49]. As the input pulse train changes, delay through the gate changes. In the DC state the body voltage is determined by leakage through the drain, source and gate, and by impact ionization.

2.10 Body Ties

Additional variation of the threshold voltage in PD-SOI (compared to bulk CMOS) is attributable to floating body effects. There are instances where effects caused by the floating body cannot be tolerated, particularly in circuits previously been used for designs on bulk silicon. In other cases, however, such variation is merely a minor inconvenience or may even be beneficial. In most designs, especially those specifically for SOI, the variation of threshold voltage can be used to advantage, permitting faster turn-on for circuits, without increasing leakage current.

Body ties [2.50] can be achieved in a number of ways and applied to a variety of applications [2.51]. They have been designed to minimize or eliminate floating-body effects and effectively suppress DC effects. However, they are not as effective as devices constructed using bulk material in eliminating body transients in AC conditions, since the body charge and discharge time may have a time constant much longer than the transient. In order to verify effective body tie design, dynamic charging due to the body resistance and capacitance must be included in simulations. Depending on the type of circuitry and frequency of operation, this can be as simple as adding a lumped equivalent for body and gate resistance, or can require more detailed simulation of the resistive and capacitive effects.

For some analog applications it is permissible to use more complicated or expensive device engineering mechanisms [2.52]. The body tie has some advantages, but carries a die area penalty [2.53]. It is effective under DC conditions, but body potential is affected by fast switching transients, and is not well regulated at high frequencies, where gate, source and drain capacitances form a distributed resistor-capacitor network to the body contact, allowing the body to be perturbed by the switching MOS device. In many analog designs threshold voltages must be closely matched. This can be achieved through the use of body ties [2.54] which may be:

(1) tied to source (figure 2.17(a)),
(2) tied to ground (figure 2.17(b)), or
(3) coupled to another device that requires matching [2.54] (figure 2.17(c)).

Samsung Exhibit 1010, Page 52 of 204

In addition transient techniques can be used such as precharging or predischarging.

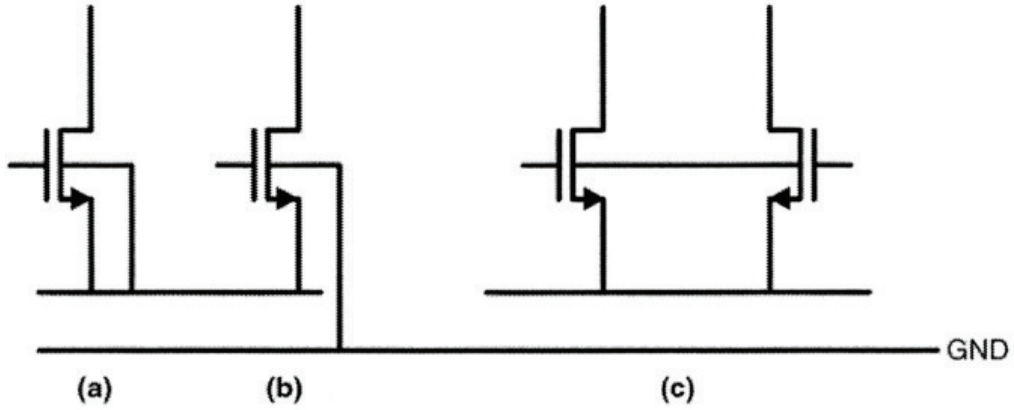


Figure 2.17: (a) Body tied to source configuration. This is the most area efficient form of body tie for most SOI. (b) Body tie to ground. This matches the body of most bulk nMOS structures. (c) Body tied to body - used where two bodies need to be maintained at the same potential but may float.

Body contacts provide a means to maintain the body at a known potential, and allow modulation of the body voltage. Body modulation can be used to improve performance through the application of a voltage to the body that is closer to the parasitic bipolar turn on potential. Positive body modulation reduces device threshold voltage, which can be a useful circuit design technique. In addition to using body biasing for improved performance, the body can be biased to provide lower IDDQ or quiescent currents, biasing the body to a more negative potential than the source (for nMOS), or to a more positive potential than the source (for pMOS).

The resistance along the body is normally tens of kilo-ohms per micron width. Depending on processing, the body resistance may not reduce much with increased gate length, due to the body diffusion profiling. If the body tie is to source, the capacitance between drain and body must be considered in the overall efficiency of the body tie, although the parallel body to source capacitance will help stabilize body voltage. If the body tie is independent of the source, both body to drain and body to source capacitances should be included in the calculation of body effect. There is also body to gate capacitance to be considered when the device is off, and body to channel effect when the device is on.

In general capacitances affecting the body voltage vary with process. It is desirable to include the distributed effects in simulations, to determine the effectiveness of particular body tied configurations. Figure 2.18 shows the

Samsung Exhibit 1010, Page 53 of 204

resistance and capacitance coupling of a body tied to source, and figure 2.19 shows the resistance and capacitance coupling of an isolated body tie.

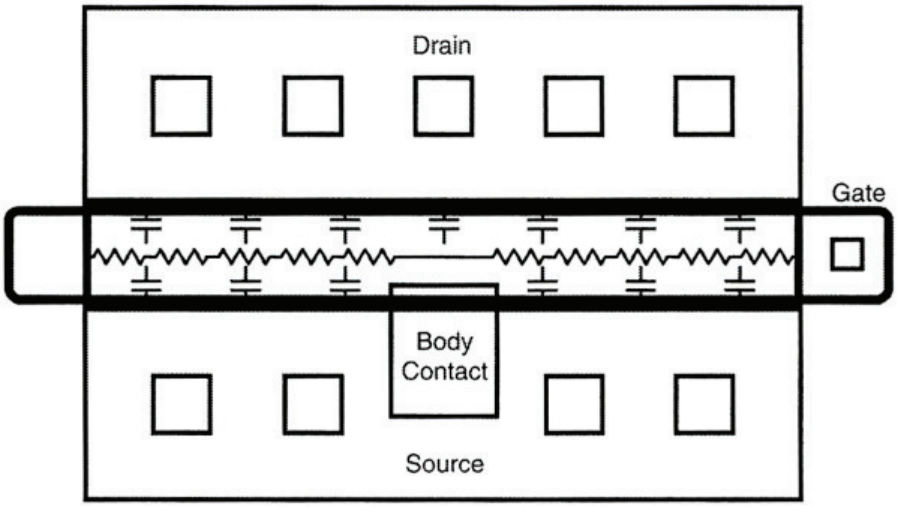


Figure 2.18: Representation of body resistance and capacitance of a body to source tied body contact (BC). The body resistance is many kiloohms per micron gate width, thus at high frequencies, or during fast transients the local body voltage may be perturbed from that of the body contact.

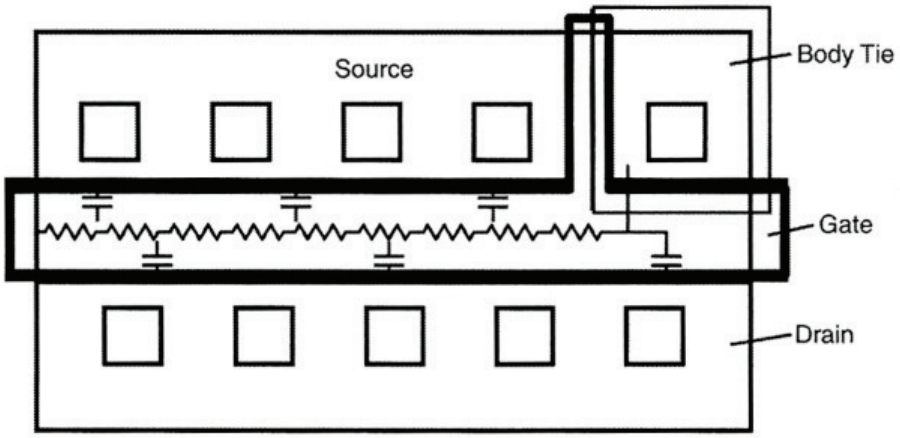


Figure 2.19: Representation of body resistance and capacitance of an independent body tied contact. The distributed body resistance causes local body voltage to vary from the contact potential.

2.10.1 Body Tied to Substrate

An area efficient variant of the body contact is the Low-Barrier Body-Contact (LBBC) Scheme [2.55]. Here a low barrier body contact is created under the source or drain region, to facilitate collection and removal of current carriers generated by impact ionization. Reduced flicker noise (compared to floating body devices) is claimed, making them useful for

Samsung Exhibit 1010, Page 54 of 204

analog applications. The scheme is more efficient for substrate current collection compared than conventional SOI contact schemes, but may be somewhat more difficult to implement.

2.10.2 Body-tied to gate Configurations

The body-tied-to-gate transistor has been proposed for a number of designs, especially high-speed digital applications [2.56]. This configuration has the effect of increasing drive current in some cases, but it has disadvantages, the most significant being that the gate voltage is limited by the parasitic bipolar transistor. As gate voltage is increased, the base-emitter (body-source) voltage becomes forward biased, limiting the voltage that can be applied between gate and source (figure 2.20).

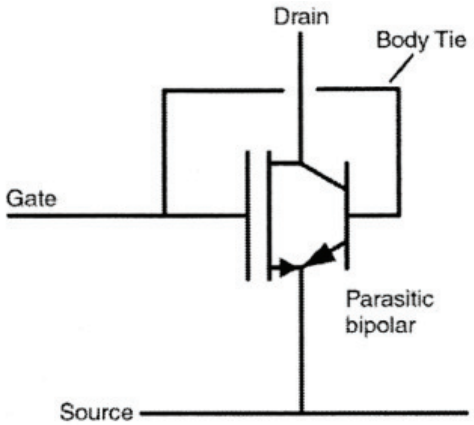


Figure 2.20: Base-emitter forward biasing caused by a direct gate-to-body tie. This can be alleviated with the use of a current controlled connection, or a voltage level shifter.

A further limitation of this configuration is that the circuit driving the gate-body tied input sees a higher capacitance than if it were just driving a gate (figure 2.21). The conventional gate configuration of a nMOS sees capacitance of the gate to source (GS), gate to drain (GD) and gate to body (GB), initially, and after reaching the threshold voltage this will become GS + GD + gate-to-channel (GC) capacitance. The gate to body tied device however, sees GS + GD + body to source (BS) capacitance + body to drain (BD) capacitance, in addition to the smaller body to substrate (BSU) capacitance. As gate voltage is increased beyond the threshold voltage, the input capacitance becomes GS + GD + GC + BS + BD + body to channel (BC) capacitance + BSU. Hence the body tied to gate configuration becomes viable if gate voltage does not change significantly, or if the gain in output current (from the similarly constructed previous stage) is higher than the extra capacitance that needs to be driven.

Samsung Exhibit 1010, Page 55 of 204

An additional issue is that the body resistance changes with gate bias: As gate bias increases the depletion region increases. Under these conditions body resistance becomes higher than the condition where the gate is at the source voltage.

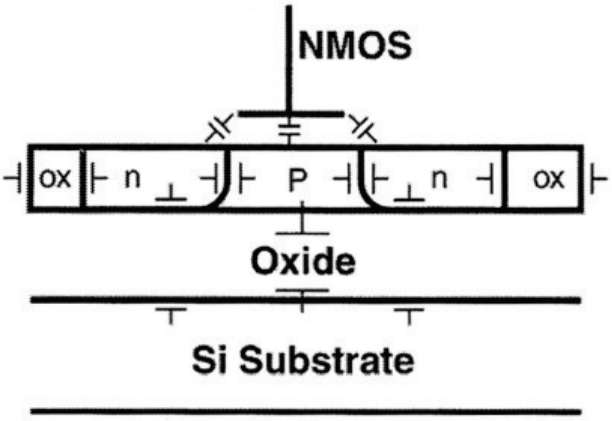


Figure 2.21: Parasitic capacitances associated with the gate and body of an SOI device.

2.10.3 Resistive Body Tie

A variant of the standard body ties the body resistively to a bias potential (often source or ground). This gives a DC state that returns relatively quickly to the source or ground voltage, to avoid high off-state leakage, but permits AC switching to modulate the body voltage for improved transient switching performance. A layout option for this is shown in figure 2.22. As distance from the body contact, along the width of the transistor increases, coupling reduces, allowing capacitive switching to more easily perturb the body voltage. In principle this may offer some advantages of improved operating Idrive, while minimizing off-state leakage. However, if the body resistance is particularly high, impact ionization can pull the body voltage up, even with just a DC bias. This increases leakage, and causes a low threshold voltage region of the device.

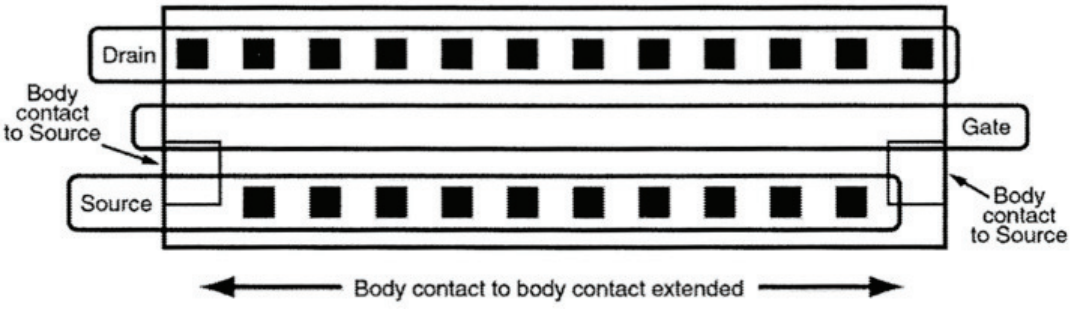


Figure 2.22: Widened body contacts allow the center of the PD-MOS device body voltage to move with capacitive coupling.

Body Pre-Charging and Biasing

There are several options for biasing the body to a known potential. The simplest implementation, in terms of circuit design, is that of body tied to source, or body tied to the appropriate supply or ground. These options do not utilize the full capabilities of the SOI devices, though they do tend to minimize leakage.

Pre-charging of the body has been proposed, and is discussed in chapter 10. This technique uses the fact that charging the body with a known current will raise the body voltage to a forward biased diode level. Thus the body voltages of two or more matched devices can be equalized prior to a measurement being taken.

Applications of body tied to unlike body

Another body tied approach, which is applicable to low voltage applications, is to tie the body of a nMOS to the body of an associated pMOS, such as the nMOS and pMOS of an inverter. This may have certain advantages at sub 1V operation, but is unlikely to be used above 1V. The reason is that in this configuration, two forward biased diodes are formed.

The temperature coefficient of the on-state forward voltage drop (Vf) of a junction diode is about -1.8mV per °C. Since Vf is typically quoted as being around 0.7V at room temperature, the Vf falls to 0.5V at about 125°C and 0.45V at 150°C. Thus, if such a circuit were raised in temperature above normal operating conditions there is danger of turning on the diode stack from supply to ground. The main advantage of this scheme is its higher current capability, without additional drive capacitance. Also, for a given supply voltage, the additional boost to current at high temperatures may give increased performance under these condition, at the expense of higher leakage.

2.11 Device Noise

There are two basic noise sources, although these can be split further into sub-set categories. These are circuit related noise, such as capacitive or substrate coupling (chapter 11) and noise generated within the active or passive devices.

Most significant among device noise considerations is MOS transistor noise caused through impact ionization, and oxide traps. Impact ionization effects are caused when the electrons from the source region (for an nMOS) are accelerated to the point where ionization can occur. This is shown in figure 2.23.

Samsung Exhibit 1010, Page 57 of 204

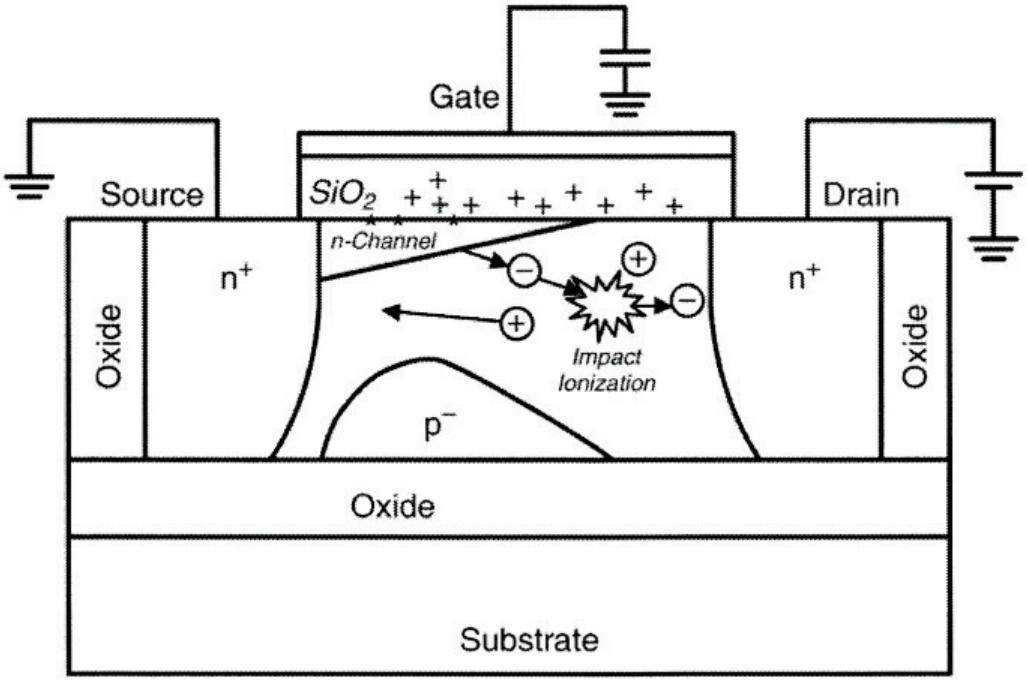


Figure 2.23: Electrons from the source and channel region can gain enough energy as they accelerate across to the drain such that an impact causes an electron hole pair to be generated. The hole tends to migrate to the gate oxide, where it can be trapped, and become a source of noise.

Once a charge unit (electron or hole) has been trapped in the oxide it can become a noise source, which will be more or less significant depending upon the trap depth within the oxide, its activation energy, and the temperature of operation of the circuit.

Figure 2.24 illustrates the trapping mechanism within the oxide. Only traps close to the Fermi level are likely to be active and thus contribute significantly to the noise level. As a result noise varies with temperature. Tunneling of carriers within the oxide is most efficient when occurring between trap centers that are at the Fermi level energy.

While it is possible for tunneling to occur at other trap levels, any traps far away from the Fermi level are statistically likely to be filled or empty, dependent upon their energy position. Thus tunneling far from the Fermi level is not significant enough to affect the overall noise characteristics.

Static noise in PD-SOI is higher than in bulk due to additional noise being induced through the floating-body effects and leakage current [2.57]. In PD-SOI there is a parasitic bipolar which can result in noise [2.58]. Body potential variability, and thus threshold voltage of devices, also affect noise.

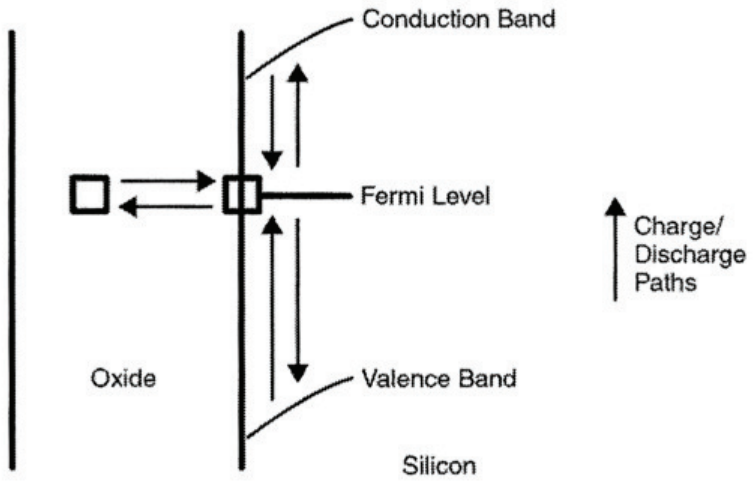


Figure 2.24: This represents a trap deep in the oxide. Traps up to about 15 Angstroms deep contribute to noise. Once filled, the trap continues to affect the channel until it depopulates the trap center.

Without successful prediction of noise, many circuits are at risk of being over designed. Static timing and noise analysis tools have demonstrated their importance in verifying digital designs [2.31, 2.59]. Transistor-level static noise analysis has been shown to be extendable to PD-SOI technology through the addition of floating-body-induced threshold voltage variation and incorporation of parasitic bipolar leakage [2.57].

To establish an initial condition for static noise analysis, a choice must be made between minimum and maximum body voltages for each transistor. Typically for memory and digital cells this might result in a worst case condition of strong noise inducing devices and weak holding devices. Although noise is normally a problem, one analog device has made beneficial use of noise. A single-stage operational transconductance amplifier in SOI has been used as a generator to produce a high level of noise at its output created by the SOI transistors [2.60].

2.12 Self Heating

Self-heating is a serious disadvantage for SOI, particularly when applied to analog circuits, although self-heating can also reduce the performance of logic circuitry and cause an increase in leakage. Self-heating has two manifestations. It can emanate from within the sub-circuit itself or from elsewhere on the same IC. Self and coupled heating can have an impact on analog circuit blocks in SOI.

Temperature rise can be significant even at relatively low power dissipations. As with bulk silicon, these effects are layout dependent.

Particularly in circuits requiring accurate matching, accounting for this type of thermal effect relies on good layout techniques and in some instances additional thermal simulation.

The buried oxide reduces thermal conductivity to the substrate (compared to bulk) resulting in locally increased temperature. This can impact circuit performance, and possibly reliability [2.27]. In addition to buried oxide, devices are relatively isolated from adjacent devices because of the use of trench isolation.

Self-heating reduces mobility and drain conductance. Analysis of drain conductance from DC to 300MHz has been performed to show that thermal dissipation can be modeled by just a single time constant [2.61]. Thus dynamic self-heating models usually provide sufficient accuracy using a single thermal resistance and capacitance. This is the type of thermal model incorporated in the BSIM-PD model (chapter 4).

Typically SIMOX has a thermal resistance of about 300°C/W (for the entire chip) and a thermal time constant of approximately 3μs. However, individual SOI devices are susceptible to local thermal heating as a result of the reduced thermal conductivity caused by the buried oxide and isolation trench. From [2.62] we can assume that the thermal resistance for a gate width of 1μm is approximately 25000°C/W.

In most logic circuits, devices conduct only during switching. Temperature rise in most devices is just a few degrees, which can normally be tolerated. This minimal effect of temperature rise on digital circuits has been confirmed experimentally: Two otherwise identical 11 and 51 stage ring oscillators on SOI were tested. Assuming leakage is low compared to switching dissipation, to a first order approximation the power dissipation per stage of the 11 stage structure is 51/11 times that of the 51 stage structure. Delay per stage of the 11 stage ring was not significantly different to that of the 51 stage ring, indicating any temperature rise difference between the two rings is not significant to circuit operation.

Analog circuits with only internal connections often have higher dissipation, and may experience a larger increase in temperature. This is of most importance in structures that are required to match, as discussed in chapter 10. Output drivers typically see temperature increases of the order of 20°C, but under switching or fault conditions this can be much higher.

Figure 2.25 shows the effect of self-heating on the MOS I-V curve. Most devices in switching circuits follow the solid curves since transient switching

Samsung Exhibit 1010, Page 60 of 204

does not result in significant power dissipation, hence temperature increase is minimal. Devices affected by self-heating follow a curve closer to that of the dashed lines, which takes into account the power consumed in the component. Drain-source resistance and drain voltage dictate the maximum power handling, and hence the device's contribution to self heating. This must be considered in both analog and high power design. It is also necessary to correct for self-heating effects when making DC SOI current measurements. For this type of measurement a typical device shows self-heating degradation in Ids values of between 3 and 10%.

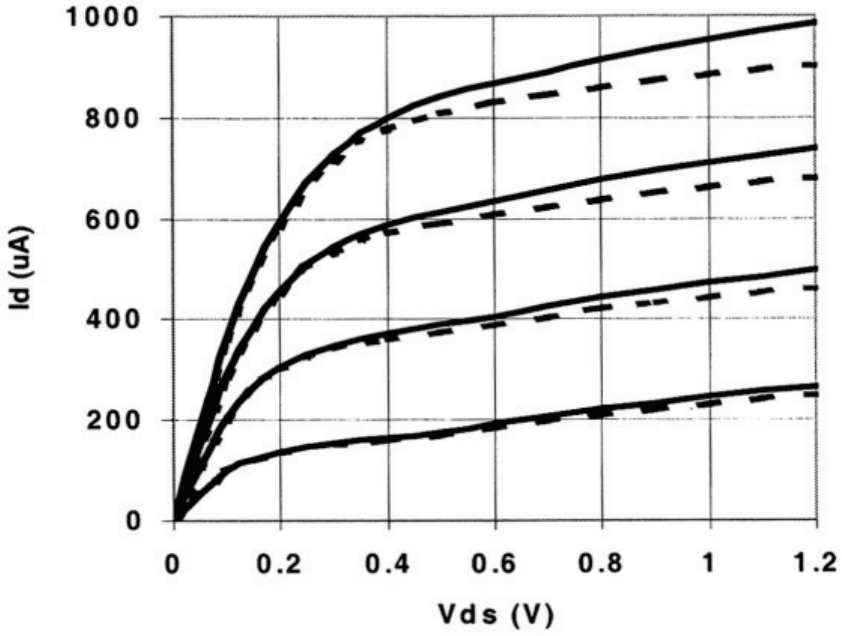


Figure 2.25: Representation of the effect of heating on a MOS device (dashed lines) compared to device operation without heating effects (solid lines). Trend lines shown for various Vgs values.

Dynamic self-heating in SOI devices is known to be an issue with analog designs [2.63]. Most SOI SPICE models, e.g. BSIM-PD and STAG v2.0 (chapter 4) include self-heating components, and it is considered essential to include self-heating in the modeling of analog circuits. This requires accurate thermal resistances and time constants [2.64, 2.65].

2.12.1 Self Heating from elsewhere on the same chip

Digital Circuits

Bulk digital CMOS design rarely needs to consider heating effects. With higher current densities of modern processes and the poor thermal

conductivity of the buried oxide layer, it is not necessarily the case that thermal effects can still be ignored. The buried oxide has a thermal conductivity approximately a factor of 100 worse than bulk silicon, making self-heating effects more pronounced. Assuming a 0.5μm thick oxide is equivalent to about 50μm of silicon, and a typical chip is about 250μm thick, then the additional equivalent thermal thickness of SOI is significant.

Analog Circuits

Within chip heating effects, from high thermal dissipation regions to other areas on the same chip are well understood, and layout techniques have been described in standard texts for bulk silicon [2.66, 2.67]. Many of the same basic configurations such as common centroid matched devices can be applied to SOI. (Cross coupling of matched devices serves more than immunity from thermal gradients, it also helps to minimize the effects of other processing related gradients that can occur). Conventional current mirrors in bulk silicon often use cross coupled devices to eliminate process variability across a chip, and thermal gradients due to external sources. Due to the high thermal resistivity of the oxide isolation between devices, cross coupling used in bulk devices may be less effective in SOI. Improvements to this scheme require all elements of the cross coupled structure to be within the same tank.

2.12.2 Self Heating from within a sub-circuit

Power is dissipated in the MOS channel as a result of the current through the channel and voltage across it. Due to poor thermal conductivity of SOI compared to bulk, the temperature of the layer above the buried oxide may increase significantly in the power-dissipating device, affecting its characteristics [2.65, 2.68]. The most typical effects of self-heating within a device are reduced threshold voltage, drive current, and increased leakage. Most models have the capability to determine dynamic local device temperature, through an externally accessible voltage node, which represents device temperature.

Self-heating effects are most important in devices where continuous current flows through a device with the source and drain biased at significant voltages. This occurs most frequently in analog designs. One of the simplest analog circuits in which this is important is the current mirror. Thermal effects are usually simulated with a RC network, representing thermal capacity of the silicon and θjc. Temperature rise within the device can be calculated from power and thermal resistance as follows:

θjs (junction-substrate thermal res.) = ΔT (Temperature rise)/Power (W)
Therefore: ΔT = θjs * W

2.12 Self Heating

W = power output = power input = Id * Vds

Hence $\Delta T = \theta js * (Id * Vds)$ (1)

Note Id has temperature dependence and usually reduces with increasing temperature.

Samsung Exhibit 1010, Page 63 of 204

References

[2.1] C. Y. Chang and S. M. Sze, Editors, "ULSI Devices", John Wiley & Sons, Inc., ISBN 0-471-24067-2

[2.2] A. Wagpmans, et. al., "3.5mW 2.5GHz Diversity Receiver and a 1.2mW 3.6GHz VCO in Silicon-On-Anything" ISSCC98, paper No. FP 16.3:A

[2.3] R. Dekker, et. al., "An Ultra Low-Power RF bipolar technology on Glass" IEDM, 1997. pp. 921 - 923.

[2.4] M. L. Alles et.al., "Investigating optical metrology issues specific to SIMOX-SOI wafers", Micro, June 2000

[2.5] Appendix 1 (2.5)

[2.6] Appendix 1 (2.6)

[2.7] R. Hannon, et.al., "0.25 μm Merged Bulk DRAM and SOI Logic using Patterned-SOI", 2000 Symposium on VLSI Technology Digest of Technical Papers, pp. 66 - 67.

[2.8] J. Haisma, et. al., Jpn.J.Appl.Phys., vol.25, 1989, pp. 1426.

[2.9] C. E. Hunt & C. A. Desmond, Proceedings of the First Symposium on Semiconductor Wafer Bonding, 1992, pp. 165.

[2.10] A. Soderbarg, Proceedings of the First Symposium on Semiconductor Wafer Bonding, 1992, pp.190.

[2.11] Appendix 1 (2.11)

[2.12] K. Sakaguchi & T. Yonehara, "SOI Wafers Based on Epitaxial Technology", Solid State Technology, Jun 2000.

[2.13] K. Sakaguchi, et. al., Jpn. J.Appl. Phys., vol.34, 1995, pp. 842 - 847.

[2.14] P. B. Mumola & G. J. Gardopee, Conference on Solid State Devices and Material, 1995, pp. 256.

[2.15] "New Technologies for silicon-on-insulator", European Semiconductor, Feb 2000, pp. 25.

[2.16] M. I. Current et. al., "Ultrashallow Junctions or Ultrathin SOI", Solid State Technology, Sept. 2000, pp. 66 - 77.

[2.17] H. Lee, et. al., “An Anomalous Device Degradation of SOI Devices with STI”, 2000 IEEE International SOI Conference, Oct. 2000, pp. 132 - 133.

[2.18] K. Bernstein & N. J. Rohrer, “SOI Circuit Design Concepts”, Kluwer Academic Publishers, January 2000, ISBN 0-7923-7762-1

[2.19] T. Houston, et. al. “Novel MESA isolation using CMP for planarization of 0.35/0.25uM SOI”, IEEE International SOI conference, Oct 1995, pp. 110 - 1.

[2.20] G. Shahidi, et. al., Proceedings of the 1992 VLSI Symposium, p. 93 - 94.

[2.21] G.G. Shahidi, et. al., “A high performance low temperature 0.3 μm CMOS on SIMOX” 1992 Symposium on VLSI Technology, 1992, pp. 106 – 107.

[2.22] L. Su, et. al., Proceedings of the 1996 VLSI Symposium.

[2.23] S. T. Liu, et. al., "Radiation Response of SOI Materials”, Electrochemical Soc. Proc. 1999, pp. 225 - 230.

[2.24] G. Shahidi, et. al., 'Mainstreaming of the SOI Technology,' Proc. IEEE Inter. SOI Conf, 1999, pp. 1-4.

[2.25] E. Leobandung, et. al., "High Performance 0.18um SOI CMOS Technology,' IEDM-99, 1999, pp. 679 - 682.

[2.26] S. Cristoloveanu, "Architecture of SOI Transistors: What's Next?", 2000 IEEE International SOI Conference, Oct. 2000, pp. 1 - 3.

[2.27] G. G. Shahidi, et. al., “Device and Circuit Design Issues in SOI Technology”, Proceedings of the IEEE, 1999, pp. 339 – 346.

[2.28] G. Shahidi et. al., "A Room Temperature 0.1μm CMOS on SOI", IEEE Transactions on Electron Devices, Vol 41, Dec. 1994, pp. 2405 - 2412.

[2.29] G. Anthony, et. al., "A 0.2-mm, 1.8-V, SOT, 550-MHz, 64-b PowerPC Microprocessor with Copper Interconnects", IEEE Journal of Solid State Circuits, Vol. 34, No. 11, Nov. 1999, pp. 1430 - 4.

[2.30] Proc. 5th Inter. Workshop on Measurement, Characterization and Modeling of ultrashallow Doping Profiles in Semiconductors, J. Vac. Sci. Technol., 2000, pp. 337 -604.

[2.31] K. Sukegawa, et. al., "High-performance 80-nm Gate Length SOI-cMOS Technology with Copper and Very-low-k Interconnects", 2000 IEEE Symposium on VLSI Technology Digest of Technical Papers

[2.32] D. Edelstein, et. al., "Full copper wiring in a sub-0.25 μm CMOS ULSI technology" IEDM Tech.Dig.,1997, pp.773 - 6.

[2.33] M. Ikeda, et. al., "Integration of organic low-k material with Cu-damascene employing novel process", Interconnect Technology Conference, 1998. pp. 131-3.

[2.34] K. Mistry, et. al., "Scalability Revisited: 100 nm PD-SOI Transistors and Implications for 50 nm Devices", IEEE VLSI Conference 2000, 0-7803-6308-6, pp. 204-5.

[2.35] R. Chau, et. al., IEDM Tech. Digest, 1997, pp. 591 - 594.

[2.36] E. Leobandung, et. al., "Scalability of SOI technology into 0.13 μm 1.2 V cMOS generation", IEDM Tech. Digest, 1998, pp. 403 - 406.

[2.37] D. Flandre, et. al., "Fully-Depleted-SOI cMOS technology for low-voltage low-power digital/analog/microwave circuits", Analog Integrated Circuits and Signal Processing. New York: Kluwer, 1998.

[2.38] J-P. Eggermont, et. al., "Potential and Modeling of 1μm SOI cMOS Operational Transconductance Amplifiers for Applications up to 1 Ghz" IEEE Journal of Solid State Circuits, Vol. 33, No. 4, April 1998, pp 640 - 643.

[2.39] S. M. Sze, "Physics of Semiconductor Devices", John Wiley and Sons, New York.

[2.40] S. K. H. Fung, et. al., "Impact of the Gate-to-Body Tunneling Current on SOI History Effect", 2000 IEEE International SOI Conference, Oct. 2000, pp. 122 - 3.

[2.41] J. Y. Choi & J. G. Fossum, "Analysis and control of floating body bipolar effect in fully Depleted submicrometer SOI MOSFET's", IEEE Trans. Electron Devices, vol.38, 1991, pp.1384 - 91.

[2.42] W. Redman-White, et. al., "Analogue design issues for SOI CMOS" IEEE International SOI Conference, 1996, pp. 6 - 8.

[2.43] Y-C. Tseng, et. al., "Local Floating Body Effect in Body-grounded-SOI nMOSFETs", Proceedings 1997 IEEE International SOI Conference, Oct 1997, pp. 26-7.

[2.44] O. Rozeau, et. al., "Impact of Floating Body and BS-Tied Architectures on SOI MOSFET's Radio-Frequency Performances", 2000 IEEE International SOI Conference, Oct. 2000, pp. 124 - 5.

[2.45] Y. C. Tseng, et. al., "Correlation between Low Frequency Noise Overshoot in SOI MOSFETs and Frequency Dependence of Floating Body Effect", 1997 Symposium on VLSI Technology Digest of Technical Papers, 1997, pp. 99 - 100.

[2.46] J. Gautier, et. al., IEDM Tech. Dig., 1995, pp. 61 - 3.

[2.47] D. Suh & J. G. Fossum, "Dynamic floating-body instabilities in partially depleted SOI CMOS circuits", IEDM Technical Digest, 1994, pp. 661 - 664.

[2.48] A. Wei, et. al., "Effect of floating-body charge on SOI MOSFET design", IEEE Trans. Electron Devices, vol. 45, Feb. 1998. pp. 430 – 438.

[2.49] F. Assaderaghi, et. al., "History-Dependence of Non-Fully Depleted (NFD) Digital SOI Circuits", VLSI Tech. Dig., 1996, pp. 122 - 3.

[2.50] J. P. Colinge, "Silicon-On-Insulator Technology: Materials to VLSI", Kluwer Academic Publishers, 1991.

[2.51] J. Eckhardt et. al., "A SOI specific PLL for 1 GHz microprocessors in 0.25 μm 1.8 V", ISSCC 1999. pp. 436 - 437.

[2.52] A. Nishiiyama, et. al., "Mechanism of the suppression of the floating-body effect for SOI MOSFET's with SiGe source structure", Proc. 1996 IEEE Int. SOI Conf., Oct. 1996, pp. 68 - 69.

[2.53] K. Suma, et. al., "An SOI-DRAM with wide operating voltage range by CMOS/SIMOX technology", IEEE J. Solid State Circuits, vol. 29, Nov. 1994, pp. 1323 - 1328.

[2.54] G. Shahidi et. al., "Partially-Depleted-SOI Technology for Digital Logic", ISSCC 1999, pp. 426 - 427.

[2.55] Silicon-On-Insulator Integrated Circuit Technology, U.S. Patent No. 5,489,792

[2.56] J.G. Fossum & G.O. Workman, "A comparative analysis of the dynamic behavior of BTG/SOI MOSFETs and circuits with distributed body resistance", IEEE Transactions on Electron Devices, Oct. 1998, pp. 2138 - 2145.

[2.57] K.L. Shepard & D-J. Kim, "Static Noise Analysis for Digital Integrated Circuits in Partially-Depleted Silicon-On-Insulator Technology", Design Automation Conference, 2000. pp. 239 – 242.

[2.58] P-F. Lu, et. al., "Floating-body effects in partially Depleted-SOI CMOS circuits", IEEE Journal of Solid-State Circuits, August 1997, pp. 1241 - 1253.

[2.59] K. L. Shepard, et. al., "Harmony: Static noise analysis for deep-submicron digital integrated circuits", IEEE Transactions on Computer Aided Design, Aug 1999, pp. 1132 - 1150.

[2.60] A. Nève, et. al., "Smart Card Circuits in SOI Technology", 2000 IEEE International SOI Conference, Oct. 2000, pp. 48-49.

[2.61] B. M. Tenbroek et. al., Proceedings ESSDERC 1993, Grenoble, France, pp. 189-192

[2.62] H. Nakayama, et. al., "SOI MOSFET Thermal Conductance and Its Geometry Dependence" 2000 IEEE International SOI Conference, Oct. 2000, pp. 128 - 9.

[2.63] B. M. Tenbroek, et. al., "Characterization of layout dependent thermal coupling in SOI CMOS current mirrors", IEEE Transactions on Electron Devices, Dec. 1996, pp. 2227 – 2232.

[2.64] B. M. Tenbroek, et. al., "Measurement and Simulation of Self Heating in SOI CMOS Analogue Circuits", Proceedings 1997 IEEE International SOI Conference, Oct. 1997, pp. 156 - 7.

[2.65] B. M Tenbroek, et. al., “Self-heating effects in SOI MOSFETs and their measurement by small signal conductance techniques” , IEEE Transactions on Electron Devices, Vol. 43, No 12, 1996, pp. 2240 - 2248.

[2.66] A. Hastings, “The Art of Analog Layout”, Prentice-Hall, ISBN: 0-13-087061-7, 2000

[2.67] P. R. Gray & R. G. Meyer, “Analysis and Design of Analog Integrated Circuits, third edition”, Wiley, 1993, ISBN 0-471-57495-3.

[2.68] M. S. L. Lee, et. al., "Modelling of thin film SOI devices for circuit simulation including per-instance dynamic self-heating effects", Proc. IEEE Int. SOI Conference, Palm Springs, CA, Oct. 1993, pp. 150 - 151.

Chapter 5: Layout for SOI

5.1 Introduction to Layout for SOI components

Conventional bulk silicon layout has been discussed in detail [5.1, 5.2]. However, for PD-SOI, components require some specific layout rules that account for floating body use, yet permit body ties. Most PD-SOI design rules remain common to bulk design rules, the most significant difference being floating body effects, and in some cases a change from junction to dielectric isolation. Figure 5.1 shows an example of a floating body nMOS transistor layout. The pMOS is very similar, except for the diffusions being of opposite type.

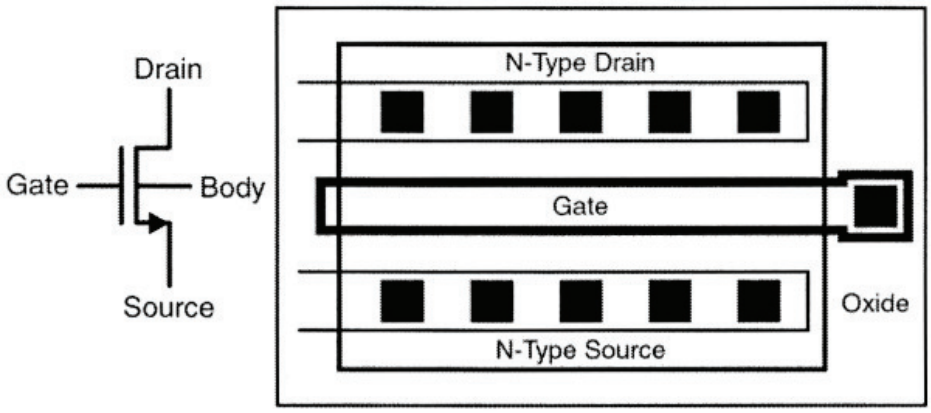


Figure 5.1: Typical layout configuration for a floating gate nMOS structure in SOI. The pMOS device is similar, but has the opposite type diffusions.

An inverter cell is shown in figure 5.2. The drains of the nMOS and pMOS are connected, as are the gates. The configuration using SOI saves some area

compared to junction isolated bulk material, due to reduced isolation requirement of the trench isolated SOI material.

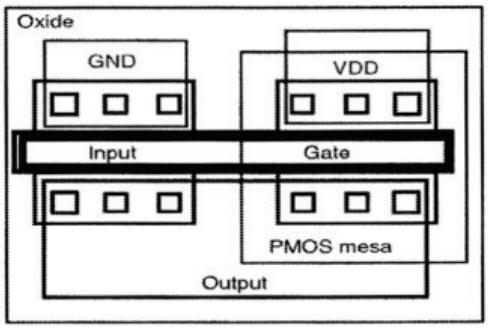


Figure 5.2: Layout configuration for a floating body inverter built in SOI. The gate can be built as a single polysilicon strip. The nMOS is shown as the left hand side MOS, the PMOS is the right hand side component.

Layout of a device with body-tied to source is shown in figure 5.3. Here the body tie is built into the source diffusion. For wide devices, two or more body-ties are required, spaced apart by a few microns, due to the high resistivity of the body region.

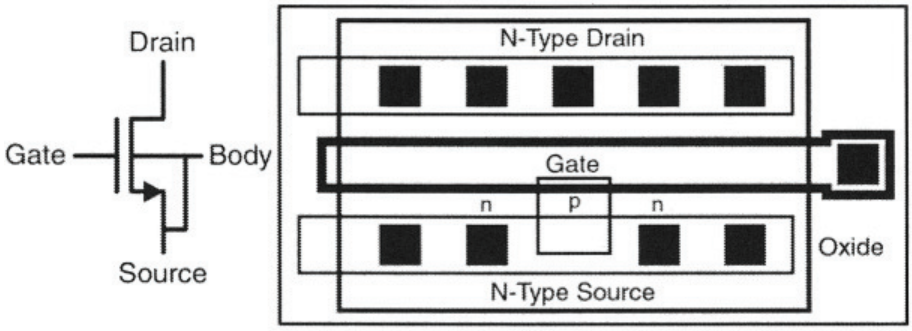


Figure 5.3: One layout example of how a body-tied to source device can be constructed in SOI. The body contact contacts to the source through the low resistivity silicided source diffusion. The body tie reduces the efficiency of the structure.

Body tied devices are often used in analog applications, as this minimizes the kink effect. At higher frequencies the RC caused by the capacitive coupling of the drain/gate to body and the distributed resistance of the body does not permit a solid connection to the entire body region. Thus some of the benefit of tying body to source is lost. At low frequencies body ties can

Samsung Exhibit 1010, Page 71 of 204

provide improved matching for input pairs of comparators or operational amplifiers.

Another layout requirement is for when the body tie is not connected to source. The configuration in figure 5.4 is used when the body must be tied to a potential other than the source, such as ground, supply or another body. This is advantageous in transmission gate devices, which are easier to implement if tied to a fixed supply rail.

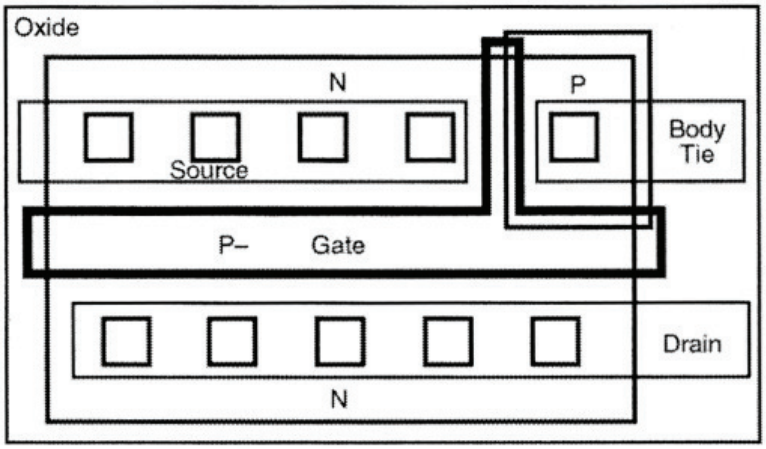


Figure 5.4: Method for producing a body tie that is isolated from the source region. Here the gate is used to mask the source region from the body tie, and the body tie diffusion is of opposite type to the source and drain. This is less efficient than the body tied to source configuration (figure 5.3).

5.2 Converting designs from Bulk to SOI

The typical, though not necessarily the best, approach to converting circuit designs from bulk to SOI, especially when modifying an existing design from bulk to SOI, is to keep as much of the bulk design as is reasonable, but redesign the sections that require it [5.3].

Circuit designs are considered in subsequent sections which use both bulk influenced designs, where many bodies are tied, and designs completely reengineered for PD-SOI, where all bodies float, or are connected in such a manner as to enhance the SOI circuit compared with the bulk counterpart.

5.2.1 Diodes

Diodes can be created using the same basic configuration as used for isolated body ties, although layout may be adapted. This is termed a gated diode, as the structure includes a MOS gate that needs to be biased appropriately to give diode operation. Figure 5.5 shows the gated diode configuration.

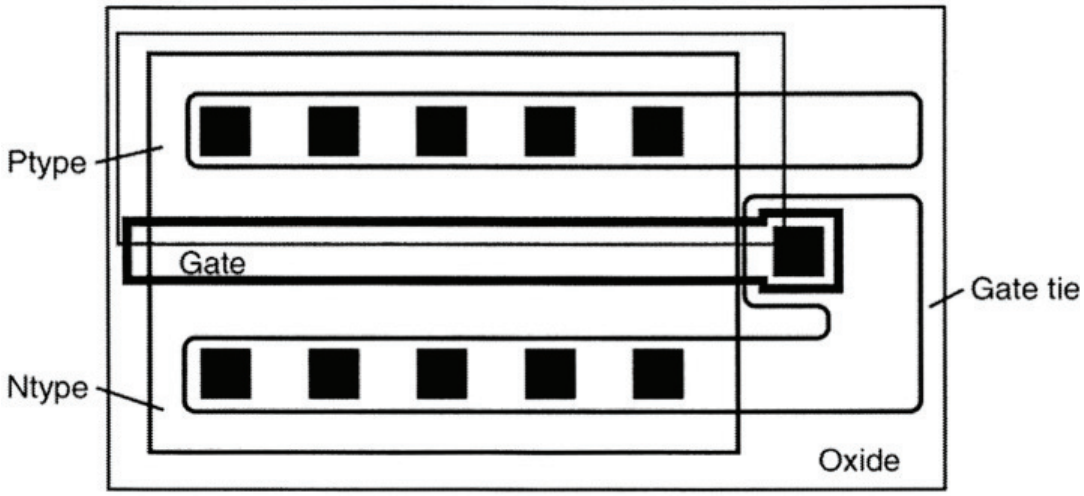


Figure 5.5: Example of a diode constructed in SOI, using the gate as the isolation mechanism between the diode anode and cathode. The gate tie is shorted to the cathode of the diode. The P-type region is the anode.

Silicide is generally included in the processing of modern ICs, to reduce contact resistance and improve MOS device performance. Silicide has the effect of shorting adjacent diffusions, unless separated by polysilicon, or the silicide is blocked.

Most processes include a silicide block option. This can be used to create a silicide block diode, which is more efficient than the gated diode structures. Figure 5.6 shows the silicide-block diode configuration.

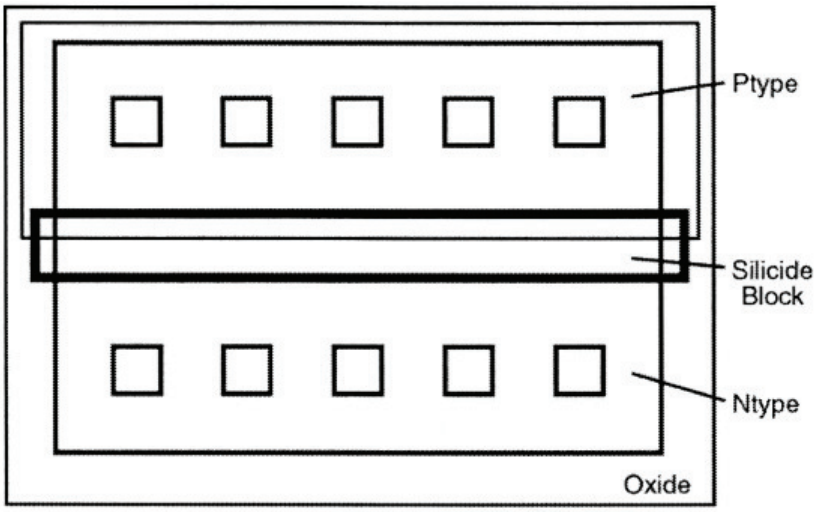


Figure 5.6: Example of a diode constructed in SOI, using silicide block as the isolation mechanism between the diode anode and cathode.

As with gated diode structures, the silicide-blocked diode structure anode is constructed of p-type silicon, and the n-type is the cathode.

5.2.2 Bipolar Transistors

In addition to basic isolated pMOS and nMOS devices, PD-SOI lends itself to high voltage and high frequency applications, and extends the options foractive and passive devices, including isolated bipolar structures. Bipolars are simply created by accessing the body contact, and connecting gate to source. Thus the nMOS and pMOS can be used as isolated NPN and PNP devices. Most of these are lateral structures, such as used for the PNP in many bipolar and BiCMOS processes. The difference being that here the gate length can be much shorter and the isolation greatly improved over the structures used in what are now mostly obsolete processes. Figure 5.7 shows the basic construction of the lateral PNP structure of a bipolar process, and figure 5.8 shows how this may be modified for use in PD-SOI. Although the most efficient variants of the bipolar structures are rather larger than their MOS counterparts, the use of bipolar devices is limited to a small proportion of the circuitry, where for example, higher precision voltage thresholds or higher frequency of operation are required than obtainable from MOS components. Due to base (body) resistance, bipolar structures are generally of higher performance if the active silicon region is relatively thick. With additional processing steps tailored to optimized bipolar structures, improved NPN and PNP devices can be created.

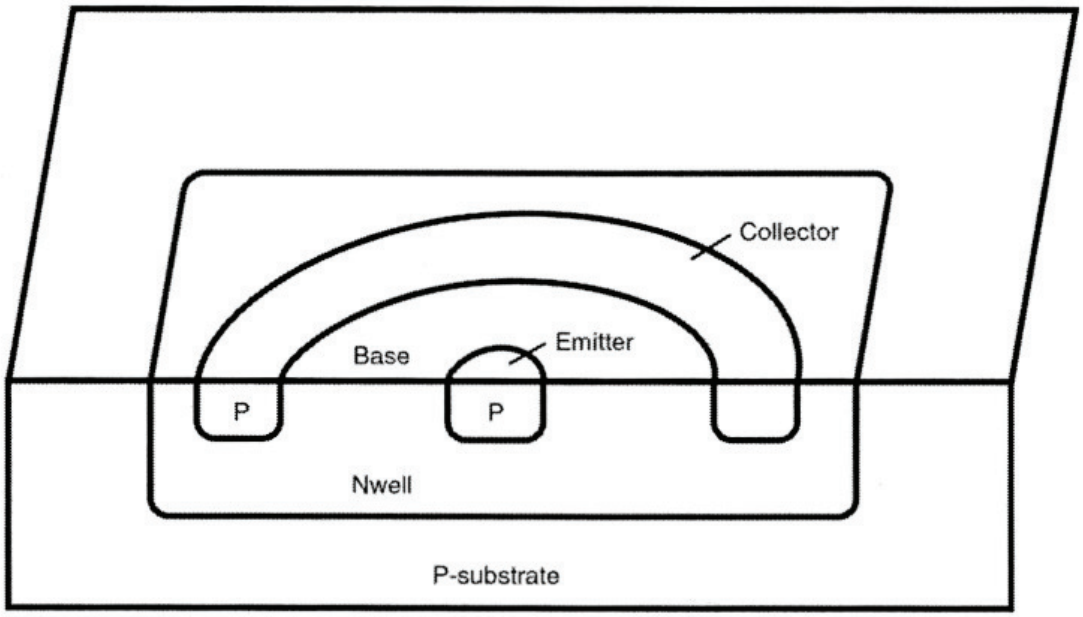


Figure 5.7: Lateral PNP design used in bulk processes.

Samsung Exhibit 1010, Page 74 of 204

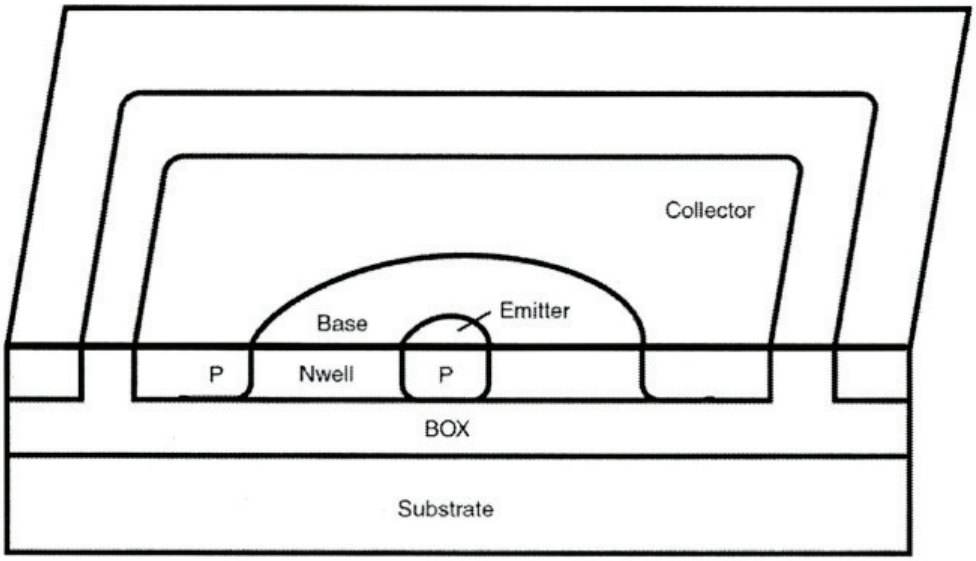


Figure 5.8: Lateral PNP design for PD-SOI.

5.3 Layout for Minimization of Thermal Self Heating Effects

Layout and circuit techniques can be employed to minimize the effect of mismatch due to two devices that have different electrical properties due to the devices being at different temperatures. Often it is possible to combine devices that require matching in the same tank. This helps equalize temperature locally within the silicon mesa. Figure 5.9 shows this for the case of a common-source device, such as a current mirror, or op-amp input pair. Here the source electrically isolates the two transistors, but since the devices are both in the same thermally conducting tank, their temperatures track.

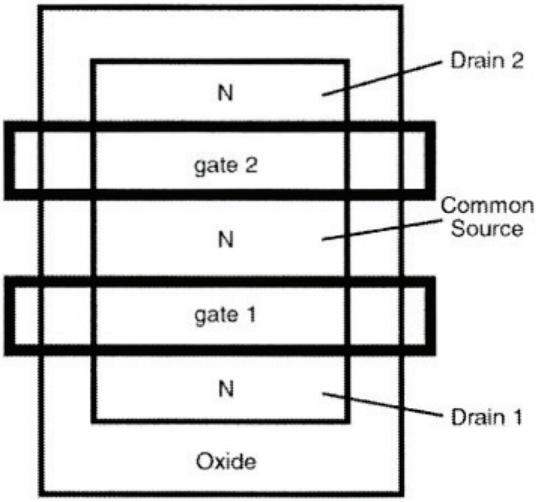


Figure 5.9: Shared tank implementation for a pair of nMOS devices. Here the source electrically isolates the transistors, but since the devices are both in the same thermally conducting tank, their temperatures track.

An alternative implementation for a common mesa also permits shared body voltage, but has specific requirements for operational conditions. Figure 5.10 shows an implementation of two side-by-side MOS devices. Here, the sources are again shared, as are the gates, so this implementation may be used in a current mirror configuration. The drawback here is that there are restrictions on the drain and gate voltages. The drains have to be very close in voltage, or in a state where a channel cannot form between the drains, preventing leakage between nodes. Although this may appear to be restrictive, it may be applicable to such as the lower stage of a cascoded mirror structure.

5.3.1 Cross coupling with thermal coupling

An enhancement to these structures that permit reasonable thermal coupling, while allowing cross-coupling in a common centroid configuration, which can be constructed as shown in figure 5.11. Here the sources are all centrally positioned within the layout and diagonally opposite drains are connected as part of the common device.

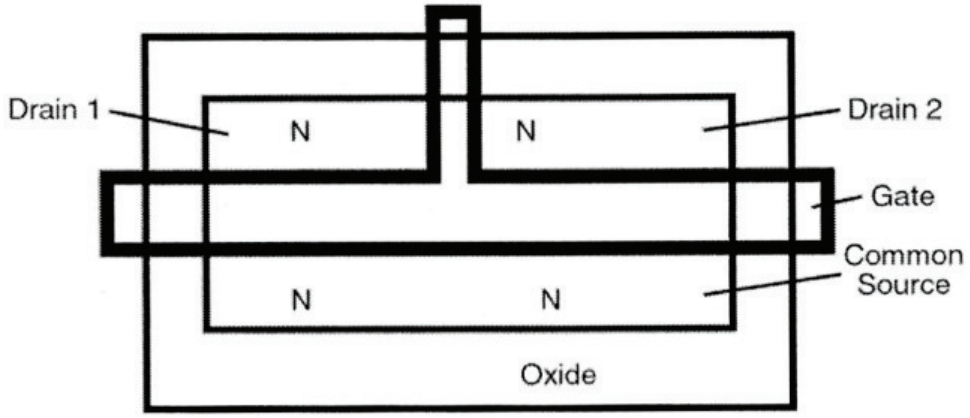


Figure 5.10: Implementation of a nMOS pair, in a side-by-side configuration. Here, the sources and gates are shared, as in a current mirror configuration.

A version of the common centroid structure can be created using partial trench to isolate the adjacent nMOS devices (figure 5.12). Here the thermal coupling is improved, but an additional process step is required for the partial trench.

Thermal coupling can also be achieved in various other components that require matching such as diode arrays and paralleled bipolar devices. There is also a benefit to placing matched polysilicon resistors over the same silicon mesa, rather than over oxide, to obtain the same thermal matching benefits.

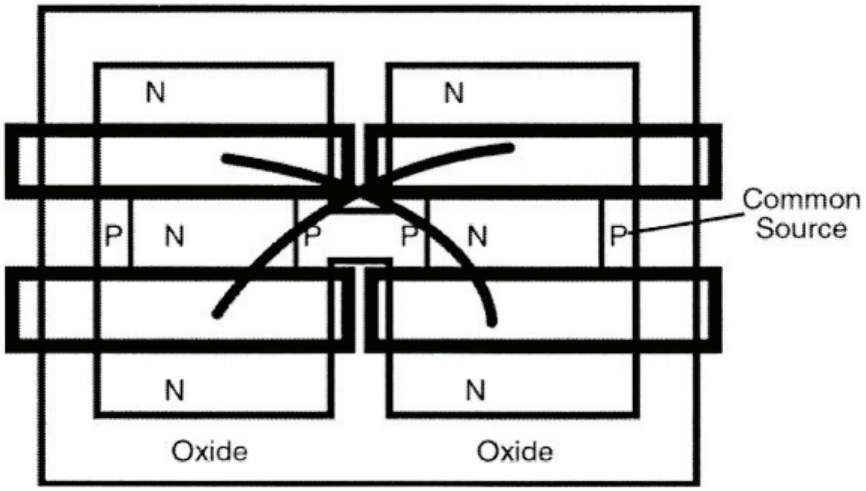


Figure 5.11: Representation of a cross-coupled input pair with common source and isolated drains. This version also ties all the body regions together with a P-type implant. For floating body implementations eliminate the P-type implant.

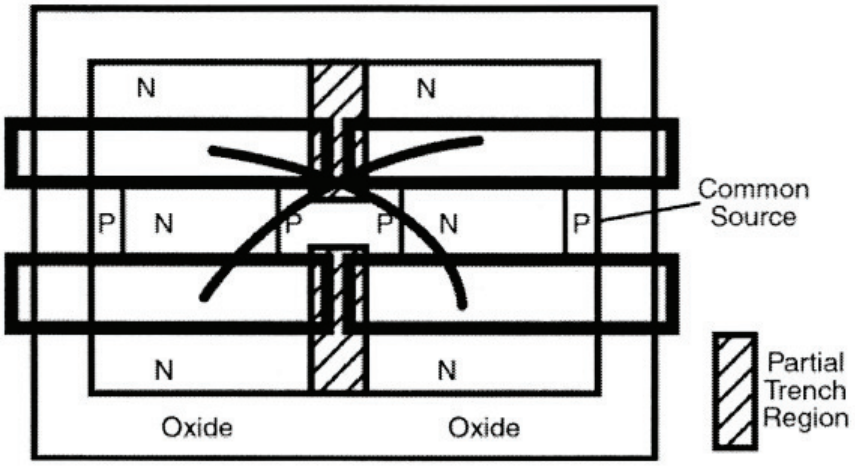


Figure 5.12: Representation of a cross-coupled input pair with common source and isolated drains, utilizing partial trench isolation between adjacent devices.

An alternative scheme, which maintains thermal matching within a mesa is shown in figure 5.13. This method is easier to use in terms of electrical circuit effects, but is not as efficient in terms of electrical matching. In this configuration transistors in the same tank are isolated electrically using gates biased to ground for nMOS structures, or to supply for a pMOS. The isolating transistors do not interfere with thermal characteristics. It is a worthwhile precaution to include the isolating transistors in the circuit

Samsung Exhibit 1010, Page 77 of 204

simulation, to ensure that transient switching of a shared source or drain does not affect other devices on the same mesa.

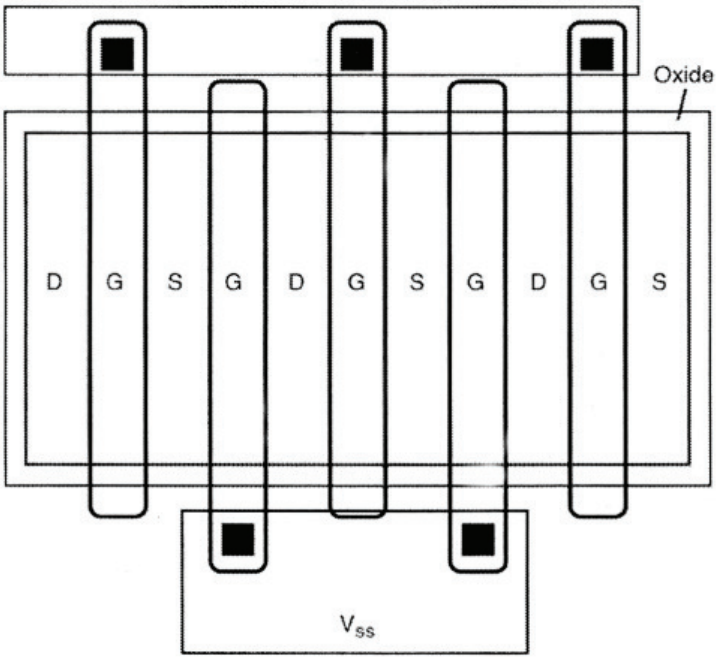


Figure 5.13: Scheme to maintain thermal matching, while permitting widely varying electrical conditions. Here the G' gates are maintained at a potential to ensure that no current can flow between adjacent source and drain nodes.

5.4 Output Stages

Output stages with high power dissipation, such as those common in class "A" amplifiers have been reported to be susceptible to local thermal effects, causing the characteristics of the driver devices to change significantly as output voltage changes. This is because of changes in the small-signal gain, including thermal effects. Self-heating causes a small reduction in gain and introduces an additional thermal zero-pole doublet in the small-signal frequency response.

Layout techniques to minimize these effects include distributed output stages, using a merged SOI with bulk technology (such as selective SIMOX), and thermal coupling through the metal levels. Some of the techniques described previously in this chapter for device thermal matching may also be applicable.

Samsung Exhibit 1010, Page 78 of 204

References

[5.1] A. Hastings, “The Art of Analog Layout”, Prentice-Hall, ISBN: 0-13-087061-7, 2000

[5.2] R. J. Baker, et. al., “CMOS Circuit Design, Layout and Simulation”, IEEE Press, ISBN: 0-7803-3416-7, 1998

[5.3] C. R. Tretz, "Circuit Design in SOI: Concept of Floating Beta Ratio", 2000 IEEE International SOI Conference, Oct. 2000, pp. 4-5.

Chapter 7: Dynamic SOI Digital Design

7.1 Introduction

This chapter focuses on dynamic circuits in partially depleted SOI technology. Charge sharing, Miller capacitance and self-heating are critical design aspects of a dynamic circuit in PD-SOI technology. Parasitic bipolar leakages can upset the functionality of dynamic circuits and are critical design parameters.

Design of dynamic logic circuit is more complex than the design considerations required for static logic circuits. However, the superior performance of dynamic logic over static is the motivation for identifying failure mechanisms. A common problem of dynamic circuits is loss of pre-charge, noise immunity, and variability in delay [7.1].

7.2 Dynamic Circuit Response

Dynamic logic is normally faster than static logic and is used frequently in digital signal processors, microprocessors and other high performance products. If charge loss occurs from a dynamic circuit node, its current logic state can be corrupted. Parasitic bipolar currents, which are of only moderate concern in static logic, can be very detrimental to the charge storage of dynamic logic circuits.

7.2.1 Dynamic History Effect

Figure 7.1 shows a dynamic CMOS circuit [7.1] susceptible to parasitic bipolar current. Consider the case when MN0 is high and MN1, MN2, and MN3 are all low. Node N1 is high and the output is low during precharge.

Since there is no path to ground, intermediate node N2 reaches V_{DD}-V_T, and over a period of time, the body voltages of MN0, MN1 and MN2 rise. Once input MN3 begins switching high, node N2 discharges to ground. The body voltage of MN3 will rise initially due to body to gate coupling. Once the transistor is completely ON, the body voltage drops.

After node N2 discharges to ground, the bodies of transistors MN0, MN1 and MN2 also discharge through their forward biased body-source diodes. The body to source current in each device causes bipolar drain-to-source current. The bipolar body to source current continues until the body is completely discharged. This current can affect the charge at intermediate node N2. Figure 7.1(b) shows the body voltage of nMOS MN3 falling as the input signal IN4 rises.

7.2.2 Dynamic Charge Sharing

Charge sharing is the capacitive voltage division between two nodes. Assuming node N2 is discharged from a previous precharge cycle and N1 is high. If three inputs MN0, MN1 and MN2 are high and MN3 is LOW, voltage is shared between the nodes N1 and N2, since there is no direct path to GND. Node N1 can fall to a voltage that is low enough to corrupt the output. The voltage on node N1 when MN0, MN1, MN2 are 'high', and MN3 'low' can be given by:

$$V_{N1} = V_{DD}*C_{N1}/(C_{N1}+C_{N2})$$

The severity of charge sharing is lower in SOI than bulk. Source/drain capacitance is approximately a factor of four lower than bulk CMOS. Reduced capacitance in SOI helps reduce charge sharing. When the gate voltage rises, the source of the nMOS transistor rises due to capacitive coupling between the source and gate. A reduction in the voltage difference between N1 and N2 causes charge sharing.

7.2.3 Capacitive Coupling Effects

The gate overlap capacitance caused by source/drain region is called Miller capacitance. Assume node N2 (figure 7.1) precharged high from a previous cycle, when the input to MN0 rises, node N2 couples to the gate and increasing its potential, which in turn couples onto output node N1 and increases its charge.

If transistor MN0 is completely ON, Miller effect will be reduced due to the reduced voltage difference between N1 and N2 since there exists a current path to ground.

Samsung Exhibit 1010, Page 81 of 204

7.2.4 Keeper Devices or Bleeders

Subthreshold leakage current and other process related leakage currents are a major cause of circuit failures in SOI. To maintain functionality from leakage currents, keeper devices are used, which are normally weak pMOS devices with extended gate lengths. Keepers replace lost charge due to parasitic bipolar leakage currents. They require careful sizing to maintain proper functionality. High current keeper devices impact hysteresis and degrade performance. In SOI technology, parasitic bipolar response is controlled better with more effective design of the nMOS evaluate stack rather than with a strong pMOS keeper.

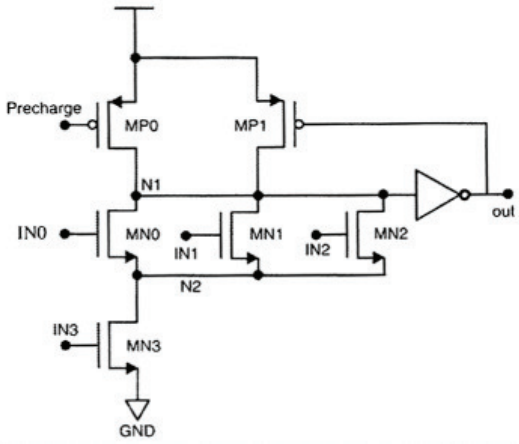


Figure 7.1(a): Dynamic Circuit vulnerability to parasitic bipolar current.

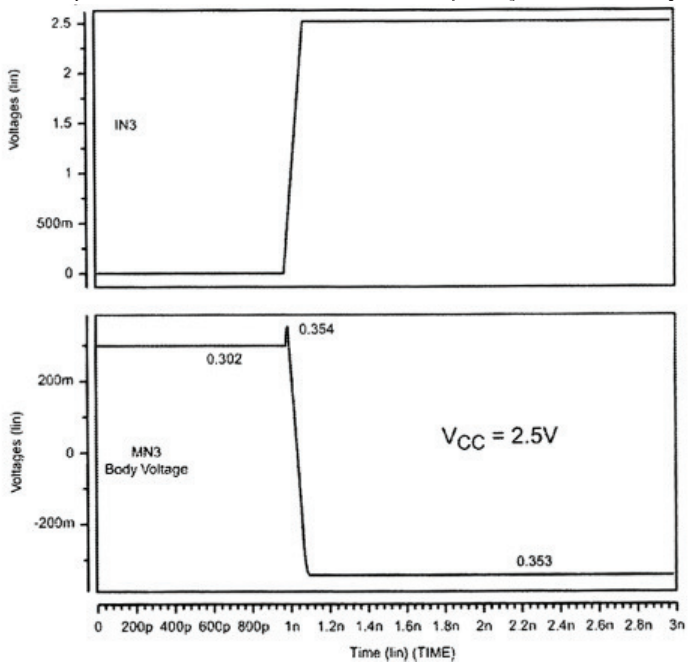


Figure 7.1(b) Input and body voltages of transistor MN3 falling from 0.354V(@V_{DD}=2.5V) to ground after the gate input raises. The body voltage dip for V_{DD}=1.2V is 0.244V.

Samsung Exhibit 1010, Page 82 of 204

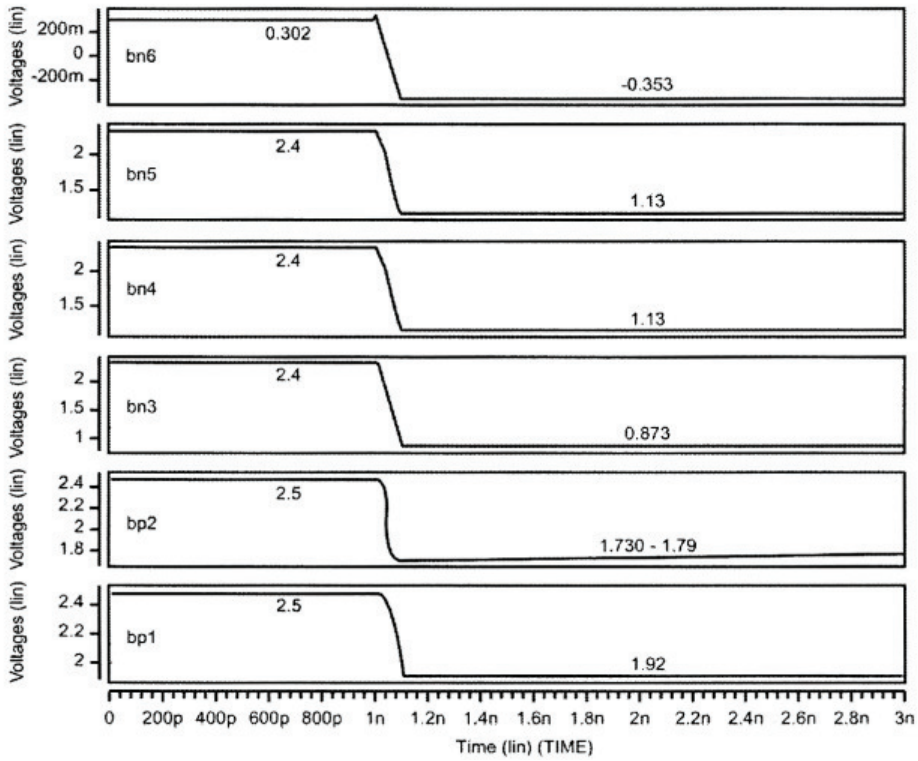


Figure 7.1(c): Node voltages associated with schematic of figure 7.1(a)

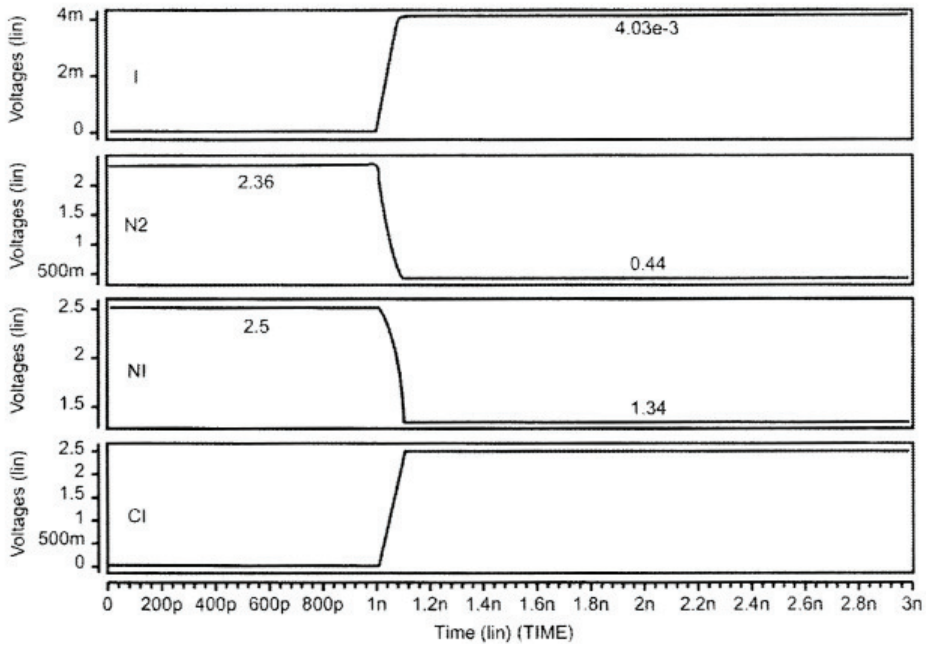


Figure 7.1(d): Body voltages associated with schematic of figure 7.1(a)

Samsung Exhibit 1010, Page 83 of 204

7.3 Dynamic Circuit Design Considerations

Pre-charging intermediate nodes in a domino stack reduces the loss caused by charge sharing and charge redistribution. There are three different precharge mechanisms to an intermediate node in a dynamic circuit. These are: (1) Precharge high, (2) Precharge Low (3) Precharge between supply rails. Precharging has different trade-offs in bulk and SOI. Refering to figure 7.1 we analyse some of the trade-offs [7.1, 7.2].

(1) Precharging N2 high results in worst case noise immunity as it charges the bodies of devices MN0-2 high. This causes bipolar devices to turn 'on' and causes increased device leakage. If intermediate node N2 is precharged high, with the source and drain of MN0-2 at V_{DD} and V_{DD}-V_T, the bodies charge to V_{DD} causing source-drain leakage. Body effect is minimal when the output is high, but results in higher drain junction capacitance. The drain body space charge region is small when the body and drain potentials are high helping noise immunity but hurting performance. Discharge performance is very slow, since the high induced charge must be discharged to get the evaluate stack to discharge.

(2) Precharging to ground results in discharging transistors bodies MN0-2 to GND, eliminating bipolar leakage, and improving noise immunity. Discharge is rapid. The diffusion capacitance is relatively low, easing charge-sharing concerns. The maximum body effect occurs when the bodies of transistors MN0-2 are low. Low drain junction capacitance occurs when the bodies of devices MN0-2 are low, since the drain body space charge region increases as the body and drain (pre-charge node) potential difference increases. This helps performance but degrades noise immunity.

(3) Intermediate charging achieves low parasitic bipolar and MOSFET leakage. Charge exists on the storage nodes, diffusion capacitance is small and charge sharing is minimal. Node N2 is not fully charged, hence the presence of body effect. Junction capacitance is not at a minimum, causing a trade off between noise immunity and performance. Discharge performance is balanced [7.3].

The sequence in which the signals arrive at the gates of the transistors in the evaluate mode is very important and may need be different case from the bulk devices. One method to reduce the losses due to bipolar current and precharge, is to cross couple inputs in the nMOS stack. Figure 7.2(a) shows the conventional dynamic logic circuit, and, figure 7.2(b) shows the same circuit after re-ordering/cross coupling the inputs. This approach also achieves favorable performance while limiting charge loss [7.1].

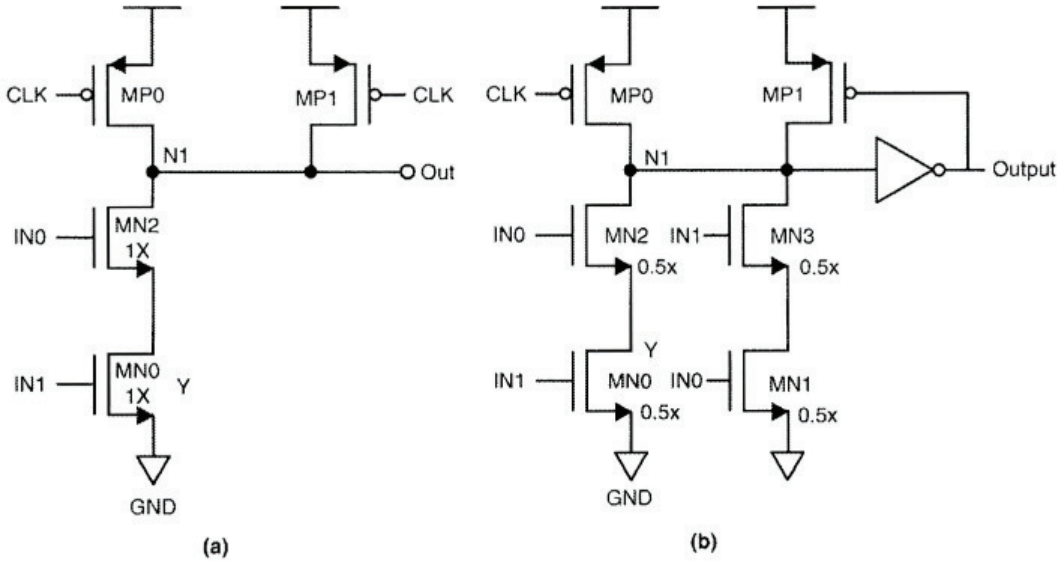


Figure 7.2: Cross-coupling for balancing performance and noise. (a) Original signal coupling as practiced in bulk and (b) Design practice in SOI. [7.1]

7.4 Re-ordering and Remapping

Latest arriving signals should be connected closer to the output in dynamic bulk circuits to prevent charge sharing, and charge redistribution. This technique proves useful for bulk CMOS circuits, however, in SOI technology, due to the parasitic bipolar leakage, it is of reduced benefit. As the number of devices in the nMOS stack reduces, the amount of charge lost to leakage increases.

Domino stages use a single path to GND for multiple inputs also reducing charge loss. Furthermore, it is useful to put a gating switch closer to the output to minimize charge loss. Figure 7.3(a) shows a dynamic CMOS circuit and figure 7.3(b) shows the circuit after re-ordering. The total number of devices developing high body potential and charge loss is reduced.

7.5 Logical Remapping

A frequently used technique is that of logical remapping. This involves, re-positioning of inputs from the dynamic portion of the circuit into the static circuits. This technique is been used in bulk dynamic circuit design frequently.

Logical re-mapping of inputs reduces the stack height, history magnitude and bipolar current loss in SOI technology. Figure 7.4 shows the

Samsung Exhibit 1010, Page 85 of 204

conventional dynamic logic circuit and the remapped circuit. The stack is reduced by one transistor.

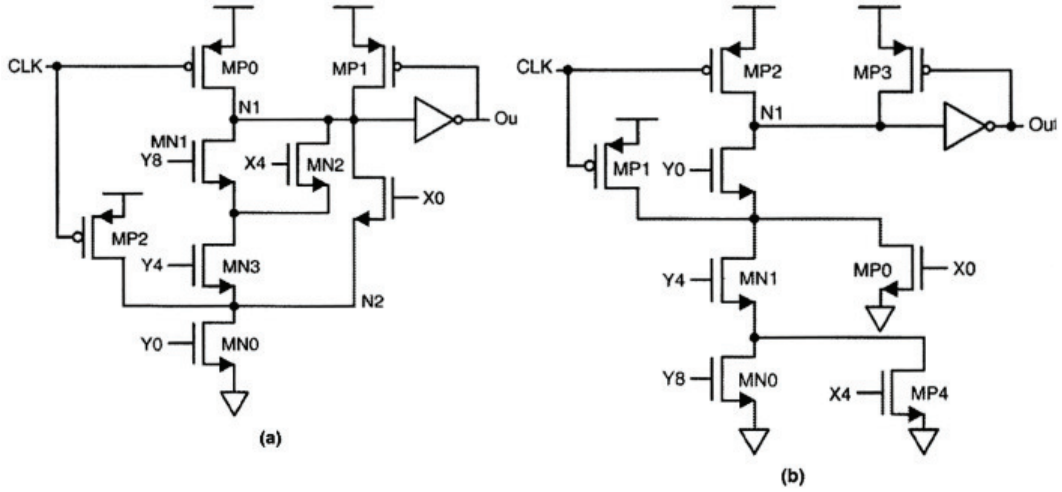


Figure 7.3: Reordered input sequence to mitigate bipolar and MOSFET leakage: (a) Original signal coupling as practiced in bulk and (b) Recommended design practice in SOI.

If the pre-charge cycle extends into the evaluate cycle, charge lost due to bipolar parasitic current is replaced by the pre-charge pMOS device. This method may be used on a selective basis, but since overlap allows DC currents to pass through the chip, care must be exercised. The technique usually requires an adjustable duty cycle clock generator.

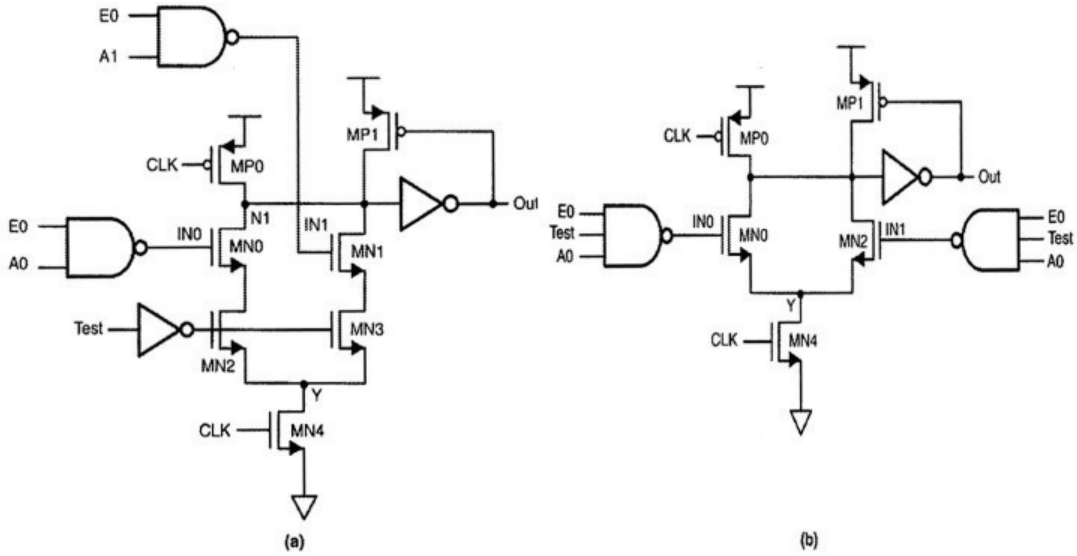


Figure 7.4: Logic Remapping in: (a) Bulk material and (b) partially depleted silicon on insulator

Samsung Exhibit 1010, Page 86 of 204

7.6 Complex Domino

Domino circuits are used to reduce leakage. Logically wide functions are designed by moving half the circuits on the precharge node to a secondary node. Both pre-charged node circuits are evaluated in parallel. The evaluated nodes are combined in the final static buffer producing a single bit output.

Such a combination avoids excessive pre-charge or evaluate delays in bulk, and reduces the total parasitic bipolar current on a single node in SOI. Limiting the bipolar current spike magnitude helps sizing keeper devices (figure 7.5).

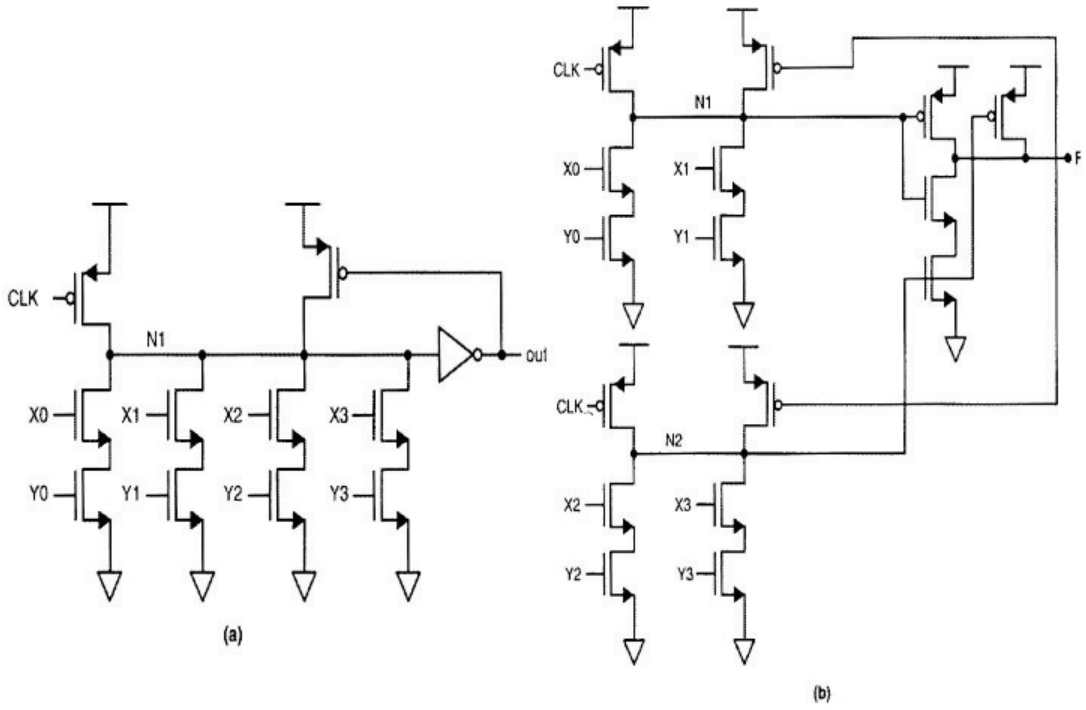


Figure 7.5: Complex domino logic induces substantial parallel leakage, and logical width reduction in SOI. This achieves a given function while cutting node leakage in half.

7.6.1 3-input Domino OR Gate

Domino is a system design style that eliminates nMOS-pMOS glitch problems without introducing pMOS type logic gates. Figure 7.6 shows a 3-input OR domino logic gate [7.4]. Precharge occurs when Φ=0 with C_X charging to a voltage $V_X=V_{DD}$. If one or more of the IN0, IN1 or IN2 inputs are "1", when Φ=1, C_X discharges, the output voltage then changes from a precharge value of 0V to a value of $V_{OUT}=V_{DD}$. When all nMOS transistors are "ON", parasitic bipolar current flows, since both source and drain were at V_{DD}. The output node discharges once Φ goes high. The intermediate node

Samsung Exhibit 1010, Page 87 of 204

will rise initially before falling low when Φ goes high due to gate-drain coupling. Device MN3's body voltage will fall once its turned 'ON'.

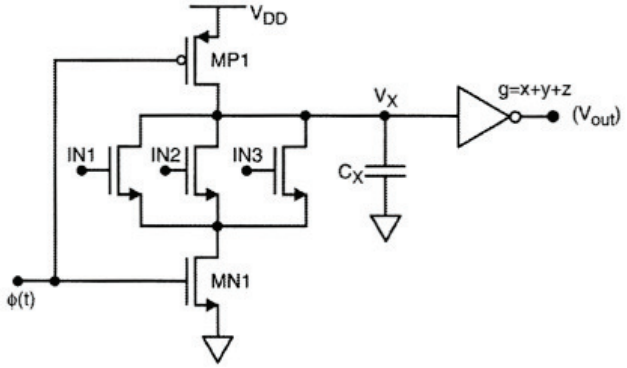


Figure 7.6: Schematic of a 3-input Domino OR Logic Gate.

7.6.2 Dynamic AND-OR Domino Gate

Figure 7.7(a) shows the AND-OR domino gate [7.4] and its simulation waveforms. Input X is maintained high initially and input Y is toggled low to high. With Φ=0, the output node N1 (V_x) is maintained high since MN1 is 'off'. The body voltage of MN1 will be high since the source and drain are high. Once input B is switched high, the body voltage of MN2 tends to go higher due to capacitive coupling.

The intermediate node voltage will be high and at threshold voltage below V_{DD} since there is no rapid discharge path to ground. Once Φ=1, intermediate node N2 discharges to ground through MN3. The body voltage initially couples high before finally settling low. The body voltages of MN1 settles lower once Φ=1. Figure 7.7(b) and (c) show the body and node voltages when input Z is low. Figure 7.7(d) and (e) shows the body and node voltages when Z is high [7.4].

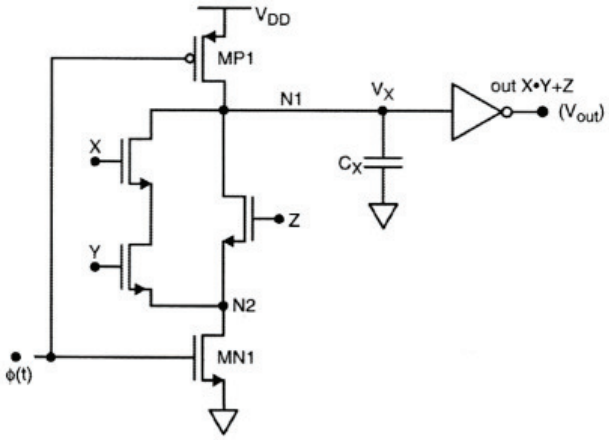


Figure 7.7(a): Dynamic AND-OR schematic.

Samsung Exhibit 1010, Page 88 of 204

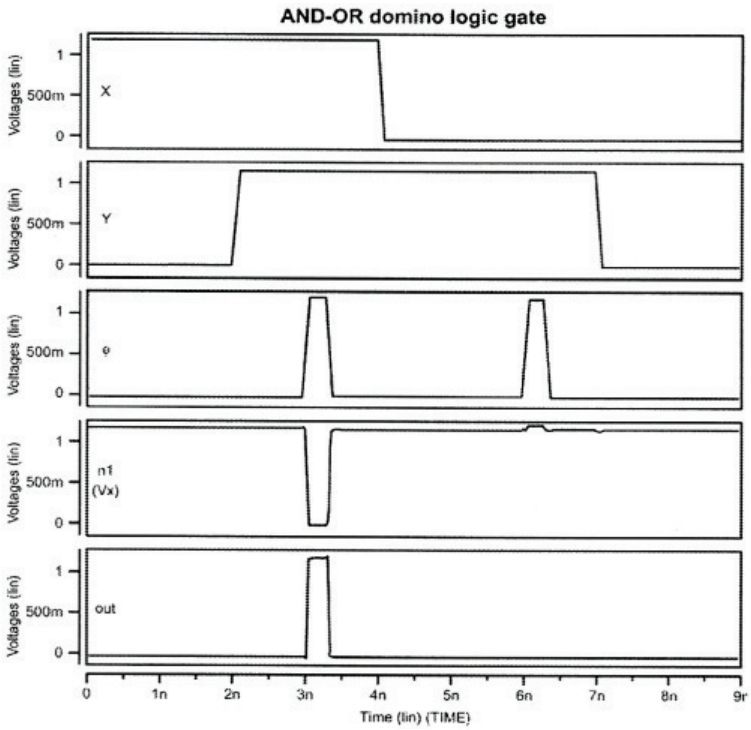


Figure 7.7(b): Waveforms when input A is high and input B is switching low to high. Body voltages with Z low.

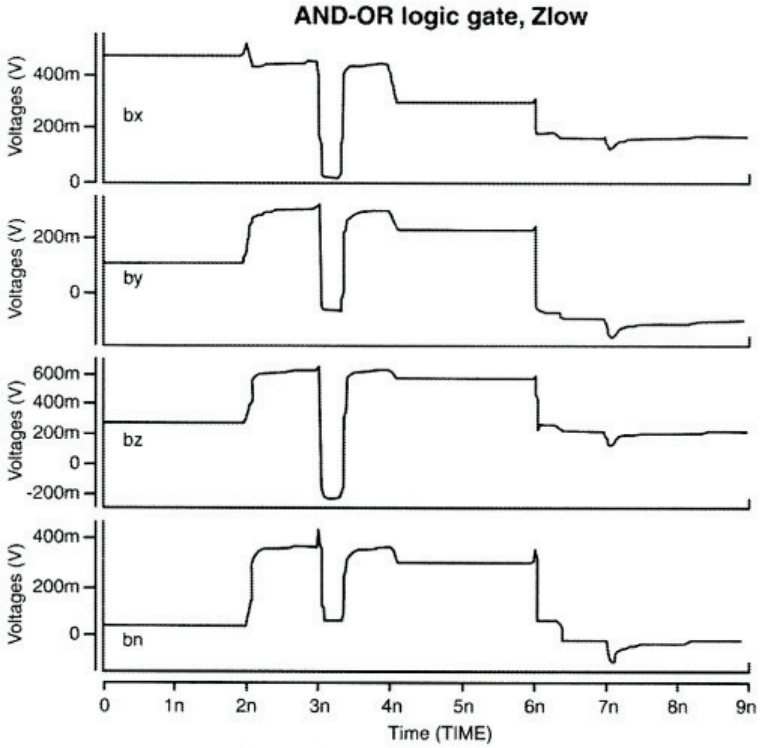


Figure 7.7(c): Waveforms when input A is high and input B is switching low to high node voltages. (Body voltages of devices with inputs X, Y, Z).

Samsung Exhibit 1010, Page 89 of 204

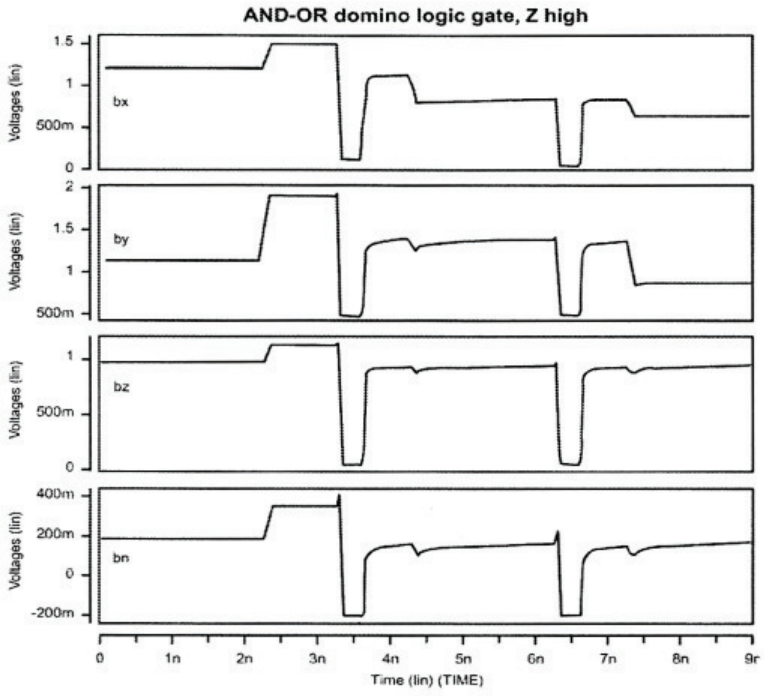


Figure 7.7(d): Node voltages for Dynamic AND-OR when input A is high and input B is switching low to high with Z high.

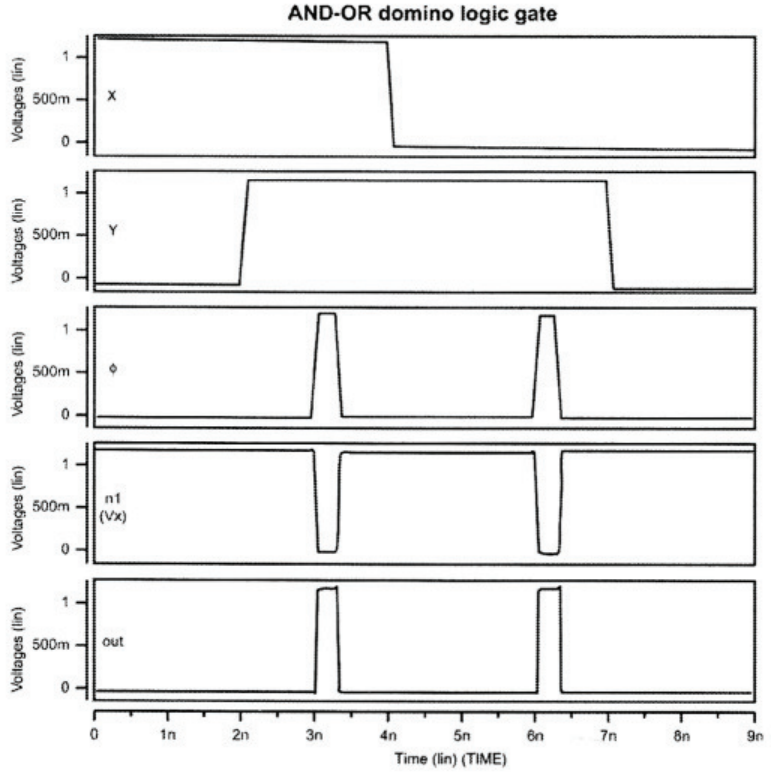


Figure 7.7(e): Node voltages for Dynamic AND-OR when input A is high and input B is switching low to high with Z high.

Samsung Exhibit 1010, Page 90 of 204

7.7 No-Race Logic (NORA)

No-Race logic was introduced to overcome signal race conditions associated with clocked MOSFETs and transmission gates to control data flow. A pass gate exists on input and output of a logic block to control the data flow. If the input to the pass gate is initially high, this signal passes through the logic and to the output. Once the input changes at the same time as the pass gate control changes, wrong data will be sent to the logic reflecting incorrect signal at the output.

Wrong data gets transmitted through the circuit reflecting a race condition between the data intended to be passed and the data passed through the logic circuitry. The signal race problem can be aggravated by the presence of clock skew in which the clock signals are displaced from each other. A large value of clock skew widens the race window, and enhances the possibility of race in the system. Skew is particularly troublesome in high-speed circuits as it limits the operating frequency.

The basic building block of NORA logic is the Φ-section logic network (Figure 7.8) [7.4]. This consists of a dynamic nMOS logic state that is cascaded into a dynamic pMOS logic gate: a C^2MOS latch is used as an output latch. Optional inverters are provided at the outputs of both logic gates for a glitch free domino nMOS-nMOS cascade. Moreover, the ordering of the logic gates may be reversed (pMOS to nMOS) without loss of generality [7.5].

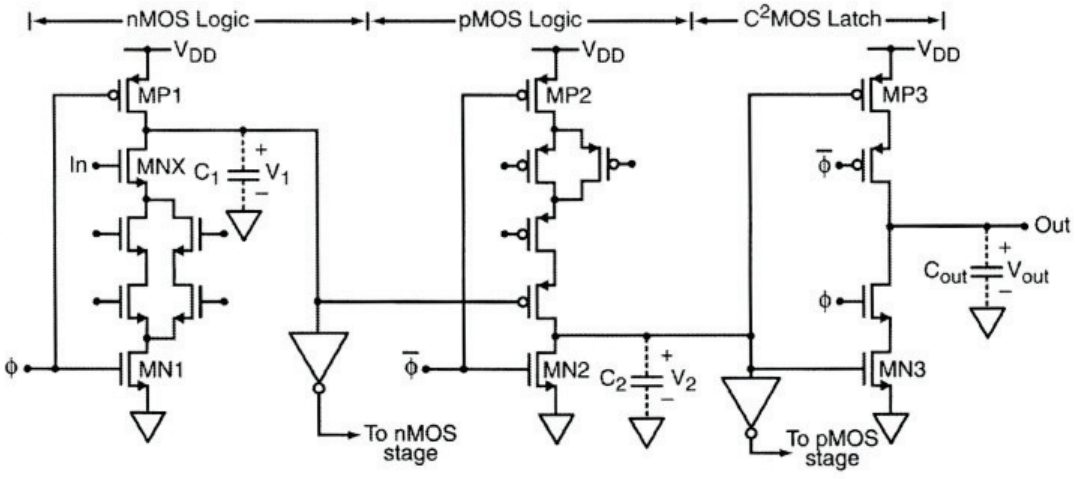


Figure 7.8(a): Schematic of a SOI NORA Φ-section logic network.

The main feature of NORA logic arises in the way the clocks are applied to the logic gates and the latch circuits. Φ=0 defines the precharge interval. The

Samsung Exhibit 1010, Page 91 of 204

output node V1 is precharged high and V2 is low. V_{OUT} is tristated during precharge. The output voltage depends on the amount of charge held in the capacitor (C_{LOAD}). Once the circuit switches to evaluation by Φ=1, the output node attains a voltage level based on the input stored (which is high in this case). Body voltage of the nMOS (MN3) also rises due to body to drain coupling since Φ switches high, as shown in figures 7.8 (b, c).

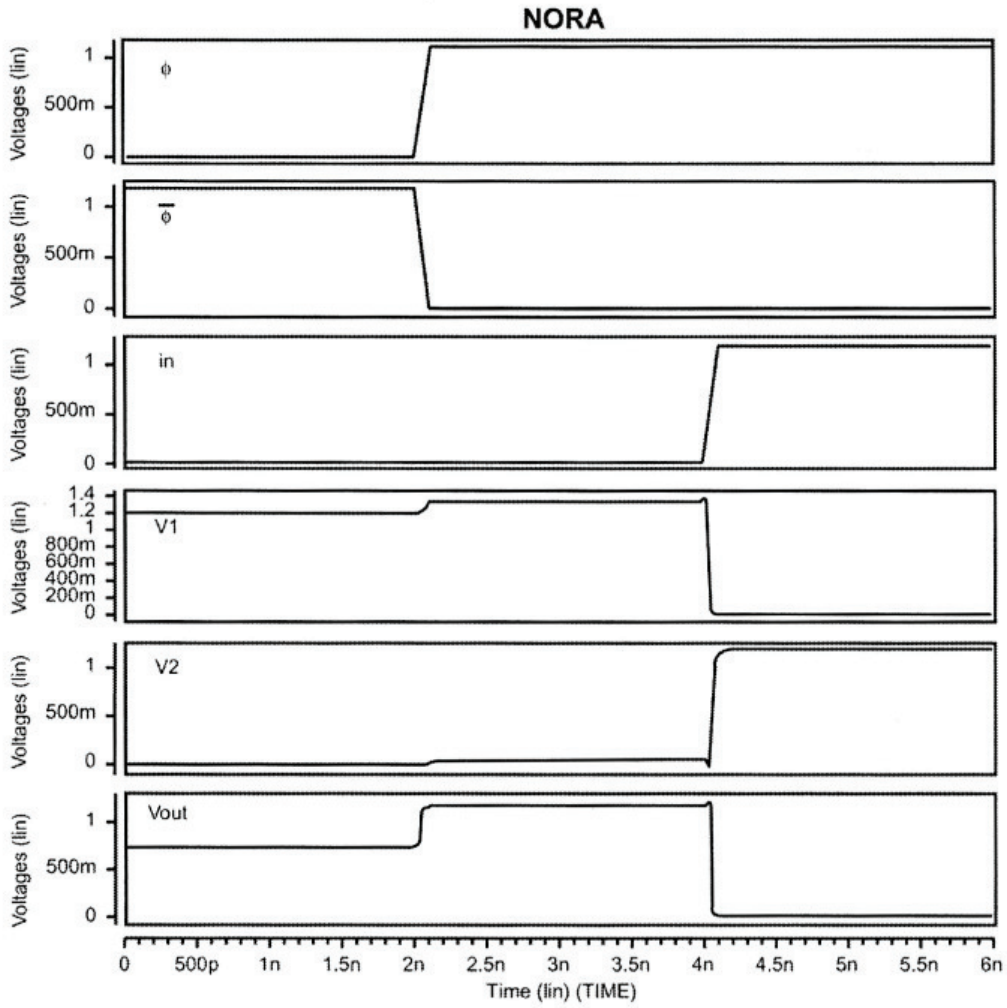


Figure 7.8(b): Additional waveforms of NORA Φ-section logic network

The NORA $\overline{\Phi}$ section may then be constructed (figure 7.9). Dynamic cascade logic gates are used with alternating polarities. This is the similar to the original Φ section except that Φ and $\overline{\Phi}$ are reversed throughout the circuit. The $\overline{\Phi}$ section precharges when Φ=1, and evaluates when Φ=0. The simulation waveforms are shown in figure 7.9(b). The body voltages of critical devices are shown in figure 7.9(c).

Samsung Exhibit 1010, Page 92 of 204

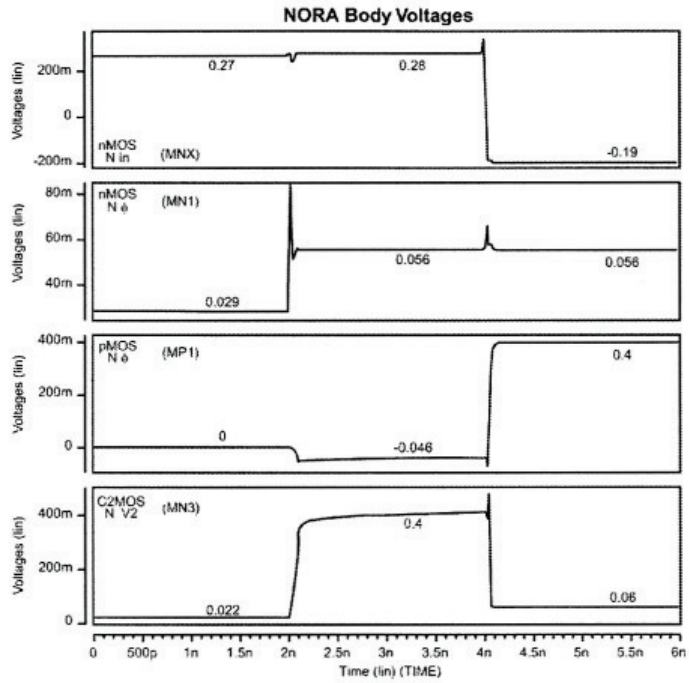


Figure 7.8(c): Body voltages of a NORA Φ-section logic network. Input MN switches low to high, and all the other nMOS are held HIGH.

When $\overline{\Phi}$ is low, the output voltage V1 will be high irrespective of the state of the input transistor MN1. The final chain output, V_{OUT}, will be tristated. Once input MN1 turns 'on', the body voltage of MN1 will rise due to body-gate coupling which in turn couples to the drain node (output of first stage V1). The output voltage V1 of the first stage droops down due to drain-gate capacitance.

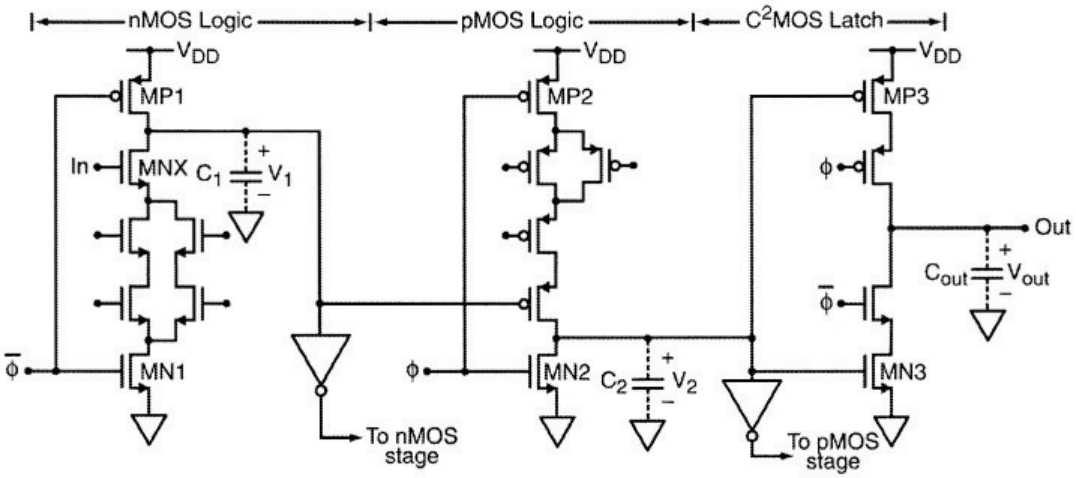


Figure 7.9 (a): NORA $\overline{\Phi}$ logic gates.

Samsung Exhibit 1010, Page 93 of 204

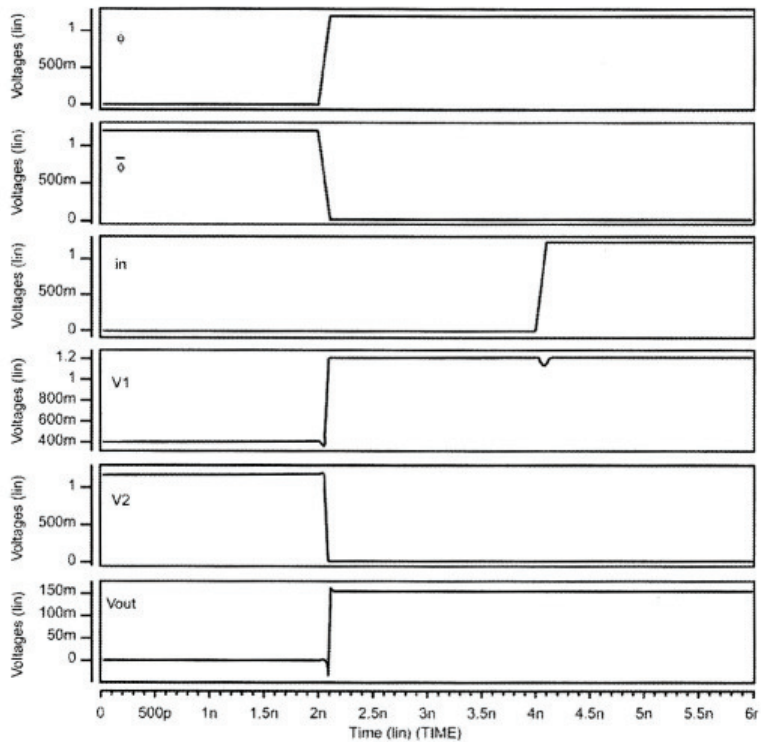


Figure 7.9 (b) NORA $\overline{\Phi}$ Section waveforms. Input N switching and all other nMOS maintained HIGH.

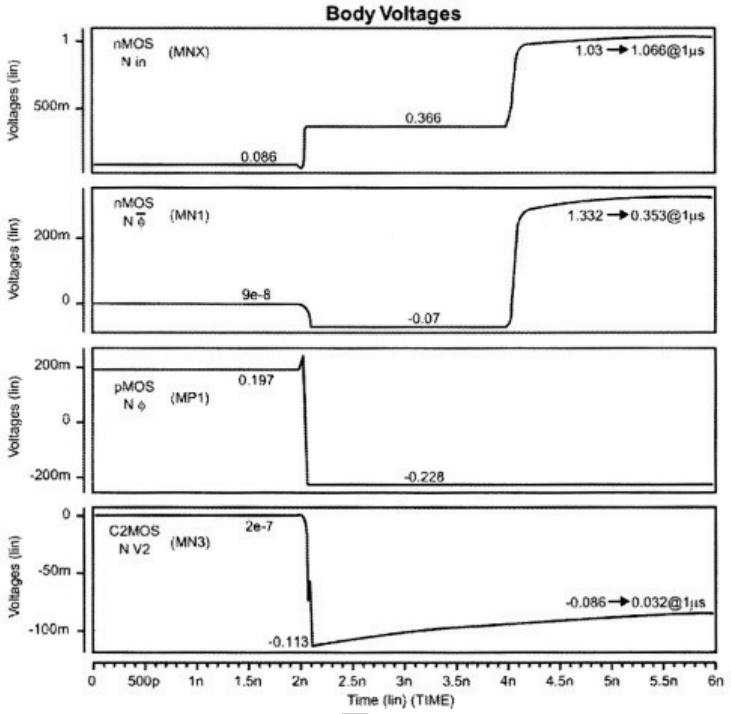


Figure 7.9(c): Body voltages of $\overline{\Phi}$ Section. Input IN switches low to high and other nMOS maintained HIGH.

Samsung Exhibit 1010, Page 94 of 204

The no-race characteristics are obtained by creating alternating cascade of Φ and $\overline{\Phi}$ sections as shown in figure 7.10. The timing of these two sections ensure that signal races do not occur through either section. During precharge Φ=1, the Φ-section are in evaluation and $\overline{\Phi}$ sections precharging. The inputs are valid during this period and produce results at the output. However, the next logic $\overline{\Phi}$ section is precharging since Φ=1, and does not accept input data values. This eliminates race conditions through the $\overline{\Phi}$ sections. Similarly, when Φ=0, the Φ-sections are in precharge and block data transmission when $\overline{\Phi}$ evaluates. The sections take turns evaluating the inputs and block data transmission as the clock frequency oscillates [7.5]. Figure 7.10(b) shows a pipelined NORA CMOS logic with C^2MOS logic.

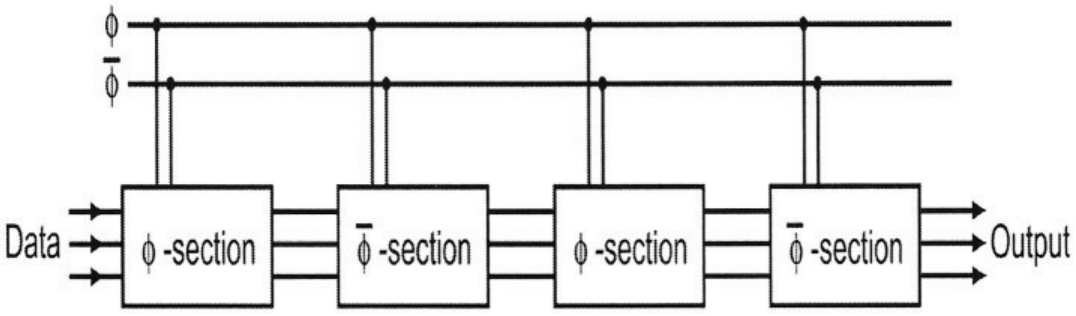


Figure 7.10(a): A NORA Pipeline cascade.

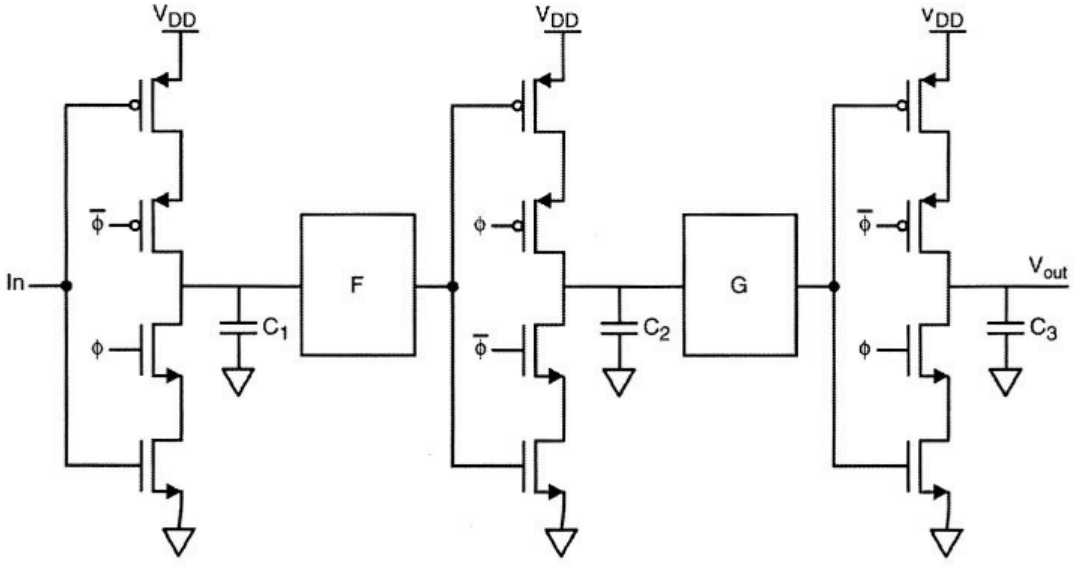


Figure 7.10 (b) Pipelined NORA CMOS logic with C^2MOS. Race free as long as all the logic functions F and G between latches are non-inverting.

Samsung Exhibit 1010, Page 95 of 204

7.8 Dynamic Noise Suppression

The parasitic bipolar response of a floating body in partially depleted SOI MOSFETs becomes more prominent at higher voltages. Most products undergo burn-in and/or voltage stress prior to shipment to determine reliability due to processing defects. Dynamic logic circuits maintain functionality but degrade in performance at elevated voltages.

Figure 7.11(a) shows a conventional domino circuit, and figure 7.11(b) shows the improved hysterisis free circuit. For robust functionality with speed trade-offs, the feedback transistor is turned ON to avoid hysteresis and is turned OFF when performance is critical. The feedback adds drain capacitance to the evaluate node slowing down the output. Figure 7.12 uses dynamic feedback to achieve the same functionality. Device MP1 should be large and keeper device MP5 should be small to minimize cycle time during functionality testing. During burn-in, MP1 must be small and MP5 large to prevent bipolar leakage.

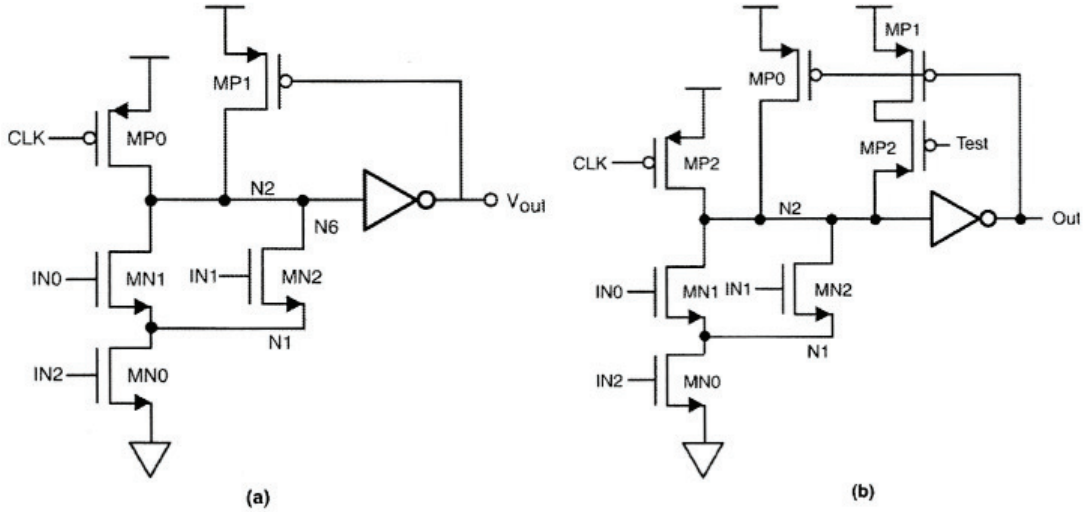


Figure 7.11: Dynamic noise suppression during high voltage stress (a) Bulk (b) additional feedback in SOI for supplement charge replacement.

During stress operation, the TEST signal dynamically increases pMOS drive strength of the parallel pMOS transistors by turning MN2 'OFF' and turning 'ON' MP4. This helps suppress noise at higher voltages.

During operational mode, MN2 is 'ON' and MP4 is 'OFF'. The sum of the device widths MP1, MP3, MP5 are the same as the precharge and the keeper devices in figure 7.5. The effective precharge device is maximized to reduce the delay for restore operation [7.1].

Samsung Exhibit 1010, Page 96 of 204

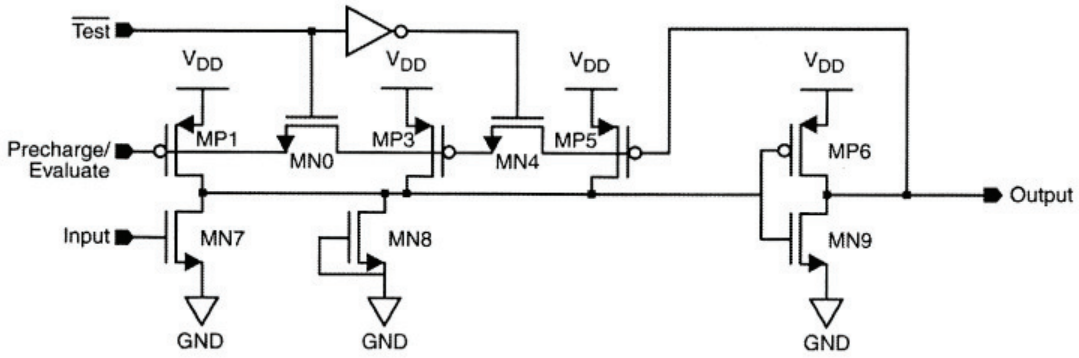


Figure 7.12: Dynamic feedback technique

7.9 Design Issues in Dynamic 2-way NAND Logic

Timing rules for modern VLSI designs are typically generated based on worst case process corners, supply, voltage, temperature, slew rate and switching patterns. For bulk CMOS, the pattern dependency of the stacked configuration degrades timing rules.

Figure 7.13(a) shows a simple dynamic 2-way NAND. Switching MN1 (when V_{IN1} switches from low to high and V_{IN2} stays High) to pull dynamic node N2 low is slower than switching MN2. This is because the voltage V1 at Node 1 is at V_{IN2}-V_T initially.

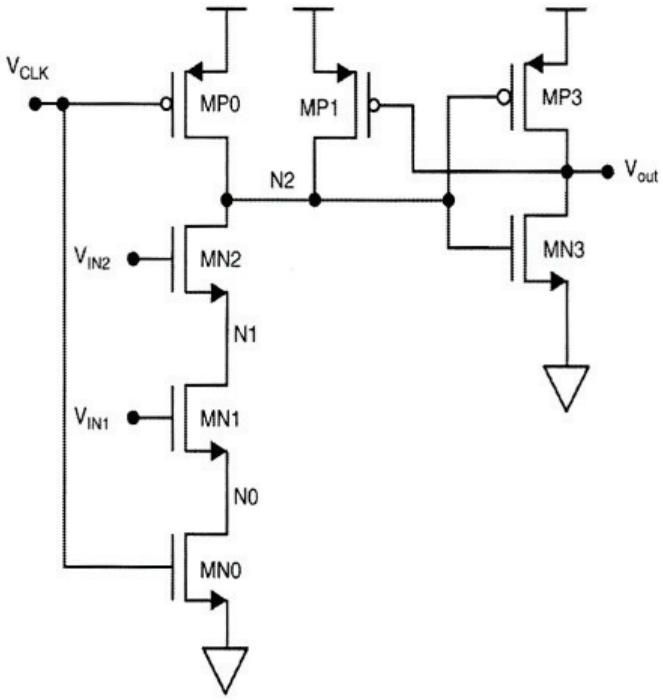


Figure 7.13(a): Schematic of a simple dynamic 2-way NAND Circuit [7.6].

Samsung Exhibit 1010, Page 97 of 204

MN2 suffers from the reverse body effect and thus has high threshold voltage initially. (With its source node N1 high and its body grounded, there is a large reverse bias between body and source of MN2, resulting in a high threshold voltage.)

Node N2 is at V_{DD} during clock low. Node N1 is high, but the body voltage of MN1 is low. Once the input to transistor MN1 turns 'ON', the body voltage of MN1 increases (0.87V) due to body to gate capacitance. The body voltage of MN0 is 0.389V when CLK is low and input high.

Waveforms are shown in figure 7.13(b)-(d). Once the clock transitions high, the nodes N0, N1 and N2 discharge to ground, and the respective nMOS body voltages also fall to ground [7.6].

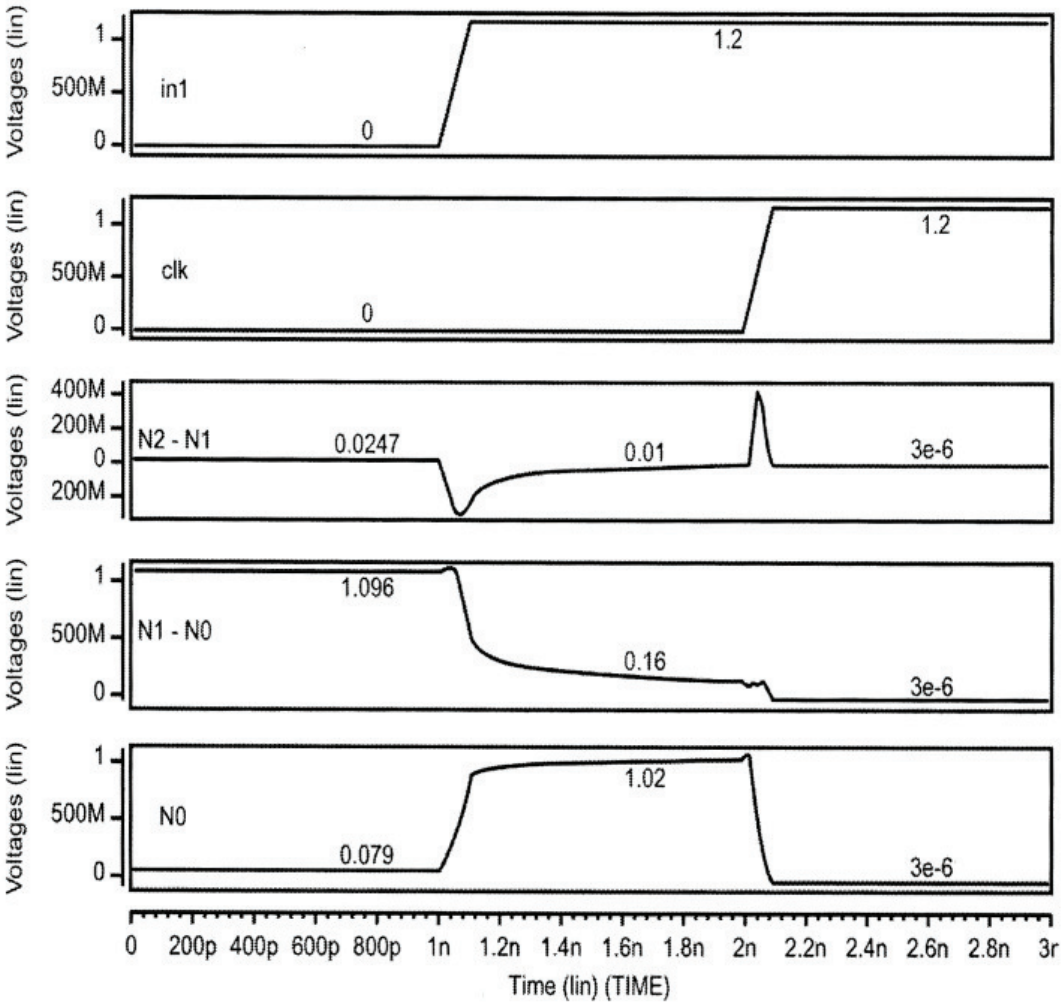


Figure 7.13(b): Dynamic 2-way Nand gate simulation waveforms. Vin2 = H.

Samsung Exhibit 1010, Page 98 of 204

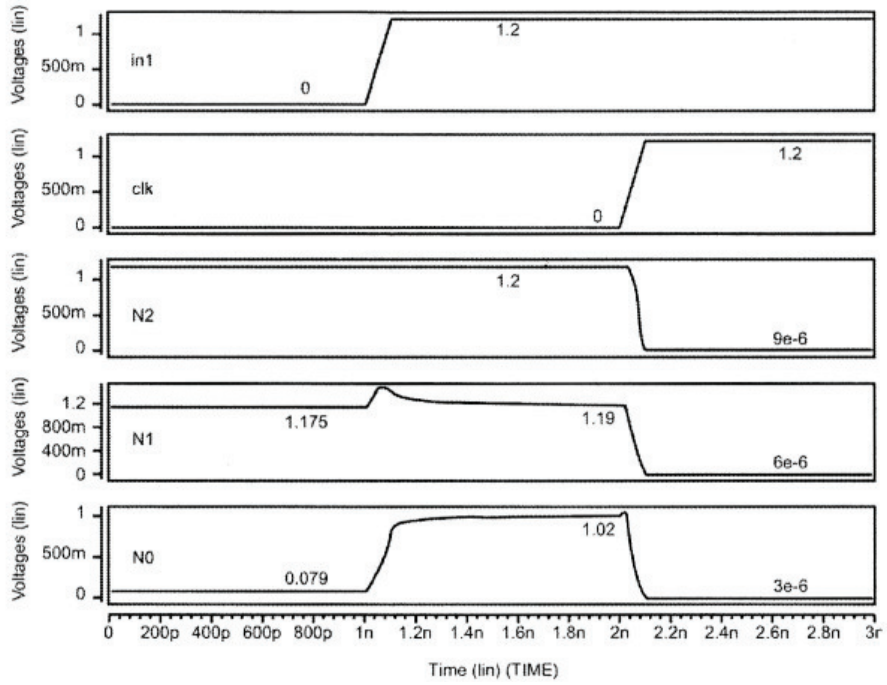


Figure 7.13(c): Intermediate node N0, N1, N2 voltages.

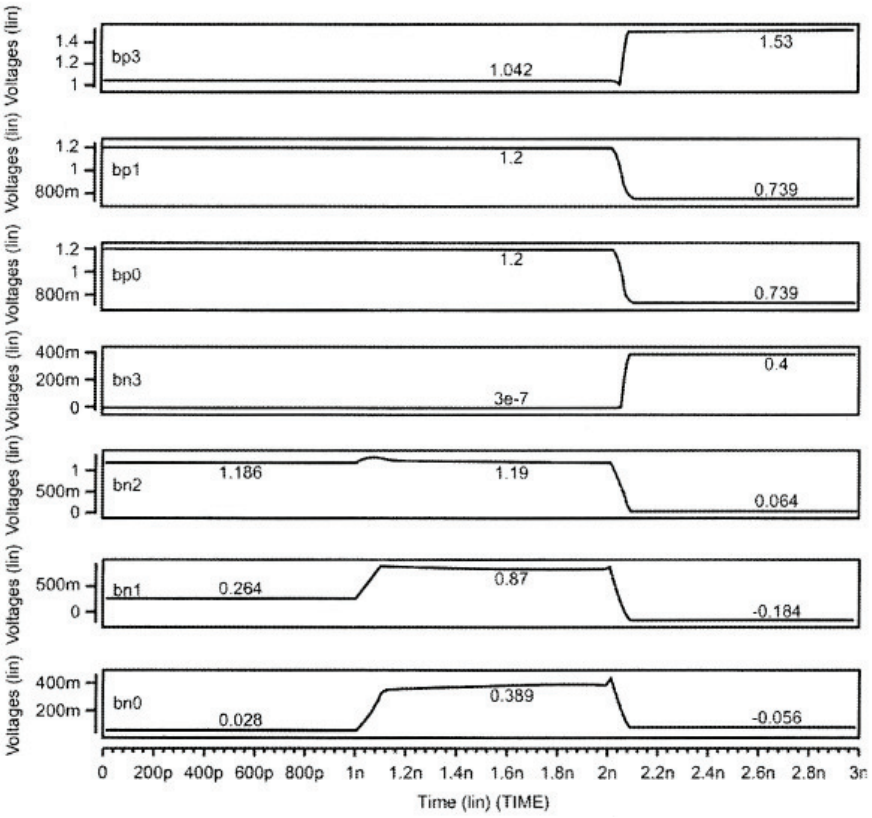


Figure 7.13(d): Body voltages of pull-down nMOS devices and pull–up pMOS devices

Samsung Exhibit 1010, Page 99 of 204

For the case of switching the top transistor MN2, full V_{DD} is present as V_{DS} across the transistor. Also, current to pull down node N2 is immediately available once MN2 switches 'ON'. While the reduced parasitic in SOI structure improves both switching cases, the improvement for the bottom transistor switching case is particularly significant.

The body voltage of MN2 lies between the voltages of nodes N2 and N1, hence, is very close to V_{DD} before N1 switches. Threshold voltage of MN2 is significantly reduced. Node N1 voltage is closer to V_{DD} than in bulk case, resulting in larger V_{DS} across MN1 to start with. The body voltage of MN1 is between N1 and ground, thus reducing V_T of MN1. The timing rules are therefore improved for the nMOS stack and pMOS stacked configurations in SOI.

Timing rules for pass transistor-based circuits, such as complementary pass gate logic devices, [7.7-7.9] are improved, primarily as a result of lack of reverse body effect in floating body SOI. The timing rules for some other circuit topologies, however, are degraded by the parasitic bipolar effect and transient threshold voltage variation. Sizing-up the holding devices, adding body contacts or widening design margin degrades circuit speed, area and timing rules.

7.10 Dynamic 2-Way OR Circuit

Parasitic bipolar leakage currents can be disastrous in dynamic logic circuits [7.10, 7.11]. Figure 7.14(a) shows a dynamic 2-way OR-AND circuit [7.12]. The dynamic circuit with nMOS stack and the evaluation is designed similar to the static OR-AND circuit discussed in chapter 6. Assume input to MN1 'high' and MN2 'low'. During precharge, when clock is low, node N2 is high, and V_{OUT} is low. Thus N1 is at V_{DD}-V_T. When MN1 switches low, due to gate source coupling node N1 couples down to a lower voltage. Once V_{CLK} goes high the circuit switches to the evaluate state.

The gate to source coupling at node N2 and parasitic bipolar current attempt to pull node N1 to ground. MP1 has to be sized very carefully, such that it is strong enough to maintain N1 high. Figure 7.14(b) shows the waveforms for the dynamic 2-way OR circuit.

When CLK is low and MN1 'high', node N1 voltage is at V_{DD}, once the input to MN1 switches low, the voltage at node N1 goes low due to the gate-body capacitance. The body voltage of node N1 is coupled down lower following switching of MN1.

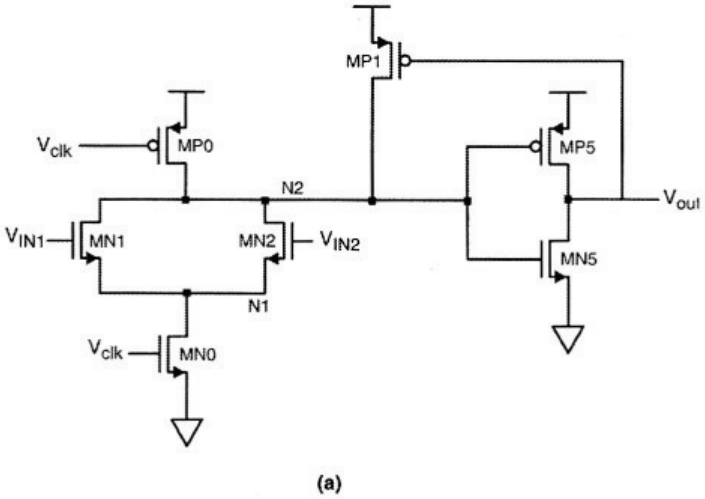


Figure 7.14(a): Schematic of 2-way dynamic-OR CMOS gate with floating bodies [7.12].

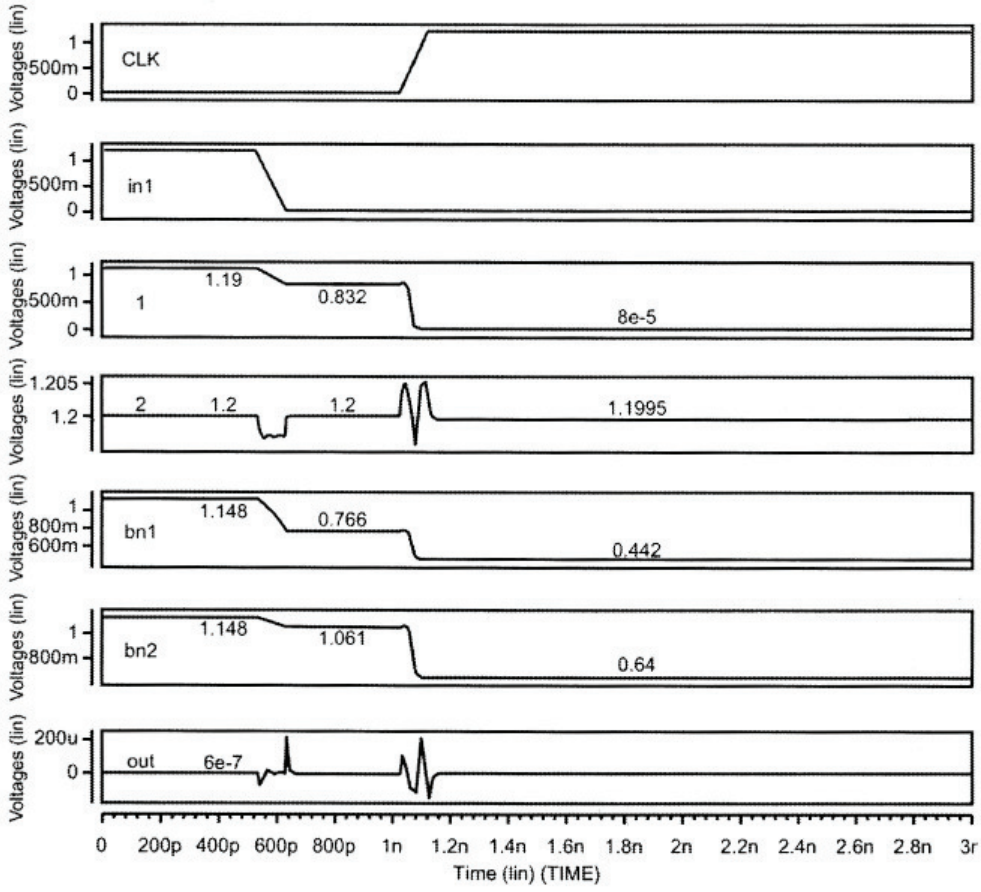


Figure 7.14(b): Dynamic OR gate switching wveforms. Node N1 voltage drops from 1.119V to 0.832V after input goes low and subsequently drops to ground after CLK high.

7.11 Dynamic Cascade Switch Logic

As with many other dynamic circuits, designing with SOI for cascade voltage switch logic (CVSL) circuits requires consideration of body effects. Multilevel voltage switch current steering type circuits may encounter much more complicated situations resulting in logic state errors [7.13]. Figure shows the schematic of a 3-input dynamic CVSL XOR gate [7.6]. In the pre-charge phase, all branches are inactive because the clocked evaluation transistor N0 is 'off ' (Figure 7.15). Node N1 and N2 are pre-charged to V_{DD}. Due to the differential input, all common source nodes in all cascade levels are 'HIGH'. Consequently, all logic transistors with LOW inputs are set up in a condition with both their drains and sources HIGH (thus, bodies are 'high' also). When the circuit evaluates, the common source nodes in the active branches are pulled 'low' and parasitic bipolar currents flow through these 'OFF' transistors. Because of the cross-coupled drain connection, each common source node is also a common drain node of the lower cascade level. Pulling down these common drain nodes causes 'inverse mode' parasitic bipolar current to flow from source to drain in the inactive branch 'off' transistors (figure 7.16) [7.6, 7.13].

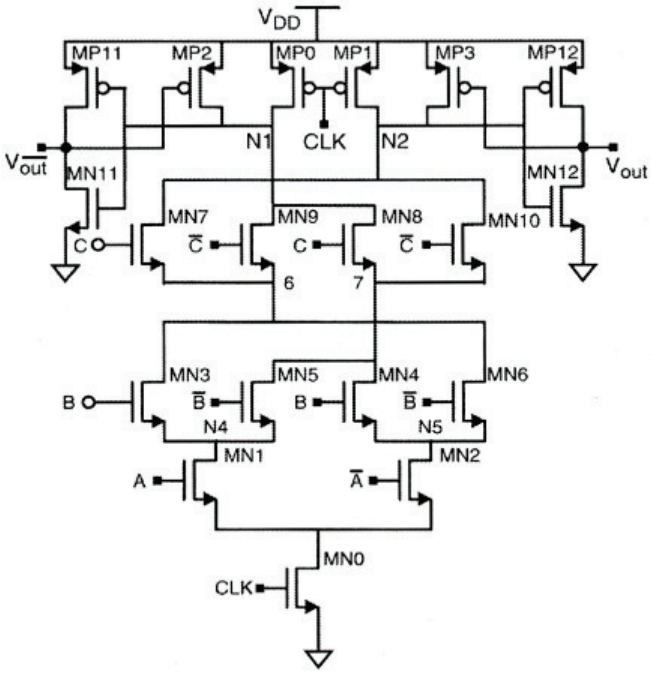


Figure 7.15: Schematics of a 3-input Dynamic Cascade voltage switch logic (CVSL) XOR Circuit [7.13].

Evaluating figure 7.16, if the inputs to the XOR gate A, B and C are (0,1,1) respectively, during clock low, there is no path to ground with MN0 'OFF'. When clock switches high and since MN1, MN3 and MN7 are also "high", node N2 is maintained high. Since transistor MN1 is 'ON' and MN2 is

Samsung Exhibit 1010, Page 102 of 204

'OFF', the body voltage of MN1 falls to ground, while the body voltage of MN2 remains 'high'. The N1 and N2 node voltages are low and high respectively and, alternatively, nodes N6 and N7 are high and low. Transistors with inputs connected to {A (N1), $\overline{B}$(N5/N6), and C (N9/N10)} having zero gate bias are susceptible to parasitic bipolar effect during evaluation. The inverse mode parasitic bipolar currents flow through the 'OFF' transistors N5 and N9. Their voltages therefore droop much faster and earlier than the source nodes. The normal mode parasitic bipolar current pulls down high node N2, resulting in an erroneous state where both node N1 and node N2 are LOW.

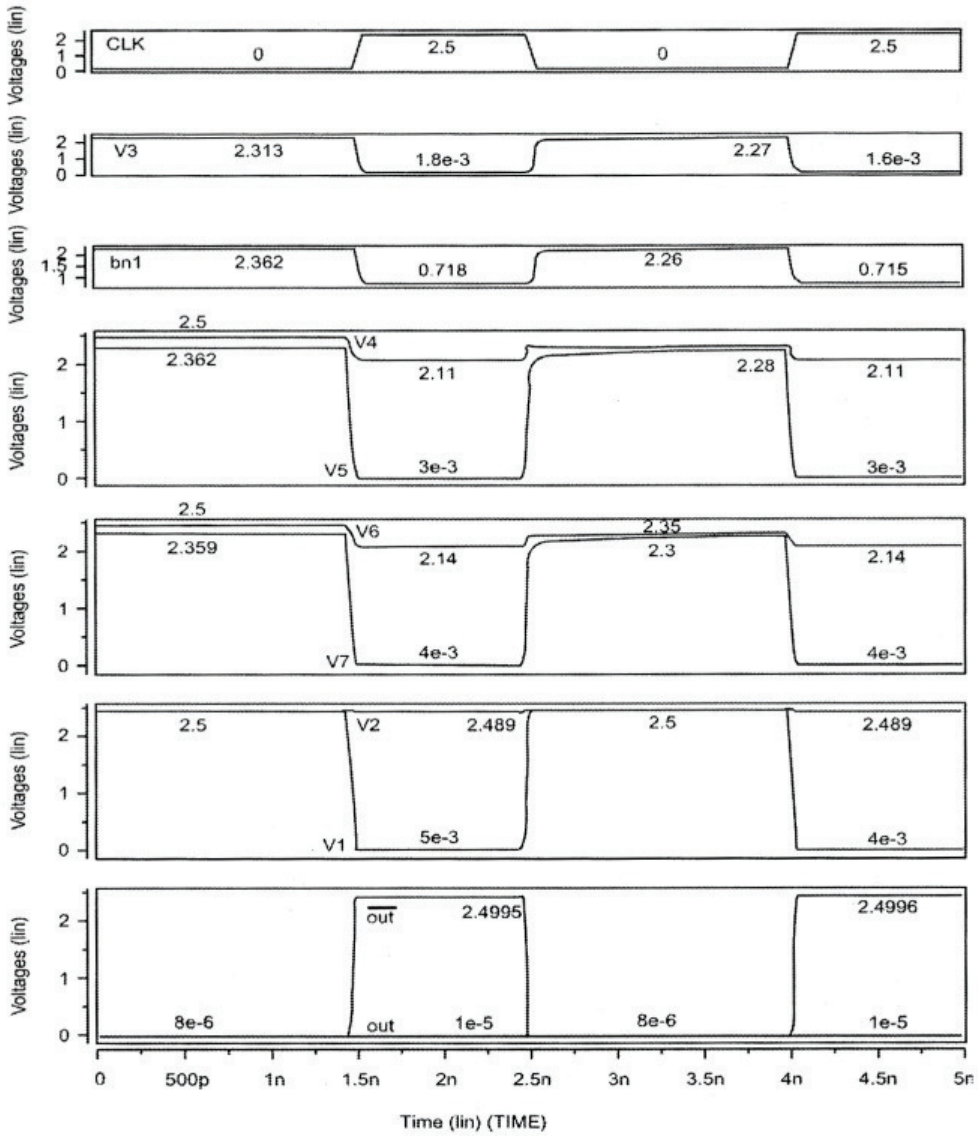


Figure 7.16: Switching Waveforms of dynamic CVSL XOR. Here, Vdd=2.5V. Input (A,B,C) = (0,1,1). The internal node voltages and the output are shown with there corresponding pairs.

Parasitic bipolar currents in the second evaluation cycle are substantially lower than those in the first evaluation cycle. This hysteretic behaviour stems from the time interval for the second pre-charge cycle being shorter than the body voltage charge up time. Cascade current switch logic are also normally used for faster logic performance trading off current consumption.

7.12 Clocked CMOS

Clocked CMOS (C^2MOS) is a logic family that combines static logic design with clock synchronization. Many small and medium scale integrated circuits have used C^2MOS logic. This technique is still implemented in modern VLSI designs as dynamic no-race (NORA) circuits explained earlier.

Figure 7.17 shows a C^2MOS gate. The inputs are connected as a static circuit, two pass gates, nMOS and pMOS are inserted between the output nodes with Φ and $\overline{\Phi}$ as the select signal. When Φ is high, both control pass-gates are 'ON', connecting the logic to the output node, and the gate behaves as its static equivalent circuit. Switching times are longer than static designs due to additional parasitics. When Φ=0, the output is isolated from the rest of the circuit [7.4].

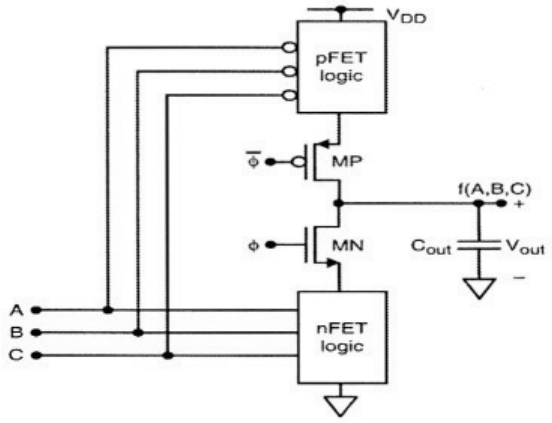


Figure 7.17: Clocked CMOS Gate Circuit [7.4].

Figure 7.18 shows a C^2MOS inverter and associated waveforms. When Φ=1, both clocked MOSFETs are active and the input controls the logic MOSFETs MP1 and MN1. If V_{IN}=0V, then V_{OUT}=V_{DD}, an input V_{IN}=V_{DD} results in V_{OUT} = 0V. With the presence of C_P and C_N, both t_{LH} and t_{HL} are larger than for a static inverter. The charging time constants are given by:

$$\tau_P = (R_{P1}+R_P)\, C_{OUT} + R_{P1}C_P$$

R_{P1} and R_{P2} are the pMOS resistances. The output is driven to a high impedance state when the clock transitions low (Φ=0). The output voltage is maintained at V_{OUT} by charge storage on C_{OUT}. The voltages V_P and V_N

Samsung Exhibit 1010, Page 104 of 204

across the capacitors C_P and C_N, respectively, can be changed by input. This votlage can also be affected by the gate-drain and drain-body coupling at V_N. The voltages from V_P and V_N are isolated from the output by the passgate. The body voltage of MN1 couples high due to gate-body capacitance when Φ=1 and settles at an intermediate voltage after Φ switches low. Body effect is minimized in SOI. A spike in the output occurs with input switching high and Φ low. This is due to the combined capacitive coupling from gate-drain and gate-body of MN1 and V_N. Due to source/drain parasitic bipolar leakage of the nMOS (closer to output), V_N spike (trying to pull low) is reflected on the output. As nMOS devices are added to the pull down, body effect is reduced and less variation occurs in threshold voltages.

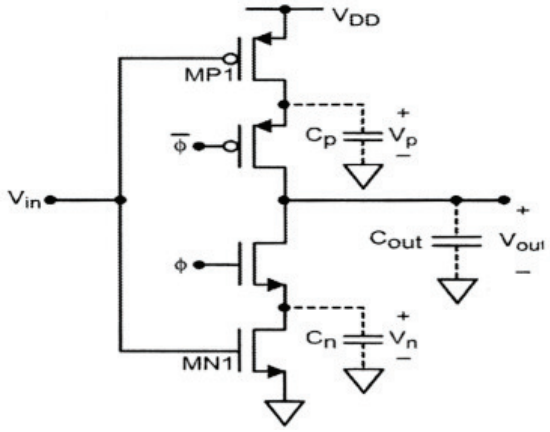


Figure 7.18(a): Clocked SOI CMOS inverter with floating bodies

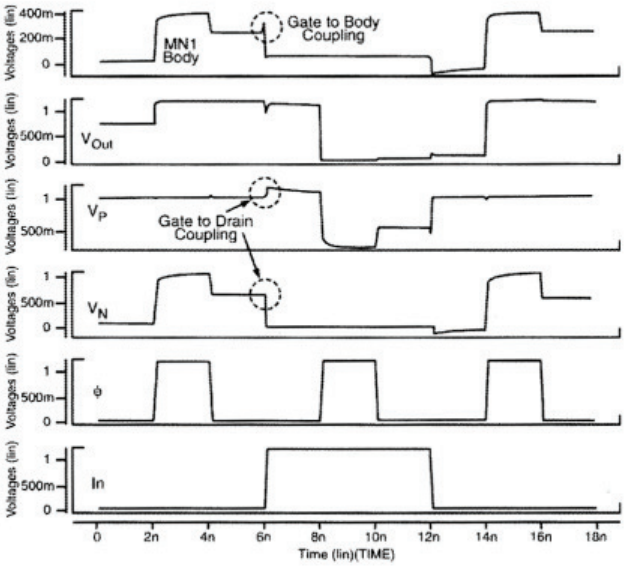


Figure 7.18(b): Waveforms of the Clocked CMOS inverter. The body voltage of MN1 raises with input for a short period of time before settling down. Once input (MN1) goes high, body switches low.

Samsung Exhibit 1010, Page 105 of 204

Figure 7.19(a) shows a clocked latch oppositely phased inverters. The timing is chosen to insure that when one inverter input is high, the other is tri-stated. The operation of this circuit is similar to the master slave D-flip flop. When Φ=1, the output of the first inverter is $\overline{Vin}$ and output of the second inverter is the same as input. Once the signal Φ switches low, the first stage output is tri-stated and the second stage accepts the $\overline{Vin}$ as input.

Figure 7.19(b) shows the waveforms. When Φ=0 and V_{IN} is low, output V_O is tri-stated, but pulls up when Φ switches high. When Φ switches low, output V_O couples low due to gate/drain coupling and drain/body capacitance. The body voltage is affected by switching the input voltage of the top nMOS device in the stack. While Φ=1, the output node is isolated from the input.

Output node V_X is V_T above ground during the next cycle before Φ goes low and then pulls high with Φ going high. V_O rises with Φ transitioninghigh due to drain-gate coupling and drain-body coupling. The voltage at the node between the two nMOS transistors in the pull down stack varies with gate-drain and body-drain coupling. Charge sharing affects are reduced in SOI nMOS stack compared to bulk.

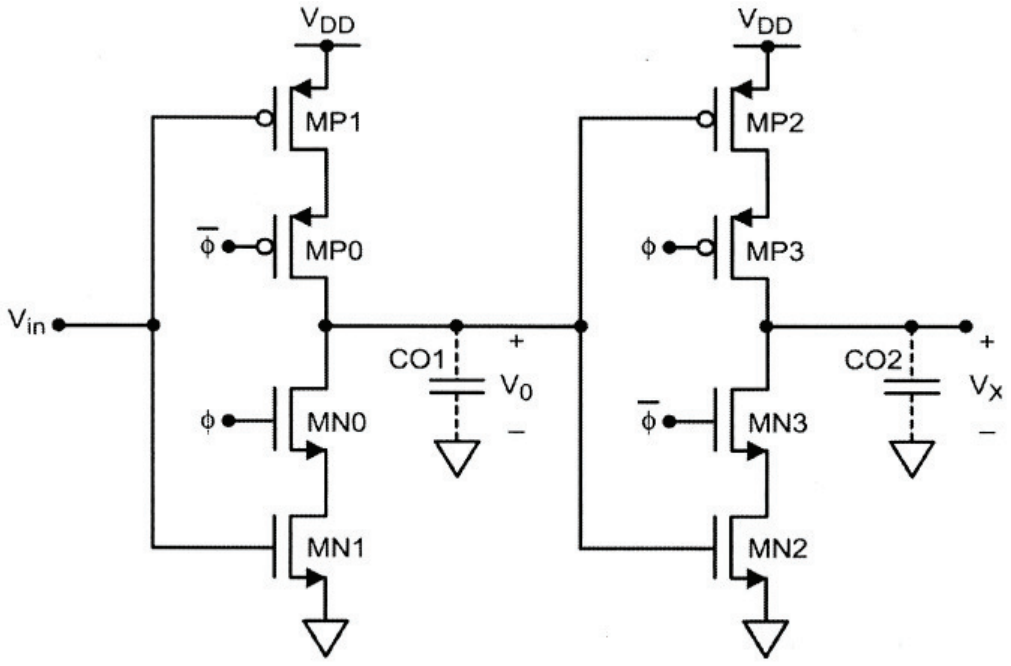


Figure 7.19(a): Clocked latch oppositely phased inverter schematic.

Samsung Exhibit 1010, Page 106 of 204

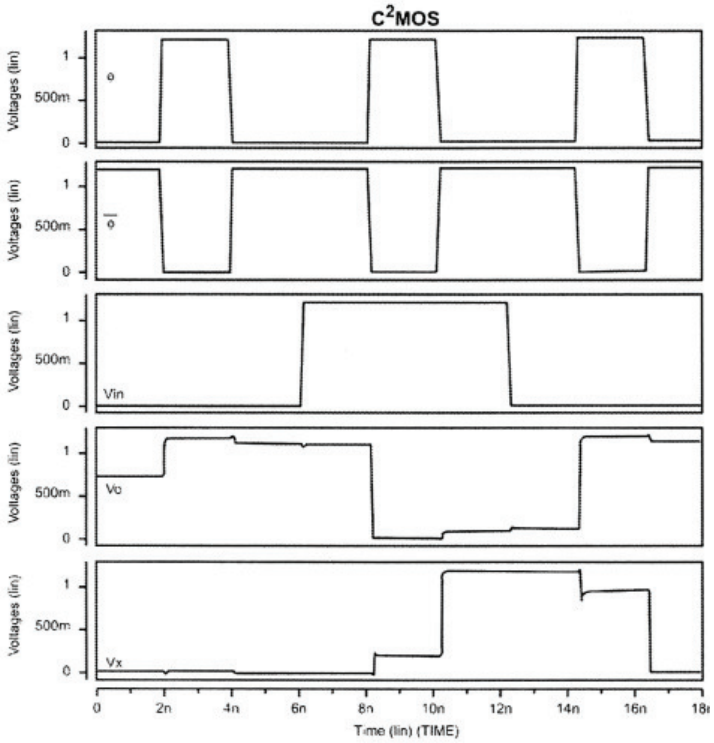
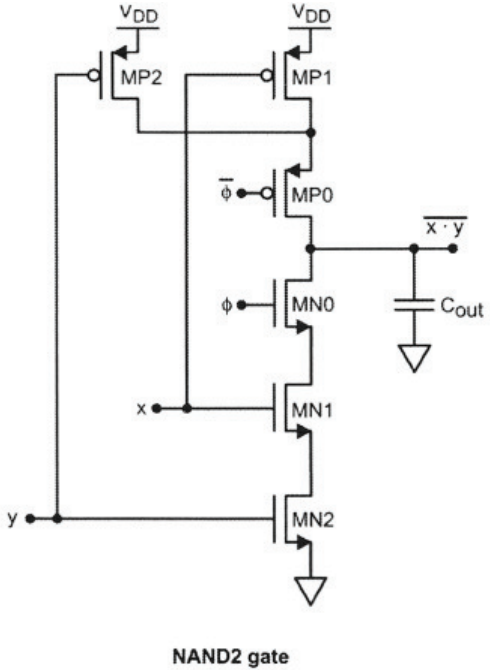


Figure 7.19(b): V_O and V_X for clocked Latch oppositely phased inverter.

Since C²MOS is based on static logic, it is simpler to design an entire family of gates with the same characteristics. Examples are the C²MOS NAND2 and NOR2 schematics shown in figures 7.20 and 7.21.



NAND2 gate

Figure 7.20: Schematic of C²MOS NAND2 logic gate.

Samsung Exhibit 1010, Page 107 of 204

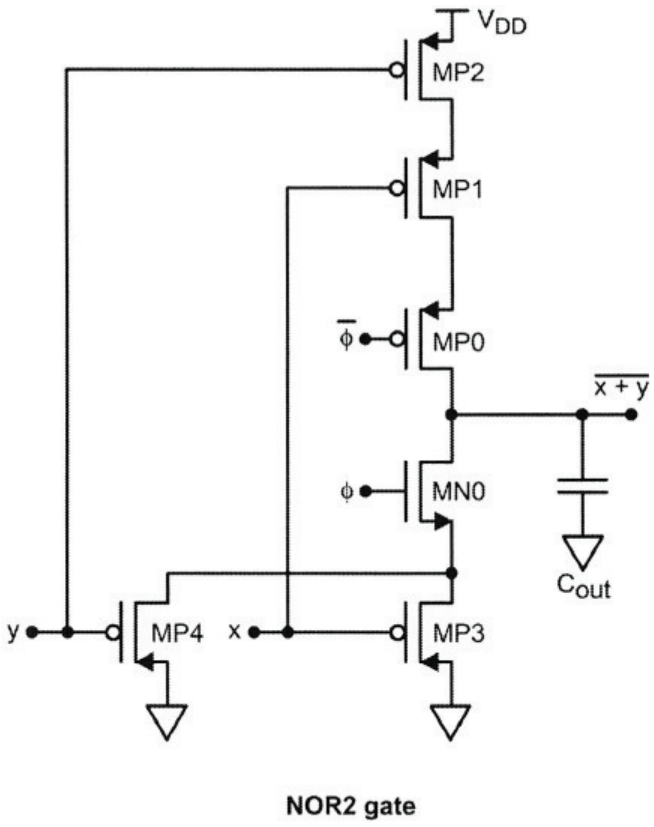


Figure 7.21: Schematic of C^2MOS NOR2 logic gate.

7.13 Pulse Stretching in Dynamic Circuits

The floating body induced transient threshold voltage exists even when the parasitic bipolar current is not significant enough to affect circuit operation. Threshold voltage variations cause a frequency dependent pulse stretching effect in partially depleted SOI CMOS inverter chains [7.14]. Such behaviour is attributed to the imbalance in charge between logic states during switching.

Figure 7.22 shows an inverter chain and depicts the pulse-stretching phenomenon. If the inverter is 'low' for a long period of time, majority carriers deplete the subsequent stage nMOS with a 'high' input. This causes low inverter inputs to accumulate most of the majority carriers, meaning that odd stages have more majority carriers than the even stages.

When the chain switches, the first stage switches with a higher current drive (lower nMOS V_T) than the second stage. The same trend extends down the entire chain. All odd stages nMOS gate inputs are LOW and even stages HIGH. Equilibrium body voltage is reached when charging and discharging currents are equal [7.4].

Samsung Exhibit 1010, Page 108 of 204

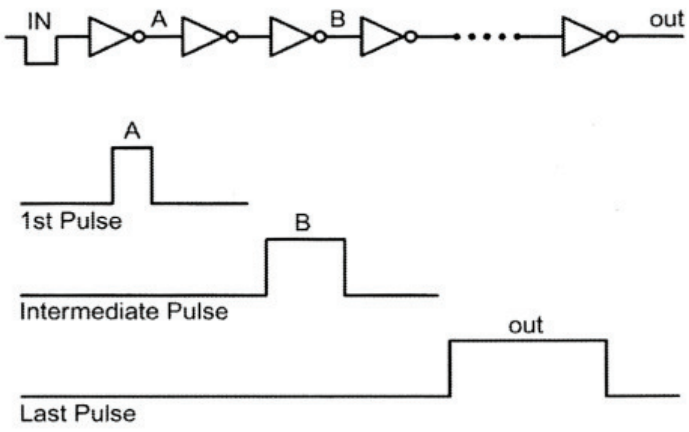


Figure 7.22: Partially depleted SOI inverter chain showing the sequence of input pulse stretching across the chain [7.14].

For even stage devices, with gate inputs HIGH and drains LOW, the body voltages are LOW, resulting in higher threshold voltage. The pMOS devices operate in a complementary fashion. Odd stage pMOS devices have reduced majority body charges and thus higher threshold voltages, while the even stage pMOS devices have more charge and lower V_T. Thus, when the input pulse rises from a sustained LOW period to HIGH, the rising edge of the input pulse propagates down the chain faster than the falling edge of the pulse. This is because all the devices involved with the propagation of the rising edge have lower threshold voltages, and the ones associated with falling stages have higher threshold voltages. The pulse, therefore, stretches as it propagates down the chain (Figure 7.22).

The pulse stretching depends on input frequency and supply voltage V_{DD}. As input frequency increases, the pulse stretching decreases because there is less time for the devices to switch and recover to equilibrium. Pulse stretching also decreases with increased V_{DD}. Drain induced body depletion reduces the equilibrium number of holes in the body and is more significant at higher supply voltages. Thus, the difference of equilibrium number of holes between the two states (figures 7.22(a) and 7.22(b)) diminishes with increasing V_{DD}.

Pulse stretching has several implications on the circuit operation. It affects the duty cycle and degrades clock skew and jitter in a clock distribution network. Circuit timing methodology is complicated and performance is degraded [7.15, 7.16]. Figure 7.23 [7.6] shows the pulse stretching per stage in a 480-stage PD-SOI CMOS inverter versus input pulse frequency and V_{DD}.

Samsung Exhibit 1010, Page 109 of 204

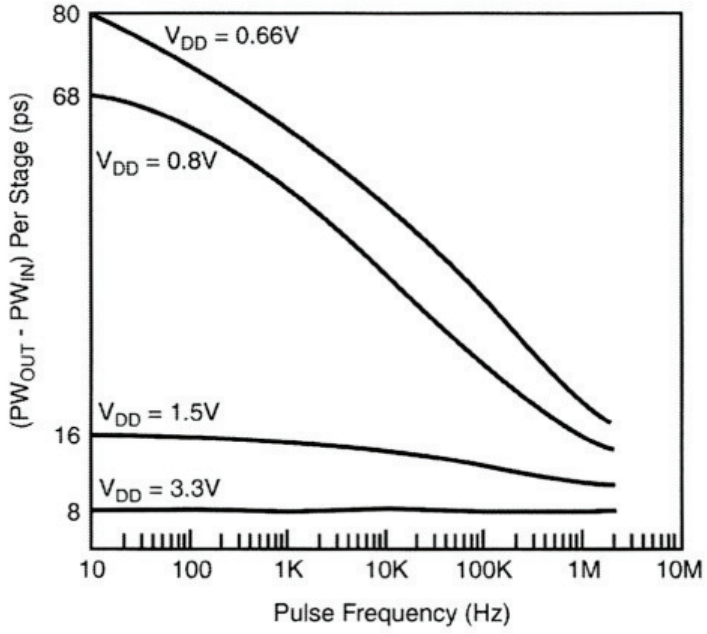


Figure 7.23: Measured pulse stretch per stage in a 480-stage PD-SOI CMOS inverter versus input pulse frequency and V_{DD}.

Figure 7.24 shows a self-resetting CMOS circuit with input and output pulses [7.14, 7.16]. The circuit uses delayed feedback loop from the output to reset the circuit in order to eliminate clock skew associated with the global clock.

Once the input signal arrives, node N1 is pulled low, and the output starts rising. Figure 7.24(b) shows the simulation waveforms when utilizing a nMOS pull- down transistor and an 11-stage inverter chain in the feedback loop.

As input IN goes high, node N1 falls and the output rises. This rising edge is fed back through a reset timing chain and then applied to precharge transistor MP0. Node N1 then falls, allowing the output to switch low. When node N1 is pre-charged HIGH, the output goes to LOW. The falling edge of the output triggers the turn 'ON' of MP0.

Pulse stretching broadens the pre-charge pulse V_{PCH}, since the rising edge of the output pulse propagates faster through the delay reset chain than the falling edge, thus restraining the evaluation cycle and degrading cycle time. The simulation waveforms shown here do not reflect much delay, but as the

Samsung Exhibit 1010, Page 110 of 204

number of inverter stages increases in the feedback loop, the feedback pMOS input pulse is widened.

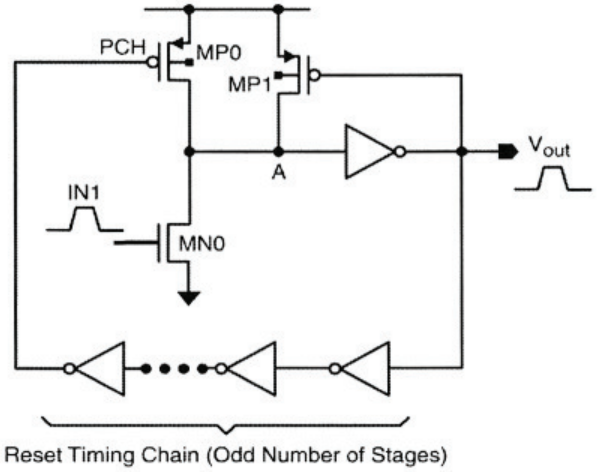


Figure 7.24(a): Schematics of a self-resetting CMOS circuit (SRCMOS) circuit. MPO is the precharge transistor, and MP1 is the feedback half latch to improve the noise margin of the dynamic node. 11-stage inverter chain in the feed back path and a single nMOS in the pulldown stack.

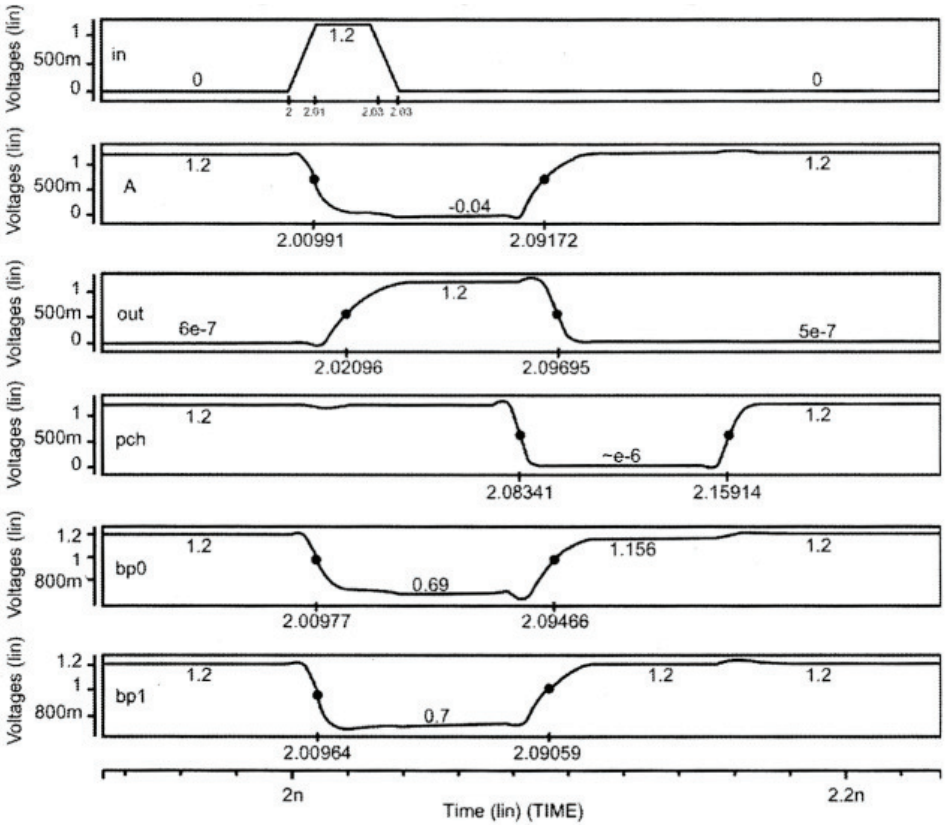


Figure 7.24(b): Simulated node and body voltages in SRCMOS circuit.

Samsung Exhibit 1010, Page 111 of 204

It is important that input pulses align properly to ensure sufficient overlap. Proper separations between pulses prevent them from overlapping. The pulse alignment becomes much more complicated in the presence of the pulse stretching effect [7.14].

7.14 Dynamic Wide-OR

Pass-gate leakage of a dynamic wide-OR (figure 7.25) is a function of the width of the OR devices. If the combined width of all the OR devices is large, then pass gate leakage can cause circuit failure at higher voltages. This is normally not a problem at nominal voltages or when the keeper is large, but at process and operating corners, problems may occur. Solutions to avoid this effect are to increase keeper device strength, eliminate MP3, or discharging node N2 periodically, e.g., during reset (figure 7.25(b)) [7.17].

Once the CLK is 'on', devices MN1 and MN3 are low, and the input to MN2 turns 'on' after a few nanoseconds, the body voltage of MN2 falls low, and the body voltage of MN_X reduces due to the presence of a discharge path to ground. The body voltage of MN2 rises (not shown) due to body to gate coupling and then settles low once the device MN2 is ON. It has been reported that [7.17], at Vdd=2.5V, parasitic leakages can cause failure if the combined widths of the OR gates are higher (>200μm). Our simulations do not show major failures until about Vcc=3.5V (and combined device widths of 500μm). The output node remains low with very small spikes caused due to parasitic leakages.

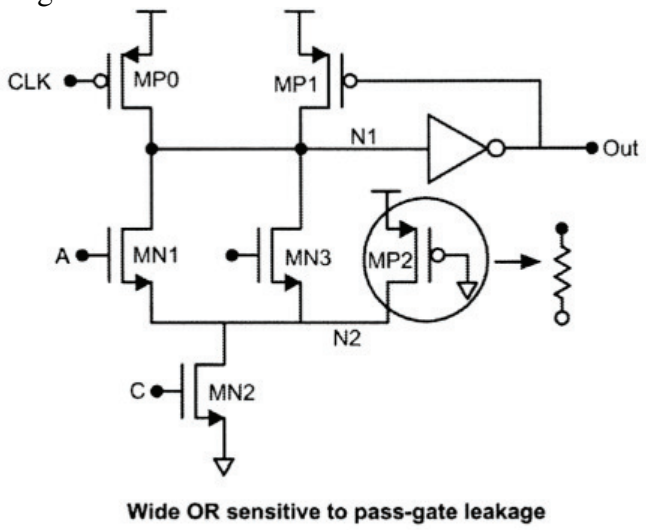


Figure 7.25(a): Wide-OR sensitive to pass-gate leakage [7.17]. nMOS MN2 has to be a big device in order to discharge to GND. MP2 has to be a weak device. Large combined width of OR nMOS gates can cause problem at very high supply voltages.

7.15 Non Overlapping Clocks

A string of pass transistors/inverters (figure 7.26) represents a dynamic shift register. When signal Φ1 goes HIGH, the first and third stages of the register are enabled. Data are passed from the input to point S0 and from point S1 to S2. If Φ2 is low while Φ1 is high, data cannot pass from S0 to S1 and from S2 to S3. If both Φ1 and Φ2 are high at the same time, the input of the shift register and the output are connected together, which is not acceptable in a shift register application.

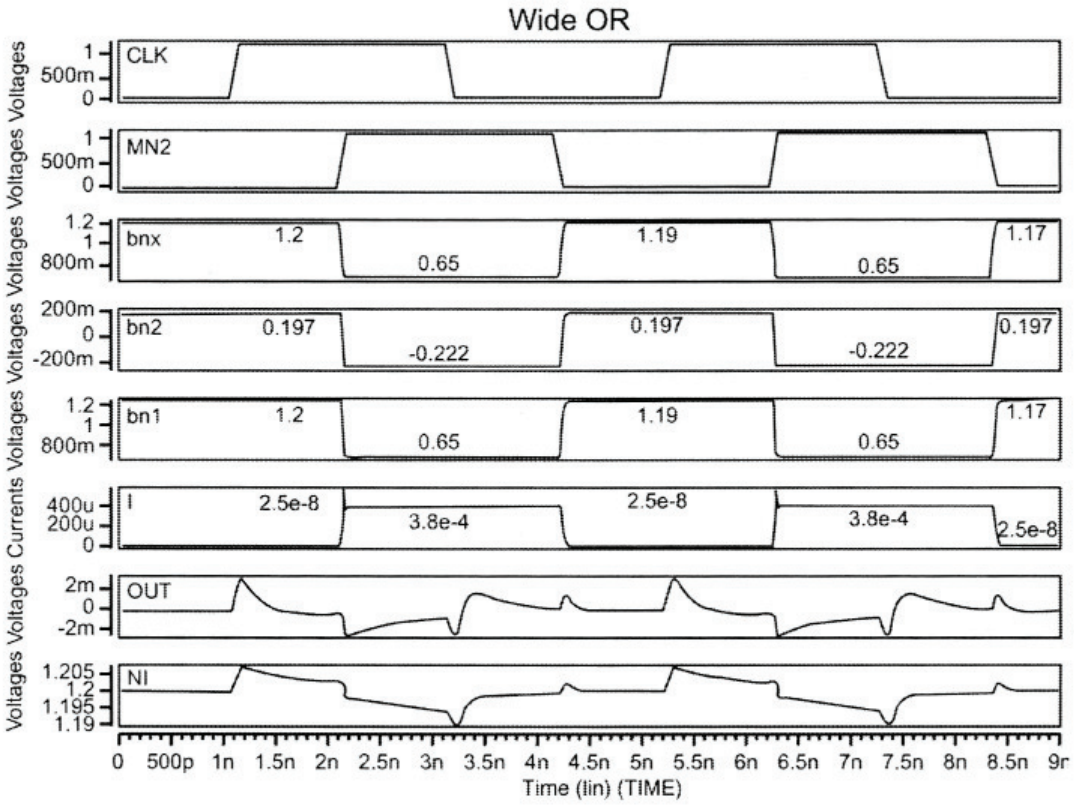


Figure 7.25(b): Simulation waveforms for dynamic Wide-OR gate.

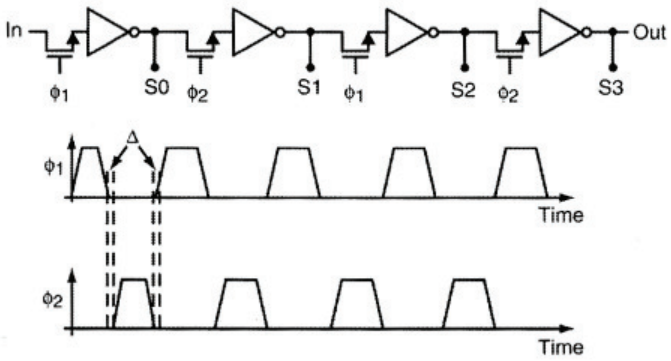


Figure 7.26: Dynamic Shift register with non-overlapping clocks.

The purpose of the inverter between pass transistors is to restore logic levels, since the nMOS pass transistor passes a high with a threshold voltage drop. A buffer instead of an inverter would eliminate logic inversion between stages. The clocks used in this dynamic circuit must be non-overlapping or logically $\Phi 1.\Phi 2 = 0$ [7.18].

A simple logic inversion will not generate non-overlapping clock signals. Figure 7.27 shows an example of non-overlapping clock generation. A clock signal is used to generate a two-phase non-overlapping clock. The gap between clocks is set by the delay through the NAND gate and the two inverters at the NAND gate output. If the input clock goes high, $\Phi 1$ is forced high and $\Phi 2$ low. After $\Phi 1$ goes low, $\Phi 2$ settles high.

When driving long transmission lines such as polysilicon interconnects, where the rise time of the signals can be significant, a large number of inverters may be required. Line drivers or a string of inverters can be used to drive large capacitances as part of the delay in the non-overlapping clock generation circuit.

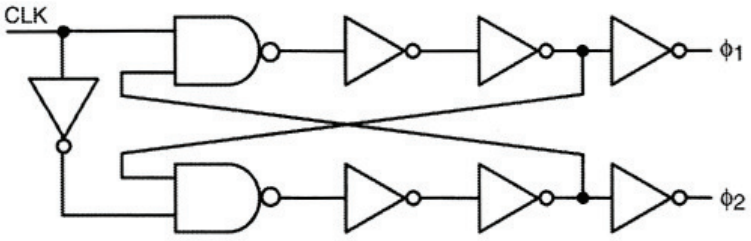


Figure 7.27: Non Overlapping Clock Generation Circuit

7.16 Pass transistor based non-overlapping clocks

A common and important application of pass gates is the lock/timing control in various latch designs [7.19]. Figure 7.28(a) depicts a two-level latch with two non-overlapping clocks, $\Phi 1$ and $\Phi 2$. After passing a high state, assume $\Phi 1$ switches low and input signal 'IN' switches low. When $\Phi 1$ is low, the pass-gate at the input to the second stage latch is supposed to be 'off', while the pass gate in the feedback loop of the first stage latch is 'on' to hold the state of the latch.

Significant parasitic bipolar current flows through the 'off' nMOS of the input pass gate to pull down node N1. Since the pass gate in the feedback loop is 'on', the pMOS in the feedback inverter fights the parasitic bipolar current to restore node N1. The result is a transient voltage dip of 'A' (figure 7.28(b)) [7.20]. The complementary situation is of lower concern as impact

Samsung Exhibit 1010, Page 114 of 204

ionization of the pMOS is reduced and current gain of the parasitic PNP transistor is lower [7.6]. The voltage dip on node N1 is lower at supply voltages of 1.5V. Figure 7.28(b) shows the node voltages when Φ1 and Φ2 switch.

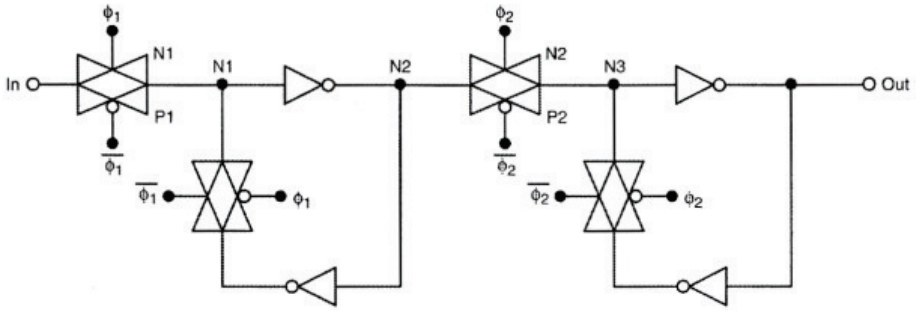


Figure 7.28(a): Pass transistor based 2-Φ Non Overlapping Clocks

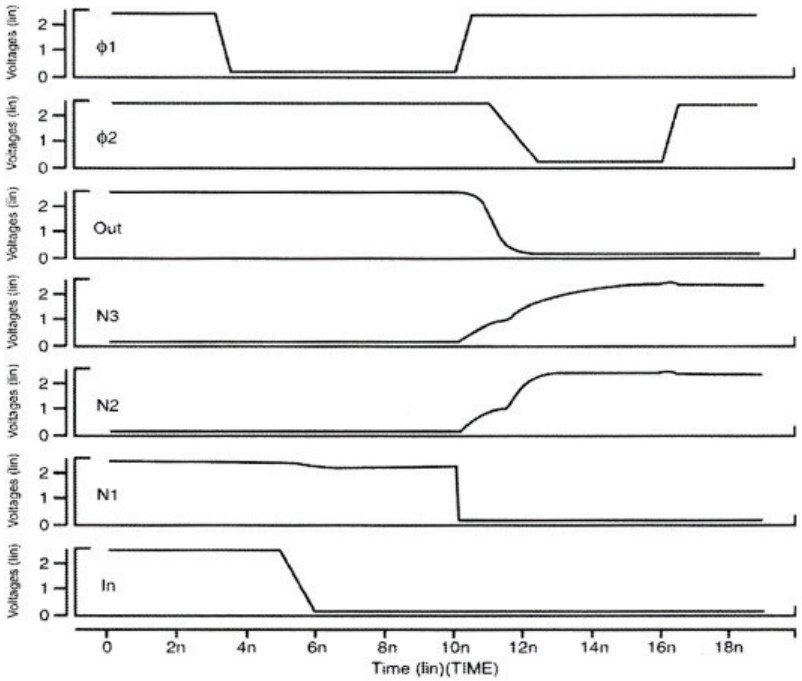


Figure 7.28(b): Waveforms of 2-phase Non Overlapping Clocks. The node voltage N1 dips slightly below Vdd once the input "IN' falls.

In some high-density designs, the feedback loop pass-gate is removed, and is replaced with a trickle inverter constructed of low gain devices. It is important to make sure that the trickle inverter has enough strength to overcome the parasitic bipolar current and restore node L1, to prevent the latch from settling in the wrong state.

The parasitic bipolar can cause errors in pseudo-two-phase dynamic logic (figure 7.29) [7.19, 7.20]. During the condition when C2 is LOW, the pass

Samsung Exhibit 1010, Page 115 of 204

gate to the second stage is 'off', and the second stage is evaluating. If data stored in the gate capacitance is HIGH and the first stage is evaluated LOW, then following the falling edge of C1, parasitic bipolar current flows through the nMOS in the OFF pass gate, discharging node N3.

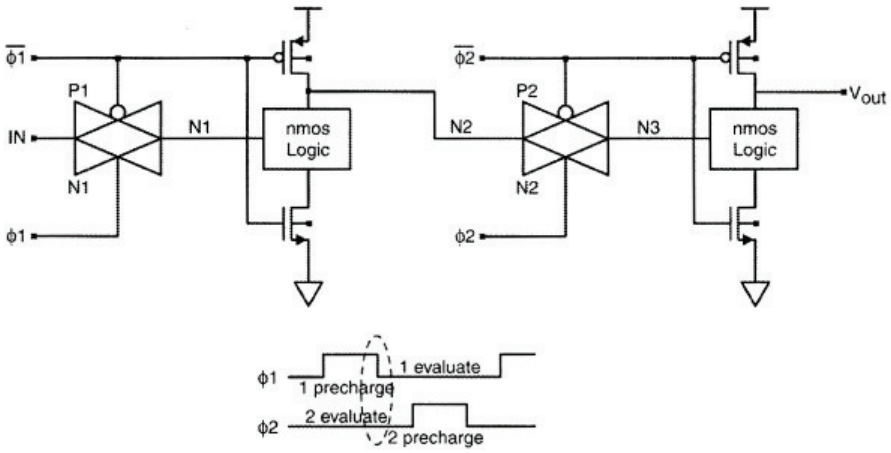


Figure 7.29: Schematic of a pseudo two-phase dynamic logic circuit.

7.17 Low Power SOI Techniques

We here consider dynamic logic specific low power SOI structures. More general low power techniques are discussed in chapter 12. Isolated bodies in SOI offer a degree of freedom for the designers to enhance the power and delay performance. The body contact can be used to achieve high speed, low voltage operation in active mode and low leakage, low power operation in standby mode. Circuits with body tied to gate reduce threshold voltages and increase drive currents. Body tied to gate circuits are often the dynamic threshold voltage MOSFETs (DTMOS). Body potential is low and threshold voltages are high in standby mode to reduce leakage. DTMOS circuits are suitable for low voltage applications. The power supply voltage is limited to less than one diode drop to avoid turning 'on' of the parasitic bipolar transistor. A circuit limiter to limit the body to source junction voltage to less than a diode threshold is necessary at higher supply voltages.

7.17.1 Dynamic Threshold SOI CMOS

A dynamic threshold voltage MOSFET inverter (DTMOS) includes static, switching and short circuit power dissipation. For the switching power dissipation, both load and device parasitic capacitances are considered.

Body tied to gate SOI dynamic threshold voltage MOSFET do not exhibit floating body effect and have better sub-threshold characteristic than conventional SOI MOSFETs. As gate voltage is increased, the gate couples onto body and forms body-source forward biased diode, reducing its

threshold voltage as a result of body effect. Hence, threshold voltage can be changed dynamically without the application of additional control circuitry. DTMOS can be operated at low power supply while still maintaining a large drain current for high-speed application, without introducing any extra standby current. Further operational restrictions are discussed in chapter 3. The advantages of dynamic threshold MOS are partially offset with a number of drawbacks. DTMOS devices connected in the pull up/pull down configuration such as inverters have increased power dissipation (compared to a conventional SOI inverter). Static power dissipation increases due to leakage of the forward biased body-drain/source P-N junctions and capacitances associated with the parasitic P-N junction diodes. These add to power dissipation during switching, increasing short circuit power dissipation [7.14].

7.17.2 Dynamic Threshold Multithreshold CMOS Logic

Dynamic threshold voltage control may be used in multi-threshold CMOS (MTCMOS) circuit [7.21] combining low V_T-CMOS logic gates with variable V_T sleep mode. This type of threshold voltage control is suitable for sub 1V applications where low standby power is very important. Figure 7.30 shows circuit delays of bulk MTCMOS and PD-SOI MTCMOS as functions of the supply voltage. The SOI-MTCMOS offers greater than 2X delay improvement and can also operate down to 0.4V, while bulk MTCMOS loses functionality around 0.5V [7.6, 7.22].

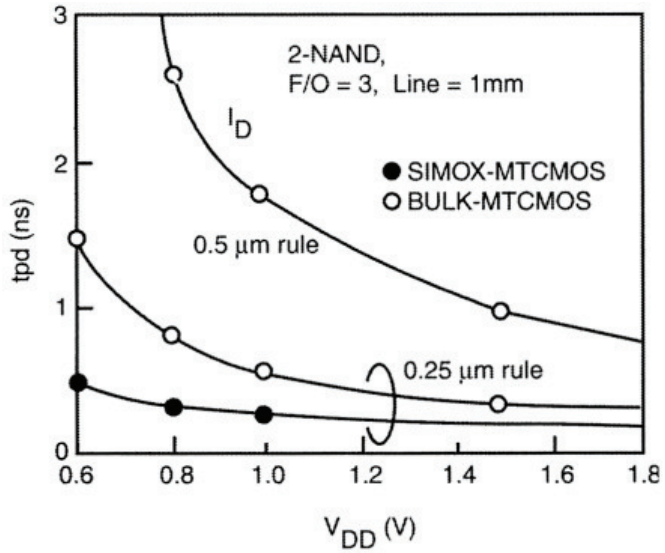


Figure 7.30: Comparison of basic logic gate delays of bulk MTCMOS and SIMOX-MTCMOS.

Figure 7.31 shows a multi-threshold CMOS logic operation at low voltages. Using a combination of fully depleted and partially depleted SOI transistors,

performance is achieved in active cycle and low power in standby mode. The fully depleted pMOS device is used to lower the body voltage of the partially depleted pMOS, resulting in decreased threshold voltage and lower operational supply voltage. The pMOS body voltage is raised during standby, increasing its threshold voltage and reducing standby current.

During the active cycle, when SL is low, if the pMOS body is tied to gate and the supply voltage is larger than one diode threshold, significant current flows from to the drain-body p-n junction to the gate. This can be suppressed by tying the pMOS body to its gate through a low V_T pMOS reverse biased diode (figure 7.31(b)). When SL is "high" (sleep mode), the body of the sleep mode control pMOS will sit at one (low) diode drop below SL.

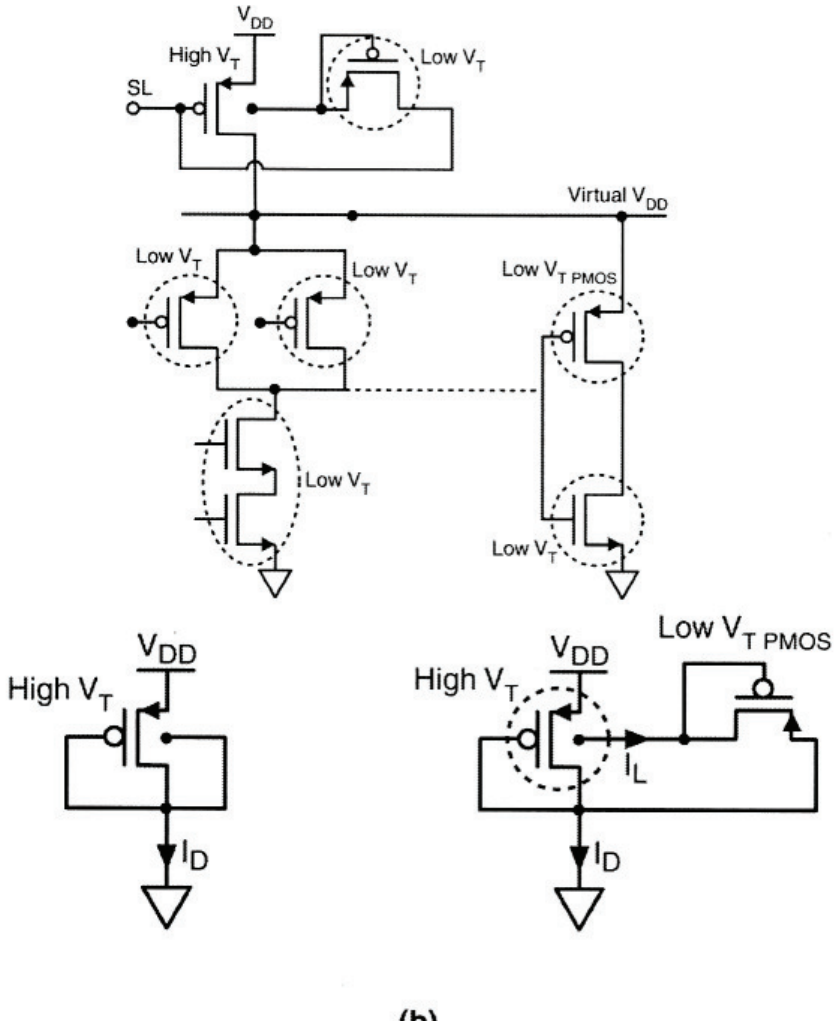


Figure 7.31: (a) SIMOX MTCMOS circuit, and (b) Current characteristics of DTCMOS and variable high V_T MOSFET with reverse biased MOS diode [7.6, 7.22].

Samsung Exhibit 1010, Page 118 of 204

7.17.3 Dynamic Threshold Pass Transistor Logic

Dynamic threshold techniques may also be applied to pass transistor logic [7.23]. Figure 7.32(a) shows a complementary pass transistor logic (CPL) network. Degradation in drive capability and threshold voltage loss in transmitting a "high" signal restrict the low voltage applications of this circuit. Figure 7.32(b) shows the pass gate bodies and the gate tied together. Body bias control can also be applied to the buffer (figure 7.32(b)).

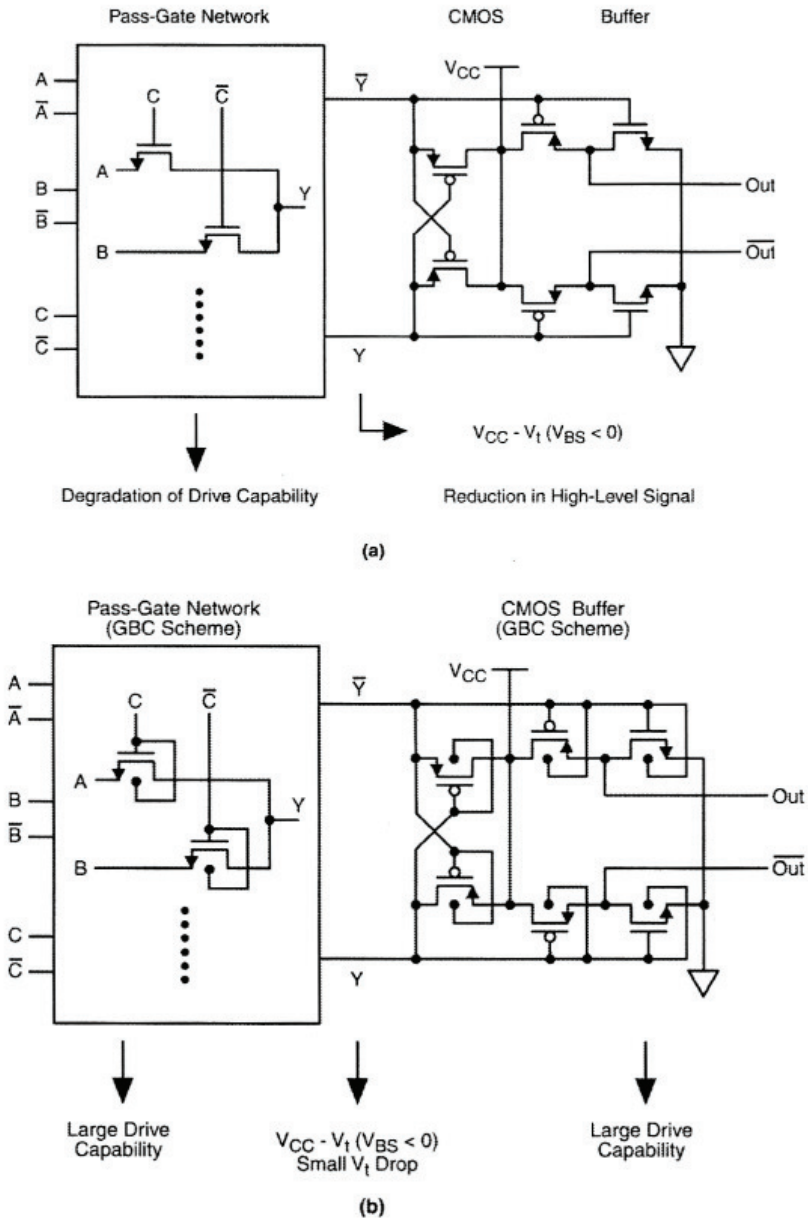


Figure 7.32: (a) Conventional complementary pass gate logic (b) Gate body connected SOI pass gate logic.

Samsung Exhibit 1010, Page 119 of 204

7.17.4 Dynamic threshold voltage Full Adder

Because of the low threshold voltage of the "ON" MOSFETs, the dynamic threshold voltage scheme reduces the delay of a full adder to approximately a third of the conventional SOI complementary pass gate logic at a supply voltage of 0.5V (figure 7.33) [7.6]. At a fixed delay of 2.5nS, the lowest operation voltage improved by 0.18V. The buffer section can be further enhanced by crosscoupling pull-ups (Figure 7.33). The bodies of the pull up pMOS can be connected to their respective gates or to the inputs (figure 7.34). With the bodies tied to gates and gates cross-coupled to the output nodes of the opposite phases, the threshold voltages of the "ON" pull up pMOS remains high until the output nodes change. It is therefore advantageous to connect the body to the input so the pMOS threshold voltage decreases as soon as the input changes, improving circuit speed and reducing short circuit current [7.23].

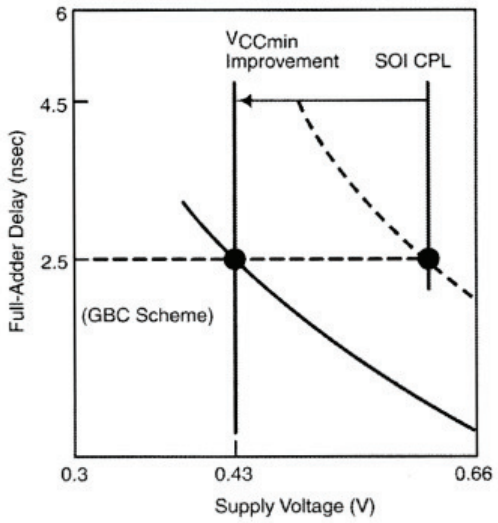


Figure 7.33: Simulated full adder delay of conventional complementary pass gate logic and gate body connected pass gate logic.

To extend the operating voltage of the body bias controlled SOI pass gate circuits to greater than one diode voltage, the boosted ground scheme as shown in figure 7.35(a) is a preferred method [7.24]. Here, a reference voltage generator, composed of drain body connected nMOS SOI transistor and a series resistor, generates reference voltage, V_{REF}. The bias applied to the maincircuitry, V_{DD}-V_{REF}, is lower than the soft breakdown voltage of the body bias controlled SOI devices, thus reducing leakage. The boosted ground scheme is driven by a body source tied SOI nMOS transistor to avoid the floating body effect and to ensure high threshold voltages to suppress the standby leakage current of the main circuitry. A charge pump boosts the supply voltage for stable operation of the analog portion of the circuits.

Samsung Exhibit 1010, Page 120 of 204

Figure 7.35(b) shows the maximum frequency and active power as functions of the supply voltage for a one stage, 32-bit ALU using the boosted ground scheme. The operating voltage range increases while restricting IDDQ. The maximum frequency remains relatively constant as supply voltage increases over 0.5V since the highest voltage applied across the main circuitry is limited to 0.5V.

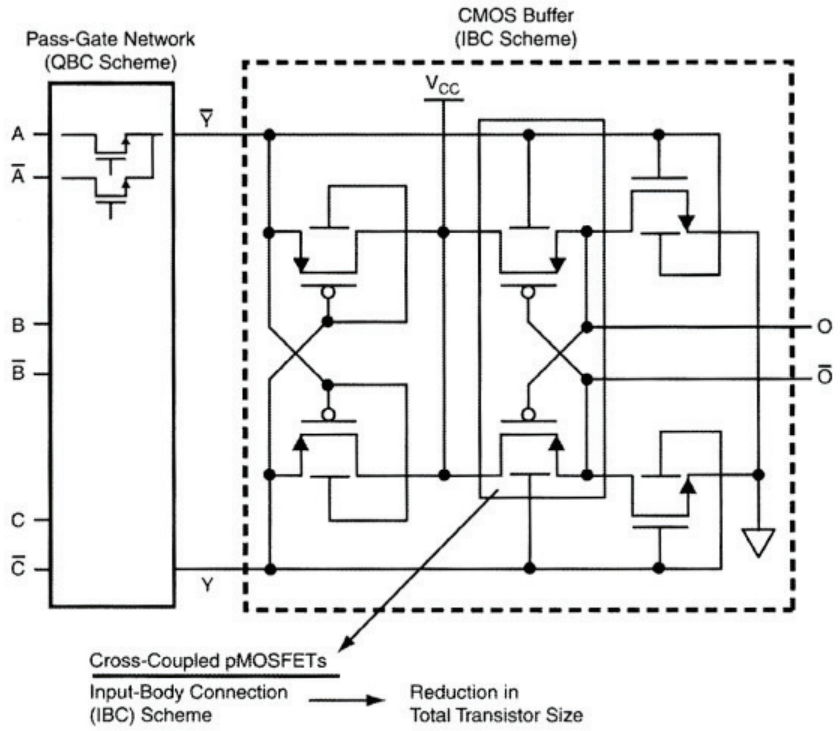


Figure 7.34: SOI CMOS buffer with cross coupled pMOS and body input connection.

Capacitive coupling can be used to maintain body bias control and extend operating voltage range. Figure 7.36(a) shows the schematic of a double gate driven CMOS (DGCMOS) circuit where the body of the switching device is dynamically connected to the gate through a capacitor [7.25]. Coupling capacitor C_B is added between the body of the pMOS and the input of the inverter and a p-n junction diode D1 is added between the pMOS and supply.

When the input switches from V_{DD} to ground, the pMOS is turned 'on' and the body voltage couples down (V_{BP}=~0.5V). This reduces its threshold voltage and increases drain current. When the pMOS body voltage falls below a diode drop from supply, the pMOS body to source junction is

charged. V_{BP}, settles at V_{DD}-V_{SBD} (~0.52V), where V_{SBD}, is the threshold voltage of the source body diode (figure 7.36(b)).

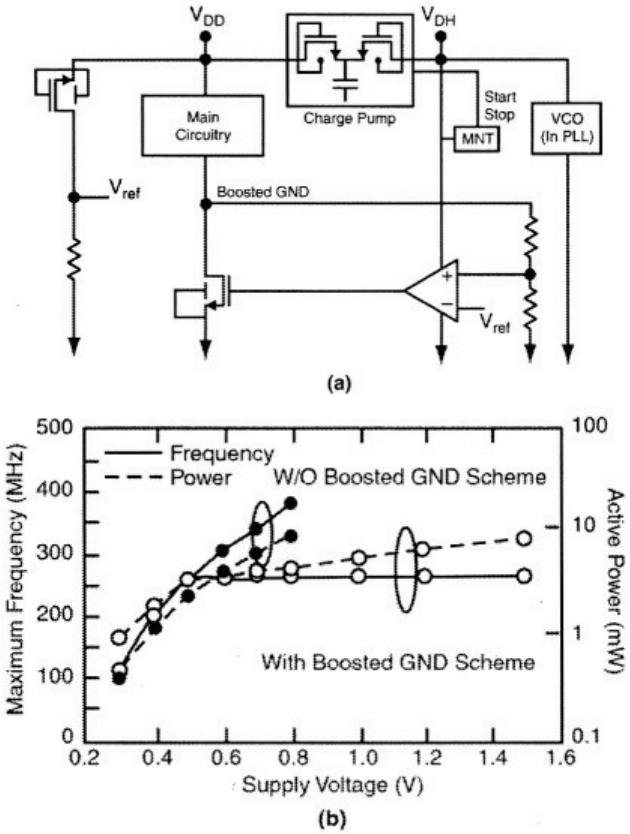


Figure 7.35: (a) Body Bias controlled SOI pas gate logic with boosted ground scheme (b) maximum operating frequency & active power versus supply voltage [7.6, 7.24].

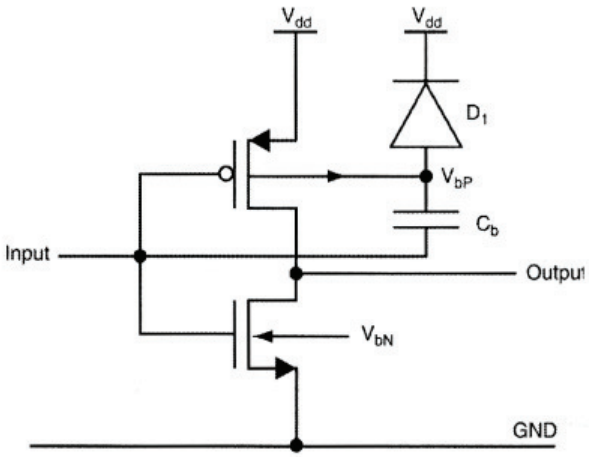


Figure 7.36:Double gate driven pMOS for an inverter [7.25].

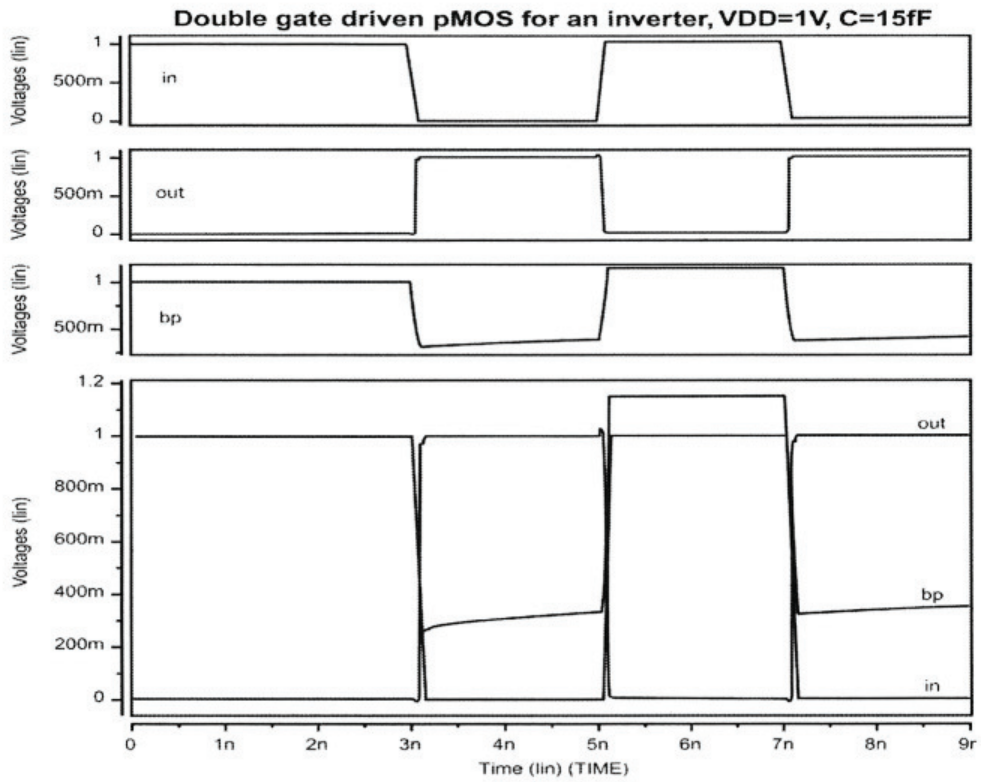


Figure 7.36(b): Inverter input, output and node waveforms. The pMOS body voltage rises from 0.15V to 1.4V during input switching low to high.

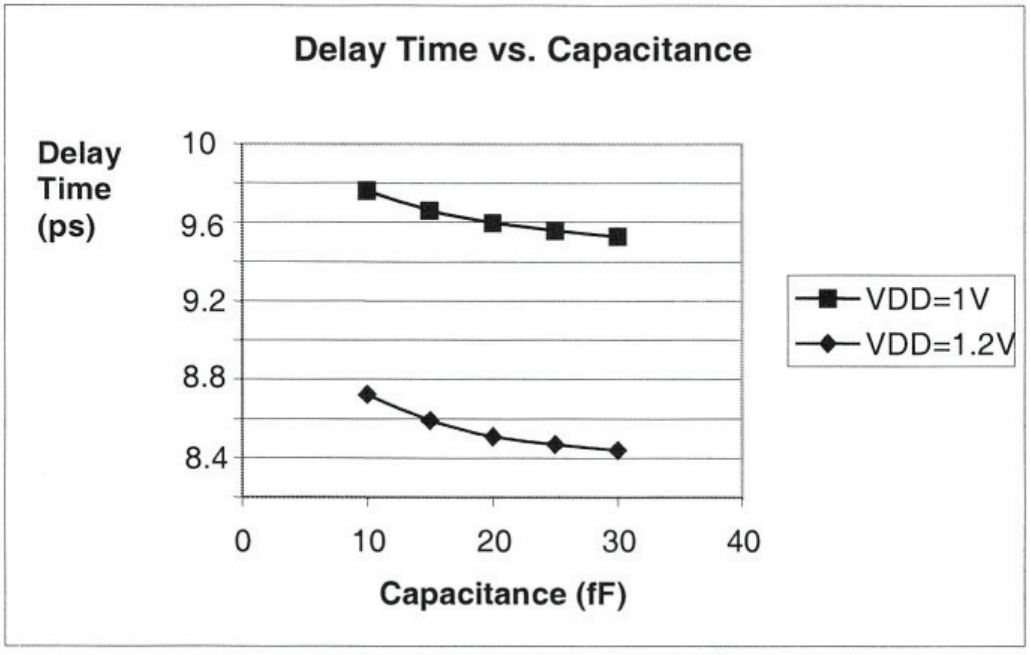


Figure 7.36(c): Delay versus capacitance for V_{DD}=1V and V_{DD}=1.2V. Delay time reduces with increased capacitance.

Samsung Exhibit 1010, Page 123 of 204

When the input switches from GND to V_{DD}, the pMOS is turned off. The pMOS body voltage V_{BP} rises from V_{DD}-V_{SBD} (~0.15V) to V_{DD}-V_{SBD}+V_{DD} (~1.4V) and eventually drops to V_{DD}+V_{DIODE} (where V_{DIODE} is the threshold voltage of the diode D1 and V_{SBD} is the threshold voltage of source-body diode) through the discharge diode D1.

This circuit can operate at any supply voltage compatible with the device design without the leakage of some other body bias controlled schemes. Larger C_B increases V_{BP} modulation and reduces leakage significantly. The drawback of this technique is the increased input capacitance, resulting in a larger load on the previous stage. C_B therefore requires a design tradeoff between the circuit speed and leakage. The delay time reduces with increased capacitance in SOI (figure 7.36c).

Device operation may become unreliable at high frequencies because of the feedback through C_B. Another alternative technique that may overcome this frequency limitation is the active body bias scheme [7.26]. Figure 7.37(a) shows two active body biased driver circuits.

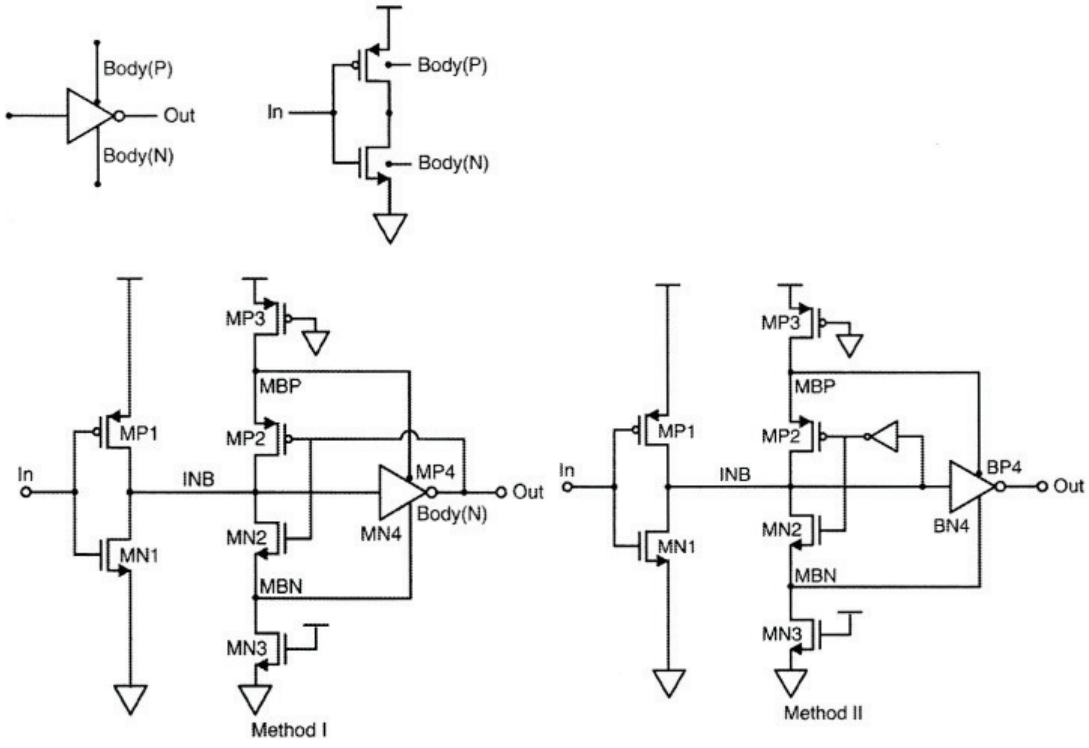


Figure 7.37(a): Active body bias SOI CMOS drivers.

The pMOS and nMOS transistors in the stack MP3/MP2/MN2/MN3 dynamically control the body voltage of the switching transistors MP4/MN4

Samsung Exhibit 1010, Page 124 of 204

in method I. If the input is "low", INT is high and the output is low (figure 7.37(b)). Then the PMOS MP4 drain is low and the gate of MP2 is low (MP2 ON and MN2 OFF). The body voltage of MP4 falls slightly after the input switches. MP2 functions like the feedback half latch in a dynamic circuit [7.19]. If the input then switches low to high, MP2 turns off and MN1 turns 'on'.

During initial switching, transistor MP2 is ON and the transistor MN1 is 'on', providing a current path from MP3 through MP2 and MN1 to ground. Transistor MP3 is sized such that its current is substantially smaller than that through MN1/MP2. Leakage current through MP3 pulls down the voltage at the intermediate node between MP3 and MP2 (body voltage of the MP4), reducing the threshold voltage of MP4, and speeding up the MP4 pull up. In standby, the output is 'high' turning OFF transistor MP2 and disconnecting the leakage path.

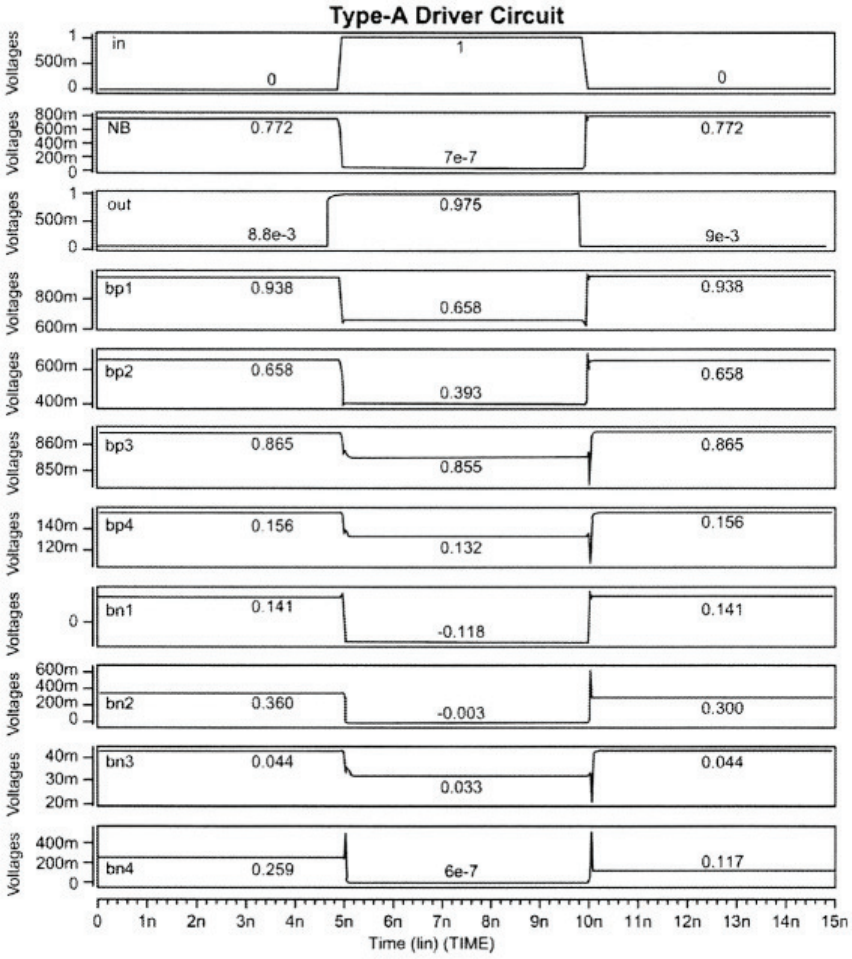


Figure 7.37(b): Active body bias SOI CMOS driver output voltages for the circuit shown as method I (figure 7.37(a)).

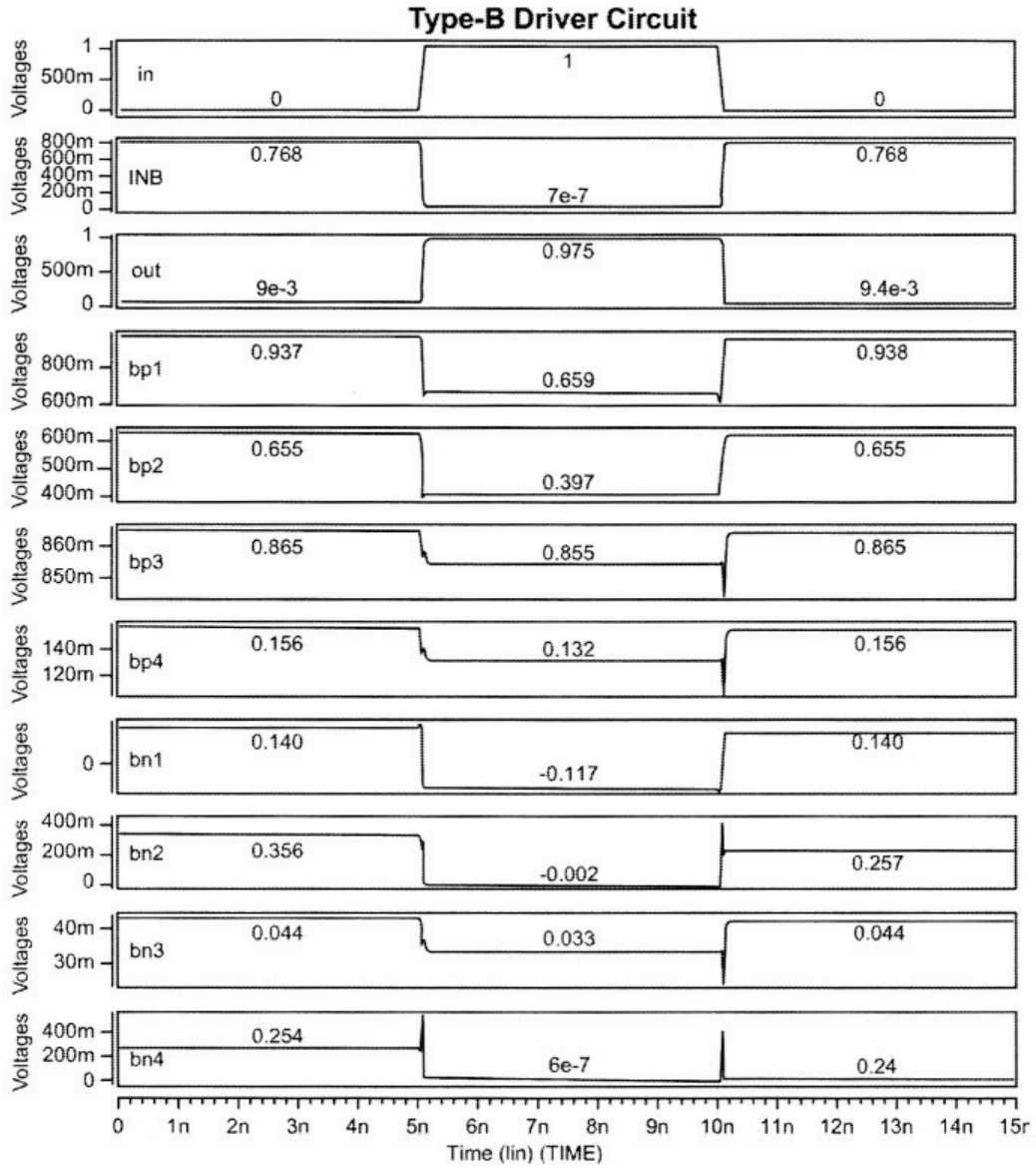


Figure 7.37(c): Active body bias SOI CMOS driver output voltages for the method II circuit of figure 7.37(a)

In the method II circuit, (figure 7.37(a)), feedback is through a small inverter. This provides long low threshold voltage periods for MP4 or MN4. Figure 7.37(b & c) shows the output voltages for the method I & II circuits.

Figure 7.37(d) shows the drain current through MN1 for method I and II circuits for input rising and falling pulses in bulk. High to low transition dissipates less power compared to low to high transitions for both the methods. Figure 7.37(e) compares the rising and fall times for the two methods in SOI as well as their standby currents and Figure 7.37(f) shows the same data in bulk designs [7.6].

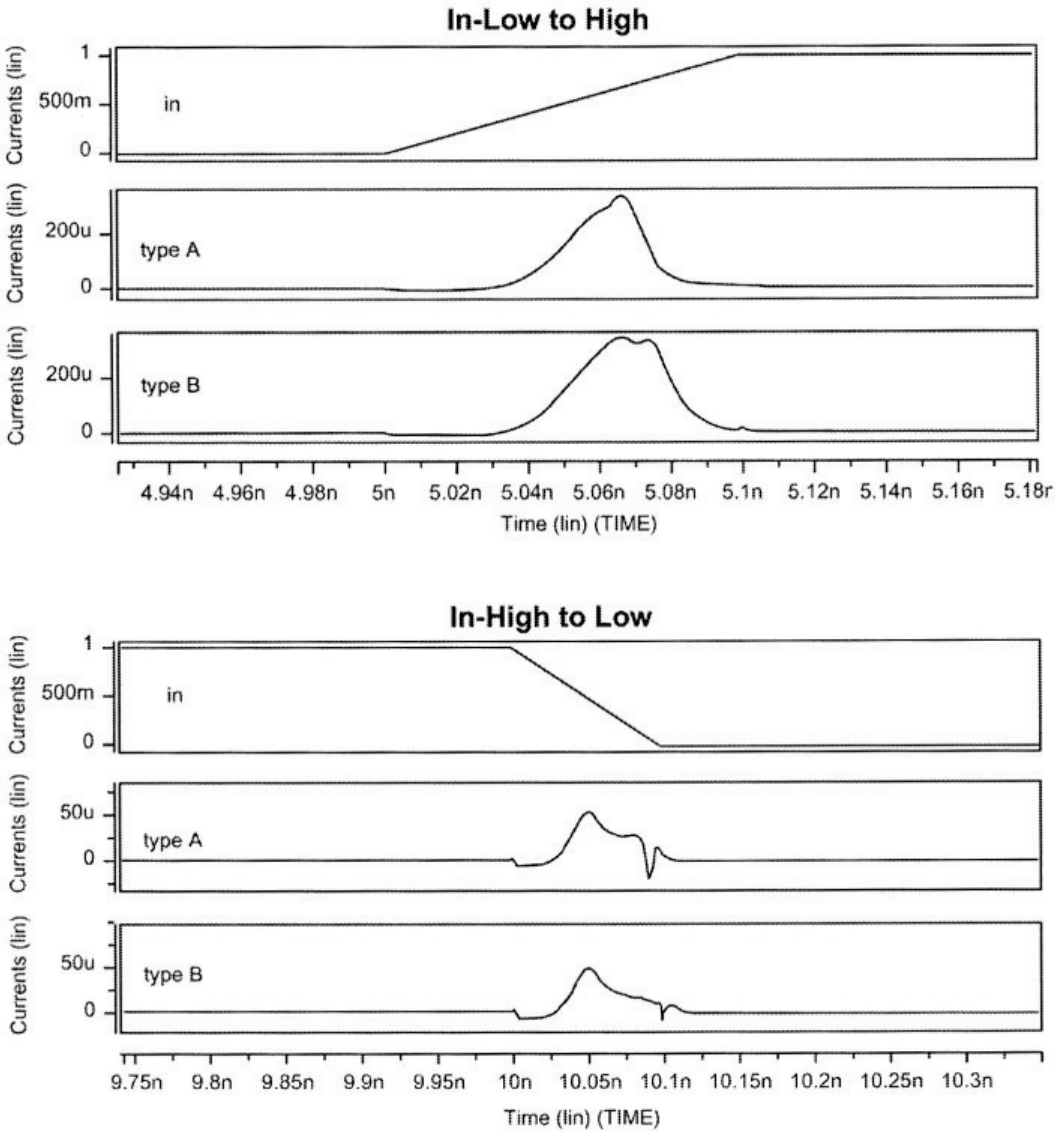


Figure 7.37(d): The drain current through MN1 for method I and II circuits for input rising and falling pulses in bulk.

The method II SOI is faster than method I in SOI and both the SOI methods are faster than bulk during rising outputs, and have faster pull downs during falling edges compared to bulk. Both the methods are also simulated in bulk (noted by bulk A and bulk B in the waveforms).

The delay for the method II circuit in SOI can be reduced by re-sizing transistors MP4 and MN4. Method II is faster than method I for rising outputs and vice versa for falling outputs. Figure 7.38 shows the comparison of various methods at different supply voltages.

Samsung Exhibit 1010, Page 127 of 204

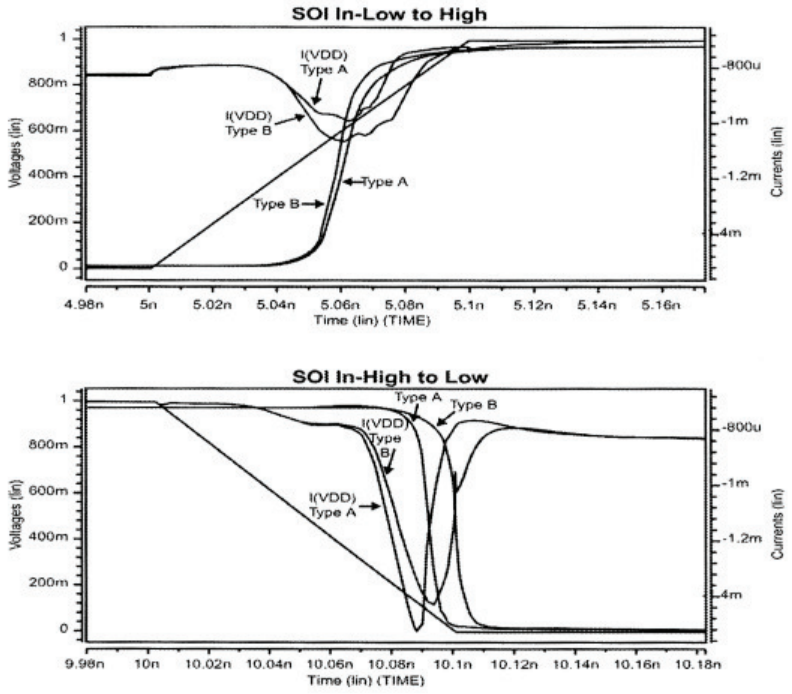


Figure 7.37(e): High to low and low to high transitionsand currents in SOI for methods I and II.

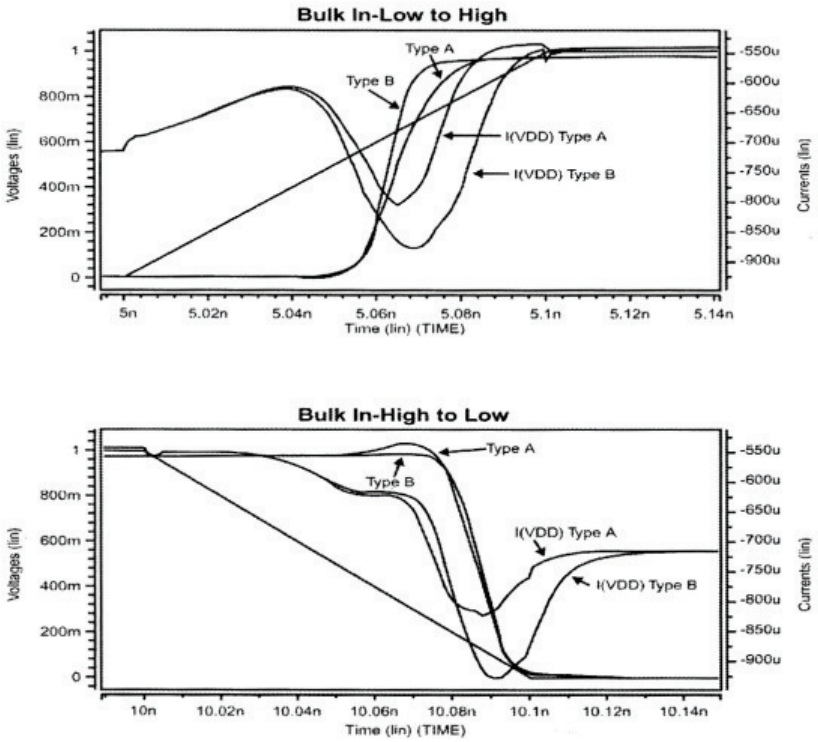


Figure 7.37(f): High to low and low to high transitions in bulk for methods I and II.

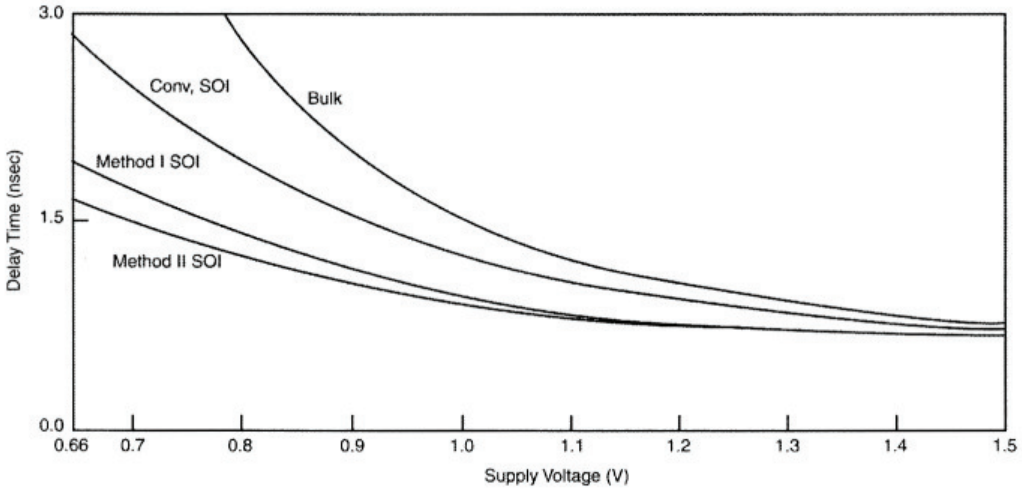


Figure 7.38: Delay time vs. supply voltage for various methods in bulk and SOI [7.26].

7.17.5 Dynamically Body Bias SOI CMOS Inverter

Figure 7.39(a) shows a dynamic body biased controlled inverter [7.27 - 7.29]. The bodies of the primary inverter transistors are controlled through another pair of alternate pMOS and nMOS transistors. The alternate transistor gates are driven from the primary gate inputs. The drains are connected to the output and the sources are connected to the bodies of the primary transistors.

As the input switches from low to high (Figure 7.39(b)) during the initial phase, the body voltage of the primary nMOS transistor increases through the alternate nMOS transistor in a source follower configuration. This reduces the threshold voltage of the primary nMOS transistor and improves pull down speed. Once the output switches low, the body of the primary transistor is reduced to zero. During the initial pull-down state, current through the alternate transistors M_{NA} charges the body of MN0 and helps pull down the output node directly. Conversely, once the output falls, capacitance of the primary transistor M_{ND} slows down the final part of the switching curve.

The threshold voltage of the subsidiary transistors can be designed to be substantially lower than the primary driving transistor since they do not provide a direct leakage current path during standby. This scheme works for any supply voltage. When the load capacitance is small, the delay improvement of the present scheme is not significant due to the increased capacitance caused by the alternate devices. As load capacitance increases, the improvement becomes significant in the dynamically body controlled inverter [7.6].

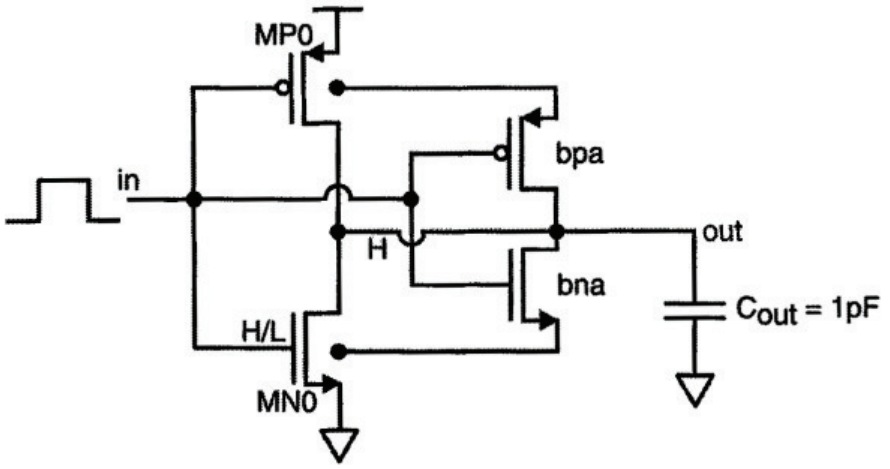


Figure 7.39(a): Schematic of a SOI CMOS dynamically body controlled inverter [7.27]

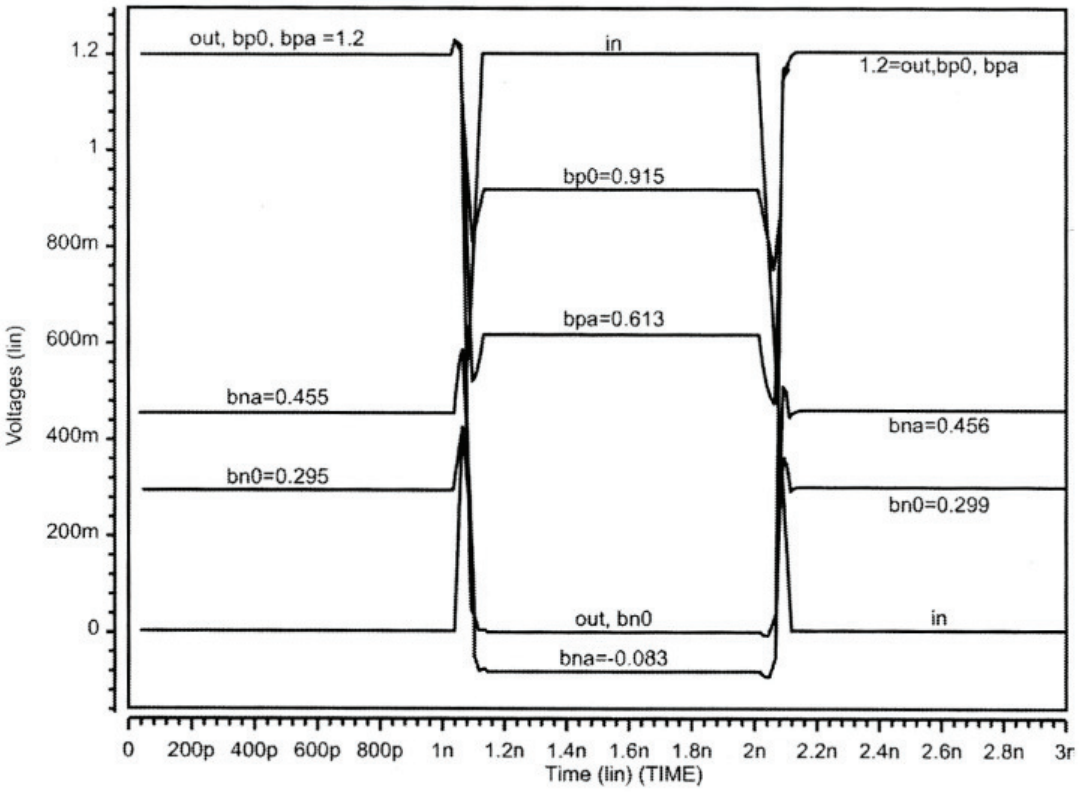


Figure 7.39(b): Waveforms for input switching low to high displaying the body voltages of the primary and alternate transistors.

Design strategy can also affect the leverage of SOI. In a dual design approach, requiring designs to work on both bulk and SOI technologies with only minor mask level adjustments, the performance in both the bulk and SOI versions is likely to be sacrificed.

The necessity to reserve area in the bulk version to accommodate body contacts in the SOI version increases the area in the bulk design. On the other hand, circuits in SOI may suffer from more severe supply and ground bounce, and degrade performance due to inadequate amount of decoupling capacitance. The long paths in the SOI may differ significantly from the bulk due to all the affects discussed above. Thus, timing optimization for the bulk version may not improve. The wire delay also degrades the advantage of the SOI version substantially.

In a silicon on insulator-only design, a global trade-off can be pursued to enhance the overall performance. For on-chip cache memory, decoupling capacitance can be used. Smart body contacts and driver configurations can be used to reduce the wire delay significantly, which tends to improves performance.

Circuit simulations and floating bodies require substantially more memory and simulation time. Simulation convergence for the initial DC solutions tends to be a problem since the initial DC potential of floating nodes in the circuits is set by small leakage currents with long time constants. The floating body related effects further complicate the identification and definition of various timing modes.

For memory applications, the circuits is more confined. The circuit design, timing, optimization and use of selective and/or smart body contacts to improve the performance appear more straightforward than for mainstream logic applications. Timing large scale logic circuits with all the floating body related effects represents the single most challenging task in bringing SOI into mainstream microprocessor application.

The device lifetime does not appear to be a problem for SOI. Adequate hot carrier lifetimes have been demonstrated for 0.35μm partially depleted SOI devices with both body floating and body grounded schemes [7.30]. Device lifetime (to 10% reduction in saturation current) similar to bulk technology has also been demonstrated in 0.25μm SOI-CMOS technology, and 10-year operation at 1.8V with effective channel length down to 0.1μm appears feasible [7.31].

References

[7.1] K. Bernstein & N. J. Rohrer, "SOI Circuit Design Concepts", Kluwer Academic Publishers, January 2000, ISBN 0-7923-7762-1

[7.2] D. H. Allen, et. al., "A 0.2um 1.8V SOI 550MHZ 64b PowerPC microprocessor with copper interconnects", Proceedings of 1999 IEEE ISSCC, 1999, pp. 438 – 439.

[7.3] A. Wei, et. al., "Minimizing floating body induced threshold voltage variation in partially depleted SOI CMOS" IEEE Electron Device Letters, Vol 17, Aug 1996, pp. 391-394.

[7.4] J. Uyemura, "CMOS Logic design style", Kluwer Academic Publishers.

[7.5] C. Kim at el., "Parallel Dynamic Logic with speed enhance skewed static logic", ISCAS 2000.

[7.6] C. T. Chuang, et. al., "SOI for Digital CMOS VLSI: Design considerations and Advances", IEEE Proceedings, Vol 86, No. 4, April 1988, pp. 689 – 720.

[7.7] K. Yano, et. al., "A 3.8nS CMOS 16x16 bit multiplier using complementary pass transistor logic", IEEE JSSC, Vol 25, Mar 1990, pp. 388 - 395.

[7.8] M. Suzuki, et. al., "A 1.5nS 32b CMOS ALUin double pass transistor logic", ISSCC Dig. Tech. Papers, 1993, pp. 90 – 91.

[7.9] Y. Sasaki, et. al., "Multilevel pass transistor logic for low power ULSI", Dig. Tech. Papers, Symp. Low power Electronics, 1995, pp. 14 - 17.

[7.10] C. T. Chuang, et. al., "Dual mode parasitic bipolar effect in dynamic CVSL XOR circuit with floating body PDSOI devices", VLSI Technology, Taipei, 1997, pp. 288 – 292.

[7.11] M. M. Pellela, et. al., "Low voltage transient bipolar effect induced by dynamic floating body charging in scaled PD-SOI MOSFET's" IEEE Electron Device Letters, May 1996, pp. 196 - 198.

[7.12] P. F. Lu, et. al., “Floating body effects in PD-SOI CMOS circuits”, Proc. 1996 Int. Symp. Low power Electronics and design, Monterey, CA, Aug 12-14, 1996, pp. 139 - 144.

[7.13] J. B. Kuo, et. al., "Compact MOS/Bipolar Charge-Control Models of Partially-Depleted SOI CMOS Devices for VLSI Circuit Simulation -- SOI - Technology (ST)-SPICE", ESSDERC, 1999.

[7.14] J. B. Kuo, “Modeling of Low-Voltage SOI CMOS VLSI Circuits”, IEEE SCV Solid State Circuits, April 2001 Meeting, (Univ. of Waterloo).

[7.15] A. Pellela, et. al., “A 2nS access, 500Mhz 288Kb SRAM Macro”, Symp. VLSI Circuits, 1996, pp. 128 – 129.

[7.16] T. I. Chappell, et. al., “A 2nS cycle, 4nS access 512Kb CMOS ECL SRAM”, ISSCC Dig. Technical papers, 1991, pp. 50 - 51.

[7.17] G. Shahidi, et. al., “Partially Depleted SOI Technology for digital logic” ISSCC 1999, pp. 426 –427.

[7.18] R. Jacob Baker, et. al., “CMOS Design, Layout and simulation”, IEEE Press, ISBN : 0-7803-3416-7

[7.19] N. Weste & K. Eshragian, “Principles of CMOS VLSI Design – A system perspective”, Reading, MA: Addison-Wesley, 1988.

[7.20] P. F. Lu, et. al., “Floating body effects in PD-SOI CMOS circuits”, IEEE JSSC, Vol 32., Aug 1997, pp. 1241 – 1253.

[7.21] S. Nutoh, et. al., “A 1V high speed digital circuit technology with 0.5um multithreshold CMOS”, Proc. IEEE Int. ASIC Conf., 1993, pp. 186 – 189.

[7.22] T. Douseki, et. al., “A 0.5V SIMOX-MTCMOS circuit with 200pS logic gate”, ISSCC Digest technical papers, 1996, pp. 84 - 85.

[7.23] T. Fuse, et. al., “0.5V SOI CMOS pass gate logic”, ISSCC Digest technical papers, 1996, pp. 88 - 89.

[7.24] T. Fuse, et. al., “A 0.5V 200Mhz, 1-stage 32b ALU using a body bias controlled SOI pass gate logic”, ISSCC Digest Technical papers, 1997, pp. 286 - 287.

[7.25] L. S. Y. Wong & G. A. Rigby, "A 1V CMOS digital circuit with double gate driven MOSFET", ISSCC Digest technical papers, 1997, pp. 292 - 293.

[7.26] Y. Wada, et. al., "Active body bias SOI-CMOS driver circuits", Symp. VLSI circuits, 1997, pp. 29 – 30.

[7.27] I. Y. Chung, et. al., "A new SOI inverter for low power applications", IEEE International SOI Conference, 1996, pp. 20 - 21.

[7.28] J. H. Lee & Y. J. Park, "High speed SOI buffer circuit with the efficient connection of subsidiary MOSFET's for dynamic threshold control", Proc. IEEE Int. SOI conference, 1997, pp. 152 - 153.

[7.29] T. W. Houston, "A novel dynamic Vt circuit configuration", Proc. IEEE SOI Conference, 1997, pp. 154 - 155.

[7.30] K. Mistry, et. al., "A 2V 0.35um PD-SOI SOI-CMOS technology" IEDM Technical digest, 1997, pp. 583 - 586.

[7.31] D. J. Schepis, et. al., "A 0.25um CMOS SOI technology and its application to 4Mb SRAM", IEDM technical digest, 1997, pp. 587 - 590.

[7.32] D. Suh & J. G. Fossum, "Dynamic floating body instabilities in PD-SOI CMOS circuits", IEDM Digest, 1994, pp. 661 – 664.

[7.33] C. Y. Chang & S. M. Sze, "ULSI Devices", John Wiley and Sons, 2000, ISBN 0-471-24067-2

Chapter 10: Analog Design

10.1 Introduction

Digital circuit designers are comfortable with PD-SOI and are taking advantage of the benefits of this technology. Somewhat less attention has been paid to analog applications in PD-SOI. Slow development of analog CAD tools for SOI applications may have contributed to this. Analog design requires consideration of threshold voltage variations, body-related effects and thermal management. Body ties can in some cases be used to stabilize threshold voltage and body related effects, but they may not always be the optimal solution.

10.1.1 Benefits of SOI for Analog Design

Improved frequency performance through reduced capacitance, higher drive current and a reduction in interconnect length are significant advantages of using SOI for analog applications. Noise and latchup are minimized through reduced substrate coupling. Silicon resistors have improved linearity with respect to absolute voltage in many cases, since they do not form reverse biased diodes to substrate (as resistor voltage increases the reverse biased diode depletion region increases in bulk material, resulting in higher resistances for the same resistor layout). Inductor Q can be enhanced through the use of very high resistivity substrates.

10.1.2 Drawbacks of Analog Design on SOI

The most significant drawbacks for analog designs on SOI are due to the floating body, and especially the kink effect. Body ties can be effective at low frequencies, however, at RF frequencies it becomes more of a challenge due to the RC time constant of the gate to body coupling. Another drawback

is poor thermal response due to buried oxide and trench isolation. Device noise is an issue when using PD-SOI devices, especially during operation near the kink region.

The Kink Region

Kink free operation of PD-SOI with a floating body is generally desirable for analog circuits. A cascode configuration (figure 10.1) makes it possible to bypass the kink effect by operating outside the voltage region in which the kink occurs. A reference voltage is provided to node V_{in}. Device M_2 is used to define the drain voltage of device M1 more precisely, and thus the output sink current of M2 is more accurately mirrored than a non-cascoded pair.

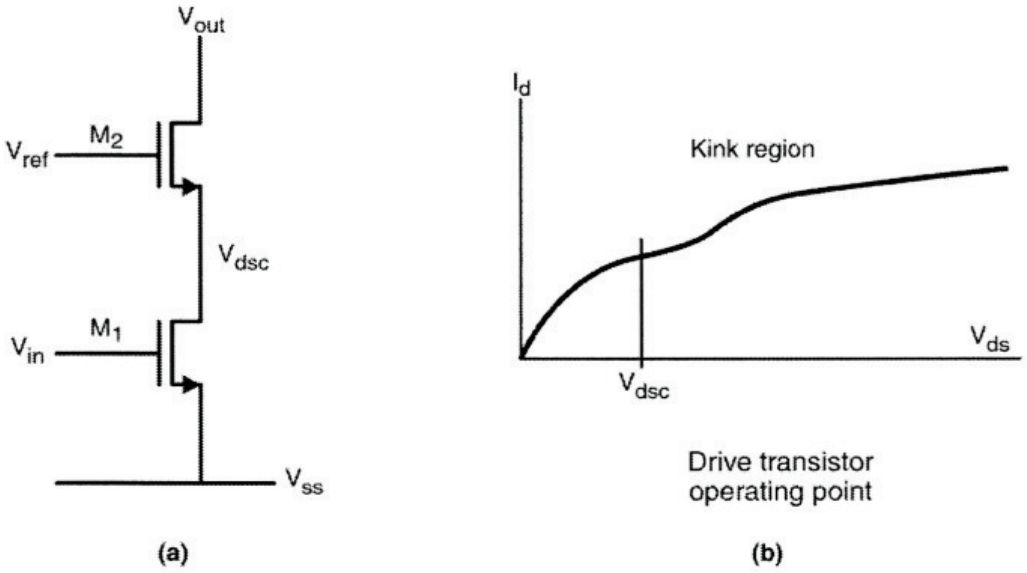


Figure 10.1: Demonstration of the operating point that can be maintained, from the PD-MOS device when used in a cascode configuration.

Figure 10.2(a) shows one example of how the circuit of figure 10.1 may be achieved in practice.

An additional benefit of operating the devices in this region is that noise resulting from impact ionization in the cascodes is reduced from the non-cascoded device configuration, as it appears in series with the high impedance of the driver device.

Figures 10.2(b) and 10.2(c) show the current and voltage waveforms as supply is ramped, for both the non-cascoded current mirror, and cascoded current mirror schemes.

Samsung Exhibit 1010, Page 136 of 204

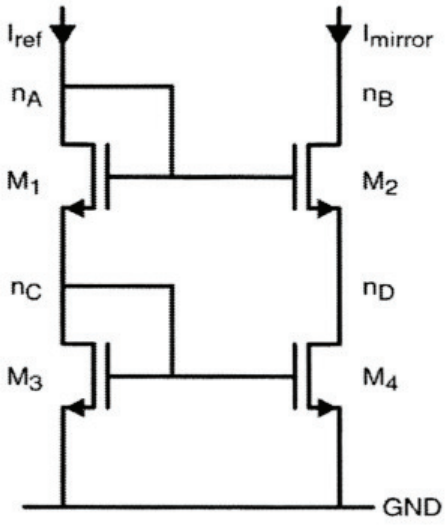


Figure 10.2(a): Basic cascode circuit design. This circuit allows the operating conditions of M4 to be restricted and keep away from the kink effect region of the MOS operating curve.

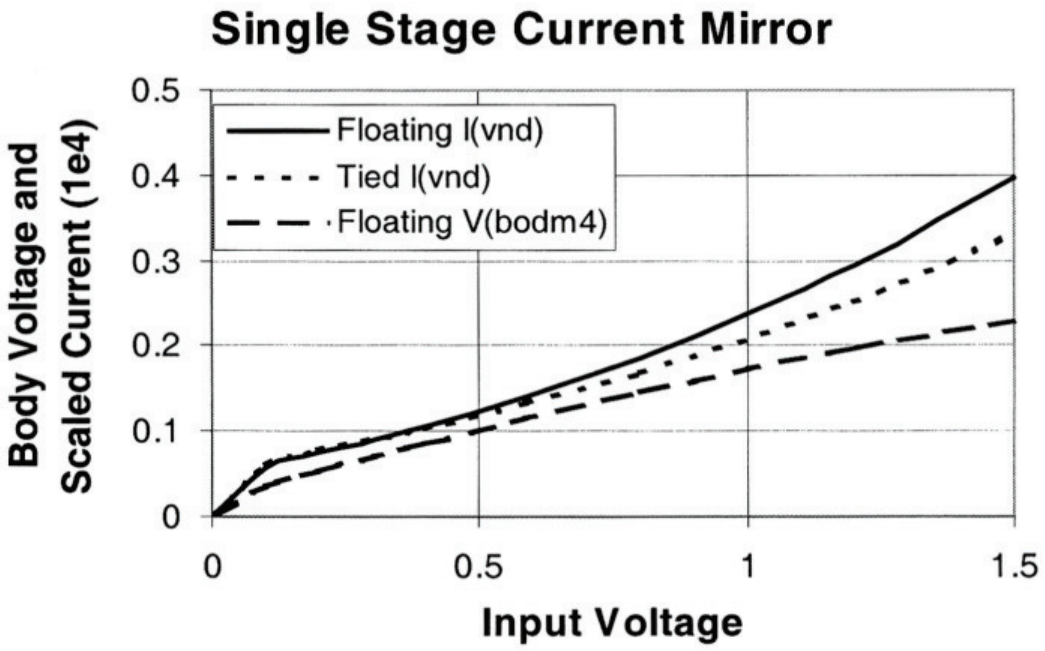


Figure 10.2(b): Current and voltage waveforms of non-cascoded current mirror configuration. Note that the SOI curve is steeper, representing poorer matching over supply voltage. However, curves for both floating body and tied body (bulk equivalent) devices have very poor mirroring.

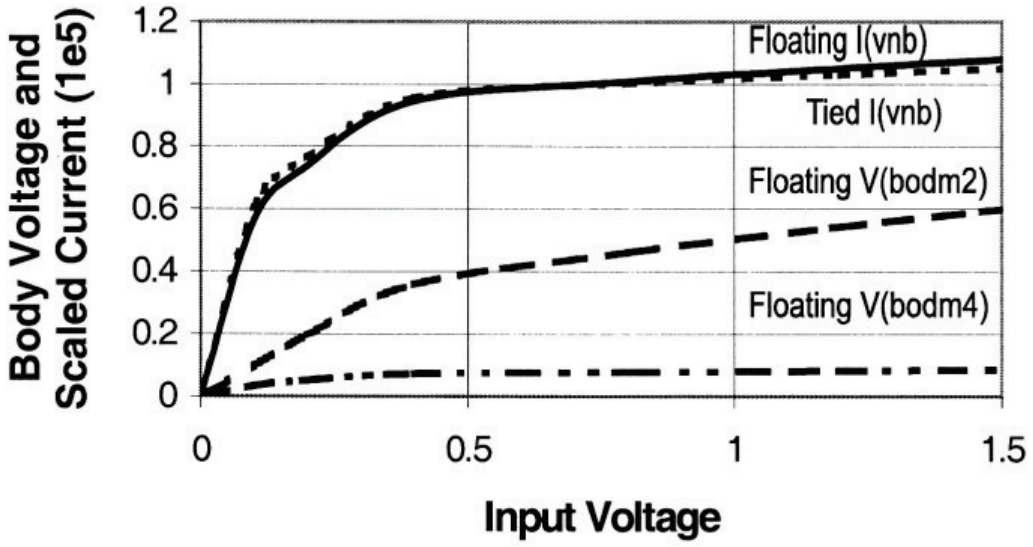


Figure 10.2(c): Current and voltage waveforms of cascoded current mirror configurations.

Cascoded circuits usually need relatively high supply voltages, or conversely output swings or input ranges are restricted. Figure 10.3 demonstrates the limitations of cascode usage in terms of supply voltage. The minimum supply voltage for accurate current mirroring is two NMOS threshold voltages (Vtn) and one PMOS threshold voltage (Vtp). This is the same as for bulk circuits with the same configuration.

10.2 Body Voltage Regulation

10.2.1 Dynamic Body

Dynamic body voltage control of PD-SOI MOS devices can be achieved through a simple connection between body and gate. However, the bias voltage limits its applicability. Active body-biasing circuits use additional circuitry to enable the increase in gate bias beyond the Vbe of the parasitic bipolar [10.1].

Figure 10.4 shows two circuit techniques for dynamic body biasing. One option is to add extra voltage, for example a forward bias diode drop, allowing the gate voltage to increase further before drawing current. No current will flow through the body path provided that the combined forward voltage is not reached. A disadvantage of the circuit is that the body voltage does not necessarily rise with the initial ramping of the gate voltage. Thus this scheme is not very efficient in fast switching environments. The other

option shown uses a current limiting component (in this case a resistor), permitting increase in the gate voltage even after the body voltage reaches the diode forward voltage drop. This has the advantage that the body voltage initially rises with the gate until it is high enough to turn on the diode. However, above this point, current flows through the current limiting circuitry and body diode, increasing operating current, and possibly limiting gate voltages.

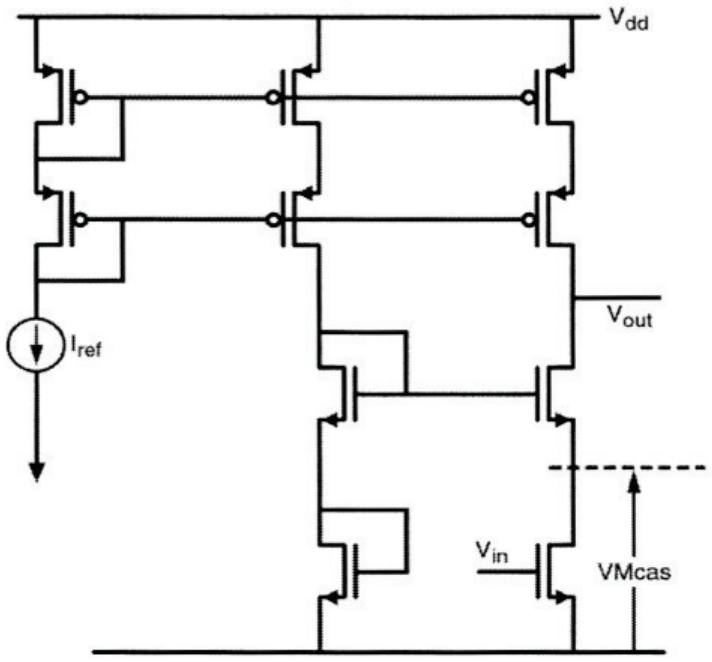


Figure 10.3: Demonstration of cascoding both PMOS and NMOS structures as a technique to avoid the kink effect.

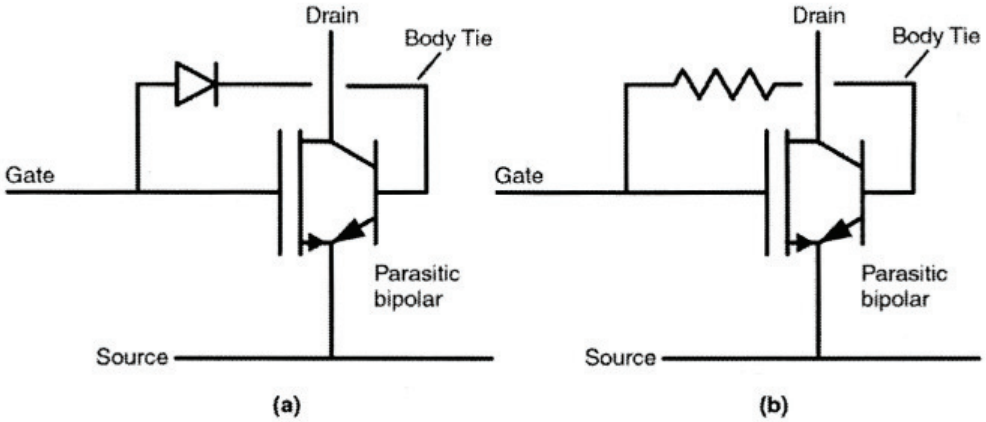


Figure 10.4: Dynamic body configurations (a) using a voltage threshold shifter (in this case a diode), and (b) utilizing a current limiting scheme (here a resistor).

Samsung Exhibit 1010, Page 139 of 204

Numerous other forms of dynamic body ties are possible, including a combination diode/resistor configuration between gate and body. The circuit of choice largely depends upon the application.

10.3 Circuit Thermal Coupling Effects

10.3.1 DC Thermal Coupling in Current Mirrors

Current mirror circuits rely on matched thermal and electrical conditions, usually through accurate layout techniques. The largest errors in bulk technology current mirrors are caused by electrical variations, particularly drain voltage mismatch between reference and mirror. Gate length reduction caused by technology scaling impacts matching of devices. Design changes such as increasing gate lengths to reduce channel modulation percentage, have minimized mismatch, but caused reduced circuit bandwidth. Channel modulation may also be reduced with cascode techniques (described above). This works well at voltages above 1.5V, but is more difficult to apply as supply voltages reduce. The current mirror in SOI has two further areas where mismatch may be introduced. These are the floating body and thermal mismatch.

External thermal effects can be minimized through adequate cross coupling and the application of common-centroid techniques. If the devices to be coupled can be combined within the same silicon mesa, thermal matching tends to be better in SOI than bulk material. However, thermal mismatch can still occur within the subcircuit cell and disturb the expected operation of the cell when the power dissipated on one side of a basic cascoded current mirror differs significantly from that of the other. For example, a 100μA DC current mirror dissipates approximately 100μA * Vt = 0.2V (20μW). The mirror device, meanwhile, may have a drain voltage of 1V, and with modulation effects this might be at close to 200μA current, thus dissipating 200μW. A local thermal resistance of 25000° C/W (chapter 11) would result in a local temperature rise of about 5° C. This compares to an insignificant rise in temperature in bulk material.

10.3.2 Transient Thermal Coupling in Current Mirrors

Thermal time constants for nominal size adjacent devices on SOI are around a microsecond [10.2, 10.3]. Transient switching of the mirroring device affects thermal dissipation. This in turn can couple to the reference device if the two are adjacent. Figure 10.5 shows a mirroring structure for determining transient thermal coupling. Repeating this structure with various device spacings permits the determination of short and long-range coupling.

Samsung Exhibit 1010, Page 140 of 204

Thermal gradients can introduce a feedback mechanism with time constants which are relatively long compared to the electrical time constants.

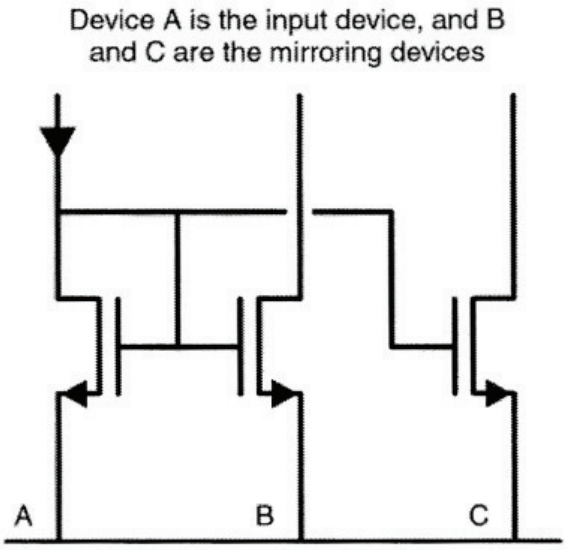


Figure 10.5: Dynamic thermal coupling configuration. This configuration can be used to determine coupling due to thermal effects, by placing multiple mirroring devices at different spacings.

A long thermal time constant introduces the possibility of unsimulated instability at frequencies less than 10-100MHz. Thus it is important to fully simulate thermal coupling in SOI circuits. In bulk silicon this effect is usually only seen in high current or high voltage structures such as power ICs. Spacing the devices apart further reduces intracell thermal coupling. However, when attempting to match for external thermal effects and process variation, increased separation is undesirable. It is worth considering placing several devices in the same tank using one of the layout schemes discussed in chapter 5 to minimize thermal mismatch, while maintaining close layout proximity.

10.4 Band-gap Designs

Most bandgap circuits use bipolar transistors or diodes as the reference element. Usually this is part of a so-called delta V_{be}, where the difference in V_{be} between two devices operating at different current densities is used to generate a reference voltage. Variations on this type of scheme, using MOS devices have been proposed, but generally have reduced accuracy. The NPNs and PNPs of a typical PD-SOI process have gains in the range of <1 to 10. Although low, it provides enough gain for some bandgap designs [10.4]. A simple bandgap structure, used frequently as a design example, is shown in figure 10.6.

Samsung Exhibit 1010, Page 141 of 204

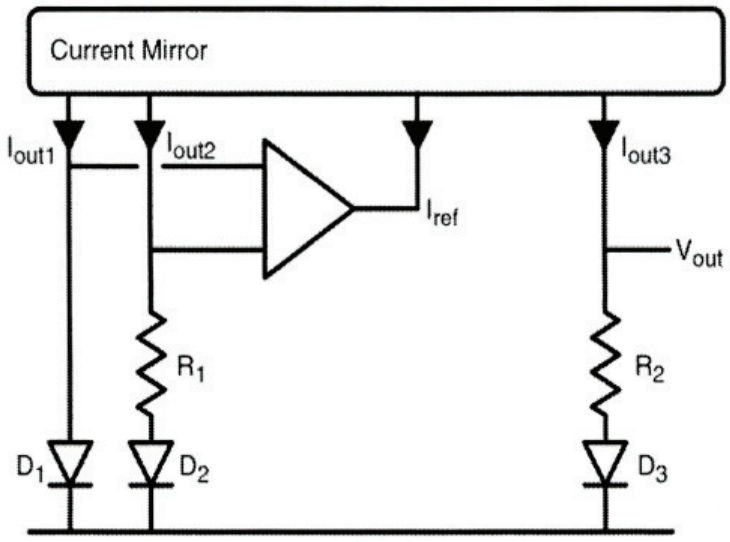


Figure 10.6: Basic conceptual bandgap circuit. Iout1 and Iout2 are usually equal. D2 is several times larger than D1, and current through R1 equalizes the amplifier input voltages. Iout1, Iout2 and Iout3 are mirrored values of the Iref current. Vout is normally the bandgap voltage of 1.2V.

The forward bias diode voltage of device D1 equals that of the larger D2 device, plus the resistor R1. Usually there are two stable solutions, the trivial state of zero current, and a current, which maintains the inputs to the amplifier at the same voltage (about 0.7V at room temperature). Circuitry (not shown) prevents the zero current option in normal operation. A typical diode area for D2 is 4x that of D1. The operating condition is based on the following assumptions:

$$V_{d1} = V_{d2} + V_{r1} \quad \ldots\ldots\ldots (1)$$

Thus:

$$V_{d1} - V_{d2} = \Delta V_d = V_{r1} \quad \ldots\ldots (2)$$

Since $\Delta V_d = \ln 4 * KTq^{-1}$ [10.5], then $V_{r1} = 36mV$ (at room temperature).

Therefore, for a 10μA diode current, the resistor must be approximately 3.6KΩ. A low temperature coefficient current can be obtained by tuning the resistor temperature coefficient, although this is not necessary if only a bandgap output voltage is required.

Most PD-SOI processes have optional bipolar devices available. By not using MOS devices floating body effects are clearly eliminated. However,

Samsung Exhibit 1010, Page 142 of 204

while they are available, most MOS SOI processes are not optimized for bipolar structures. If the beta of the bipolars being used is less than 10, some compensation for low gain operation may be required, possibly including the use of MOS beta helper devices. Figure 10.7 shows a simple bandgap circuit which uses bipolar devices. This circuit functions as follows: At equilibrium conditions the voltage across Ql and Q4 base-emitters equals the voltage across R1 and the base-emitter nodes of Q3 and Q2. Assuming Q2 is 4x the area of Ql and Q3 and Q4 are of equal size, and if the base current is small with respect to the collector current, the following equation applies:

$$VQ1be + VQ4be = VQ3be + VQ2be + VR1 \quad . \quad . \quad . \quad . \quad . \quad (3)$$

Neglecting base current, Ql and Q3 are part of one current path, and Q2 and Q4 are part of a different current path. The two currents are not necessarily (or even usually) equal. Re-arranging (3):

$$VQ3be - VQ1be = VQ4be - VQ2be - VR1 \quad . \quad . \quad . \quad . \quad . \quad (4)$$

If Q3 and Ql are the same size, then (4) simplifies to:

$$VR1 = VQ4be\text{-}VQ2be \quad . \quad . \quad . \quad . \quad . \quad (5)$$

This can be shown to be the same as equation (2) above.

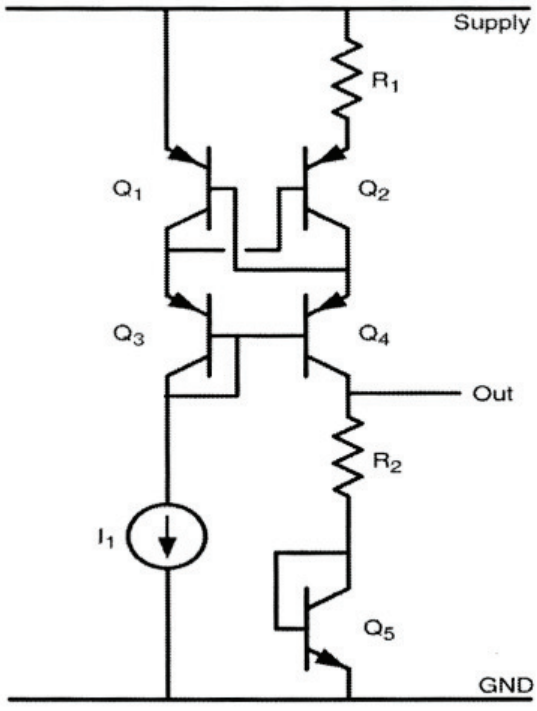


Figure 10.7: Bipolar based bandgap reference circuit

Samsung Exhibit 1010, Page 143 of 204

If bipolar gain is less than about 10, it is better to use MOS devices in most parts of the circuit. MOS devices can replace bipolar devices in current mirror structures, and can either be floating body devices, possibly with cascoding, or body tied devices. The bandgap circuit is a good candidate for body ties, since the circuit operates under DC conditions. Depending upon accuracy requirements, without any special design considerations, accuracy of approximately 20% is achieved with floating body SOI designs. With cascoding this improves to better than 10%. The use of body ties brings this to between 2-5%, similar to that of circuits built on bulk material. Trimming techniques allow for better than 1% accuracy.

When designing bandgap circuits for SOI it is important to account for the start-up condition of any floating body MOS devices. This is because the time constant of the body voltage is of the order of milliseconds. During startup, the bandgap itself could be expected to be fully operational within a few microseconds. However, floating bodies within the bandgap circuitry may affect the output voltage for several milliseconds.

10.4.1 β helper circuitry

Figure 10.8 shows a simple bandgap design [19.6]. This is effective if transistor gain is greater than about 50, but loses accuracy rapidly as gain reduces. This is the result of current being diverted from the collector of Ql into Ql and Q2 bases. Thus current mirrored into the output device M3 is lower than expected, and so the bandgap output voltage, BG_{out}, is low.

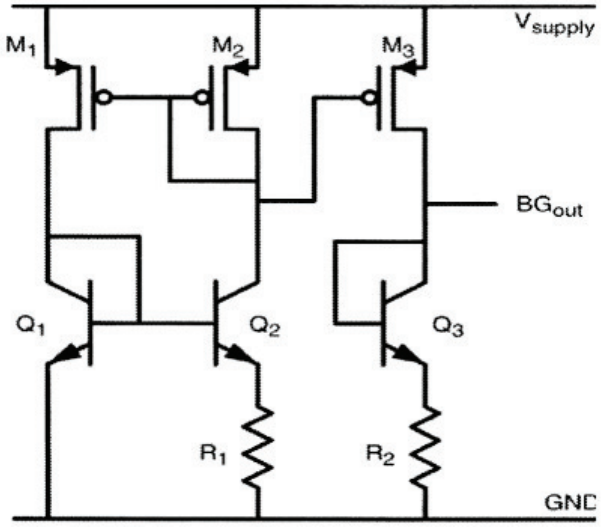


Figure 10.8: Simple bandgap circuit. This loses accuracy as the transistor gain reduces, and is thus only useful when a well behaved, high gain bipolar is available (M1, M2 and M3 are body tied to source structures).

Samsung Exhibit 1010, Page 144 of 204

This circuit can be adapted for low gain bipolar devices, such as those typical of PD-SOI processing, with the addition of a β-helper. β-helper devices compensate for low β bipolar transistors by providing base current from a low impedance supply (figure 10.9) [10.7]. Here, components M4, M5 and M6 have been added. Hence transistor M4 eliminates the base current losses but inaccuracy may still persist. If Q2 gain is very low significantly more current flows through Rl than through M2. To compensate for this it is possible to mirror 50% of the M4 current back into Q3 and R2. This circuit works with very low gain bipolar devices.

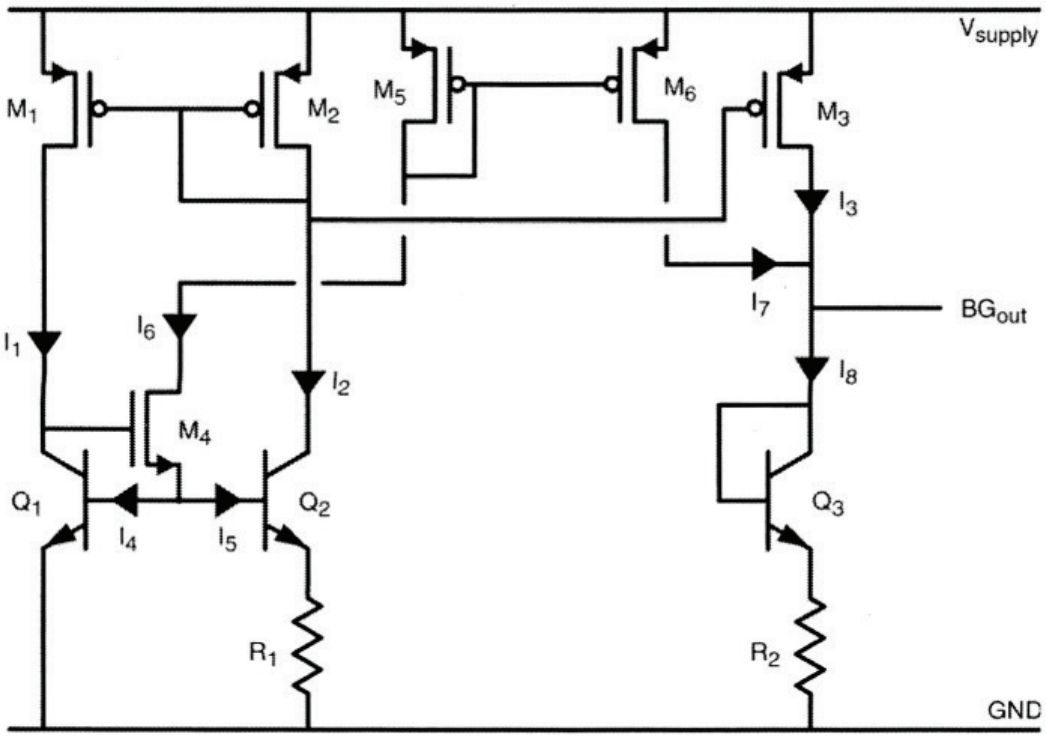


Figure 10.9: Compensation scheme for low gain bipolar structures such as those typically available in PD-SOI processes (here M1, M2, M3, M5 and M6 are body tied to source structures, M4 can float).

In the simplest case we assume that base currents I4 and I5 are equal

Therefore, I6 = 2*I5 = 2*I7

With an ideal current mirror, I1 = I2 = I3

Therefore Vbgout = Vbeq3 + (R2 / R1) * Δ Vbe

With appropriate sizing of R2 and Rl the bandgap output voltage, V_{bgout}, can be made virtually constant over typical operating conditions. Figure 10.10 shows output voltage over temperature for the circuit in figure 10.9.

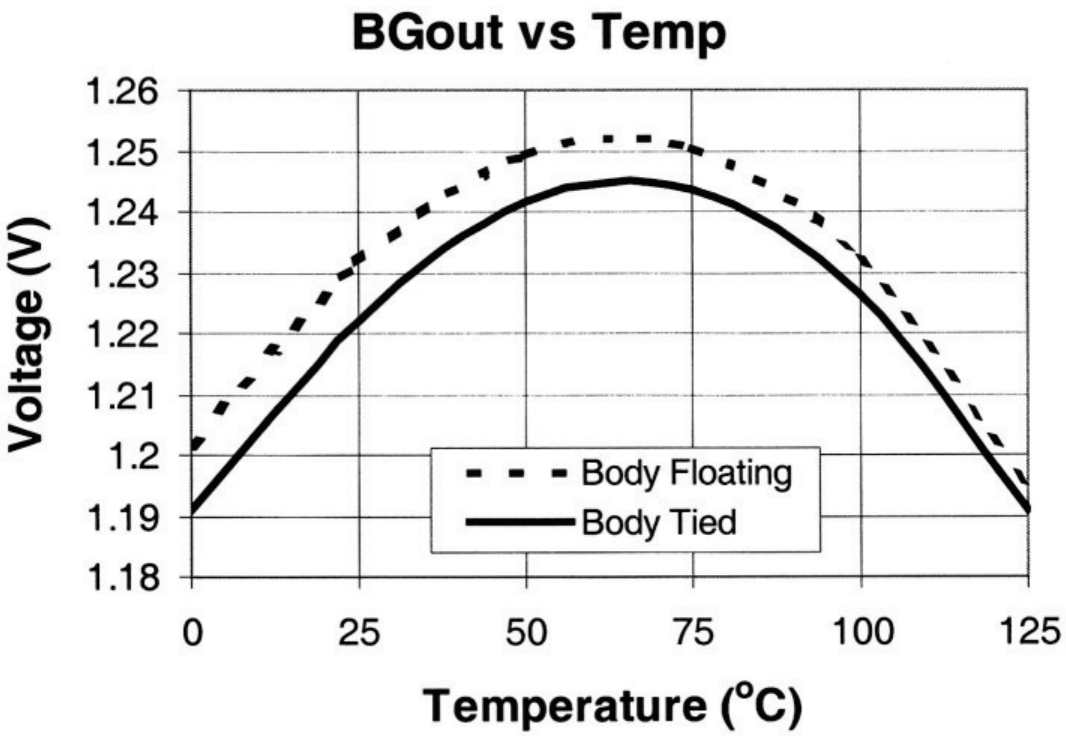


Figure 10.10: Output voltage waveforms for floating body and body-tied versions of the bandgap circuit shown in figure 10.9.

10.4.2 Voltage Reference using "Threshold Voltage Difference"

The "threshold voltage difference" principle makes use of the difference between gate-source threshold voltages of two MOSFET devices with different Vt implants [10.8]. This difference remains almost constant, independent of temperature, current or body voltage. The threshold voltage difference principle can be used for creating voltage reference circuits that operate up to 275°C [10.9].

The circuit is shown in figure 10.11, and is based on an operational transconductance amplifier (section 10.7.4). Device Ml has a higher threshold voltage than M2. Feedback through the resistor divider (R1 and R2) enables the generation of a bandgap voltage that is relatively constant. Optimum performance is achieved with body tied components, particularly for Ml and M2, although body tying M3 through M6 is advisable. No significant benefit is gained from body tying M7 through M11.

The output voltage V_{bg} is defined as:

$$V_{bg} = ((R2+R1)/R1) * (VtM1 - VtM2)$$

Samsung Exhibit 1010, Page 146 of 204

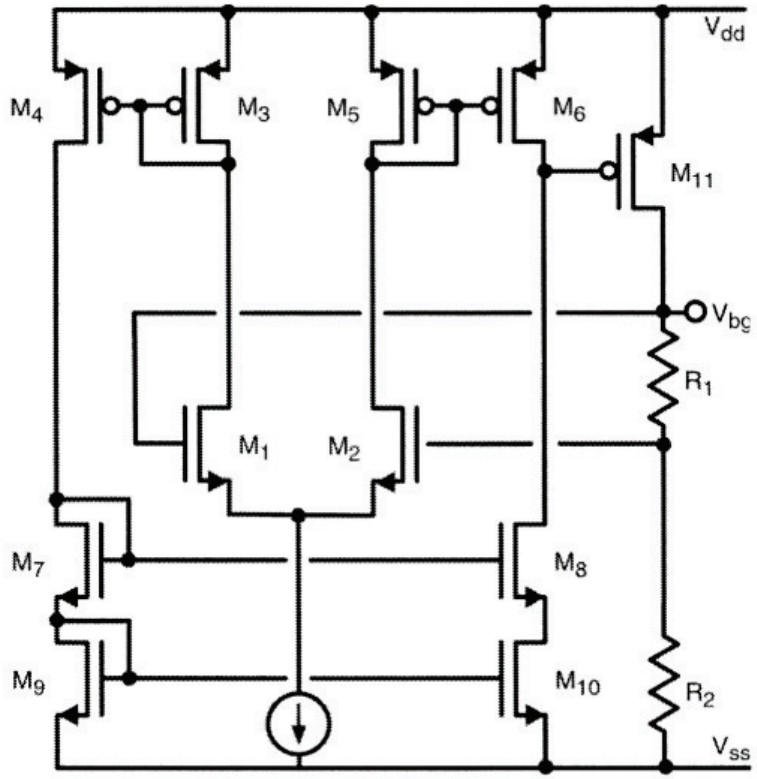


Figure 10.11: Threshold Voltage Difference type of bandgap reference circuit. This structure can be built on bulk silicon or SOI. Resistor matching may be better in some cases in SOI, but body voltage of the input pair M1 and M2 needs to be adequately grounded, or tied to source for optimal SOI performance.

10.5 Charge Pump Circuitry

Charge pump circuits are used to provide a voltage outside the normally available power supply rails, for example a voltage higher than supply, or a reversed polarity voltage. A common application is biasing the pass gates of DRAM devices (chapter 9). Figure 10.12 shows a typical charge pump design for generating a voltage above the supply. A 50% duty cycle clock provides the switching input, often operating at a frequency around 1-50 MHz. A signal 180° out of phase with the clock input is generated with an inverter.

Each of the MOS devices Ml through M4 acts as a unidirectional switch. An unloaded output voltage of over 3V is attainable, with a supply of 1V and a MOS threshold voltage of 0.2V [10.10]. This type of circuit is often easier to implement in SOI than in bulk, as there is complete isolation of the MOS devices. Isolation of the devices eliminates the possibility of latchup and reduces the number of leakage paths. No body ties are required in this circuit

design; indeed adding them may cause unwanted leakage in some modes of operation (refer also to chapter 9).

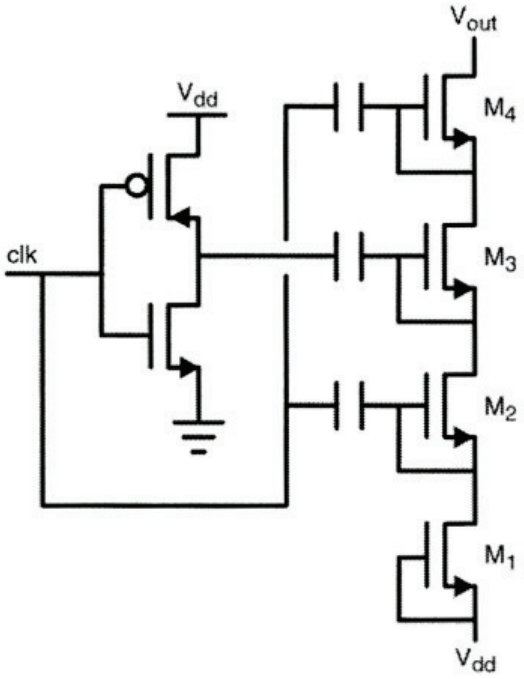


Figure 10.12: Voltage quadrupler charge pump configuration. The MOS devices in this configuration are completely isolated in SOI, thus unlike their counterparts on bulk silicon there is no risk of latchup.

10.6 Amplifiers

10.6.1 Sense Amplifier

Dynamic SOI sense amplifiers for memory applications are discussed in detail in chapter 8, but are considered here briefly in the context of general analog design. Sense amplifiers on PD-SOI are susceptible to body voltage induced variation and mismatch, especially if the read operation is repeatedly performed in one state [10.11]. This can cause asymmetric charge accumulation, resulting in read failure. One solution is to tie the bodies to source or supply (Vss for NMOS, Vdd for PMOS). This, however can lead to undesirably high threshold voltages, and reduce the operating range of the amplifier.

An option for equalizing body voltages is to flood the input devices with charge prior to read [10.11]. Body voltage rises, limiting at the voltage where the parasitic bipolar turns on, which is a similar voltage for both devices. Small PMOS devices are used to charge the body-contacted NMOS devices, as in figure 10.13 (This can also be applied to PMOS input pairs, by

Samsung Exhibit 1010, Page 148 of 204

using NMOS charging devices). The charging devices (PM1 and PM2) are turned on at some time before the amplifier is to read. After both bodies have reached equilibrium PM1 and PM2 are turned off. This has to occur just long enough before the 'read' for the parasitic bipolar to turn-off. The minimum time between turning off current to PM1 and PM2, and the 'read' is defined by the base (body) minority carrier recombination time. Minority carrier recombination time is typically less than 1μs. Providing the read is done while the input pair body voltages remain in a similarly charged state, improved matching is achieved at reduced threshold voltage. The body modulation technique can be used for any comparator input, providing continual read of the input is not required, as there is the potential for the charging phase to affect the amplifier output state.

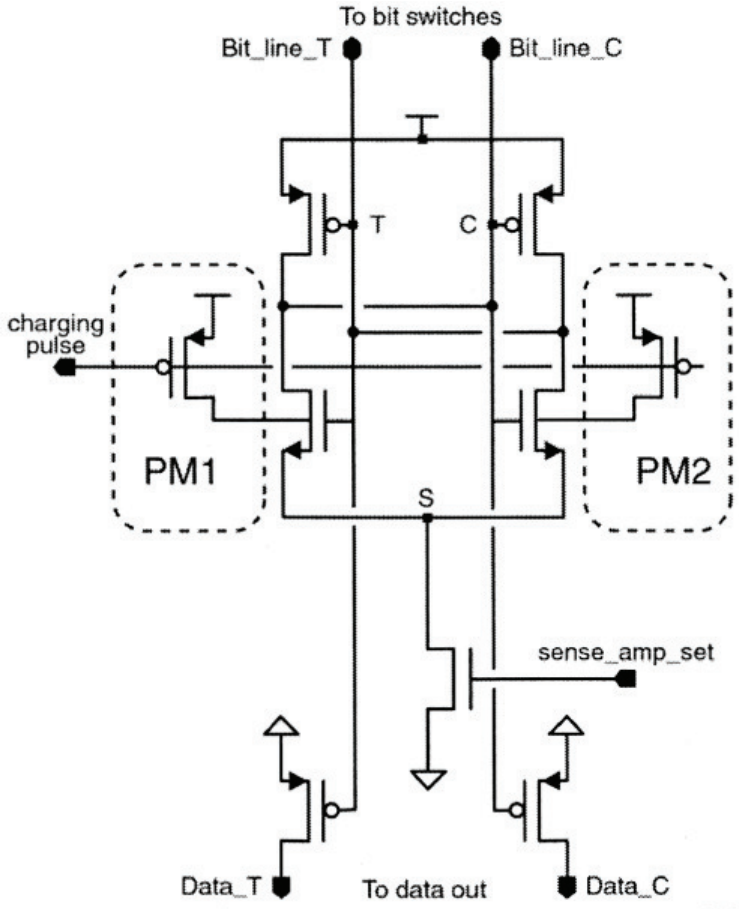


Figure 10.13: Schematic showing the use of body-charge modulated concept for a RAM sense amplifier.

10.6.2 Operational Amplifiers

A simple topology used for a CMOS operational amplifier (op-amp) is shown in figure 10.14(a). This uses a matched pair of input devices, with the output brought being a simple class A design. The CMOS op-amp does not

Samsung Exhibit 1010, Page 149 of 204

have the gain, offset or frequency of its bipolar counterpart, but has gained acceptance due to ease of integration into mixed signal IC designs.

The voltage gain of the basic operational amplifier can be determined by considering the input and output stages individually. Assuming NMOS devices Ml and M2, and PMOS devices M3 and M4 are matched, the small-signal voltage gain is [10.5]:

$$A = - gm1 gm6/((go2+go4)(go6+go7))$$

Where gm is the device transconductance and go is the device small-signal output conductance. In PD-SOI there is no guarantee that an assumption of matched devices are, in fact, matched. Even with bulk processes variation can occur due to channel modulation, and with PD-SOI that is compounded by the addition of the kink effect. Thus this circuit is of limited applicability with SOI technology.

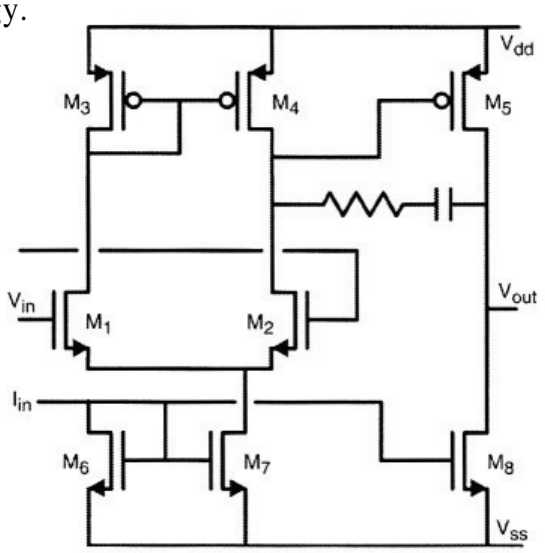


Figure 10.14(a): Schematic for a PMOS input, CMOS operational amplifier. This circuit is prone to offset problems when used with SOI processes.

Figure 10.14(b) shows a simulation of the body bias of the circuit shown in figure 10.14(a). Inputs in1 and in2 represent the input voltages, and bv1 and bv2 the corresponding input pair body voltages. As expected the body voltages vary depending upon the applied input voltage. In particular, body voltage 2 follows the rising large-signal input, until the switching threshold is reached. After the input MOS2 turns on, the body voltage is clamped at the source/drain voltage, collapsing the body voltage. Close to the crossover threshold the body voltages are closer, but even here there is an offset, due to the non-symmetry of the circuit and input ramp rate.

Samsung Exhibit 1010, Page 150 of 204

Figure 10.14(c) shows the same circuitry, simulated with a very slow ramp. It is evident that the ramp speed significantly affects the body voltage of the floating input pair. Analysis of the crossover threshold also shows that this is significantly impacted by the transition speed, which can alter the threshold point by up to 25mV in this circuit.

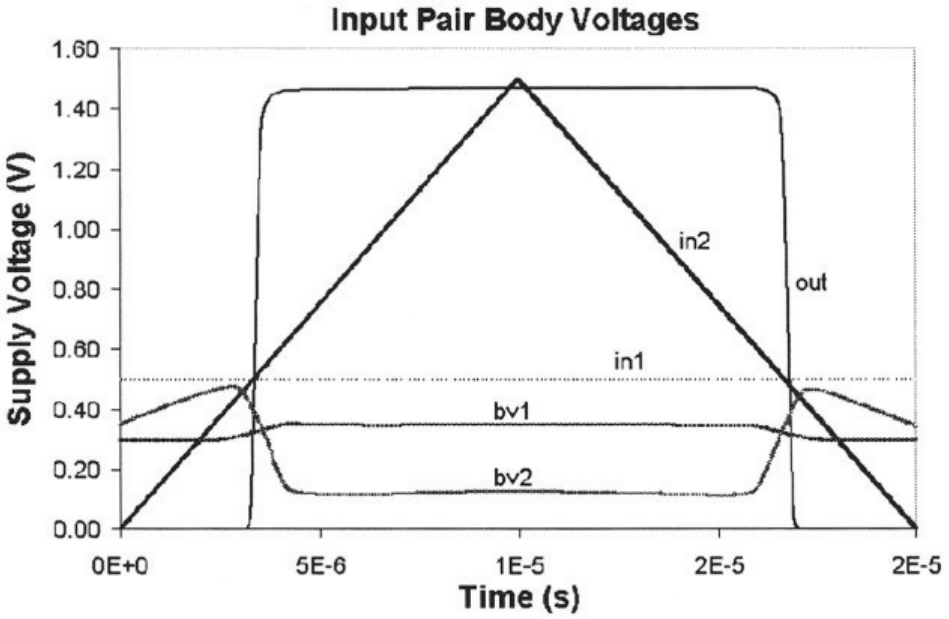


Figure 10.14(b): Simulation of the body voltage variation for the circuit shown in figure 10.14(a).

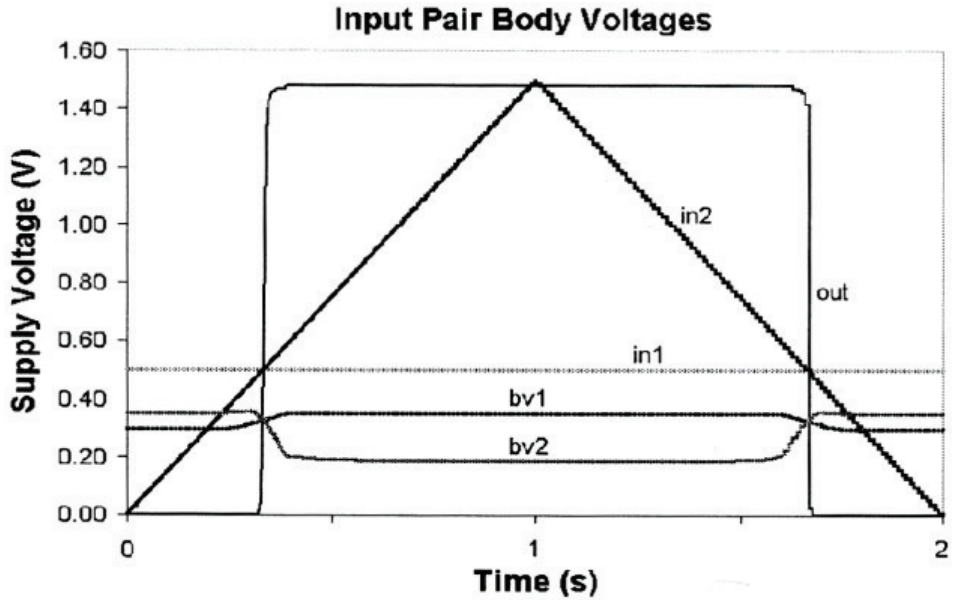


Figure 10.14(c): Simulation of the body voltage variation induced in the circuit shown in figure 10.14(a), for a very slow ramp. This is slow enough that capacitive coupling of the input ramp does not affect body voltage.

Cascoding within the op-amp has some advantages: Voltage gain can be improved, as a result of increased output resistance of the configuration. High frequency capacitive feedback is also reduced. Cascoding also helps to maintain drain voltages, which stabilizes the body-voltage, and minimizes the gain slope with respect to variations in supply voltage. A cascoded op-amp is shown in figure 10.15. The PMOS input transistors M1, and M2 are cascoded using NMOS devices M3 and M4. This circuit has a higher gain than the circuit shown in figure 10.14, and is also less susceptible to body effects. However, the output voltage swing is degraded compared to non-cascoded schemes. Additional cascoding of the input pair further restricts the voltage variation at the source-drains of the input pair (figure 10.16(a)), limiting the leakage induced body voltage drift.

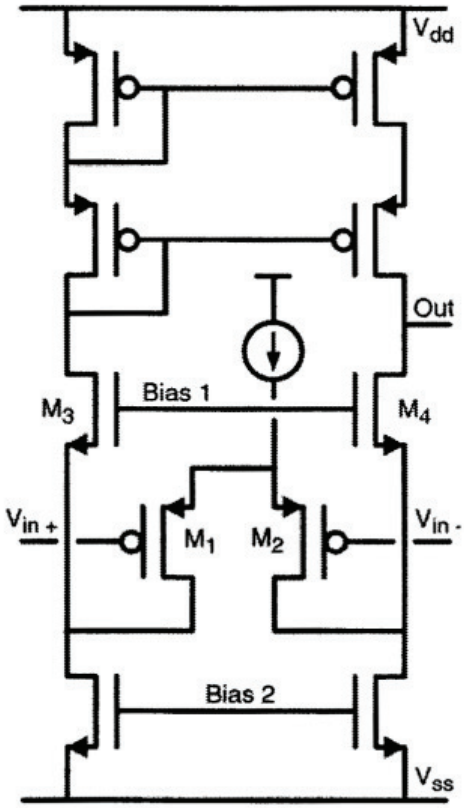


Figure 10.15: Cascoded opamp design that holds the input pair output voltages at approximately a constant voltage.

Simulated waveforms showing input, output and body conditions for the circuit are shown in figure 10.16(b) and figure 10.16(c). These indicate the improvement that can be made to body voltage stability, resulting in improvements to the offset over all conditions.

Samsung Exhibit 1010, Page 152 of 204

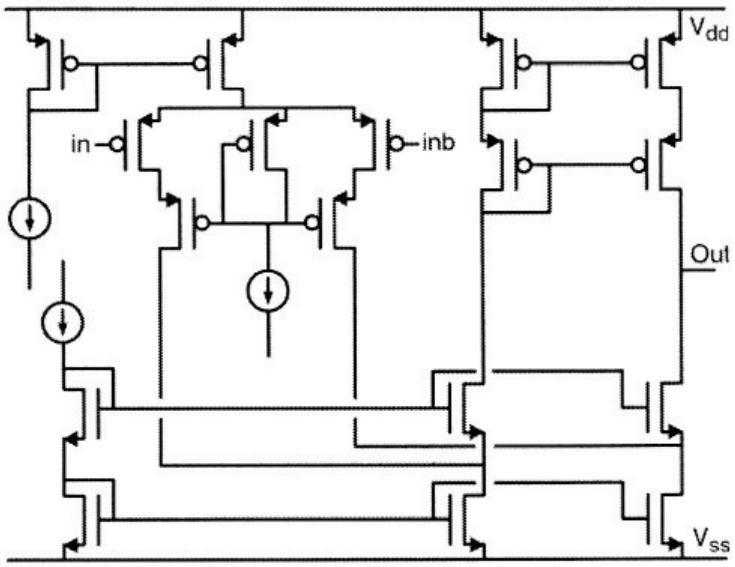


Figure 10.16(a): Further circuit modifications restrict the drain-source voltages of the input pair, inhibiting leakage dependent voltage drift.

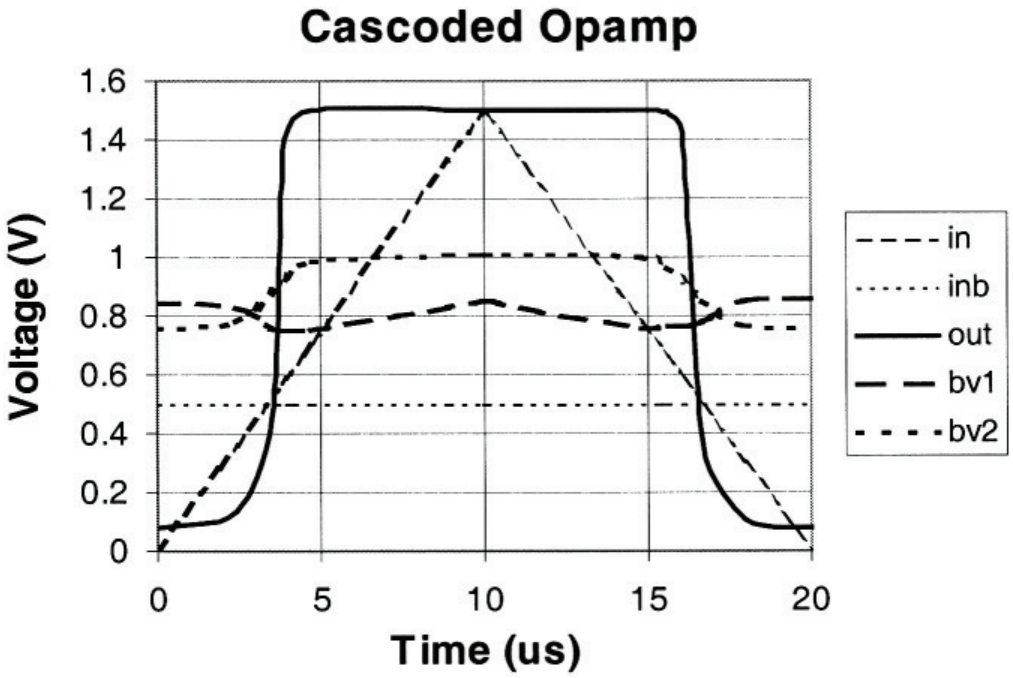


Figure 10.16(b): HSpice Simulation of the body voltage variation for a cascoded input operational amplifier, with a fast input ramp.

If a high enough power supply voltage is available telescopic designs help maintain the DC body voltage characteristics. For example, the circuit in figure 10.17 requires a voltage of approximately three NMOS threshold voltages and two PMOS threshold voltages as the minimum supply voltage.

Samsung Exhibit 1010, Page 153 of 204

Even this circuit is prone to some variation due to the non-cascoded M9 and M10 current mirror.

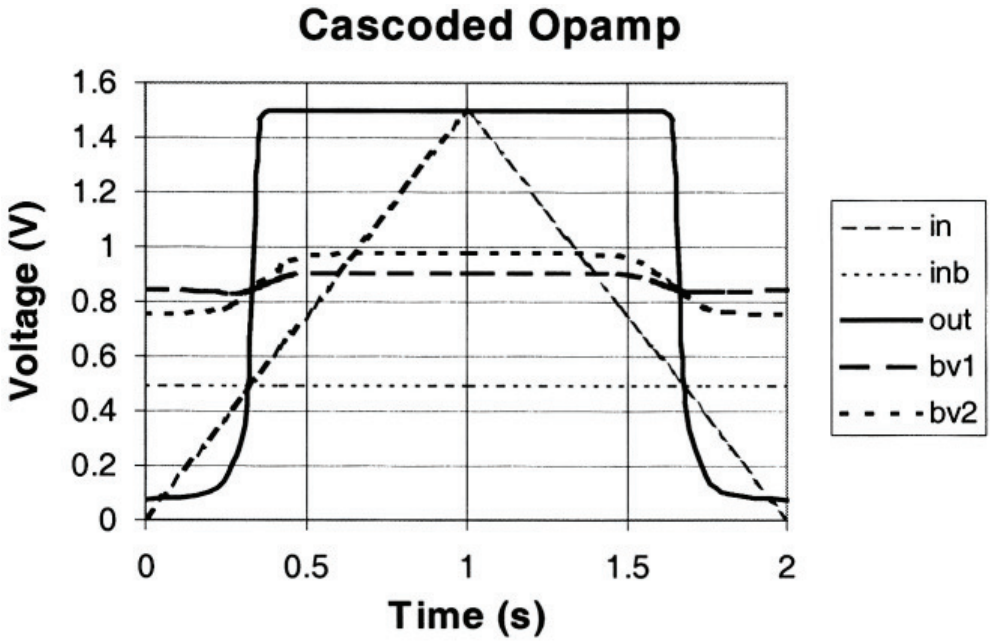


Figure 10.16(c): HSpice Simulation of the body voltage variation induced in a cascoded input operational amplifier, for a very slow ramp of 1.5V/second.

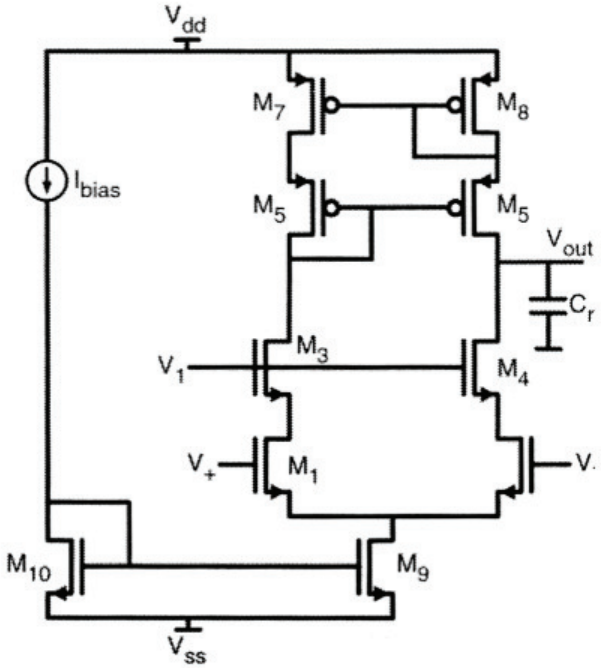


Figure 10.17: Example of a telescopic op-amp design. The drawback of this type of design is its requirement for a supply voltage higher than permitted in many SOI processes.

Samsung Exhibit 1010, Page 154 of 204

10.6.3 Operational Transconductance Amplifier (OTA) Design

Even the basic OTA design has reasonable component matching to ensure balanced operation (figure 10.18). This is particularly useful in SOI applications. As a result high frequency OTAs have been successfully produced in SOI [10.12]. Technology improvements can boost the operating frequency of transconductance amplifiers above that normally obtainable from bulk material, through reduction of source/drain-to-substrate capacitances [10.13]. Folded-cascode OTAs have also been implemented in SOI.

OTAs for switched-capacitor applications drive a capacitive load and require a high-impedance output. In addition they have to be stable in unity-gain feedback mode. This requires good modeling capability. To ensure stability the second pole of the circuit performance must be higher than the maximum threshold frequency, to provide adequate phase margin and ensure stability. For frequencies above about 100 MHz, transconductance and capacitances are highly frequency dependent. Most circuit simulations substitute a lumped gate resistance model for the physically distributed gate resistance. For high gate resistance systems operating at high frequencies and where the device transconductance frequency limit is included, the lumped gate resistance model is not valid.

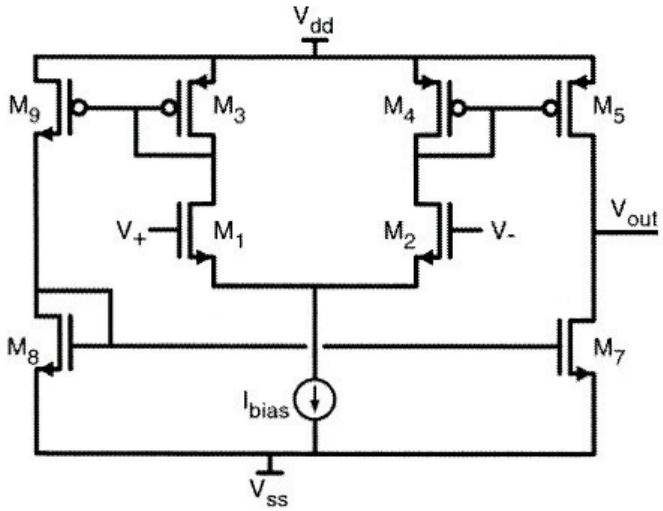


Figure 10.18: Basic, single-stage Operational Transconductance Amplifier.

Examples also exist of OTA designs for radiation-hard environments [10.14]. This structure uses a CMOS SOI process using "gate-all-around" (GAA) devices [10.15]. Most GAA processes require two additional process steps over standard SOI to create a cavity under the transistor areas (chapter

Samsung Exhibit 1010, Page 155 of 204

13). The single stage OTA is reasonably good for SOI applications, since the voltages are matched on all stages except the output stage. Further improvement can be achieved through cascoding of the NMOS current mirror.

10.7 Matching

Some component matching techniques in SOI technology are similar to those in bulk silicon. SOI devices, in certain applications, are less sensitive to supply voltage variation, which can cause problems with circuits using bulk material. This is mostly in components requiring specific non-supply or ground body biasing, or tank resistor biasing, which, when diffused into bulk silicon, may cause device differences.

Matching of MOS devices uses the same techniques in SOI and bulk (figure 10.19). A cross-coupled pair of nMOS devices is used, all being orientated similarly. Device '1' is a combination of structures 'a' and 'c', and device '2' of the matched pair is a combination of structures 'b' and 'd' (body ties not shown). This structure has good immunity to external thermal and process related gradients, but does not account for local device heating within the cross coupled configurations.

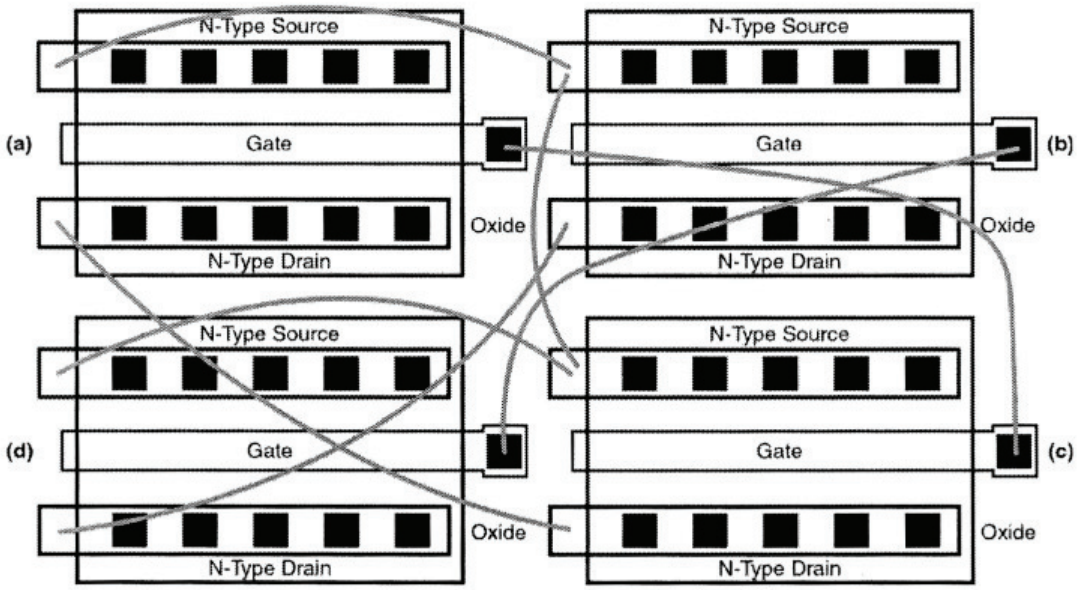


Figure 10.19: Cross coupling technique, showing coupling method for source, drain and gate, for a common source input pair.

Drain conductance varies with frequency as a result of self-heating [10.16]. This implies self heating impacts the behavior of small-signal amplifying

stages. Gain versus frequency plots show self-heating causes a gain change at low frequencies. In addition simulations demonstrate early roll-off, introduced by thermal time constants.

10.8 Output Stages / Buffers

Output stages may be hundreds or thousands of times larger than the width of a device used for core logic. It is worthwhile allowing the body to float, in order to achieve a higher current density capability during switching. This, however, can add to quiescent current leakage.

While it is not universally applicable, due to specific circuitry requirements, to reduce leakage in output structures it is often worth using a body tie configuration that is at ground potential in standby conditions. This achieves low standby leakage, but permits the body to float during operation. Positive body modulation during operation improves current density (figure 10.20).

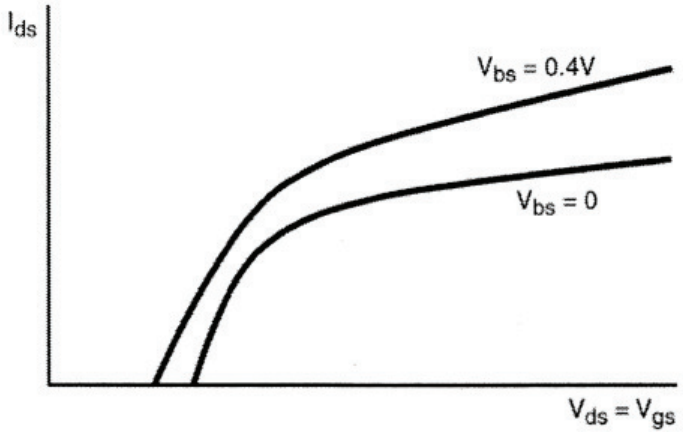


Figure 10.20: Graph showing the Ids variation with body modulation, illustrating improved performance in the operating state.

The two effects can be combined by using a body-tied-to-source state for standby and during operation tying the body to a somewhat positive potential for an NMOS (or negative with respect to supply for a PMOS). This gives the required drive current capability and the potential for standby current minimization through reduction of the output device size. An example of this combination of a PD-SOI buffer circuit with dynamic body biasing is shown in figure 10.21.

When V_{in} is switched low, the MN1 output device is switched on, and its body is biased high by the low current MP2 device. When V_{in} is switched high, the MN1 body floats. The reverse mechanism applies for the MP1 output driver.

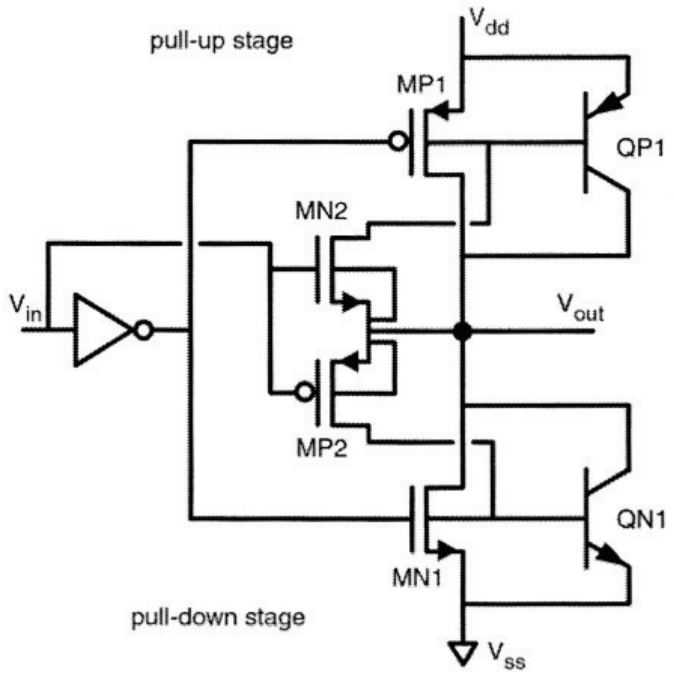


Figure 10.21: Buffer output stage with dynamic body biasing.

10.9 High Voltage and Power Applications

SOI has significant advantages over bulk silicon when high voltage circuitry is required. Due to component isolation in SOI material, it is easy to design high voltage devices without adding excessive process complexity or cost. It is also simpler to avoid high voltage parasitics caused by inversion of the active region. High voltage structures, including the DMOS power transistor, have been discussed in chapter 3.

Output stages usually drive high voltages and/or currents when they interface to the outside world. Power dissipation can significantly increase device temperature, reducing performance and efficiency. It is generally considered important in SOI design that simulations of output structures are completed with the thermal dissipation (temperature) node activated (chapter 5).

10.10 Sample and Hold Circuitry

The design of sample and hold circuitry on SOI poses some specific design problems (figure 10.22). The input and output buffers require the same considerations as operational amplifier designs. The electronic switch is usually a MOSFET. In the case of PD-SOI the risk of leakage due to the floating body dictates that the body should be tied to the appropriate power supply rail in most cases. SOI based sample and hold circuits have reduced stray capacitance associated with the electronic switch and therefore

Samsung Exhibit 1010, Page 158 of 204

contribute reduced capacitive coupling offset. This can permit smaller size storage elements. Conversely, with thinner gate oxides, gate leakage may become an important consideration in circuit design (in both bulk and SOI designs) (refer also to chapter 6).

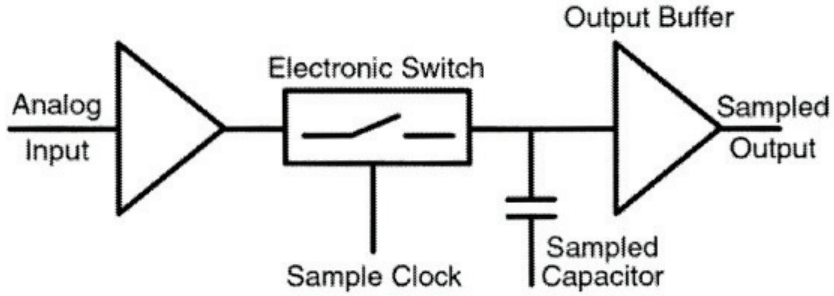


Figure 10.22: Block diagram of a sample and hold circuit. The input signal is buffered before passing through an electronic switch (usually a MOSFET). A storage capacitor maintains the voltage, which is buffered through a high- input-impedance unity-gain op-amp.

10.11 Circuits for RF/Wireless Applications

SOI is used for RF applications in the low GHz range [10.17], and the need for low-cost, low-power system-on-a-chip applications has led to investigation of SOI as a substrate for wireless applications [10.18]. High-resistivity substrates improve inductor Q values to a point where they are adequate for RF applications.

The RF-transmitter may use SiGe bipolar, silicon bipolar or sometimes MOS devices, thus combined bipolar and CMOS SOI is useful for full integration of analog and digital functions on one chip. SOI also provides isolation between the digital and analog circuitry, and input and power output sections of the chip. MOS devices on SOI have superior RF performance because of the inherent device oxide isolation [10.19, 10.20].

A direct-conversion architecture for receiver and transmitter is typical. [10.21]. Delta-Sigma modulators have been constructed in SOI [10.22], creating a mixed signal SOI CMOS process. Direct up-conversion transmitter architectures are commonly used. The baseband signal is mixed with a local oscillator (LO) at the transmission frequency (figure 10.23).

The route between antenna and low noise amplifier is termed the receive path. Once amplified, this signal is mixed with a locally adjusted oscillation frequency (shown here as a VCO). If an intermediate frequency is used it is often achieved with a fixed frequency local oscillator.

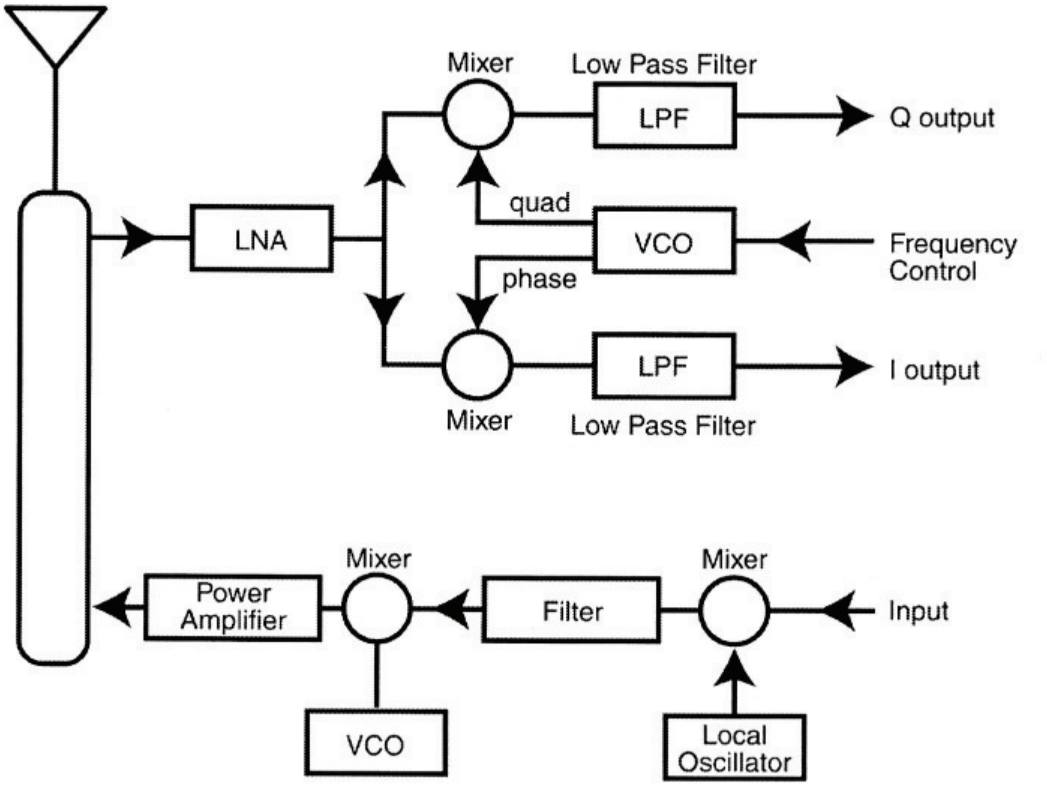


Figure 10.23: Wireless transceiver architecture. This block schematic shows that most circuit blocks are made of simpler elements, described elsewhere in this chapter.

Wireless architectures are made from many simple building blocks, such as low noise amplifiers, mixers and voltage controlled oscillators. Most of these are described within this chapter.

10.11.1 Radio Frequency Low Noise Amplifier (LNA)

SOI makes the task of integration of a single chip wireless transceiver very much simpler. The reduced capacitance of SOI over bulk MOS devices results in higher frequency capability. SOI provides the option of isolated high frequency bipolar transistors and also permits isolation between all types of devices. Furthermore, high resistivity, low-loss dielectric substrates enhance the quality factor of inductors. The frequency limit of operation in monolithic integrated circuits are defined by both the frequency capabilities of the transistors and the properties of the passive components [10.23].

A two-stage radio-frequency amplifier topology designed in SOI is shown in figure 10.24 [10.24]. On-chip inductive source degeneration is used for improved impedance matching and optimized noise figure. This topology has been demonstrated to operate with a 1V supply.

Samsung Exhibit 1010, Page 160 of 204

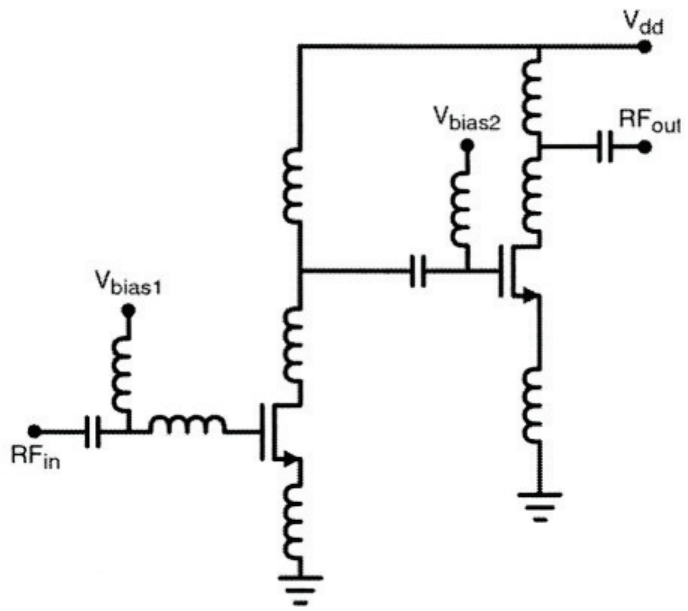


Figure 10.24: Two transistor LNA, designed for SOI. The passive components, in particular the inductors, benefit from a high resistivity substrate.

A single stage LNA design is shown in figure 10.25. This comprises a similar input configuration to the two stage structure shown above, with a cascode device in place of the second gain stage used in the previous example. Input inductor L_g is directly connected to the gate. Parasitic capacitances of the bond-pad and inductor impact operating frequency limit and noise figure, and must be considered in simulations. In addition, third-order intermodulation is observed as a result of non-linearity in the current-voltage characteristics.

Distortion sources in MOSFETs are transconductance non-linearity, voltage dependence of the drain junction to body, and output conductance non-linearity [10.17]. While transconductance non-linearity is common to circuits built on both SOI and Bulk, those on SOI can be designed to minimize the voltage-dependent drain capacitance however the "kink" effect is significant in DC output conductance non-linearity.

The cascode configuration increases output impedance and reduces the SOI MOS output conductance non-linearity [10.17]. Use of a high resistivity substrate for the LNA improves performance by increasing the inductor Q factor, and shifts the peak frequency of the Q factor up from just over 1GHz with 10 Ω cm material to over 2GHz with 1000 Ω-cm material.

Samsung Exhibit 1010, Page 161 of 204

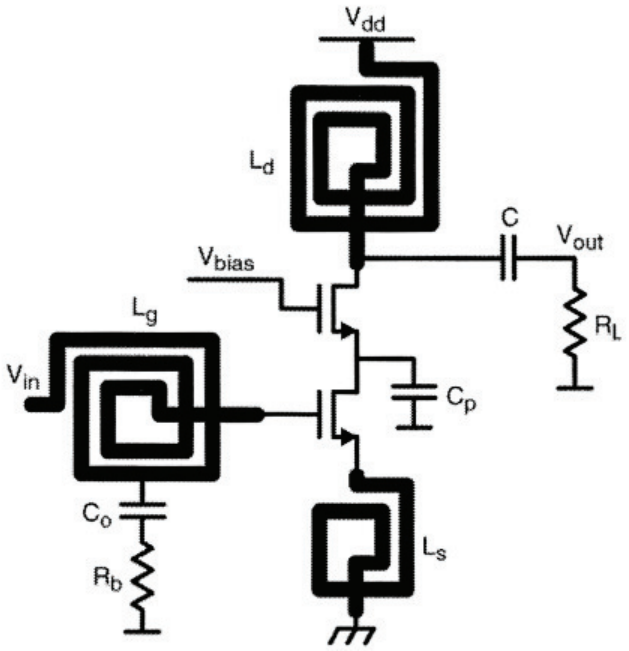


Figure 10.25: Radio Frequency Low Noise Amplifier, with cascoded output stage.

10.11.2 Mixers and Analog Multipliers

Analog multipliers combine or generate non-linear signals, such as multiplication, division, square, square root etc. They are useful as building blocks in a variety of circuits, including adaptive filters, function generators and wireless systems. They are particularly prone to mobility reduction effects and body effect [10.25]. Body effect mismatch is reduced in PD-SOI, since the NMOS body is not automatically tied to substrate, but can instead be tied to source, maintaining low offset between devices.

Gilbert Mixer

Most wireless systems use some variant of the familiar Gilbert mixer (figure 10.26)[10.26]. Mixers are among the highest power dissipation circuits in most wireless systems. However, for wireless systems, it is also a requirement to minimize power, since this allows reduced battery size, improved operating capability and lower standby current. It is also important to maximize the level of circuit integration for reduced cost and improved performance. CMOS on SOI is particularly suitable for helping achieve all of these requirements. For wireless systems, mixers are required on both the receiver, to convert the RF signal to lower frequencies, and on the transmitter, to mix low frequencies with the RF carrier. Frequently, the most important characteristics of mixers in wireless applications are high linearity, low noise and high gain.

Samsung Exhibit 1010, Page 162 of 204

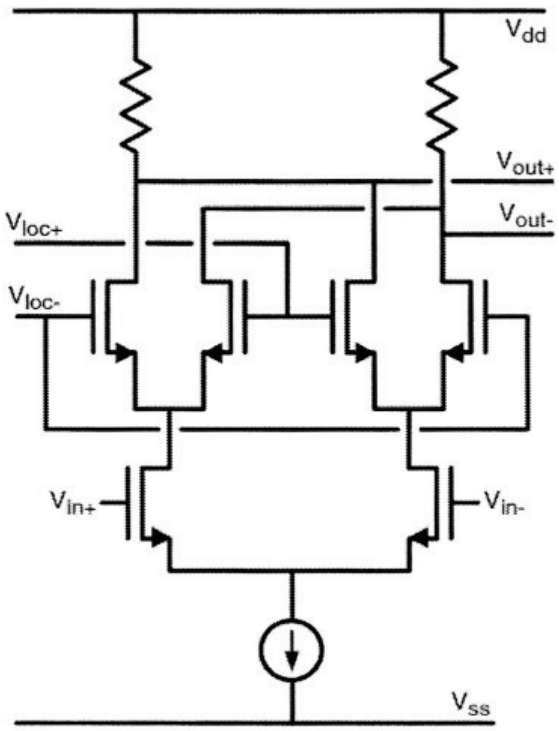


Figure 10.26: Schematic of a CMOS-based Gilbert mixer.

The conventional Gilbert mixer structure on PD-SOI has the drawback that local matching is usually inadequate, and that supply voltage headroom may be marginal for many low voltage SOI processes. SOI mixers benefit from reduced capacitance, aiding high frequency applications while reducing power and providing improvements in passive components.

The simple dual gate mixer shown in figure 10.27 will operate to 1V or less, and in SOI the low substrate parasitics result in high performance [10.27]. To operate at 1V, this scheme uses zero threshold voltage devices. If higher supply voltages can be tolerated, higher threshold voltages may be used. In figure 10.27, the lower device (M1) is the mixing device, and is biased in the linear region. The upper MOS device is biased in saturation and provides amplification. Careful biasing is required to avoid kink-region operation, where noise and non-linearity are increased.

10.11.3 Delay Locked Loop

Delay Locked Loop (DLL) designs are often used for frequency multiplication applications. This is achieved by taking advantage of an inherently low-jitter frequency reference (such as a crystal oscillator), and generating between each reference pulse a burst of evenly spaced edges. The bursts are adjusted in frequency to form a continuous higher frequency, with a higher long-term stability than possible without the reference signal.

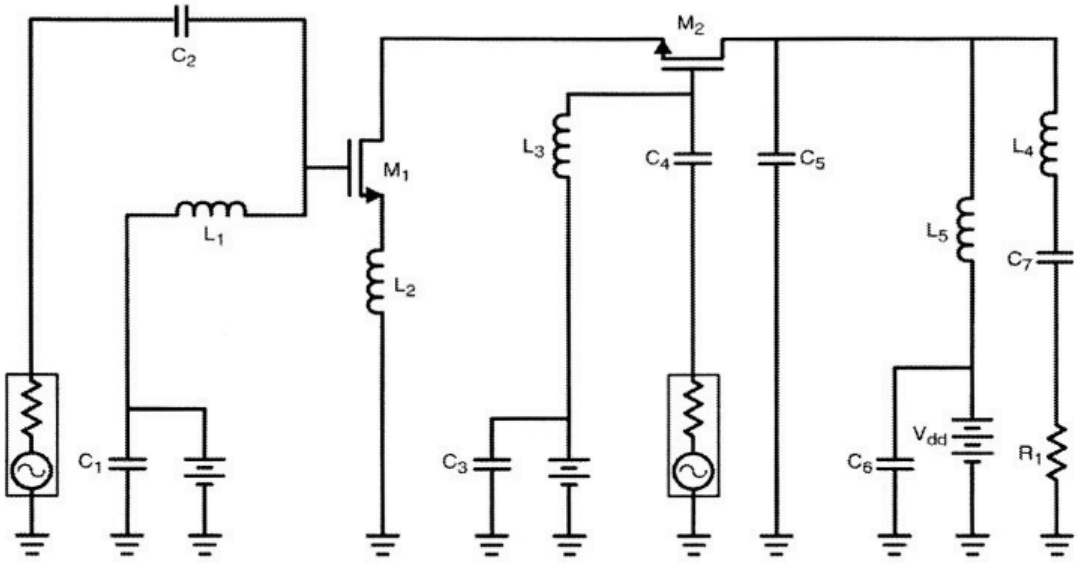


Figure 10.27: Two-transistor dual gate mixer, designed for a PD-SOI process, and operation at 1V.

To generate controlled, evenly spaced pulse edges a voltage controlled delay line is formed, using as its basis a voltage controlled ring oscillator that has been split to form a chain. A phase detector senses the phase shift between the input and output, generating an error signal, which is used to adjust the delay per stage through the chain (figure 10.28). DLL systems have better long-term jitter performance than PLL designs as timing error is reset with each reference pulse.

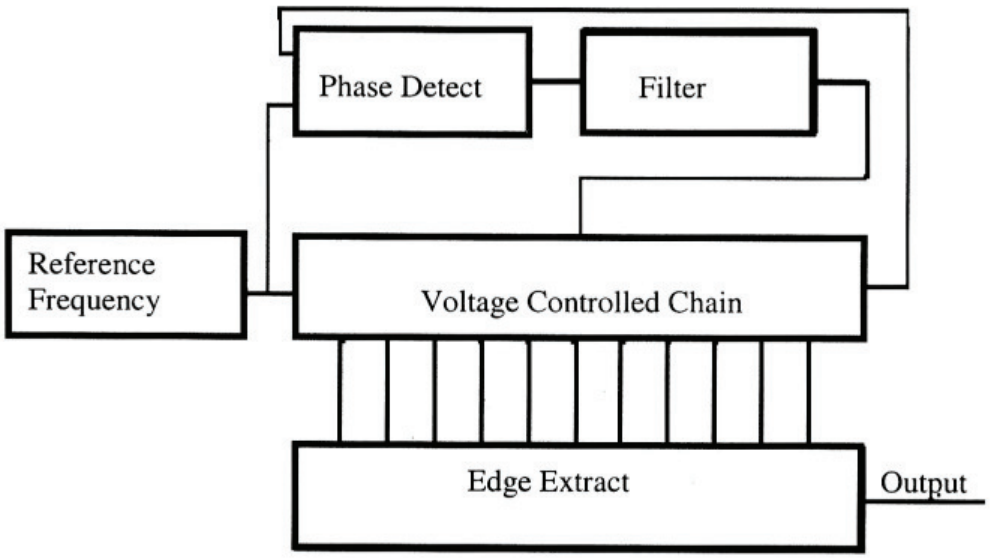


Figure 10.28: Typical Delay Locked Loop.

Samsung Exhibit 1010, Page 164 of 204

A DLL for graphics display applications has been compared for performance in bulk, PD-SOI and FD-SOI [10.28]. The FD version displays the shortest minimum delay and highest precision per stage, and bulk the longest minimum delay per stage. History effect of the SOI material did not cause a significant increase in jitter.

10.11.4 Phase Locked Loop

Phase Locked loop (PLL) systems are used extensively in wireless and communications systems particularly frequency synthesis and demodulation. The PLL consists of a filter and amplifier, with a phase detector comparing the input signal, and a frequency dependent signal derived from the output voltage (figure 10.29).

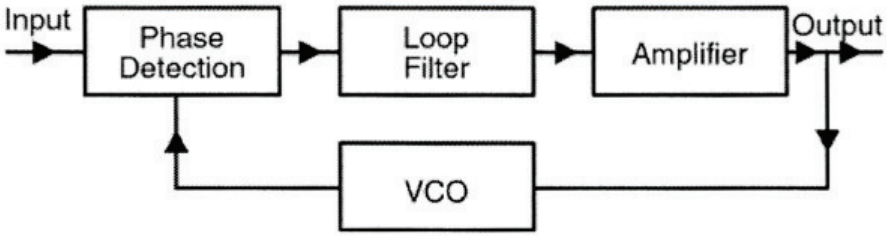


Figure 10.29: Typical Phase Locked Loop block diagram.

The reference and feedback are compared using a phase detector. The input of the loop filter and amplifier is an error signal from the phase detector. Synchronization is maintained as the output amplification completes the feedback loop through the VCO. The ideal steady state condition is a zero phase difference between the input and VCO output.

Various forms of jitter, or cycle differences, caused by noise or spurious signals limit PLL performance. Difference between successive periods causes cycle-to-cycle jitter. Phase jitter is related to modulation of successive pulses referenced to a continuous oscillator. Period jitter relates to the variation of period during non-successive periods. Random jitter is the result of noise components such as flicker noise or thermal noise and spurious signals. Additional device noise coupling from floating body structures, and spurious signals from the supply are critical issues to be addressed in SOI design. However, there is also a reduction of noise coupling through the substrate.

10.11.5 Phase Detector

The phase detector compares the phase of the reference signal to the feedback signal from the output, and generates a signal that is proportional

Samsung Exhibit 1010, Page 165 of 204

to the phase error. Digital phase detectors include edge-triggered flip-flops and exclusive OR gates. It is necessary to ensure that the phase detector accounts for the memory effect of PD-SOI. If the phase detect is operating in a stable state, any memory effect should also stabilize, however, this may take several milliseconds, especially at circuit power-up.

10.11.6 Loop Filter

The simplest form of filter used in phase lock loop systems is the passive analog type. This includes resistor-capacitor (RC) and inductor-capacitor (LC) filters. Most passive filters require some internal damping to prevent ringing following a frequency step. Many fully integrated filters have been of the RC type, due to the ease of construction and the low 'Q' factor associated with integrated inductors on bulk material. The potential for improved 'Q' with SOI shifts the point where it becomes economical or even possible to integrate the inductor. Off-chip filters are often of the LC type. On chip active analog filters are also widely used, and digital filter schemes are gaining popularity due to their capability for simple re-programmation for multi-standard wireless specifications. Hybrid filters, consisting of a reprogrammable digital filter and a relaxed specification for the analog filtering, may also be used.

10.11.7 Oscillators

Three types of oscillator in common use for VCO applications are the LC resonant circuit (for example the Colpitts oscillator), oscillators based on capacitive charging/discharging (often referred to as relaxation oscillators) and delay-based oscillators (such as the ring oscillator). A merged voltage-controlled oscillator and RF receiver have been demonstrated on the "silicon-on-anything" version of SOI [10.29].

Inductive resonant circuits such as the Colpitts or Clapp oscillator [figure 10.30] are favored in many applications due to their frequency stability. The circuit operating point is defined by the LCR resonant frequency. Inductive resonant circuits have proved difficult to integrate successfully in bulk material due to limitations of integrated inductor design. New techniques, applicable to SOI, have improved the on-chip inductor characteristics (chapter 3). These oscillators can be converted into VCOs by replacing the fixed capacitor with a varactor. Depending on circuit requirements, these can be optimized for linearity, Q and phase noise. Most varactors have a limited tuning range, unless several volts can be applied. One method to circumvent the tuning range limits, is to use several smaller tuning ranges with switchable varactors.

Samsung Exhibit 1010, Page 166 of 204

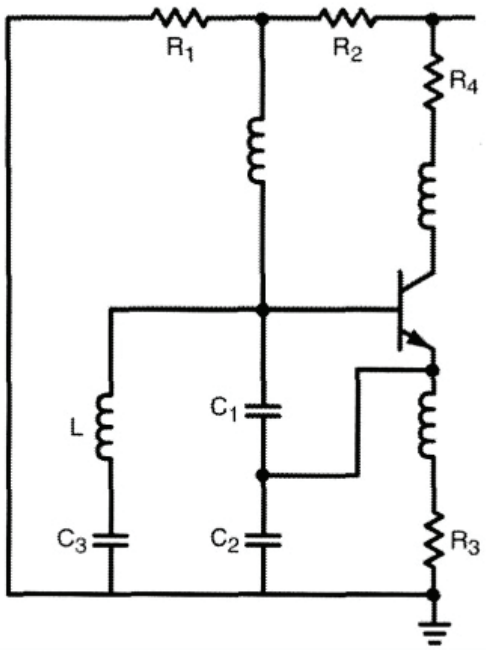


Figure 10.30: Typical Clapp Oscillator. This type of oscillator is more stable than ring or relaxation oscillators, a requirement in some wireless systems.

Relaxation oscillators (or multivibrators) are common oscillator designs in ICs. These operate through a continual charging and discharging of one or more capacitors between two voltage levels. A multivibrator is readily controllable using a voltage-controlled current source that supplies the charging and discharging currents (Figure 10.31). Basic relaxation oscillators tend to be sensitive to thermal effects, supply voltage variation, and phase noise. Design techniques such as temperature stabilized current supplies and controlled voltage thresholds aid in minimizing these effects.

The resistors in this circuit may be implemented as diffused components or polysilicon. For large resistances it is usual to use diffused resistors. In bulk these are fabricated straight into the substrate. Isolation from the substrate is achieved through a reverse biased diode junction. As reverse bias increases (voltage on the resistor increases) the resistance per unit length increases. This can lead to unexpectedly low switching threshold voltages. This is not a problem in SOI, since resistors are electrically isolated from the substrate.

Assume the capacitor is discharged, voltage at the top plate of the capacitor, V_c, is then close to ground. The output will then be close to V_{DD}. This permits charging of the capacitor through the controlled current source "I-charge". When the capacitor has charged above the level of V_{Low}, defined by a resistive divider, comprising R1, R2 and R3, the comparator output

Samsung Exhibit 1010, Page 167 of 204

switches to a level 1, thus inputs to the latch are both at a level '1'. When the capacitor has charged further, its potential reaches V_{high}. This forces comparator 1 to switch to level 0, changing the output state of the oscillator. The capacitor then begins to discharge. As soon as the capacitor voltage reduces below Vhigh the output of comparator 1 again switches high, without affecting the output voltage. When the capacitor voltage falls to Vlow, comparator 2 switches, changing the output state back to high. The cycle is repeated.

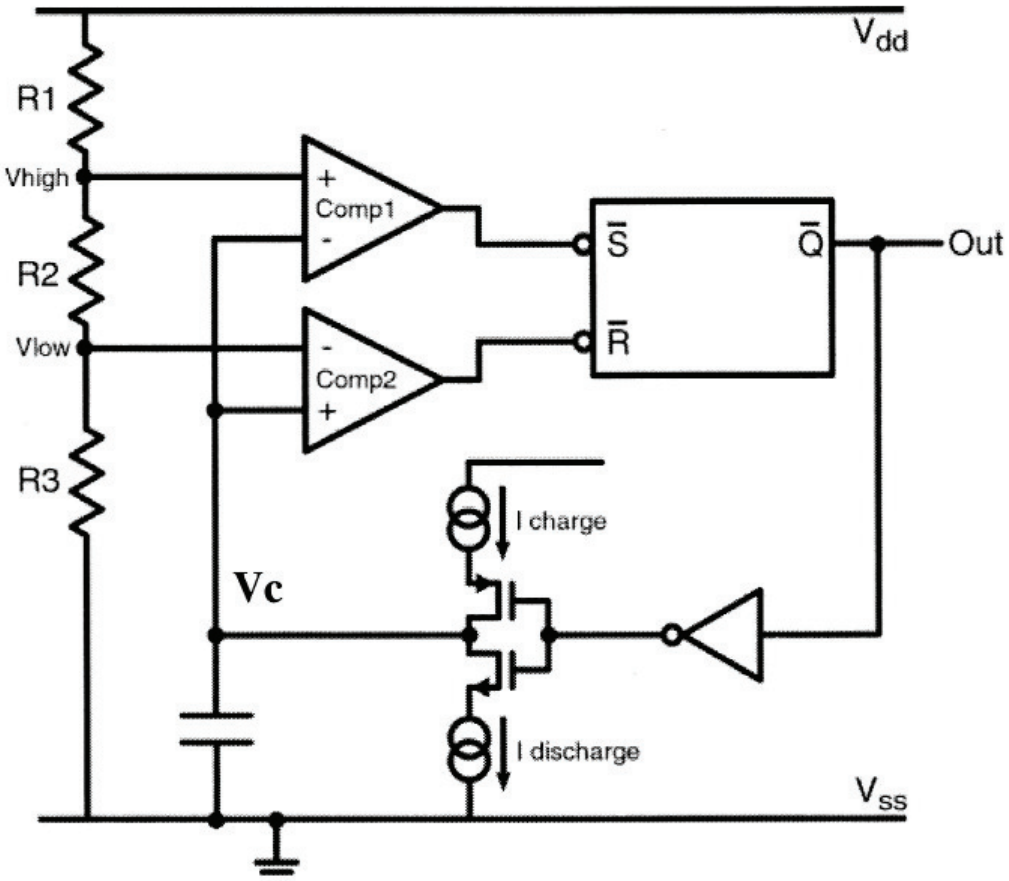


Figure 10.31: Example of a relaxation oscillator design.

There are a number of advantages and drawbacks to the use of this type of oscillator in SOI compared to bulk. When properly designed, the parasitic capacitances in SOI will be reduced. This improves accuracy and speed and furthermore reduces power if the charging capacitor size is reduced. Resistors diffused into the silicon (as opposed to polysilicon resistors) have more linear characteristics in SOI. When using this type of circuit, the same precautions should be taken in comparator design as would be taken for an operational amplifier design.

Samsung Exhibit 1010, Page 168 of 204

Ring oscillators are constructed with a series of gate or comparator delays. To create a VCO from this type of oscillator the delay cell has to be converted into a variable delay cell. This is readily achieved in the case of a comparator unit delay by adjusting the supply current, the supply current being approximately proportional to the inverse of gate delay. The circuit oscillates with a period equal to the cell delay times twice the number of delay stages. An example of this type of VCO is shown in figures 10.32 and 10.33. An advantage of most ring oscillator designs is that they can readily be adapted to provide quadrature outputs, useful in phase lock loop applications. The frequency is controlled through the I_{ss} current. This basic design has potential problems in PD-SOI due to floating body variability, and is most accurate as a body tied implementation.

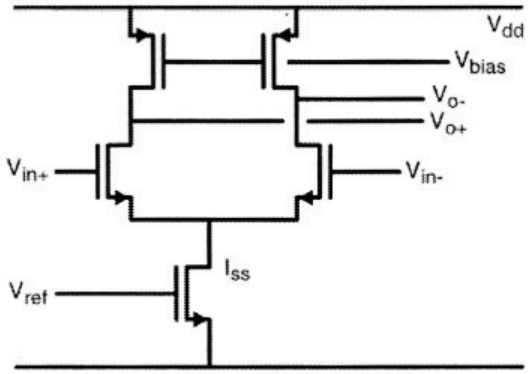


Figure 10.32: One stage of a ring oscillator type VCO. To alter frequency, I_{ss} is adjusted, which affects the delay timing.

Each stage is combined in a ring of many stages, as shown in figure 10.33. This represents a ring of 'n' oscillator. The structure has a common control for current, and a single inversion of the chain interconnect ensures oscillation (chapter 6).

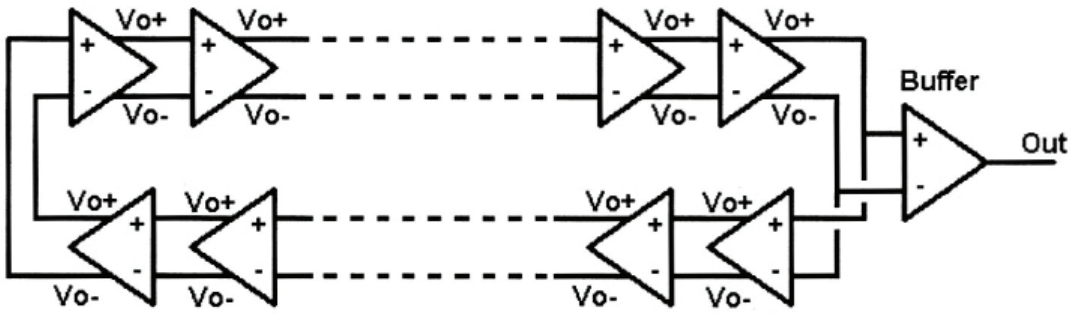


Figure 10.33: Block diagram of a voltage controlled ring oscillator. Each stage consists of the circuit in figure 10.32.

Samsung Exhibit 1010, Page 169 of 204

Self-heating in current controlled ring oscillators has been studied [10.16]. It has been found that no significant differences were observed between long and short chains. This indicates that self-heating is not important in this circuit.

10.12 Microwave Applications

Solid state microwave applications cover approximately the 1-30 GHz frequency range. At higher microwave frequencies circuit applications are fairly limited, typically being restricted to, for example, oscillators, amplifiers, frequency multipliers and mixers. Until recently many microwave amplifiers used GaAs as the semiconductor material. More recently Si implementations in both bulk and SOI have been developed [10.23].

Although currently only applicable to the lower frequencies of the microwave band, there are a number of advantages to SOI, including higher performance active components and improvements to passive components. In addition, some microwave devices are used in high radiation applications, where the potential to integrate microwave applications with rad-hard logic and memory is attractive.

Single FET mixers, similar in design to the circuits described elsewhere in this chapter, and other microwave circuits have been developed for board level and monolithic applications [10.30].

Silicon substrates used in SOI usually have relatively low resistivity (often around 20 ohm cm), and may vary substantially from wafer to wafer. When transmission lines are fabricated on silicon, variability in resistivity can cause a wide variation to the characteristic impedance of the transmission lines. The process dependency, and frequency dependent characteristics have to be considered in the designed. If variability of resistivity or absolute resistivity are issues, these can be minimized through additional process controls. Bonded wafer methods of SOI preparation have the advantage that the substrate can be tailored to specific applications. Silicon substrates can be chosen for optimum performance. In some cases alternative substrates (usually insulating quartz or glass) can be substituted.

Simulation procedures can be used which permit the determination of equivalent circuit parameters for small-signal MOS models at individual bias points. However, difficulties exist in extracting characteristics at higher frequencies. Channel charging delays can significantly impact the phase-margin of very high-frequency operational transconductance amplifier (OTA) designs, and can also affect input matching for low noise amplifiers.

Samsung Exhibit 1010, Page 170 of 204

Other high frequency circuits are also affected, such as mixers and high speed switching circuitry. With physical microwave models for SOI, circuitry can be optimized.

10.13 Voltage Regulation

Voltage regulators are very common circuits. They accept a somewhat variable DC input voltage and output a higher precision voltage that can be used as a power supply for other circuits. Two common types of voltage regulator are the "series" regulator and low-drop out (LDO) regulator.

10.13.1 Series Regulator

The output voltage of the series regulator is maintained by a power transistor (in this case nMOS) in series with the output. Figure 10.34 shows the components of a series regulator. A reference voltage is generated, typically using a bandgap reference. This reference voltage is fed to the non-inverting input of an operational amplifier, where it is compared with a divided sample of the output.

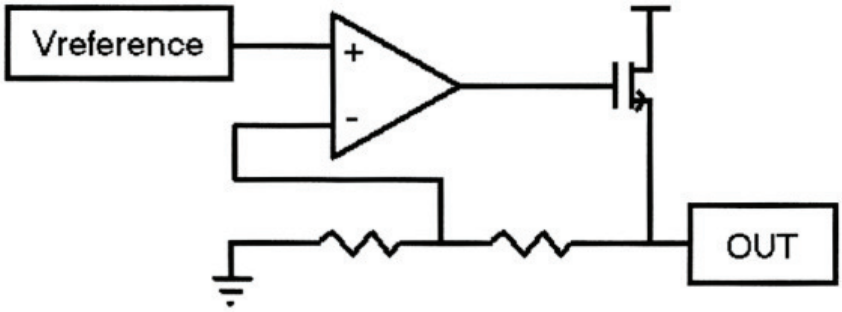


Figure 10.34: Schematic of a series voltage regulator.

Particular precautions required for the series regulator design as applied to PD-SOI processing have largely been covered in the sections on bandgap design and operational amplifiers. The power output transistor can be a floating body MOS device, but for highest precision a body tied device may be substituted.

10.13.2 LDO Regulator

The LDO regulator is a form of series regulator, but with the capability to retain regulation very close to the supply voltage. This type of regulator is much more difficult to stabilize than the series regulator, but is necessary in the compendium of low voltage circuits. The basic components of the LDO are similar to those of the series regulator, and are shown in figure 10.35. Bandgap, operational amplifier and voltage divider are usually the same or similar to those used for the series regulator. The controlling transistor is here a pMOS, which should be body-tied for optimum performance.

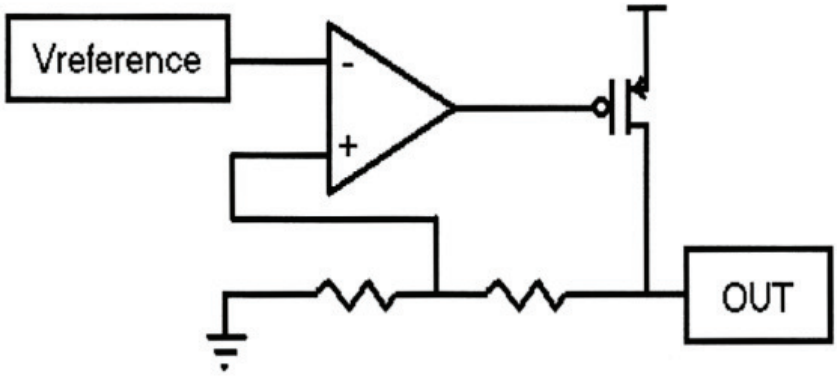


Figure 10.35: Schematic of a LDO regulator.

10.14 Analog to Digital Converters (ADC)

ADCs are vital components in converting real world inputs into digital signals that can be manipulated by digital signal processors or microprocessors. Requirements of the system dictate the type of ADC used, and is based on input voltage range, resolution, acquisition time, linearity, offset, power dissipation, conversion time and die area. The input voltage range refers to the maximum and minimum voltage to be digitized by the ADC. The ADC resolution is the number of steps into which the input range is divided, and is usually expressed as number of bits (n), where the number of steps is 2^n-1. Acquisition time is the time the input voltage must be sampled to get a reliable output voltage. To reduce this time when slow ADCs are being used, it is common to add a sample-and-hold circuit to the ADC input to freeze an otherwise varying analog voltage at the moment the sample is required. This voltage is held constant while the ADC digitizes the signal. Linearity is a measure of the equivalency of the input to output voltage. In practice each quantized ADC output step is offset from ideal, which leads to non-linearity in a plot of ADC output against input signal. Offset error affects all bits, and is a measure of the difference of the zero voltage input (or other specified input) to the output.

10.14.1 Successive Approximation ADC

A relatively slow but area efficient ADC uses the successive approximation topology (figure 10.36). The output of the comparator is a signal that is either high or low depending on the input voltage which can be higher or lower than the reference voltage from the digital to analog converter (DAC), described elsewhere in this chapter. Control logic increments or decrements the digital word, using one of numerous algorithms, and the digital output is converted to an analog signal by the DAC. Once the reference threshold of the DAC crosses the input voltage, the comparator output switches and the digital output can be read. This type of ADC can be free running, or can

Samsung Exhibit 1010, Page 172 of 204

perform a single conversion and then await a further signal from inputs to the control logic before repeating the sequence.

For SOI designs, no particular precautions are required for the digital portions of the circuitry, however care must be exercised for operational amplifier designs to ensure the comparator does not introduce offset into the converter. Refer to the section on DACs in this chapter.

Marginally improved performance can be expected with the successive approximation ADC built in SOI, compared to bulk, due to frequency improvements of the individual blocks. These improvements are mainly from reduced capacitance of the analog and digital structures, and higher drive strength of the digital control logic.

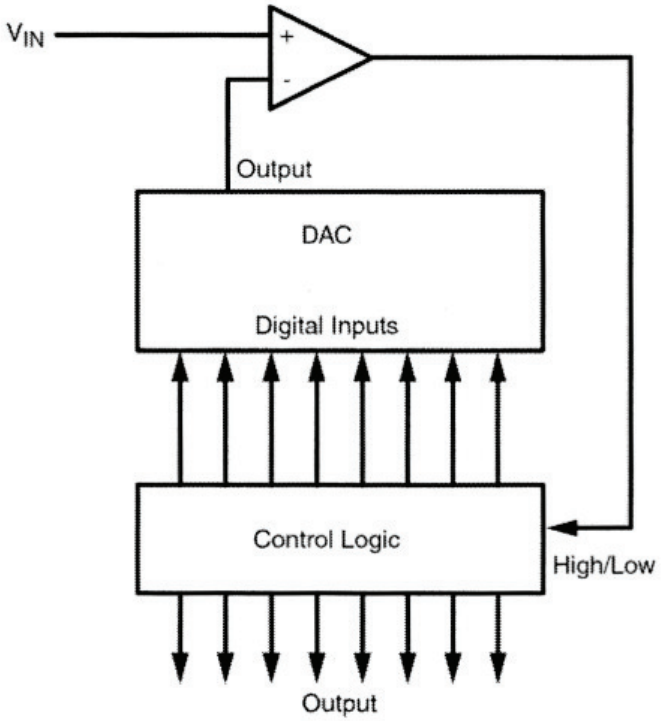


Figure 10.36: Successive Approximation ADC implementation.

10.14.2 Flash Converters

The flash (or Parallel-Encoding) ADC provides the fastest operation of all ADC architectures. However, for n-bit converters (n-1) comparators are required. This is expensive in terms of die area, the very large input capacitance of all the paralleled inputs and high supply power requirements. The large die area consumed can result in inaccuracies being introduced as a result of thermal mismatch and physical separation of the comparators. A resistor network sets discrete thresholds for the comparators. Decode logic

Samsung Exhibit 1010, Page 173 of 204

converts the comparator outputs to a usable digital sequence. Figure 10.37 shows a three bit flash implementation.

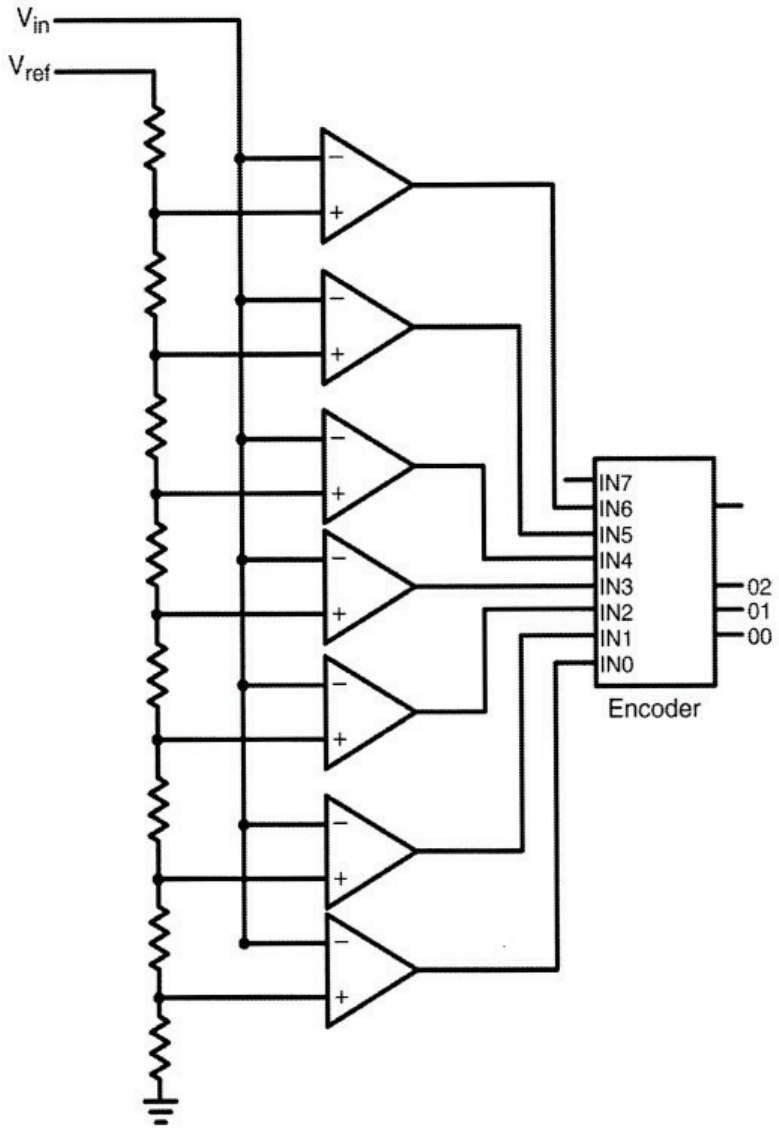


Figure 10.37: Implementation of a 3 bit flash analog to digital converter. This simplified diagram shows that the basic building blocks for the flash are comparators and digital logic.

A reference signal is applied to the resistive divider network. The outputs from the resistor ladder are the reference inputs for the comparators. When the input signal is higher than the reference the comparator output is low. When the input signal is lower than the reference the comparator output is high. All comparator outputs are fed to the encoding logic, which converts the signals into a digital output that can be used by the subsequent digital decode circuitry.

Samsung Exhibit 1010, Page 174 of 204

Comparative performance of designs for a flash ADC on bulk and PD-SOI, for the most part, favors PD-SOI. The resistor ladder can be built more accurately in SOI. The decoding logic is faster and smaller in SOI. In addition, comparators are faster (or alternatively can operate at lower power) in SOI. However, body ties or modified comparator design is required to equalize the body potential of the input pair. The simplest floating body comparators are prone to high and variable offsets which are unacceptable.

10.14.3 Pipelined ADCs

To minimize die area when high resolution and relatively high speed are required, pipelined architectures may be used. Figure 10.38 shows a typical multiple stage pipeline ADC architecture. Stages are typically scaled smaller at higher stage numbers, optimizing noise performance and power requirement.

Each stage quantizes the output from the previous stage into one or more bits using a flash ADC architecture. The quantized result is converted to an analog signal using a digital to analog converter and subtracted from the sampled signal. The resulting difference signal, which is smaller than the LSB of the stage is then amplified and is available for the next stage.

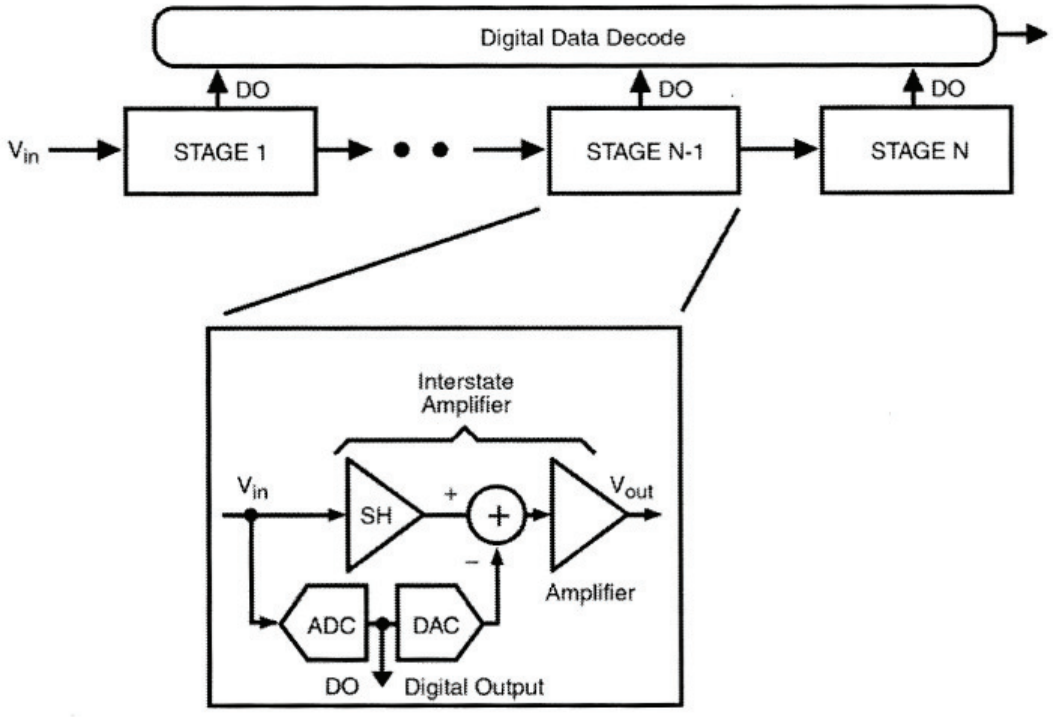


Figure 10.38: Pipelined architecture for an ADC. This is more efficient in terms of die area requirements than the Flash ADC architecture.

Samsung Exhibit 1010, Page 175 of 204

For PD-SOI operation of pipeline structures all precautions discussed in flash ADCs and DACs are applicable. It is particularly important to avoid errors, which will be amplified as the signal passes from stage to stage. Errors in the opamp and comparator thresholds can lead to errors in the difference signal, causing missing or spurious codes. Capacitor mismatch, an important source of gain error, is lower in SOI material than in bulk. Digital error correction techniques used for pipelined ADC architectures in bulk material are also applicable to pipelined architectures on SOI.

10.15 Digital-to-Analog Converters (DAC)

Accurate current sources and device mismatch minimization are critical in DAC design. In addition to the mismatch seen in bulk material, mismatch in SOI can cause thermal differences. The impact of localized heating on the design of DACs in SOI has been previously studied [10.16], where it was demonstrated that thermal behavior influenced linearity. However, it was also shown that this could be minimized to the point of being insignificant with careful design practice. A 10-bit DAC has been designed based on a PD-SOI technology. This uses the technique of biasing the operating region outside the kink region [10.31].

Most DACs are required to output a linear scale, with voltage or current weighted according to the binary value of the digital signal. Perhaps the simplest DAC in general use is based on a resistive ladder. Figure 10.39 shows the basic implementation of this configuration, which is termed the R-2R ladder DAC.

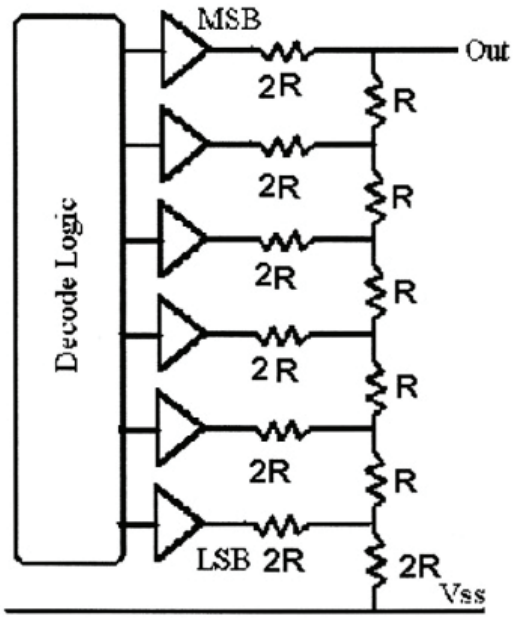


Figure 10.39: R-2R type DAC

The mode of operation of the circuit in figure 10.39 is as follows: The decode logic determines the output pattern to the ladder. If all decoded outputs are at logic level zero, then the output is at 0V. If the output is at a higher level, then one or more decode logic outputs is at a logic level 1. The output voltage from the ladder can be determined following an analysis of the currents through and voltages across the network.

This circuit benefits significantly from the use of SOI. The buffers can be smaller and decode logic is faster and smaller. Resistor area may be reduced for the same linearity and resistance. This leads to reduced capacitance and faster DAC operation. No particular precautions need be taken in the conversion of this structure to SOI from bulk unless the output is buffered using an op-amp.

Figure 10.40 shows an alternative configuration for a DAC. This is based on combining currents. This does not generally give a DAC output that swings rail to rail, as achieved with the DAC shown in figure 10.37, but it is more versatile in terms of the range of adjustment that can be made for different conditions such as supply voltage and thermal effects.

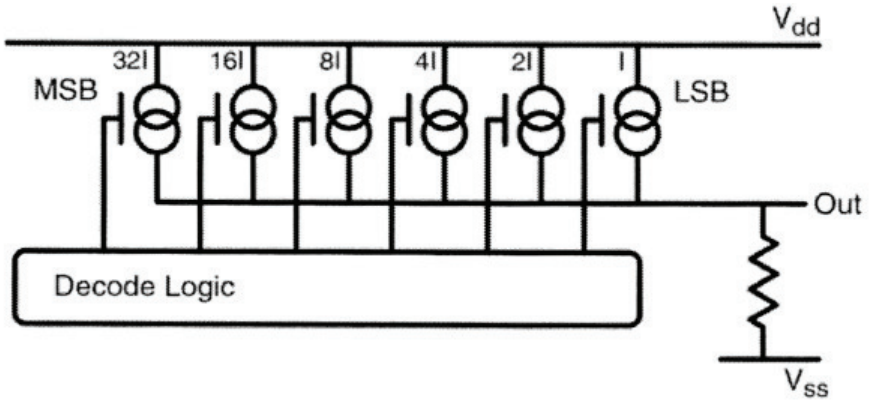


Figure 10.40: Binary weighted current type DAC

The mode of operation of the current scheme of DAC is straightforward. Binary weighted current sources are used to create a voltage across a resistor. These currents are matched to the characteristics of the resistor. The currents are compensated for temperature and possibly supply voltage. As previously discussed matching of resistors is easier in most cases for SOI material, but care must be taken in matching the current mirrors required for the current sources.

10.16 Sigma Delta Modulator

Sigma-Delta modulators are widely used in filters, phase-locked loops and as a method to convert between analog and digital circuitry, and are also

Samsung Exhibit 1010, Page 177 of 204

important in mobile communications applications. Basic operation of a sigma-delta modulator is as follows: The forward path consists of a filter and quantizer (figure 10.41). The low pass filter input is the difference between the input and feedback loop. Thus the average value of the filter output equals the average value of the input signal. The filter provides an analog representation of the digital output. The filter normally includes one or more operational amplifiers. The simplest way of dealing with a PD-SOI low pass filter is to make use of body ties, to avoid integration of any body-voltage-induced input offset. In addition the op-amps of the filter should be low-noise, again, using body ties keeps the body away from the higher noise kink region.

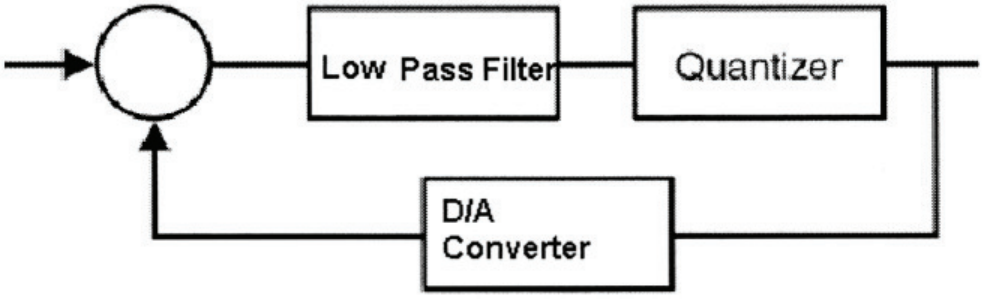


Figure 10.41: Block diagram for a sigma-delta modulator.

10.17 Interface between Digital and Analog Circuitry

An important area of circuit design that is frequently overlooked is the interface region between analog and digital circuitry. A common method to interface a signal between the two types of circuitry is the use of a level shifter. This is particularly appropriate when the logic operates at a different voltage to the analog circuitry. Such a situation is common with low voltage processes, where logic operates at a low voltage for power consumption reasons, but analog and interface circuitry has to operate at higher voltages. An example of interfacing to digital circuitry from an analog circuitry might be from a comparator output to a digital input. In this case an interface block such as figure 10.42, might be used. This converts the comparator output to a digital level signal. Circuit design for SOI processes remains similar to bulk, although fewer precautions need be observed for SOI material, due to the inherent PMOS tank isolation of SOI.

Some design and operating conditions may permit voltage V1 to be zero volts. An initial analysis of this might lead to the expectation that the output stage latch connected to V2 will maintain the same state as defined prior to the removal of the V1 supply. However, leakage effects do not guarantee this, and with the uncertainty of the leakage due to SOI body effects it is

Samsung Exhibit 1010, Page 178 of 204

advisable to use bypass circuitry to define the state in the event that voltage V1 falls below the threshold voltage of the V2 stage NMOS components.

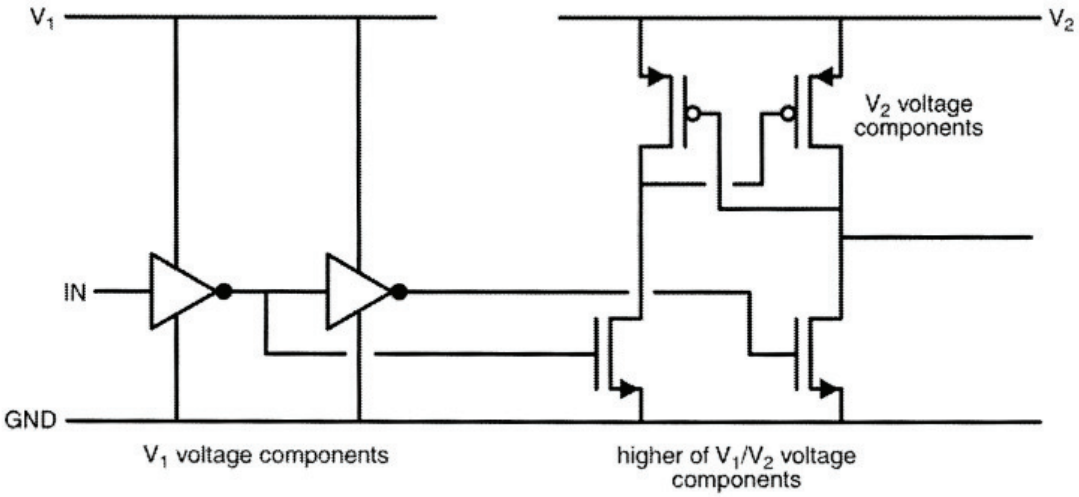


Figure 10.42: Example of a level shifting circuit used to interface between analog and digital circuitry, with different voltage supplies.

10.18 Power Amplifiers

Power amplifiers are used in many applications, often using DMOS (Double Diffused MOS) transistors. Power dissipation issues associated with DMOS and other high current density components have been discussed in chapter 3. High frequency integrated SOI power amplifiers have also been described [10.32]. Wireless power amplifier operates at 900MHz, and includes integrated MOS transistors, inductors and capacitors on a 1.5μm SOI BiMOS technology. The amplifier output stage is an LDMOS, in a class E configuration. The ability to integrate the RF power output onto SOI material improves the performance to cost ratio of the material.

10.19 Sensors and Actuators

Since the early 1990s a wide variety of integrated sensors and actuators have been developed. These range from Hall-effect sensors to Digital Light Processing technology. Most of these have been built on bulk silicon, but increasingly, a variety of Micro-mechanical (MEMS) devices, such as gyroscopes and accelerometers have been demonstrated in SOI. SOI provides the advantage of simple construction of electrically isolated, three-dimensional micro-mechanical structures, and enhances the variety, shape and layer thickness that can be fabricated.

Infrared sensors have experienced a recurring problem with sensitivity and precision due to high thermal dissipation through the silicon. The thermal

Samsung Exhibit 1010, Page 179 of 204

isolation afforded by surrounding oxide is expected to improve sensor sensitivity. In addition, the low capacitance to substrate should benefit thermal sensor performance.

SOI design of Hall Effect sensors has also been demonstrated for high temperature automotive applications [10.33]. To improve amplifier offset performance a bipolar chopper amplifier was used. The use of SOI enabled both elevated temperature and low leakage performance.

Samsung Exhibit 1010, Page 180 of 204

References

[10.1] M.R. Casu, et. al., "Comparative Analysis of PD-SOI Active Body-Biasing Circuits", 2000 IEEE International SOI Conference, Oct. 2000, pp. 94-95.

[10.2] 0. L. Neel & H. Haond, "Electrical transient study of negative resistance in SOI MOS transistors", Electron. Lett., vol. 26, no. 1, 1990, pp. 73-74.

[10.3] B. M. Tenbroek, et.al., "Self-heating effects in SOI MOSFET's and their measurement by small signal conductance techniques", IEEE Trans. Electron Devices, vol. 43, Dec. 1996, pp. 2240-2248.

[10.4] A. Marshall, "Beta Helper for Voltage and Current Reference Circuits" US patent number 5684394, November 4th, 1997

[10.5] P. R. Gray & R. G. Meyer, "Analysis and Design of Analog Integrated Circuits, third edition", Wiley, 1993, ISBN 0-471-57495-3.

[10.6] A. P. Brokaw, "A Simple Three-Terminal IC Bandgap Reference", IEEE Journal of Solid State Circuits, Vol SC-9, 1974, pp. 388-394.

[10.7] A. Marshall, et. al., "Compensation for low gain bipolar transistors in voltage and current reference circuits", United States Patent #5,349,286, September 20, 1994

[10.8] R.A. Blauschild, et. al., "A New NMOS Temperature-Stable Voltage Reference", IEEE Journal of Solid-State Circuits, Vol. SC-13, No. 6, December 1978, pp. 767-773.

[10.9] C. Eisenhut & J. W. Klein, "SIMOX Voltage References for Applications up to 275°C using the Threshold Difference Principle", Proceedings 1997 IEEE International SOI Conference, Oct 1997, pp. 110-1.

[10.10] A Nève, et. al., "Smart Card Circuits in SOI Technology", 2000 IEEE International SOI Conference, Oct. 2000, pp.48-49.

[10.11] J.B. Kuang, et. al., "Dynamic Body Charge Modulation for Sense Amplifiers in Partially Depleted SOI Technology", IEEE Journal of Solid-State Circuits, Vol. 36, No. 4, April 2001, pp. 597-604.

[10.12] J-P. Eggermont, et. al., "Potential and Modeling of 1μm SOI CMOS Operational Transconductance Amplifiers for Applications up to 1 Ghz" IEEE Journal of Solid State Circuits, Vol. 33, No. 4, April 1998, pp 640-643.

[10.13] D. Flandre, et.al., "Fully-depleted SOI CMOS technology for low-voltage low-power digital/analog/microwave circuits", Analog Integrated Circuits and Signal Processing. New York: Kluwer, 1998.

[10.14] A. Vandooren, et. al., "Performance of Irradiated Gate-All-Around SOI MOS OTA Amplifiers" Proceedings 1997 IEEE International SOI Conference, Oct 1997, p62-3.

[10.15] P. Francis, et. al., "Radiation-hard design for SOI MOS inverters", IEEE Transactions on Nuclear Science, Volume 41, Issue 2 , April 1994, pp. 402-407.

[10.16] S. H. Voldman, "The State of the Art of Electrostatic Discharge Protection: Physics, Technology, Circuits, Design, Simulation, and Scaling", IEEE Journal of Solid State Circuits, Vol 34, No. 9, Sept. 1999, pp. 1272-1282.

[10.17] A. O. Adan, et. al., "Linearity and Low-Noise Performance of SOI MOSFETs for RF Applications ", 2000 IEEE International SOI Conference, Oct. 2000, pp.30-31.

[10.18] M. Kumar, et.al. "A 900MHz SOI Fully Integrated RF Power Amplifier for Wireless Transceivers" ISSCC 2000, pp.382-3.

[10.19] D. Buss, "Device Issues in the Integration of Analog/RF Functions in Deep Submicron Digital CMOS", ISSCC 2000 (short course) ISBN 0-7803-6241-1

[10.20] J. P. Colinge, et. al., "A low-voltage, low-power microwave SOI MOSFET", IEEE International SOI Conference Proceedings, Oct. 1996, pp. 128-9.

[10.21] S. V. Kishore, et. al., "A SOI-BiCMOS RF-transmitter for personal digital cellular communication (PDC)" Symposium on VLSI Circuits, 2000. pp. 62-65.

[10.22] C. F. Edwards, et. al., "A Multibit Modulator in Floating-Body SOS/SOI CMOS for Extreme Radiation Environments", IEEE Journal of Solid State Circuits, Vol. 34, No. 7, July 1999, pp. 937-948.

[10.23] R. Kokozinski, et. al., "Microwave wideband in bulk-CMOS and CMOS/SIMOX technologies", Proc. IEEE ISSCC Conf., San-Francisco, CA, Feb. 1995, pp. 188-189.

[10.24] H. Jin & C. A. T. Salama, "A I-V, 1.9-GHz CDMA, CMOS on SOI, Low Noise Amplifier", 2000 IEEE International SOI Conference, Oct. 2000, pp. 102-103.

[10.25] E. Ibaragi, et. al., "A CMOS Analog Multiplier Free from Mobility Reduction and Body Effect", IEICE Transactions Fundamentals, Vol. E82-A, No. 2, Feb. 1999, pp. 327-334.

[10.26] B. Gilbert, "A Precise Four-Quadrant Multiplier with Subnanosecond Response", IEEE Journal of Solid State Circuits, Vol. SC-3, Dec 1968, pp. 365-373.

[10.27] S. Ye & C. A. T. Salama, "A 1 V, 1.9 GHz, Low Distortion Dual-Gate CMOS on SOI Mixer", 2000 IEEE International SOI Conference, Oct. 2000, pp. 104-5.

[10.28] P. Delatte, et. al., "Comparison of 0.25 μm Bulk, PD and FD SOI CMOS implementations of a Low-Voltage Low-Power Programmable DLL for Linear Delay Generation", 2000 IEEE International SOI Conference, Oct. 2000, pp. 92-93.

[10.29] R. Dekker, et. al., "An Ultra Low-Power RF bipolar technology on Glass" IEEE International Electron Devices Meeting, 1997, pp. 921-923.

[10.30] G. D. Vendelin et.al., "Microwave Circuit Design Using Linear and Nonlinear Techniques" Wiley Interscience 1990, ISBN 0-471-58060-0

[10.31] D. Chang, et. al., "Kink-Free Analog Circuit Design with Floating-Body NFD/SOI CMOS: A Current-Steering D-A Converter", Proceedings 1997 IEEE International SOI Conference, Oct. 1997, pp. 158-9.

[10.32] Y. Tan et. al., "A 900 MHz Fully Integrated SOI Power Amplifier of Single-Chip Wireless Transceiver Applications", IEEE Journal of Solid-State Circuits, Vol. 35, No. 10, October 2000, pp. 1481 – 1486.

[10.33] N. Kordas et.al., "An SOI 0.6mV Offset Temperature-Compensated Hall Sensor Readout IC for Automotive Applications up to 200 degrees C" ISSCC 1999, pp. 134-5.

Samsung Exhibit 1010, Page 184 of 204

Chapter 11: Global Design Issues

11.1 Introduction to Global Design Issues

Some issues of IC design are common to multiple types of design, rather than as purely analog, digital or memory. In this chapter we discuss questions related to SOI that span individual design disciplines, including temperature effects, clock distribution, and parasitic resistance and capacitance.

11.1.1 Cell Libraries

Attempts to use a cell library modified from a bulk library, for SOI designs has proven to be inefficient, since it does not account for all the performance enhancements resulting from floating body effects. As a result, the modified bulk library has to assume worst case delays.

To make full use of the benefits of SOI designs with floating body and/or dynamic body contacts require detailed circuit characterization. This is a design resource issue rather than a fundamental roadblock, and should be given priority for optimum performance simulations.

11.1.2 Clock Distribution

Clock distribution and skew / jitter minimization have been challenges in high performance designs. In floating body SOI configuration, uncertainty of the floating body potential and hysteresis effect translates into clock skew and jitter, degrading performance. It is difficult to design the clock distribution tree to balance out these effects, thus body contacts should be considered in critical paths.

11.1.3 Decoupling Capacitance and Series Resistance in SOI

SOI material has significantly reduced on-chip decoupling capacitance. This can lead to increased supply bounce. In bulk material, about 50% of the decoupling capacitance is from the junction to substrate and well to substrate capacitances.

In SOI, with faster circuit speed and absence of the built-in decoupling capacitance, supply and ground bounce are more severe. Thus decoupling capacitance must be specifically added, and distributed around the chip. However, although more severe, the isolated nature of the MOS devices on SOI often reduces susceptibility to supply bounce.

11.1.4 High Temperature Operation

Circuits operate at much higher temperatures using SOI material than possible using bulk material. SOI devices in general, and FD-SOI devices in particular have leakage currents two to three orders of magnitude lower than bulk, particularly at elevated temperatures. Due to lower forward voltage drop of diodes at high temperatures, typical bulk silicon processes display reduced immunity to noise, and an increased tendency to latch-up. SOI circuit design avoids leakage to substrate including leakage through the PMOS tank.

Figure 11.1 shows leakage paths for a NAND in both bulk and SOI. Neglecting MOS gate leakage (which, at high temperatures, is insignificant compared to drain-source leakage) overall leakage is defined by the lowest leakage component.

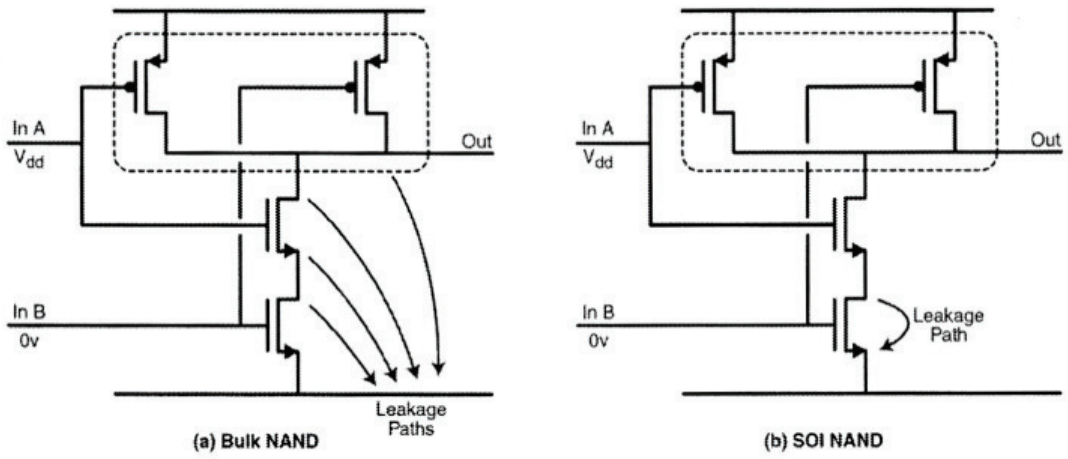


Figure 11.1: Leakage paths associated with a NAND (a) in bulk silicon, and (b) in SOI material, showing leakage path through the off-state SOI device, and reverse biased diodes, including the PMOS tank in bulk material.

Samsung Exhibit 1010, Page 186 of 204

For most applications PD-SOI can operate to about 250°C [11.1], while bulk is marginal even at 200°C [11.2]. However, very high temperature systems often benefit from the use of fully-depleted silicon, when operation is possible up to 300°C or higher [11.1, 11.3].

11.1.5 Gate Leakage

MOS transistor gate length has shrunk with process technology improvements. To maintain performance at lower voltages gate oxide thickness has also been forced to reduce [11.4]. Gate leakage is a significant proportion of the total leakage, especially at lower temperatures. Gate leakages can affect operation in memory cells and analog circuits even in bulk material. In circuits built on PD-SOI material gate tunneling modifies the history effect [11.4]. The gate leakage component can be included in some transistor models, such as BSIM4.

11.2 Noise Immunity

Noise issues are similar in bulk and SOI. Noise effects, however are aggravated in PD-SOI due to the floating body, and faster circuit switching. The most common types of noise are due to crosstalk, simultaneous switching, delay and logic noise. Synchronous noise may occur at the clock edges when latches are triggered. When a noise event occurs without any timing relation, this is termed asynchronous noise. While absolute noise may be higher, the isolated nature of many components means a higher level of noise can be tolerated, particularly in static logic applications.

11.2.1 Circuit Noise

Removal of junction isolation in favor of dielectric isolation relieves the designer of certain thyristor latchup issues related to MOS designs built on bulk processes. Thyristor latchup is of particular concern in power integrated circuits, automotive applications and other noisy environments. Design for automotive applications often includes a variety of tests to verify latchup immunity. This testing is administered to the chip as part of qualification and ongoing testing [11.5]. In addition, switch-mode regulators, and drivers for motors are specifically prone to latchup from inductive spiking [11.6]. Many high power chips include additional highly doped buried layers and deep high concentration diffusions to minimize such effects [11.6].

The replacement of junction isolation with dielectric isolation would, therefore appear to be beneficial. However junction isolated parts have one distinct advantage that SOI lacks, that of significant built-in capacitance from supply to ground, through the PMOS body contact to substrate (figure 11.2). Usually the PMOS body is created using an N-type tank diffusion into

Samsung Exhibit 1010, Page 187 of 204

a P-type substrate. The substrate is electrically connected to ground, as is the NMOS body contact. The N-well diffused into the substrate creates a reverse biased diode between supply and ground. This diode can be a quite large proportion of the chip area, and can add several tens of picofarads of capacitance between supply and ground. This helps minimize voltage switching transients caused by resistive and inductive wire bonds within the package.

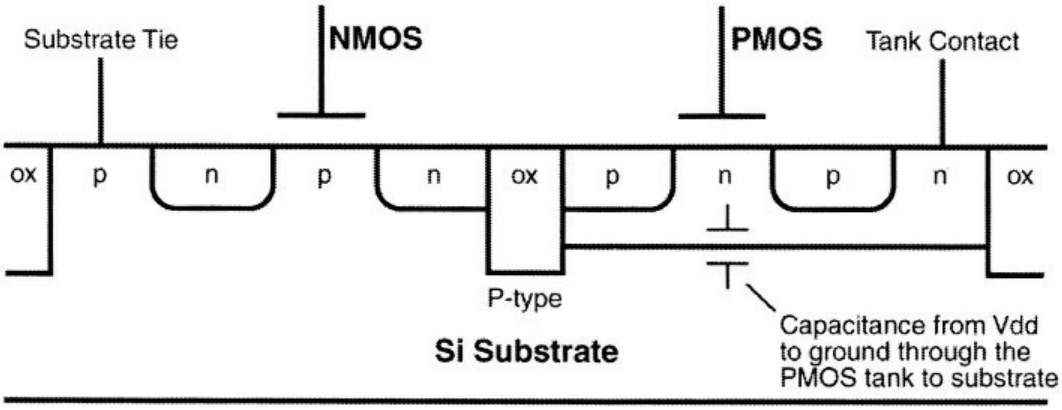


Figure 11.2: Demonstration of the junction capacitance that is commonplace in bulk IC designs, but absent in SOI. The cross-section shown is the capacitance in bulk material that is dielectric isolated. Capacitance in bulk material that is junction isolated is similar.

11.2.2 Capacitive Coupling Noise

Adjacent metal leads are capacitively coupled. The current coupling is given by:

$$I=C*dV/dT$$

where C is the capacitance between the wires and dV/dT the rate of change of voltage between the two wires.

Voltage switching of a wire induces a pulse on the adjacent signal. Crosstalk noise is caused by the coupling of the two signals. Memory arrays are susceptible to this type of noise. If the bit is maintaining a HIGH logic level, and the complementary bit switches LOW, the bit line develops a tendency to pull LOW due to coupling from the adjacent bitlines. Many methods have been used to reduce bit line to bit line coupling, including the use of twist lines forming pairs of signals. In general, however, the effects of capacitive coupling between adjacent metal traces may be more severe in SOI due to

Samsung Exhibit 1010, Page 188 of 204

the reduction in source and drain capacitance, and possible reductions in the interconnect to substrate capacitance.

11.2.3 Delay Noise

Delay noise refers to crosstalk coupling generated by one signal such that the adjacent coupling signal swing in either the same direction or in opposing directions. If both signals swing in the same direction, capacitive coupling speeds up the signal. If the signals switch in opposing directions capacitive couplings slows down the signal. This type of delay noise can therefore cause a race condition, as signals arrive sooner or later than expected, potentially causing chip failures.

11.2.4 Logic Noise

When a neighbouring signal pulls down a signal that is supposed to maintain a steady voltage functional failures may result. A memory circuit may have parallel bit lines. If one of two adjacent bit lines switches from HIGH to LOW, if the coupling capacitance is too high, then the bit line trying to maintain a HIGH level will tend to be pulled lower, possibly reading corrupted data out to the sense amplifiers. Dynamic and pass gates are more susceptible to logic noise fails than static logic circuits.

11.2.5 Decoupling Capacitors

In the absence of the supply-ground junction capacitance of bulk designs, SOI designers have explored different methods for achieving immunity from transient switching effects. One option is the addition of thin-oxide decoupling capacitors [11.7]. These have been used to supply surges in current from the chip, bypassing series impedance with the power pads. Integrated circuits that are substantially digital in nature can use distributed thin-oxide capacitors [11.8], to achieve a measure of noise immunity. In most cases it is adequate to add decoupling capacitors in all available space.

11.3 Latchup Immunity

Figure 11.3 shows the potential for latchup of conventional CMOS, through turning ON the intrinsic thyristor [11.1]. Latchup can occur as a result of the transient switch triggering a PNPN (thyristor or SCR) structure between supply and ground. The PMOS tank may provide enough resistance (R1) that the N-well tank voltage is at V_{be} below supply. This turns on the parasitic PNP (Q2) from Vdd to substrate. Current flowing through the substrate causes a voltage gradient, which can turn ON the NPN structure comprising the N-well, NMOS source and p-substrate. Careful layout eliminates this possibility, but clearly these parasitics cannot activate in SOI, where no direct path exists to cause a thyristor latch. It is still possible to

Samsung Exhibit 1010, Page 189 of 204

create a thyristor action in SOI, leading to uncontrolled current and/or circuit damage due to extremes in current or excessive thermal dissipation, however, it is much more difficult, and must be part of the circuit design (whether intented or not).

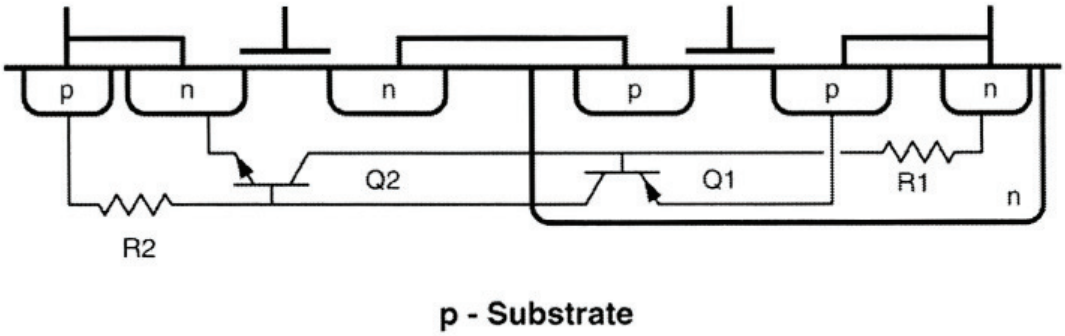


Figure 11.3: Cross sectional view of a bulk layout that can result in latchup. If resistances are not kept low through careful layout, the simple bulk CMOS inverter gate structure can be the source of a thyristor action. Resistance shown is formed between the Vdd or ground connection and the region that acts as a bipolar base.

Figure 11.4 shows the simplified electrical schematic of the latchup path of figure 11.3. To attain latchup of this circuit the overall gain of the circuit must be greater than unity. Process changes can be implemented to reduce the gains of transistors Q1 and Q2. Layout affects all components.

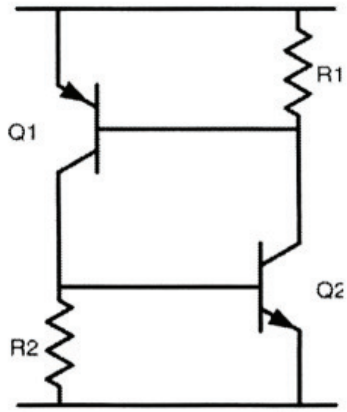


Figure 11.4: Electrical representation of the thyristor capable of causing latchup that is extractable from conventional bulk CMOS. The resistances and transistors are distributed, and as a result great care must be taken in positioning of body and tank ties, to keep the thyristor resistances low. This gives a desirable high hold current. (Note that the transistor and resistor identifiers correspond to the same devices numbers in figure 11.3)

Samsung Exhibit 1010, Page 190 of 204

The latchup immunity of SOI is a significant benefit to certain applications. In principle, however, PD SOI can still provide a multi-device latchup path, even though parasitic bipolars to substrate are absent. Latchup in SOI is possible where body tie structures are utilized [11.9]. Figure 11.5 shows how the use of body ties can create a thyristor function from the bipolar structure that is a parasitic of the MOS device.

Figure 11.5(a) is electrically equivalent to figure 11.5(b), and may represent two different ways to lay out the circuit. In the case of figure 11.5(b), with input LOW, the inverter output is HIGH, thus the PMOS output driver is off, and the NMOS body driver is also off. The NMOS output driver is on. Thus point 'C' is a low resistance to ground. If the body tie between the NMOS body driver and node C (shown as lead "nBres") is resistive, a latchable thyristor structure can be created. In most cases this structure would be far more robust against thyristor latchup than its bulk counterpart, but in the presence of certain transients on the output latchup cannot automatically be ruled out.

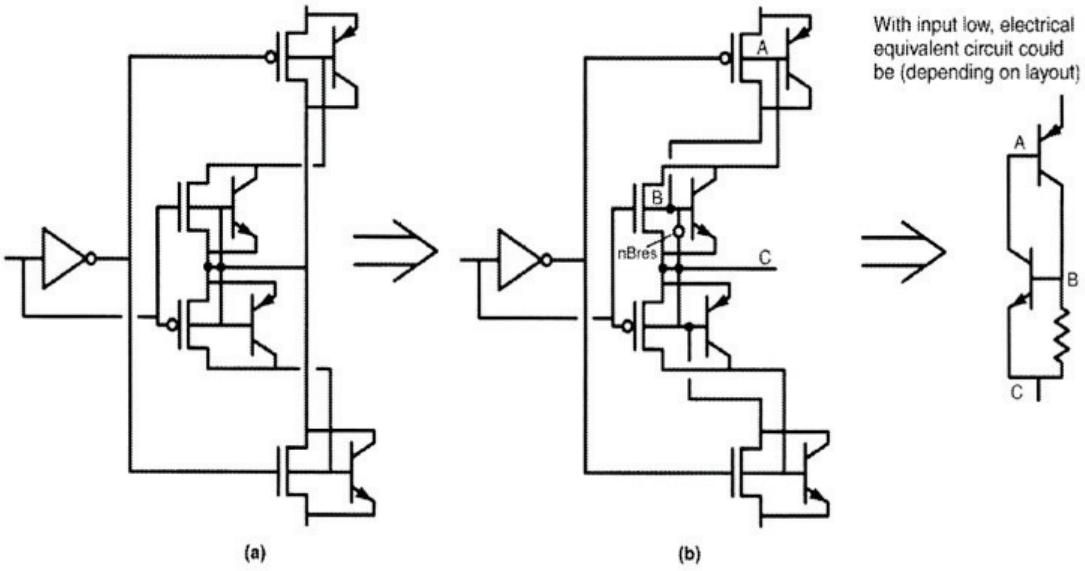


Figure 11.5: Demonstration of how a body tied PD-SOI structure can be prone to a thyristor type latchup, if layout is not carefully considered In this case when the input is low, the output 'C' would also be low. This turns off the PMOS output device and the NMOS body biasing device, resulting in a thyristor structure between supply and the output.

Latch-up can even occur in single SOI transistor if carrier generation due to impact ionization is higher than the source recombination (typically at high Vds) [11.10, 11.11].

Samsung Exhibit 1010, Page 191 of 204

11.4 Self Heating

The higher thermal resistance of SOI compared to bulk material is often not a problem, but care should be taken to ensure matched components are not at different temperatures, or that a high temperature element is not adjacent to temperature sensitive circuitry. Self heating is a problem even in some circuit designs on bulk material, and techniques have been developed to improve heat removal from the active silicon. There are various options for circumventing poor thermal characteristics. Perhaps the simplest and least costly is the use of metal layers above the heat generating component as a lateral heat spreader. Heat spreading can perform two functions. It can be used either to spread heat for dissipation outside the device area, or to spread heat to adjacent components that are required to maintain a similar temperature [11.1]. Another technique uses the heat-dissipating properties of bump technology [11.12, 11.13]. Bump technology combined with flip-chip packaging can be as efficient in removing heat from a package as conventional schemes. Much of the heat passes through the bumps (usually gold or solder plated copper), and through the electrically conducting traces on the substrate, or through the substrate itself. Figure 11.6 shows copper bump flip chip technology on a power IC.

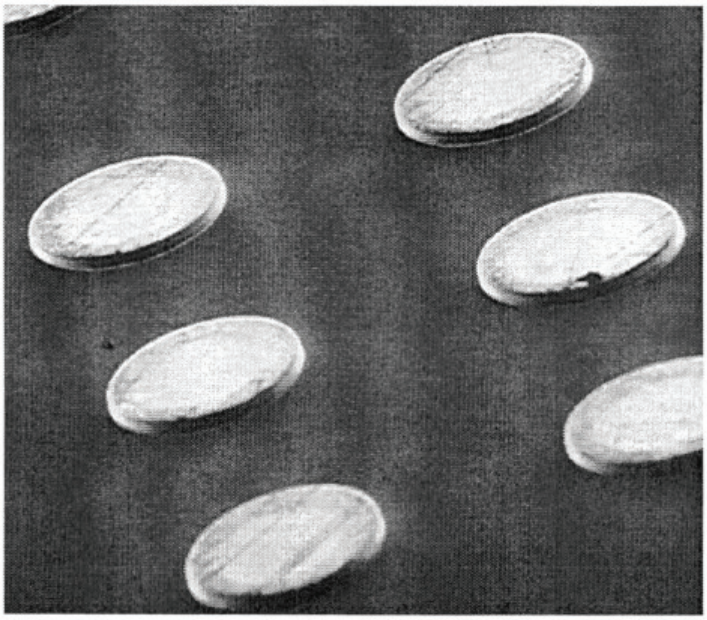


Figure 11.6: Photograph of copper bumps on a high thermal dissipation copper bump technology used for flip-chip packaging.

Figure 11.7 shows how a bumped IC mounts on to a flip-chip package. The bumps act as a low thermal resistance path to the leadframe. In many cases the ground leads of the package are positioned for maximized heat transfer.

Samsung Exhibit 1010, Page 192 of 204

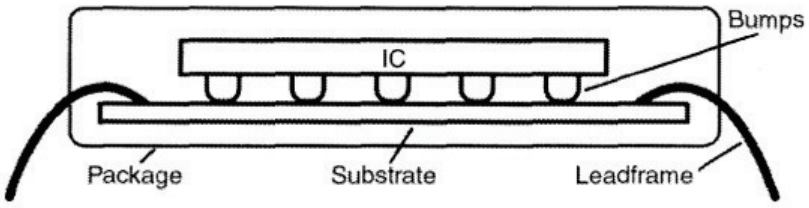


Figure 11.7: Improvement to thermal dissipation issues by the use of bump technology. The substrate is capable of high thermal dissipation, and contains patterned copper to connect to the leadframe.

A further development combines flip chip dissipation capabilities with that of conventional heat sink (Figure 11.8), enabling thermal dissipation from both sides of the silicon [11.14]. While not as effective as applying the same heat sink to bulk material, it improves the capabilities to levels adequate for most designs.

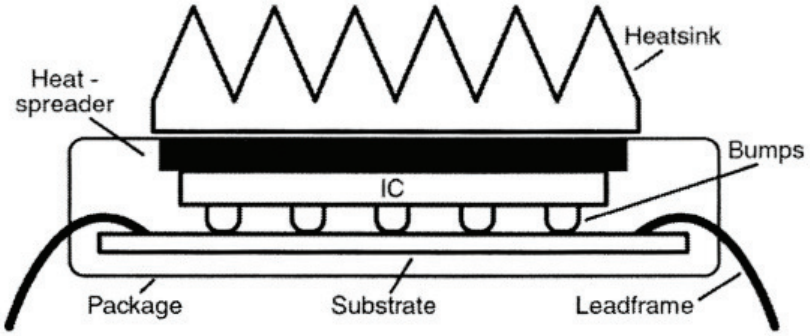


Figure 11.8: Package that permits heat removal from both sides of the silicon. This works by the use of bump technology to remove heat from the IC surface, and a heat spreader with heatsink to remove heat from the non-circuitry side of the chip.

11.5 Electrostatic Discharge (ESD)

On-chip ESD protection is standard on practically all integrated circuits. This is incorporated to improve reliability and yield. The three major ESD test methods are Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM). The HBM simulates the action of a static discharge from a human body to ground. It uses a charged 100pF capacitor discharging through a 1500Ω resistor. The MM simulates static discharge from a machine to ground. It uses a charged 200pF capacitor discharging through a resistance of less than 1Ω. The CDM simulates charging and discharging events within production equipment. CDM is tested by charging an IC, then discharging through the package leads.

Samsung Exhibit 1010, Page 193 of 204

Damage due to ESD is usually thermal in nature although oxide breakdown may occur if the protection clamps are not properly designed. Therefore, typical protection design requires consideration of both the current path that can cause thermal damage and the subsequent voltage drop to avoid gate oxide damage. ESD protection elements have to dissipate currents that are considered high by the standards of operation of the IC, without failure. ESD circuits on SOI have the disadvantage that the oxide does not allow rapid thermal dissipation of heat generated in the element. Electrical and thermal models are routinely used to develop ESD circuits, and these have been modified for use with SOI [11.15, 11.16]. Studies indicate that the SOI diode, when compared with a bulk diode, has reduced junction area and is thermally isolated from the substrate heat sink resulting in significant self heating.

ESD protection networks and simulation have had to be modified for SOI applications. It was originally thought that ESD protection for SOI would be more difficult than for bulk. In part this was due to reduced capacitances and the fact that the substrate was no-longer available as an integral part of the ESD protection scheme. It has been demonstrated, however, that superior ESD robustness can be achieved without any increase in die area [11.17 - 11.19]. Industry standard ESD protection is generally achieved with gated and Zener diodes, and gate-coupled or body-coupled MOSFETS [11.20 - 11.26].

11.5.1 ESD Protection in Output Structures

When voltage is applied from an ESD transient to a logic output, a current path is created either to supply or ground, usually through the drain to body diode (figure 11.9). Additional, protection is afforded from the bipolar action of the structure, and from the turn-on of the MOS device in the reverse direction to supply. A vertical PNP to substrate can also turn-on directly to ground. Capacitive coupling can cause the parastic NPN of the output nMOS to turn-on momentarily.

With PD-SOI material, assuming no body ties are present, the diode is not present, and the bipolar devices can only turn on momentarily, since they are only capacitively coupled. For an ESD transient this may not matter, but for longer voltage transients, such as the automotive load dump, bipolars should not be considered as part of the protection capability. Protection is still obtained, however, from turn-on of the pMOS device. Figure 11.10 uses the example of a positive voltage spike, although a negative going voltage transient can be analyzed in a similar manner. Here, as the pMOS drain voltage raises above the source and gate, the device turns on in reverse (i.e.

Samsung Exhibit 1010, Page 194 of 204

the roles of source and drain switch). When the output to gate voltage rises above the Vt, the pMOS can turn on, sinking current into the supply. (For FD-SOI, the available paths are further limited, as there is no contribution from the capacitor-connected bipolar structure).

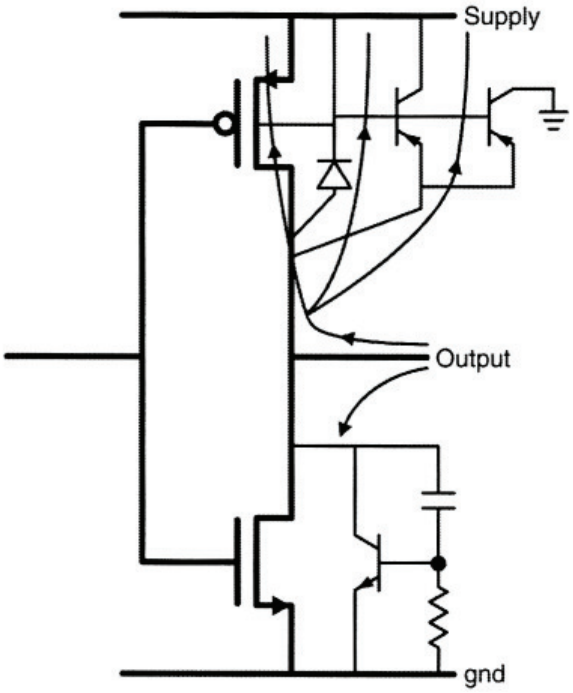


Figure 11.9: Bulk inverter output stage, showing available, current paths to ground, during a positive transient voltage spike.

While it may appear that SOI devices do not provide the same level of protection as bulk, there are two benefits which help offset the reduction in available paths. In SOI structures additional protection is provided through the fact that the output is not connected to ground or supply through a low resistance path. This allows the gate and body to float to some extent with respect to ground, providing a measure of protection not available from bulk material. In addition, the risk of destructive thyristor latchup is significantly reduced.

11.6 Radiation Hard (Rad-Hard) Circuits

Radiation affects circuitry in different ways, to a greater or lesser degree. Memory circuitry is highly susceptible, in particular because an entire memory array has to maintain radiation insensitivity even as cell areas reduce and array sizes increase. Memory elements, particularly those of dynamic RAM are particularly sensitive to the radiation effects, which can charge or discharge storage capacitors.

Samsung Exhibit 1010, Page 195 of 204

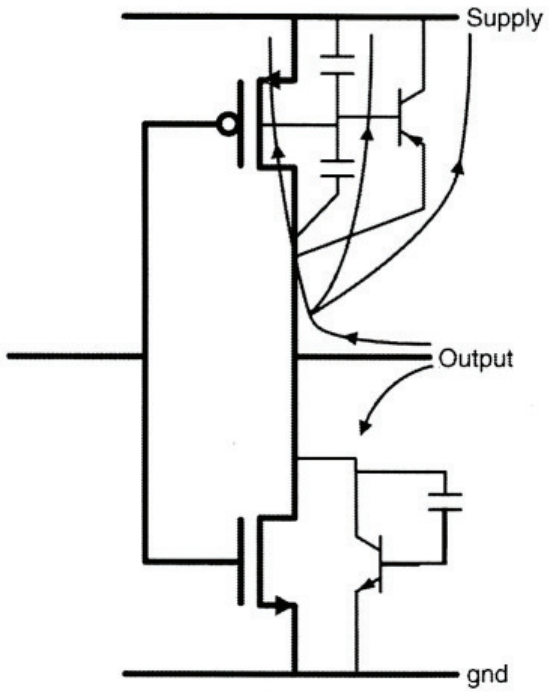


Figure 11.10: PD-SOI inverter output stage, showing available, current paths to ground, during a positive transient voltage spike.

Radiation insensitive components are required for computer systems in satellites, spacebourne systems and avionics. Numerous companies manufacture SOI components aimed specifically at rad-hard applications. Products available include CMOS, ASICs, SRAMs, ROMs, FIFOs, Non-Volatile Memories (MRAM), data bus interfaces and a limited number of analog circuits.

Threshold voltage shifts, caused by ionization and subsequent hole trapping in the gate, can affect all types of circuitry, through this is possibly less significant in digital than in analog designs, where a very small threshold voltage shifts can affect circuit operation. Within a digital system a small threshold voltage shift may not cause an affect on the device operation, particularly along a non-critical path. However, for analog circuits, a small change in Vt on a sensitive node can lead to a large change in circuit operating point [11.27], and cause parametric failure.

11.7 Reliability

There are several SOI specific aspects to reliability. The body voltage can go beyond the rail as a result of voltage pumping. This can potentially cause reliability issues, as the gate to body voltage may exceed the design limits for a substantial proportion of the operational condition. Gate oxide has been

Samsung Exhibit 1010, Page 196 of 204

demonstrated to be most susceptible to destruction at the same location as buried oxide leakage spots. Degradation of the gate oxide is the result of mechanical damage associated with deformation of the buried oxide [11.28].

Techniques for detecting reliability failures can be broadly split into "At-frequency" and "DC methods". "At-frequency" testing determines which ICs fall outside expected norms at given supply voltages, and temperature conditions. This determines failure due to certain abnormal resistive and leakage paths. These techniques tend not to be significantly different in their application from bulk. DC methods for reliability monitoring to detect failure mechanisms include quiescent supply current (IDDQ) testing. IDDQ analyses the DC leakage of an IC and variations of at-frequency test.

11.7.1 IDDQ (Quiescent Idd)

Excessive IDDQ may be caused by poor design practices, for example when a tristate node is allowed to float or when a bus conflict occurs. This becomes particularly problematic when the error-state occurs in a device sleep mode. IDDQ can also be high when process related problems occur, leading to excessive junction leakage or shorted transistors. Typically a design level IDDQ estimator is used. This determines leakage for static test cases. Excessive leakage is a signal that an unexpected leakage path exists, which is often a sign of a chip defect, which could cause failures later. Such units are screened out at test. IDDQ for SOI is similar, but some leakage paths are different. Clearly direct leakage paths to substrate no longer exist. Usually a leakage manifests itself from the body to source, and could be detected that way, but it might require more specific patterns for the IDDQ test vectors. Iddq is the current measured from Vdd with the device in a static or quiescent state. In a defect free circuit, the only current measured should be the device's normal off-state quiescent current. This should take the form of a distribution that should lie well below the customer requirement. If the circuit IDDQ is low enough, the IDDQ of outlier units susceptible to early failure is detectable with an IDDQ test as shown in figure 11.11.

Even with bulk material, due to node charging and capacitive effects, it takes tens of microseconds for a chip to settle into a state of true quiescence. Until the settled time is reached, the quiescent current is usually higher than the true IDDQ value. This is shown in figure 11.12. For floating body PD-SOI this time constant is extended, and can be milliseconds. This can cause excessively long test times, which is expensive. To avoid this, it is speculated that it may be possible to test IDDQ as a delta measurement,

Samsung Exhibit 1010, Page 197 of 204

while current is settling, by measuring IDDQ at two or more points during the settling time, and extrapolating the current trend.

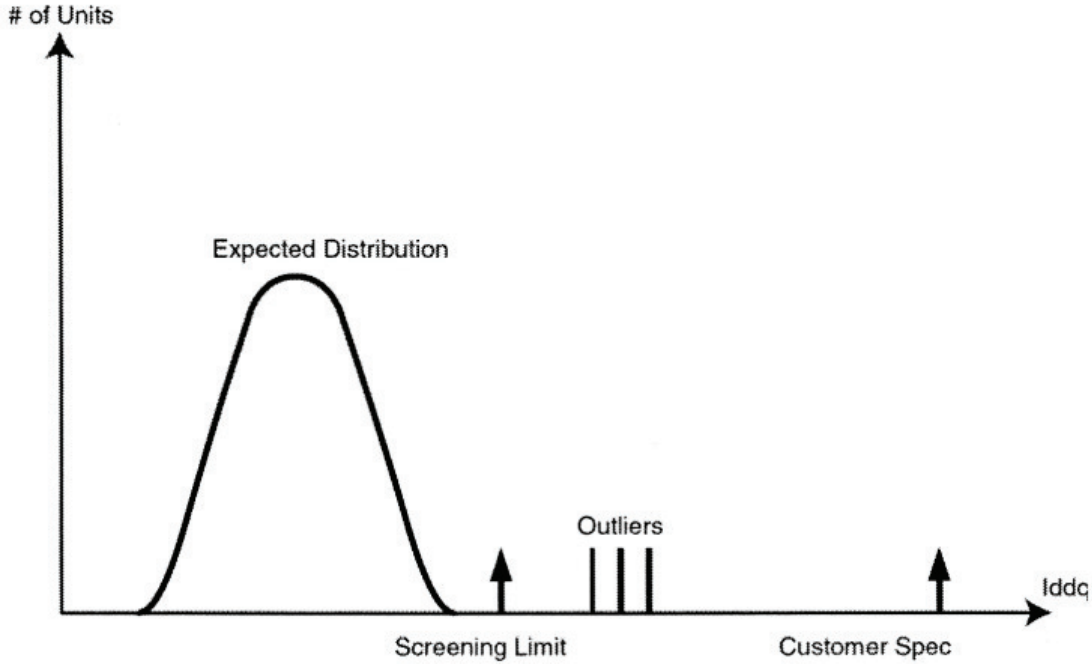


Figure 11.11: Graph of IDDQ showing expected distribution of IDDQ when the chip is in a quiescent state. The test limit is chosen to screen outliers, which are prone to early life failure.

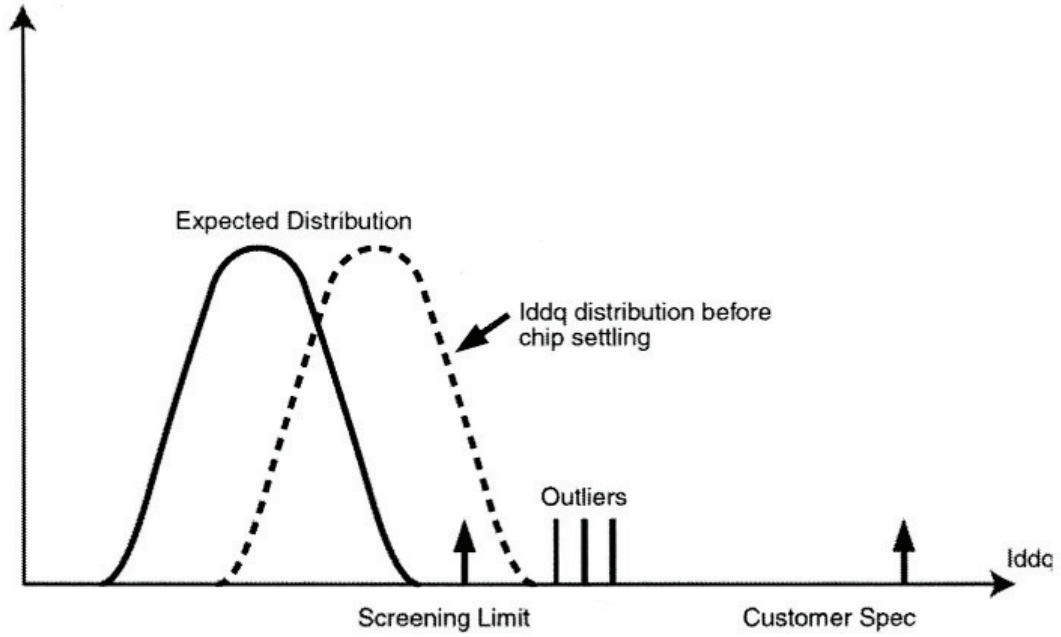


Figure 11.12: IDDQ limits before complete settling of the chip has occurred. This shows the potential to lose yield due to false detection of IDDQ failures.

Samsung Exhibit 1010, Page 198 of 204

Circuits on SOI can hide some faults that are easily tested in bulk CMOS, such as gate-oxide pinholes, since the current path is not to the substrate but to the body, then the source, and then possibly through another transistor that is off. As in the case of channel leakage in bulk-CMOS circuits, Iddq fault detection would require test patterns that turn on the transistors to complete the current path when detecting such failures. In contrast to channel leakage, for gate-oxide holes on SOI, the faulty transistor itself must be turned on rather than off to detect the leakage.

IDDQ is a useful measure of how likely a part may be to pass burn-in testing, or fail early in the product life. Various IDDQ tests are available and these are developed in detail in other works [11.29, 11.30]. It is worth noting, however, that the floating body of SOI material requires additional considerations when planning IDDQ testing. IDDQ usually detects excess oxide or channel leakage, or bridging faults in polysilicon or metal. Leakage current of SOI material may take several milliseconds to settle into a DC condition, due to the time constant of the body voltages. This can increase testing time.

As described above, SOI devices are not susceptible to diode leakage to substrate, or from body to source or drain, except at the gate edges because most of the device is oxide isolated. Figure 11.13 shows this for a NAND gate. Here a defect in the upper NMOS gate does not show up if the lower NMOS is off (figure 11.13a), whereas in conventional bulk CMOS the same fault would show up as a leakage to substrate even when the lower NMOS device is off (figure 11.13b). The same type of defect in a comparator input pair may manifest itself as a variation in offset, whereas in bulk material there would be a high gate to ground leakage.

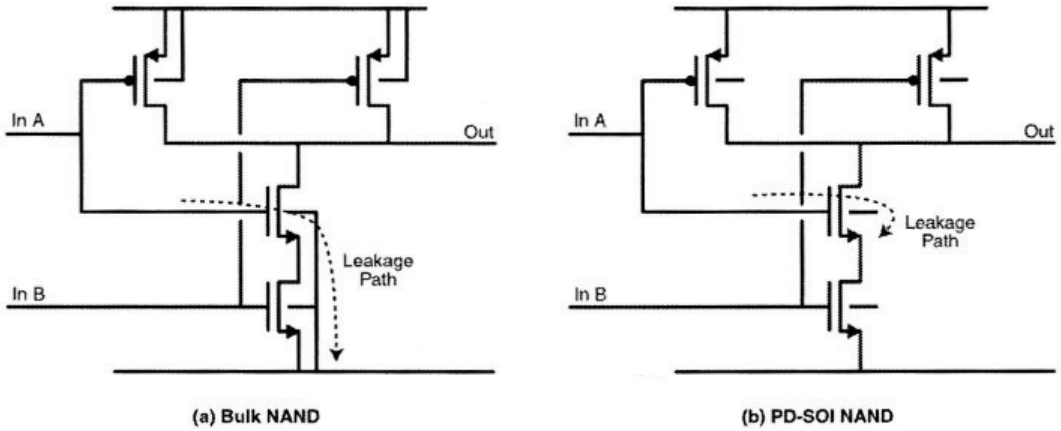


Figure 11.13: Nand gate configurations for bulk and SOI, showing defect leakage path for a gate fault in the upper NMOS structure. Under some conditions this will be observed as an IDDQ failure in bulk, but not in SOI.

Samsung Exhibit 1010, Page 199 of 204

11.7.2 Delay fault testing

The aim of delay fault reliability testing is to determine failure mechanisms, which can cause out-of-specification switching at either reduced or increased voltages [11.31, 11.32]. Often several conditions are tested beyond the normal operating limits, usually at a voltage just above the minimum theoretical operating point, and also at a high voltage, just below the maximum voltage sustainable by the gate oxides [11.30]. The expected variation of frequency with supply voltage depends on circuit type, but can be represented by a supply voltage vs frequency graph, for weak, nominal and strong device characteristics (figure 11.14).

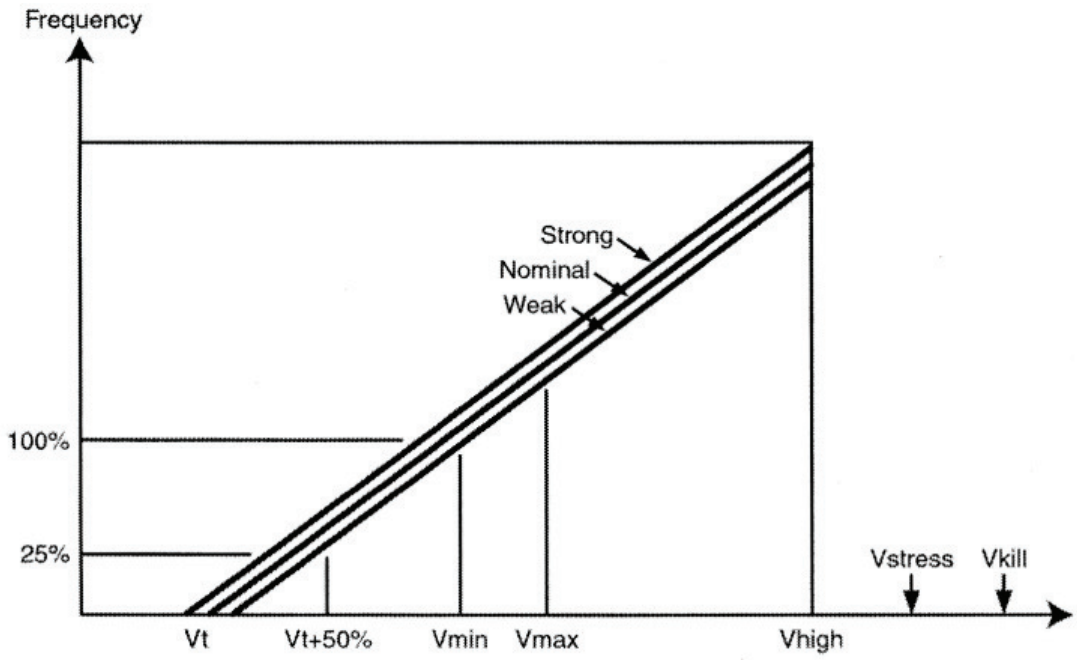


Figure 11.14: Graph showing conceptually how frequency of a critical path may change with frequency. To detect failures caused by bridging faults and resistive contacts, testing is done at voltages below and above normal operation.

The low voltage test point is applicable to SOI, and should not cause added testing difficulty, although the variation of critical path delays due to body voltage and threshold voltage variation needs consideration. At lower voltages this is not normally a problem but at the high voltage extreme, it may be an issue. At high voltages there is the possibility of a gate being pumped beyond the source, below ground for an NMOS and above the supply rail for a PMOS. Unless the at-frequency high voltage testing accounts for this there is a significant danger of exceeding gate breakdown

Samsung Exhibit 1010, Page 200 of 204

conditions. In addition, higher voltages lead to an increased variation of the path delay time, further increasing frequency uncertainty.

11.8 Package and Bond wire

Bond wires, package pins, printed circuit board traces, and IC metal all have parasitic inductances. When a SOI CMOS circuit switches, a current spike flows through the power bus. When current changes through an inductor, a voltage is generated across the inductor which is equal to L*dI/dt. This causes internal power rail ringing, which may cause errors. Ground bounce can adversely affect performance of the circuit, especially input-output circuits.

References

[11.1] C. Eisenhut & J. W. Klein, "SIMOX Voltage References for Applications up to 275°C using the Threshold Difference Principle", Proceedings 1997 IEEE International SOI Conference, Oct 1997, pp. 110-1.

[11.2] A. Marshall, "Operating Power ICs at 200 degrees", IEEE Power Electronics Specialists Conference, Madrid, Spain 1992, pp. 1033-9

[11.3] Appendix 1: (11.3)

[11.4] S. K. H. Fung, et. al., "Impact of the Gate-to-Body Tunneling Current on SOI History Effect", 2000 IEEE International SOI Conference, pp. 122-3.

[11.5] T. Efland, et. al., "The load dump (automobiles)", IEEE Workshop on Electronic Applications in Transportation, 1990, pp. 73-78.

[11.6] A. Marshall & J. Devore, "Dual switch-mode regulator IC" International Solid-State Circuits Conference (ISSCC), 1995. pp. 52–53.

[11.7] D. W. Dobberpuld, et. al., "A 200-MHz 64-b dual-issue CMOS microprocessor", IEEE J. Solid-State Circuits, vol. 27, Nov. 1992, pp. 1555-1567.

[11.8] R. Berger, et. al., "A 1.3-GHz SOI CMOS Test Chip for Low-Power High-Speed Pulse Processing", IEEE Journal of Solid State Circuits, Vol. 33, No. 8, Aug 1998, pp. 1259-6.

[11.9] J-H. Lee & Y-J. Park, "High speed SOI buffer Circuit with the Efficient Connection of Subsidiary MOSFET's for Dynamic Threshold Control", Proceedings 1997 IEEE International SOI Conference, Oct 1997, pp. 152-3.

[11.10] C.Chen, et. al.,"Single-transistor latch in SOI MOSFET's", IEEE Electron Device Letters, vol.9, 1988, pp.636-8.

[11.11] J. Gautier & A.J.Auberton-Herve, "A Latch Pheonomenon in buried N-body SOI NMOSFET's", IEEE Electron Device Letter, vol.12, 1991, pp.372-4.

[11.12] A. Marshall & F. Carvajal, "Power+ Logic Methodology Applied to a Six Output Power Driver", IEEE 1993 Bipolar/BiCMOS Circuits and

Technology Meeting, Minneapolis, Minnesota, Oct 4-5, 1993. IEEE Cat No. 93CH3315-9, pp. 72-75.

[11.13] "Flip-chip bumping on 300mm wafers", European Semiconductor, Feb 2000, p38

[11.14] J. Klein, "Bottomless SO-8 Package Boosts MOSFET Performance", Power Conversion and Intelligent Motion, May 2000, pp. 110.

[11.15] Y. Wang et.al., "Electrothermal Modeling of ESD Diodes in Bulk-Si and SOI Technologies," EOS/ESD Symp. Proc., pp. 430-436, 2000.

[11.16] S. Ramaswamy et. al., "EOS/ESD Protection Circuit Design for Submicron SOI Technology," EOS/ESD Symp. Proc., pp. 212-217, 1995.

[11.17] G. G. Shahidi, et. al., "CMOS scaling for high performance applications" IBM J. Res. Development, vol. 39, Jan./Mar. 1995, pp. 229-244.

[11.18] S. H. Voldman, "The State of the Art of Electrostatic Discharge Protection: Physics, Technology, Circuits, Design, Simulation, and Scaling", IEEE Journal of Solid State Circuits, Vol 34, No. 9, Sept. 1999, pp. 1272-1282.

[11.19] P. Raha, et. al., "EOS/ESD Reliability of Partially Depleted SOI Technology", IEEE Trans. Electron Device., Vol. 46, No. 2, Feb. 1999, pp. 429-431.

[11.20] S. Voldman, et. al., "Dynamic Threshold Body and Gate-Coupled SOI ESD Protection Networks," Jounral of Electrostatics, 44, pp. 239-255, 1998.

[11.21] C. Duvvury, et. al., "ESD design for deep submicron SOI technology,"Symp. VLSI Technology Dig. Tech. Papers, 1996, pp. 194-195.

[11.22] J. C. Smith, et. al., "ESD protection circuits for TFSOI technology," Proc. 1996 IEEE Int. SOI Conf., 1996, pp. 170-171.

[11.23] S. Voldman et. al., "CMOS-on-SOI ESD protection networks", Proc. EOSIESD Symp., Sept. 1996, pp. 291-301.

[11.24] M. Chan, et. al., "Comparison of ESD protection capability of SOI and bulk CMOS output buffers" Proc. IRPS, 1994.

[11.25] K. Verhaege, et. al., "Double snapback in SOI NMOSFET's and its application for SOI ESD protection", IEEE Electron Device Lett., vol. 14, July 1993, pp. 326-328.

[11.26] "Analysis of snapback in SOI NMOSFET's and its use for an SOI ESD protection circuit", Proc. of the IEEE SOI Conf., 1992, pp. 140-141.

[11.27] T. P. Ma & P. V. Dressendorfer, Editors, "Ionizing Radiation Effects in MOS Devices and Circuits", New York: Wiley, 1989.

[11.28] Y. Minami, et. al., "Direct Observation of Gate Oxide Destruction due to BOX Breakdown in SOI" 2000 IEEE International SOI Conference, Oct. 2000, pp. 130-131.

[11.29] S. Chakravarty & P.J. Thadikaran, "Introduction to IDDQ Testing", Kluwer Academic Publishers, 1997

[11.30] B. T. Mitchell, "Operating-Extremes Test Improves Reliability", Test and Measurement World, Nov 2000, pp. 45-50.

[11.31] A. Krstic & K-T Cheng, "Delay Fault Testing for VLSI Circuits", Kluwer Academic Publishers, Boston, 1998.

[11.32] K. Baker, et. al., "Defect-based delay testing of Resistive Vias-contacts, a critical evaluation", International Test Conference ITC 1999, pp. 467-476

Samsung Exhibit 1010, Page 204 of 204