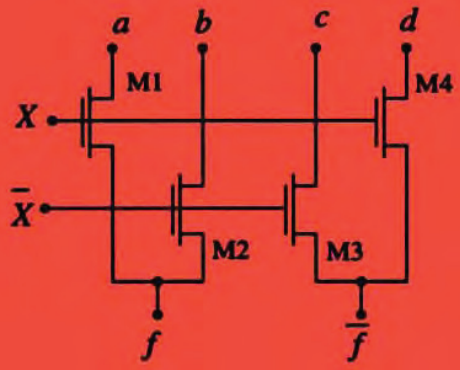
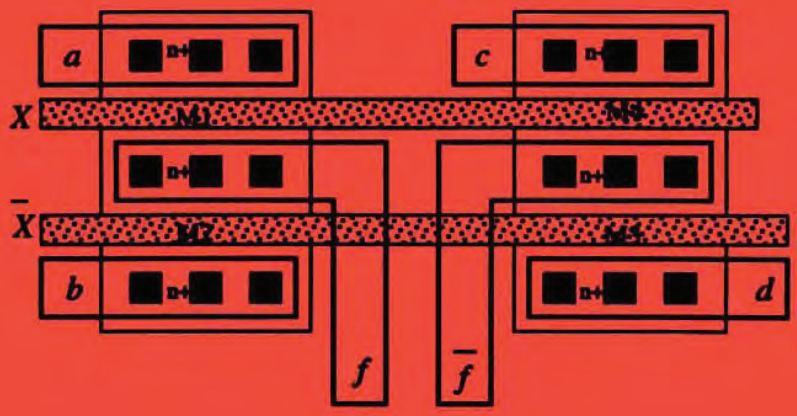
CMOS LOGIC CIRCUIT DESIGN





John P. Uyemura

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Dedication

This book is dedicated to

Christine and Valerie

for all of the joy and happiness
that they bring into my life



植　村

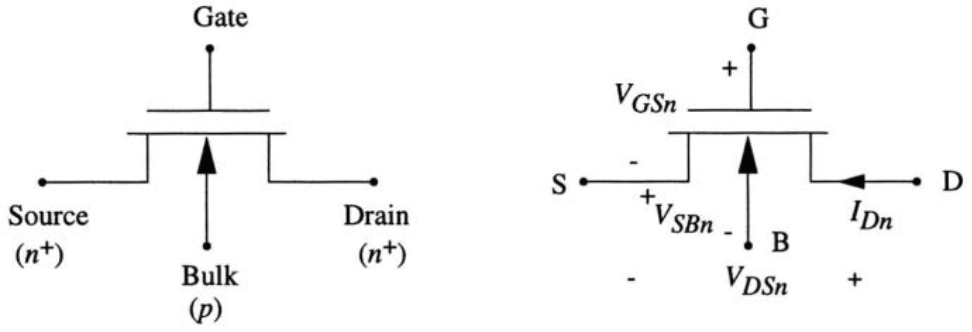
Chapter 1

Physics and Modelling of MOSFETs

MOSFETs (metal-oxide-semiconductor field-effect transistors) are the switching devices used in CMOS integrated circuits. In this chapter, we will examine the current flow through a MOSFET by analyzing is the path that the charge carriers follow. This results in an equation set that will be used for the entire book. Some advanced VLSI effects are also discussed in the second half of the chapter.

1.1 Basic MOSFET Characteristics

The circuit symbol for an n-channel MOSFET (**nFET** or **nMOS**) is shown in Figure 1.1(a). The MOSFET is a 4-terminal device with the terminals named the **gate, source, drain,** and **bulk.** The device voltages are shown in Figure 1.l(b). In general, the gate acts as the control electrode. The value of the gate-source voltage V_{GSn} is used to control the drain current I_{Dn} that flows through the device from drain to source. The actual value of I_{Dn} is determined by both V_{GSn} and the drain-



(a) nFET symbol (b) Current and voltages

Figure 1.1 n-channel MOSFET symbol

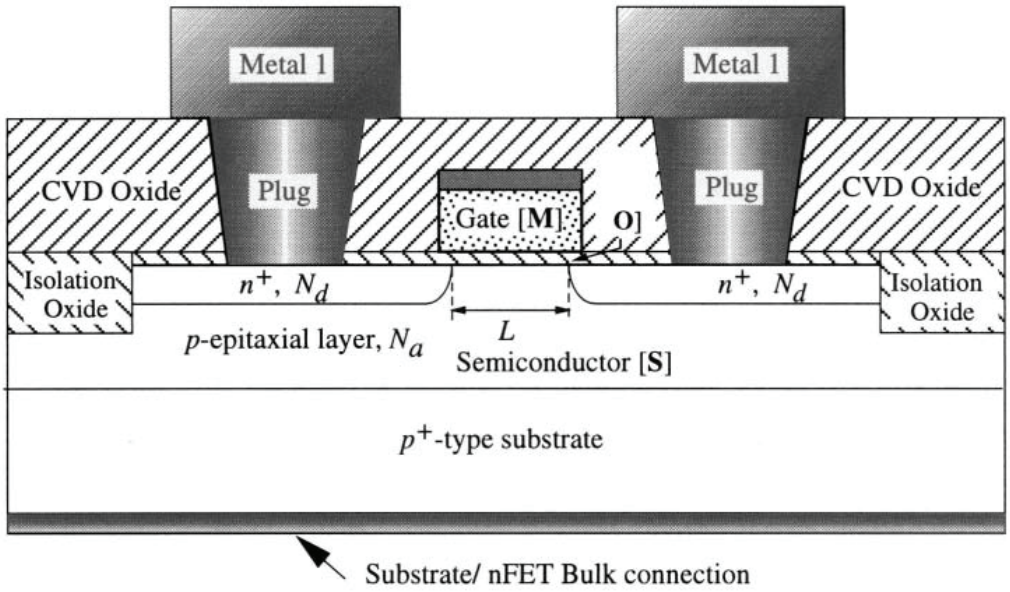


Figure 1.2 Cross-sectional view of a typical nFET

source voltage V_{DSn}. The source-bulk voltage V_{SBn} also affects the current flow to a lesser degree.

Figure 1.2 shows a typical nFET that will be used for the analysis. The central region of the device consists of a **metal-oxide-semiconductor** (**MOS**) subsystem made up of a conducting region called the **gate** [M], on top of an insulating silicon dioxide layer [O] shown as a cross-hatched region directly underneath the gate, and a p-type silicon [S] epitaxial layer on top of a $\mathbf{p^+}$-substrate. The existence of this capacitor substructure between the gate and the semiconductor is implied by the schematic symbol. The *I-V* characteristics of the transistor result from the physics of the MOS system when coupled to the $\mathbf{n^+}$ regions on the left and right sides. The $\mathbf{n^+}$ regions themselves constitute the drain and source terminals of the MOSFET, while the bulk electrode corresponds to the electrical connection made to the p-type substrate. The distance between the two $\mathbf{n^+}$ regions defines the **channel length** *L* of the MOSFET. As will be seen in the discussion, the channel length is one of the critical dimensions that establishes the electrical characteristics of the device.

A top view of the nFET is shown in Figure 1.3. This drawing defines the **channel width** *W* for the FET, and is the width of the region that supports current flow between the two $\mathbf{n^+}$ regions. The ratio (*W/L*) of the channel width to the channel length is called the **aspect ratio,** and is the important circuit design parameter. Note that the top view shows the length *L'* as the visual distance between the two $\mathbf{n^+}$ regions. This is called the **drawn channel length** and is larger than the electrical channel length *L*.

The *I-V* characteristics of a MOSFET are referenced to the **threshold voltage** V_T of the device; the actual value V_T for a particular device is set in the fabrication parameters. CMOS designs are based on **enhancement-mode** (E-mode) transistors where the gate voltage is used to enhance the conduction between the drain and source. By definition, an n-channel E-mode MOSFET has a positive threshold voltage $V_{Tn} > 0$, with a typical value ranging from about 0.5 to 0.9 volts. The value of the threshold voltage V_{Tn} is especially important to high performance circuit design.

In an ideal n-channel MOSFET, setting the gate-source voltage to a value $V_{GSn} < V_{Tn}$ places the transistor into **cutoff** where (ideally) the current flow is zero: $I_{Dn} = 0$; this is shown in Figure 1.4(a). Increasing the gate-source voltage to a value where $V_{GSn} > V_{Tn}$ allows the transistor to conduct cur-

saturation current and the saturation voltage. Owing to this observation, the bulk-charge model is often used as the basis of many advanced SPICE models. However, for calculator-based circuit estimates, the increased complexity offsets the gain in precision. Because of this reason, square-law equations are the most common for manual circuit analysis.

1.2.3 The Role of Simple Device Models

Both the square-law and bulk-charge models derived above are oversimplifications of the actual physics in a modern transistor. One reason is that they are both derived using the gradual-channel approximation, which is only valid for long channel lengths, typically requiring values greater than about $20\mu m$. With modern devices approaching values of $L \leq 0.20\ \mu m$, the simple equations ignore many short-device effects that arise in the 2-dimensional electrostatics and current flow. These and other important items are discussed later in this chapter.

One must always be careful not to depend on closed-form analytic equations. This is particularly true for semiconductor devices such as MOSFETs. Although their accuracy is always limited, analytic models remain extremely useful for circuit design, even if sub-micron size devices are employed. This is because the equations provide reasonable *estimates* of the *behavior* of the current-voltage characteristics that can be used for obtaining first-cut designs. Once the circuit is created, it can be simulated, analyzed, and re-designed using computer tools. When applied in a careful manner, this approach allows the engineer to perform intelligent design, not just produce a trial-and-error set of SPICE runs.

1.3 p-Channel MOSFETs

Perhaps the most important circuit design aspect of CMOS is the use of both n-channel and p-channel transistors in complementary arrangements. Adhering to this technique guarantees the desired properties of minimum DC power dissipation and rail-to-rail output logic swings.

The operational physics of a p-channel MOSFET (**pFET** or **pMOS**) is the complement of that used to describe the operation of an n-channel device. This means that we should

- change n-type to p-type regions, and
- change p-type to n-type regions.

Then, we

- reverse the roll of electrons and holes,
- reverse the polarities of all voltages, and
- reverse the direction of current flow.

Rather than duplicating the derivation of the MOSFET equations, we will just write down the important equations using these observations. Square-law models will be used throughout for simplicity, but the analogy can be extended to more complex models if desired.

A p-channel MOSFET must be constructed in an n-type background region. If a p-substrate is used as a starting point, then an **n-well** must be provided at all pMOS locations.[7] Figure 1.19 illustrates a pMOS transistor in this type of process; note that the pMOS bulk (the n-well) is connected to the highest voltage in the system, typically the power supply voltage V_{DD}. This is required to insure that the pn junctions do not become forward biased. The channel length L for the pFET is defined as the distance between the two p^+ regions. A top view of the pFET is shown in Figure 1.20. The channel width W defines the width of the current flow path, and the aspect ratio is (W/L). L' is again used to represent the drawn channel length. The power supply connection (V_{DD}) to the n-well is shown explicitly in the layout; this bias is critical to the operation of the device, and the

[7] The concept of an n-well is discussed in Chapter 2.

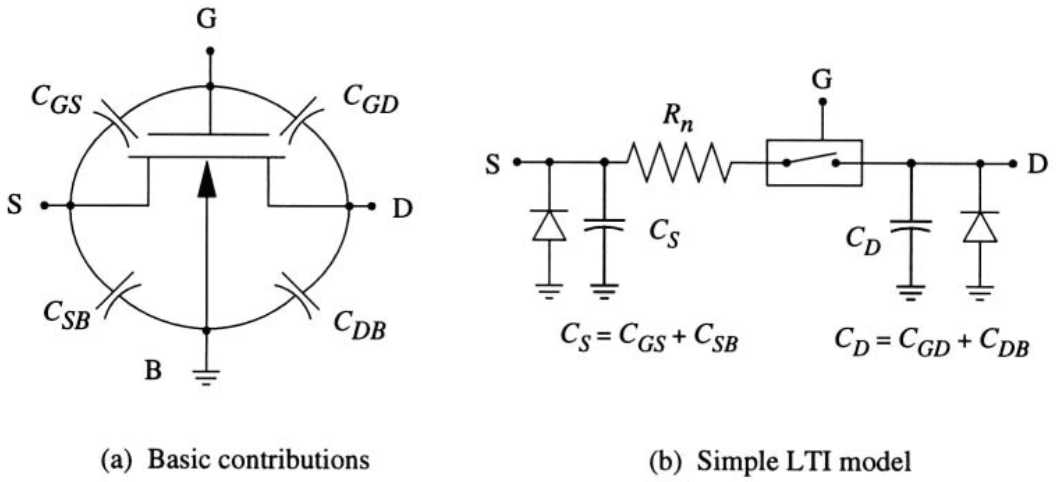


Figure 1.34 Simplified linear FET model for timing estimates

estimate on the performance during the design phases.

1.4.3 Junction Leakage Currents

In addition to the parasitic depletion capacitances, the pn junctions that are formed by the drain-bulk and source-bulk interfaces in a MOSFET introduce a component of leakage current that is often important in high-performance circuit design.

Consider the pn junction shown in Figure 1.35(a) which shows a pn junction with a reverse bias V_R applied. For a general forward bias voltage $V = -V_R$, the current is given by

$$I = I_o(e^{V/(kT/q)} - 1) + I_{dep} \tag{1.106}$$

where I_o is the **saturation current,** and I_{dep} is the current due to recombination or generation events in the depletion region. In a MOSFET, the drain-bulk and source-bulk regions are always biased with a reverse voltage V_R=-V. The reverse leakage current I_R=-I through the junction is then

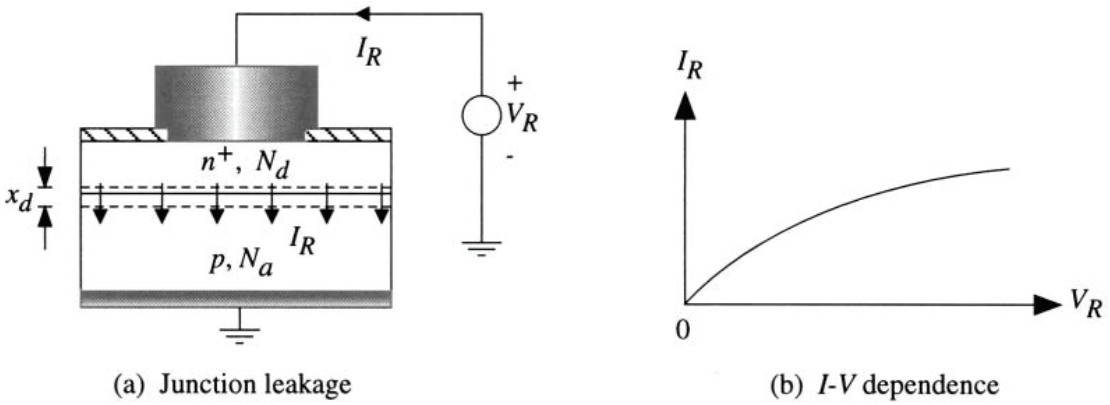


Figure 1.35 Reverse-bias pn junction leakage current

$$I_R = I_o + I_{gen} \approx I_{gen} \tag{1.107}$$

where I_{gen} is the **generation current** that dominates the reverse current flow in a silicon diode at normal operating temperatures. Analyzing the generation current in a step-profile junction gives

$$I_{gen} \approx I_{go}\left[\sqrt{1 + \frac{V_R}{\phi_o}} - 1\right] \tag{1.108}$$

where

$$I_{go} = \frac{qAn_i x_{d0}}{2\tau_o} \tag{1.109}$$

with A the area of the junction, and τ_o the effective carrier lifetime. The reverse current I_R is plotted as a function of the reverse voltage V_R in Figure 1.35(b). Note that I_R increases with the reverse bias voltage; this is opposite to the behavior of the junction capacitance, which decreases with increasing V_R.

The origin of the leakage current in a MOSFET is illustrated in Figure 1.36. Since the drain and source n^+ regions are always at a voltage greater than or equal to $0v$, the grounding of the p-type bulk region implies that they will always exhibit leakage flows regardless of the state of conduction of the transistor itself.

A MOSFET switching model that includes both the capacitances and the junction leakage currents is shown in Figure 1.37. This models the leakage current as a controlled current source with a value

$$I_R = I_{gen} \approx I_{go}\left[\sqrt{1 + \frac{V_R}{\phi_o}} - 1\right] \tag{1.110}$$

at each junction. Although this is highly simplified, it is generally sufficient for initial design estimates. It has the important characteristics that the leakage current is proportional to the junction area A, and increases with the reverse bias V_R.

For a more general doping profile, we may replace the voltage dependence with

$$I_{gen} \approx I_{gom}\left[\left(1 + \frac{V_R}{\phi_o}\right)^m - 1\right] \tag{1.111}$$

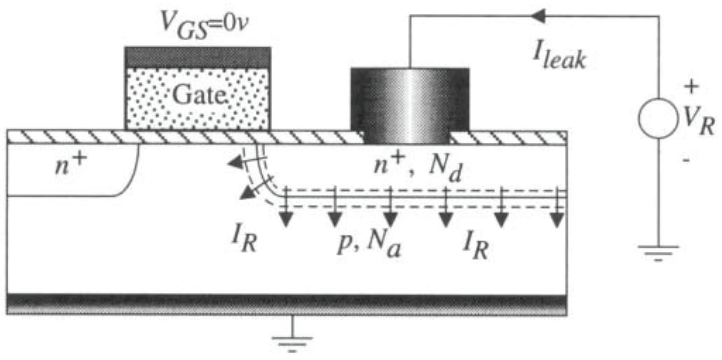


Figure 1.36 MOSFET reverse-bias junction leakage

2.4.3 Trench Isolation

An alternate to LOCOS uses oxide-coated trenches that have been etched into the silicon wafer to isolate devices. Although the technology needed to perform trench isolation is more difficult than that used for LOCOS, the trenches require less surface area and thus allow for a higher integration density. In addition, some dynamic random-access memory (DRAM) cells use the trenches to create charge storage capacitors.

Conceptually, trench isolation is very straightforward to study. Reactive ion etching (RIE) is used to define vertical-walled trenches in the silicon substrate as shown in Figure 2.17(a). Oxygen is passed over the wafer, growing an oxide layer on the walls and bottom. Polysilicon is then used to fill-up the trenches, and a final oxide growth and addition of the FETs gives the structure shown in Figure 2.17(d). The isolation action is obvious: lateral current flows (i.e., parallel to the surface) are blocked by the insulating trenches. Overall, this yields a more planar surface that makes it easier to add above-wafer interconnect layers.

2.5 The CMOS Process Flow

Let us now follow the basic sequence that is needed to fabricate nFETs and pFETs in a p-type wafer. This is called an n-well process, since an n-region must be introduced to accommodate the pFETs. The cross-sectional views of the wafer during the steps described in the next few para-

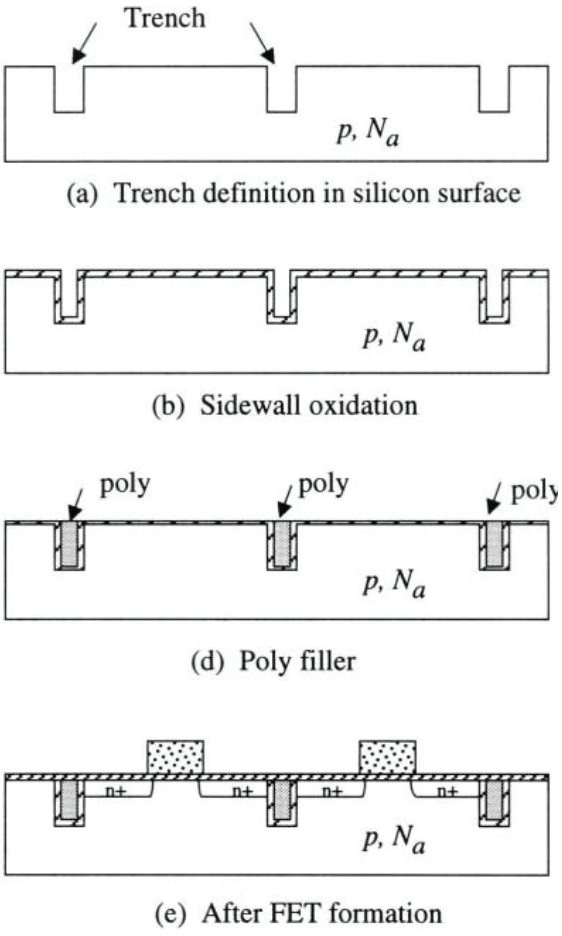


Figure 2.17 Basic steps in trench isolation

graphs are shown in the drawings of Figures 2.18 to 2.22. It is important to note that the drawings are not to scale since the thicknesses have been exaggerated for clarity.

The starting point in our example process is a heavily doped p^+ wafer that we will generally call the substrate. A thin p^- silicon epitaxial layer is grown on top of the wafer to provide a well-defined background for the transistors; this results in the cross-sectional view with the general structure depicted in Figure 2.18(a). Typically, the boron (acceptor) doping of the epitaxial layer is less than about $N_a=10^{15}\ cm^3$, and the epi layer is only a few microns thick. In the remaining views, only the epitaxial layer will be shown; the wafer itself will be omitted in an attempt to preserve at least some of the scaling. Since nFETs have a p-type bulk, they can be created in the epitaxial layer. A pFET, on the other hand, requires an n-type bulk, so that we provide an n-well in the p-epitaxial layer for these transistors. The n-well is created using a deep ion implant that is diffused deeper into the substrate, resulting in the cross-section shown in Figure 2.18(b). Once this has been accomplished, the threshold voltage ion implant adjustments must be performed for both nFETs and pFETs. These are shown in Figures 2.18(c) and (d). Creating a positive nFET threshold voltage V_{Tn} requires a boron (p-type) with a dose D_I determined by the oxide thickness, doping levels, and other physical parameters. The working value of the pFET threshold voltage $V_{Tp} < 0$ is also established by a ion implantation step; a donor implant makes the value more negative while an acceptor implant makes the value less negative. The next step is the creation of the dielectric isolation regions. This is summarized by the steps shown in Figure 2.18(e) and (f) for a LOCOS process, and results in the characteristics discussed in the previous section.

The next group of processing steps are used to form the transistors themselves. Access to the bare silicon surface [Figure 2.19(a)] is achieved by stripping the nitride and stress-relief oxide layers. This allows the careful growth of the gate oxide layer in which x_{ox} is established as in Figure 2.19(b). The gate oxide establishes the value of the oxide capacitance per unit area

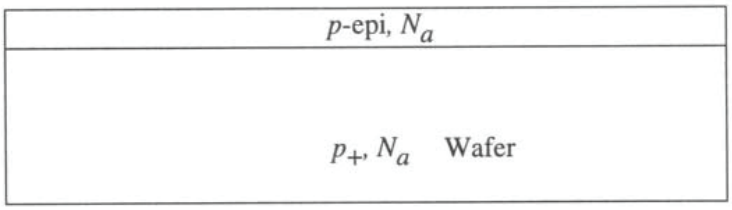
$$C_{ox} = \frac{\varepsilon_{ox}}{x_{ox}} \tag{2.28}$$

and is considered one of the most critical steps in the CMOS process flow. The next step is to deposit the gate polysilicon layer, which is then patterned by lithography according to the location of the transistor gates; this results in the structure shown in Figure 2.19(c).

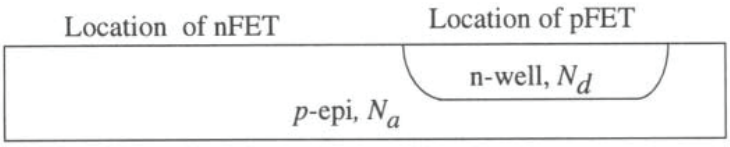
The transistors themselves are formed by ion implants using the self-aligned scheme. pFETs are created using a p-type boron implant in which nFET locations are blocked with photoresist; the resulting cross-section is portrayed in Figure 2.19(d). Similarly, nFETs require an n-type implant for drain and source regions. To accomplish this, pFET locations are blocked with resist while the n-implant is performed, leaving the structure shown in Figure 2.19(e). At this point, both FET polarities are established.

Figure 2.20 illustrates the "above-wafer" steps in the processing sequence. In (a), the surface has been coated with a CVD oxide that acts to electrically insulate the device from overlaying conductors. In advanced processes, this is followed by steps that planarize the surface for the next material layer. Contact cuts are etched into the oxide where needed, and then filled with a metal "plug" such as tungsten [Figure 2.20(b)] . The first layer of metal interconnect, denoted generically as "Metal1" is deposited and patterned as implied by the view in Figure 2.20(c).This is repeated for each subsequent interconnect level. Figure 2.21 illustrates the cross-sectional view after the deposition of the second metal (denoted as metal2 in the drawing); in this case, the contacts are called "vias."

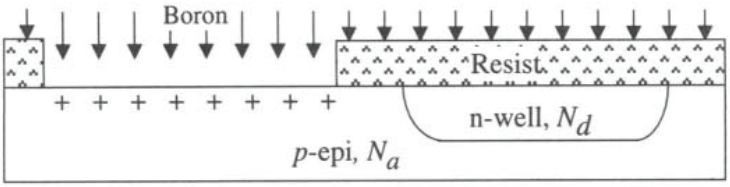
State-of-the-art CMOS processing has become quite complex, with many interconnect layers used to ease the layout and signal distribution problems. Figure 2.22 shows the layers in a hypothetical 4-metal process.The numerical values indicate thicknesses in units of microns, and are typical of those found in a modern process. The materials themselves vary with the manufacturer. Various compounds are used at interface layers, and the aluminum is often the material of choice for the



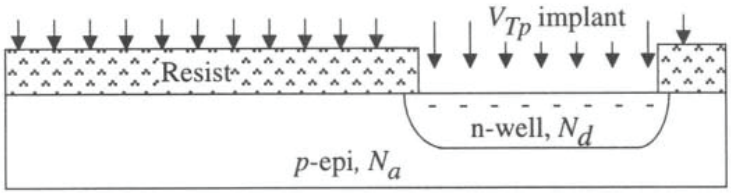
(a) Epitaxial layer growth



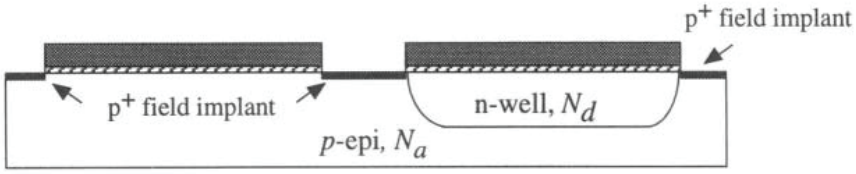
(b) After n-well creation



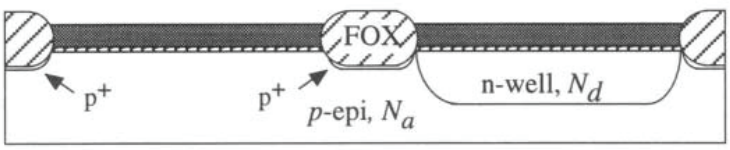
(c) nFET threshold implant



(d) pFET threshold implant



(e) Active area definition and field implant



(f) Local oxidation

Figure 2.18 Initial steps in a bulk n-well CMOS process

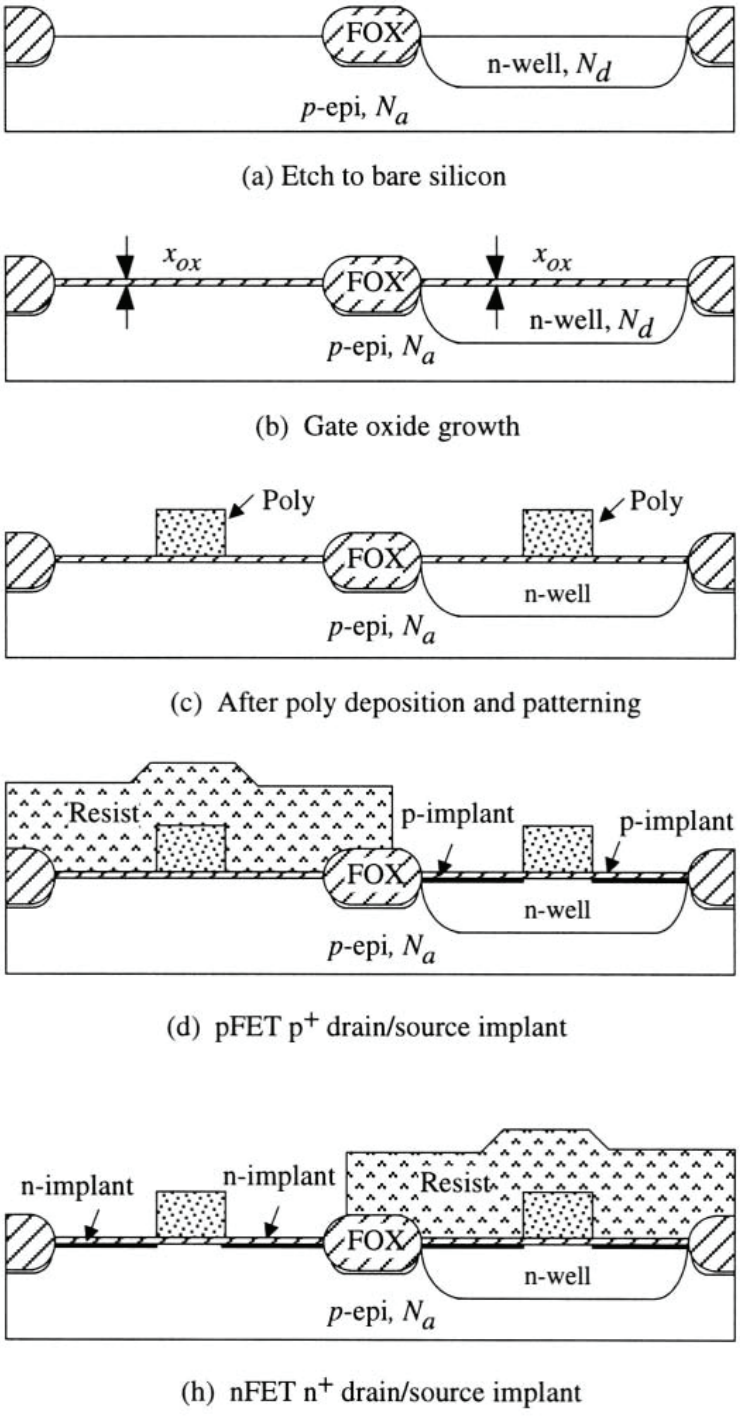
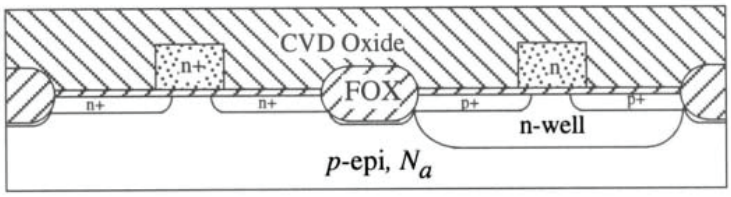
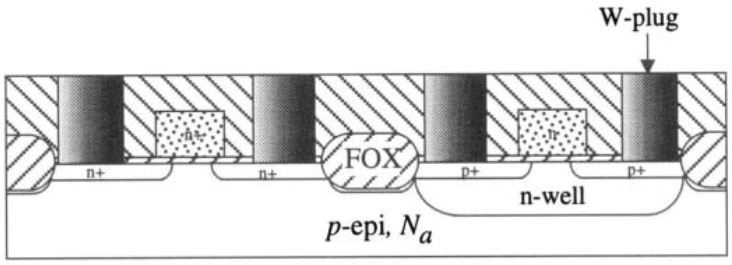


Figure 2.19 Formation of MOSFETs in the CMOS process

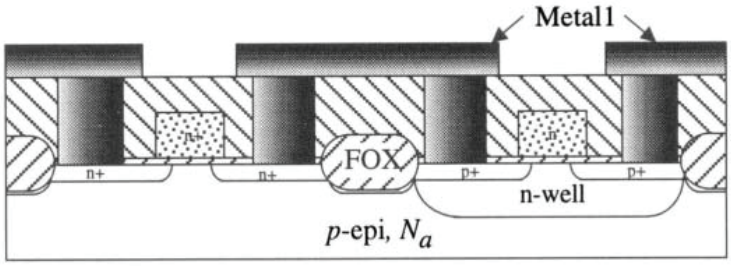
high level layer(s). Although the structures vary, the circuit designer is generally not overly concerned with specifics such as the materials, since it is the electrical characteristics that are of prime importance.



(a) CVD oxide and planarization



(b) Active contacts and tungsten plugs



(c) Metal1 Deposition and patterning

Figure 2.20 First metallization step

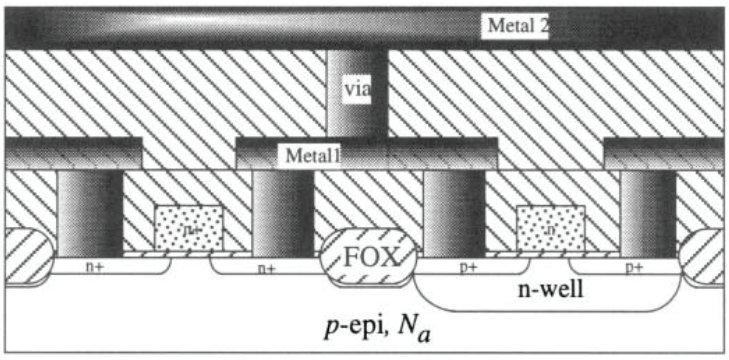


Figure 2.21 Cross-sectional view after second metal deposition

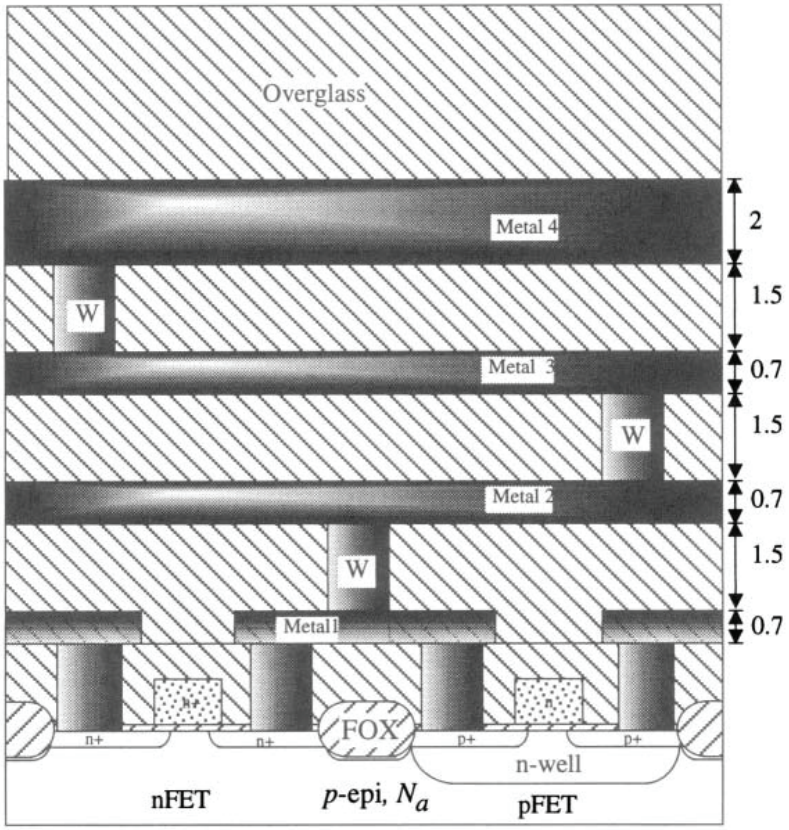


Figure 2.22 Visualization of 4-metal interconnect structure

2.5.1 Silicide Structures

Polysilicon is used for the gate material because the material has excellent coverage, adheres well to the silicon dioxide, and can be doped. Unfortunately, even heavily doped poly has a relatively high resistivity which limits it use as an interconnect. This problem is solved by using a high-temperature (refractory) metal such as titanium as a "coating" on the top, creating what is called a **silicide.**

The sequence in Figure 2.23 shows how a silicide can be created in the basic process flow. After the drain and source implants have been completed, a layer of titanium is patterned on top of the transistors; this yields titanium silicide $TiSi_2$ on both the poly gate and the drain/source regions as shown in Figure 2.23(a). Next, a CVD insulating oxide layer is applied [Figure 2.23(b)]. Contact cuts and tungsten plugs complete the sequence, and results in the structure shown in Figure 2.23(c). In this example, the tungsten plugs are used to contact the silicide drain and source regions. Silicides appear in many different forms and structures, but all have the same objective: reduce the resistance of the polysilicon line.

2.5.2 Other Bulk Technologies

In addition to n-well CMOS, two other bulk processes can be created: p-well and twin-well (also known as twin-tub). These are illustrated in Figure 2.24. The p-well process in 2.24(a) starts with an n-type bulk wafer. pFETs can be placed in the substrate, but a p-well must be added to accom-

2.6.4 General Comments

Design rule listings are process-specific. Numerical values for every required mask dimension are derived by considering details such as the capabilities of the lithographic imaging equipment, and physical effects such as pn junction depletion widths and coupling parasitics. Since they are concerned with minimum sizes, the design rule set acts as the limiting factor for circuit integration. A critical observation is the fact that the size of a MOSFET is almost negligible compared to the area consumed by interconnect lines and other wiring. The means that the area of a CMOS layout tends to be limited by the interconnect itself.

CMOS design is directly related to layout, but in modern circuit engineering, the need to master layout varies with the scope of the position. Some chip designers "push polygons" on a daily basis, while others let layout technicians provide amazingly compact solutions that can be analyzed and simulated. The philosophy as to whether a chip designer should or should not perform the layout seems to vary with the company, or even depend upon the "culture" of a particular group within a company. If you are a student and just learning the subject, it is generally accepted that "the more you know, the better off you are."[6]

2.7 Latch-Up

The structure of a bulk CMOS process introduces a problem known as latch-up in which the circuits fail to operate and the chip draws excessive power supply current. In practice, this may arise in two different situations:

- The chip is operating normally, and then goes into the latch-up state. The only way to restore normal conditions is to disconnect the power supply, and then reapply. The chip may go into latch-up again.
- The chip goes into latch-up immediately upon application of the power supply.

In the worst case scenario, the chip will be destroyed by heat. In the early days of CMOS development, latch-up was a major problem that slowed the growth of the technology. Although the factors that induce the condition are now understood, there are times when it can still be a problem.

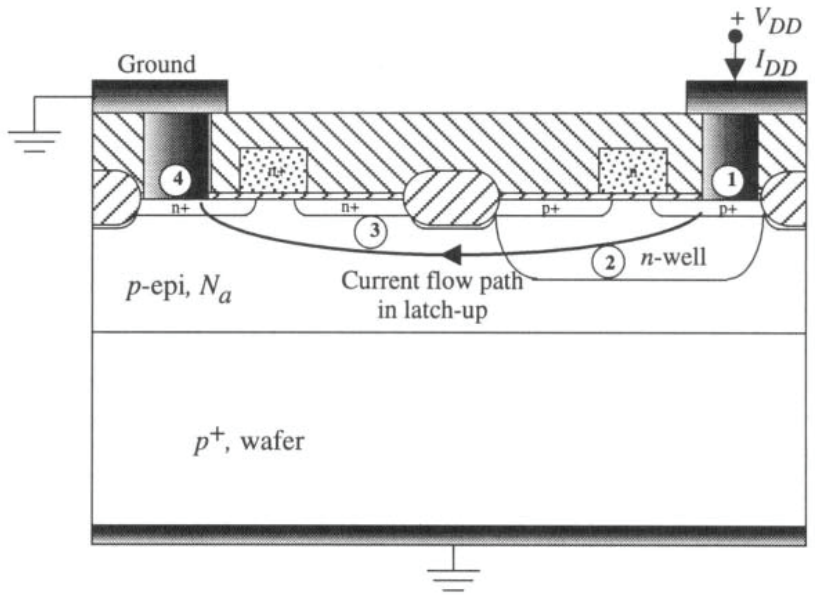
The origins of latch-up can be shown using the drawing in Figure 2.35(a). This identifies four distinct layers and the current flow path from the power supply voltage (V_{DD}) to ground associated with the latch-up condition. Under normal operating conditions, current along this path would only consist of leakage components. However, the nature of the layering scheme gives rise to parasitic bipolar transistors as shown in Figure 2.35(b). As discussed below, the bipolar transistors form a feedback loop that may induce latch-up.

The left drawing in Figure 2.36 shows how the layers 1 through 4 in the CMOS structure can be viewed as creating a 4-layer device with the pnpn layering. In power electronics, this is called a **silicon-controlled rectifier** (SCR) where it is used as a switching device between the top (p) and bottom (n) regions. From the qualitative viewpoint, the 4-layer structure blocks current flow from the power supply to ground due to the presence of reverse-biased pn junctions in the path. However, if one of the internal regions (n-well or p-epi) can be electrically shorted, then we would be left with a forward biased pn junction from the top to the bottom. This would give I_{DD} exponential characteristics of the form

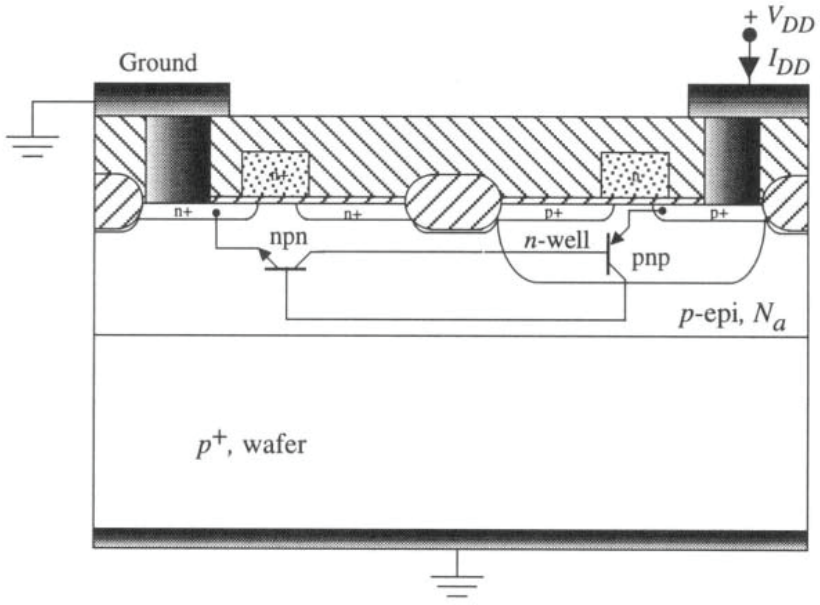
$$I_{SS} \approx I_S \exp\left(\frac{V_{DD}}{kT/q}\right) \tag{2.33}$$

indicating a large current flow. To describe this type of behavior, we will construct an equivalent

[6] So you should sign up for the next VLSI systems course that is offered!



(a) Current flow path



(b) Parasitic bipolar transistor model

Figure 2.35 Latch-up current flow paths in the n-well structure

pair of npn and pnp bipolar transistors from the structure as shown on the right side of Figure 2.36. This shows that the base of the pnp also acts as the collector of the npn transistor. Similarly, the collector of the pnp is electrically the same as the base of the npn. The pnp-npn pair thus form a set of coupled bipolar transistors where the current flow through one affects the conduction characteristics of the other.

The effect of the parasitic bipolar transistors can be understood using the equivalent circuit shown in Figure 2.37(a). Resistors have been added to represent the parasitic effects of the silicon regions. This circuit diagram illustrates the fact that the two transistors are connected in a manner that creates a feedback loop between the them; this is the middle window in the circuit schematic.

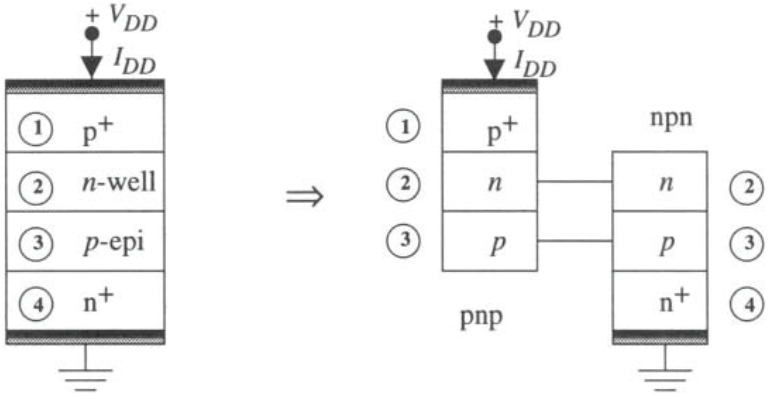
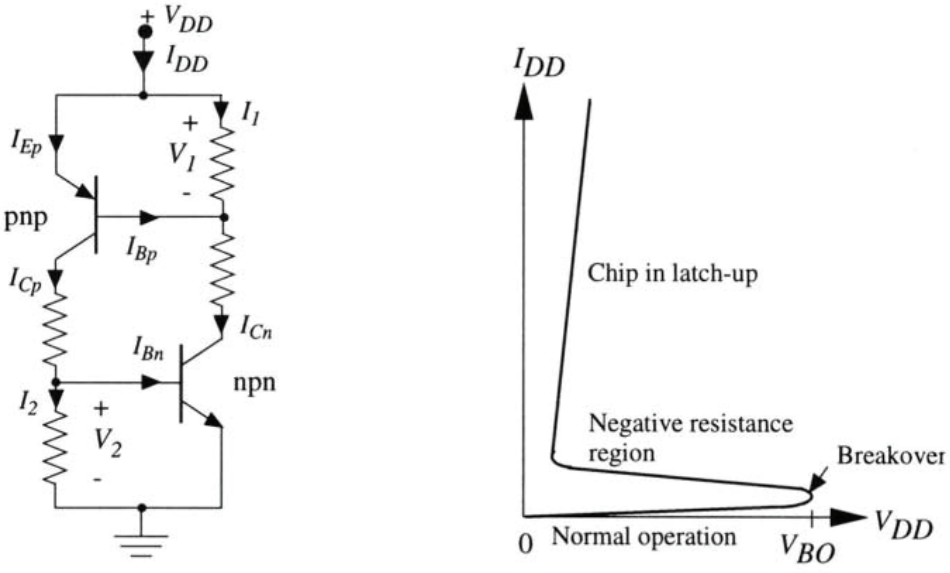


Figure 2.36 4-layer modelling of the latchup network

Consider the current I_1 on the right-hand side of the circuit. Under normal conditions, this will be leakage current. However, it creates a voltage V_1 that acts as an emitter-base voltage $V_1=V_{EB1}$ across the pnp transistor, enhancing the flow of I_{Ep} and I_{Cp} in the device. Most of this current contributes to I_2 which establishes the voltage $V_2=V_{BE2}$ across the base-emitter junction of the npn transistor. This in turn enhances the collector current I_{Cn}, which increases I_1 and completes the feedback loop. If both transistors are conducting, then the structure may induce the latchup condition.

A plot of I_{DD} as a function of V_{DD} is shown in Figure 2.37(b). For small values of V_{DD}, the current is restricted to small leakage levels and there is no problem with the structure. However, if V_{DD} is increased to a value V_{BO}, known as the **break-over voltage,** the blocking characteristics of the 4-



(a) Equivalent circuit (b) *I-V* characteristic

Figure 2.37 Bipolar transistor modelling of latch-up

$$t_H \approx \frac{C_{out}(V_f - V_{IH})}{(3I_{Rn} - I_{Rp})} \tag{8.22}$$

due to the three nFET leakage paths. Also note that C_{out} has contributions from Mp and all three logic transistors.

Complex logic gates can be designed in the same manner. Figure 8.11 shows two examples. In Figure 8.11 (a), the transistors are arranged to provide the function

$$f = \overline{(x+y)\cdot z} \tag{8.23}$$

when the clock swings to the evaluation interval with ϕ=1. The circuit in Figure 8.11(b) is the exclusive-OR

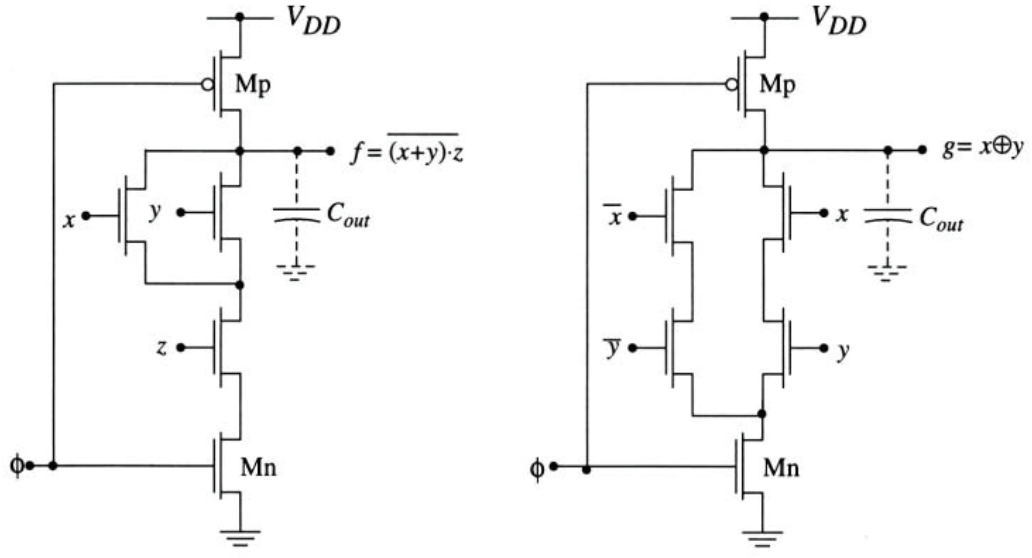
$$g = x \oplus y \tag{8.24}$$

as can be verified by applying the nFET rules. The important point being reiterated here is that the rules remain the same as in static logic design, but only the nFET array is needed. Eliminating the logic pFETs gives much simpler layout wiring and reduced capacitance levels.

8.2.3 nMOS-nMOS Cascades

Let us now examine the concept of cascading P/E gates to form a logic chain. The simplest approach is to cascade dynamic stages as shown in Figure 8.12. This drawing only shows one of the datapaths through the logic chain. This means that every input to Stages 2, 3, and 4 is assumed to originate from a preceding logic gate that is electrically similar to Stage 1.

The clock is distributed to every stage in the chain with the same phase, which gives the operation shown in Figure 8.13. Precharge occurs with ϕ=0 as shown in (a). Since the stages are all synchronized to the clock, every stage undergoes precharge at this time. This causes the output voltages to rise to V_{DD} as shown. A clock transition to ϕ=1 causes the chain to undergo evaluation.



(a) Complex logic gate (b) Exclusive-OR

Figure 8.11 Examples of dynamic complex logic gates

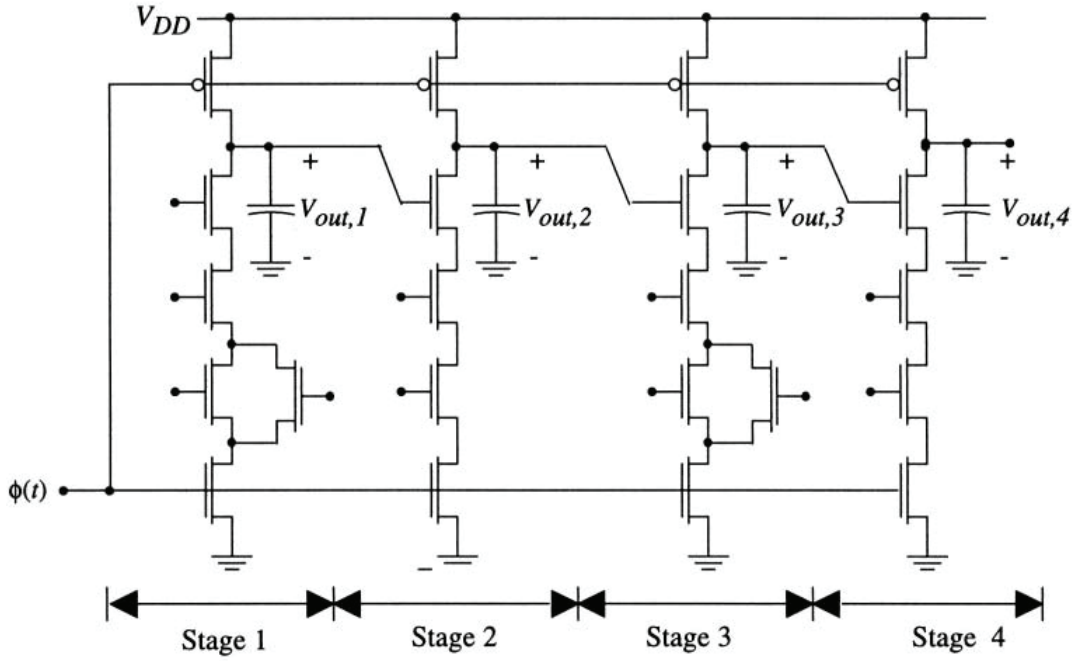


Figure 8.12 Cascade of dynamic logic gates

During this time, the output of each circuit is transferred to the input of the next stage(s), so that the logic "ripples" down the chain from left to right. In Figure 8.13(b), we have indicated the conditional discharge event by showing the currents $I_{dis,m}$ for $m = 1, 2, 3, 4$. If current flow is permitted through an nFET logic array, then the output voltage of that stage decays to 0*v*. A hold condition in the j-h stage is characterized by $I_{dis,j} = 0$. This acts to keep the output voltage $V_{out,j}$ at a high value, indicating a logic 1 result from the output of the gate.

Although this appears to be a straightforward scheme, cascading one nMOS stage into another nMOS logic stage introduces the possibility of a logic **glitch** in which an incorrect logic value is created by a circuit problem. To understand the origin of the problem, let us analyze the 2-stage NAND-NAND cascade shown in Figure 8.14(a). During the precharge event, ϕ=1 drives both Mpl and Mp2 into conduction, charging both output nodes to V_{DD}. Note in particular that, since

$$V_{out,1} = V_{DD} \tag{8.25}$$

the logic nFET MX in the second stage is driven into an active conduction state.

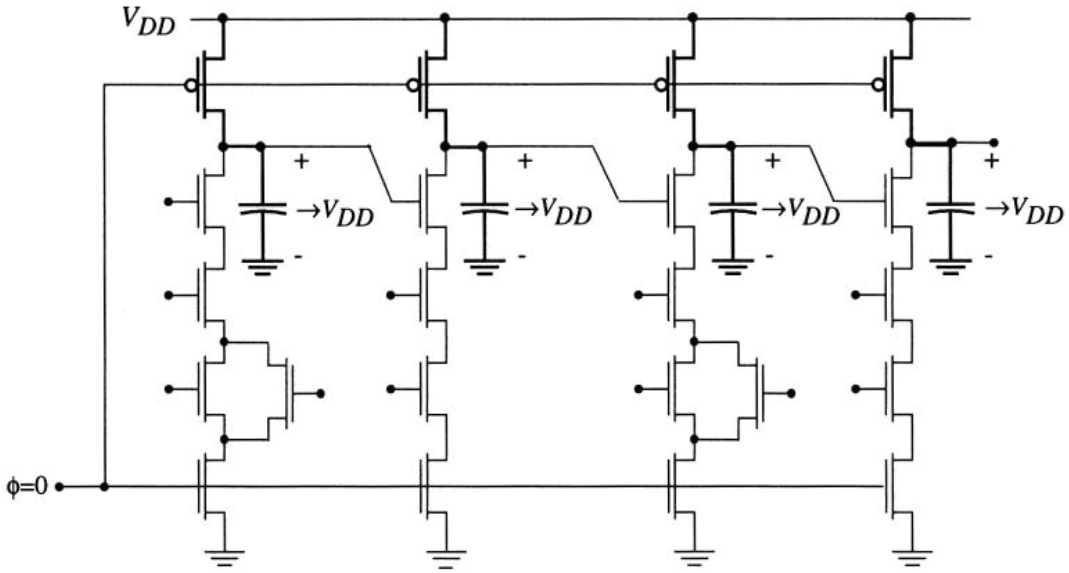
The possibility of a logic glitch can be seen by the situation Figure 8.14(b) where all of the inputs have been set at logic 1 levels. Consider the first stage. Since all inputs are high, $C_{out,1}$ will discharge in a characteristic time

$$\tau_{dis,1} = 4R_nC_{out} + 3R_nC_1 + 2R_nC_2 + R_nC_3 \tag{8.26}$$

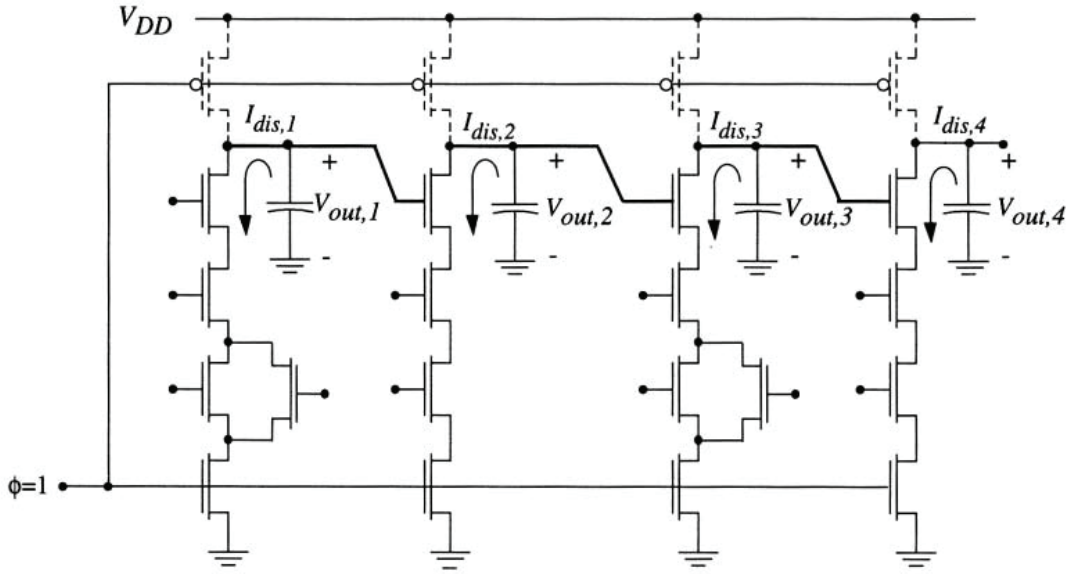
where we have assumed that all of the logic transistors have the same aspect ratio for simplicity. The value of $V_{out,1}(t)$ decays according to

$$V_{out,1}(t) = V_{DD}e^{-t/\tau_{dis,1}} \tag{8.27}$$

However, the logic nFET MX in the second stage conducts current until a time t_1 that is defined by the condition $V_{out,1}(t_1) = V_{Tn}$. Solving,



(a) Precharge

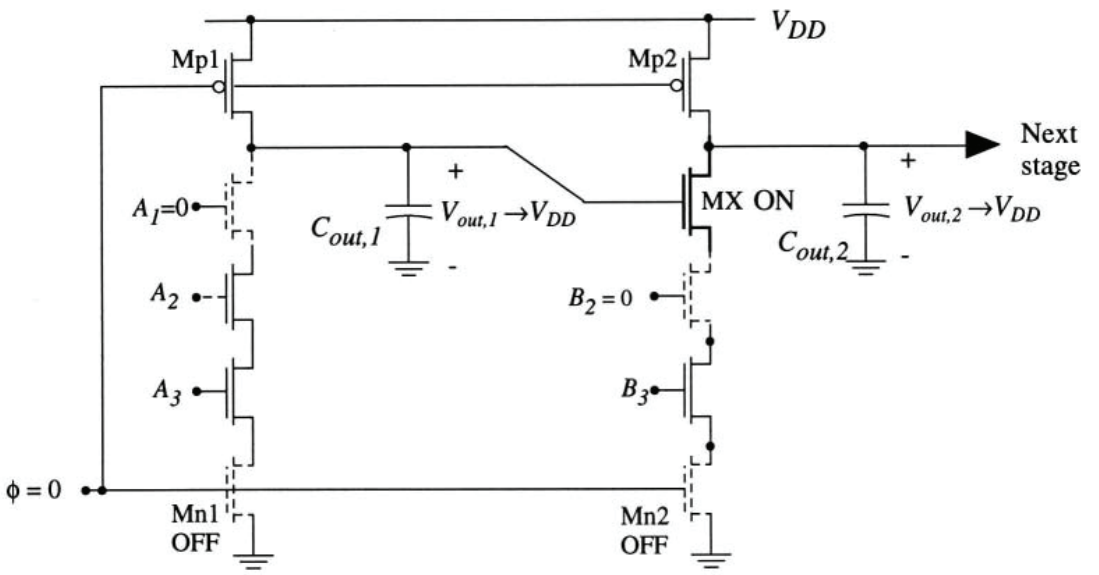


(b) Evaluate

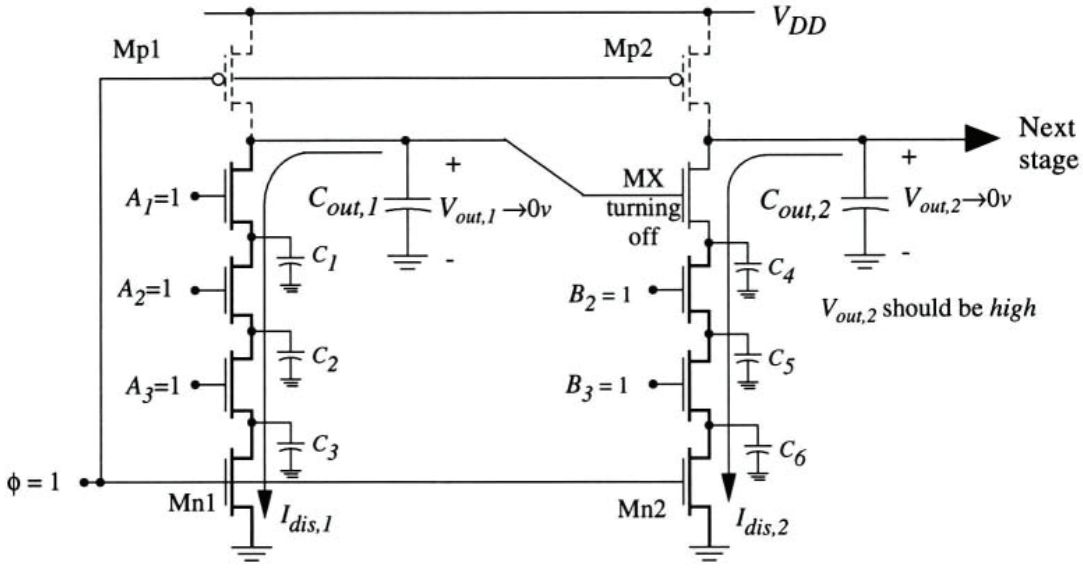
Figure 8.13 Internal operation of the dynamic logic cascade

$$t_1 = \tau_{dis,1} \ln\left[\frac{V_{DD}}{V_{Tn}}\right] \tag{8.28}$$

The potential for a problem can be seen by examining the behavior of the second stage while $C_{out,1}$ in discharging. During the time that $V_{out,1}$ is falling from V_{DD} to V_{Tn}, $C_{out,2}$ is discharging as long as MX is active. A glitch occurs if the final value of $V_{out,2}$ is so low that it is incorrectly interpreted



(a) Precharge



(b) Evaluate

Figure 8.14 The glitch problem in an nMOS-nMOS cascade

as a logic 0 voltage in the next (third) stage of the cascade.

To understand the problem, let us approximate the output voltage by the exponential form

$$V_{out,2}(t) = V_{DD} e^{-t/\tau_{dis,2}} \tag{8.29}$$

where $\tau_{dis,2}$ is the discharge time constant for the second stage characterizing the conducting path with $C_{out,2}$, C_4, C_5, and C_6. A glitch will occur if $V_{out,2}(t_1)$ falls below V_{IH} of the next stage. The