UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., AND SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Case IPR2024-01402
Patent No. 7,745,886

PETITION FOR *INTER PARTES* REVIEW

TABLE OF CONTENTS

I. Preliminary Statement 1

II. The ’886 Patent 2

A. Specification 2

B. Prosecution History 4

C. Claim Construction 5

III. Statement of Precise Relief Requested 5

A. Prior Art 5

B. Challenges 6

IV. Level of Ordinary Skill in the Art 6

V. Claims 1-19 Are Unpatentable 7

A. Ground 1: Claims 1, 2, 4, and 5 Are Anticipated by *Okashita* 7

1. Overview of *Okashita* 7

2. Independent Claim 1 9

a. [1pre]: “A switching circuit comprising:” 9

b. [1a]: “a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;” 9

c. [1b(i)]: “each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer,” 11

d. [1b(ii)]: “thereby forming a source/drain junction capacitance;” 13

e. [1c(i)]: "at least one trench extending through said device layer and contacting a top surface of said buried oxide layer,"....16

f. [1c(ii)]: "thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer." 18

3. Claim 2 23

a. [2]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer." 23

4. Claim 4 24

a. [4]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is an NFET with a gate driven by a switch control signal in a wireless communications device." 24

5. Claim 5 27

a. [5]: "The switching circuit of claim 4, wherein said switch control signal drives said gate of said NFET through at least one resistor."....27

B. Ground 2: Claims 1-7 Are Obvious over *Okashita*....28

1. Independent Claim 1 28

a. [1pre]: "A switching circuit comprising:" 28

b. [1a]: "a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;" 28

c. [1b(i)]: "each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer," 33

d. [1b(ii)]: "thereby forming a source/drain junction capacitance;" 34

e. [1c(i)]: "at least one trench extending through said device layer and contacting a top surface of said buried oxide layer," 34

f. [1c(ii)]: "thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer." 34

2. Claim 2 35

a. [2]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer." 35

3. Claim 3 35

a. [3]: "The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer." 35

4. Claim 4 37

a. [4]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is an NFET with a gate driven by a switch control signal in a wireless communications device." 37

5. Claim 5 37

a. [5]: "The switching circuit of claim 4, wherein said switch control signal drives said gate of said NFET through at least one resistor." 37

6. Claim 6 37

a. [6]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors

is a PFET with a gate driven by a switch control signal in a wireless communications device." 37

7. Claim 7 39

a. [7]: "The switching circuit of claim 6, wherein said switch control signal drives said gate of said PFET through at least one resistor." 39

C. Ground 3: Claims 1-7 Are Obvious Over *Okashita* and *Yu* 39

1. Overview of *Yu* 39

2. Combining *Okashita* and *Yu* 42

3. Independent Claim 1 44

a. [1pre]: "A switching circuit comprising:" 44

b. [1a]: "a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;" 44

c. [1b(i)]: "each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer," 44

d. [1b(ii)]: "thereby forming a source/drain junction capacitance;" 45

e. [1c(i)]: "at least one trench extending through said device layer and contacting a top surface of said buried oxide layer," 46

f. [1c(ii)]: "thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer." 46

4. Claim 2 46

5. Claim 3 46

a. "The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer." 46

6. Claim 4-7 49

D. Ground 4: Claims 1, 2, and 3 Are Anticipated by *Yu* 49

1. Independent Claim 1 49

a. [1pre]: "A switching circuit comprising:" 49

b. [1a]: "a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;" 50

c. [1b(i)]: "each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer," 51

d. [1b(ii)]: "thereby forming a source/drain junction capacitance;" 52

e. [1c(i)]: "at least one trench extending through said device layer and contacting a top surface of said buried oxide layer," 53

f. [1c(ii)]: "thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer." 53

2. Claim 2 56

a. [2]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer." 56

3. Claim 3 56

a. [3]: "The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer." 56

E. Ground 5: Claims 1-19 Are Obvious Over *Burgener* and *Okashita* 57

1. Overview of *Burgener* 57

2. Combining *Burgener* with *Okashita* 59

3. Independent Claim 1 64

a. [1pre]: "A switching circuit comprising:" 64

b. [1a]: "a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;" 64

c. [1b(i)-1b(ii)]: "each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;" 66

d. [1c(i)-1c(ii)]: "at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer." 66

4. Claim 2 67

a. [2]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer." 67

5. Claim 3 69

a. [3]: "The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer." 69

6. Claim 4 69

a. [4]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is an NFET with a gate driven by a switch control signal in a wireless communications device." 69

7. Claim 5 71

a. [5]: "The switching circuit of claim 4, wherein said switch control signal drives said gate of said NFET through at least one resistor." 71

8. Claim 6 72

a. [6]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is a PFET with a gate driven by a switch control signal in a wireless communications device." 72

9. Claim 7 73

a. [7]: "The switching circuit of claim 6, wherein said switch control signal drives said gate of said PFET through at least one resistor." 73

10. Claim 8 73

a. [8a]: "The switching circuit of claim 1, wherein a power amplifier in a wireless communications device provides an input to said switching circuit, and wherein an output of said switching circuit drives an antenna in said wireless communications device," 73

b. [8b]: "and said switching circuit is controlled by a switch control signal in said wireless communications device." 75

11. Claim 9 76

a. [9]: "The switching circuit of claim 8, wherein said wireless communications device is selected from the group consisting of a cellular telephone, a wireless personal computer, a wireless audio player, a wireless video player, and a wireless personal assistance device." 76

12. Claim 10 76

a. [10a]: "The switching circuit of claim 1, wherein an antenna in a wireless communications device provides an input to said switching circuit, and wherein an output of said switching circuit drives a low noise amplifier in said wireless communications device," 76

b. [10b]: "and wherein said switching circuit is controlled by a switch control signal in said wireless communications device." 77

13. Claim 11 78

a. [11]: "The switching circuit of claim 10, wherein said wireless communications device is selected from the group consisting of a cellular telephone, a wireless personal computer, a wireless audio player, a wireless video player, and a wireless personal assistance device." 78

14. Independent Claim 12 78

a. [12pre]: "A wireless communications device comprising a power amplifier and an antenna, said wireless communications device further comprising:" 78

b. [12a]: "a switching circuit controlled by a switch control signal and interposed between said power

amplifier and said antenna, said switching circuit including:" 79

c. [12b]: "a plurality of cascaded transistors …;" 81

d. [12c]: "at least one trench extending …." 81

15. Claims 13-15 81

16. Independent Claim 16 81

a. [16pre]: "A wireless communications device comprising an antenna and a low noise amplifier, said wireless communications device further comprising:" 81

b. [16a]: "a switching circuit controlled by a switch control signal and interposed between said antenna and said low noise amplifier, said switching circuit including:" 82

c. [16b]: "a plurality of cascaded transistors …;" 83

d. [16c]: "at least one trench extending …." 83

17. Claims 17-19 83

F. Ground 6: Claims 1-19 Are Obvious Over *Burgener*, *Okashita*, and *Yu* 83

1. Combining *Burgener* with *Okashita* and *Yu* 83

2. Claims 1-19 85

VI. Discretionary Denial Is Not Warranted 86

A. Denial of Institution Is Not Warranted Under *Fintiv* 86

B. Denial of Institution Is Not Warranted Under 35 U.S.C. §325(d) 87

VII. Mandatory Notices 88

A. Real Parties-in-Interest 88

B. Related Matters 88

C. Lead and Backup Counsel, and Service Information 88

VIII. Grounds For Standing 90

IX. Conclusion 90

CLAIMS APPENDIX 1

PETITIONER'S EXHIBIT LIST

Exhibit	Description
Ex. 1001	U.S. Patent No. 7,745,886 to Zwingman ("'886 patent")
Ex. 1002	Declaration of Scott Emmet Thompson, Ph.D. ("Thompson")
Ex. 1003	Prosecution History of the '886 patent (downloaded from Public PAIR)
Ex. 1004	U.S. Patent No. 6,836,172 to Okashita et al. ("*Okashita*")
Ex. 1005	U.S. Patent No. 6,737,682 to Yu ("*Yu*")
Ex. 1006	U.S. Patent Publication No. 2006/0270367 to Burgener et al. ("*Burgener*")
Ex. 1007	Webster's Ninth New Collegiate Dictionary, Merriam-Webster, Inc., Springfield, Massachusetts, U.S.A., 1985, p. 211.
Ex. 1008	"Fundamentals of Semiconductor Physics and Devices," Rolf Enderlin and Norman J.M. Horing, World Scientific, 1996, pp. 535-539, 620-622.
Ex. 1009	"Electronics Circuits and Analysis," Dinesh C. Dube, Alpha Science International Ltd., 2005, pp. 202-207.
Ex. 1010	"SOI Design: Analog, Memory and Digital Techniques," Andrew Marshall and Sreedhar Natarajan, Kulwer Academic Publishers, 2003, pp. 1-46, 75-84, 125-179, 289-338, 340-358.
Ex. 1011	"CMOS Logic Circuit Design," John P. Uyemura, Kluwer Academic Publishers, 2002, pp. 1-2, 19, 35-36, 78-83, 94-96, 359-362.
Ex. 1012	"The Stuff Dreams Are Made Of [Part 1]," Paul DeMone, May 8, 2002, Available at: https://www.realworldtech.com/cmos-basics
Ex. 1013	"SOI for Digital CMOS VLSI: Design Considerations and Advances," Ching-Te Chuang et al., Proceedings of the IEEE, Vol. 86, No. 4, April 1998, pp. 689-720.
Ex. 1014	"1 Giga bit SOI DRAM with fully bulk compatible process and body-contacted SOI MOSFET structure," Yo-Hwan Koh et al., 1997 International Electron Devices Meeting Technical Digest, Washington, DC, USA, 1997, pp. 579-582.

Exhibit	Description
Ex. 1015	U.S. Patent No. 6,121,148 to Bashir et al. ("Bashir"), published September 19, 2000.
Ex. 1016	"Speeding up Transistors: IBM to Make SOI Chips," Katherine Derbyshire, Semiconductor Online, August 18, 1998.
Ex. 1017	"SOI-CMOS Device Technology," Yasuhiro Fukuda, et al., Special Edition on 21st Century Solutions, OKI Technical Review 185, Vol. 68, March 2001, pp. 54-57.
Ex. 1018	"Impact of high-k gate stack material with metal gates on LF noise in n- and p-MOSFETs," P. Srinivasan et al., Microelectronic Engineering 80 (2005) 226–229.
Ex. 1019	U.S. 2004/0150045 A1 to Nonaka et al., published August 5, 2004 ("*Nonaka*").
Ex. 1020	U.S. Patent No. 6,498,371 B1 to Krishnan et al., published December 24, 2002 ("*Krishnan*").
Ex. 1021	U.S. Patent No. 6,933,569 B2 to Koh et al., published August 23, 2005 ("*Koh*").
Ex. 1022	"Temperature-Dependent Thermal Conductivity of Single-Crystal Silicon Layers in SOI Substrates," M. Asheghi et al., Transactions of the ASME, Journal of Heat Transfer, Vol. 120, February 1998, pp. 30-36.
Ex. 1023	"Current Mode Digital Gates for Mixed Mode Reprogrammable Integrated System," P. Pawlowski, Proceedings of the 1st IEEE International Conference on Circuits and Systems for Communications, 26-28 June, 2002, St. Petersburg State Polytechnic University Publishing House, 2002, pp. 178-181.
Ex. 1024	*Harbor Island Dynamic, LLC v. Samsung Electronics Co. Ltd. et al*, Case No. 2:24-cv-00140, Plaintiff's Infringement Contentions Cover Pleading (July 18, 2024)
Ex. 1025	*Harbor Island Dynamic, LLC v. Samsung Electronics Co. Ltd. et al*, Case No. 2:24-cv-00140, Dkt. No. 38, Docket Control Order (E.D. Tex. August 2, 2024)

I. Preliminary Statement

Petitioner Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. (collectively "Samsung"), requests *inter partes* review of U.S. Patent No. 7,745,886 (Ex. 1001), assigned to Patent Owner Harbor Island Dynamic, LLC ("HID"), and cancellation of claims 1-19.

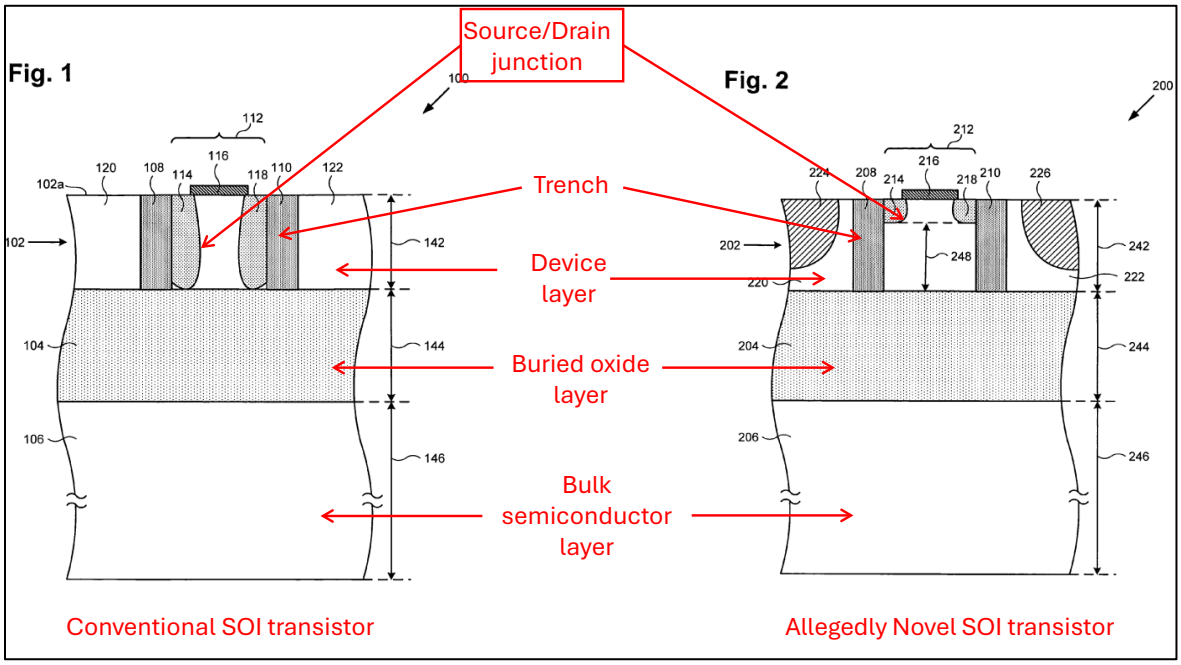
The challenged claims pertain to a semiconductor on insulator (SOI) switching circuit. The claimed switching circuit includes multiple cascaded transistors in a device layer. The transistors have source/drain junctions that do not contact a buried oxide (BOX) layer, and an isolation trench extends through the device layer and contacts a top surface of the BOX layer. However, transistors with this exact configuration were widely known before the alleged invention date. For instance, they were disclosed by both *Okashita* and *Yu*. The other limitations in the challenged claims merely describe common characteristics of a switching device as disclosed by *Burgener*. None of these references were considered by the Examiner.

As detailed below and in the supporting declaration of Scott Thompson, Ph.D., Thompson, ¶¶1-267, challenged claims 1-19 are unpatentable based on the grounds presented herein. The Board should institute review and cancel all claims.

II. The ’886 Patent

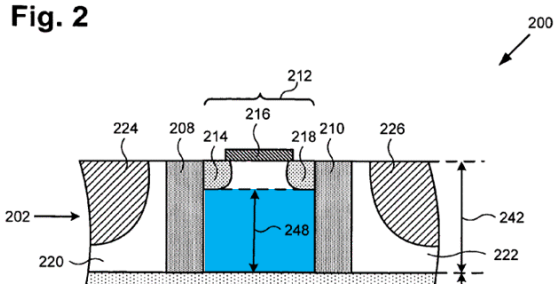
A. Specification

The ’886 patent acknowledges that transistors and isolating trenches have been conventionally fabricated on both bulk silicon wafers and SOI wafers. ’886 patent, 1:19-27. According to the ’886 patent, the transistors fabricated on a bulk silicon wafer face challenges with current leakage and interference between neighboring transistor devices, whereas the transistors fabricated on an SOI wafer benefit from better isolation due to the additional buried oxide layer. *Id*., 1:28-42. The ’886 patent further notes that to redesign circuits for fabrication on an SOI wafer increases cost and complexity. *Id*., 1:42-50; Thompson, ¶¶61-63. Below is a side-by-side comparison of a “conventional” transistor structure (Fig. 1) with the ’886 patent’s allegedly inventive transistor (Fig. 2).



’886 patent, Figs. 1-2[1]; 1:62-65, 2:29-4:64; Thompson, ¶66. Both transistors are fabricated on a SOI wafter (i.e., Figure 1’s layers 102, 104, 106 and Figure 2’s layers 202, 204, 206). Both transistors are also surrounded by trenches (i.e., 108 and 110 in Figure 1 and 208 and 210 in Figure 2) that extend through the device layer to the top surface of the buried oxide layer to form an isolated island in the device layer between the trenches. ’886 patent, 2:60-3:5, 4:37-47; Thompson, ¶67. Lastly, both transistors are also formed in the isolated island in the device layer. ’886 patent, 2:60-3:5, 4:37-47, Figs. 1, 2.

However, to address the concerns with the increased cost and complexity in fabricating transistors on a SOI wafer, the ’886 patent suggests adding “junction capacitance” to the transistors, as shown in Figure 2, which simply means to maintain an “intervening thickness 248” between the bottom surfaces of the source and drain and the top surface of the buried oxide layer as shown below. *Id.*, 4:11-36.



[1] All colored annotations in figures of this Petition have been added.

Id., Excerpt of Fig. 2. This "intervening thickness 248" forms a corresponding source/drain junction capacitance. *Id.*, 4:11-36; Thompson, ¶¶68-69. According to the '886 patent, Figure 1's conventional transistor has "no, or almost no" semiconductor material between the source and drain (114, 118) and the buried oxide layer (104), resulting in "low or non-existent" junction capacitance. '886 patent, 3:17-28; Thompson, ¶¶64-65. In contrast, the intervening thickness 248 in Figure 2 results in a junction capacitance similar to that of a transistor fabricated on a bulk silicon wafer, and thus, enables the use of existing design tools meant for bulk silicon transistors. '886 patent, 4:11-36; Thompson, ¶¶68-69. Notably, the presence of the ***additional device layer material*** between the bottom surfaces of the source and drain and the top surface of the buried oxide layer ***is the only distinction*** between the conventional transistor structure and the disclosed transistor structure and the only reason for the resulting source/drain junction capacitance. Thompson, ¶70; *see* '886 patent, 3:17-28, 4:11-18.

B. Prosecution History

The '886 patent was allowed in the first office action. Ex. 1003, 33-37. During prosecution, the Examiner did not consider any of the references used in this petition—*Okashita*, *Yu*, and *Burgener*. As discussed below, these references render the challenged claims unpatentable. Thompson, ¶71.

C. Claim Construction

The Board construes claims per *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. §42.100(b). Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Here, no terms need construction to resolve the controversy in this forum.[2]

III. Statement of Precise Relief Requested

A. Prior Art

The application that resulted in the ’886 patent was filed on September 29, 2008, claiming priority to Provisional Application No. 61/007,035, filed on December 10, 2007. Ex. 1003, 47-87. Thus, the earliest claimed priority date is December 10, 2007.

- *Okashita* (Ex. 1004, U.S. Patent No. 6,836,172), issued on December 28, 2004, is prior art under pre-AIA 35 U.S.C. §§102(a), 102(b), and 102(e).
- *Yu* (Ex. 1005, U.S. Patent No. 6,737,682, issued on May 18, 2004, is prior art under §§102(a), 102(b), and 102(e).

[2] Petitioner reserves the right to argue in an appropriate forum that certain limitations in the challenged claims are indefinite.

- *Burgener* (Ex. 1006, U.S. Patent Publication No. 2006/0270367), published on November 30, 2006, is prior art under §§102(a), 102(b), and 102(e).

B. Challenges

Ground	Challenged Claims	Basis	Prior Art
1	1, 2, 4, and 5	§102	*Okashita*
2	1-7	§103	*Okashita*
3	1-7	§103	*Okashita* and *Yu*
4	1-3	§102	*Yu*
5	1-19	§103	*Burgener* and *Okashita*
6	1-19	§103	*Burgener*, *Okashita*, and *Yu*

IV. Level of Ordinary Skill in the Art

A person of ordinary skill in the art ("POSITA") would have had at least a master's degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems and semiconductor dice. Additional relevant work experience can compensate for less education, and *vice versa*. Thompson, ¶¶105-107.

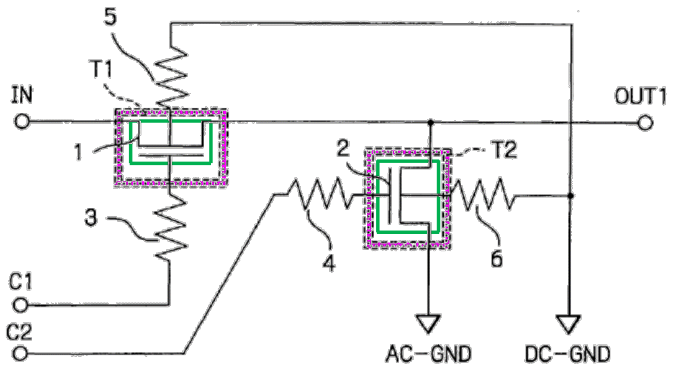
V. Claims 1-19 Are Unpatentable

A. Ground 1: Claims 1, 2, 4, and 5 Are Anticipated by *Okashita*

1. Overview of *Okashita*

Okashita discloses "a semiconductor switch apparatus" that is "used for switching the operation of an antenna circuit and a receiving and transmitting circuit" in a mobile telephone, as shown below. *Okashita*, 1:7-15, *see,* Figs. 7, 12, 16, 17, 19; Thompson, ¶¶75-76. *Okashita* is analogous art to the '886 patent since both are from the same field of endeavor. Thompson, ¶77. For example, both relate to a semiconductor switching circuit with cascaded transistors having an SOI configuration. *See Okashita*, 1:43-61, 9:27-12:44; '886 patent, 1:14-17, 7:25-31, 8:63-10:55.

Fig. 7

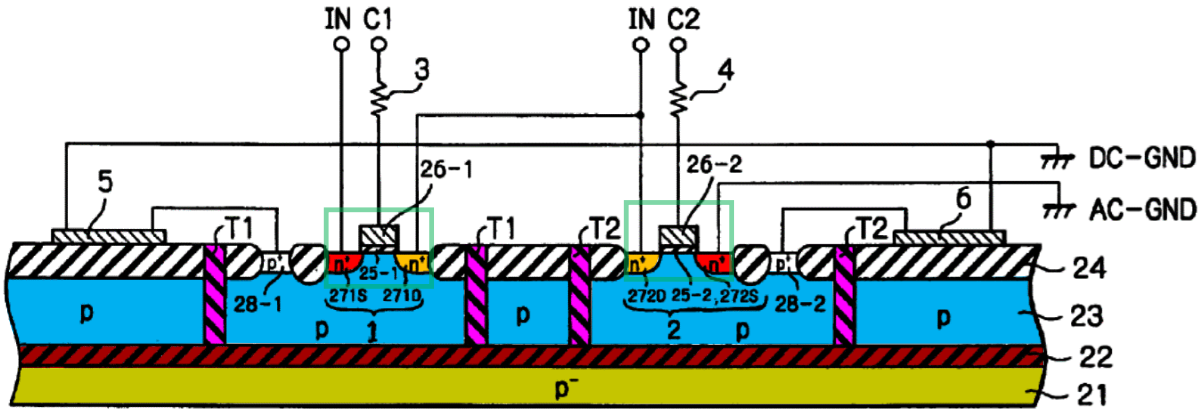


Okashita, Fig. 7. *Okashita*'s semiconductor switch apparatus includes a MOS transistor 1 that is connected to another MOS transistor 2, where the MOS

transistors 1, 2 are isolated by the insulating trenches T1, T2, respectively. *Okashita*, 5:22-40, 8:30-37; Thompson, ¶¶78-80.

Okashita's semiconductor switch apparatus (comprising the MOS transistors 1, 2) is fabricated using an SOI configuration, as shown below.

Fig. 9



Okashita, Fig. 9; Thompson, ¶¶78-79. *Okashita*'s SOI configuration comprises a p-type silicon layer 23 that is grown on a silicon oxide layer 22 that is formed on a monocrystalline silicon substrate 21. *Okashita*, 5:41-44; Thompson, ¶79. As such, the silicon oxide layer 22 is a buried oxide layer. Thompson, ¶79. As *Okashita* explains, the SOI configuration helps to suppress the leakage of radio frequency signals via the silicon substrate 21. *Okashita*, 6:1-7; Thompson, ¶¶80-81. Since the MOS Transistors 1, 2 are surrounded by trenches T1, T2, the leakage of radio frequency signals via the p-type silicon layer 23 is also suppressed. *Okashita*, 6:8-17; Thompson, ¶81.

Similar to the ’886 patent, *Okashita*’s Figure 9 also shows an intervening thickness of the silicon layer 23 separating the bottom surfaces of the MOS transistors 1 and 2’s sources (271S, 272S) and drains (271D, 272D) and the top surface of the buried oxide layer 22. *Okashita*, Fig. 9; *see also id.*, Figs. 11, 14, and 15; Thompson, ¶¶82-83. As was well known in the field, the presence of the intervening silicon layer results in these transistors having a source/drain junction capacitance. Thompson, ¶¶47-51, 84-88.

2. Independent Claim 1

a. [1pre]: “A switching circuit comprising:”

To the extent the preamble is limiting, *Okashita* discloses a “switching circuit” because *Okashita*’s “semiconductor switch apparatus” is “used for switching the operation of an antenna circuit and a receiving and transmitting circuit.” *Okashita*, 1:7-15; Thompson, ¶111.

b. [1a]: “a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;”

Okashita discloses this limitation because *Okashita*’s MOS transistors 1, 2 are fabricated in a p-type silicon layer that is over a silicon oxide layer and a monocrystalline silicon substrate, as shown below. Thompson, ¶¶112-117; *see* Ex. 1011, 21-24.

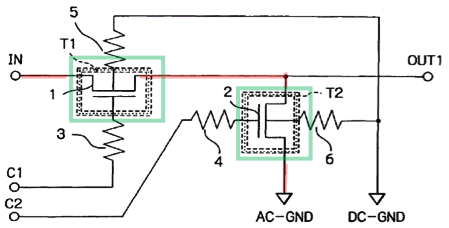
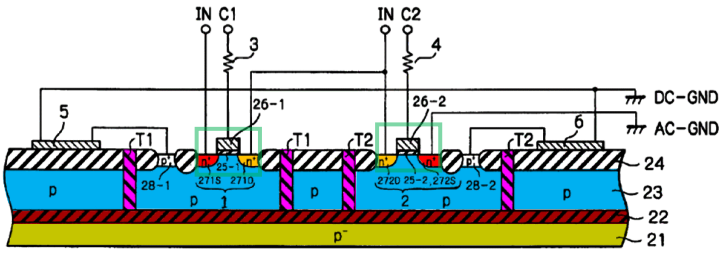


Fig. 7

Fig. 9



Okashita, Figs. 7, 9. Because *Okashita*'s MOS transistors 1, 2 are fabricated in the p-type silicon layer, the p-type silicon layer is the claimed device layer that is situated over a silicon oxide layer 22 and a semiconductor substrate. *Okashita*, 9:36-42, 5:40-63; Thompson, ¶¶113-114.

Moreover, *Okashita*'s MOS transistors 1, 2 are "cascaded"[3] transistors. Thompson, ¶¶115-116; Ex. 1007, 5 ("Cascaded transistors" refer to transistors "arranged in a series or in a succession of stages so that each stage derives from or acts upon the product of the preceding."); Ex. 1011, 21-24 (providing multiple examples of cascaded transistors where each subsequent transistor operates on the output of the preceding one). As shown in Figure 7, *Okashita*'s MOS transistors 1, 2 are connected in series at least from the input terminal (IN) to the AC ground terminal (AC-GND), such that the MOS transistor 2 acts upon the output of the

[3] In the '886 patent, transistors that are "coupled in series" are considered "cascaded." '886 patent, 6:50-51.

MOS transistor 1 when a threshold voltage (V_{th}) is exceeded at the MOS transistor 2. Thompson, ¶116; *Okashita*, 7:7-17. Accordingly, at least in this scenario, the MOS transistor 2 receives, and acts upon, the output of the MOS transistor 1 and, thus, MOS transistors 1, 2 are "cascaded." Thompson, ¶¶116-117.

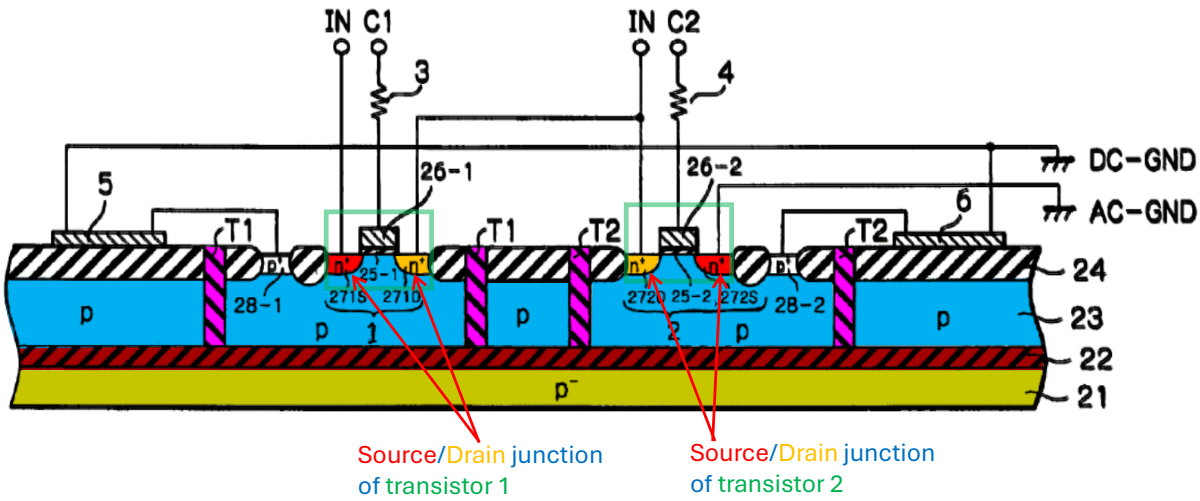
c. [1b(i)]: "each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer,"

Okashita discloses this limitation because the MOS transistors 1, 2's source/drain junctions do not contact the silicon oxide layer 22. Thompson, ¶¶118-122.

In a transistor, the source/drain junction refers to the interface between the source and drain regions and the silicon layer on which the source and drain are formed. Thompson, ¶119; *see* Ex. 1011, 10 ("pn junctions [] are formed by the drain-bulk and source-bulk interfaces in a MOSFET"), 11 (Fig. 1.36); *see* Ex. 1010, 43.

In *Okashita*, the source/drain junction of the MOS transistor 1 is the interface between the regions 271S, 271D and the p-type silicon layer 23, and the source/drain junction of the MOS transistor 2 is the interface between the regions 272S, 272D and the p-type silicon layer 23. Thompson, ¶¶119-120, *see Okashita*, 5:55-63.

Fig. 9



Okashita, Fig. 9. As further shown in Figure 9,[4] none of the source/drain junctions contact the silicon oxide layer 22, and, instead, there is an intervening layer of silicon material (layer 23) between the source/drain junctions of the MOS transistors 1, 2 and the top surface of the silicon oxide layer 22. *Id.*, Fig. 9; *see also id.*, 6:43-67, Figs. 11, 14, 15; Thompson, ¶¶120-122. Because the claim merely

[4] Features clearly shown in prior art drawings can be relied on for anticipation. *In re Mraz*, 455 F.2d 1069, 1072 (C.C.P.A. 1972); *Ex parte Jurek*, Appeal 2018-006215, p. 6 (P.T.A.B. Apr. 17, 2019); *see also Current Lighting Solutions LLC v. Jiaxing Super Lighting Electric Appliance Co.,* IPR2023-00269, Paper 18 at 22-26 (P.T.A.B. Aug. 16, 2023). A drawing teaches all that it reasonably discloses and suggests to a POSITA. *In re Aslanian*, 590 F.2d 911, 914 (C.C.P.A. 1979).

recites a "source/drain junction that does not contact said buried oxide layer" and *Okashita*'s Figure 9 clearly shows that the source/drain junctions of the MOS transistors 1, 2 do not contact the silicon oxide layer 22, *Okashita* discloses this limitation. Thompson, ¶122.

d. [1b(ii)]: "thereby forming a source/drain junction capacitance;"

Okashita's cascaded MOS transistors 1, 2 have a source/drain junction that forms a source/drain junction capacitance. Thompson, ¶¶123-127. In particular, a POSITA would have recognized that the presence of the intervening silicon layer 23 between the bottom surfaces of *Okashita*'s sources (271S and 272S) and drains (271D and 272D) of the MOS transistors 1, 2 and the top surface of the silicon oxide layer 22 (*see supra* §V.A.2.c; *see Okashita*, Fig. 9) results in the source/drain junctions of *Okashita*'s transistors 1 and 2 having a source/drain junction capacitance. Thompson, ¶¶123-124. *See, e.g.*, *Acoustic Tech., Inc. v. Itron Networked Sols. Inc.*, 949 F.3d 1366 (Fed. Cir. 2020) (affirming anticipation ground as supported by expert testimony of what a skilled artisan would have recognized the prior art reference as disclosing); *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376 (Fed. Cir. 2015) (finding "a reference can anticipate a claim … if a personal of skill in the art, reading the reference, would 'at once envisage' the claimed arrangement or combination").

Indeed, consistent with the teachings of the ’886 patent,[5] it is well known that including a silicon layer between the bottom of the source and drain of a transistor and the top of the buried oxide layer, such “structure has larger junction capacitance than the normal SOI structure.” Thompson, ¶124; Ex. 1013, 25-26; Ex. 1014, 3, 5. This is shown below:

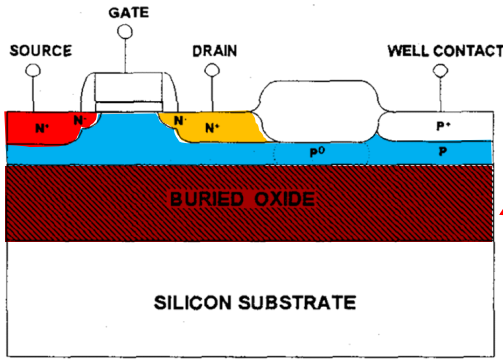


Fig. 1. A cross-sectional illustration of BC-SOI MOSFET structure.

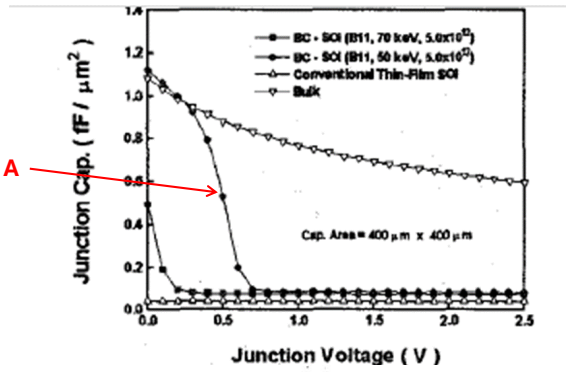


Fig. 11. A n+ junction capacitance characteristics of BC-SOI MOSFET structure compared with that of bulk-silicon MOSFET.

[5] As the ’886 patent notes, when there is little to no semiconductor material in the device layer between the source and drain and the buried oxide layer, there is minimal or no semiconductor junction to create a capacitive load, which results in low or non-existent junction capacitance. ’886 patent, 3:17-23. Conversely, when an intervening device layer remains between the source and drain and the buried oxide layer, a semiconductor junction with associated source/drain junction capacitance is formed within the device layer. *Id*. 4:11-18, 5:63-65 (“This remaining semiconductor would result in source/drain junction capacitance[.]”).

Ex. 1014, Figs. 1, 11. In the above figures, the addition of an intervening silicon layer results in a source/drain junction capacitance (Figure 11, curve A) that is greater than a transistor fabricated on a conventional thin-film SOI structure. Thompson, ¶¶47-51, 125-126; *see* Ex. 1014, 2-5.

The junction capacitance created by the additional silicon layer is also seen in the gate delay time, such that the bigger the junction capacitance, the longer the delay time. Thompson, ¶¶51, 125-126; *see* Ex. 1012, 2, 4; *see* Ex. 1013, 26 (explaining that reducing the junction capacitance allows circuits to operate at higher speed). The below figure shows the gate delay time—and by inference the source/drain junction capacitance—between a conventional SOI structure (curve ○), a bulk semiconductor structure (curve △), and a structure having an intervening silicon film of 75 mm (i.e., structure (a) in Fig. 48(a); curve ■). Thompson, ¶50.

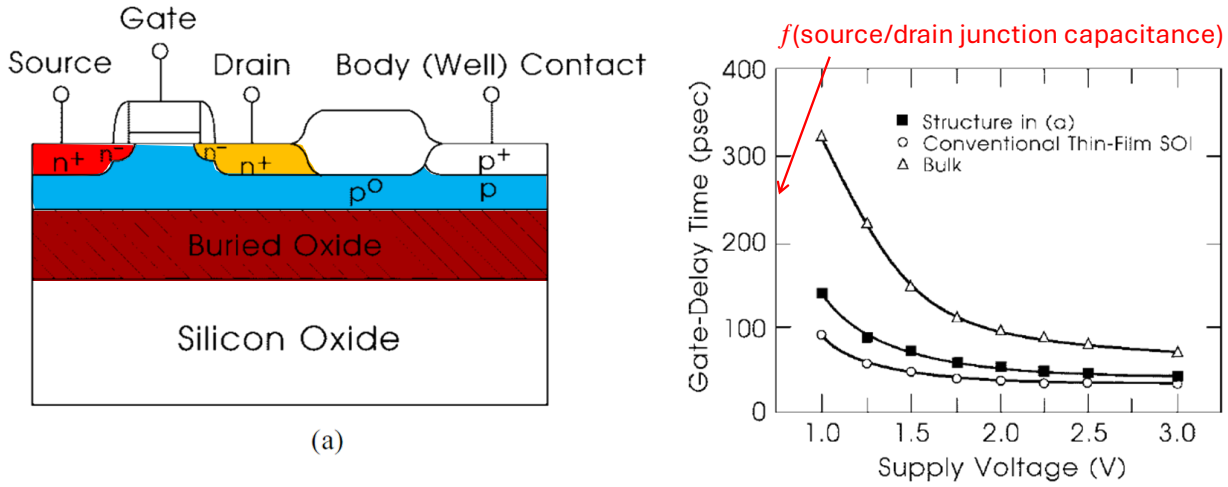


Fig. 48

Ex. 1013, 26. As shown, the structure with a thin silicon film has an increased gate-delay time (curve ■) than that of a conventional SOI structure (curve ○), corresponding to an increase in the source/drain junction capacitance. *Id*.

Thus, the intervening layer of the silicon material (layer 23) between the source/drain junctions of *Okashita*'s MOS transistors 1, 2 and the top surface of the silicon oxide layer 22 (*see supra* §V.A.2.c) results in these transistors having a source/drain junction capacitance. Thompson, ¶¶123-127.

e. [1c(i)]: "at least one trench extending through said device layer and contacting a top surface of said buried oxide layer,"

Okashita discloses this limitation because *Okashita*'s trenches T1, T2 extend through the silicon layer 23 to contact the top surface of silicon oxide layer 22,[6] as illustrated in Figure 9 below. *See Okashita*, Fig. 9; Thompson, ¶¶128-132.

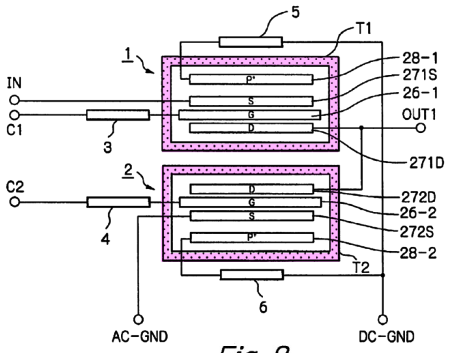


Fig. 8

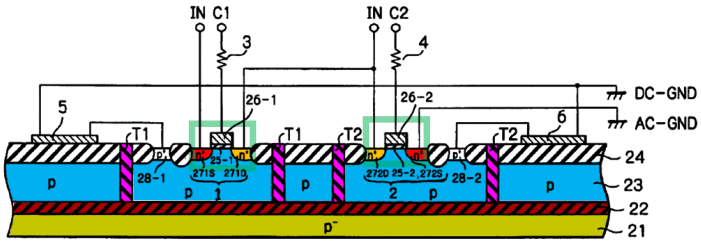
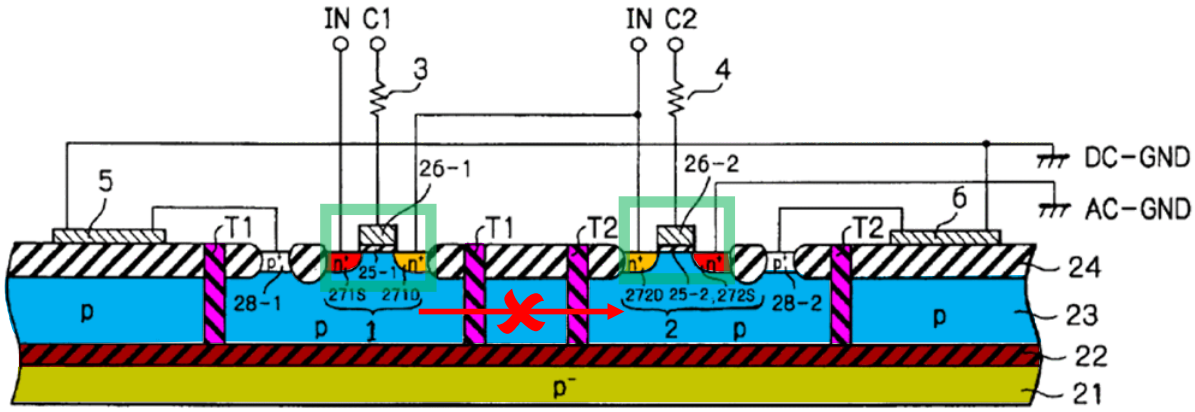


Fig. 9

[6] This is clearly illustrated in *Okashita*'s Fig. 9. *See* FN3.

Okashita, Figs. 8, 9. *Okashita*'s trenches T1, T2 are formed using a photolithography process and a plasma dry etching process to etch "grooves" into the field silicon oxide layer 24 and the silicon layer 23. *Okashita*, 5:46-54; Thompson, ¶129. After the dry etching process, an insulating silicon oxide layer is then deposited into the etched cavities to form the trenches T1, T2. Thompson, ¶¶129-130; *see Okashita*, 5:46-54. A POSITA reading *Okashita* would have understood that *Okashita*'s trenches T1, T2 contact the top surface of silicon oxide layer 22 because the trenches T1, T2 not only completely surround the respective MOS transistors 1, 2 (*Okashita*, 5:55-63), they also suppress any leakage of radio frequency signals through the silicon layer 23, as shown by the "×" mark in the figure below.

Fig. 9



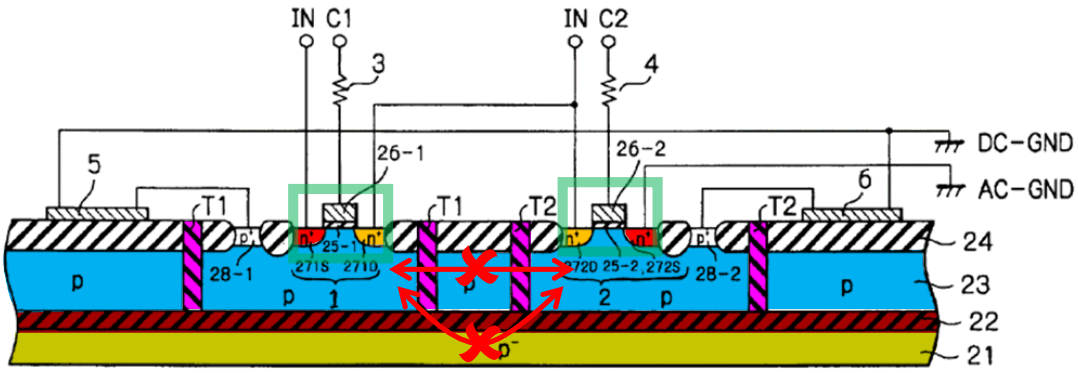
Id., Fig. 9, 6:1-16; Thompson, ¶¶129-130. Because the trenches T1, T2 prevent leakage of signals through the silicon layer 23, a POSITA reading *Okashita* would

have understood that the trenches T1, T2 contact the top surface of the silicon oxide layer 22 to prevent any signal leakage through any gap that may otherwise exist between the trenches T1 and T2 and the silicon oxide layer 22. Thompson, ¶¶131-132.

f. [1c(ii)]: "thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer."

Okashita discloses that the "MOS transistor 1 is isolated by a trench insulating layer T1 from the other elements, and [] MOS transistor 2 is isolated by a trench insulating layer T2 from the other elements." *Okashita,* 5:29-32. *Okashita* further explains that, because the trenches T1, T2 extend through the silicon layer 23 and contact a top surface of the silicon oxide layer 22, leakage of electrical signals between the MOS transistor 1 and MOS transistor 2 through the silicon layer 23 and through the silicon substrate 21 below the silicon oxide layer 22 is suppressed. *Okashita*, 6:1-16; Thompson, ¶¶133-135; *supra* §V.A.2.e.

Fig. 9

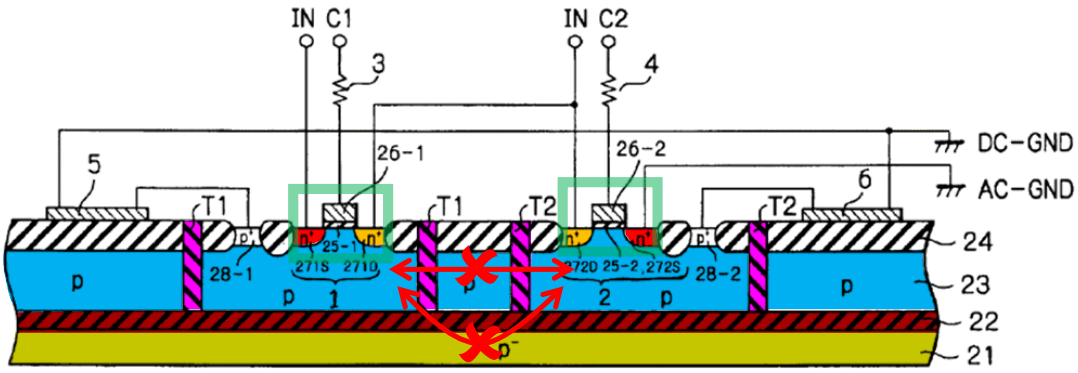


Okashita, Fig. 9. As Dr. Thompson explains, the trench T1 electrically isolates the MOS transistor 1 from other elements (including the MOS transistor 2) of the switch apparatus, and the trench T2 electrically isolates the MOS transistor 2 from other elements (including the MOS transistor 1). Thompson, ¶¶134-135. This isolation prevents signals from these other elements from reaching the silicon layer 23 within trench T1 around the MOS transistor 1 (and within trench T2 around the MOS transistor 2) and inducing voltage and current fluctuations in the silicon layer 23. Thompson, ¶135; *see* Ex. 1023, 3.

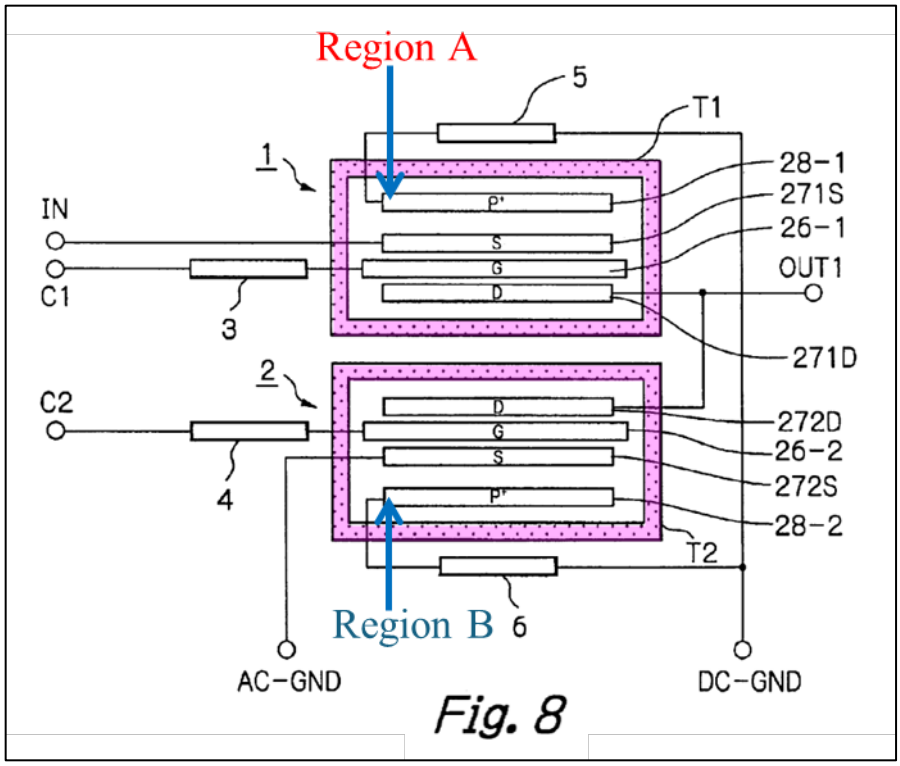
Indeed, this conclusion is consistent with the teachings of the ’886 patent.[7] Similar to the transistors of the ’886 patent, *Okashita*’s MOS transistors 1, 2 are fabricated in islands that are surrounded by trenches T1, T2, which electrically isolate the MOS transistors 1, 2 from other elements of the switch apparatus, as shown below. *Okashita*, 5:29-32; Thompson, ¶¶63, 66-67, 136.

[7] As the ’886 patent explains, when a transistor is fabricated in an island surrounded by trenches that extend through the device layer and contact the buried oxide layer, the transistor “is electrically isolated from neighboring islands … by trenches … and buried oxide layer … [thereby allowing the transistor] to experience positive and negative voltage excursions without affecting neighboring devices[.]” ’886 patent, 2:65-3:11, *see also* 6:10-15. As a result of such electrical isolation, the switching circuit “exhibit[s] reduced voltage and current fluctuations in [the] device layer.” *Id*., 6:33-42; Thompson, ¶136.

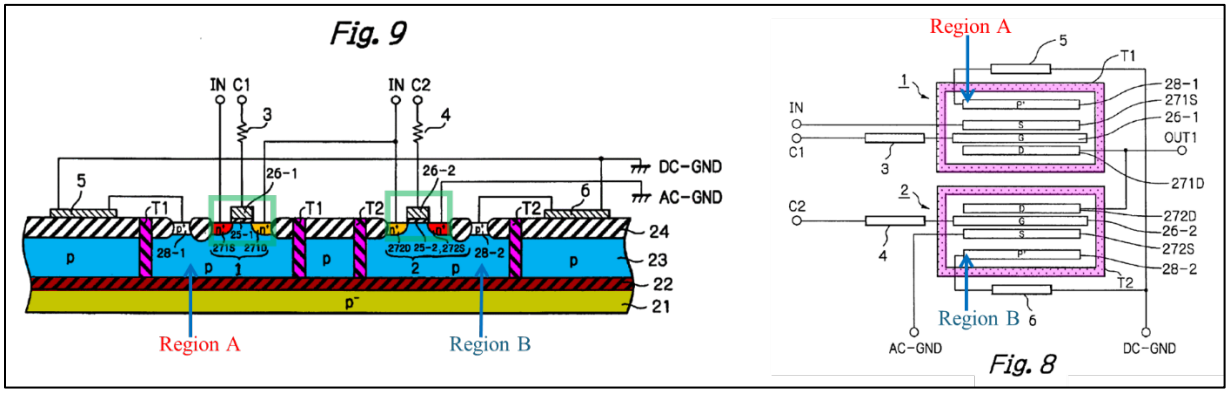
Fig. 9



Okashita, Fig. 9. Without such electrical isolations, any leakages of electrical signals from the MOS transistor 1 (Region A in the below Figures 8 and 9) to the MOS transistor 2 (Region B) would cause the voltage and current in the MOS transistor 2 to change or fluctuate. *Okashita*, 3:11-16, 7:7-12; Thompson, ¶¶137-139.



Okashita, Fig. 8. Thus, electrically isolating Region A from Region B in *Okashita* using trenches T1 and T2 suppresses any leakage of electrical signals and, thereby, reduces the resulting voltage and current fluctuations (or electrical noise) in the silicon layer 23 of Region B. *Okashita*, 5:29-32; Thompson, ¶¶138-139; *see* Ex. 1010, 187-189.



Okashita, Figs. 8, 9.

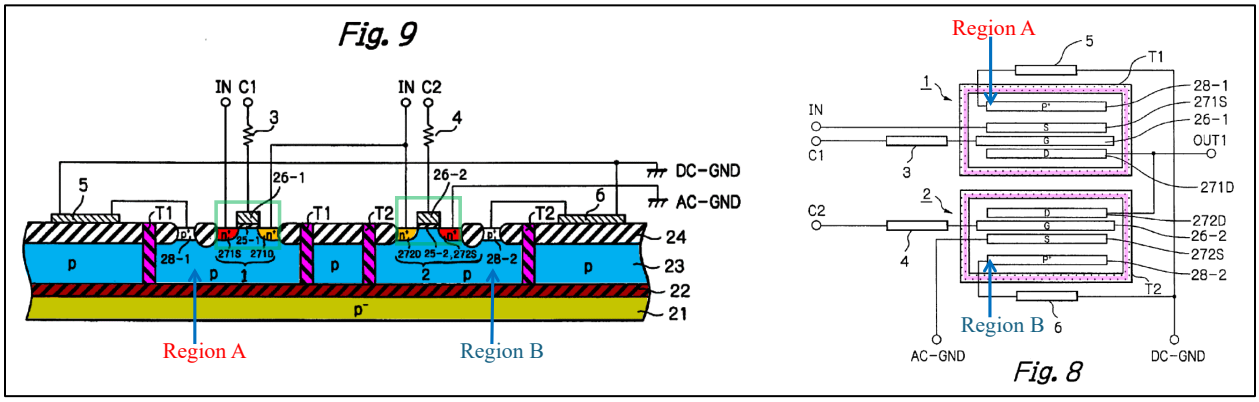
Because *Okashita*'s MOS transistors 1, 2 are fabricated in isolated islands that are surrounded by trenches T1 and T2 that extend through the silicon layer 23 to contact the top surface of the silicon oxide layer 22, they are electrically isolated so as to reduce voltage and current fluctuations in silicon layer 23. Thompson, ¶¶138-139; *see* Ex. 1010, 187-189.

3. Claim 2

a. [2]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer."

Okashita discloses the additional limitation of claim 2. Thompson, ¶¶140-141.

As explained *supra* with reference to limitations [1c(i)] and 1[c(ii)], *Okashita*'s MOS transistor 1 is formed in "an area" (i.e., Region A) that is "surrounded by" trench T1 and "isolated" from the other elements of the switch apparatus. *Okashita*, 5:29-32, 5:55-63; Thompson, ¶141.



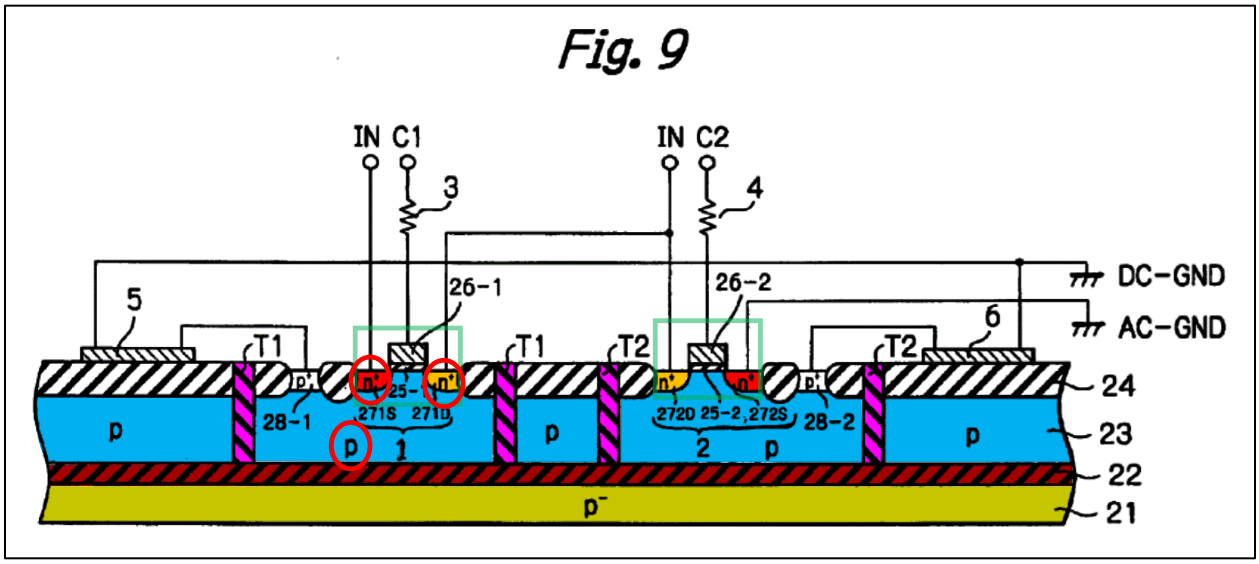
Okashita, Figs. 8, 9. Thus, the MOS transistor 1 is situated within an isolated island (i.e., Region A) in the silicon layer 23, where the isolated island is defined by the side walls of trench T1 and the top surface of silicon oxide layer 22. Thompson, ¶141.

4. Claim 4

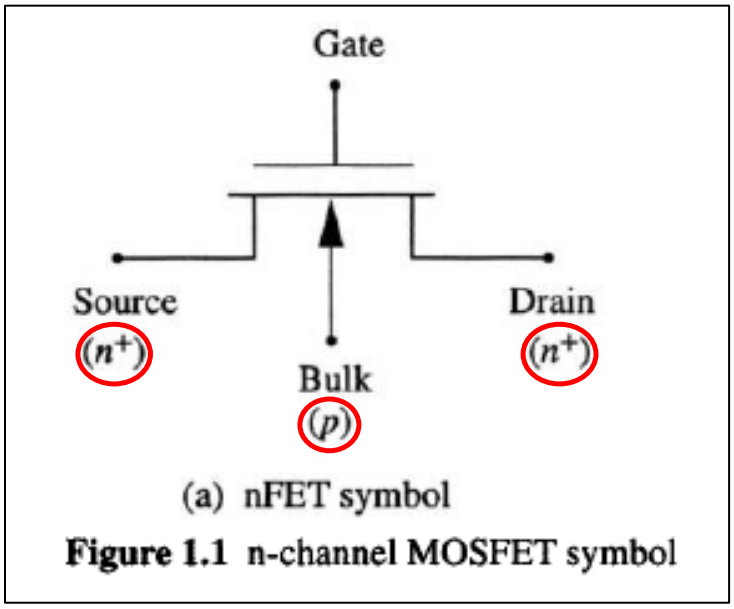
a. [4]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is an NFET with a gate driven by a switch control signal in a wireless communications device."

Okashita discloses the additional limitation of claim 4. Thompson, ¶¶142-146.

Okashita's MOS transistors 1, 2 are NFETs. Thompson, ¶¶142-143. *Okashita*'s MOS transistors 1, 2 are composed of a p-type silicon body (p-type silicon layer 23) with n+-type source 271S and drain 271D. *Okashita*, 5:40-43, 55-63, Fig. 9.



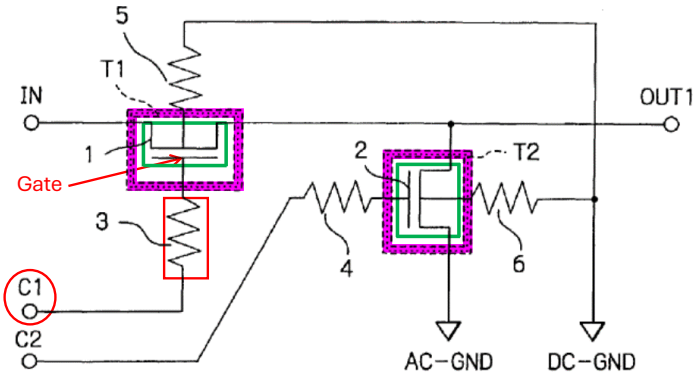
Okashita, Fig. 9. A POSITA would have recognized this configuration as an NMOSFET (or NFET). Thompson, ¶¶142-143; Ex. 1011, 7-8; Ex. 1010, 36-37; Ex. 1012, 2 ("The NFET starts with an underlying body or substrate of p-type silicon," with "[t]wo side by side regions in the top of the substrate [that] are changed to n-type silicon[.]"). Moreover, as illustrated below, an nFET has a p-type body with n+-type source and drain, which is identical with *Okashita*'s MOS transistors 1, 2.



Ex. 1011, 7; *see Okashita*, 5:55-59, Fig. 9; Thompson, ¶143.

Moreover, the MOS transistor 1's gate is driven by a switch control signal C1. Thompson, ¶¶144-145; *Okashita*, 7:7-12. As *Okashita* explains, "the control voltages applied to the control terminals C1 and C2" control whether the MOS transistors 1 and 2 are turned ON or OFF. *Okashita*, 7:7-12.

Fig. 7



Okashita, Fig. 7. Thus, MOS transistor 1 is driven by control voltages applied to control terminal C1 connected to its gate. Thompson, ¶145.

Lastly, *Okashita*'s switch apparatus may be used in "a mobile communication apparatus such as a mobile telephone apparatus … for switching the operation of an antenna circuit and a receiving and transmitting circuit." *Okashita*, 1:11-15; Thompson, ¶146. *Okashita*'s MOS transistor 1 is an NFET with its gate driven by a switch control signal in a wireless communications device.

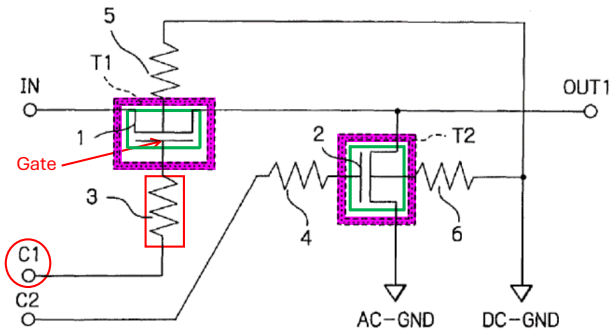
5. Claim 5

a. [5]: "The switching circuit of claim 4, wherein said switch control signal drives said gate of said NFET through at least one resistor."

Okashita discloses the additional limitation of claim 5. Thompson, ¶¶147-148.

Okashita's control terminal C1 is connected to the gate of the MOS transistor 1 through a gate protection resistor 3, as shown. *Okashita,* 5:64-67, Figs. 7-9; Thompson, ¶¶147-148.

Fig. 7



Okashita, Fig. 7. Therefore, the switch control signal drives the gate of transistor 1 through at least resistor 3. Thompson, ¶148.

B. Ground 2: Claims 1-7 Are Obvious over *Okashita*

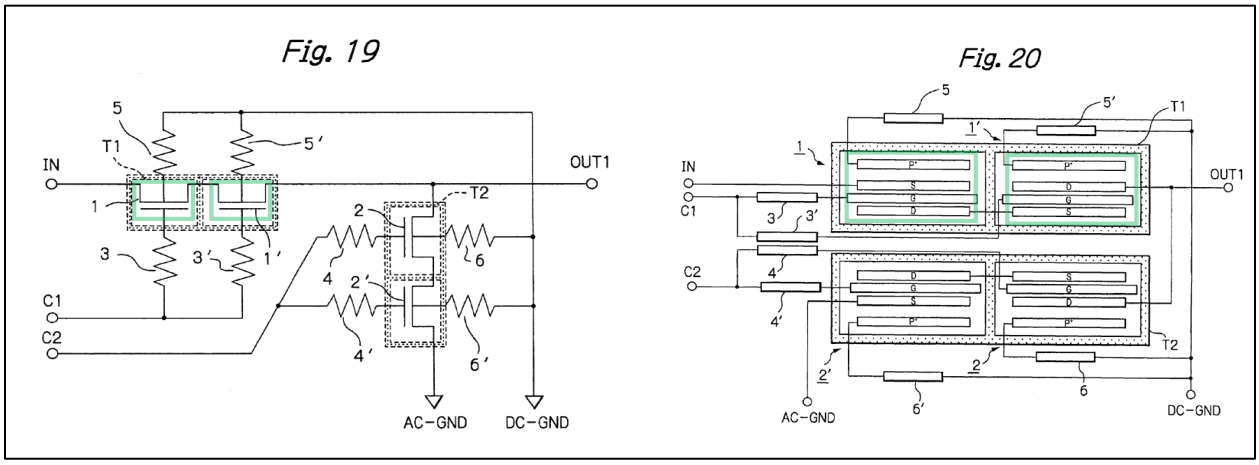
1. Independent Claim 1

a. [1pre]: "A switching circuit comprising:"

To the extent the preamble is limiting, *Okashita* discloses this limitation for the same reasons as stated for [1pre] of ground 1. Thompson, ¶149.

b. [1a]: "a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;"

Okashita teaches this limitation because *Okashita*'s switch apparatus may include a plurality of transistors connected in series. Thompson, ¶¶150-160. In Figures 19-20, a MOS transistor 1′ is "connected in series" to the "MOS transistor 1 of Fig. 7[.]" *Okashita*, 8:30-37.



Okashita, Figs. 19 and 20; *see also 8*:65-67 ("[T]hree or more series MOS transistors can be connected in series[.]"), 2:19-21, 5:36-40, Figs. 7-9; *see also* '886 patent, 6:50-51. *Okashita*'s MOS transistors 1 and 1′ are, thus, cascaded transistors. Thompson, ¶¶150-151.

As explained in [1a] of ground 1, *Okashita*'s MOS transistor 1 is fabricated in a silicon layer 23 over a silicon oxide layer 22 and silicon substrate 21. *Okashita*, 5:41-49, 55-63; Thompson, ¶152. A POSITA would have recognized that the MOS transistor 1′, which is connected in series to the MOS transistor 1 in Figure 7, would have also been fabricated in exactly the same way as the MOS transistor 1. Thompson, ¶¶153-155.

A POSITA would have recognized that the MOS transistor 1 would have also been fabricated in the silicon layer 23. Thompson, ¶¶153-154; *Okashita*, 10:43-57 ("[A] plurality of series MOS transistors formed within a first region of [a] semiconductor layer [that is formed on an insulating layer on a semiconductor

substrate] and connected in series[.]"). It would have been obvious that both of *Okashita*'s MOS transistors 1 and 1′ would have been fabricated with the SOI configuration of Figure 7. *Okashita*, Abstract, 1:47-58, 5:41-44, 6:1; Thompson, ¶¶155-160; *see* Ex. 1010, 36-38 (showing the simultaneous fabrication of multiple transistors on a substrate); Ex. 1016, 1 ("SOI fabricates circuits on a thin layer of silicon on top of an insulator."); Ex. 1017, 1 ("The term SOI means Silicon On Insulator structure, which consists of devices on silicon thin film (SOI layers) that exists on insulating film."). Since *Okashita* teaches the fabrication of the MOS transistor 1 in a silicon layer 23, a POSITA would have had a reasonable expectation of success in fabricating the MOS transistor 1′ also in a silicon layer 23. Thompson, ¶159.

Moreover, it would have been obvious that both MOS transistors 1′ and MOS transistor 1 will have a similar geometry—with an intervening silicon layer separating their source/drain junctions from the top surface of the silicon oxide layer (as shown in Figure 9)—for at least three reasons. Thompson, ¶155.

First, a POSITA would have been motivated to maintain a consistent geometry for the adjacently located MOS transistors 1, 1′ (*see Okashita*, Fig. 20) because doing so would simplify the manufacturing process by enabling the same processes (such as doping, etching, and metal deposition) to be used to fabricate

both transistors at the same time. Thompson, ¶156; *see* Ex. 1011, 12-17. A POSITA would have been motivated to ensure uniform device geometry for the MOS transistors 1, 1′ to enable the use of the same "design methodology," "device models," and "design kits" during their design and fabrication, and thus significantly reduce manufacturing and integration complexity and costs. Thompson, ¶156;'886 patent, 3:24-35; 1:43-47.

Second, having consistent geometry ensures similar electrical characteristics (such as threshold voltage, junction capacitance, gate delay time, etc.) between the transistors. Thompson, ¶157; *see* Ex. 1013, 25-29; Ex. 1014, 2-5. A POSITA would have been motivated to keep consistent geometry for both MOS transistors 1, 1′ to ensure that both transistors would have similar electrical characteristics. Thompson, ¶157. Otherwise, there may be uneven threshold voltages between the two MOS transistors 1', 1 due to a lack of uniformity in their geometries. Thompson, ¶157; *see* Ex. 1013 at 29 ("SOI MOSFET's are typically designed to have higher threshold voltage than their bulk counterparts."). Such variations in threshold voltages (V_{Th}) would cause discrepancies in the switching behavior of the MOS transistors 1 and 1′ during the operation of the switch apparatus. Thompson, ¶157; *see* Ex. 1013 at 29 ("V_T variation has been shown to cause 5-6% frequency-dependent delay variation in simple circuits[.]"). To avoid this, a POSITA would

have been motivated to keep consistent geometry between the transistors to ensure similar electrical characteristics. Thompson, ¶157.

Third, having consistent geometry also ensures similar thermal characteristics (such as operating temperature, thermal resistance, etc.) between the transistors. Thompson, ¶158. The silicon dioxide used in the buried oxide layer generally has lower thermal conductivity compared to silicon in the bulk silicon layer. Thompson, ¶158; Ex. 1013, 27 (explaining that the self-heating in SOI poses a design challenge due to silicon dioxide's thermal conductivity being about 100 times lower than silicon's); Ex. 1022, 1 (explaining that the buried silicon dioxide results in a large thermal resistance between the device and the substrate causing a major problem for SOI transistors). This reduction in thermal conductivity increases localized temperature, which further impacts circuit performance and reliability. Thompson, ¶158; Ex. 1010, 60; Ex. 1013, 28 (explaining that channel temperature rise in SOI devices can be up to ten times higher than in bulk silicon devices). Thus, uneven geometry would cause the MOS transistors 1, 1' to operate at different temperatures. Thompson, ¶158. To avoid this, a POSITA would have been motivated to keep consistent geometry between the transistors to ensure similar thermal characteristics. *Id*.

Accordingly, a POSITA would have recognized that differences in electrical and thermal characteristics between the serially connected MOS transistors 1, 1′

could cause signal delays and other errors, thereby motivating the POSITA to maintain consistent geometry for the two MOS transistors 1, 1'. Thompson, ¶159; Ex. 1010, 75 ("two devices [] have different electrical properties due to the devices being at different temperatures"), *see also id*. 34, 52-53, 59-60, 140, 155-156. Moreover, fabricating the MOS transistor 1' with the same geometry as the MOS transistor 1 to have the intervening silicon layer would yield entirely predictable results for a POSITA, and a POSITA would have thus had a reasonable expectation of success in doing so. Thompson, ¶159. Therefore, it would have been obvious that the source/drain junction of the MOS transistor 1′ would have been also fabricated in exactly the same way as the MOS transistor 1 so as not to contact the silicon oxide layer. Thompson, ¶160. Accordingly, it would have been obvious that *Okashita*'s MOS transistors 1 and 1′ are fabricated in a silicon layer situated over a silicon oxide layer and a monocrystalline silicon substrate. Thompson, ¶¶152-160.

c. [1b(i)]: "each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer,"

Okashita teaches this limitation. Thompson, ¶¶161-162. As explained in [1b(i)] of Ground 1, *Okashita*'s MOS transistor 1's source/drain junction does not contact the silicon oxide layer 22. Thompson, ¶161. It would have been obvious that the MOS transistor 1′, which is connected in series with the earlier MOS

transistor 1, would also have a source/drain junction that does not contact the silicon oxide layer, as explained in [1(a)], *supra*. Thompson, ¶162; *Okashita*, Fig. 9.

d. [1b(ii)]: "thereby forming a source/drain junction capacitance;"

Okashita teaches this limitation. For the same reasons that the structure of *Okashita* in ground 1 forms a source/drain junction capacitance, the corresponding structure in this ground, namely source/drain junctions of the MOS transistors, 1, 1' with the intervening silicon layer, also forms a source/drain junction capacitance. Thompson, ¶163.

e. [1c(i)]: "at least one trench extending through said device layer and contacting a top surface of said buried oxide layer,"

Okashita teaches this limitation for the same reasons as stated in ground 1. *Okashita*, 8:30-37; Thompson, ¶164.

f. [1c(ii)]: "thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer."

Okashita teaches this limitation for the same reasons as stated in ground 1. Thompson, ¶165.

2. Claim 2

a. [2]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer."

Okashita teaches the additional limitation of claim 2 for the same reasons as stated in ground 1 for claim 2. Thompson, ¶166. The MOS transistor 1 of the cascaded pair of MOS transistors 1, 1′ is situated within an isolated island in the silicon layer. Thompson, ¶166; *Okashita*, 8:30-37, 47-54.

3. Claim 3

a. [3]: "The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer."

Okashita teaches the additional limitation of claim 3. Thompson, ¶¶167-168. For example, *Okashita* teaches (1) a plurality of MOS transistors that is "connected in series" and "formed within a first region of" the silicon layer and (2) a trench that surrounds the MOS transistors. *Okashita*, 10:43-67; *supra* §§V.B.1.e-V.B.1.f. A POSITA reading *Okashita* would have understood that the trench T1 surrounding the plurality of MOS transistors 1, 1' effectively places these MOS transistors within an isolated "first region" in the silicon layer to minimize radio frequency signal leakage from, and to, the first region. Thompson, ¶167, *See Okashita*, 8:47-54, 9:21-25, Figs. 19-20.

To the extent Patent Owner contends otherwise, a POSITA would have recognized that situating both MOS transistors 1, 1' within the same isolated region, as *Okashita* teaches, ensures consistent performance characteristics among the transistors. Thompson, ¶168; Ex. 1010, 75; Ex. 1020, 3:22-59, 1:47-63, Figs. 1-2B (A pair of SOI transistors are formed within an isolated island, which is surrounded by an isolation trench, to ensure consistent switching rates for both transistors). Locating multiple transistors in an isolated region provides at least two benefits: better tracking of thermal temperature and consistent switching rate. Thompson, ¶168; Ex. 1010, 75; Ex. 1020, 3:22-59, 1:47-63, Figs. 1-2B. Moreover, it was well known in the art to situate multiple transistors in the same isolated region surrounded by an insulating trench to ensure that these transistors have consistent performance characteristics. Ex. 1021, Fig. 28A, 16:15-57, 13:5-42. Thompson, ¶¶52-60. A POSITA would have been motivated to situate the MOS transistor 1' within the same isolated island with the MOS transistor 1 to ensure consistent electrical performance and reliability. Thompson, ¶168; *see* Ex. 1010, 75-77; Ex. 1020, 3:22-59, 1:47-63, Figs. 1-2B. And a POSITA would have had a reasonable expectation of success in doing so. Thompson, ¶168. Such an approach was standard practice in the field and would have been no more than applying a known technique to a known device to produce predictable results. *Id*.

4. Claim 4

a. [4]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is an NFET with a gate driven by a switch control signal in a wireless communications device."

Okashita teaches the additional limitation of claim 4 for the same reasons as stated in ground 1 for claim 4. Thompson, ¶169.

5. Claim 5

a. [5]: "The switching circuit of claim 4, wherein said switch control signal drives said gate of said NFET through at least one resistor."

Okashita teaches the additional limitation of claim 5 for the same reasons as stated in ground 1 for claim 5. Thompson, ¶170.

6. Claim 6

a. [6]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is a PFET with a gate driven by a switch control signal in a wireless communications device."

Okashita teaches the additional limitation of claim 6. Thompson, ¶¶171-174. Although *Okashita*'s MOS transistor 1 in Figure 19 is an NFET, it would have been obvious to implement the MOS transistor 1 as a PFET instead, because *Okashita* teaches using both "p-channel MOS transistors" and "N-channel MOS transistors." *Okashita*, 7:30-33, Fig. 16; Thompson, ¶¶172-173. It would have also been obvious to substitute the NFET with a PFET because there are two basic

types of field-effect transistor (FET) (e.g., PFET and NFET). Thompson, ¶¶172-173; Ex. 1008, 20 (explaining that there two types of MOSFETS—n-channel MOSFETS and p-channel MOSFETS); Ex. 1012, 2 (PFET "starts with an n-type substrate…into which p-type source and drain regions are implanted on either side of a gate structure."); Ex. 1010, 70 ("pMOS is very similar [to nMOS], except for the diffusions being of opposite type."). Indeed, the '886 patent itself acknowledges that in a conventional switching circuit, the transistors can be NFETs or PFETs. '886 patent, 3:13-15.

A POSITA would have been motivated to substitute the NFET with a PFET to enable the use of the switch apparatus in noise-sensitive applications. Thompson, ¶173. As Dr. Thompson explains, it was well-established that PFETs (or PMOS transistors) generate less noise compared to NFETs (or NMOS transistors). Thompson, ¶173; Ex. 1018, 4 (PMOS devices exhibit "lower noise magnitude" compared to NMOS devices), 3 (A noise spectral density two orders of magnitude lower was observed in PMOS than in NMOS). Thus, a POSITA would have been motivated to implement the MOS transistor 1 as a PFET in a switch apparatus that is intended for noise-sensitive devices. Thompson, ¶173; *see Okashita* 1:11-15.

When a PFET is used in *Okashita*'s switch apparatus, the transistor gate would continue to be driven by the switch control signal. Thompson, ¶174; Ex.

1012, 2 (A "PFET operates when the voltage of the gate is lowered relative to that of the source or drain region."). Thus, it would have been well within the skill of a POSITA to substitute a PFET in *Okashita*'s switch apparatus in place of an NFET, a POSITA would have had a reasonable expectation of success in doing so, and the results of the substitution would have been predictable. Thompson, ¶174; Ex. 1011, 9; *Burgener*, ¶[0079].

7. Claim 7

a. [7]: "The switching circuit of claim 6, wherein said switch control signal drives said gate of said PFET through at least one resistor."

Okashita teaches the additional limitation of claim 7. Thompson, ¶175. *Okashita*'s MOS transistor 1, as modified to use a PFET, would have been driven by the switch control signal through a gate protection resistor for the same reasons as stated in ground 1 for claim 5. Thompson, ¶175; *Okashita*, 4:17-21.

C. Ground 3: Claims 1-7 Are Obvious Over *Okashita* and *Yu*

1. Overview of *Yu*

Yu discloses "a low-voltage triggering, silicon-controlled rectifier" (LVT-SCR) that is fabricated using an SOI system. *Yu*, 1:10-13, 3:53-62. An SCR is a "switching device." Thompson, ¶¶89-91; Ex. 1011, 18; *see also Yu*, 6:4-11. As *Yu* explains, the SOI system includes a silicon layer 34 formed on a buried oxide layer 32, which is formed on a substrate 30, as shown in *Yu*'s Figure 3. *Yu* is analogous

art to the ’886 patent since both are from the same field of endeavor. Thompson, ¶¶90-91. For example, both patents relate to a semiconductor switching circuit with cascaded transistors having an SOI configuration. *See* Yu, 3:43-4:15, 5:44-57, 6:4-11, 55-60; ’886 patent, 8:63-10:55.

FIG. 3

Yu, Fig. 3, 3:67-4:3, 5:55-66. According to *Yu*, prior art SCR devices fabricated using a bulk semiconductor use shallow trench isolation (STI) to define areas for active devices, or OD area. *Id*., 1:28-33. Forming SCR devices in an SOI process with STI, however, presents problems. *Id*., 2:4-9, 10-17, 6:55-60.

To address these problems, *Yu* teaches that it is important not only to form the STI regions in the silicon layer 34 of the SOI to define an active area, but to keep the STI regions outside of the active area of the planned LVT-SCR device as shown below, contrary to prior art processes. *Yu*, 4:8-15; Thompson, ¶¶92-93. Indeed, these STI regions “do not extend into the LVT-SCR device nor do they separate the first or second type doped regions [formed in silicon layer 42, 44].” *Yu*, 5:16-19.

FIG. 4

Id., Fig. 4. By forming the STI regions down to the buried insulator layer, each active area may be completely isolated. *Id*., 1:67-2:3. Accordingly, any transistors within the active area are situated within an isolated island that is surrounded by STI regions. *Id*., 4:8-10, Fig. 10; Thompson, ¶94.

Within the active area are, for example, two MOS transistors that are connected "in series" or "cascaded, or stacked," as shown below. *Yu*, 5:44-57.

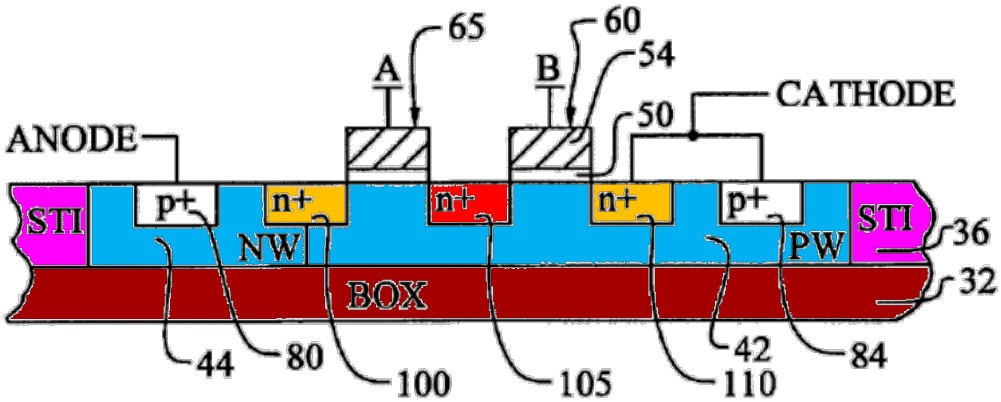


FIG. 10

Id., Fig. 10. In particular, a first NMOS transistor is formed by a gate 60, a doped region 110, and a doped region 105. *Id*., 5:44-57. A second MOS transistor is formed by a gate 65, a doped region 105, and a doped region 100. *Id.* These doped regions 100, 105, and 110 serve as the source and drains of the first and second transistors. Thompson, ¶¶95-96; *Yu*, 6:40-45. The interfaces between these doped regions and the silicon layer 34 form source/drain junctions. Thompson, ¶¶96-97; *Yu*, 6:40-45, Fig. 11; *see* Ex. 1011, 10 ("pn junctions [] are formed by the drain-bulk and source-bulk interfaces in a MOSFET"), 11 (Fig. 1.36).

Another "important feature" of *Yu* is that "[t]he doped regions 80, 84, 100, 105, and 110, are formed in the upper part of the wells 42 and 44 and do not extend to the buried oxide layer 32." *Yu*, 6:46-54, Fig. 10. In other words, "the original silicon layer … is thick enough so that the doped regions do not completely deplete the wells 42 and 44" into the buried oxide layer 32. *Id*.

2. Combining *Okashita* and *Yu*

Okashita and *Yu* are similar. Thompson, ¶176. Both devices have transistors that are fabricated on an SOI structure. *Okashita*, 1:47-58, 5:41-46, Fig. 9; *Yu*, 3:53-4:3, Fig. 3. Furthermore, the transistors in *Okashita* and *Yu* are both "cascaded," *Okashita*, 8:30-34; *Yu*, 5:44-57, and they are situated within an isolated island that is surrounded by a shallow trench isolation (STI) region 36, *Okashita*, 6:50-51; *Yu*, 4:8-10, Fig. 10; Thompson, ¶176. A POSITA would have

found it obvious to fabricate *Okashita*'s transistors using an SOI process, as *Yu* teaches, so the transistors would have been within the active area that is surrounded by a trench isolation region. Thompson, ¶¶177-178. A POSITA would have been motivated to ensure that *Okashita*'s trench isolation regions are not formed within the active area and to maintain a sufficient thickness in the silicon layer so that the transistors' source/drain interfaces do not extend to the silicon oxide layer, as taught by *Yu* (*supra* §V.C.1), because doing so would achieve similar thermal and electrical benefits as described by *Yu* in *Okashita*'s switching device. *See Yu*, 2:4-17; Thompson, ¶¶177-178. Indeed, a POSITA would have recognized that, due to the lower thermal conductivity of silicon dioxide compared to silicon, if the source/drain junctions of *Okashita*'s cascaded transistors were to contact the silicon oxide layer, the transistors would operate at higher temperatures, which could then negatively impact circuit performance and "fail at a lower energy dissipation level" as taught by *Yu* (2:4-17). Thompson, ¶¶97-98, 179; s*ee* Ex. 1010, 59-60; Ex. 1013, 27-28. Since both *Okashita* and *Yu* disclose a switching circuit with cascaded transistors that are formed in an isolated island that is surrounded by a trench, a POSITA would have had a reasonable expectation of success in fabricating *Okashita*'s transistors based on *Yu*'s SOI process. Thompson, ¶180. Furthermore, applying *Yu*'s teaching to *Okashita* would have been a straightforward use of a known technique to enhance a similar device in the

same manner. *KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 417-18 (2007); Thompson, ¶180.

3. Independent Claim 1

a. [1pre]: "A switching circuit comprising:"

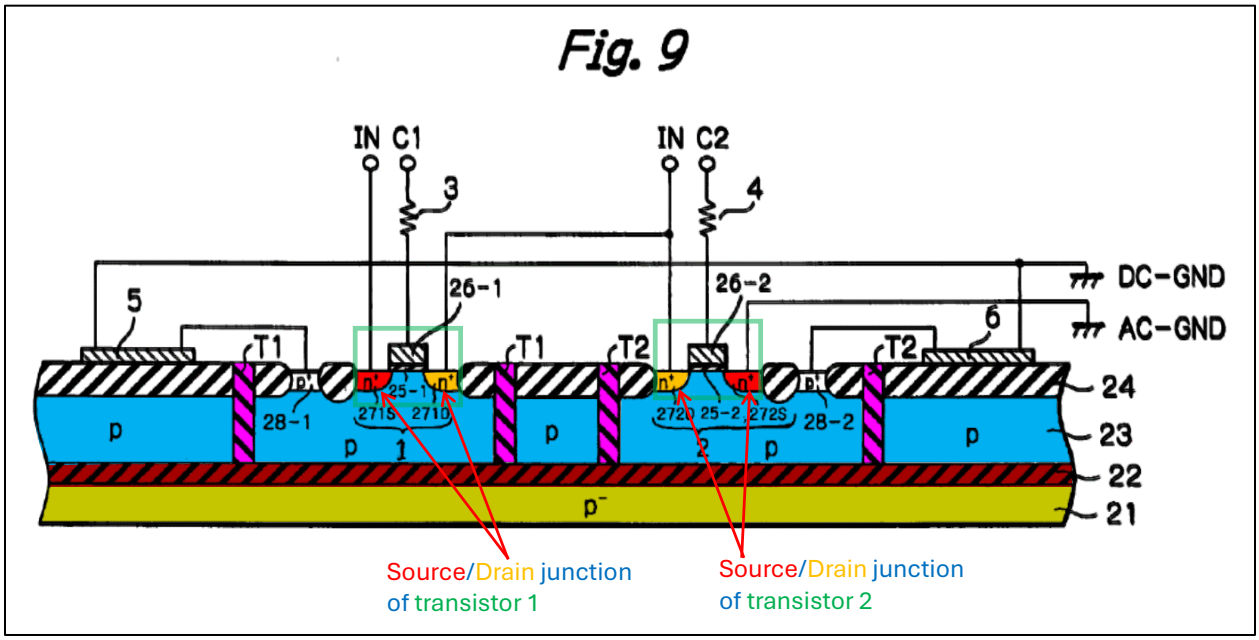
To the extent the preamble is limiting, *Okashita* discloses it for the same reasons as stated in claim [1pre] for grounds 1 and 2. Thompson, ¶181.

b. [1a]: "a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;"

Okashita teaches this limitation for the same reasons as stated in claim [1a] for ground 2. *See* claim [1a], *supra*. Thompson, ¶182.

c. [1b(i)]: "each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer,"

Okashita in view of *Yu* teaches this limitation. Thompson, ¶¶183-184. As previously discussed, the source/drain junction of *Okashita*'s MOS transistors 1, 1′ are positioned apart from the top surface of the buried oxide layer for the same reasons as stated in ground 2 for claim [1b(i)], *supra*. Thompson, ¶183.



Okashita, Fig. 9. To the extent Patent Owner contends that *Okashita* does not explicitly mention this feature, it would have been obvious in view of *Okashita* and *Yu*. A POSITA would have been motivated to ensure a sufficiently thick silicon layer remains between *Okashita*'s source/drain junctions and the top surface of the silicon oxide layer, as *Yu* teaches, to achieve similar thermal and electrical benefits. *Supra* §§V.C.1-V.C.2; *Yu*, 2:4-17; Thompson, ¶184.

d. [1b(ii)]: "thereby forming a source/drain junction capacitance;"

Okashita in view of *Yu* teaches this limitation. For the same reasons that the structure of *Okashita* in ground 1 forms a source/drain junction capacitance, the corresponding structure in this ground, namely source/drain junctions of MOS transistors, 1, 1' separated from the silicon oxide layer by the silicon layer, as *Yu*

teaches (*see supra* §V.C.2), also forms a source/drain junction capacitance. Thompson, ¶185.

e. [1c(i)]: "at least one trench extending through said device layer and contacting a top surface of said buried oxide layer,"

Okashita teaches this limitation for the same reasons as stated in grounds 1 and 2. Thompson, ¶186.

f. [1c(ii)]: "thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer."

Okashita teaches this limitation for the same reasons as stated in grounds 1 and 2. Thompson, ¶187.

4. Claim 2

Okashita teaches the additional limitation of claim 2 for the same reasons as stated in grounds 1 and 2 for claim 2, *supra*. Thompson, ¶188.

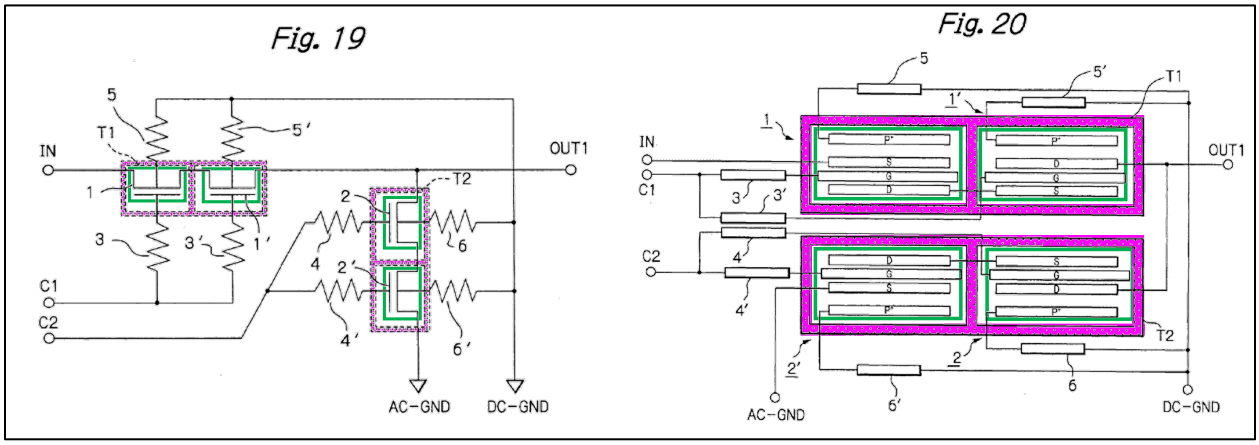
5. Claim 3

a. "The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer."

Okashita in view of *Yu* teaches the additional limitation of claim 3 for the same reasons as stated in ground 2 for claim 3. Thompson, ¶¶189-194; *Okashita*, 10:49-67. To the extent Patent Owner disputes this, a POSITA would have been

motivated to situate the MOS transistor 1′ on the same isolated island as the MOS transistor 1, as *Yu* teaches. Thompson, ¶¶191-192.

Okashita discloses "each of the MOS transistors 1, 1′, 2 and 2′ is isolated by the trench insulating layers T1 and T2, so that the leakage of radio frequency signals from the silicon layer 23 of the MOS transistor 1 to that of the MOS transistor 1′ … can be sufficiently suppressed." *Okashita*, 8:47-54.



Okashita, Figs. 19-20. It would have been obvious to place both of *Okashita*'s cascaded MOS transistors 1, 1' within the same isolated island to ensure consistent performance characteristics of these two transistors. Thompson, ¶191.

Yu discloses two cascaded transistors being situated in the same isolated island that is surrounded by trenches. Thompson, ¶192.

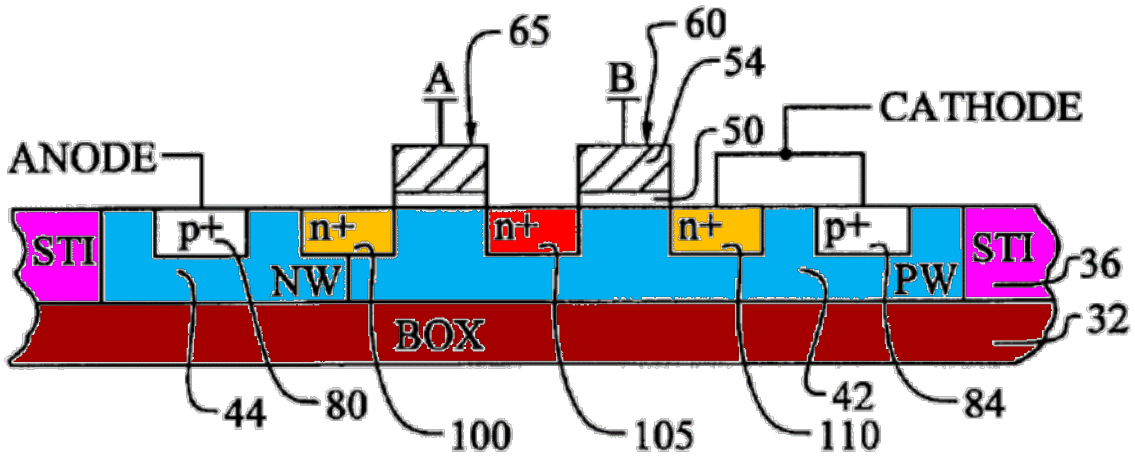


FIG. 10

Yu, Fig. 10. For example, in *Yu*, the first and second transistors are cascaded and located in an isolated island that is surrounded by STI regions. Thompson, ¶192; *Supra* §§V.C.1-V.C.2; *Yu*, 5:44-55, 6:46-60. "[T]he STI regions are formed down to the buried insulator layer such that each active area is completely isolated from other active areas." *Yu*, 1:67-2:3, 6:55-60. Importantly, these STI regions "do not extend into the LVT-SCR device nor do they separate the first or second type doped regions [formed in silicon layer 42, 44]." *Yu*, 5:16-19. As explained with reference to claims [1b(i)] and [3] of ground 2, a POSITA would have recognized that *Okashita*'s MOS transistors 1′ will have a different electrical performance and reliability than the MOS transistor 1 if they operate at different temperatures. Thompson, ¶193; *see* Ex. 1010, 75. A POSITA, therefore, would have been

motivated to situate both MOS transistors 1, 1′ in the same isolated island, as *Yu* teaches, so they both have consistent temperatures and electrical properties. As previously explained with reference to claims [1b(i)] and [3] of ground 2, it was well understood that placing multiple transistors within the same isolated region surrounded by a trench reduces performance variations between the transistors. Thompson, ¶¶193-194. Since both *Okashita* and *Yu* teach switching circuits with cascaded transistors having an SOI configuration with trench isolation, a POSITA would have had a reasonable expectation of success in incorporating the teaching of *Yu* in *Okashita*. Thompson, ¶194.

6. Claim 4-7

Okashita teaches the additional limitations of claim 4-7 for the same reasons as stated in claims 4-7 of grounds 1 and 2, *supra*. Thompson, ¶195.

D. Ground 4: Claims 1, 2, and 3 Are Anticipated by *Yu*

1. Independent Claim 1

a. [1pre]: "A switching circuit comprising:"

To the extent the preamble is limiting, *Yu* discloses an LVT-SCR, which is a switching circuit. *Yu*, 1:10-13, 3:53-62, 6:4-11; Thompson, ¶196; Ex. 1011, 18.

b. [1a]: "a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;"

Yu discloses this limitation. Thompson, ¶¶197-199. *Yu*'s LVT-SCR includes two MOS transistors 60, 65 that are connected "in series" and, therefore, are "cascaded, or stacked." *Yu*, 5:44-57; Thompson, ¶¶197-198. *Yu*'s cascaded transistors 60, 65 are also fabricated in a silicon layer that is situated over a buried oxide layer 32, as shown below. *Yu*, 5:58-66; Thompson, ¶197.

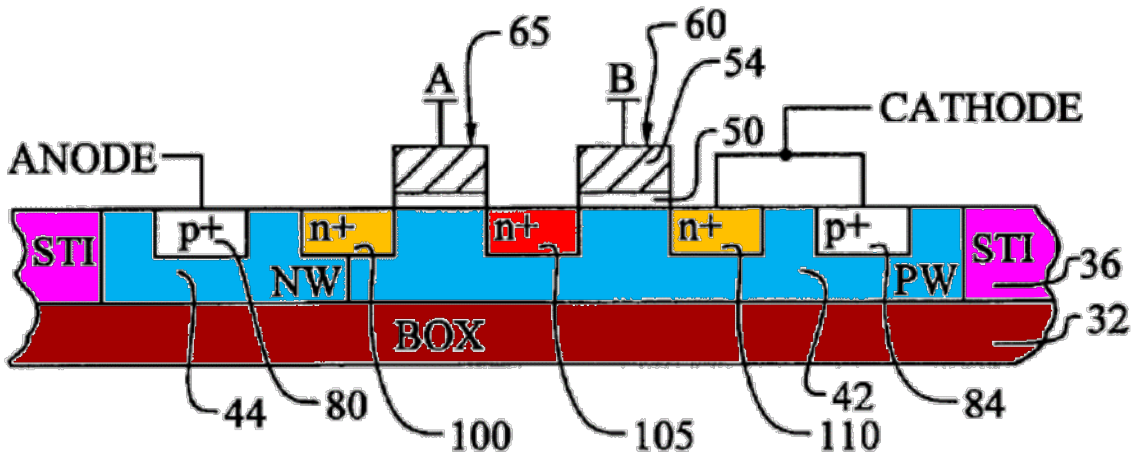


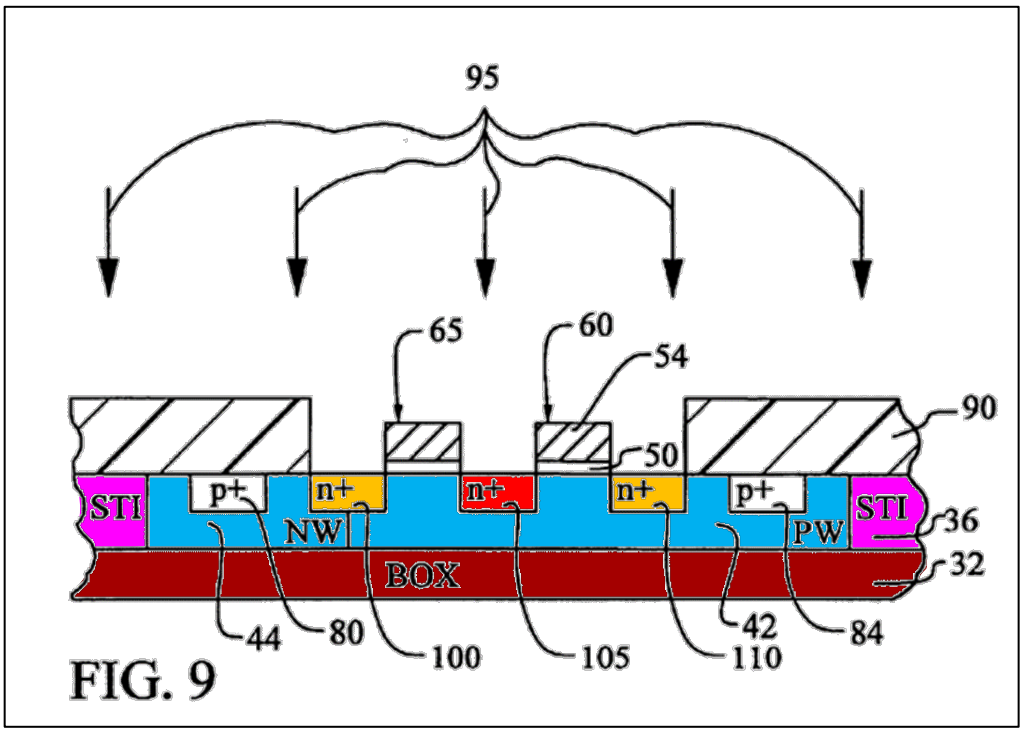
FIG. 10

Id., Fig. 10. In *Yu*, the STI regions define the "active area regions of silicon layer 34 where active devices may be subsequently formed." *Id.*, 4:8-12, 6:55-60. Accordingly, the silicon layer is the claimed device layer. Thompson, ¶¶198-199. While the bulk semiconductor substrate layer is not shown in Figure 10 for "simplicity," *Yu*'s LVT-SCR device is fabricated as an SOI system where the

buried oxide layer "is either grown or deposited overlying the silicon substrate." *Yu*, 3:44-47, 53-62, 4:5-7, Fig. 3; Thompson, ¶198. Accordingly, the plurality of the cascaded transistors are fabricated in a device layer situated over a BOX layer and a bulk semiconductor layer. Thompson, ¶199.

c. [1b(i)]: "each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer,"

Yu discloses this limitation. Thompson, ¶¶200-202. As *Yu* explains, each of the transistors includes doped regions that form the source and drain of the transistors, as shown below. Thompson, ¶200.



Yu, Fig. 9. For example, the first NMOS transistor 60 includes an n^+ doped region 105 as its source and an n^+ doped region 110 as its drain. *Yu*, 5:44-57; *see also id.*,

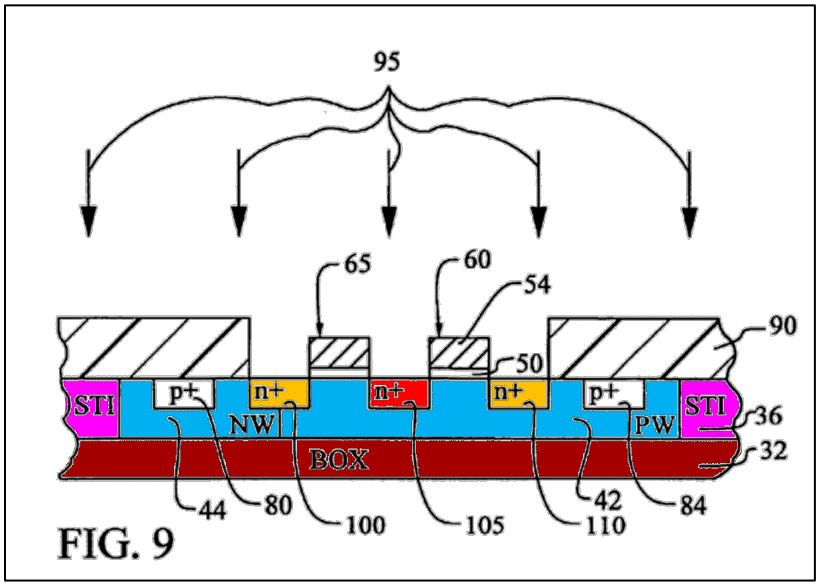
4:17-24, 5:4-12; Thompson, ¶201. The second MOS transistor 65 shares the n+ doped region 105 as its source and has an n^+ doped region 100 as its drain. *Yu*, 5:44-55; *see also id.*, 4:17-24, 5:4-12; Thompson, ¶201. The interfaces between these doped regions and the silicon layer, therefore, form the source/drain junctions for the respective transistors. Thompson, ¶201; *see Yu*, 6:40-45, Fig. 11; *see, e.g.*, Ex. 1009, 4; Ex. 1010, 35-39; Ex. 1011, 10-11. The source/drain junction for each of the cascaded transistors does not extend to the buried oxide layer 32. *Yu*, 6:46-54, Fig. 10 (showing a "thick" silicon layer between the transistors and the BOX layer); Thompson, ¶202.

d. [1b(ii)]: "thereby forming a source/drain junction capacitance;"

Yu discloses this limitation. For the same reasons that the structure of *Okashita* in ground 1 forms a source/drain junction capacitance, the corresponding structure in this ground, namely the source/drain junctions of transistors 60, 65 separated from the BOX layer by the "thick" silicon layer, also forms a source/drain junction capacitance. Thompson, ¶203; *Yu*, 6:46-54; *see also* Ex. 1013, 25-26; Ex. 1014, 2-5; *see, e.g.*, *Acoustic Tech.*, 949 F.3d 1366; *Kennametal*, 780 F.3d 1376.

e. [1c(i)]: "at least one trench extending through said device layer and contacting a top surface of said buried oxide layer,"

Yu discloses this limitation because *Yu*'s STI regions "are formed down to the buried insulator layer such that each active area is completely isolated from other active areas," as shown below. *Yu*, Fig. 9, 1:67-2:3; Thompson, ¶¶204-205.



Yu, Fig. 9. *Yu*'s STI region 36 extends through the silicon layer and contacts a top surface of the buried oxide layer 32. Thompson, ¶205.

f. [1c(ii)]: "thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer."

Yu discloses this limitation. Thompson, ¶¶206-208. As explained *supra* §V.C.1, *Yu*'s STI regions define an "active area region" (or "OD region") where "active devices may be subsequently formed." *Yu*, 4:8-15; Thompson, ¶¶206-207.

As shown in Figure 12 below, "[t]he OD region 200 represents the active device area." *Yu*, 6:55-60.

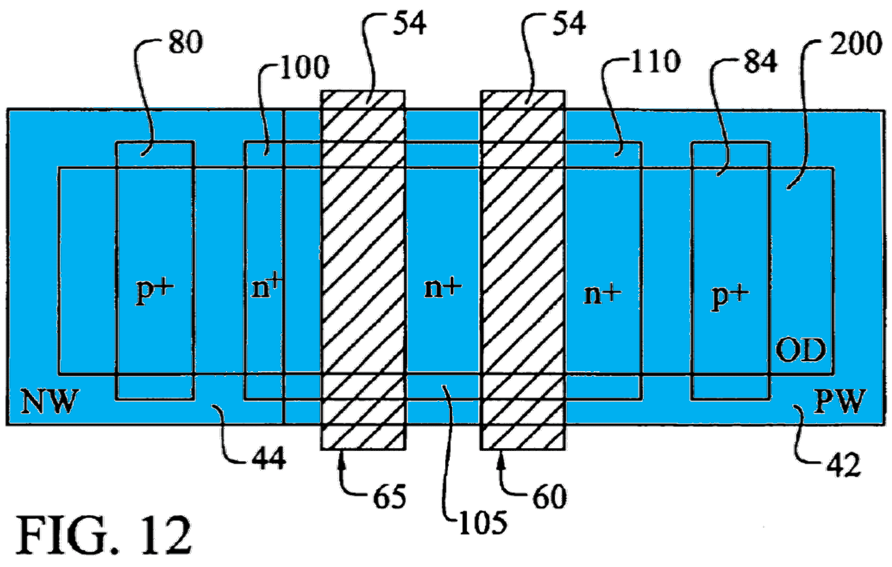


FIG. 12

Yu, Fig. 12, 6:55-7:4. While the STI regions are not shown in Figure 12, *Yu* explains that the STI regions are "formed in the area outside of the OD box 200," (6:55-60, 4:8-15), and "do not extend into the LVT-SCR device nor do they separate the first or second type doped regions [formed in silicon layer 42, 44]," as shown below. *Id.*, 5:16-19; Thompson, ¶¶207-208.

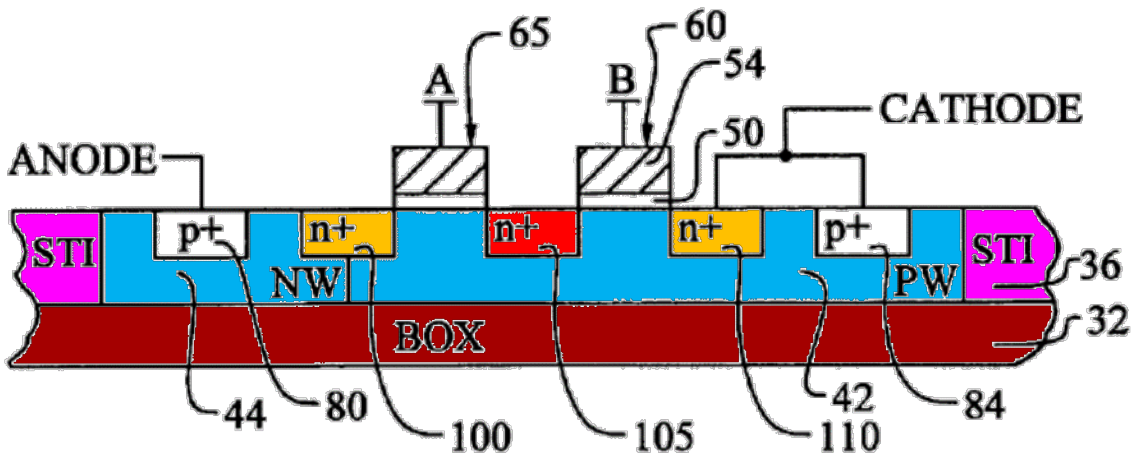


FIG. 10

Yu, Fig. 10. Therefore, the STI regions electrically isolate the first and second transistors from devices in other active areas. Thompson, ¶208. As explained previously with reference to claim [1c(ii)] of ground 1, as a result of this electrical isolation of the transistors, electrical signals from the silicon layer surrounding the first and second transistors will not leak and cause voltage and current fluctuations in the silicon layer of adjacent active areas. Thompson, ¶208; *see also* '886 patent, 2:65-3:11, 6:10-15, 6:33-42. Accordingly, *Yu*'s STI regions will also reduce voltage and current fluctuations in the device layer. Thompson, ¶208.

2. Claim 2

a. [2]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer."

Yu discloses this limitation. Thompson, ¶209. As explained above with reference to claims [1c(i)] and [1c(ii)], the first NMOS and second MOS transistors are formed in an active area of silicon layer that is surrounded by STI regions that extend through the silicon layer to the buried oxide layer 32, such that the active area is "completely isolated" from other active areas. *Yu*, 1:67-2:3, 4:8-15; Thompson, ¶209. In other words, the first NMOS and second MOS transistors are situated within an isolated island in the silicon layer that is defined by the walls of the surrounding STI region 36 and the top surface of the buried oxide layer 32. Thompson, ¶209.

3. Claim 3

a. [3]: "The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer."

Yu discloses this limitation, because as explained above with reference to claim 2, both of the cascaded NMOS and MOS transistors are situated within the isolated island in the silicon layer. Thompson, ¶210.

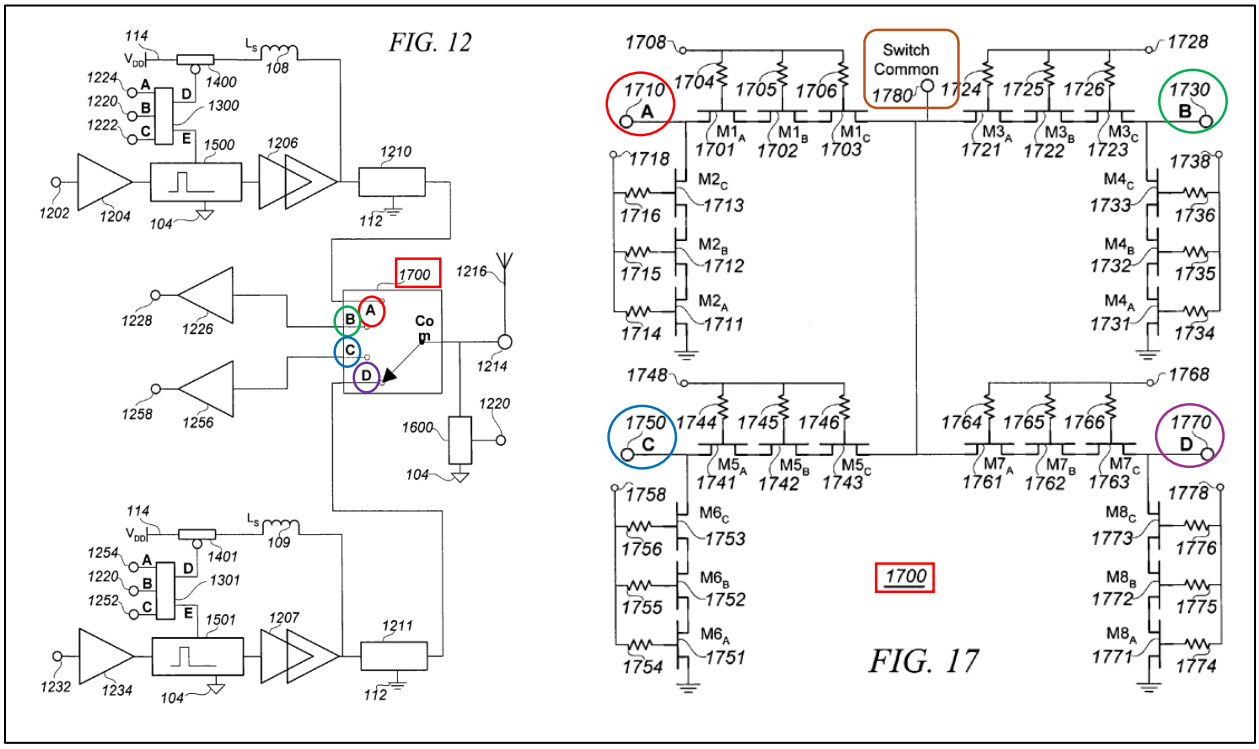
E. Ground 5: Claims 1-19 Are Obvious Over *Burgener* and *Okashita*

1. Overview of *Burgener*

Burgener discloses an "integrated circuit (IC)" that includes "all RF front end or transceiver elements for a portable communication device," such as a cellular telephone and other wireless communications device. *Burgener*, Abstract, ¶[0006]. According to *Burgener*, the RF front end may be implemented by stacks of multiple Field Effect Transistors (FETs) connected in series to operate as a switching device. *Burgener*, Abstract, ¶[0009]; Thompson, ¶100.

Burgener is analogous art to the '886 patent since both are from the same field of endeavor. Thompson, ¶¶99-101. For example, both relate to a semiconductor switching circuit with cascaded transistors having an SOI configuration. *See Burgener*, Abstract, ¶¶[0005]-[0006], [0105]; Thompson, ¶101; '886 patent, 1:14-17, 7:25-31.

Burgener's RF transceiver, as shown in Figure 12 below, includes an "antenna switch 1700" (i.e., "a power-switching circuit" as shown in Figure 17 below) that selectably directs incoming signals from an antenna 1216 to low-noise amplifiers 1226, 1256 and outgoing signals from power amplifiers 1206, 1207 to the antenna 1216. *Burgener*, ¶¶[0085], [0090]-[0094]; Thompson, ¶102.



Burgener, Figs. 12, 17.

The antenna switch 1700, for example, enables the antenna 1216 (connected to common node 1780) to be selectably coupled to the different RF ports (port A 1710, port B 1730, port C 1750, or port D 1770) and to the respective low-noise and power amplifiers. *Burgener*, ¶[0102]; Thompson, ¶103. As an example, to transmit outgoing signals from a power amplifier 1206 or 1207, the antenna switch 1700 would connect the antenna (via a common node 1780) to port A 1710 or port D 1770. But to transmit incoming signals to low-noise amplifier 1226 or 1256, the antenna switch 1700 would connect the antenna (via a common node 1780) to port

B 1730 or port C 1750. Thompson, ¶¶103-104. This switching function is accomplished by applying control voltages to the selected control nodes of the FETs (e.g., nodes 1708, 1718, 1728, 1738, etc.). *Burgener*, ¶¶[0090], [0092], [0101]; Thompson, ¶103. As illustrated in Figure 17, the antenna switch 1700 of the RF transceiver (Figure 12) includes multiple cascaded FETs. *Burgener*, Fig. 17.

2. Combining *Burgener* with *Okashita*

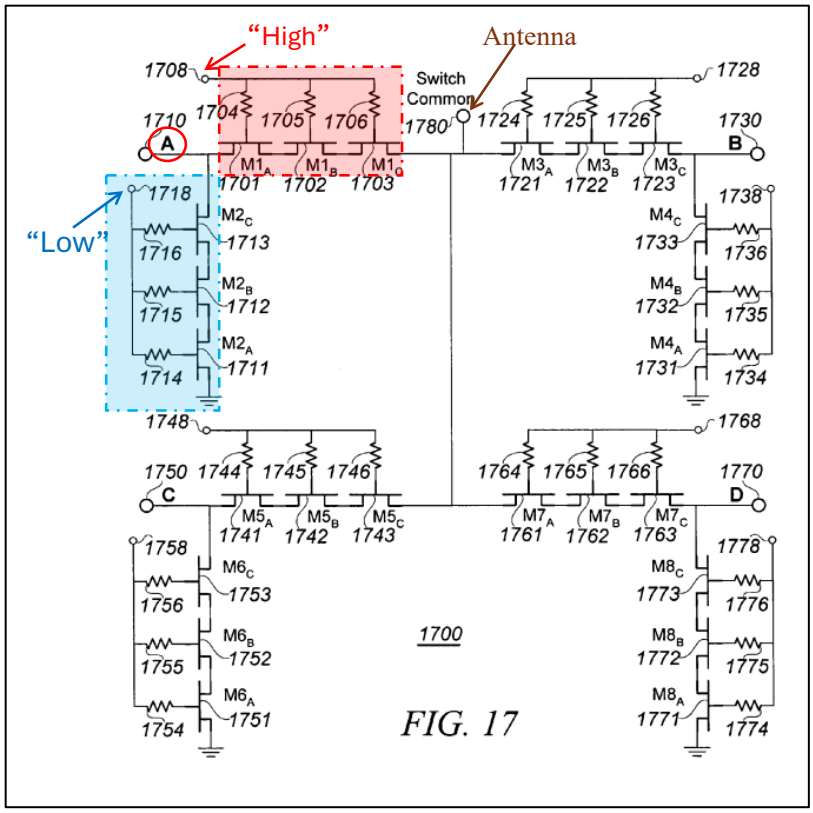
While *Burgener* does not expressly provide details related to integrated circuit fabrication, *Burgener* explains that its integrated circuit may be fabricated using "semiconductor-on-insulator (SOI) techniques," such as those taught by *Okashita*. *Burgener*, ¶[0105]; *Okashita*, 1:7-15, 5:41-43, Fig. 9; Thompson, ¶¶104, 211. As explained with reference to claims [1pre]-[1b(ii)] of ground 2, *Okashita* discloses a "semiconductor switch apparatus" that includes cascaded MOS transistors 1, 1′ having an SOI configuration with an intervening silicon layer between the transistors' source/drain junctions and the buried silicon oxide layer. *Okashita*, 1:7-15, 5:41-43, Fig. 12; Thompson, ¶212. Further, as explained with reference to claims [1c(i)]-[1c(ii)] of ground 2, *Okashita*'s MOS transistors are isolated by a trench T1 that extends through the silicon layer to contact the silicon oxide layer to prevent leakage of radio frequency signals from these MOS transistors to other components of the switch apparatus. Thompson, ¶212.

It would have been obvious for a POSITA to fabricate *Burgener*'s integrated circuit (e.g., antenna switch 1700 and the corresponding cascaded FETs) with (i) an intervening silicon layer between the source/drain junctions and the buried silicon oxide layer, and (ii) trenches, as *Okashita* teaches. Thompson, ¶¶213-218. A POSITA would have been motivated to combine *Burgener* and *Okashita* for at least three reasons. Thompson, ¶213.

First, a POSITA would have been motivated to fabricate *Burgener*'s cascaded FETs with an intervening silicon layer, as *Okashita* teaches, such that the source/drain junctions of these FETs are separated from the buried oxide layer by the intervening silicon layer. Thompson, ¶214. As explained with reference to claims [1b(i)]-[1b(ii)] of ground 2, a POSITA would have recognized that, because the buried oxide layer has lower thermal conductivity compared to the bulk silicon layer, conventional SOI transistors tend to operate at higher temperatures, which can adversely affect their performance and reliability. Thompson, ¶214; *see, e.g.*, Ex. 1010, 60; Ex. 1013, 26-28; Ex. 1022, 1. Instead of using a conventional SOI structure, a POSITA would have been motivated to add an intervening silicon layer between the source/drain junction and the buried oxide layer, as *Okashita* discloses, because doing so would reduce the operating temperature of the transistors and, thereby, enhance their performance and reliability. Thompson, ¶214; *see, e.g.*, Ex. 1010, 60; Ex. 1013, 27; *see supra* §V.B.1.c. Accordingly, it

would have been obvious for a POSITA to fabricate *Burgener*'s cascaded FETs with an intervening silicon layer, as *Okashita* teaches, to decrease the operating temperature of *Burgener*'s transistors and improve their performance and reliability. Thompson, ¶214.

Second, a POSITA would have been motivated to fabricate *Burgener*'s cascaded SOI FETs using the isolation technique, as *Okashita* teaches, to prevent leakage of radio frequency signals from the cascaded SOI FETs to other components of antenna switch 1700. Thompson, ¶215. As illustrated in below Figure 17, the gates of FETs $M1_A$ 1701, $M1_B$ 1702, $M1_C$ 1703 are connected to control node 1708 while the gates of FETs $M2_A$ 1711, $M2_B$ 1712, $M2_C$ 1713 are connected to control node 1718. To selectively connect port A 1710 to the antenna, a "high" voltage is applied to control node 1708, and a "low" voltage is applied to control node 1718. *Burgener*, ¶[0103].



Burgener, Fig, 17; Thompson, ¶215. Because *Burgener*'s antenna switch 1700 selectively switches between different RF ports by applying high and low control voltages to various cascaded FETs, a POSITA would have been motivated to place, for example, the cascaded FETs $M1_A$ 1701, $M1_B$ 1702, $M1_C$ 1703 together in one isolated region surrounded by a trench and/or the cascaded FETs $M2_A$ 1711, $M2_B$ 1712, $M2_C$ 1713 together in another isolated region surrounded by a second trench, as *Okashita* teaches, because doing so would prevent the voltage applied to FETs 1701-1703 from leaking and causing voltage and current fluctuations in FETs 1711-1713, and vice versa. Thompson, ¶¶215-216; *supra* §V.E.1.

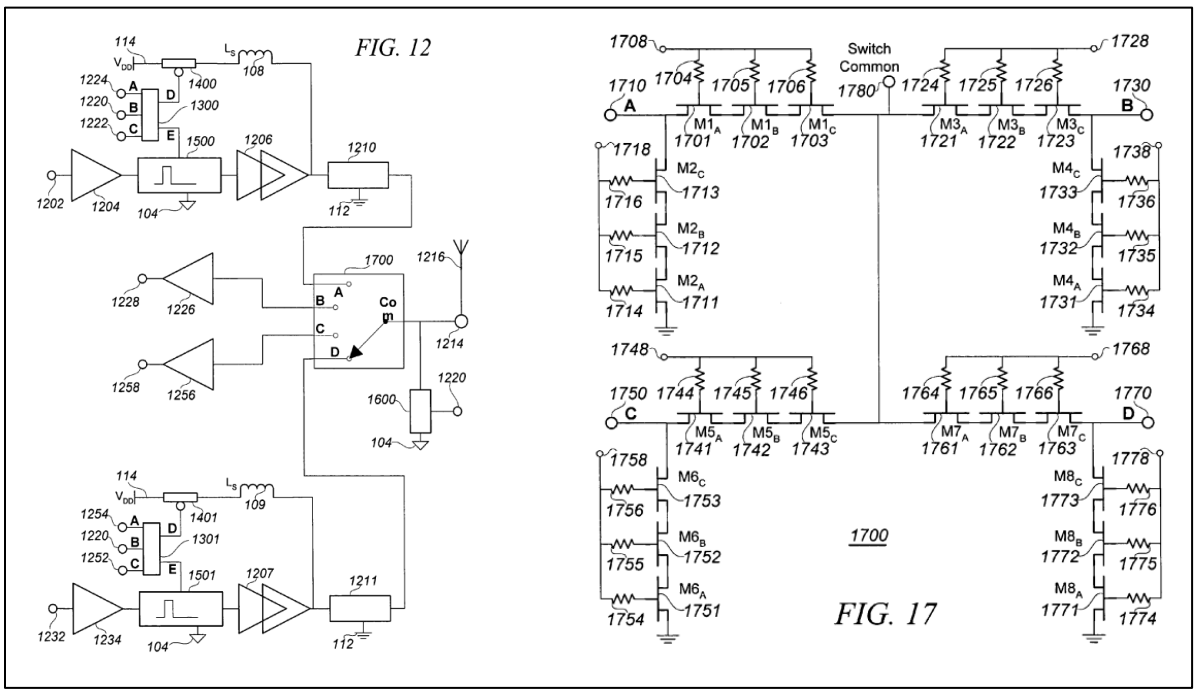
Third, as explained previously with reference to claims [1b(i)] and [3] of ground 2, a POSITA would have been motivated to locate each set of FETs together in one isolated region that is surrounded by a trench, as *Okashita* teaches, to ensure that the FETs have consistent performance characteristics because doing so would also "minimize the effect of mismatch due to" the FETs having different electrical properties and being at different temperatures. Thompson, ¶217; Ex. 1010, 75-78.

A POSITA would have reasonably expected success in fabricating *Burgener*'s integrated circuits using the SOI techniques *Okashita* teaches because both references describe switching circuits that use cascaded transistors in an SOI configuration. Thompson, ¶218. It would have been no more than applying a known technique to a known device to yield predictable results. Thompson, ¶218. Indeed, the techniques of adding an intervening silicon layer or placing multiple transistors within an isolated region were already well-established in the field. Thompson, ¶¶47-60, 218; *see, e.g.*, Ex. 1010, 24-25; Ex. 1013, 25-26; Ex. 1016, 1; Ex. 1015, 1:22-28; Ex. 1020, 4:47-5:12. Accordingly, applying these teachings of *Okashita* to *Burgener* would have been a straightforward use of a known technique to improve a similar device in the same way. Thompson, ¶218.

3. Independent Claim 1

a. [1pre]: "A switching circuit comprising:"

To the extent the preamble is limiting, *Burgener* discloses this limitation because *Burgener*'s antenna switch 1700 is a switching circuit. *Burgener*, ¶¶[0088], [0104] ("The FET stacks … provide the switching functions[.]"); Thompson, ¶¶219-220; *supra* §V.E.1; *Burgener*, ¶¶[0090]-[0094].

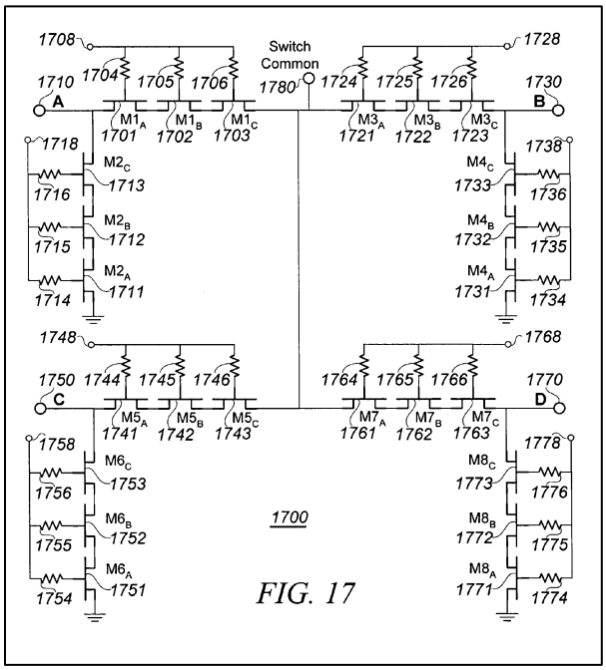


Burgener, Figs. 12, 17.

b. [1a]: "a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;"

Burgener in view of *Okashita* teaches this limitation. Thompson, ¶¶221-222. *Burgener*'s antenna switch 1700 includes "[s]tacks of multiple FETs [that are

connected] in series to operate as a switching device," as shown below. *Burgener*, Abstract, Fig. 17; Thompson, ¶221.



Burgener, Fig. 17. A POSITA would have understood that *Burgener*'s FETs are cascaded transistors because they are connected in series. Thompson, ¶221; *Yu*, 5:53-55; '886 patent, 6:50-51 (acknowledging that transistors "coupled in series" are considered "cascaded").

As discussed in §V.E.2, it would have been obvious for a POSITA to fabricate *Burgener*'s integrated circuit (e.g., antenna switch 1700 and the corresponding cascaded FETs) using *Okashita*'s SOI configuration. Thompson, ¶222. In *Burgener*'s antenna switch as modified by *Okashita*, the plurality of cascaded transistors would have been fabricated in *Okashita*'s silicon layer that is

situated over a silicon oxide layer and a bulk silicon substrate as described with reference to claim [1a] of ground 2. Thompson, ¶222.

c. [1b(i)-1b(ii)]: "each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;"

Burgener in view of *Okashita* teaches these limitations. Thompson, ¶223. In *Burgener*'s antenna switch as modified by *Okashita*, as described with reference to claims [1b(i)]-[1b(ii)] of grounds 1 and 2, each of the plurality of cascaded transistors have a source/drain junction that does not contact the silicon oxide layer, thereby forming a source/drain junction capacitance. *Supra* §V.E.2; Thompson, ¶223.

d. [1c(i)-1c(ii)]: "at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer."

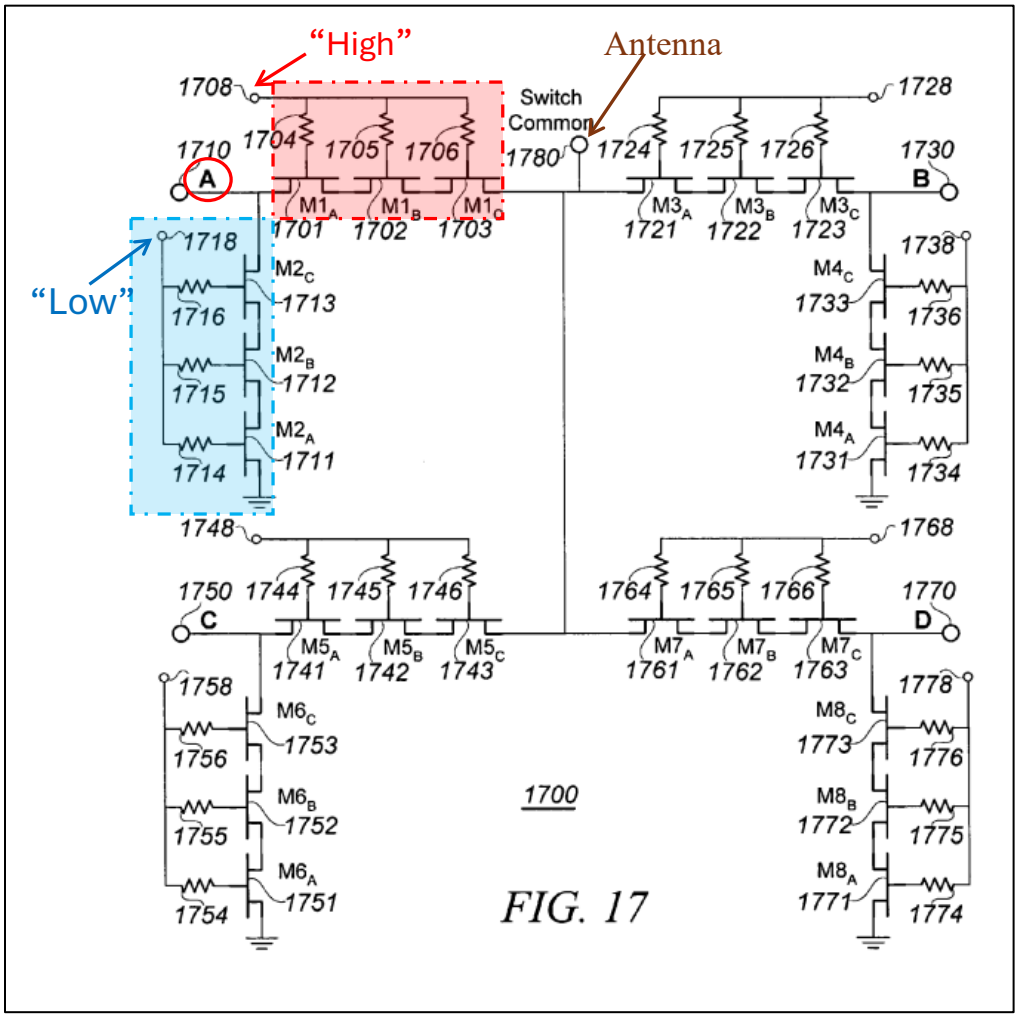
Burgener in view of *Okashita* teaches these limitations. Thompson, ¶224. In *Burgener*'s antenna switch as modified by *Okashita*, as described with reference to claims [1c(i)]-[1c(ii)] of grounds 1 and 2, there would be at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded

transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer. *Supra* §V.E.2; Thompson, ¶224.

4. Claim 2

a. [2]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer."

Burgener in view of *Okashita* teaches the additional limitation of this claim. Thompson, ¶¶225-226. For example, at least one of the plurality of *Burgener*'s FETs would be situated within an isolated island, as *Okashita* teaches. *See supra* §V.E.2,



Burgener, Fig. 17. For example, as discussed with reference to claim 3 of ground 2 and §V.E.2, based on the teachings of *Okashita*, a POSITA would have recognized that placing the cascaded FETs 1701-1703 in one isolated region that is surrounded by a trench and/or the cascaded FETs 1711-1713 in another isolated region that is surrounded by another trench would prevent the voltage applied to FETs 1701-1703 from leaking and causing voltage and current fluctuations in the device layer around FETs 1711-1713. Thompson, ¶226. Therefore, in *Burgener* as modified by

Okashita, at least one of the cascaded transistors (e.g., one of the FETs in FETs 1701-1703 or one of the FETs in FETs 1711-1713) would be located within an isolated island in the device layer. Thompson, ¶226.

5. Claim 3

a. [3]: "The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer."

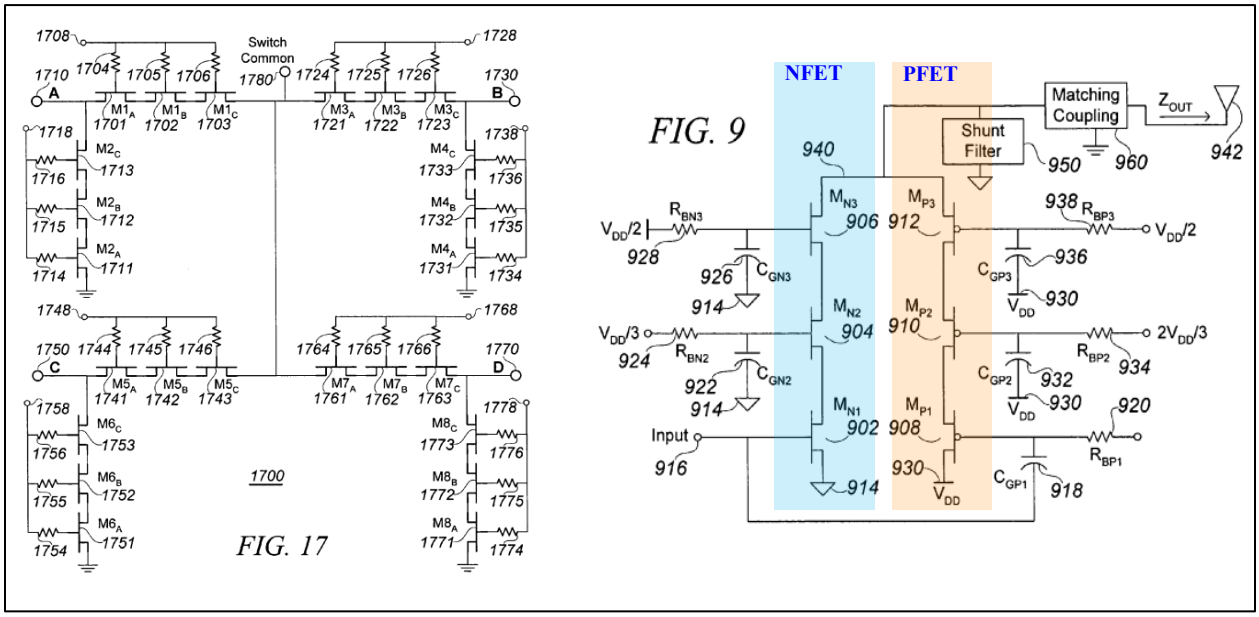
Burgener in view of *Okashita* teaches the additional limitation of this claim. Thompson, ¶227. As explained with reference to claim 2 and §V.E.2, *Burgener*'s cascaded FETs 1701-1703 would have been situated within an isolated island surrounded by a trench. Thompson, ¶227. Alternatively, or additionally, the cascaded FETs 1711-1713 would have been situated within an isolated island surrounded by a trench. Thompson, ¶227. Therefore, *Burgener* in view of *Okashita* teaches a plurality of the cascaded transistors situated within an isolated island in said device layer. Thompson, ¶227.

6. Claim 4

a. [4]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is an NFET with a gate driven by a switch control signal in a wireless communications device."

Burgener teaches the additional limitation of this claim. Thompson, ¶¶228-231. According to *Burgener*, a FET stack may be N-channel FETs (NFETs) or P-

channel FET (PFET). *Burgener*, ¶[0079]. To fabricate PFET stacks, "the polarity of each voltage and polarized component associated with the stack" is reversed. *Id.* *Burgener*'s Figure 9, as shown below, shows an exemplary circuit that employs both NFET stack and PFET stack. *Id.*, ¶[0080].



Id., Figs. 9, 17. While *Burgener* does not explicitly state that the FETs of antenna switch 1700 are NFETs, a POSITA would have recognized that the symbol of the FETs used in Figure 17 is that of an NFET. Thompson, ¶229. For example, the symbol of a PFET has a small circle on the gate in the symbol, but the symbol of an NFET does not. *Id.*

Moreover, the FET stacks are also controlled by a control signal that is applied to the gates of the FETs. Thompson, ¶230; *Burgener*, ¶[0104]; *supra* §§V.E.1-V.E.2. A POSITA would have known that applying "high" and "low"

control voltages to the gates of these FETs selectively switches them ON and OFF to direct signals from the antenna to one of the ports. Thompson, ¶230. Therefore, the gates of these FETs are driven by a switch control signal. *Id*. Additionally, *Burgener* discloses that its IC with the antenna switch 1700 is used in a wireless communications device. *Burgener*, ¶[0005]; Thompson, ¶231.

Thus, *Burgener* in view of *Okashita* discloses at least one of the cascaded FETs of antenna switch 1700 is an NFET with a gate driven by a switch control signal in a wireless communications device. Thompson, ¶¶229-231.

7. Claim 5

a. [5]: "The switching circuit of claim 4, wherein said switch control signal drives said gate of said NFET through at least one resistor."

Burgener teaches the additional limitation of this claim. Thompson, ¶232. As *Burgener* shows, the control signal drives the gates of the FETs through gate resistors (e.g., resistors 1704, 1705, 1706 of Fig. 17). *See Burgener*, Fig. 17; Thompson, ¶232.

8. Claim 6

a. [6]: "The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is a PFET with a gate driven by a switch control signal in a wireless communications device."

Burgener teaches the additional limitation of this claim. Thompson, ¶¶233-235. As discussed with reference to claim 6 of ground 2, it would have been obvious for a POSITA to use PFET in noise-sensitive applications because PFETs exhibit lower noise than NFETs and are more suitable in noise sensitive applications. Thompson, ¶233; Ex. 1018, 3-4. Further, *Burgener* teaches that PFETs may be analogously fabricated by "reversing the polarity of each voltage and polarized component associated with the stack." *Burgener*, ¶¶[0079]-[0080]. A POSITA would have a reasonable expectation of success in incorporating PFETs in antenna switch 1700, as *Burgener* suggests, because there are only two ways to make a transistor (either as a NFET or a PFET). Thompson, ¶234; Ex. 1012, 2; Ex. 1010, 70. Thus, a POSITA would have been motivated to use PFETs in the modified *Burgener* antenna switch 1700 for use in noise-sensitive mobile phone application. Thompson, ¶234; *see Burgener*, ¶[0005].

Further, as discussed above with reference to claim 4, the gates of the FETs in *Burgener*'s antenna switch 1700 are controlled by a switch control signal in a mobile phone. Thompson, ¶235. A POSITA would have known that, when a PFET

stack is used in an antenna switch 1700, its gates would still be driven by a control signal by reversing the gate voltage. *Burgener*, ¶[0079]; Thompson, ¶235; Ex. 1012, 2.

9. Claim 7

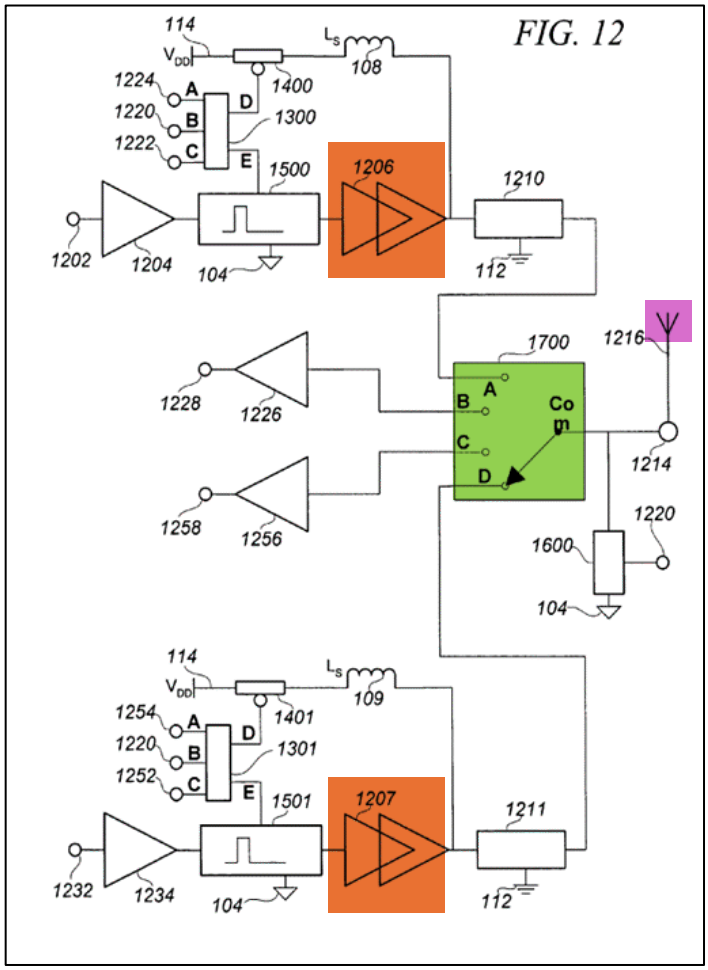
a. [7]: "The switching circuit of claim 6, wherein said switch control signal drives said gate of said PFET through at least one resistor."

Burgener teaches the additional limitation of this claim. Thompson, ¶236. As explained with reference to claim 5 of this ground, the control signal drives the gates of *Burgener*'s FETs through gate resistors (e.g., resistors 1704, 1705, 1706 of Fig. 17). *See Burgener*, Fig. 17; Thompson, ¶236. When PFETs are used in *Burgener*'s modified antenna switch 1700, the gates of the PFETs will continue to be driven by the switch control signal through gate resistors. Thompson, ¶236.

10. Claim 8

a. [8a]: "The switching circuit of claim 1, wherein a power amplifier in a wireless communications device provides an input to said switching circuit, and wherein an output of said switching circuit drives an antenna in said wireless communications device,"

Burgener teaches these additional limitations. Thompson, ¶¶237-240. *Burgener*'s RF transceiver uses a power amplifier (PA) 1206, 1207 to provide a conditioned PA signal to the antenna switch 1700, as shown below. *Burgener*, Abstract, ¶¶ [0011], [0015], [0037]; Thompson, ¶¶237-238.

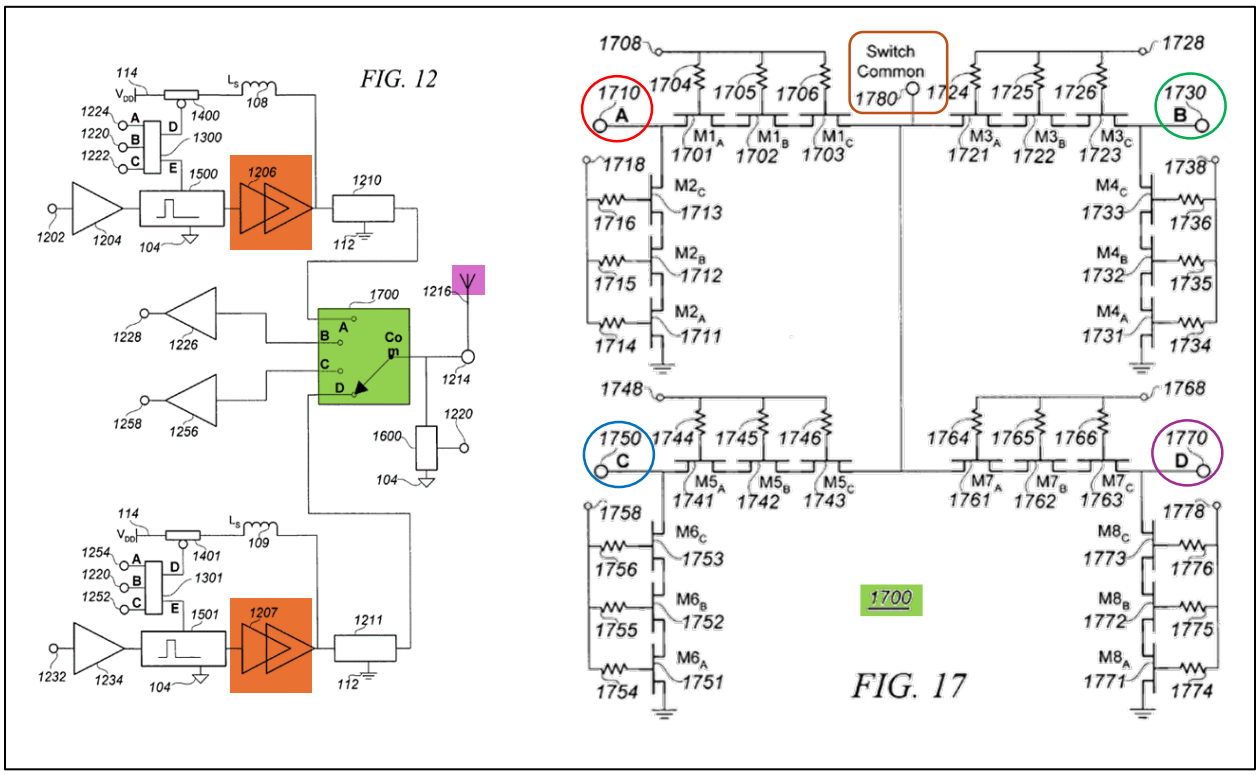


Burgener, Fig. 12. The antenna switch 1700 selectably couples the conditioned PA signal "to the antenna node 1214, from whence it may be coupled, for example by transmission line, to an antenna[.]" *Burgener*, ¶[0090]. Accordingly, the output of the antenna switch 1700 drives the antenna of a wireless communication unit, such as a cellular telephone. *Burgener*, ¶¶[0005]-[0006]; Thompson, ¶239. Thus, in *Burgener*'s wireless communication device, a power amplifier 1206 or 1207 provides an input to the antenna switch 1700, and an output of the antenna switch

1700 drives an antenna of the wireless communication device. Thompson, ¶¶238-240.

b. [8b]: "and said switching circuit is controlled by a switch control signal in said wireless communications device."

Burgener teaches the additional limitation. Thompson, ¶¶241-242. As explained *supra* §§V.E.1-V.E.2, *Burgener*'s antenna switch 1700 selectively connects different RF ports (A, B, C, D) to an antenna by applying high and low control voltages to control the RF nodes. *Burgener*, ¶¶[0090]-[0092]; Thompson, ¶¶241-242.



Burgener, Figs. 12, 17. Therefore, antenna switch 1700 is controlled by a switch control signal in the wireless communications device. Thompson, ¶242.

11. Claim 9

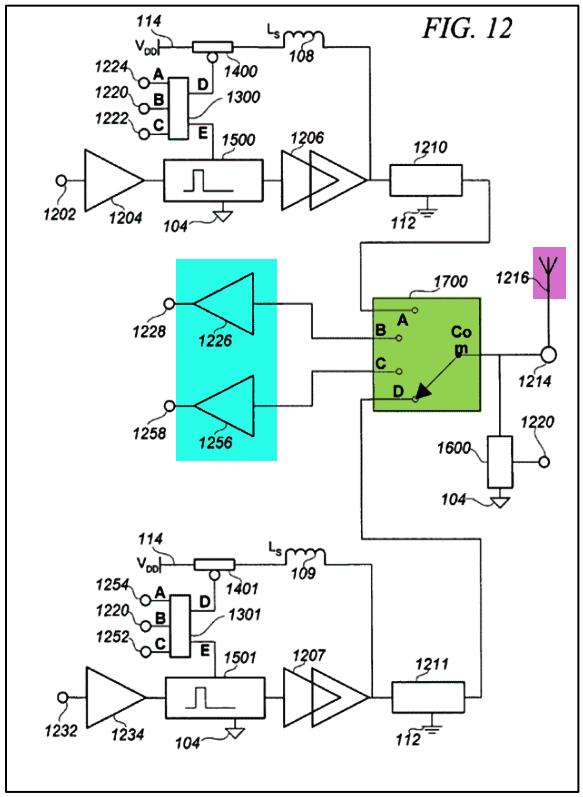
a. [9]: "The switching circuit of claim 8, wherein said wireless communications device is selected from the group consisting of a cellular telephone, a wireless personal computer, a wireless audio player, a wireless video player, and a wireless personal assistance device."

Burgener discloses the additional limitations of this claim. Thompson, ¶243. *Burgener*'s antenna switch 1700 may be used in "[w]ireless communications devices … [such as] cellular mobile telephones." *Burgener*, ¶[0005]; Thompson, ¶243.

12. Claim 10

a. [10a]: "The switching circuit of claim 1, wherein an antenna in a wireless communications device provides an input to said switching circuit, and wherein an output of said switching circuit drives a low noise amplifier in said wireless communications device,"

Burgener discloses these additional limitations. Thompson, ¶¶244-246. *Burgener*'s RF transceiver includes low noise amplifiers (LNA) 1226, 1256. *Burgener*, Abstract, ¶¶ [0005], [0037], [0092]; Thompson, ¶244.



Burgener, Fig. 12. The antenna switch 1700 selectably couples the antenna to RF ports B or C "to deliver a signal received from the antenna" to one of the LNAs 1226, 1256. *Burgener*, ¶[0092]; Thompson, ¶¶245-246. Thus, the output of the antenna switch 1700 drives a LNA in said wireless communications device. Thompson, ¶246.

b. [10b]: "and wherein said switching circuit is controlled by a switch control signal in said wireless communications device."

Burgener discloses this additional limitation. Thompson, ¶247. As discussed previously with reference to claim [8b] of this ground and §V.E.1, *Burgener*'s

antenna switch 1700 is controlled by a switch control signal in the wireless communications device. *Supra*; Thompson, ¶247.

13. Claim 11

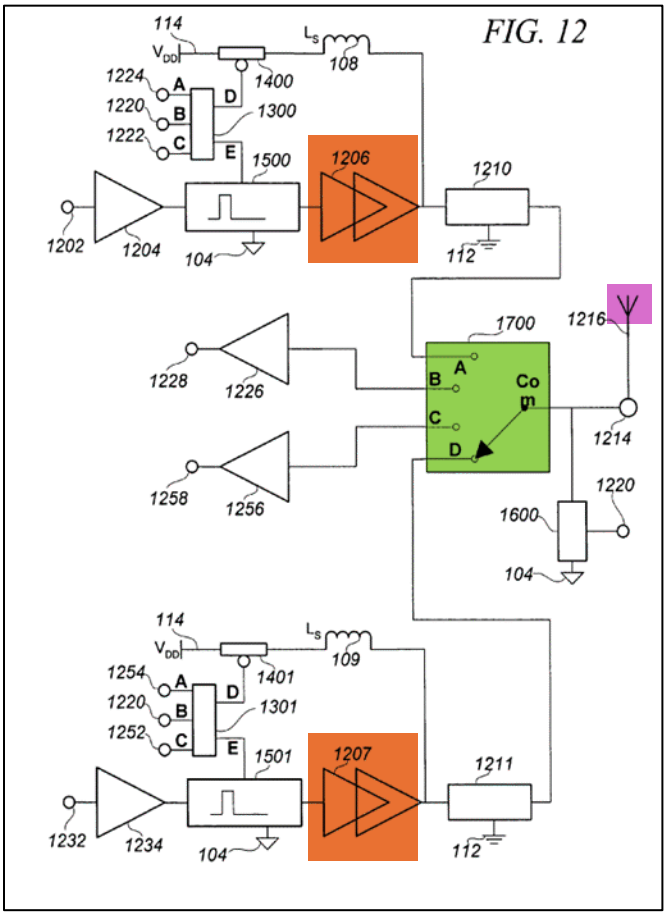
a. [11]: "The switching circuit of claim 10, wherein said wireless communications device is selected from the group consisting of a cellular telephone, a wireless personal computer, a wireless audio player, a wireless video player, and a wireless personal assistance device."

Burgener discloses this additional limitation. Thompson, ¶248. As explained in claim 9 of this ground, *Burgener*'s wireless communications device may be a cellular telephone. *Id*.

14. Independent Claim 12

a. [12pre]: "A wireless communications device comprising a power amplifier and an antenna, said wireless communications device further comprising:"

To the extent the preamble is limiting, *Burgener* discloses a "wireless communications device," such as "cellular mobile telephone" with a RF transceiver that includes power amplifiers (PA) 1206, 1207 and an antenna. *Burgener*, Abstract, ¶¶ [0005], [0037], [0090], [0093]; Thompson, ¶249.

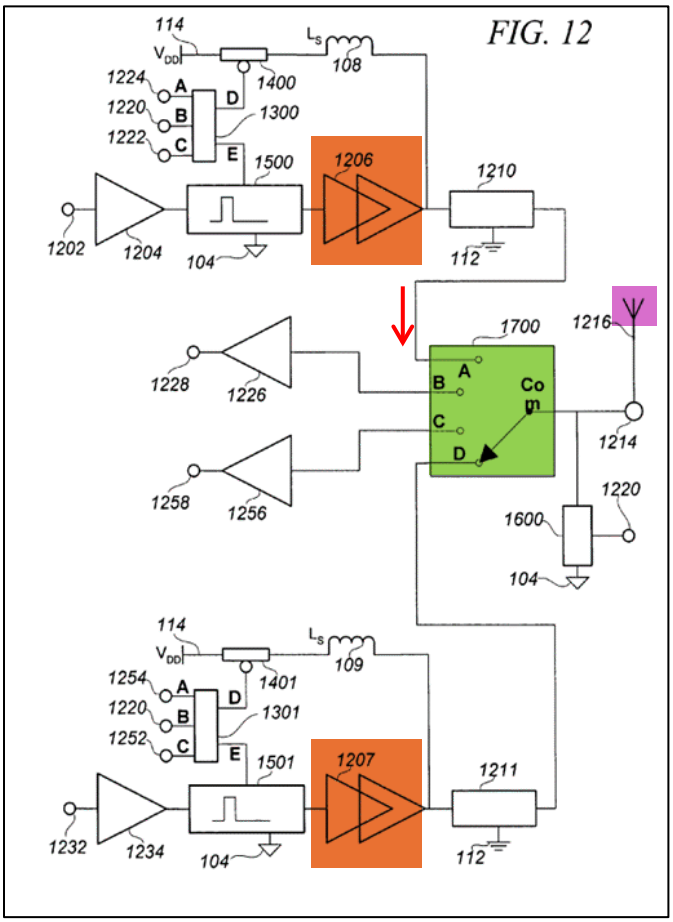


Burgener, Fig. 12.

b. [12a]: "a switching circuit controlled by a switch control signal and interposed between said power amplifier and said antenna, said switching circuit including:"

Burgener discloses this limitation. Thompson, ¶¶250-251. As explained in claim [1pre] of this ground, *Burgener*'s antenna switch 1700 is a switching circuit. *Burgener*, ¶¶[0090]-[0094], [0104]; Thompson, ¶250. As explained in claim [8b] of this ground and §V.E.1, the antenna switch 1700 is controlled by a switch control signal to select one of the RF ports A, B, C, or D. Thompson, ¶250.

Further, the antenna switch 1700 is interposed between the power amplifiers (PA) 1206, 1207 and an antenna, as shown below.



Burgener, Fig. 12. For example, the output signal from the power amplifier 1206 is directed to the port A input of the antenna switch 1700, which selectably couples this signal to the antenna 1216. *Burgener*, ¶[0090]; Thompson, ¶251. Similarly, antenna switch 1700 selectably couples output signal from the power amplifier 1207 to the antenna 1216. *Burgener*, ¶[0093]; Thompson, ¶251. Thus, antenna

switch 1700 is interposed between power amplifiers 1206, 1207 and antenna 1216. Thompson, ¶251.

c. [12b]: "a plurality of cascaded transistors …;"

Burgener in view of *Okashita* teaches these additional limitations for the same reasons stated in claim 1 of this ground. Thompson, ¶252.

d. [12c]: "at least one trench extending …."

Burgener in view of *Okashita* teaches these additional limitations for the same reasons stated in claim 1 of this ground. Thompson, ¶253.

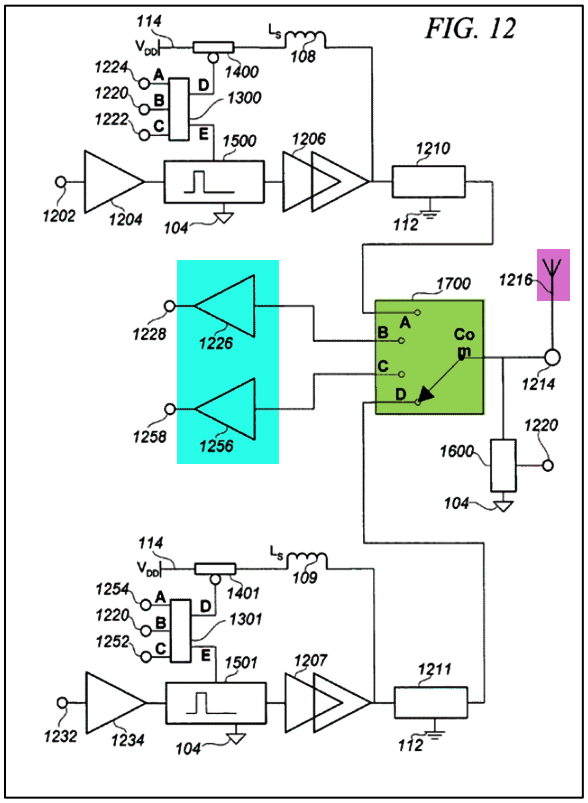
15. Claims 13-15

Burgener in view of *Okashita* renders the additional limitations of each of claims 13-15 obvious for the same reasons as stated in claims 2, 3, and 9, respectively, of this ground. Thompson, ¶254.

16. Independent Claim 16

a. [16pre]: "A wireless communications device comprising an antenna and a low noise amplifier, said wireless communications device further comprising:"

To the extent the preamble is limiting, *Burgener* discloses a "wireless communications device," such as a "cellular mobile telephone," with a RF transceiver that includes an antenna 1216, an antenna switch 1700, and low noise amplifiers 1226, 1256, as shown below. *Burgener*, Abstract, ¶¶[0005], [0037], [0092]; *supra* §V.E.1; Thompson, ¶255.



Burgener, Fig. 12.

b. [16a]: "a switching circuit controlled by a switch control signal and interposed between said antenna and said low noise amplifier, said switching circuit including:"

Burgener discloses this limitation. Thompson, ¶256. As explained in claims [1pre], [10b], and [12a] of this ground, antenna switch 1700 is a switching circuit that is controlled by a switch control signal. *Burgener*, ¶[0104]; Thompson, ¶256; *see supra* §V.E.1. Because the antenna switch 1700 delivers "a signal received from the antenna [1216] to" the low noise amplifier 1226 or low noise amplifier

1256, *Burgener*, ¶[0092], the antenna switch 1700 is interposed between the low noise amplifiers 1226, 1256 and the antenna 1216. Thompson, ¶256.

c. [16b]: "a plurality of cascaded transistors …;"

Burgener in view of *Okashita* teaches these additional limitations for the same reasons stated in claim 1 of this ground. Thompson, ¶257.

d. [16c]: "at least one trench extending …."

Burgener in view of *Okashita* teaches these additional limitations for the same reasons stated in claim 1 of this ground. Thompson, ¶258.

17. Claims 17-19

Burgener in view of *Okashita* renders the additional limitations of each of claims 17-19 obvious for the same reasons as stated in claims 2, 3, and 9, respectively, of this ground. Thompson, ¶259.

F. Ground 6: Claims 1-19 Are Obvious Over *Burgener*, *Okashita*, and *Yu*

1. Combining *Burgener* with *Okashita* and *Yu*

As explained in Ground 5, *supra*, it would have been obvious for a POSITA to:

(1) isolate *Burgener*'s cascaded FETs, as *Okashita* teaches, to prevent leakage of radio frequency signals between these cascaded FETs—Thompson, ¶260; and

(2) maintain an intervening silicon layer, as *Okashita* teaches, to separate the source/drain junctions of these FETs from the buried oxide layer to decrease the operating temperature of the FETs and thereby improve their performance and reliability—Thompson, ¶260; *see* Ex. 1010, 60; Ex. 1013, 27.

To the extent that Patent Owner contends otherwise, this would have been obvious in further view of *Yu*, for the same reasons as stated in Ground 3, *supra*. Thompson, ¶261. *Yu* teaches two "important" features to reduce problems for devices formed in a conventional SOI process:

(1) maintaining a sufficiently "thick" intervening silicon layer so that the doped regions "do not extend to the buried oxide layer"– *Yu*, 6:46-54; Thompson, ¶261; and

(2) using trench insolation structures that remain *completely* outside of the active device region–*Yu*, 5:16-19 ("The STI regions 36 do not extend into the LVT-SCR device nor do they separate the first or second type doped regions [formed in silicon layer 42, 44]."); Thompson, ¶261.

See also Yu, 2:4-17; *see also* Ex. 1010, 60; Ex. 1013, 27-28. A POSITA would have been motivated to ensure that an intervening silicon layer is sufficiently thick in the active area and that the cascaded FETs are completely within an isolated

island of the active area, as *Yu* teaches, to ensure that the switching device does not fail at a lower energy dissipation level and to achieve the electrical benefits described by *Yu* (*see* 2:4-17). Thompson, ¶262. Since *Burgener*, *Okashita*, and *Yu* all disclose switching circuits with cascaded transistors having an SOI configuration, a POSITA would have had a reasonable expectation of success in incorporating *Yu*'s teaching into *Burgener* and *Okashita*. Thompson, ¶262.

2. Claims 1-19

Burgener in view of *Okashita* teaches all the limitations of claims 1-19 as described in ground 5 above. Thompson, ¶¶263-264. To the extent Patent Owner contends that *Okashita* does not explicitly mention that "each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer," as recited in claims [1b(i)], [12b], and [16b], as explained in §V.F.1, it would have been obvious in view of *Okashita* and *Yu*. Thompson, ¶¶263-264.

As explained in §V.F.1 and §V.C.2, a POSITA would have been motivated to ensure that the intervening silicon layer between the source/drain junctions of *Burgener*'s FET as modified by *Okashita* (*see supra* §V.E.2) is sufficiently thick in the active area, as taught by *Yu*, such that the source/drain junctions remain separated from the buried oxide layer to ensure that the modified *Burgener* switching device does not fail at a lower energy dissipation level and to achieve the

electrical benefits described by *Yu*. *See Yu*, 2:4-17; Thompson, ¶264. Thus, *Burgener* in view of *Okashita* and *Yu* renders obvious claims 1-19. Thompson, ¶264.

VI. Discretionary Denial Is Not Warranted

A. Denial of Institution Is Not Warranted Under *Fintiv*

Fintiv and the Office's interim guidelines dated June 21, 2022 ("Interim Procedures") require institution. Factor 6 requires institution because Petitioner presents a compelling unpatentability challenge; Factors 3 and 4 favor institution; and Factors 1, 2, and 5 are, at worst, neutral.

Factor 3 favors institution because Petitioner acted diligently and almost no parallel investment has occurred. Patent Owner served infringement contentions only on July 18, 2024. Ex. 1024. Fact discovery opened only last month, and will not close until August 18, 2025, with expert discovery closing September 22, 2025. Ex. 1025, 3. The parties will not begin claim construction until March 4, 2025, and the hearing will not take place until July 8, 2025. *Id.*

Factor 4 favors institution because this Petition additionally challenges claims 2 and 4-19, which are not involved in the litigation. Moreover, Petitioner has not served invalidity contentions, so no overlap currently exists. Petitioner reserves the right to submit a stipulation after serving invalidity contentions.

Regarding Factors 1, 2, and 5, no stay has been requested, and trial is currently scheduled for January 5, 2026, (*id.*, 1), two months before the anticipated FWD in March 2026. In these circumstances, Factors 1, 2, and 5 are at worst neutral. *Protect Animals with Satellites v. OnPoint Sys.*, IPR2021-01483, Paper 11 at 12-13, 17 (Mar. 4, 2022). Indeed, the Board has instituted with far more time between trial and FWD. *See NetNut v. Bright Data*, IPR2021-01492, Paper 12 at 9-16 (Mar. 21, 2022) (instituting IPR without stipulation and patent owner arguing trial date six months before FWD); *Protect Animals*, IPR2021-01483, Paper 11 at 18-19 (same with patent owner arguing trial date two months before FWD); Interim Procedures, 8.

Denial of institution is not warranted under *Fintiv*.

B. Denial of Institution Is Not Warranted Under 35 U.S.C. §325(d)

No other proceedings involving the ’886 patent are currently pending or have been brought before the Patent Office. Additionally, none of the asserted prior art references (*Okashita*, *Burgener*, and *Yu*) were before the Examiner during prosecution. Thus, the same or substantially the same prior art or arguments have not been previously presented to the Patent Office, and denial of institution is not warranted under §325(d).

VII. Mandatory Notices

A. Real Parties-in-Interest

The real parties-in-interest are Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc.

B. Related Matters

HID asserted the ’886 patent in *Harbor Island Dynamic, LLC v. Samsung Electronics Co., Ltd.*, Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex.).

The ’886 Patent is not related to any known pending applications.

C. Lead and Backup Counsel, and Service Information

Lead Counsel	Backup Counsel
Joshua L. Goldberg, Reg. No. 59,369 joshua.goldberg@finnegan.com Finnegan, Henderson, Farabow, Garrett & Dunner, LLP 901 New York Avenue NW Washington, DC 20001-4413 Phone: 202-408-6092 Fax: 202-408-4400	Alexander E. Harding, *pro hac vice* to be filed alexander.harding@finnegan.com, Finnegan, Henderson, Farabow, Garrett & Dunner, LLP 901 New York Avenue NW Washington, DC 20001-4413 Phone: 202-408-4324 Fax: 202-408-4400 Abhay A. Watwe, Reg. No. 59,461 abhay.watwe@finnegan.com Finnegan, Henderson, Farabow, Garrett & Dunner, LLP 1875 Explorer Street, Suite 800 Reston, VA 20190-6023 Phone: 571-203-2716 Fax: 202-408-4400

Lead Counsel	Backup Counsel
	Chen Zang, Reg. No. 81,568 chen.zang@finnegan.com Finnegan, Henderson, Farabow, Garrett & Dunner, LLP 901 New York Avenue NW Washington, DC 20001-4413 Phone: 202-408-4416 Fax: 202-408-4400 Biju I. Chandran, Reg. No. 63,684 biju.chandran@finnegan.com Finnegan, Henderson, Farabow, Garrett & Dunner, LLP 1875 Explorer Street, Suite 800 Reston, VA, 20190-6023 Phone: 571-203-2414 Fax: 202-408-4400 Shawn S. Chang, Reg. No. 81,437 shawn.chang@finnegan.com Finnegan, Henderson, Farabow, Garrett & Dunner, LLP 271 17th Street, NW, Suite 1400 Atlanta, GA, 30363-6209 Phone: 404-653-6455 Fax: 202-408-4400

Please address all correspondence to counsel at the address above. Petitioner consents to electronic service by email at the above email addresses.

VIII. Grounds For Standing

Petitioner certifies that the ’886 patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims on the grounds identified herein.

IX. Conclusion

For the reasons above, Petitioner requests institution of IPR and cancellation of each challenged claim. The Office may charge any required fees to Deposit Account No. 06-0916.

Dated: September 24, 2024

By: / Joshua L. Goldberg/
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CLAIMS APPENDIX

1. **[1pre]** A switching circuit comprising:

   [1a] a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;

   [1b(i)] each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, **[1b(ii)]** thereby forming a source/drain junction capacitance;

   [1c(i)] at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, **[1c(ii)]** thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.

2. **[2]** The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer.

3. **[3]** The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer.

4. **[4]** The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is an NFET with a gate driven by a switch control signal in a wireless communications device.

5. **[5]** The switching circuit of claim 4, wherein said switch control signal drives said gate of said NFET through at least one resistor.

6. **[6]** The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is a PFET with a gate driven by a switch control signal in a wireless communications device.

7. **[7]** The switching circuit of claim 6, wherein said switch control signal drives said gate of said PFET through at least one resistor.

8. **[8a]** The switching circuit of claim 1, wherein a power amplifier in a wireless communications device provides an input to said switching circuit, and wherein an output of said switching circuit drives an antenna in said wireless communications device, **[8b]** and said switching circuit is controlled by a switch control signal in said wireless communications device.

9. **[9]** The switching circuit of claim 8, wherein said wireless communications device is selected from the group consisting of a cellular telephone, a wireless personal computer, a wireless audio player, a wireless video player, and a wireless personal assistance device.

10. **[10a]** The switching circuit of claim 1, wherein an antenna in a wireless communications device provides an input to said switching circuit, and wherein an output of said switching circuit drives a low noise amplifier in said wireless communications device, **[10b]** and wherein said switching circuit is controlled by a switch control signal in said wireless communications device.

11. **[11]** The switching circuit of claim 10, wherein said wireless communications device is selected from the group consisting of a cellular telephone, a wireless personal computer, a wireless audio player, a wireless video player, and a wireless personal assistance device.

12. **[12pre]** A wireless communications device comprising a power amplifier and an antenna, said wireless communications device further comprising:

[12a] a switching circuit controlled by a switch control signal and interposed between said power amplifier and said antenna, said switching circuit including:

[12b] a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer, each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;

[12c] at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.

13. **[13]** The wireless communications device of claim 12, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer.

14. **[14]** The wireless communications device of claim 12, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer.

15. **[15]** The wireless communications device of claim 12, wherein said wireless communications device is selected from the group consisting of a cellular telephone, a wireless personal computer, a wireless audio player, a wireless video player, and a wireless personal assistance device.

16. **[16pre]** A wireless communications device comprising an antenna and a low noise amplifier, said wireless communications device further comprising:

[16a] a switching circuit controlled by a switch control signal and interposed between said antenna and said low noise amplifier, said switching circuit including:

[16b] a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer, each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;

[16c] at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded

transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.

17. **[17]** The wireless communications device of claim 16, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer.

18. **[18]** The wireless communications device of claim 16, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer.

19. **[19]** The wireless communications device of claim 16, wherein said wireless communications device is selected from the group consisting of a cellular telephone, a wireless personal computer, a wireless audio player, a wireless video player, and a wireless personal assistance device.

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. §42.24, Petitioner certifies that the word count of Petitioner's Petition for *Inter Partes* Review (exclusive of any table of contents, table of authorities, mandatory notices under §42.8, certificates of service and word count, and list of exhibits or claim listing) as measured by Microsoft Word is 13,918.

Dated: September 24, 2024

By: /Joshua L. Goldberg/
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§42.6(e) and 42.105(a), the undersigned certifies that on September 24, 2024, a copy of the foregoing Petition for *Inter Partes* Review, the associated powers of attorney, and Exhibits 1001-1025 were served by FedEx Priority Overnight on the correspondence address of record indicated in the Patent Office's public Patent Center system for U.S. Patent No. 7,745,886:

BEVER HOFFMAN & HARMS, LLP
c/o Carrie Reddick, Office Manager
18486 Spring Valley Drive
Grass Valley, CA 95945

Date: September 24, 2024

By: /William Esper/
William Esper
Legal Assistant and PTAB Coordinator
FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, LLP