

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. AND
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioners,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Patent No. 7,745,886

Filing Date: September 29, 2008

Issue Date: June 29, 2010

Inventors: Robert L. Zwingman and Marco Racanelli

Title: SEMICONDUCTOR ON INSULATOR (SOI)
SWITCHING CIRCUIT

PATENT OWNER'S PRELIMINARY RESPONSE

Case No. IPR2024-01402

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LIST OF EXHIBITS

Exhibit No.	Description of Document
2001	Docket Control Order, Dkt. 38, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Aug. 5, 2024)
2002	Order Denying Samsung's Motion to Stay Pending <i>Inter Partes</i> Review, Dkt. 62, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Dec. 19, 2024)
2003	Defendants' Invalidity Contentions, served on September 26, 2024, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex.)
2004	U.S. Patent No. 6,804,502 entitled SWITCH CIRCUIT AND METHOD OF SWITCHING RADIO FREQUENCY SIGNALS to Burgener et al., issued October 12, 2004

I. INTRODUCTION

On September 24, 2024, Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, “Petitioner”) submitted a Petition (Paper 1, “Petition” or “Pet.”) to institute *inter partes* review (“IPR”) of U.S. Patent No. 7,745,886 (Ex. 1001, the “’886 Patent”), challenging Claims 1-19 (the “Challenged Claims”). The Petition asserts that: (i) Claims 1, 2, 4, and 5 are anticipated by U.S. Patent No. 6,836,172 to Okashita (“Okashita” or Ex. 1004); (ii) Claims 1-7 are rendered obvious over Okashita; (iii) Claims 1-7 are rendered obvious over Okashita and U.S. Patent No. 6,737,682 to Yu (“Yu” Ex. 1005); (iv) Claims 1-3 are anticipated by Yu; (v) Claims 1-19 are rendered obvious over U.S. Patent Application Publication No. US 2006/0270367 to Burgener et al. (Ex. 1006) and Okashita; and (vi) Claims 1-19 are obvious over Burgener, Okashita, and Yu.

The Board should deny the Petition because the Petition is internally inconsistent with respect to claim construction, as it both states that no claim constructions are necessary for the Petition to be instituted, and also proposes a definition of the term “cascaded transistors,” allegedly supported by extrinsic evidence and, thus, the Petition also appears to be advocating for a particular construction of that term.

The Board should also deny the Petition for at least the reasons described briefly below.

In Ground 1, *Okashita* does not anticipate the claims because, even under Petitioner's proposed definition of "cascaded transistors," *Okashita* does not disclose this claim element. *Okashita* also does not disclose trenches for electrical isolation between the transistors as required by the claims.

In Ground 2, the Petition proposes combining embodiments in *Okashita*, but fails to provide the motivation to do so.

In Ground 3, the Petition proposes combining *Okashita* with *Yu*, but the combination fails for the same reasons as Grounds 1 and 2.

In Ground 4, the Petition does not show that the claims are anticipated by *Yu*, because *Yu* discloses that the source/drain junction of one of the transistors is coupled to the buried oxide layer.

In Ground 5, the Petition cannot meet its burden to show that the POSITA would have been motivated to fabricate the transistors in *Burgener* using the technology of *Okashita*, because *Burgener* discloses that those transistors can be fabricated using a different technology that eliminates the need for isolating trenches.

In Ground 6, the Petition adds a third reference, *Yu*, to the *Burgener-Okashita* combination, but Ground 6 fails for the same reasons as Ground 5.

As discussed below, the Petition should also be denied in the discretion of the Director under 35 U.S.C. § 314(a), as the projected Final Written Decision date in April 2026 is after the January 5, 2026 trial date in the underlying litigation.

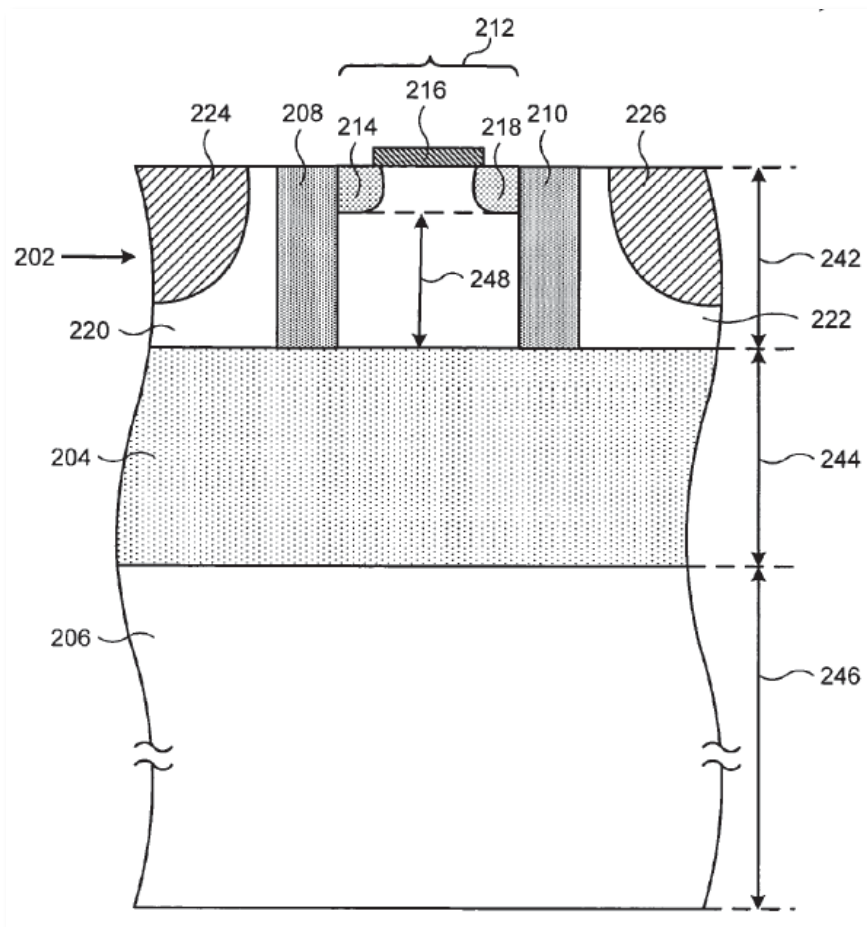
II. THE '886 PATENT

U.S. Patent No. 7,745,886 (Ex. 1001, “the ’886 Patent”) is titled “Semiconductor on Insulator (SOI) Switching Circuit” and issued on June 29, 2010. The ’886 Patent names two inventors, Robert L. Zwingman and Marco Racanelli, and was filed by and issued to Newport Fab, LLC, a subsidiary of Tower Semiconductor, Inc. which manufactures semiconductor wafers in Newport Beach, California.

The ’886 Patent describes and claims an improvement in switching circuitry that includes a number of transistors built using silicon on insulator, or SOI, technology. ’886 Patent, Abstract. According to the ’886 Patent, “it is difficult to electrically isolate semiconductor structures fabricated on conventional bulk silicon wafer” because electric current can flow under trenches. *Id.*, 1:29-36. This can be partially solved using silicon-on-insulator technology, but “circuits designed for fabrication in a bulk silicon wafer must be redesigned for fabrication in a

conventional silicon on insulator wafer, which significantly increases manufacturing and integration complexity and cost.” *Id.*, 1:43-47.

An embodiment of the invention of the '886 Patent is shown in Figure 2, below:



'886 Patent, Fig. 2. According to the '886 Patent, Figure 2 shows a SOI cross section, where a device layer 202 sits atop a buried oxide layer 204 that acts as an insulator, which sits atop a conventional bulk semiconductor layer 206. *Id.* 3:49-67. Each of

these three layers is made much thicker than typical silicon devices. *Id.*, 3:49-4:3. A transistor 212 is built in the device layer, and “[b]ecause of the increased thickness of device layer 202, source 214 and drain 218 do not extend all the way through device layer 202 to contact the top surface of buried oxide layer 204.” *Id.* 4:8-11. The source/drain junctions of the transistor have capacitances, and these capacitances “behave similarly to the junction capacitances of a transistor implemented in a conventional bulk silicon wafer, instead of a conventional SOI wafer, in part because of the greater thickness of device layer 202 compared to the thickness of conventional device layer 102.” *Id.* 4:19-24.

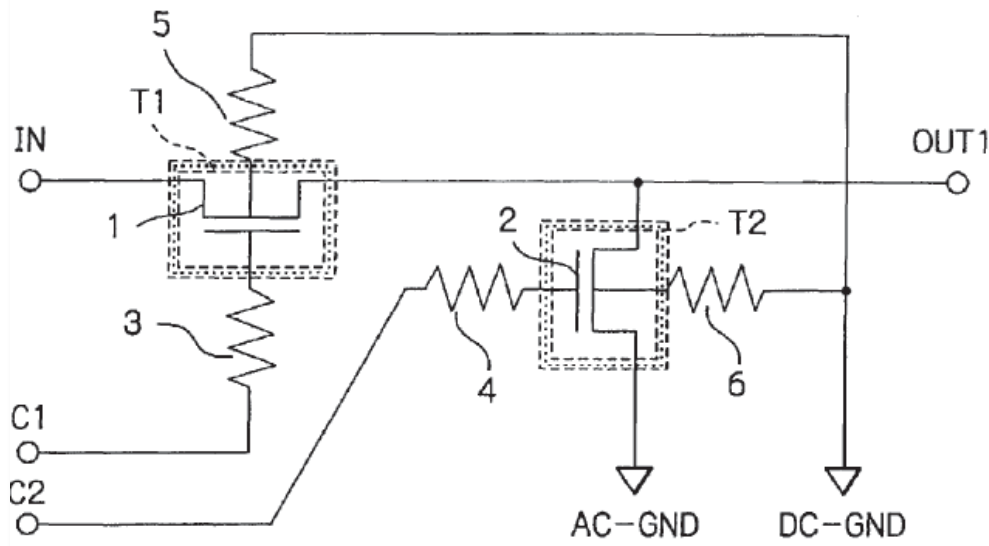
The ’886 Patent provides several advantages, including that the thick layers aid in implementing high performance circuits, and that “[a]n engineer using design methodologies suitable for conventional bulk semiconductor devices and circuits, without using specialized design techniques or device models required for conventional SOI technology, can readily design and implement high performance circuits utilizing various embodiments of the invention’s SOI transistors and other SOI structures.” *Id.*, 8:22-31.

III. THE ALLEGED PRIOR ART

A. Okashita

U.S. Patent No. 6,836,127 to Okashita issued on December 28, 2004 and is titled “Semiconductor Switch Apparatus Including Isolated MOS Transistors.” *Okashita* describes a semiconductor switch apparatus that includes “at least one shunt MOS transistor connected between one of the input terminal and the output terminal and the AC ground terminal.” Ex. 1004, Abstract. *Okashita* describes that prior art semiconductor switches using Gallium-Arsenide have a high resistance, and thus the leakage of radio signals via the substrate can be suppressed, but GaAs substrates are very expensive. *Id.*, 1:16-28. *Okashita* describes a system including a series MOS transistor T1 and a shunt MOS transistor 2, shown below in Figure 7:

Fig. 7

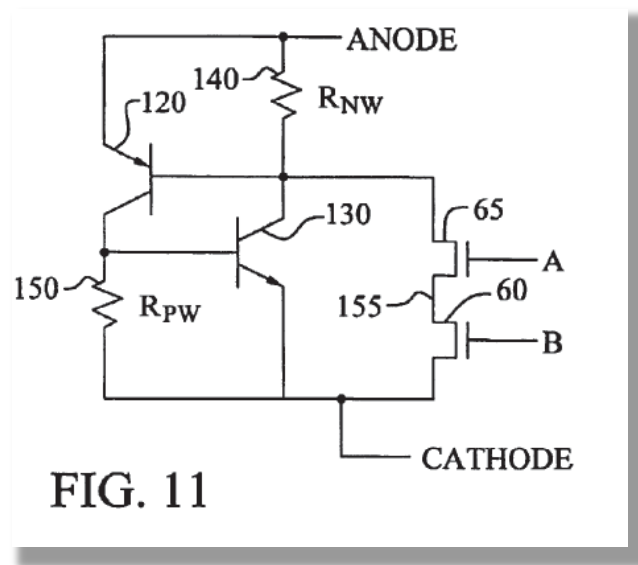


Ex. 1004, Fig. 7. According to *Okashita*, “a resistor 5 is connected between the back gate of the MOS transistor 1 and the DC ground terminal DC-GND of FIG. 3, and a resistor 6 is connected between the back gate of the MOS transistor 2 and the DC ground terminal DC-GND of FIG. 3.” *Id.*, 5:21-27.

B. Yu

U.S. Patent No. 6,737,682 to Ta-Lee Yu issued on May 18, 2004 and is titled “High Voltage Tolerant and Low Voltage Triggering Floating-Well Silicon Controlled Rectifier On Silicon-On-Insulator For Input Or Output.” Yu discloses a particular type of thyristor, called a low voltage triggering, silicon-controlled

rectifier. Ex. 1005, 1:10-14. As recognized by *Yu*, these circuits are typically used for ESD (electrostatic discharge) protection. *Id.* 1:24-27. Figure 11 of *Yu* discloses the circuitry of the silicon-controlled rectifier in *Yu*, which includes a single cathode and anode, as well as two MOS transistors with control inputs A and B:



Ex. 1005, FIG. 11. *Yu* describes that, during an ESD event, the devices 60 and 65 “operate due to the bipolar effect taking place between the source of the bottom NMOS device 60 and the drain of the top NMOS device 65” and that the silicon-controlled rectifier is “triggered by the current generated when the stacked NMOS devices 60 and 65 enter avalanche breakdown.” *Id.* 6:40-45.

Yu also discloses a cross section of this circuit, shown in Figure 10:

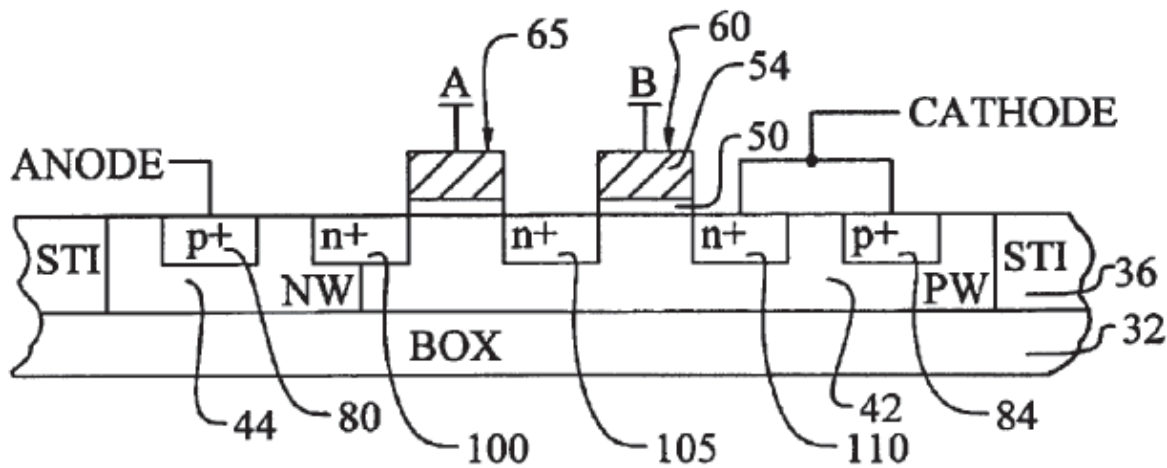


FIG. 10

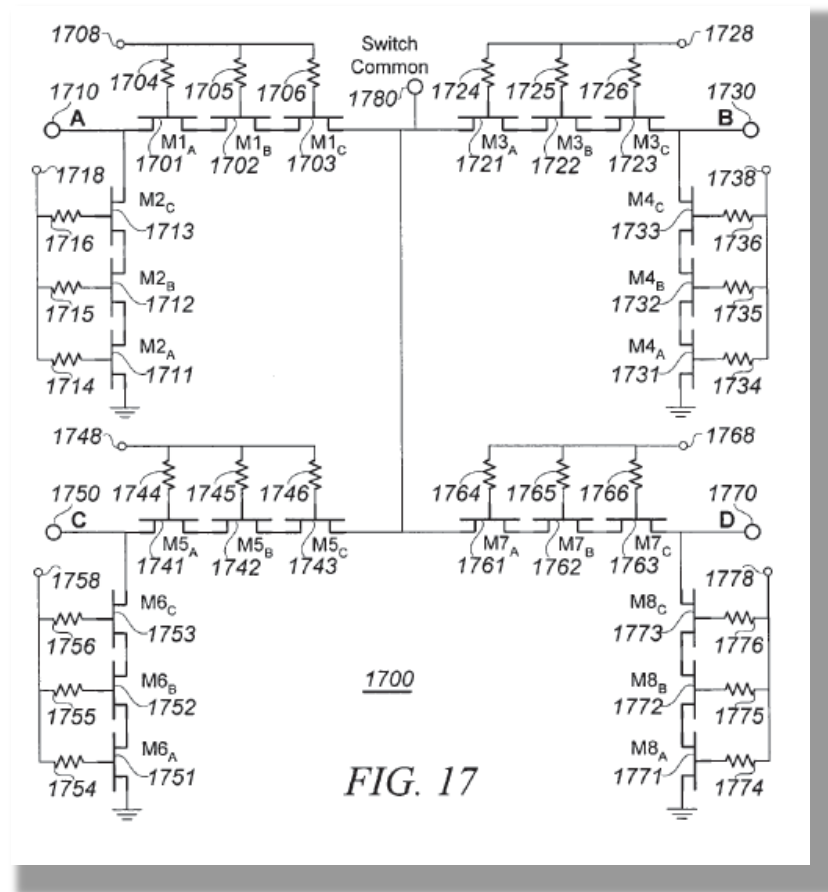
Ex. 1005, FIG. 10. Disclosed is a N-well 44 in which the anode is formed, and a P-well 42 in which the cathode is formed. *Id.*, 5:28-42. The N+ well 100 that forms the source of transistor 65 is located partly in the N-well 44 and partly in the P-well 42. *Id.*, 5:36-37.

C. Burgener

U.S. Patent Application Publication No. US 2006/0270367 was published on November 30, 2006 and is titled “Integrated RF Front End With Stacked Transistor Switch.” *Burgener* discloses an “integrated circuit (IC)” that includes “all RF front end or transceiver elements for a portable communication device,” such as a cellular telephone and other wireless communications device. Ex. 1006, Abstract, ¶ [0006].

The RF front end may be implemented by stacks of multiple Field Effect Transistors (FETs) connected in series to operate as a switching device. *Id.*, Abstract, ¶ [0009].

Burgener discloses an “antenna switch 1700” that directs input signals from an antenna to amplifiers, and output signals from the power amplifiers to the antenna, shown in Figure 17:



Ex. 1006, FIG. 17. *Burgener* states “FIG. 17 is a simplified schematic of exemplary circuitry 1700 for an antenna switch. Further details regarding design and fabrication

of such an RF switch may be found in U.S. Pat. No. 6,804,502, issued Oct. 12, 2004 and entitled ‘Switch Circuit and Method of Switching Radio Frequency Signals.’” Ex. 1006, ¶ [0101]. U.S. Patent No. 6,804,502 (Ex. 2004, “*Burgener II*”) states that the transistors in the RF switch can be made using ultra-thin silicon-on-sapphire technology, which eliminates the need for “[t]raditional transistor isolation wells” that are used for thick silicon. Ex. 2004, 10:66-11:1.

IV. LEVEL OF ORDINARY SKILL IN THE ART

For the purposes of this Preliminary Response only, Patent Owner utilizes Petitioner’s proposed level of skill in the art: “at least a master’s degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems and semiconductor dice. Additional relevant work experience can compensate for less education, and *vice versa*.” Pet. at 6 (citations omitted).

V. CLAIM CONSTRUCTION

Petitioner asserts that no claim terms need construction “to resolve the controversy in this forum.” . Pet. at 5. However, Petitioner contradicts this position in its own Petition by proposing a dictionary definition for the meaning of “cascaded transistors.” Pet. at 10 (“‘Cascaded transistors’ refer to transistors ‘arranged in a series or in a succession of stages so that each stage derives from or acts upon the

product of the proceeding”). Petitioner’s contrary positions on claim construction in its Petition are sufficient grounds to deny institution. 37 C.F.R. § 42.104(b)(3); *see also OrthoPediatrics Corp. v. K2M, Inc.*, IPR2018-01548, Paper 9 at 9-11 (P.T.A.B. March 1, 2019) (holding Petition insufficient where petitioner stated that no specific claim term requires construction, and alternatively stated that the petition is based on the claim constructions “urged by Patent Owner in the related district court litigation.”). Therefore, the Petition fails for this reason alone.

As discussed below, even assuming the interpretation of this claim term as advanced by Petitioner, each of Petitioner’s grounds for anticipation and obviousness fail. Therefore, it is not necessary for the Board to construe this claim term or reach this issue in order to deny institution.

**VI. PETITIONER HAS NOT DEMONSTRATED A REASONABLE
LIKELIHOOD OF SUCCESS FOR THE GROUNDS
ADVANCED IN THE PETITION, AND THE PETITION
SHOULD BE DENIED**

In order to anticipate the claimed invention, a prior art reference must “disclose all elements of the claim within the four corners of the document,” and it must “disclose those elements ‘arranged as in the claim.’” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). “However, a reference can

anticipate a claim even if it ‘d[oes] not expressly spell out’ all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would ‘at once envisage’ the claimed arrangement or combination.” *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015) (quoting *In re Petering*, 301 F.2d 676, 681 (C.C.P.A. 1962)).

The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) so-called secondary considerations where in evidence. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966); *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1537 (Fed. Cir. 1983).

The Board has held that a failure to identify the differences between the claimed subject matter and the prior art is fatal to an obviousness challenge. See *Apple, Inc. v. Contentguard Holdings, Inc.*, IPR2015-00355, Decision Denying Institution of *Inter Partes* Review, Paper 9 at 9-10 (P.T.A.B. June 26, 2015)

(denying institution for failure to identify the differences between the claimed subject matter and the prior art).

In arriving at an obviousness determination, the Board must sufficiently explain and support the conclusions that the prior art references disclose all the elements recited in the Challenged Claims and a relevant, skilled artisan not only could have made, but would have been motivated to combine all the prior art references in the way the patent claims and reasonably expected success. *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017). That is, even if all the claim elements are found across a number of references, an obviousness determination must consider whether a person of ordinary skill in the art would have the motivation to combine those references. *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1368 (Fed. Cir. 2016); *Los Angeles Biomedical Rsch. Inst. at Harbor-UCLA Med. Ctr. v. Eli Lilly & Co.*, 849 F.3d 1049, 1067 (Fed. Cir. 2017) (vacating and remanding an obviousness determination, in part, because the Board did not make factual finding as to whether there was an apparent reason to combine all three prior art references to achieve the claimed invention and whether a person of skill in the art would have had a reasonable expectation of success from such a combination). This combinability determination, as supported by an

articulated motivation to combine, requires a plausible rationale as to why those prior art references would have worked together. *Broadcom Corp. v. Emulex Corp.*, 732 F.3d 1325, 1335 (Fed. Cir. 2013). Absent some articulated rationale, a “common sense” finding is no different than the conclusory statement “would have been obvious.” *In re Van Os*, 844 F.3d 1359, 1361 (Fed. Cir. 2017). Of additional importance, “knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references” *Innogenetics, N.V. v. Abbott Lab’ys.*, 512 F.3d 1363, 1373 (Fed. Cir. 2008).

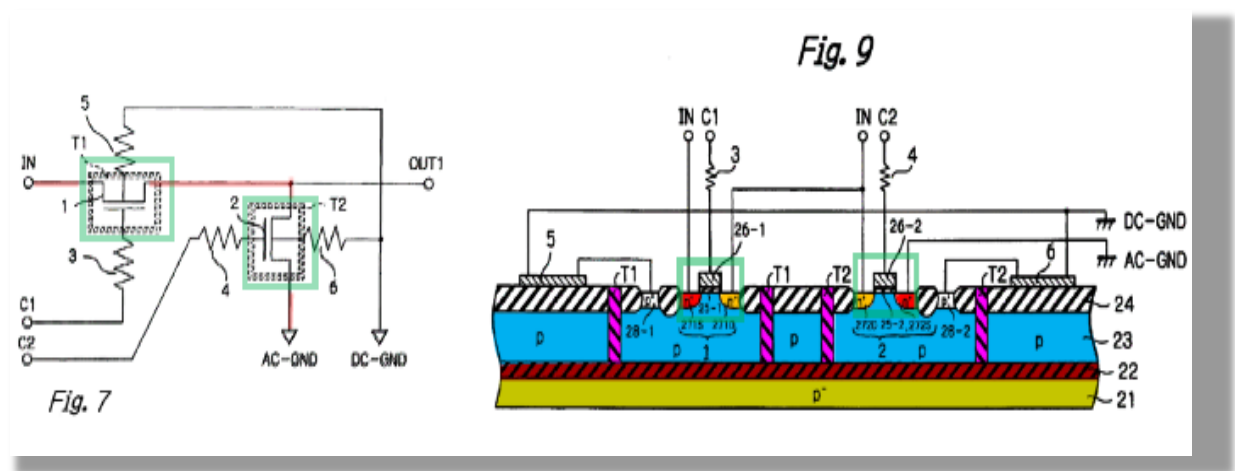
To demonstrate inherent obviousness, an inherent limitation must necessarily be present in the combination of references. *See Pers. Web Techs., LLC v. Apple, Inc.*, 917 F.3d 1376 (Fed. Cir. 2019); *LBT IP I LLC v. Apple Inc.*, No. 2022-1613, 2023 WL 3914920, at *3 (Fed. Cir. June 9, 2023). It is not enough to merely show that it is likely to be present. *Id.*

**A. GROUND 1: The Challenged Claims Are Not Challenged
Claims Are Not Anticipated by *Okashita***

**1. The Petition Does Not Show that *Okashita* Discloses
“a plurality of cascaded transistors fabricated in a
device layer situated over a buried oxide layer and a
bulk semiconductor layer”**

Ground 1 only challenges Claims 1, 2, 4, and 5 of the ’886 Patent, and each of these claims require “a plurality of cascaded transistors fabricated in a device layer

situated over a buried oxide layer and bulk semiconductor layer.” ’886 Patent Cl. 1. The Petitioner argues that this disclosure is met by *Okashita*’s disclosure in Figure 7 and Figure 9, showing “MOS transistors 1, 2 are fabricated in a p-type silicon layer that is over a silicon oxide layer and a monocrystalline silicon substrate,” as well as the Thompson Declaration alleging that *Okashita*’s transistors are “cascaded” transistors. Pet. at 9-11 (citing Ex. 1002, ¶¶ 115-116; Ex. 1007, 5). The Petition provides annotated Figure 7 and Figure 9, as shown below:



Pet. at 10 (annotating Ex. 1004, Figs. 7, 9).

Petitioner alleges that the embodiment shown in Figure 7 discloses “MOS transistors 1, 2 are fabricated in a p-type silicon layer that is over a silicon oxide layer and a monocrystalline silicon substrate,” where the “MOS transistors 1, 2 are fabricated in the p-type silicon layer, the p-type silicon layer is the claimed device

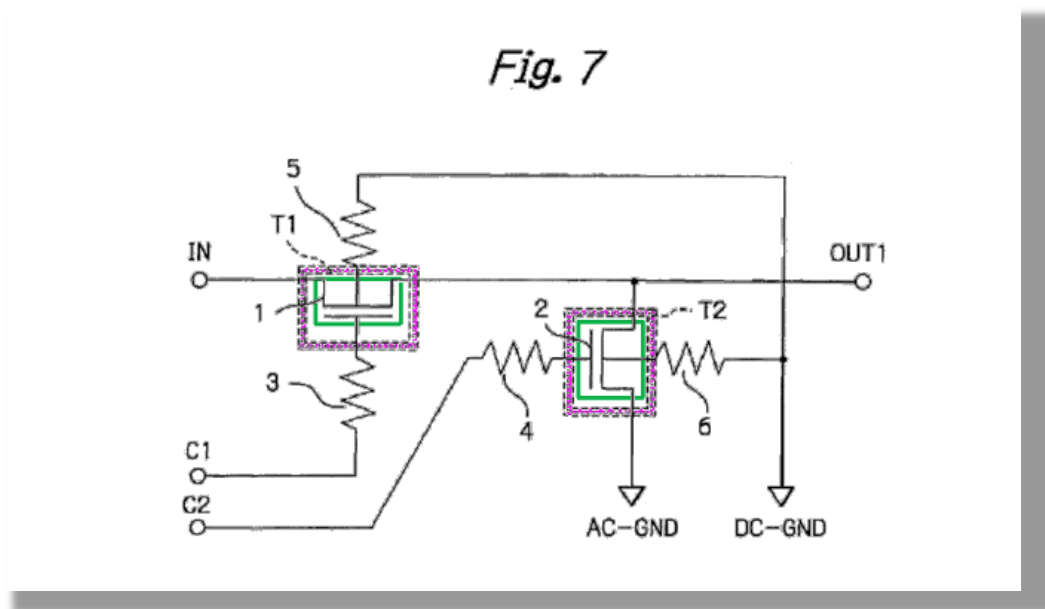
layer that is situated over a silicon oxide layer 22 and a semiconductor substrate.”
Pet. 9-10; Ex. 1002, ¶¶ 115-116).

Okashita does not disclose the requisite claim elements, because the transistors 1 and 2 in *Okashita* are not “cascaded” under Petitioner’s own definition. Petitioner claims that *Okashita*’s MOS transistors 1, 2 are “cascaded” transistors. Pet. at 10; Ex. 1002, ¶¶ 115-116. While Dr. Thompson claims that “cascaded transistors” refer to transistors “arranged in a series or in a succession of stages so that each stage derives from or acts upon the product of the preceding,” his explanation of Figure 7 in *Okashita* does not align with his own statement. Dr. Thompson states that:

[W]hen control voltages of 3V and 0V are applied to control terminals C1 and C2, MOS transistor 1 is turned ON and MOS transistor 2 is turned OFF, thereby transferring radio frequency signals applied to input terminal (IN) to output terminal (OUT). *Okashita*, 7:7-12; see *Okashita*, 3:11-16, 5:21-45, 4:11-18. When the amplitude of the radio frequency signal applied to input terminal (IN) is ΔV_{in} , $\frac{1}{2} \Delta V_{in}$ gets applied between the drain and gate of MOS transistor 2. *Okashita*, 7:12-15. When $\frac{1}{2} \Delta V_{in}$ exceeds the threshold voltage of MOS transistor 2, it would turn ON and the radio frequency signals passing through MOS transistor 1 would pass through MOS transistor 2 to the ground.

Ex. 1002, ¶ 116. In this configuration, Transistor 2 does not derive upon the acts of the preceding Transistor 1. Instead, Transistor 2 must turn ON based on the acts of input terminal (IN). When $\frac{1}{2} \Delta V_{in}$ exceeds the threshold voltage of MOS transistor 2, Transistor 2 will turn ON and Transistor 2 merely acts as a ground shunt. *See* Ex. 1004, 6:8-16. Transistor 2 does not “derive from or act upon the product” of Transistor 1, because Transistor 2 merely provides a path to ground when it is turned on by a separate control signal C2. If Transistor 2 is off, it is invisible to Transistor 1. If it is on, the output of Transistor 1 is irrelevant because everything output from Transistor 1 is shunted to AC-Ground. Ex. 1004, Fig. 7.

The Petition, citing Figure 7 in *Okashita* shown below, further argues that Transistor 1 and Transistor 2 are in the “same configuration,” as described by the ’886 Patent:



Pet. at 7 (annotating Ex. 1004, Fig. 7). This is false. A POSITA would recognize that, although Transistor 1 in Figure 7 is connected to the IN and OUT1 terminals, Transistor 2, which is merely a shunt resistor, is not cascaded with Transistor 1. Transistor 1 and Transistor 2 also have different control signals, C1, and C2, respectively. This not only fails to disclose the Challenged Claims, but actively teaches away from the '886 Patent. Because Transistor 1 and Transistor 2 in *Okashita* are not “cascaded” under Petitioner’s own definition of that term, the Petition fails to allege that *Okashita* anticipates the '886 Patent.

2. The Petition Does Not Show that *Okashita* Discloses “thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer”

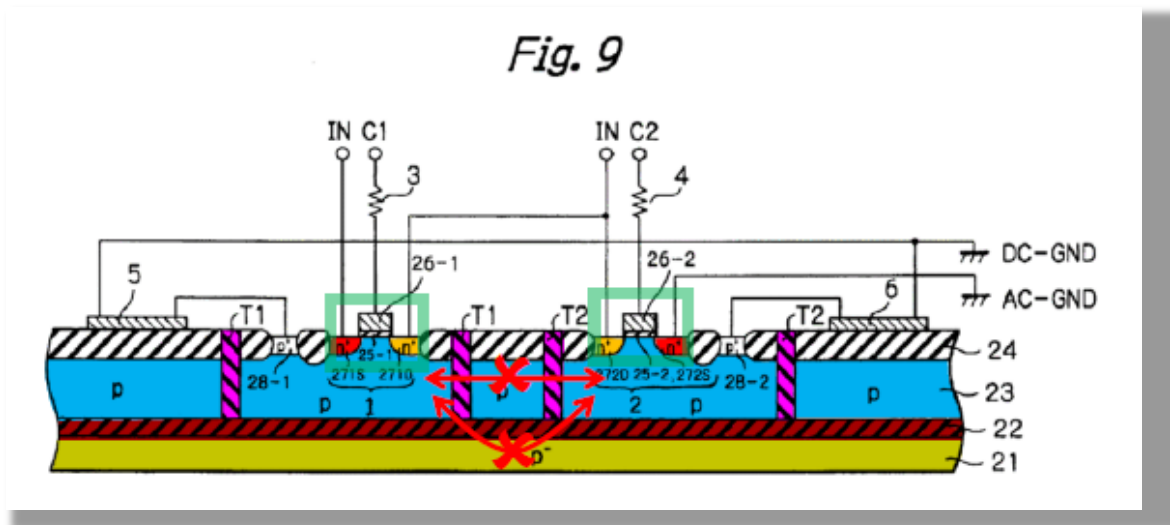
Petitioner mischaracterizes *Okashita*’s mechanical isolation trenches as providing electrical isolation. Petitioner relies on *Okashita*’s “trench insulating layers” T1 and T2. Pet. at 18. “*Okashita* further explains that, because the trenches T1, T2 extend through the silicon layer 23 and contact a top surface of the silicon oxide layer 22, leakage of electrical signals between the MOS transistor 1 and MOS transistor 2 through the silicon layer 23 and through the silicon substrate 21 below the silicon oxide layer 22 is suppressed.” Pet. at 18 (citing Ex. 1004, 6:1-16).

But Petitioner’s paraphrase misrepresents the prior art. The full quotation is:

[I]n FIGS. 8 and 9, since the series MOS transistor 1 is surrounded by the trench insulating layer T1 and the shunt MOS transistor 2 is surrounded by the trench insulating trench layer T2, the leakage of radio frequency signals from the p-type silicon layer 23 surrounded by the trench insulating layer T1 for the series MOS transistor 1 via the p-type silicon layer 23 between the trench insulating layers T1 and T2 to the p-type silicon layer 23 surrounded by the trench insulating layer T2 for the shunt MOS transistor 2 can be suppressed.

Ex 1004, 6:1-16. *Okashita* never mentions silicon substrate 21 or the silicon oxide layer 22 in this section.

The Petition then presents a misleading annotation of Figure 9, shown below, adding two red “X”s where Petitioner would like for there to be electrical isolation in *Okashita*:



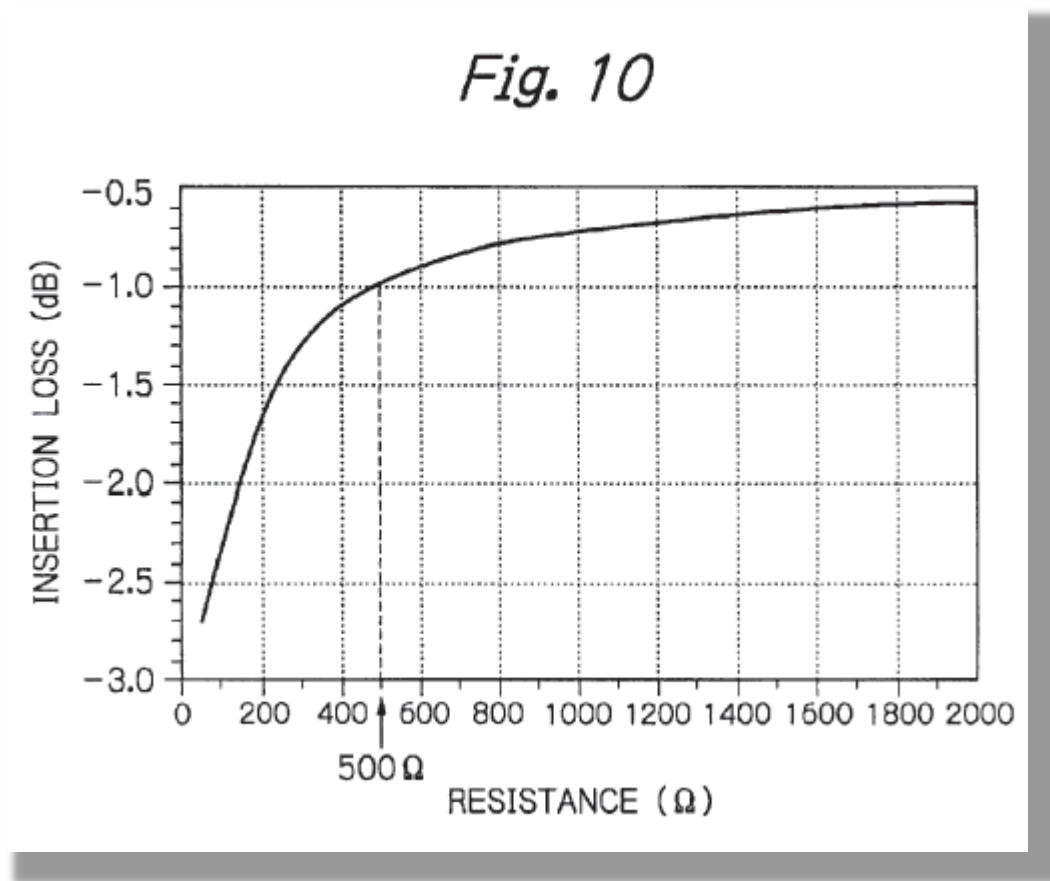
Pet. at 19 (annotating Ex. 1004, Fig. 9). The bottom “X” is irrelevant, because Claim 1 of the ’886 Patent requires reducing voltage and current in the device layer.

Additionally, the Petition misinterprets *Okashita*’s isolation entirely. The trenches T1 and T2 in *Okashita* are used for mechanical isolation only, and do “electrically isolate[e] at least one of said plurality of cascaded transistors” as required by Claim 1. ’886 Patent, Cl. 1. This is because each of the transistors shown in Figure 9 of *Okashita* is connected to the same DC Ground and the same two inputs, as shown below:

[illegible]

Ex. 1004, Fig. 9 (annotated). Nothing is “isolated” electrically between the two transistors, because of the significant number of signals connected between them. The trenches T1 and T2 in *Okashita* are used for mechanical isolation only, rather than for electrical isolation in the device layer, as required by Claim 1.

Okashita's lack of *electrical* isolation between the transistors is specifically acknowledged in its discussion of Figures 9 and 10. *Okashita* discusses insertion losses (the loss of signal energy as it travels through the circuit) due to coupling the RF signal through the ground circuits. These insertion losses are shown in Figure 10:



Ex. 1004, Fig. 10. These insertion loss characteristics are discussed at 6:26-42 of *Okashita*, and the noted “leakage current to the DC ground terminal” is evidence that the transistors T1 and T2 of *Okashita* are not electrically isolated.

Therefore, for this additional reason, the Petition fails to show that Claim 1 is anticipated by *Okashita*.

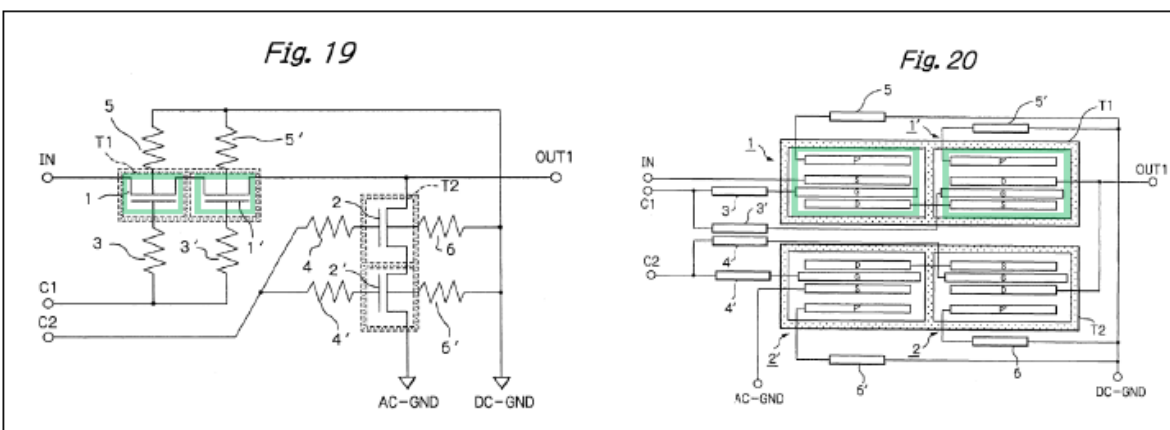
B. GROUND 2: The Challenged Claims Are Not Obvious Over *Okashita*

1. *Okashita* Does Not Render Obvious the Claimed Invention Because it Does Not Provide a POSITA with a Motivation to Create “a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer”

In an apparent recognition of the weakness of *Okashita* as an anticipatory reference, the Petition presents Ground 2 as single-reference obviousness, but relies upon a different transistor configuration shown in a different embodiment of *Okashita* to allegedly render obvious the “cascaded transistors” claim element. Since there is no disclosure of how the transistors in this other embodiment of *Okashita* are fabricated, the Petition argues that it would have been obvious to fabricate them in the same way as one another. Pet. at 29 (“A POSITA would have recognized that the MOS transistor 1’, which is connected in series to the MOS transistor 1 in Figure 7, would have also been fabricated in exactly the same way as the MOS transistor 1” (citing Ex. 1002, ¶¶ 153-155)). The Petition’s analysis is faulty, and fails to explain which of the several transistor fabrication techniques disclosed in *Okashita* would have been used to fabricate the transistors shown in Figure 20.

The Challenged Claims each require “a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk

semiconductor layer.” ’886 Patent, Cl. 1. The Petitioner argues that this limitation is rendered obvious by *Okashita*’s disclosure in its annotated Figure 19 and Figure 20, shown below, allegedly showing “a MOS transistor 1’ is ‘connected in series’ to the “MOS transistor 1 of Fig. 7.” Pet. at 28-29. Petitioner further alleges that based on these Figures, a POSITA would have recognized “that the MOS transistor 1, which is connected in series to the MOS transistor 1 in Figure 7, would have also been fabricated in exactly the same way as the MOS transistor 1,” “a POSITA would have recognized that the MOS transistor 1 would have also been fabricated in the silicon layer 23,” “and that a POSITA would recognize that both MOS transistors 1’ and MOS transistor 1 will have a similar geometry—with an intervening silicon layer separating their source/drain junctions from the top surface of the silicon oxide layer.” Pet. at 28-30 (citing Ex. 1002, ¶¶ 153-155, 159)).



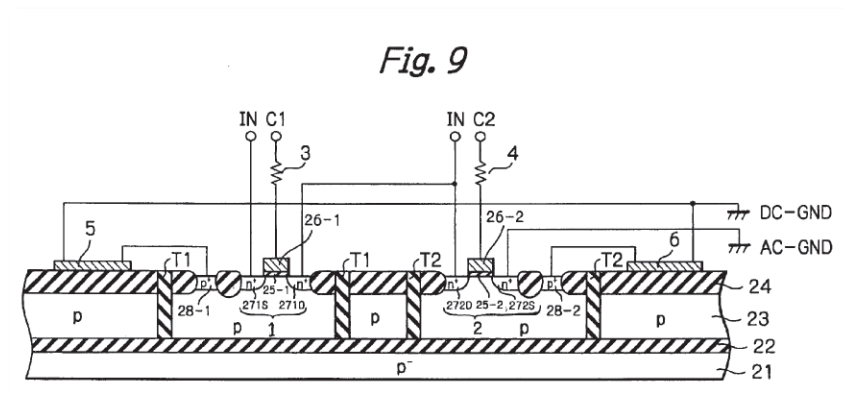
Pet. at 29 (annotating Ex. 1004 Figs. 19-20).

Petitioner begins its argument with the vague statement that “*Okashita*’s switch apparatus *may* include a plurality of transistors connected in series.” *Id.* at 28 (emphasis added). At face value, Petitioner’s ambiguous argument casts doubt as to whether the above Figures even disclose the claim limitation at issue.

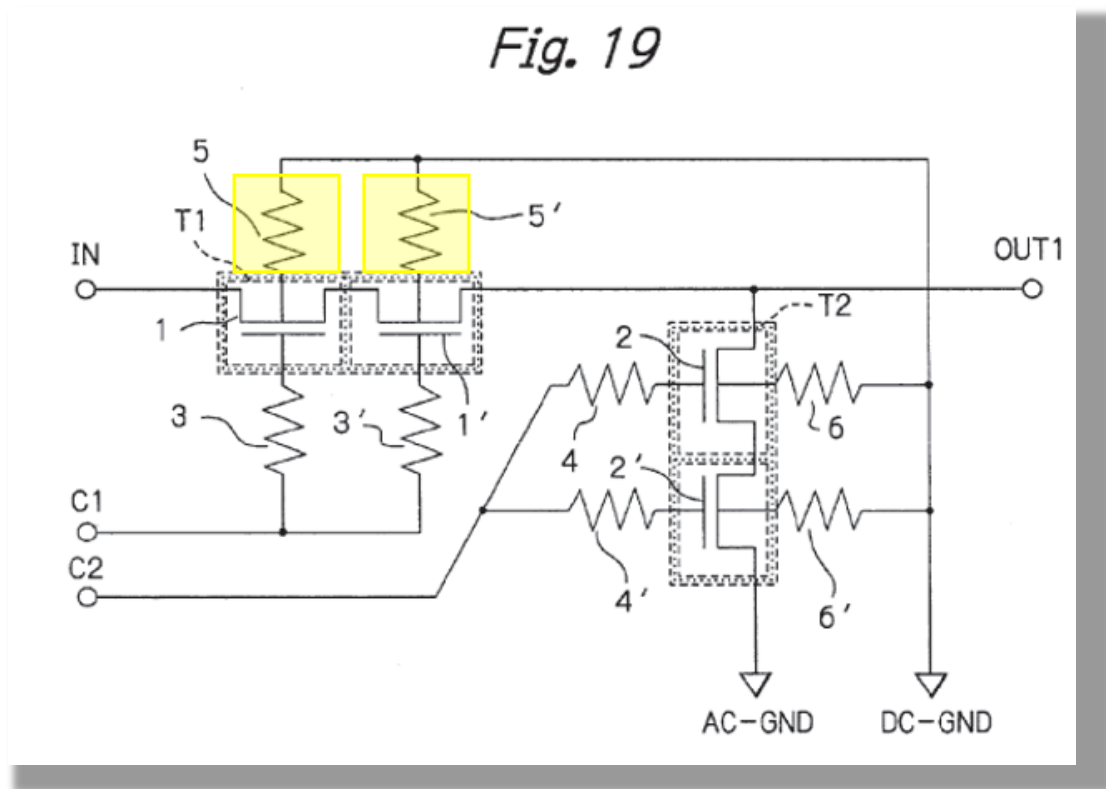
Petitioner makes further unsupported conclusory statements, by alleging that “a POSITA would have recognized that the MOS transistor 1’, which is connected in series to the MOS transistor 1 in Figure 7, would have also been fabricated in exactly the same way as the MOS transistor 1.” Pet. at 29. The Petition never explains or states which of the several disclosed transistor fabrication techniques disclosed in *Okashita* would have been used and, therefore, its obviousness analysis fails for this reason. Even ignoring *Okashita*’s discussion of the prior art, Figures 9, 11, 14, and 15 of *Okashita* and the associated text, each disclose separate transistor fabrication techniques. Because the Petition fails to state which of these techniques would be used to create the transistors in Figure 20, the Petition fails to meet its burden to show that Claim 1 is obvious.

Although it is highly improper to use an expert declaration to subvert the word limits by introducing new arguments not contained in the Petition, Petitioner cites to

the Thompson Declaration, in which Figure 9 is cited, and it is alleged that “[a] POSITA would have recognized that the MOS transistor 1 would have also been fabricated in the silicon layer 23.” Pet. at 29 (citing Thompson ¶¶ 153-154).



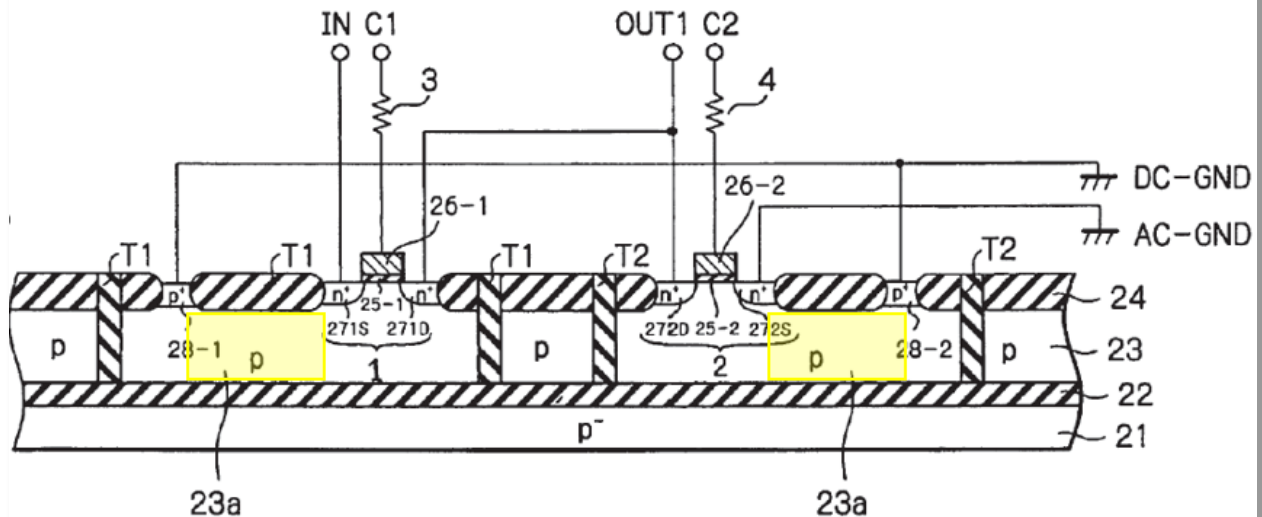
Ex. 1004, Fig. 9. Even assuming through this disclosure that the Petition meant that the transistors of Figure 20 would have been fabricated using the techniques shown in Figure 9 (despite this statement not being present in the Petition), the Petition still fails because Petitioner fails to explain why a POSITA would look to Figure 9 specifically in view of Figures 19-20. The “cascaded transistors” shown in Figures 19 and 20, relied upon by Petitioner, each contain a shunt resistor 5 and 5’ to DC ground:



Ex. 1004, Fig. 19 (annotated).

The POSITA, reviewing the disclosure of *Okashita*, would not have been motivated to use the transistor fabrication technique in Figure 9, as stated by Dr. Thompson, because other fabrication techniques disclosed in *Okashita* already have these resistors built in. For example, *Okashita*'s Figure 15 describes that the silicon layer 23 is lengthened to serve as resistors. Ex. 1004, 6:66-7:6. This is shown in the annotated Figure 15, below:

Fig. 15



Ex. 1004, Fig. 15 (annotated). The Petition makes no attempt to argue why the POSITA would have chosen to use the structure shown in Figure 9 over Figure 15, and Petitioner should not be permitted to modify its argument to refer to Figure 15 when it was specifically left out of the Petition. Therefore, Petitioner’s obviousness analysis is flawed, and the Petition should not be instituted.

2. The Petition Does Not Show that *Okashita* Discloses “thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer”

For the same reasons as described in Section VII.2, Petitioner fails to show that *Okashita* renders this Claim obvious.

C. GROUND 3: The Challenged Claims Are Not Obvious Over *Okashita* and *Yu*

- 1. The Combination of *Okashita* and *Yu* Does Not Render Obvious the Claimed Invention Because it Does Not Provide a POSITA with a Motivation to Create “a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer”**

For Ground 3, although combining *Okashita* with a different secondary reference, the Petition relies entirely on *Okashita* for this claim element. Pet. at 44. For the same reasons stated with respect to Ground 2 in Section VIII.1, *Okashita* does not render this claim element obvious because the Petition fails to disclose how the transistors disclosed in Figures 19 and 20 of *Okashita* would have been constructed and, if Dr. Thompson’s citation to Figure 9 of *Okashita* is credited despite not being cited in the Petition, then a POSITA would not have been motivated to look to this Figure in view of other Figures in *Okashita* that would have been used to construct the ground shunt resistors.

2. **The Petition Does Not Show that the Combination of *Okashita* and *Yu* Discloses “thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer”**

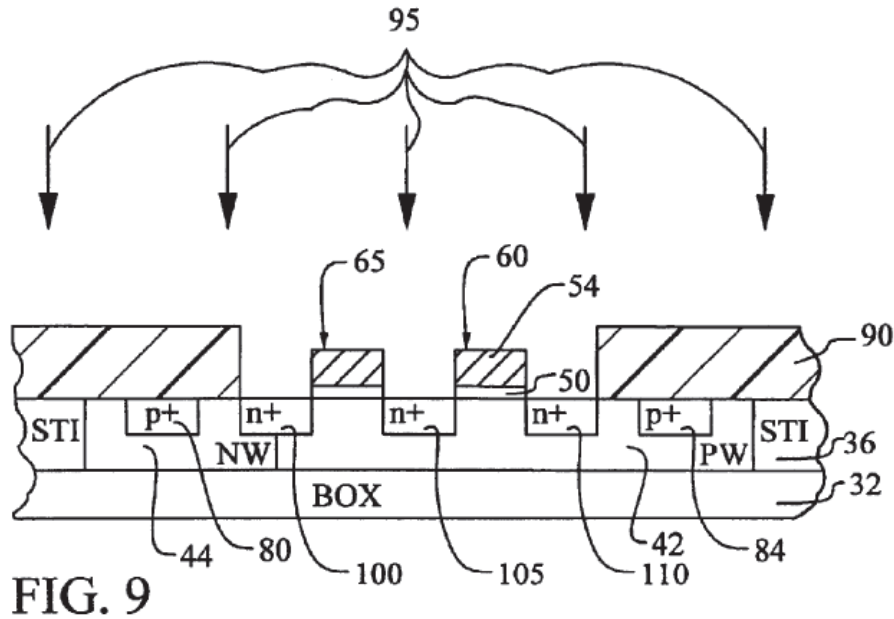
The Petition relies on *Okashita* only and the identical arguments in Grounds 1 and 2 for this claim element. As discussed above, *Okashita* does not disclose trenches for electrical isolation and, therefore, this Ground fails for the same reasons as Grounds 1 and 2. Therefore, Ground 3 also fails.

D. GROUND 4: The Challenged Claims Are Not Anticipated by *Yu*

1. **The Petition Does Not Show that *Yu* Discloses “each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer”**

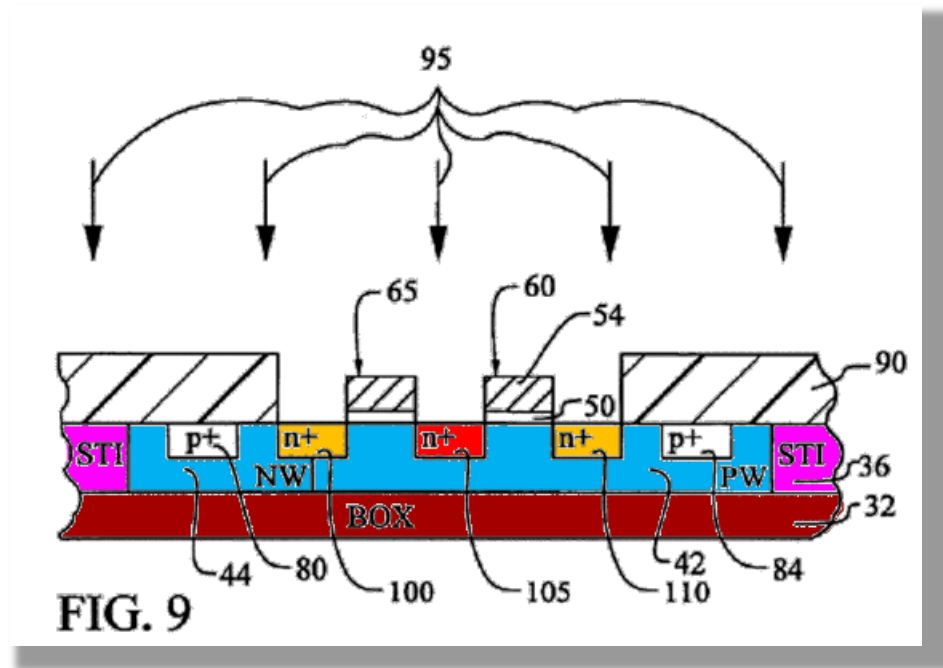
Yu does not anticipate any of Claims 1, 2, or 3 of the '886 Patent, because the Figures and disclosures in *Yu* clearly show that the source/drain junction of one of the transistors electrically contacts the buried oxide layer, as prohibited by the claims.

Yu discloses an N-well 44 and a P-well 42 built in the same layer, as shown in Figure 9:

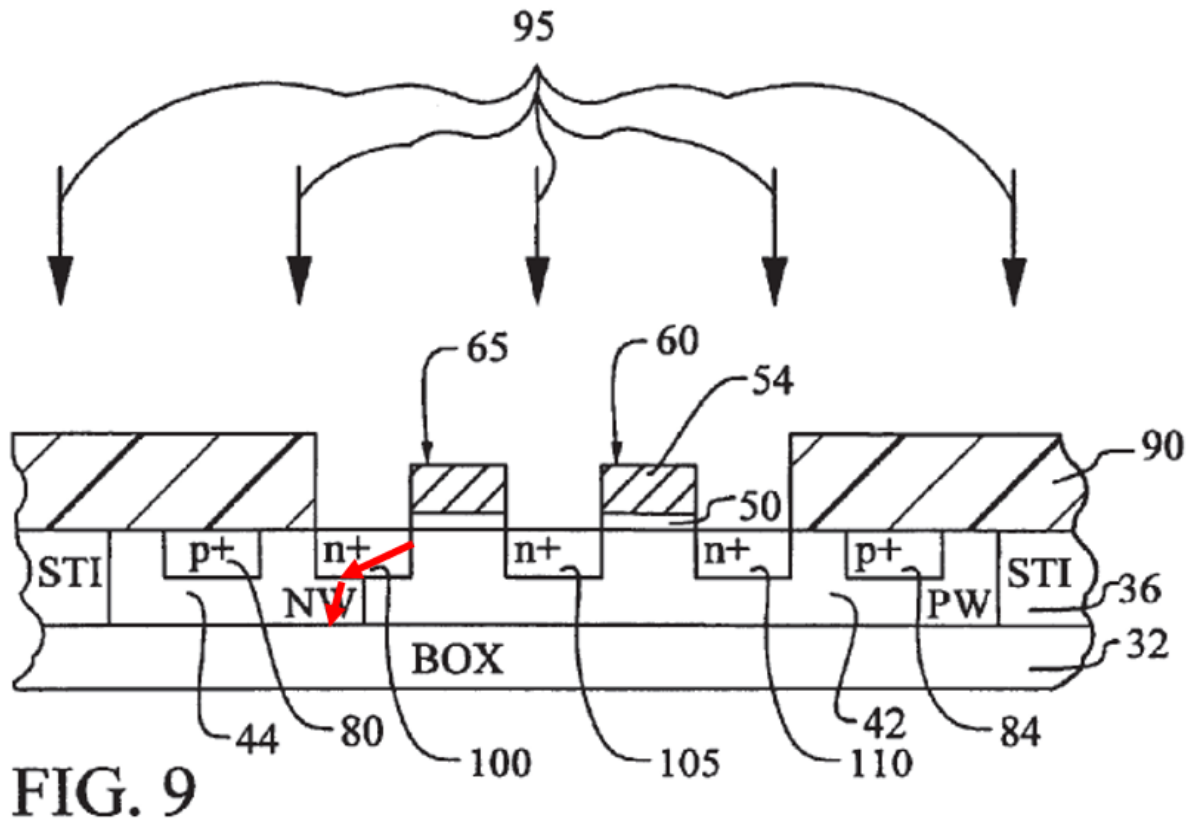


Ex. 1005, at FIG. 9; *see also* Ex. 1005, 4:16-20 (“a first well 42 of a first type is formed, and a second well 44 of a second type is formed. In the preferred embodiment, the first well 42 is p-type and is therefore called the p-well. The second well 44 is n-type and is called the n-well.”).

The Petition intentionally annotated both of these wells with the same color to disingenuously present them as a single well:



Pet. at 50-51 (annotating Ex. 1005, FIG. 9). The presence of the N-well 100 is critical to the analysis of *Yu* with respect to the '886 Patent. Because the source region of the first transistor 100 is doped N+, and is partially located in the N-Well 44, it is, in fact, electrically in contact with to the buried oxide layer as prohibited by Claim 1 of the '886 Patent. This is shown, as annotated in Figure 9 of *Yu*, below:



Ex. 1005, FIG. 9 (annotated).

In its explanation of the nearly identical Figure 10, *Yu* states, “[t]he second gate 65 is between the fourth and fifth doped regions 105 and 100. The doped regions are not separated by isolation oxide. Two MOS transistors are formed by the gates 60 and 65. In particular, a first NMOS transistor is formed by first gate 60, third doped region 110, and fourth doped region 105. A second MOS transistor is formed by second gate 65, fourth doped region 105, and fifth doped region 100. The first

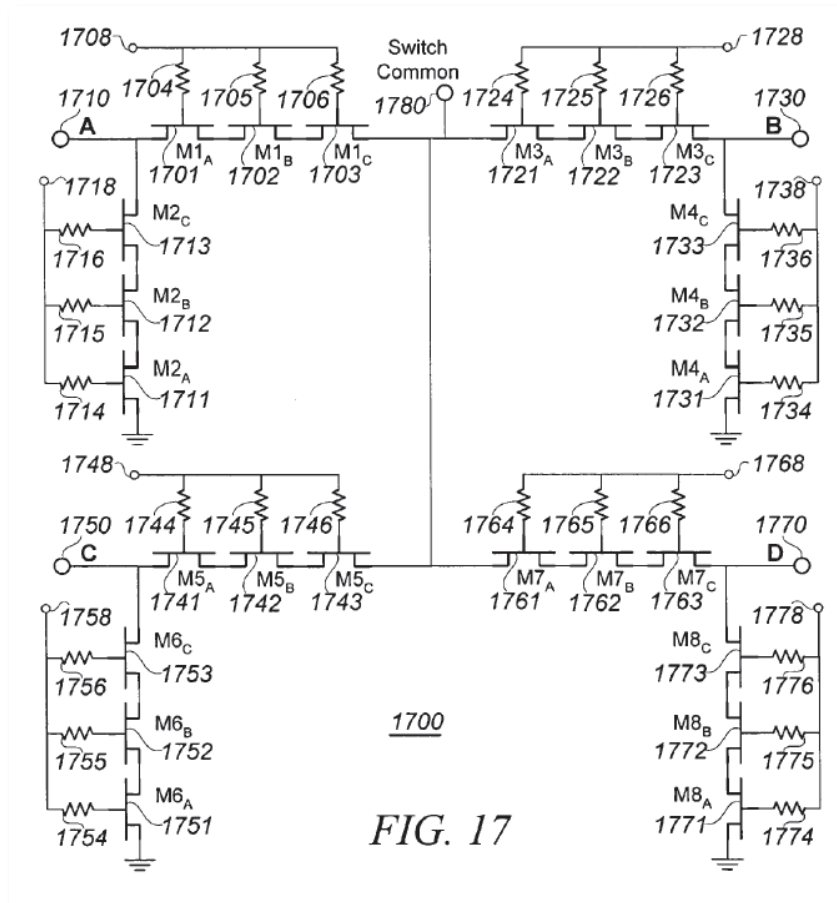
and second transistors are in series between the third doped region 110 and the fifth doped region 100. Further, the *fifth doped region 100 is coupled to the second well 44*, and the third doped region is coupled to the first doped region to form the cathode.” *Id.*, 5:41-53 (emphasis added). As *Yu* explains, the doped n+ regions form the source/drain junctions of the transistor, and as expressly stated by *Yu*, “doped region 100 is coupled to the second well 44,” and, therefore, doped region 100 (the N+ well) *does* contact the buried oxide layer. *Id.*, 5:51. Therefore, *Yu* cannot anticipate Claim 1 and Ground 4 fails.

E. GROUND 5: The Challenged Claims Are Not Obvious Over *Burgener* and *Okashita*

1. A POSITA Would Not Be Motivated to Build *Burgener*’s Antenna Switch Using the Technology of *Okashita*

Petitioner claims that “[i]t would have been obvious for a POSITA to fabricate *Burgener*’s integrated circuit (e.g., antenna switch 1700 and the corresponding cascaded FETs)” with *Okashita*’s teachings; however *Burgener* and *Okashita* disclose differing inventions that a POSITA would not be motivated to combine, and this combination does not render the Challenged Claims obvious. Pet. at 60 (citing Ex. 1002, ¶ 213).

The Petition relies on Figure 17 of *Burgener*, and argues that “it would have been obvious for a POSITA to fabricate *Burgener’s* integrated circuit (e.g., antenna switch 1700 and the corresponding cascaded FETs) using *Okashita’s* SOI configuration.” Pet. at 65 (citing Ex. 1002, ¶ 222). Figure 17 of *Burgener* is reproduced below:



Ex. 1006, FIG. 17.

A POSITA would not have been motivated to look to *Okashita* to build the transistors in *Burgener*. *Burgener*'s antenna switch shown in Figure 17 only has a common ground. But *Okashita* is entirely focused on keeping AC and DC grounds separate. Ex. 1004, Abstract (“In a semiconductor switch apparatus including an input terminal, an output terminal, an AC ground terminal, a DC ground terminal, at least one series MOS transistor connected between the input terminal and the output terminal, and at least one shunt MOS transistor connected between one of the input terminal and the output terminal and the AC ground terminal, the series MOS transistor is formed within a first region of a semiconductor layer on a silicon-on-insulator configuration surrounded by a first trench insulating layer, and the shunt MOS transistor is formed within a second region of the semiconductor layer surrounded by a second trench insulating layer.”). This problem is not present in *Burgener* because Figure 17 does not have separate AC and DC grounds that need to be kept separate.

In addition to these differences, *Burgener* also provides specific guidance to the POSITA as to how the transistors of Figure 17 would be constructed, and this guidance teaches away from using the technology of *Okashita*. In discussing Figure 17, the specific circuit of *Burgener* relied upon by Petitioner, *Burgener* states “FIG.

17 is a simplified schematic of exemplary circuitry 1700 for an antenna switch. Further details regarding design and fabrication of such an RF switch may be found in U.S. Pat. No. 6,804,502, issued Oct. 12, 2004 and entitled ‘Switch Circuit and Method of Switching Radio Frequency Signals.’” Ex. 1006, ¶ [101]. This patent, the ’502 Patent (Ex. 2004, “*Burgener IP*”), states specifically that the antenna switch is to be made with sapphire on silicon technology:

[T]he MOSFET transistors of the inventive RF switch are implemented using “Ultra-Thin-Silicon (UTSi)” (also referred to herein as “ultrathin silicon-on-sapphire”) technology. In accordance with UTSi manufacturing methods, the transistors used to implement the inventive RF switch are formed in an extremely thin layer of silicon in an insulating sapphire wafer. The fully insulating sapphire substrate enhances the performance characteristics of the inventive RF switch by reducing the deleterious substrate coupling effects associated with non-insulating and partially insulating substrates. For example, improvements in insertion loss are realized by lowering the transistor on resistances and by reducing parasitic substrate resistances. In addition, switch isolation is improved using the fully insulating substrates provided by UTSi technology. Owing to the fully insulating nature of silicon-on-sapphire technology, the parasitic capacitance between the nodes of the RF switch 30 are greatly reduced as compared with bulk CMOS and other traditional integrated circuit manufacturing technologies. Consequently, the inventive RF switch exhibits improved switch isolation as compared with the prior art RF switch designs.

Ex. 2004, 7:43-64. Additionally, *Burgener II* teaches that forming the electronic devices in a thin layer of silicon on an insulating synthetic sapphire wafer eliminates the needs for “[t]raditional transistor isolation wells” which simplifies transistor processing and increases circuit density. *Id.* 10:59-11:1.

The Petition does not address *Burgener’s* specific reference to *Burgener II*, nor does it address *Burgener II’s* disclosure that the transistors in the RF switch can be implemented using thin silicon-on-sapphire technology that eliminates the need for isolation wells as shown in *Okashita*. Given this failure, the Petition does not show that the combination of *Burgener* and *Okashita* would have been made by a POSITA, because the great weight of evidence present in *Burgener* is that the technology disclosed in *Okashita* would not be used.

Given *Burgener’s* specific reference to *Burgener II’s* disclosure of ultra-thin silicon-on-sapphire technology to build the RF antenna switch 17 of *Burgener*, Petitioner’s unsupported statements that a POSITA would have been motivated instead to look to the disclosure of *Okashita* to build the same switch using thick silicon-on-insulator technology containing the very wells that *Burgener II* states are unnecessary (Pet. at 59-63) fails.

2. The Combination of *Burgener* and *Okashita* Does Not Teach the Required Electrical Isolation

As above, the Petition relies entirely on the disclosures of *Okashita* for the electrical isolation claim elements. For the same reasons explained in Sections VII.2 and VIII.2, *Okashita* does not disclose a trench “electrically isolating” at least one of the transistors as required by Claims 1, 12, and 16 of the ’886 Patent. Therefore, the combination of *Burgener* and *Okashita* does not render the Challenged Claims obvious.

F. GROUND 6: The Challenged Claims Are Not Obvious Over *Burgener*, *Okashita*, and *Yu*

Ground 6 fails for the same reasons as Ground 5. In addition to *Burgener* and *Okashita*, the Petition adds *Yu* for claim elements not discussed in this Preliminary Response. Because *Okashita* and *Burgener* cannot be combined, and because *Okashita* does not disclose the electrical isolation claim element, Ground 6 fails for the same reasons as Ground 5.

VII. THE PETITION SHOULD BE DENIED IN THE DISCRETION OF THE DIRECTOR UNDER 35 U.S.C. § 314(A)

Based on Petitioner’s reasons regarding § 314(a), the Board should exercise its discretion to deny this Petition.

The circumstances of the parallel District Court Litigation, *Harbor Island Dynamic LLC v. Samsung Elecs. Co.*, No. 2:24-cv-00140-JRG-RSP (E.D. Tex.) necessitate denial of the Petition under the Board’s precedent, as every factor considered in relation to efficiency, fairness, and the merits supports denial. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11, at 6 (P.T.A.B. Mar. 20, 2020) (precedential) (considering (a) “whether the petitioner and the defendant in the parallel proceeding are the same party”; (b) “overlap between issues raised in the petition and in the parallel proceeding” (c) “proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision”; (d) “investment in the parallel proceeding by the court and the parties”; (e) “whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted”; and (f) “other circumstances that impact the Board’s exercise of discretion, including the merits.”).

As set forth below, these factors collectively demonstrate that efficiency and integrity of the AIA are best served by denying review. First, the Petitioner is the Defendant in the parallel proceeding. *See infra* Section VII.A. Second, the asserted claims in the District Court Litigation are all at issue in the Petition. *See infra* Section VII.B. Third, trial in the District Court Litigation is set for January 5, 2026, which

is over three months before projected statutory deadline for a Final Written Decision of this Petition in April, 2026. *See infra* Section VII.C. Fourth, the parties (and Patent Owner in particular) have invested significant resources in developing legal and factual issues of validity and infringement in the District Court Litigation and will have invested substantially more resources before any decision on this Petition. *See infra* Section VII.D. Fifth, the Court has already denied a stay pending this Petition. *See infra* Section VII.E. Finally, no other factors favor institution. *See infra* Section VII.F.

Accordingly, the Board should exercise its discretion under § 314(a) and deny the Petition because institution of this proceeding would not be consistent with the objective of the AIA to “provide an effective and efficient alternative to district court litigation.” *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8, at 20 (P.T.A.B. Sept. 12, 2018) (quoting *Gen. Plastic Indus. Co. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19, at 16–17 (P.T.A.B. Sept. 6, 2017) (precedential)).

**A. The Parallel District Court Litigation and the Petition
Involve the Same Parties**

As Petitioner notes, there exists a parallel District Court Litigation between the same parties regarding the same subject patent (the '886 Patent). Pet. at 86-87.

Petitioner is a party to the District Court Litigation captioned as *Harbor Island Dynamic LLC v. Samsung Elecs. Co.*, No. 2:24-cv-00140-JRG-RSP (E.D. Tex.). Accordingly, this factor weighs in favor of discretionary denial.

B. The District Court Litigation Involves Substantially the Same Claims

All of the asserted claims of the '886 Patent in the District Court Litigation are at issue in this Petition. “In at least these ways, the parallel proceedings would duplicate effort. This is an inefficient use of Board, party, and judicial resources and raises the possibility of conflicting decisions.” *Cisco Sys., Inc. v. Ramot at Tel Aviv Univ. Ltd.*, IPR2020-00122, Paper 15 at 10 (P.T.A.B. May 15, 2020). Accordingly, this fact weighs in favor of discretionary denial.

C. Proximity of the District Court’s Trial Date

The proximity of the District Court Litigation’s trial date to the Board’s projected statutory deadline for a Final Written Decision strongly weighs in favor of discretionary denial.

The parties’ trial is scheduled for January 5, 2026. Ex. 2001 (Docket Control Order, Dkt. 38, *Harbor Island Dynamic LLC v. Samsung Elecs. Co.*, No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Aug. 5, 2024)). Pursuant to 35 U.S.C. §§ 314(b)(1) and 316(a)(11), the projected statutory deadline for a Final Written Decision of this

Petition is April 13, 2026.¹ As the District Court’s trial will be three months before the projected statutory deadline, this factor weighs strongly in favor of denying institution. *See Supercell Oy v. Gree, Inc.*, IPR2020-00513, Paper 11 at 10-12 (P.T.A.B. June 24, 2020) (denying institution where the jury trial was scheduled to conclude approximately ten months before the statutory deadline); *Edward LifeSciences Corp. v. Evalve, Inc.*, IPR2019-01479, Paper 7, at 6-13 (P.T.A.B. Feb. 26, 2020) (denying institution where jury trial would conclude more than nine months before a final decision would be due); *Samsung Elecs. Am., Inc. v. Uniloc 2017 LLC*, IPR2019-01218, Paper 7, at 7-10 (P.T.A.B. Jan. 7, 2020) (denying institution where jury selection was scheduled for approximately six months before trial in the Board proceeding would conclude); *Next Caller Inc. v. TrustID, Inc.*, IPR2019-00961, -00962, Paper 10, at 8-16 (P.T.A.B. Oct. 16, 2019) (denying institution where trial was scheduled to conclude “several months,” before a final

¹ The statutory deadline for institution is April 13, 2025, “three months after receiving a preliminary response to the petition under section 313.” *See* 35 U.S.C. § 314(b)(1). If instituted, the statutory deadline for Final Written Decision is April 13, 2026, “not later than 1 year after the date on which the Director notices the institution of a review.”

decision would be due); *Cisco Sys., Inc.*, IPR2020-00122, Paper 15 at 8 (“Because the trial date is substantially earlier than the projected statutory deadline for the Board’s final decision, this factor weighs in favor of discretionary denial.”).

Petitioner does not contest that the proximity of the trial favors denial of institution. Thus, this factor also weighs in favor of discretionary denial.

D. Significant Investment and Petitioner’s Delay in Filing the Petition

The parties’ investment in the parallel proceeding weighs in favor of discretionary denial. In the District Court Litigation, the Court has already entered a Docket Control Order (Dkt. 38), Discovery Order (Dkt. 39), and Protective Order (Dkt. 44). Discovery is also well under way. The parties have already exchanged infringement contentions pursuant to P.R. 3-1 and invalidity contentions pursuant to P.R. 3-3. Ex. 2001 (Docket Control Order). A trial date is also set for January 5, 2026. *Id.* Thus, the parties’ and Court’s substantial investment in this proceeding weighs in favor of denial of institution under this factor.

E. No Stay of the Parallel District Court Litigation

There is no stay of the parallel District Court Litigation and, in fact, a motion for a stay by Petitioner has already been denied. *See* Dkt. 62, *Harbor Island Dynamic, LLC v. Samsung Elecs. Co.*, No. 2:24-cv-00140-JRG-RSP (E.D. Tex.

December 19, 2024). Ex. 2002. Even if the Petition were instituted and Petitioner filed another motion to stay the District Court Litigation, prejudice, tactical disadvantage to Patent Owner, the late stage of the litigation, and the lack of potential simplification would weigh strongly against such a motion. *See Lennon Image Techs., LLC v. Macy's Retail Holdings, Inc.*, 2:13-CV-00235-JRG, 2014 WL 4652117, at *1 (E.D. Tex. Sept. 18, 2014).

Moreover, a stay would not decrease the burden on the Court and the parties since any instituted IPR would not cover all of the obviousness challenges that Petitioner has raised in the District Court Litigation, and do not include Petitioner's challenges under § 101, § 102, or § 112. *See generally* Ex. 2003 (Invalidity Contentions), at 39-41, 48-51. *Intell. Ventures II LLC v. FedEx Corp.*, No. 2:16-cv-00980-JRG, Dkt. 141 at 3-4 (E.D. Tex. Oct. 24, 2017) (“[T]he instituted IPRs only cover a narrow slice of the invalidity arguments Defendants have raised in this case. For example, Defendants have argued that the ’715 Patent is invalid under § 102 with respect to at least eight references . . . under § 103 with respect to at least twenty-six combinations . . . under § 112 [], and under § 101.”).

Accordingly, it would be unlikely for the Court to hold that a stay would streamline the litigation and this factor supports denial of institution.

F. Other Factors Favor Discretionary Denial

Petitioner does not present a strong case on the merits, further supporting denial of institution. *See supra* Section VI. Petitioner also does not identify any other factors which weigh against discretionary denial. Pet. at 86-87.

Thus, when viewing the factors together, the Petition should be denied in the Director's discretion under 35 U.S.C. § 314(a).

VIII. THE BOARD SHOULD REJECT ANY LATE SOTERA STIPULATION

Petitioner has not made a *Sotera*-style stipulation that “if IPR is instituted, [Petitioner] will not pursue in the District Court Litigation any ground raised or that could have been reasonably raised in an IPR” in its Petition, which weighs further in favor of discretionarily denying institution. *See Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12, 13-14 (P.T.A.B. Dec. 1, 2020) (designated Dec. 17, 2020).

The Board should not accept any late *Sotera* stipulation after this Patent Owner Preliminary Response. Petitioner has known about the related District Court Litigation since Patent Owner filed a Complaint asserting infringement of the '886 Patent against Petitioner (February 27, 2024) over six months before the Petition (Sept. 24, 2024) and has had a docket control order for the District Court Litigation,

anticipating a trial date for January 5, 2026. Ex. 2001 (Docket Control Order). Any withholding of the *Sotera* stipulation in its Petition is gamesmanship and prejudicial to Patent Owner in this proceeding and is inconsistent with 37 C.F.R. § 42.1(b)'s mandate to “secure the just, speedy, and inexpensive resolution of every proceeding.”

Both the Board and the Director are abundantly clear that Petitioner cannot wait until after the Board renders its Institution Decision to address the issue of *Fintiv*, the Board's discretionary authority, and to submit a *Sotera* stipulation. *NXP USA, Inc. v Impinj, Inc.*, IPR2021-01556, Paper 12, 5-6 (P.T.A.B. Aug. 25, 2022); *see also id.*, IPR2021-01556, Paper 13, 3-4 (P.T.A.B. Sept. 7, 2022) (the Director finding “that the Board correctly determined that a stipulation, offered by a petitioner for the first time after a decision denying institution, is not a proper basis for granting rehearing of the decision on institution;” “[p]ermitting a petitioner to wait and see if the Board denies institution under *Fintiv*, and then offer such a stipulation for the first time on rehearing, frustrates these goals [of avoiding conflicting decisions] and would open the door to gamesmanship;” “***the only appropriate time for a petitioner to offer a stipulation related to the Fintiv factor 4 analysis is prior to the Board's decision of whether to institute review.***”) (emphasis added).

IX. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board deny institution of the Petition in its entirety.

Respectfully submitted,

Dated: January 10, 2025

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IPR2024-01402
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CERTIFICATE OF WORD COUNT

The undersigned hereby certifies that the portions of the above-captioned PATENT OWNER'S PRELIMINARY RESPONSE specified in 37 C.F.R. § 42.24 has 8,030 words in compliance with the 14,000 word limit set forth in 37 C.F.R. § 42.24. This word count was prepared using Microsoft Word for Office 365.

Respectfully submitted,

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CERTIFICATE OF SERVICE

A copy of the foregoing Patent Owner's Preliminary Response and Exhibits
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