

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. and
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,
Patent Owner.

IPR2024-01402
Patent 7,745,886 B1

Before WILLIAM V. SAINDON, GREGG I. ANDERSON, and
ARTHUR M. PESLAK, *Administrative Patent Judges*.

SAINDON, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background and Summary

Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1–19 (“the challenged claims”) of U.S. Patent No. 7,745,886 B1 (Ex. 1001, “the ’886 patent”). Harbor Island Dynamic, LLC (“Patent Owner”) filed a Preliminary Response (Paper 7, “Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review under 35 U.S.C. § 314(b) and 37 C.F.R. § 42.4(a). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” For the reasons provided below, we determine that Petitioner has demonstrated a reasonable likelihood that at least one claim of the ’886 patent is unpatentable, and we institute an *inter partes* review. 37 C.F.R. § 42.108(a).

Our findings of fact, conclusions of law, and reasoning discussed below are made for the sole purpose of determining whether the Petition meets the threshold for initiating review. This decision to institute review is not a final decision as to the patentability of any challenged claim or the construction of any claim limitation.

B. Real Parties in Interest

The parties assert that they are the sole real parties in interest. Pet. 88; Paper 5, 2 (Patent Owner’s Mandatory Notice).

C. Related Matters

The parties have identified the following pending district court cases:

- *Harbor Island Dynamic, LLC v. Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.*, Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex.) (“District Court Litigation”); and
- *Harbor Island Dynamic, LLC v. NXP Semiconductor, N.V. et al.*, Case No. 2:24-cv-00717-JRG-RSP (E.D. Tex.).

Pet. 88; Paper 5, 2.

D. Prior Art and Asserted Grounds

Petitioner’s grounds rely on the following prior art references:

Name	Reference	Exhibit No.
Yu	U.S. Pat. 6,737,682 B1, iss. May 18, 2004	1005
Okashita	U.S. Pat. 6,836,172 B2, iss. Dec. 28, 2004	1004
Burgener	U.S. Pat. App. Pub. 2006/027367, pub. Nov. 30, 2006	1006

Petitioner asserts that the challenged claims would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 4, 5	102	Okashita
1–7	103	Okashita
1–7	103	Okashita, Yu
1–3	103	Yu
1–19	103	Burgener, Okashita
1–19	103	Burgener, Okashita, Yu

E. Overview of the '886 Patent

The '886 patent is directed to a circuit for correcting distortion of radio signals, in particular:

a switching circuit including a number of transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer. Each transistor has a source/ drain junction that does not contact the buried oxide layer, thus forming a source/drain junction capacitance. The disclosed switching circuit also includes at least one trench extending through the device layer and contacting a top surface of the buried oxide layer, thus electrically isolating at least one of the transistors in the switching circuit so as to reduce voltage and current fluctuations in the device layer. The disclosed switching circuit may be coupled to a power amplifier or a low noise amplifier and an antenna in a wireless communications device, and be controlled by a switch control signal in the wireless communications device.

Ex. 1001, code (57).

F. Challenged Claims

Claims 1–19 are challenged. Claims 1, 12, and 16 are independent. Claim 1 is reproduced below.

1. A switching circuit comprising:

a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;

each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;

at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.

The issues raised by the parties at this time are limited to elements recited in claim 1. At a high level, claim 1 is directed to a switching circuit made of three layers. A device layer contains the transistors of the switching circuit situated over a buried oxide layer and a bulk semiconductor layer. The issues raised involve the requirements of claim 1 for: (1) a plurality of cascaded transistors, (2) each of the cascaded transistors to have a source/drain junction that does not contact the buried oxide layer, and (3) at least one trench extending through the device layer and contacting the buried oxide layer.

II. DISCRETIONARY ANALYSIS

Patent Owner argues that, because of co-pending district court litigation between Patent Owner and Petitioner (noted in the Related Matters section above), we should exercise our discretion to deny institution under *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”). Prelim. Resp. 40–47.

We consider the advanced state of a parallel district court action as a factor that may weigh in favor of denying a petition under 35 U.S.C. § 314(a). See *NHK Spring Co. v. Intrix-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 20 (PTAB Sept. 12, 2018) (precedential). The following factors inform our assessment of “whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel proceeding”:

- 1) whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;

2) proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;

3) investment in the parallel proceeding by the court and the parties;

4) overlap of issues raised in the petition and in the parallel proceeding;

5) whether the petitioner and the defendant in the parallel proceeding are the same party; and

6) other circumstances that impact the Board’s exercise of discretion, including the merits.

Fintiv, IPR2020-00019, Paper 11 at 5–6. Our analysis is also guided by the Chief Administrative Patent Judge’s March 24, 2025 Memorandum, “Guidance on USPTO’s rescission of ‘Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation’” (“CAPJ Memo”).¹

A. Fintiv Factor 1

Fintiv factor 1 asks whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted. Patent Owner contends this factor supports exercising our discretion to deny institution because “[t]here is no stay of the parallel District Court Litigation and, in fact a motion for a stay by Petitioner has already been denied.” Prelim. Resp. 45–46 (citing Ex. 2002, 1). Petitioner argues that this factor is “at worst neutral.” Pet. 86.

¹ Available at https://www.uspto.gov/sites/default/files/documents/guidance_memo_on_interim_procedure_rescission_20250324.pdf

Petitioner's motion for a stay of the District Court Litigation was denied "as premature" because "the Patent Trial and Appeal Board has not yet acted on a petition for *inter partes* review." Ex. 2002, 1. Although no stay of the District Court Litigation has been issued, it appears that the district court would entertain a renewed request by Petitioner for a stay after this Decision on Institution is entered. Consequently, we find that this factor is neutral.

B. Fintiv Factor 2

Fintiv factor 2 considers the proximity of the court's trial date to the Board's projected statutory deadline for a final written decision. Patent Owner contends that this factor "strongly weighs in favor of discretionary denial." Prelim. Resp. 43–45. Patent Owner argues that trial in the District Court Litigation "is scheduled for January 5, 2026" which is "three months before the projected statutory deadline" for a Final Written Decision in this proceeding. *Id.* at 44 (citing Ex. 2001). Petitioner argues that this factor is "at worst neutral." Pet. 86.

The district court's Docket Control Order, entered by the district court on August 5, 2024, sets January 5, 2026 as the date to commence jury selection in the column labelled "Original Date." Ex. 2001, 1. The column next to "Original Date" is labelled "Amended Date" and that column is blank. *Id.* The Docket Control Order is prefaced with the statement "it is hereby **ORDERED** that the following schedule of deadlines is in effect until further order of this Court." *Id.* The Docket Control Order also contemplates that the trial date may be continued under certain circumstances. *See id.* at 6 ("Motions for Continuance"). Based on this, it appears that the Docket Control Order at least contemplates the possibility of

a continuance. Nonetheless, there remains the possibility that a trial could be concluded prior to our statutory deadline in this case.

Fintiv instructs us that “the decision to institute will likely implicate other factors” when “the court’s trial date is at or around the same time as the projected statutory deadline.” *Fintiv*, IPR2020-00019, Paper 11 at 9. Given that the originally-scheduled trial date is far away, and the final decision date in this case will be approximately four months after the originally scheduled trial date, we find that this factor weighs slightly in favor of exercising our discretion to deny institution.

C. *Fintiv Factor 3*

Fintiv factor 3 asks us to consider investment in the parallel proceeding by the court and the parties. Patent Owner contends that this factor weighs heavily in favor of exercising our discretion because the district court has issued various orders, discovery is under way, and the parties exchanged infringement contentions and invalidity contentions. Prelim. Resp. 45.

Petitioner contends that this factor favors institution because it “acted diligently and almost no parallel investment has occurred.” Pet. 86. According to Petitioner, Patent Owner served infringement contentions on July 18, 2024, fact discovery does not close until August 18, 2025, expert discovery closes on September 22, 2025, claim construction efforts by the parties began on March 4, 2025, and the *Markman* hearing will not take place until July 8, 2025. *Id.* (citing Ex. 1016; Ex. 1017, 3–4).

Although the parties and district court have invested sometime in the District Court Litigation, substantial work remains to be done including the completion of fact and expert discovery, claim construction briefing and

decision, pretrial motions, and preparation of a joint pretrial order. *See* Ex. 2001, 1–5.

For these reasons, we find that this factor weighs in favor of not exercising our discretion to deny institution.

D. Fintiv Factor 4

Fintiv factor 4 asks us to consider the overlap of issues raised in the petition and in the parallel proceeding. After the Preliminary Response was filed, Petitioner submitted a stipulation stating that it will not pursue, in the District Court Litigation, any ground that was raised or could have reasonably been raised in this proceeding. Paper 8, 1. Petitioner’s stipulation aligns with the stipulation relied on by the Board in *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 at 18–19 (PTAB Dec. 1, 2020) (precedential).

Patent Owner argues that we should reject any “late” *Sotera* stipulation. Prelim. Resp. 47–48. The only authority cited for this argument are Board decisions concerning stipulations filed *after* a Decision on Institution was entered. *Id.* As Petitioner’s stipulation was filed prior to this Decision being entered, it is not “late” under the authority Patent Owner cites, and, thus, on this record, we decline to reject Petitioner’s stipulation. *See NXP USA, Inc. v. Impinj, Inc.*, IPR2021-01556, Paper 13 (Sept. 7, 2022) (precedential) (holding that the only appropriate time for a petitioner to offer a stipulation is prior to the Board’s decision on institution) cited in CAPJ Memo, 2 n.1.

In *Sotera Wireless*, the Board found that a stipulation such as the one proffered here by Petitioner addressed “concerns of duplicative efforts between the district court and the Board, as well as concerns of potentially

conflicting decisions” and “ensures that an *inter partes* review is a ‘true alternative’ to the district court proceeding.” *Sotera*, IPR2020-01019, Paper 12 at 19. For these reasons, we find that this factor weighs “strongly in favor of not exercising discretion to deny institution.” *Id.*

E. Fintiv Factor 5

Fintiv factor 5 asks us to consider whether the petitioner and the defendant in the parallel proceeding are the same party. Patent Owner contends this factor weighs in favor of exercising our discretion to deny institution because Petitioner and Patent Owner are parties in the District Court Litigation. Prelim. Resp. 42–43. Petitioner argues that this factor is “at worst neutral.” Pet. 87.

Because Petitioner is the defendant in the District Court Litigation, this factor weighs in favor of exercising our discretion to deny institution.

F. Fintiv Factor 6

Fintiv factor 6 asks us to consider other circumstances that impact the Board’s exercise of discretion, including the merits. Patent Owner contends that “Petitioner does not present a strong case on the merits, further supporting denial of institution.” Prelim. Resp. 47. Petitioner contends that the merits support institution. Pet. 86.

As discussed below, the Petition sets forth challenges that meet the reasonable likelihood standard for institution based on the present record. In addition, Petitioner has provided reasonably strong evidence in support of its position, whereas Patent Owner has only offered attorney argument that does not call into doubt any aspect of Petitioner’s case at this time. We find that this factor favors institution.

G. Fintiv Conclusion

When we evaluate the *Fintiv* factors, we take “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Fintiv*, IPR2020-00019, Paper 11 at 6. As discussed above, factor 4 weighs strongly in favor of not exercising our discretion to deny institution and factors 3 and 6 also weigh in favor of not exercising our discretion to deny institution, while factors 2 and 5 weigh slightly in various degrees in favor of exercising our discretion to deny. After consideration of all factors, we determine that efficiency, fairness, and integrity of the system are best served by not exercising our discretion to deny institution.

III. MERITS ANALYSIS

Petitioner’s grounds are based upon the prior art teachings of Okashita, Yu, Burgener, or combinations thereof. Pet. 6. Patent Owner offers specific arguments against each of the grounds, with each argument based on the limitations of claim 1. *See* Prelim. Resp. 2–3. We will proceed to analyze each ground with our focus on claim 1. Before turning to the grounds, we will briefly review the legal standards used in our merits analysis, the level of ordinary skill in the art, and any claim construction issues that need to be addressed at this time.

A. Legal Standards Used in the Merits Analysis

“In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to

each claim”)); *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

“Under 35 U.S.C. § 102(b), a prior art reference will anticipate if it ‘disclose[s] each and every element of the claimed invention . . . arranged or combined in the same way as in the claim.’” *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1341 (Fed. Cir. 2016) (alterations in original) (footnote omitted). The Federal Circuit went on to explain that “a reference can anticipate a claim even if it ‘d[oes] not expressly spell out’ all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would ‘at once envisage’ the claimed arrangement or combination.” *Id.* (quoting *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015)) (alteration in original).

A claim is unpatentable under 35 U.S.C. § 103 if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (citing 35 U.S.C. § 103 (2000)). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner asserts:

A person of ordinary skill in the art (“POSITA”) would have had at least a master’s degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems and semiconductor dice. Additional relevant work experience can compensate for less education, and vice versa.

Pet. 6 (citing Ex. 1002 ¶¶ 105–107). At this stage of the proceeding, Patent Owner applies Petitioner’s proposed level of ordinary skill in the art.

Prelim. Resp. 11. We use Petitioner’s definition for purposes of this Decision because it appears consistent with the level of skill reflected in the prior art and the ’886 patent.

C. Claim Construction

Under 37 C.F.R. § 42.100(b), we apply the claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). That is, “the words of a claim ‘are generally given their ordinary and customary meaning,’” which is “the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention i.e., as of the effective filing date of the patent application.” *Id.* at 1312–13.

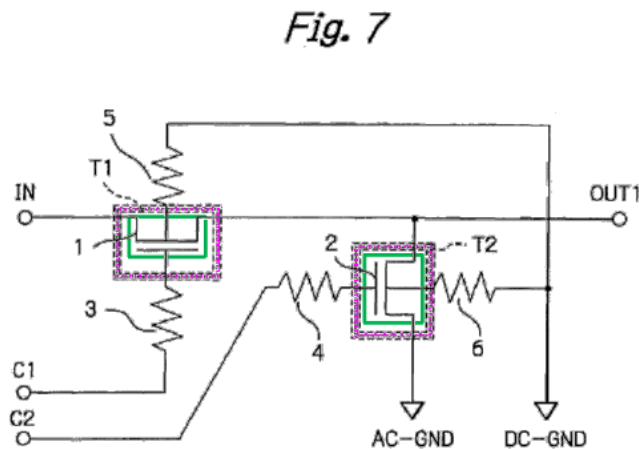
Petitioner and Patent Owner both assert that no terms require express construction. Pet. 5; Prelim. Resp. 11–12. We agree with the parties and do not construe any terms at this time. *Realtime, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

*D. Asserted Anticipation by Okashita
(Claims 1, 2, 4, and 5)*

Petitioner asserts that claims 1, 2, 4, and 5 are anticipated by Okashita. Pet. 7–28. Petitioner relies on the embodiment shown in Figures 7 and 9 of Okashita. We will provide a brief overview of Okashita before turning to the dispute between the parties.

1. Okashita

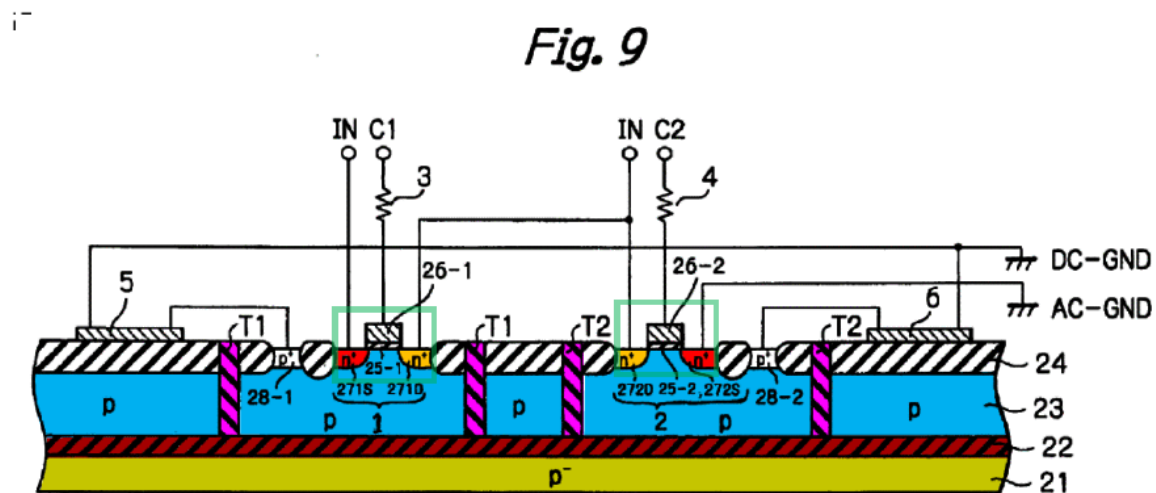
Figure 7 of Okashita, with annotations provided by Petitioner, is reproduced below:



Pet. 7 (providing an annotated copy of Ex. 1004, Fig. 7). Figure 7 of Okashita depicts a semiconductor switch apparatus. Ex. 1004, 5:21–23. Series transistor 1 (green-colored box) is connected between input terminal IN and output terminal OUT1, and shunt transistor 2 (green-colored box) is connected between output terminal OUT1 and AC ground terminal AC-

GND. *Id.* at 4:11–17.² Control terminals C1 and C2 are connected to the gates of transistors 1 and 2, and the back gates of the transistors are connected to DC ground terminal DC-GND. *Id.* at 4:17–23. Okashita states that the features in Figure 7 that distinguish it over the prior art are resistors 5 and 6, as well as isolation trenches T1 and T2 (purple-colored boxes). *Id.* at 5:29–35. The resistors and trenches are for “preventing radio frequency signals from superposing on each other.” *Id.*

Figure 9 of Okashita is a cross-sectional view of the semiconductor switch apparatus of Figure 7. *Id.* at 2:24–25; 5:36–40. An annotated version of Figure 9 of Okashita is reproduced below:



Pet. 8 (providing an annotated copy of Ex. 1004, Fig. 9). The semiconductor depicted in Figure 9 of Okashita is a semiconductor-on-insulator configuration, with base silicon substrate 21 (colored gold), silicon oxide layer 22 (colored red), and p-type silicon layer 23 (colored blue). Ex. 1004,

² Okashita does not explicitly describe all of the elements of the circuit in Figure 7. Thus, we cite Okashita’s earlier descriptions of functionally similar elements.

5:41–44. Transistor 1 is depicted as made of a gate (25-1, 26-1), source (271S, colored red), and drain (271D, colored yellow). *See id.* at 5:55–63. Notably, none of the gate, source, or drain extends down to silicon oxide layer 22. *Id.* at Fig. 9. In contrast, isolating trench T1 (colored purple) extends down to silicon oxide layer 22, surrounding p-type silicon layer 23. *Id.* at 5:46–54, Fig. 9.

2. *Petitioner’s Okashita Anticipation Ground*

Petitioner first asserts that Okashita describes the claimed three layers of the semiconductor device, namely, “a device layer situated over a buried oxide layer and a bulk semiconductor layer,” mapping these limitations onto silicon layer 23, silicon oxide layer 22, and silicon substrate 21, respectively. Pet. 9–10. Petitioner then asserts that Okashita’s transistors 1 and 2 are “cascaded transistors” as claimed because they are connected in series with respect to input terminal IN and AC ground terminal AC-GND. *Id.* at 10. Petitioner asserts that the source/drain junctions in Okashita “do[] not contact said buried oxide layer” as claimed because they are clearly shown in Figure 9 to have an intervening layer of silicon material 23 between the source/drain junctions (e.g., 271S, 271D) in the top surface of silicon oxide layer 22. *Id.* at 11–13. Lastly, Petitioner asserts that Okashita’s trenches T1 and T2 “extend through said device layer and contact a top surface of said buried oxide layer” as claimed because they are clearly shown in Figure 9 to extend all the way down to silicon oxide layer 22. *Id.* at 16–18. According to Petitioner, these trenches electrically isolate the transistors because they extend through silicon layer 23 and contact the top surface of silicon oxide layer 22. *Id.* at 18 (citing Ex. 1004, 6:1–16; Ex. 1002 ¶¶ 133–135).

3. *Disputed Limitations of Okashita Anticipation Ground*

Patent Owner focuses its Preliminary Response on the limitations in claim 1 requiring “cascaded transistors” and requiring the trenches to “electrically isolate” the cascaded transistors. Prelim. Resp. 15–23. We address each in turn.

a) “cascaded transistors”

With respect to the “cascaded transistors” limitation, Petitioner’s declarant asserts that “cascaded transistors” refer to transistors “arranged [] in a series or in a succession of stages so that each stage derives from or acts upon the product of the preceding.” Ex. 1002 ¶ 115 (citing Pet. 10). Applying this understanding to Okashita, Petitioner’s position is that transistors 1 and 2 are connected in series from the input terminal (IN) to the AC ground terminal (AC-GND) when the threshold voltage of transistor 2 is exceeded ($\Delta V_{in}/2 > V_{th}$). Pet. 10–11 (citing Ex. 1004, 7:7–17). In this situation, both transistors 1 and 2 are “on” and current flows from one into the other.

Patent Owner argues that the transistors in Okashita are not cascaded, even under Petitioner’s declarant’s definition of “cascaded transistors.” Prelim. Resp. 17–19. Patent Owner walks through the operation of the circuit in Figure 7 of Okashita and points out that when control signal C1 is on, control signal C2 is off, and vice versa. *Id.* Thus, Patent Owner’s position is that neither transistor is affected by the other. *Id.* As to Petitioner’s argument about the threshold voltage scenario ($\Delta V_{in}/2 > V_{th}$), Patent Owner argues that transistor 2 does not “derive from or act upon the product” of transistor 1 because transistor 2 merely provides a path to the ground. *Id.* at 18.

We begin our analysis by pointing out that neither party offers a claim construction of “cascaded transistors,” though both parties reference the understanding of the term set forth by Petitioner’s declarant. Although we do not reject Petitioner’s declarant’s definition, we also do not adopt it as the meaning of “cascaded transistors” at this time, absent the parties’ proposal that we do. According to the ’886 patent, transistors simply “coupled in series” are “cascaded.” Ex. 1001, 6:50–51. We use this disclosure to guide our analysis.

Reviewing Figure 7 of Okashita, we see a configuration of transistors 1 and 2 that appears, on this record, to be coupled in series. When transistor 2 acts as a shunt for transistor 1, i.e., when the threshold voltage of transistor 2 has been overcome, then current flows through transistor 1, through transistor 2, and then to ground. Ex. 1004, 7:15–17. At this preliminary stage, this is a sufficient showing that Okashita’s transistors are “cascaded” as contemplated by the ’886 patent.

b) trenches that “electrically isolate” the cascaded transistors

Petitioner identifies T1 and T2 in Okashita, which “extend through the silicon layer 23 and contact a top surface of the silicon oxide layer 22,” as the claimed trenches that electrically isolate at least one of the cascaded transistors. Pet. 18. Petitioner asserts that this structure suppresses the leakage of electrical signals between the transistors, which is consistent with the description in Okashita. *Id.* (citing Ex. 1004, 6:1–16; Ex. 1002 ¶¶ 133–135).

Patent Owner argues that Petitioner has misrepresented the prior art because Okashita “never mentions silicon substrate 21 or the silicon oxide layer 22.” Prelim. Resp. 20. Patent Owner argues that the trenches in

Okashita are for mechanical isolation, and asserts that this is because the transistors are connected to the same DC ground. *Id.* at 21–22; *see also id.* at 22–23 (citing Ex. 1004, Fig. 10).

We turn to the '886 patent for guidance as to the electrical isolation required by claim 1. In our view, the '886 patent states that the electrical isolation of the trenches is caused by the fact that they extend through the device layer and contact the buried oxide layer. First, claim 1 says that the “trench extending through said device layer and contacting a top surface of said buried oxide layer” “*thereby* electrically isolat[es] at least one of said plurality of cascaded transistors” (emphasis added). In this way, claim 1 provides a condition (“extending through . . . and contacting”) that “thereby” causes a result (“electrical isolation”). Second, the specification of the '886 patent provides a similar characterization. Ex. 1001, 3:2–5 (“Transistor 112 . . . is electrically isolated from neighboring islands 120 and 122 by trenches 108 and 110.”), 4:39–43 (“In order to achieve this isolation . . . , trenches 208 and 210 are etched to extend all the way . . . through device layer 202 and contact . . . the top surface of buried oxide layer 204.”). The '886 patent does not appear to discuss the electrical isolation as being due to any particular other features of the trenches beyond their being extended to the buried oxide layer.

Thus, on this record, it appears that Okashita's trenches cause the claimed electrical isolation by extending down to the buried oxide layer. Patent Owner provides insufficient evidence in support of its argument that the trenches in Okashita are only for mechanical isolation. In contrast, Okashita states that the function of the trenches is to suppress leakage of

radio frequency signals; a statement that indicates electrical isolation. Ex. 1004, 6:1–7.

Accordingly, on this record, we are not persuaded by Patent Owner’s arguments that the trenches in Okashita do not provide the claimed electrical isolation.

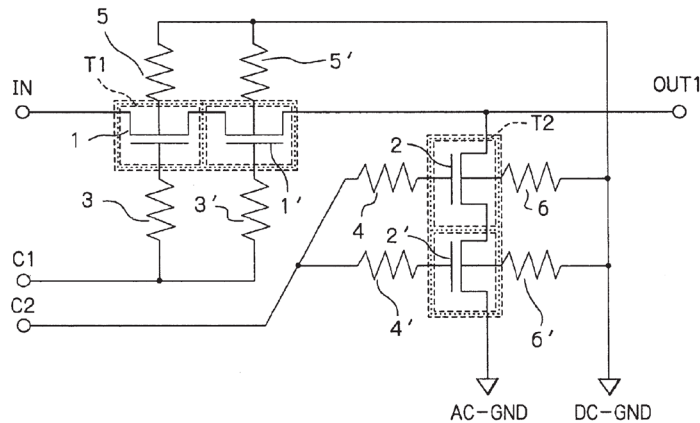
4. Conclusion for Okashita Anticipation Ground

Having reviewed the Petition and the Preliminary Response, we determine that Petitioner has established a reasonable likelihood that claim 1 is anticipated by Okashita. For the remaining claims and grounds, we will limit our analysis to the disputes raised by Patent Owner in its Preliminary Response.

E. Asserted Obviousness Over Okashita (Claims 1–7)

Petitioner asserts that claims 1–7 would have been obvious in view of Okashita. Pet. 28–39. With respect to claim 1, the difference between this obviousness ground and Petitioner’s anticipation ground is that the obviousness ground relies on an embodiment disclosed in Figures 19 and 20 of Okashita. Pet. 28–33. Figure 19 of Okashita is reproduced below:

Fig. 19



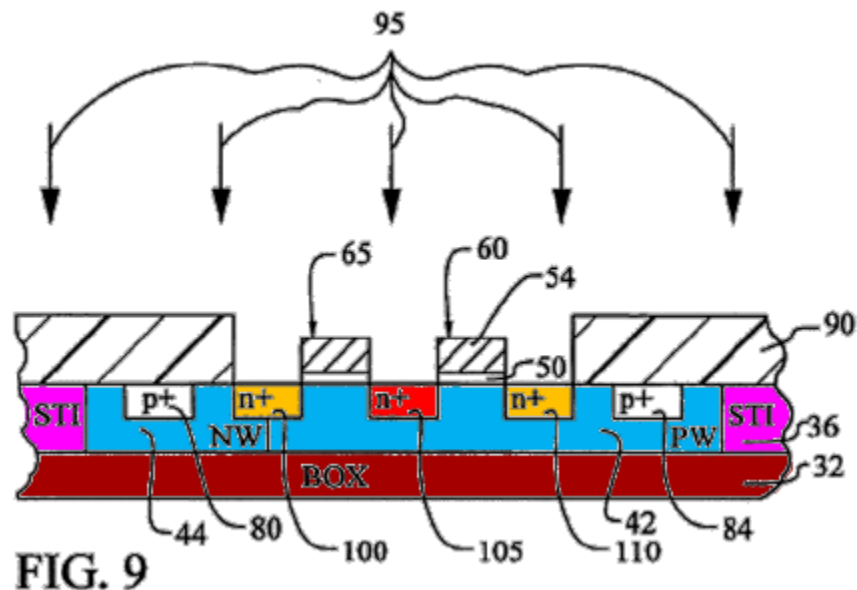
Ex. 1004, Fig. 19. Figure 19 of Okashita is similar to Figure 7 discussed above, with the difference being that in Figure 19, transistor 1 is connected in series with transistor 1', and transistor 2 is connected in series with transistor 2'. *Id.*; *id.* at 8:30–37. Adding the second transistor to each of the existing transistors serves to modify the threshold voltage required to turn on transistors 2 and 2'. *Id.* at 8:38–46 (to $\Delta V_{in}/4 > V_{th}$ instead of $\Delta V_{in}/2 > V_{th}$, as there are now 4 transistors instead of 2). Further, each of the transistors is isolated by the trench insulating layers T1 and T2 “so that the leakage of radio frequency signals . . . can be sufficiently suppressed.” *Id.* at 8:47–54.

Petitioner asserts that it would have been obvious that all of the transistors shown in the Figure 19 embodiment would have been fabricated with the same technique shown earlier in the Figure 7 embodiment. Pet. 29–33. Patent Owner disputes Petitioner’s reasoning, arguing that Petitioner “never explains or states which of the several disclosed transistor fabrication techniques disclosed in Okashita would have been used.” Prelim. Resp. 26; *see also id.* at 25–29. However, as Okashita explains, the embodiment in

Figure 19 is based on the transistors of Figure 7, and the transistors in Figure 7 are the same as the transistors in Figure 9. Ex. 1004, 2:24–25, 8:30–37. Accordingly, Petitioner’s position that it would have been obvious to a person of ordinary skill in the art to use the same techniques as in Figures 7 and 9 for the circuit in Figure 19 is persuasive on this record.

*F. Asserted Anticipation by Yu
(Claims 1–3)*

Petitioner asserts that claims 1–3 are anticipated by Yu. Pet. 49–56. Patent Owner’s arguments focus on the limitation of claim 1 requiring “a source/drain junction that does not contact said buried oxide layer.” Prelim. Resp. 31–35. Petitioner provides the following annotated version of Figure 9 of Yu to illustrate its position:



Pet. 51 (reproducing an annotated version of Ex. 1005, Fig. 9). Figure 9 of Yu discloses two transistors in a semiconductor-on-insulator configuration. The first transistor is formed by gate 60, doped region 110 (colored yellow),

and doped region 105 (colored red). The second transistor is formed by gate 65, doped region 105 (colored red), and doped region 100 (colored yellow). The doped regions 100, 105, and 110 are depicted within silicon wells 42 and 44, but not extending all the way down to buried oxide layer 32 (labeled “BOX,” colored brown). *Id.*; Ex. 1005, 6:46–54. The transistors are depicted as surrounded by shallow trench isolations 36 (labeled “STI,” colored purple), which extend down to buried oxide layer 32. Pet. 51; Ex. 1005, 5:16–19, 4:8–12, 3:63–64.

Petitioner’s position is that doped region 105 is the source for both transistors and the doped regions 100 and 110 are the respective drains for the transistors. Pet. 51–52. Petitioner asserts that none of the doped regions extend to buried oxide layer 32, meeting the limitation, “a source/drain junction that does not contact said buried oxide layer.” *Id.* at 52 (citing Ex. 1005, 6:46–54; Ex. 1002 ¶ 202). Patent Owner argues that doped region 100 is partially in n-well 44 and p-well 42, meaning that doped region 100 (one of Petitioner’s asserted drains) is in *electrical* contact with buried oxide layer 32 via n-well 44. Prelim. Resp. 31–35.

Patent Owner’s argument is unpersuasive because claim 1 requires the source/drain junction not to contact the buried oxide layer. The ’886 patent indicates that the contact precluded is *physical* contact, which provides the beneficial features. For example, the ’886 patent states that prior art sources and drains “typically extend all the way through device layer [] and contact the top surface of [the] buried oxide layer,” which leads to “no, or almost no, capacitive load.” Ex. 1001, 3:15–21. The configuration taught in the ’886 patent, in contrast, “do[es] not extend all the way through device layer 202 to contact the top surface of the buried oxide layer 204,” providing “an

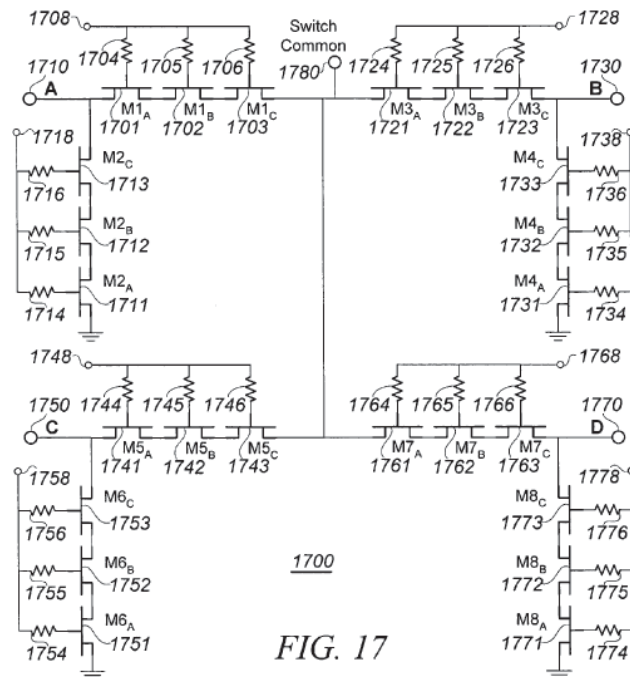
associated junction capacitance.” *Id.* at 4:8–18. Accordingly, the “source/drain junction capacitance” that is “thereby formed” in claim 1 appears to be due to the fact that the “source/drain junction [] does not contact said buried oxide layer.” *Id.* at 9:1–4.

We recognize Patent Owner’s position may be that the alleged electrical connection in Yu prevents the capacitance from being formed, notwithstanding the physical disconnection. However, this is merely attorney argument at this time, as Patent Owner does not have sufficient evidence of record to support its position and persuasively rebut Petitioner’s evidence of record (e.g., Ex. 1002 ¶ 202; Ex. 1005, 6:46–54). Accordingly, Patent Owner’s argument is unpersuasive on this record.

*G. Asserted Obviousness Over Burgener and Okashita
(Claims 1–19)*

Petitioner asserts that claims 1–19 would have been obvious in view of Burgener and Okashita. Pet. 57–83. Patent Owner’s arguments focus on whether there was a reason to combine the references. Prelim. Resp. 35–39. At a high level, Petitioner’s ground takes Burgener’s integrated circuit and proposes to manufacture it using the techniques described in Okashita. *See* Pet. 60 (“Instead of using a conventional [silicon-on-insulator] structure [as taught in Burgener], a [person of ordinary skill in the art] would have been motivated to add an intervening silicon layer between the source/drain junction and the buried oxide layer, as Okashita discloses.”). We will briefly discuss the references and their combination before providing our analysis of the issue raised by Patent Owner.

Figure 17 of Burgener is reproduced below:



Ex. 1006, Fig. 17. Figure 17 is a schematic diagram of antenna switch 1700. *Id.* ¶ 101. The antenna switch is shown as having four components labeled A, B, C, D, each connected to switch common 1780. As explained in Burgener, RF port A (1710) has “+” control node 1708 and “-” control node 1718, which turn on and off transistor stacks 1701–1703 and 1711–1713. *Id.* ¶¶ 101–104. Each of the ports is connected to either a receive or a transmit element of a dual-band transceiver. *Id.* ¶¶ 89, 91; *see also id.* at Fig. 12 (showing antenna switch 1700 in context). Burgener explains that “fabrication details are not provided” but that “preferred embodiments . . . may be fabricated in accordance with ultrathin silicon on sapphire processing” or that “other semiconductor-on-insulator . . . techniques may be used.” *Id.* ¶ 105.

Petitioner asserts that it would have been obvious to a person of ordinary skill in the art to fabricate Burgener’s antenna switch using the principles taught in Okashita—namely, the isolating trenches and an

intervening silicon layer between the source/drain junctions and the buried silicon oxide layer. Pet. 60. Petitioner asserts that a person of ordinary skill in the art would have had a reason to take advantage of Okashita's design: (1) to "reduce the operating temperature of the transistors," which will "enhance their performance and reliability," (2) to "prevent leakage of radio frequency signals," and (3) to "minimize the effect of mismatch." *Id.* at 60–63.

Patent Owner's first argument is that a person of ordinary skill in the art would not look to Okashita because Okashita "is entirely focused on keeping AC and DC grounds separate," something Patent Owner argues "is not present in Burgener." Prelim. Resp. 37. It is not clear to us on this record that Patent Owner is correct that keeping AC and DC grounds separate is not present in Burgener, given that Burgener has both AC signals coming in from ports A–D, as well as digital control signals coming in from the control ports (e.g., 1708 and 1718, for port A). *See* Ex. 1006 ¶¶ 100–101 (discussing RF ports and control signals). In any event, even if the particular problem solved by Okashita is not one of the problems articulated in Burgener, that does not mean that the teachings of Okashita cannot be applied to Burgener. *KSR*, 550 U.S. at 420 ("any need or problem known in the field . . . and addressed by the patent can provide a reason for combining the elements in the manner claimed"). Petitioner has asserted three reasons, mentioned above, why a person of ordinary skill in the art would look to improve Burgener with Okashita's teachings, and Patent Owner does not appear to contest them at this time.

Patent Owner's second argument is that Burgener teaches away from using the technology of Okashita. Prelim. Resp. 37–39. In particular, Patent

Owner points to the language we cited above where “some preferred embodiments” in Burgener use “ultrathin silicon on sapphire processing.” Ex. 1006 ¶ 105. However, Burgener also proposes “[o]ther . . . techniques” (*id.*), and even if the ultrathin technique is preferred, it is well settled that an expression of preferences does not teach away from alternatives. *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009) (“A reference does not teach away, however, if it merely expresses a general preference for an alternative invention but does not ‘criticize, discredit, or otherwise discourage’ investigation into the invention claimed.”) (quoting *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004) (“mere disclosure of alternative designs does not teach away”)).

In sum, Patent Owner’s arguments against the combinability of Burgener and Okashita are not persuasive on this record.

H. Remaining Grounds and Claims

The remaining grounds and claims do not present any materially different issues beyond those we have addressed above.

IV. CONCLUSION

For the reasons given above, we determine that Petitioner has established a reasonable likelihood of success in showing that claim 1 of the ’886 patent would have been anticipated by Okashita. Accordingly, we institute *inter partes* review of all claims and grounds raised in the Petition. 37 C.F.R. § 42.108(a).

V. ORDER

In consideration of the foregoing, it is hereby
ORDERED that the Petition requesting *inter partes* review of claims
1–19 of the '886 patent is *granted*; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(a), the *inter
partes* review of the '886 patent commences on the entry date of this
Decision, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is
hereby given of the institution of a trial.

IPR2024-01402
Patent 7,745,886 B1

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