

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. AND
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioners,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Patent No. 7,745,886

Filing Date: September 29, 2008

Issue Date: June 29, 2010

Inventors: Robert L. Zwingman and Marco Racanelli

Title: SEMICONDUCTOR ON INSULATOR (SOI)
SWITCHING CIRCUIT

PATENT OWNER'S RESPONSE

Case No. IPR2024-01402

TABLE OF CONTENTS

	Page(s)
I. INTRODUCTION	1
II. THE '886 PATENT	2
III. THE ALLEGED PRIOR ART	5
A. Okashita	5
B. Yu	7
C. Burgener	8
IV. LEVEL OF ORDINARY SKILL IN THE ART	11
V. CLAIM CONSTRUCTION	11
VI. PETITIONER'S CITED ART DOES NOT ANTICIPATE OR RENDER OBVIOUS CLAIMS 3 AND 8-19	12
A. GROUND 1	15
B. GROUND 2: Claim 3 Is Not Obvious Over <i>Okashita</i>	15
1. <i>Okashita</i> Does Not Render Claim 3 Obvious Because There Is No Motivation to Modify <i>Okashita</i> to Change the Isolation	15
C. GROUND 3: The Challenged Claims Are Not Obvious Over <i>Okashita</i> and <i>Yu</i>	18
1. The Person of Ordinary Skill in the Art Would Not Have Been Motivated to Combine <i>Yu</i> and <i>Okashita</i> with a Reasonable Expectation of Success	18
D. GROUND 4: The Challenged Claims Are Not Anticipated by <i>Yu</i>	23

1.	The Petition Does Not Show that <i>Yu</i> Discloses “each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer”	23
E.	GROUND 5: The Challenged Claims Are Not Obvious Over <i>Burgener</i> and <i>Okashita</i>	27
1.	A POSITA Would Not Be Motivated to Build <i>Burgener’s</i> Antenna Switch Using the Technology of <i>Okashita</i>	27
2.	The Combination of <i>Burgener</i> and <i>Okashita</i> Does Not Teach the Required Electrical Isolation of Claim 3.....	34
F.	GROUND 6: The Challenged Claims Are Not Obvious Over <i>Burgener</i> , <i>Okashita</i> , and <i>Yu</i>	35
VII.	CONCLUSION.....	35

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>Apple, Inc. v. Contentguard Holdings, Inc.</i> , IPR2015-00355, Paper 9 at 9-10 (P.T.A.B. June 26, 2015)	13
<i>Broadcom Corp. v. Emulex Corp.</i> , 732 F.3d 1325 (Fed. Cir. 2013)	14
<i>Connell v. Sears, Roebuck & Co.</i> , 722 F.2d 1542 (Fed. Cir. 1983)	12
<i>Graham v. John Deere Co. of Kansas City</i> , 383 U.S. 1 (1966).....	12
<i>Innogenetics, N.V. v. Abbott Lab 'ys.</i> , 512 F.3d 1363 (Fed. Cir. 2008)	14
<i>Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.</i> , 821 F.3d 1359 (Fed. Cir. 2016)	14
<i>K-Tec, Inc. v. Vita-Mix Corp.</i> , 696 F.3d 1364 (Fed. Cir. 2012)	22
<i>Kennametal, Inc. v. Ingersoll Cutting Tool Co.</i> , 780 F.3d 1376 (Fed. Cir. 2015)	12
<i>KSR Int'l Co. v. Teleflex Inc.</i> , 550 U.S. 398 (2007).....	12, 17
<i>LBT IP I LLC v. Apple Inc.</i> , No. 2022-1613, 2023 WL 3914920 (Fed. Cir. June 9, 2023).....	15
<i>Los Angeles Biomedical Rsch. Inst. at Harbor-UCLA Med. Ctr. v.</i> <i>Eli Lilly & Co.</i> , 849 F.3d 1049 (Fed. Cir. 2017)	14

<i>Net MoneyIN, Inc. v. VeriSign, Inc.</i> , 545 F.3d 1359 (Fed. Cir. 2008)	12
<i>Pers. Web Techs., LLC v. Apple, Inc.</i> , 848 F.3d 987 (Fed. Cir. 2017)	13
<i>Pers. Web Techs., LLC v. Apple, Inc.</i> , 917 F.3d 1376 (Fed. Cir. 2019)	14
<i>In re Petering</i> , 301 F.2d 676 (C.C.P.A. 1962)	12
<i>Stratoflex, Inc. v. Aeroquip Corp.</i> , 713 F.2d 1530 (Fed. Cir. 1983)	13
<i>In re Van Os</i> , 844 F.3d 1359 (Fed. Cir. 2017)	14
<i>Virtek Vision Int’l ULC v. Assembly Guidance Sys., Inc.</i> , 97 F.4th 882 (Fed. Cir. 2024)	17

LIST OF EXHIBITS

Exhibit No.	Description of Document
2001	Docket Control Order, Dkt. 38, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Aug. 5, 2024)
2002	Order Denying Samsung's Motion to Stay Pending <i>Inter Partes</i> Review, Dkt. 62, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Dec. 19, 2024)
2003	Defendants' Invalidity Contentions, served on September 26, 2024, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex.)
2004	U.S. Patent No. 6,804,502 entitled SWITCH CIRCUIT AND METHOD OF SWITCHING RADIO FREQUENCY SIGNALS to Burgener et al., issued October 12, 2004
2005	Deposition of Scott E. Thompson, Ph.D., taken on June 17, 2025
2006	Declaration of Mr. John Berg
2007	Email from Board authorizing Patent Owner to file a Motion to Amend

I. INTRODUCTION

On September 24, 2024, Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, “Petitioner”) submitted a Petition (Paper 1, “Petition” or “Pet.”) to institute *inter partes* review (“IPR”) of U.S. Patent No. 7,745,886 (Ex. 1001, the “’886 Patent”), challenging Claims 1-19 (the “Challenged Claims”). The Petition asserts that: (i) Claims 1, 2, 4, and 5 are anticipated by U.S. Patent No. 6,836,172 to Okashita (“Okashita” or Ex. 1004); (ii) Claims 1-7 are rendered obvious over Okashita; (iii) Claims 1-7 are rendered obvious over Okashita and U.S. Patent No. 6,737,682 to Yu (“Yu” Ex. 1005); (iv) Claims 1-3 are anticipated by Yu; (v) Claims 1-19 are rendered obvious over U.S. Patent Application Publication No. US 2006/0270367 to Burgener et al. (Ex. 1006) and Okashita; and (vi) Claims 1-19 are obvious over Burgener, Okashita, and Yu.

Patent Owner is concurrently filing a motion to amend which requests cancellation of claims 1-2 and 4-7 of the ’886 Patent.

With respect to the remaining Challenged Claims, the Board should reject Petitioner’s arguments that the prior art renders Claims 3 and 8-19 anticipated or obvious.

With respect to Ground 2, Okashita does not render Claim 3 obvious because this claim requires the plurality of cascaded transistors to be located within an

isolated island. Petitioner admits that Okashita discloses each transistor located in its own island, and the Petition relies on impermissible hindsight to provide the alleged motivation to modify this reference, in express contradiction with the teachings of Okashita which require these transistors to be isolated from one another.

With respect to Ground 3, the Petition does not provide a motivation for the POSITA to combine Okashita and Yu with a reasonable expectation of success, because Okashita and Yu are from completely different fields of endeavor.

With respect to Ground 4, Yu does not anticipate any claim because one of the cascaded transistors in Yu has a source/drain junction that does not have any source/drain junction capacitance as required by the claims.

With respect to Grounds 5 and 6, there is no motivation to combine Burgener and Okashita and/or Yu, because Burgener teaches that the circuitry cited by the Petition should be built with an Ultrathin Silicon on Sapphire technology, rather than the relatively thick SOI technology taught by Okashita or Yu.

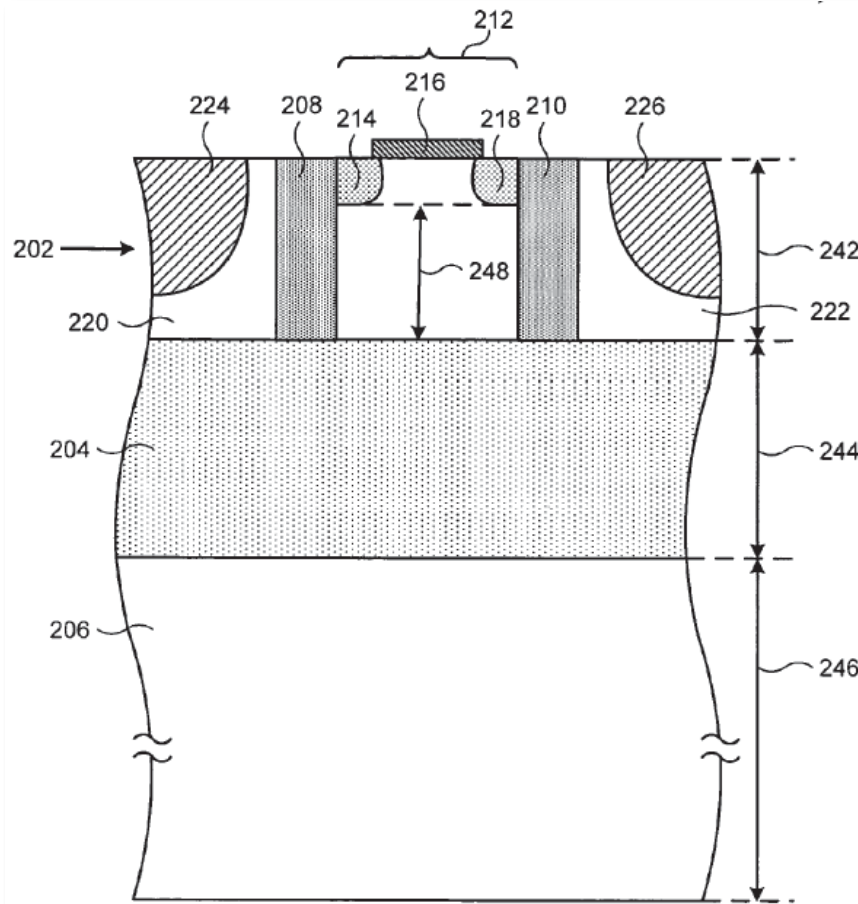
II. THE '886 PATENT

U.S. Patent No. 7,745,886 (Ex. 1001, the "'886 Patent") is titled "Semiconductor on Insulator (SOI) Switching Circuit" and issued on June 29, 2010. The '886 Patent names two inventors, Robert L. Zwingman and Marco Racanelli, and was filed by and issued to Newport Fab, LLC, a subsidiary of Tower

Semiconductor, Inc. which manufactures semiconductor wafers in Newport Beach, California.

The '886 Patent describes and claims an improvement in switching circuitry that includes a number of transistors built using silicon on insulator, or SOI, technology. '886 Patent, Abstract. According to the '886 Patent, “it is difficult to electrically isolate semiconductor structures fabricated on a conventional bulk silicon wafer” because electric current can flow under trenches. *Id.*, 1:29-36. This can be partially solved using silicon-on-insulator technology, but “circuits designed for fabrication in a bulk silicon wafer must be redesigned for fabrication in a conventional silicon on insulator wafer, which significantly increases manufacturing and integration complexity and cost.” *Id.*, 1:43-47.

An embodiment of the invention of the '886 Patent is shown in Figure 2, below:



'886 Patent, Fig. 2. According to the '886 Patent, Figure 2 shows a SOI cross section, where a device layer 202 sits atop a buried oxide layer 204 that acts as an insulator, which sits atop a conventional bulk semiconductor layer 206. *Id.* 3:49-67. Each of these three layers is made much thicker than in typical silicon devices. *Id.*, 3:49-4:3. A transistor 212 is built in the device layer, and “[b]ecause of the increased thickness of device layer 202, source 214 and drain 218 do not extend all the way through device layer 202 to contact the top surface of buried oxide layer 204.” *Id.* 4:8-11.

The source/drain junctions of the transistor have capacitances, and these capacitances “behave similarly to the junction capacitances of a transistor implemented in a conventional bulk silicon wafer, instead of a conventional SOI wafer, in part because of the greater thickness of device layer 202 compared to the thickness of conventional device layer 102.” *Id.* 4:19-24.

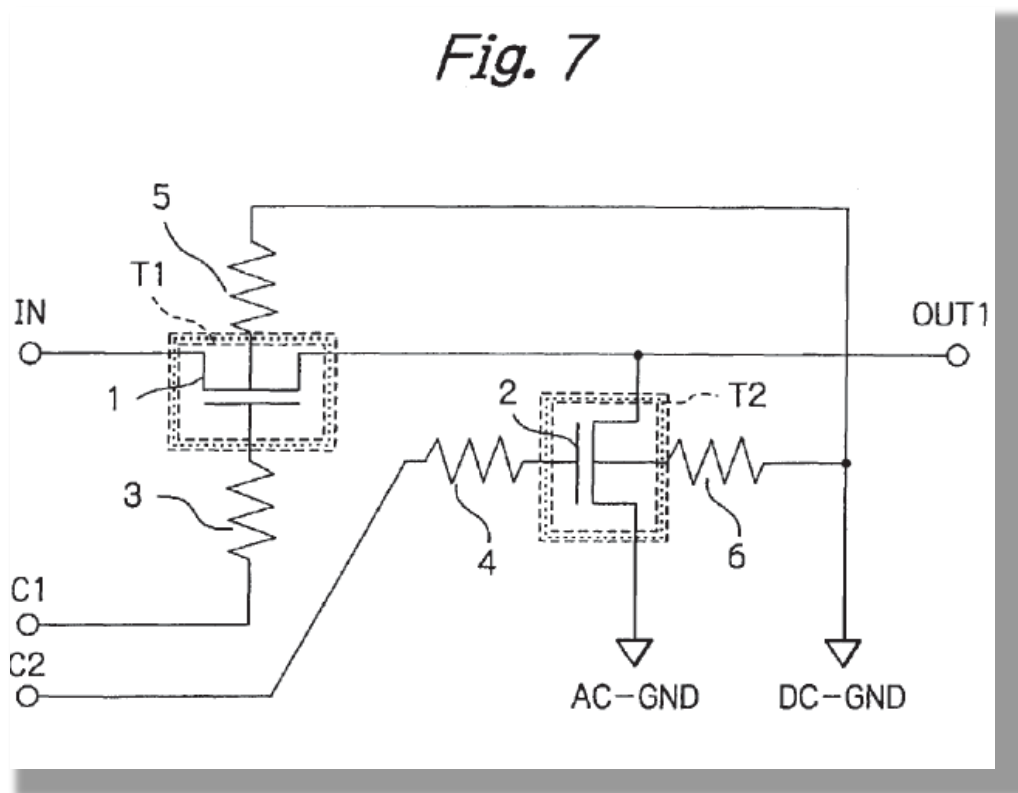
The ’886 Patent provides several advantages, including that the thick layers aid in implementing high performance circuits, and that “[a]n engineer using design methodologies suitable for conventional bulk semiconductor devices and circuits, without using specialized design techniques or device models required for conventional SOI technology, can readily design and implement high performance circuits utilizing various embodiments of the invention’s SOI transistors and other SOI structures.” *Id.*, 8:22-31.

III. THE ALLEGED PRIOR ART

A. Okashita

U.S. Patent No. 6,836,172 to Okashita issued on December 28, 2004 and is titled “Semiconductor Switch Apparatus Including Isolated MOS Transistors.” *Okashita* describes a semiconductor switch apparatus that includes “at least one shunt MOS transistor connected between one of the input terminal and the output terminal and the AC ground terminal.” Ex. 1004, Abstract. *Okashita* describes that

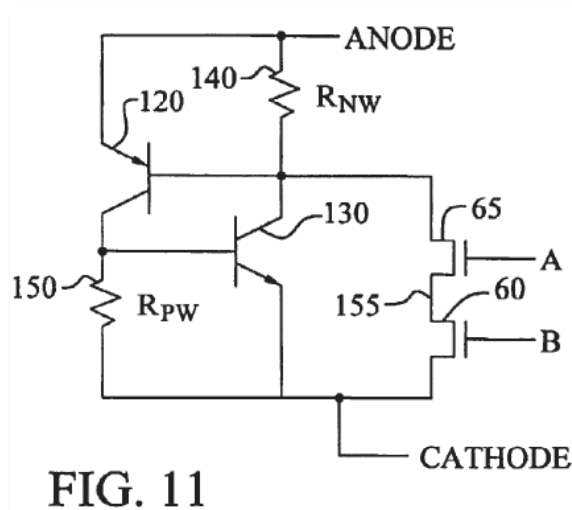
prior art semiconductor switches using Gallium-Arsenide have a high resistance, and thus the leakage of radio signals via the substrate can be suppressed, but GaAs substrates are very expensive. *Id.*, 1:16-28. *Okashita* describes a system including a series MOS transistor T1 and a shunt MOS transistor 2, shown below in Figure 7:



Ex. 1004, Fig. 7. According to *Okashita*, “a resistor 5 is connected between the back gate of the MOS transistor 1 and the DC ground terminal DC-GND of FIG. 3, and a resistor 6 is connected between the back gate of the MOS transistor 2 and the DC ground terminal DC-GND of FIG. 3.” *Id.*, 5:21-27.

B. Yu

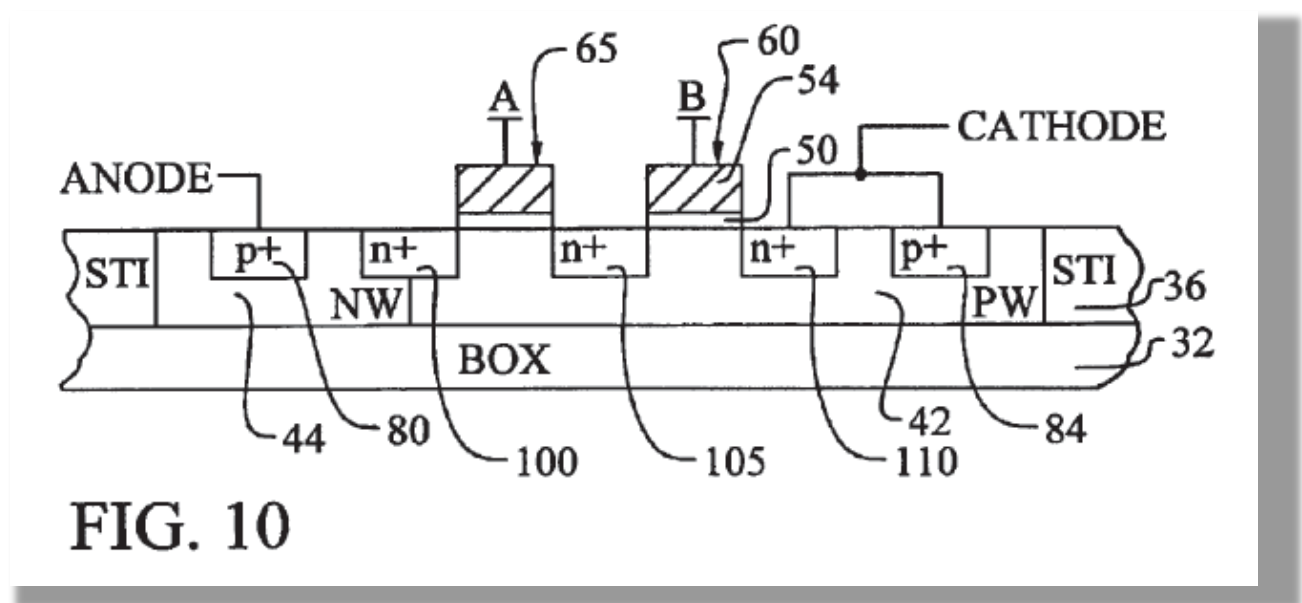
U.S. Patent No. 6,737,682 to Ta-Lee Yu issued on May 18, 2004 and is titled “High Voltage Tolerant and Low Voltage Triggering Floating-Well Silicon Controlled Rectifier On Silicon-On-Insulator For Input Or Output.” *Yu* discloses a particular type of thyristor, called a low voltage triggering, silicon-controlled rectifier. Ex. 1005, 1:10-14. As recognized by *Yu*, these circuits are typically used for ESD (electrostatic discharge) protection. *Id.* 1:24-27. Figure 11 of *Yu* discloses the circuitry of the silicon-controlled rectifier in *Yu*, which includes a single cathode and anode, as well as two MOS transistors with control inputs A and B:



Ex. 1005, FIG. 11. *Yu* describes that, during an ESD event, the devices 60 and 65 “operate due to the bipolar effect taking place between the source of the bottom

NMOS device 60 and the drain of the top NMOS device 65,” and that the silicon-controlled rectifier is “triggered by the current generated when the stacked NMOS devices 60 and 65 enter avalanche breakdown.” *Id.* 6:40-45.

Yu also discloses a cross section of this circuit, shown in Figure 10:



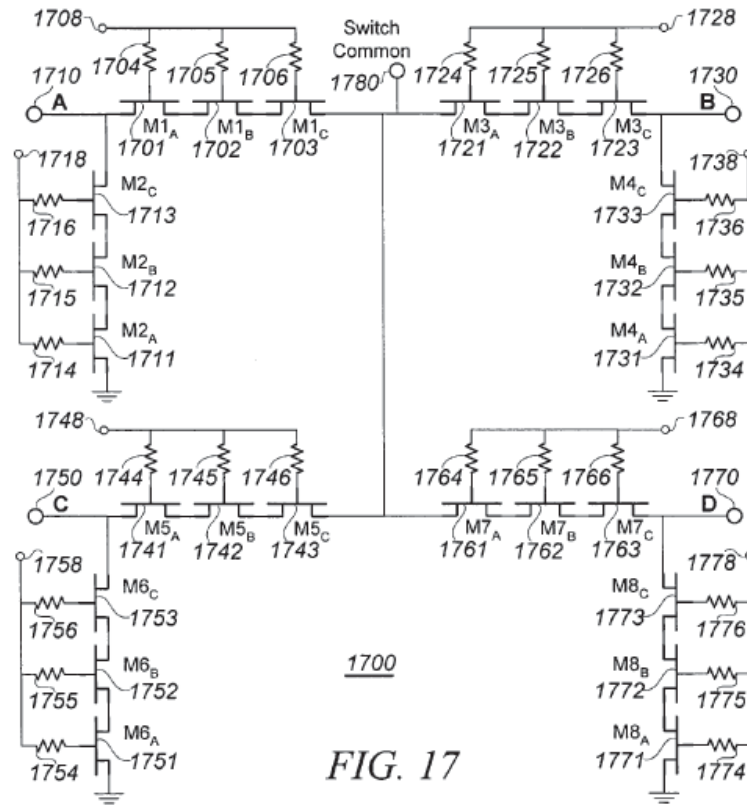
Ex. 1005, FIG. 10. Disclosed is a N-well 44 in which the anode is formed, and a P-well 42 in which the cathode is formed. *Id.*, 5:28-42. The N+ well 100 that forms the source of transistor 65 is located partly in the N-well 44 and partly in the P-well 42. *Id.*, 5:36-37.

C. Burgener

U.S. Patent Application Publication No. US 2006/0270367 was published on November 30, 2006 to Burgener, et al. and is titled “Integrated RF Front End With

Stacked Transistor Switch.” *Burgener* discloses an “integrated circuit (IC)” that includes “all RF front end or transceiver elements for a portable communication device,” such as a cellular telephone and other wireless communications device. Ex. 1006, Abstract, ¶ [0006]. The RF front end may be implemented by stacks of multiple Field Effect Transistors (FETs) connected in series to operate as a switching device. *Id.*, Abstract, ¶ [0009].

Burgener discloses an “antenna switch 1700” that directs input signals from an antenna to amplifiers, and output signals from the power amplifiers to the antenna, shown in Figure 17:



Ex. 1006, FIG. 17. *Burgener* states “FIG. 17 is a simplified schematic of exemplary circuitry 1700 for an antenna switch. Further details regarding design and fabrication of such an RF switch may be found in U.S. Pat. No. 6,804,502, issued Oct. 12, 2004 and entitled ‘Switch Circuit and Method of Switching Radio Frequency Signals.’” Ex. 1006, ¶ [0101]. U.S. Patent No. 6,804,502 (Ex. 2004, “*Burgener II*”) states that the transistors in the RF switch can be made using ultra-thin silicon-on-sapphire

technology, which eliminates the need for “[t]raditional transistor isolation wells” that are used for thick silicon. Ex. 2004, 10:66-11:1.

IV. LEVEL OF ORDINARY SKILL IN THE ART

As Mr. Berg explains, a POSITA would have (1) a Bachelor of Science degree or equivalent degree in electrical engineering, physics, materials science, or a similar field; and (2) at least two years of industry experience in semiconductor design and/or fabrication. Additional formal education (such as Master of Science degrees) would compensate for less technical experience and vice versa. Ex. 2006, ¶¶ 21-26.

Petitioner’s proposed level of skill in the art – “at least a master’s degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems”—imposes a requirement of a master’s degree. Pet., 6. As Mr. Berg explains, engineers working in this field, and implementing designs such as that described in the ’886 Patent, typically have bachelor’s degrees. Ex. 2006, ¶ 24. Such engineers are the target audience for the ’886 Patent, and thus, a POSITA need not have a master’s degree. *Id.*

V. CLAIM CONSTRUCTION

Petitioner asserts that no claim terms need construction “to resolve the controversy in this forum.” Pet. at 5. It is not necessary for the Board to construe this

claim term or reach this issue in order to deny the Petition and confirm the patentability of Claims 3 and 8-19.

VI. PETITIONER’S CITED ART DOES NOT ANTICIPATE OR RENDER OBVIOUS CLAIMS 3 AND 8-19

In order to anticipate the claimed invention, a prior art reference must “disclose all elements of the claim within the four corners of the document,” and it must “disclose those elements ‘arranged as in the claim.’” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). “However, a reference can anticipate a claim even if it ‘d[oes] not expressly spell out’ all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would ‘at once envisage’ the claimed arrangement or combination.” *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015) (quoting *In re Petering*, 301 F.2d 676, 681 (C.C.P.A. 1962)).

The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) so-called secondary considerations where in evidence. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966); *KSR Int’l Co. v. Teleflex*

Inc., 550 U.S. 398, 406 (2007). The question is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1537 (Fed. Cir. 1983).

The Board has held that a failure to identify the differences between the claimed subject matter and the prior art is fatal to an obviousness challenge. *See Apple, Inc. v. Contentguard Holdings, Inc.*, IPR2015-00355, Decision Denying Institution of *Inter Partes* Review, Paper 9 at 9-10 (P.T.A.B. June 26, 2015) (denying institution for failure to identify the differences between the claimed subject matter and the prior art).

In arriving at an obviousness determination, the Board must sufficiently explain and support the conclusions that the prior art references disclose all the elements recited in the Challenged Claims and a relevant, skilled artisan not only could have made, but would have been motivated to combine all the prior art references in the way the patent claims and reasonably expected success. *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017). That is, even if all the claim elements are found across a number of references, an obviousness determination must consider whether a person of ordinary skill in the art would have

the motivation to combine those references. *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1368 (Fed. Cir. 2016); *Los Angeles Biomedical Rsch. Inst. at Harbor-UCLA Med. Ctr. v. Eli Lilly & Co.*, 849 F.3d 1049, 1067 (Fed. Cir. 2017) (vacating and remanding an obviousness determination, in part, because the Board did not make factual finding as to whether there was an apparent reason to combine all three prior art references to achieve the claimed invention and whether a person of skill in the art would have had a reasonable expectation of success from such a combination). This combinability determination, as supported by an articulated motivation to combine, requires a plausible rationale as to why those prior art references would have worked together. *Broadcom Corp. v. Emulex Corp.*, 732 F.3d 1325, 1335 (Fed. Cir. 2013). Absent some articulated rationale, a “common sense” finding is no different than the conclusory statement “would have been obvious.” *In re Van Os*, 844 F.3d 1359, 1361 (Fed. Cir. 2017). Of additional importance, “knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references” *Innogenetics, N.V. v. Abbott Lab’ys.*, 512 F.3d 1363, 1373 (Fed. Cir. 2008).

To demonstrate inherent obviousness, an inherent limitation must necessarily be present in the combination of references. *See Pers. Web Techs., LLC v. Apple*,

Inc., 917 F.3d 1376 (Fed. Cir. 2019); *LBT IP I LLC v. Apple Inc.*, No. 2022-1613, 2023 WL 3914920, at *3 (Fed. Cir. June 9, 2023). It is not enough to merely show that it is likely to be present. *Id.*

A. GROUND 1

Ground 1 only relates to claims for which Patent Owner requests cancellation and, therefore, will not be discussed here.

B. GROUND 2: Claim 3 Is Not Obvious Over *Okashita*

1. *Okashita* Does Not Render Claim 3 Obvious Because There Is No Motivation to Modify *Okashita* to Change the Isolation

Claim 3 of the '886 Patent requires the entire plurality of cascaded transistors to be located within an isolated island, whereas Claim 2 requires each transistor to be in its own isolated island:

1. A switching circuit comprising:
a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;
each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;
at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device

layer.

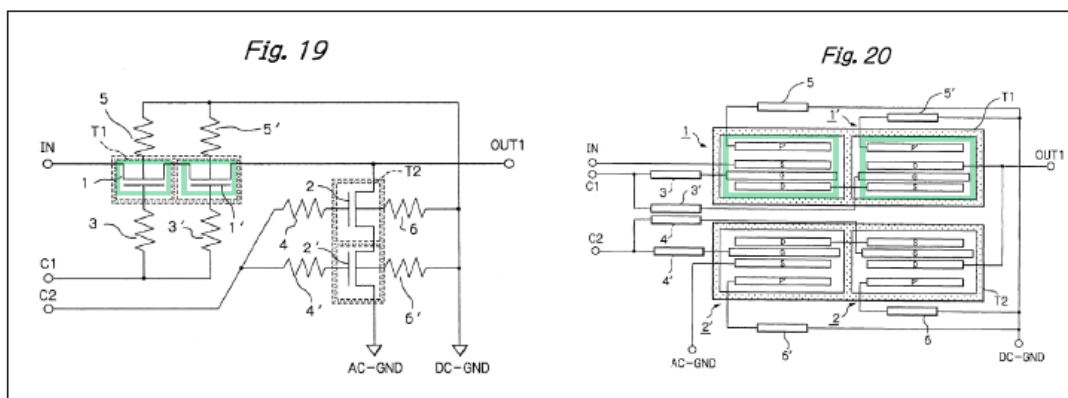
2. The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer.

3. *The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer.*

'886 Patent, Claims 1-3 (emphasis added).

The Petition claims that *Okashita* anticipates Claim 2 because it shows each transistor in its own isolated island, but renders obvious Claim 3 with a modification to the structure of the isolated island. Pet. at 35-36 (citing Ex. 1002, ¶¶ 140-141; 167-168).

Okashita's relevant disclosure is shown below in Figures 19 and 20, which shows each of what Petitioner claims is the cascaded transistors located in its own isolated island:



Ex. 1002, ¶ 150 (annotating *Okashita* Figs. 19 and 20)

Petitioner admits that *Okashita* does not disclose Claim 3, but states that “a POSITA would have recognized that situating both MOS transistors 1, 1’ within the same isolated island, as *Okashita* teaches, ensures consistent performance characteristics among the transistors.” Pet., 36 (citing Ex. 1002, ¶ 168). According to Petitioner, this would provide two benefits: better tracking of thermal temperature and consistent switching rate. *Id.*

Petitioner’s motivation to modify *Okashita* is based entirely on impermissible hindsight. *Virtek Vision Int’l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 886-87 (Fed. Cir. 2024) (holding that a Petition did not provide a motivation to select one of two existing prior art elements). The Petition focuses on what would be possible for the POSITA to accomplish, without providing a motivation for the POSITA to do so. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007). According to Mr. Berg, there is no motivation to modify the isolated islands that isolate each transistor 1, 1’ to place the transistors both in the same isolated island. Ex. 2006, ¶ 45. *Okashita* specifically teaches that “each of the MOS transistors 1, 1’, 2 and 2’ is isolated by the trench insulating layers T1 and T2, so that the leakage of radio frequency signals from the silicon layer 23 of the MOS transistor 1 to that

of the MOS transistor 1'. . . can be sufficiently suppressed." Ex. 1004, 8:47-54. (emphasis added).

Since *Okashita* teaches the need to suppress leakage of radio signals between MOS transistor 1 and MOS transistor 1', the POSITA would not have been motivated to remove the isolation trenches between these two transistors, merely to ensure more consistent performance. Ex. 2006, ¶ 46. Therefore, the Petition has not articulated a motivation to modify *Okashita* to reach the invention of Claim 3.

C. GROUND 3: The Challenged Claims Are Not Obvious Over *Okashita* and *Yu*

1. The Person of Ordinary Skill in the Art Would Not Have Been Motivated to Combine *Yu* and *Okashita* with a Reasonable Expectation of Success

The Petition states that it would have been obvious to fabricate *Okashita's* transistors using an SOI process, as taught by *Yu*. Pet. at 42-44. But the Petition does not account for the multiple, meaningful differences between the circuitry in *Okashita* and *Yu*, and therefore fails to provide a sufficient motivation to combine with a reasonable expectation of success. Ex. 2006, ¶¶ 47-54.

Yu describes a silicon-controlled rectifier that is used to switch very high voltages. *Yu*, Abstract. The field of endeavor in *Yu* is specifically limited to "a method to form a low voltage triggering, silicon-controlled rectifier (SCR) SOI

device having improved ESD performance.” *Id.* 1:10-13. ESD refers to electrostatic discharge. *Id.*, ¶ 47.

Okashita, on the other hand, relates to “a semiconductor switch apparatus for radio frequency signals.” Ex. 1004, 1:7-8. *Okashita* discloses a switching circuit that works between, at most, -3V and 3V. *Id.* at 7:18-29. In fact, *Okashita* repeatedly refers to 3 volts as a high voltage. *Id.* at 3:11, 3:40; Ex. 2006, ¶ 48.

Petitioner does not account for these meaningful differences in use cases, merely stating that “a POSITA would have found it obvious to fabricate *Okashita*’s transistors using an SOI process, as *Yu* teaches, so the transistors would have been within the active area that is surrounded by a trench isolation region.” Ex. 1002, ¶ 178. Dr. Thompson goes on to state that silicon dioxide has lower thermal conductivity than silicon, so if the source/drain junctions of *Okashita* were to contact the silicon oxide layer, the transistors would operate at higher temperatures, which could negatively impact circuit performance. *Id.* at ¶ 179. Ex. 2006, ¶ 49.

The problems described by *Okashita* include:

In a mobile communication apparatus such as a mobile telephone apparatus using radio frequency signals such as GHz microwave signals, semiconductor switch apparatuses are used for switching the operation of an antenna circuit and a receiving and transmitting circuit.

A prior art semiconductor switch apparatus using GaAs FETs is very simple and therefore, can be constructed by one semiconductor chip. That is, since the GaAs FETs serve as passive elements such as resistors and capacitors, bias circuits for the GaAs FETs are unnecessary. Also, since a substrate of the GaAs FETs is made of semi-insulating material having a high resistance, the leakage of radio frequency signals via the substrate can be suppressed. This will be explained later in detail.

In the above-described prior art semiconductor switch apparatus using GaAs FETs, however, since GaAs substrates are expensive, the manufacturing cost is very high.

In another prior art semiconductor switch apparatus using silicon MOS transistors, in order to suppress the leakage of radio frequency signals, a silicon-on-insulator (SOI) configuration is adopted (see: JP-A-2000-294786) or a resistor is inserted between the back gate of each of the MOS transistors and a ground terminal (see: U.S. Pat. No. 6,094,088). This also will be explained later in detail.

In the above-described prior art semiconductor switch apparatus using silicon MOS transistors, although the manufacturing cost can be low, suppression of the leakage of radio frequency signals is still insufficient, which also will be explained later in detail.

Ex. 1004, 1:11-40.

Meanwhile, *Yu* is concerned entirely with ESD protection and heat transfer for SOI devices:

The SCR and LVT-SCR devices of the prior present several difficulties in integration with a SOI process. In an

SOI process, the devices must be formed in a relatively thin silicon layer overlying a buried insulator layer. This buried insulator layer, in turn, overlies the bulk substrate. The presence of the buried insulator layer improves MOS transistor performance, especially for very short channel devices, and reduces substrate coupling issues by providing excellent device-to-device isolation. Typically, the STI regions are formed down to the buried insulator layer such that each active area is completely isolated from other active areas.

However, these characteristics cause several problems for SCR devices formed in an SOI process having STI isolation. First, the presence of the STI regions within the SCR and LVT-SCR devices reduces the lateral heat transfer property during an ESD event. Consequently, the devices fail at a lower energy dissipation level. Second, the STI pull-down impacts both low-current and high-current characteristics and influences the diode leakage characteristics. Third, the thickness of the silicon layer overlying the buried insulator can restrict the formation of the SCR device. If the silicon layer is relatively thin, then the heavily doped (n⁺ and p⁺) regions will extend down to the buried insulator layer. In this case, the traditional SCR and LVT-SCR design will not work because the bipolar devices will not function.

Ex. 1005, 1:59-2:17.

These fields of art and pertinent problems not only have nothing to do with one another they also have nothing to do with the problem solved by the '886 Patent and therefore are not analogous art. Ex. 2006, ¶ 52. The '886 Patent relates to intentionally increasing the capacitance of structures built using SOI to mimic the

characteristics of circuits designed to be built using bulk silicon, so that circuits designed for fabrication using bulk silicon do not need to be redesigned for use in SOI. '886 Patent, 1:37-50; 3:21-48. But in order to be analogous, the reference must be from the same field of endeavor or must be reasonable pertinent to the particular problem with which the inventor is involved. *K-Tec, Inc. v. Vita-Mix Corp.*, 696 F.3d 1364, 1375 (Fed. Cir. 2012). Neither *Okashita* nor *Yu* are analogous to the '886 Patent.

According to Mr. Berg, the POSITA would have been motivated to combine *Okashita* and *Yu* with a reasonable expectation of success, for several reasons.

First, the POSITA looking to modify the SOI process in *Okashita* would not have looked to *Yu* for that modification because *Okashita* is a low voltage wireless switching circuit and *Yu* discloses a high voltage silicon-controlled rectifier that is outside of that field of endeavor. Second, *Okashita* already provides teachings for an SOI process for a switching apparatus, and therefore there would be no motivation to look to a completely different process in *Yu* that solves a different problem and is designed to operate at very different voltages. Third, with respect to Claim 3, the POSITA would not have been motivated to look to *Yu*, which does not isolate the individual transistors from one another, as *Okashita* specifically teaches that “each

of the MOS transistors 1, 1', 2 and 2' is isolated by the trench insulating layers T1 and T2, so that the leakage of radio frequency signals from the silicon layer 23 of the MOS transistor 1 *to that of the MOS transistor 1'*. . . can be sufficiently suppressed.” Ex. 1004, 8:47-54. (emphasis added); Ex. 2006, ¶ 53.

D. GROUND 4: The Challenged Claims Are Not Anticipated by *Yu*

1. The Petition Does Not Show that *Yu* Discloses “each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer”

Yu does not anticipate any of Claims 1, 2, or 3 of the '886 Patent, because the Figures and disclosures in *Yu* clearly show that the source/drain junction of one of the transistors electrically contacts the buried oxide layer, as prohibited by the claims.

Claim 1 of the '886 Patent requires that “each” of the cascaded transistors has a source/drain junction that does not contact the buried oxide layer and forms a source/drain junction capacitance:

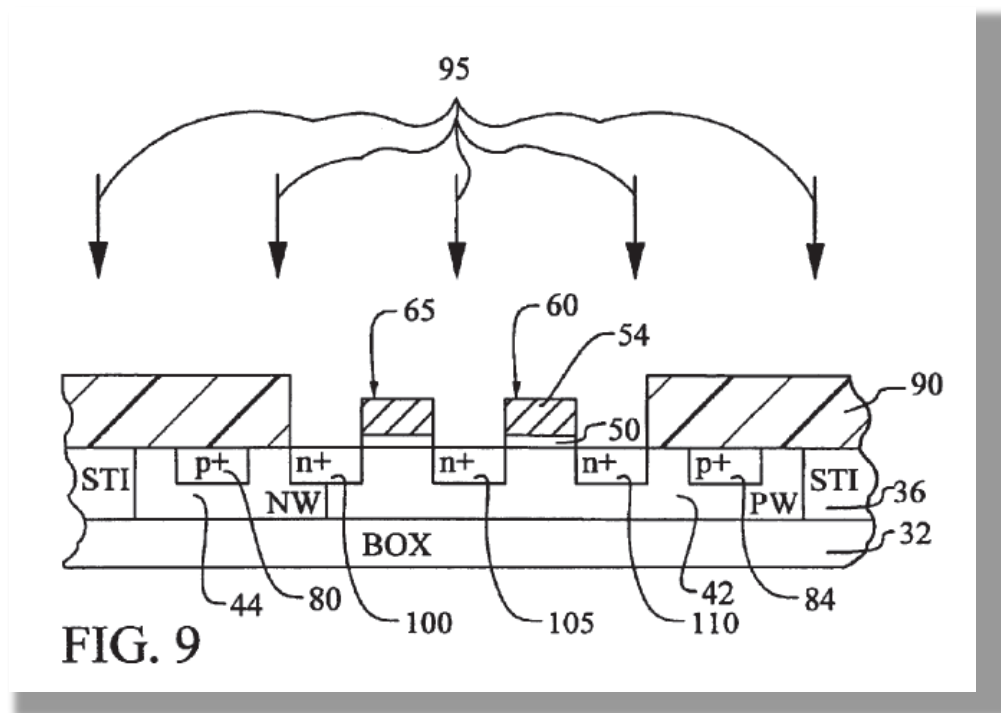
1. A switching circuit comprising:
a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;
each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried

oxide layer, thereby forming a source/drain junction capacitance;
at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.

'886 Patent, Claim 1 (emphasis added).

Yu discloses an N-well 44 and a P-well 42 built in the same layer, as shown in

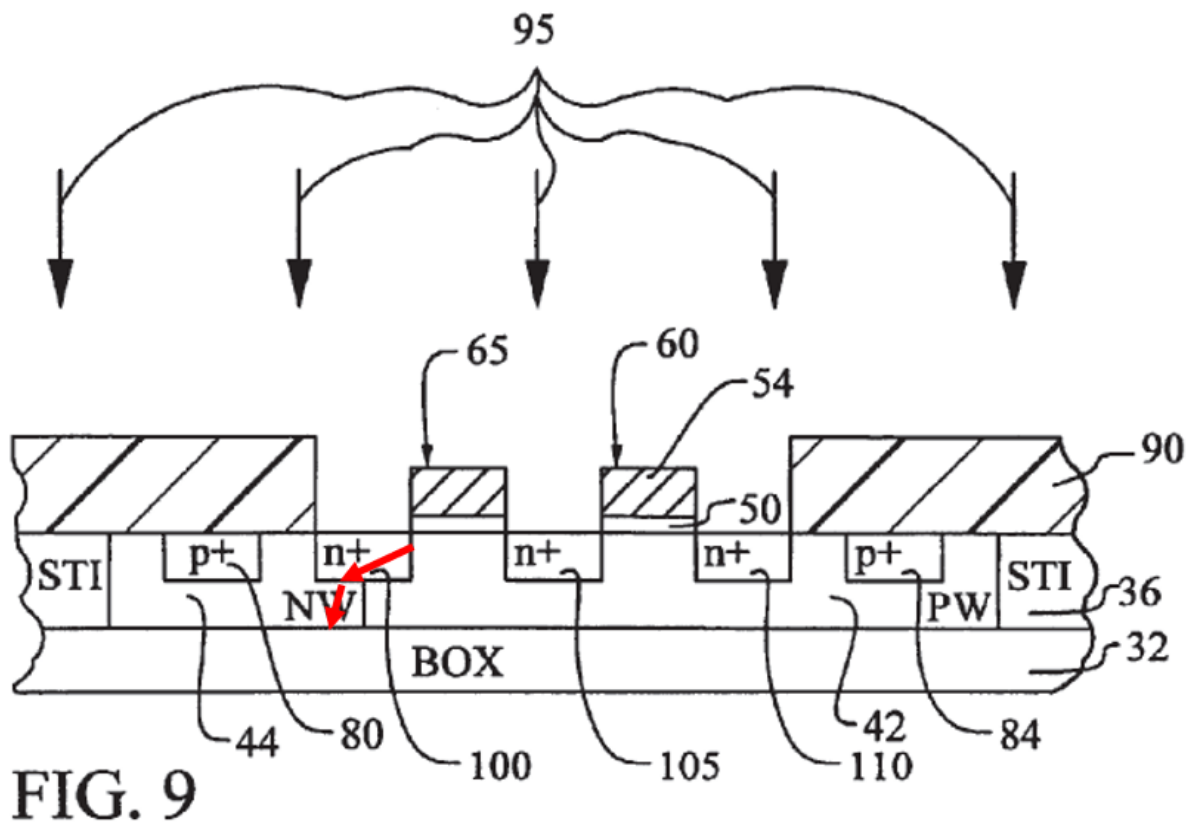
Figure 9:



Ex. 1005, at FIG. 9; *see also* Ex. 1005, 4:16-20 (“a first well 42 of a first type is formed, and a second well 44 of a second type is formed. In the preferred

embodiment, the first well 42 is p-type and is therefore called the p-well. The second well 44 is n-type and is called the n-well.”).

The presence of the N-well 100 is critical to the analysis of *Yu* with respect to the '886 Patent. Because the source region of the first transistor 100 is doped N⁺, and is partially located in the N-Well 44; it is, in fact, electrically in contact with the buried oxide layer as prohibited by Claim 1 of the '886 Patent. This is shown, as annotated in Figure 9 of *Yu*, below:



Ex. 1005, FIG. 9 (annotated); Ex. 2006, ¶ 61.

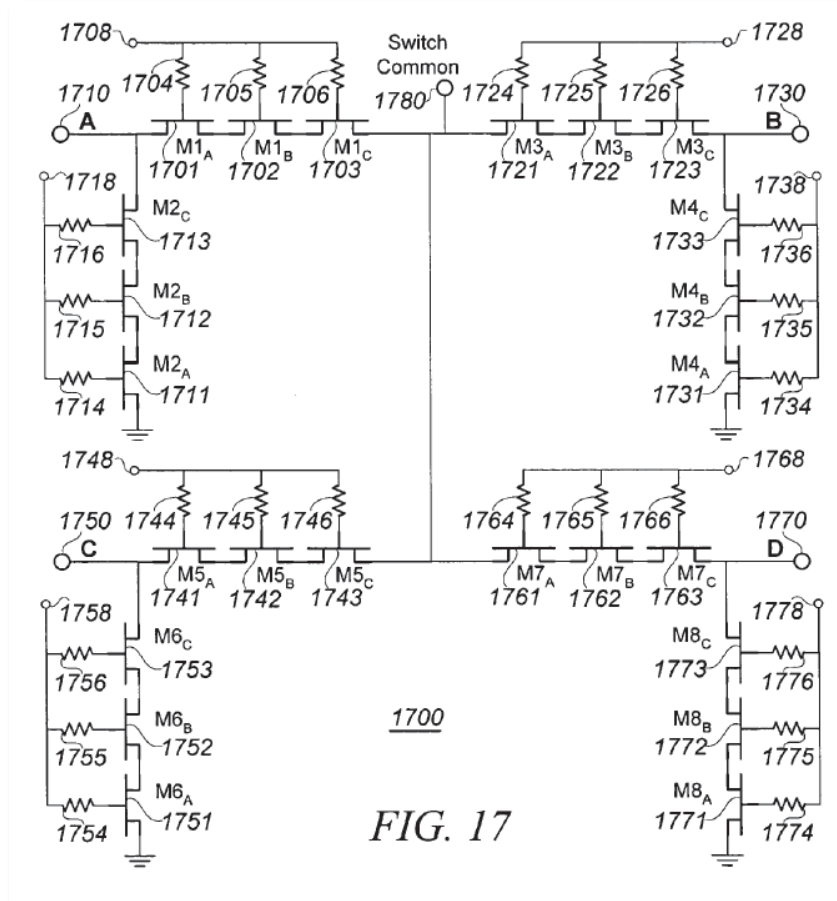
In its explanation of the nearly identical Figure 10, *Yu* states, “[t]he second gate 65 is between the fourth and fifth doped regions 105 and 100. The doped regions are not separated by isolation oxide. Two MOS transistors are formed by the gates 60 and 65. In particular, a first NMOS transistor is formed by first gate 60, third doped region 110, and fourth doped region 105. A second MOS transistor is formed by second gate 65, fourth doped region 105, and fifth doped region 100. The first and second transistors are in series between the third doped region 110 and the fifth doped region 100. Further, the *fifth doped region 100 is coupled to the second well 44*, and the third doped region is coupled to the first doped region to form the cathode.” Ex. 1005, 5:41-53 (emphasis added). As *Yu* explains, the doped n⁺ regions form the source/drain junctions of the transistor, and as expressly stated by *Yu*, “doped region 100 is coupled to the second well 44” and, therefore, doped region 100 (the N⁺ well) *does* electrically contact the buried oxide layer, even if there is no physical contact. Ex. 2006, ¶ 63. Therefore, *Yu* cannot anticipate Claim 1 and Ground 4 fails.

**E. GROUND 5: The Challenged Claims Are Not Obvious Over
Burgener and *Okashita***

**1. A POSITA Would Not Be Motivated to Build
Burgener's Antenna Switch Using the Technology of
*Okashita***

Petitioner claims that “[i]t would have been obvious for a POSITA to fabricate *Burgener*'s integrated circuit (e.g., antenna switch 1700 and the corresponding cascaded FETs)” with *Okashita*'s teachings; however *Burgener* and *Okashita* disclose differing inventions that a POSITA would not be motivated to combine, and this combination does not render the Challenged Claims obvious. Pet. at 60 (citing Ex. 1002, ¶ 213).

The Petition relies on Figure 17 of *Burgener*, and argues that “it would have been obvious for a POSITA to fabricate *Burgener*'s integrated circuit (e.g., antenna switch 1700 and the corresponding cascaded FETs) using *Okashita*'s SOI configuration.” Pet. at 65 (citing Ex. 1002, ¶ 222). Figure 17 of *Burgener* is reproduced below:



Ex. 1006, FIG. 17.

A POSITA would not have been motivated to look to *Okashita* to build the transistors in *Burgener*. Although *Burgener* discloses that its integrated circuit may be fabricated using “semiconductor-on-insulator (SOI) techniques” (Ex. 1006, ¶ [0105]), the POSITA would not have been motivated to use the specific SOI design in *Okashita* to create *Burgener*’s switch. Ex. 2006, ¶ 64.

The Petition states that the POSITA would have been motivated to build *Burgener's* integrated circuit using the teachings of *Okashita* for three reasons. Pet., 60. First, it states that the POSITA would have been motivated to use the intervening silicon layer from *Okashita* because it would reduce the operating temperature of the transistors. *Id.* at 60-61 (citing Ex. 1002, ¶ 214). Second, it states that the POSITA would have been motivated to fabricate *Burgener's* circuit using *Okashita's* teachings “to prevent leakage of radio frequency signals from the cascaded SOI FETs to other components of antenna switch 1700.” *Id.* at 61-62 (citing Ex. 1002, ¶¶ 215-16). Third, it states that the POSITA would have been motivated to locate each set of FETs together in one isolated region “to ensure that the[se] FETs have consistent performance characteristics” *Id.* at 63 (citing Ex. 1002 ¶ 217).

According to Mr. Berg, the POSITA would not have been motivated to use the SOI process disclosed in *Okashita* to fabricate the circuits in *Burgener* because, if Dr. Thompson is to be believed, *Okashita's* configuration increases source/drain capacitance and, therefore, would create a slower switching circuit. But, in the event Dr. Thompson is correct that such capacitance exists, it is my opinion that this capacitance would create performance issues that the POSITA would consider unfavorable. Ex. 2006, ¶ 66.

Dr. Thompson relies explicitly on *Burgener*'s Figure 17 for the disclosure of the "cascaded transistors" limitation. Ex. 1002, ¶ 221. *Burgener* states that: "Fig. 17 is a simplified schematic of exemplary circuitry 1700 for an antenna switch. *Further details regarding design and fabrication of such an RF switch may be found in U.S. Pat. No. 6,804,502, issued Oct. 12, 2004 and entitled "Switch Circuit and Method of Switching Radio Frequency Signals."* Ex. 1006, ¶ [0101]. According to Mr. Berg, given this express statement that the POSITA could look to the cited '502 patent for fabrication details specifically related to this circuit, the POSITA would have not been motivated to further look to *Okashita* in order to fabricate *Burgener*'s transistors. Ex. 2006, ¶ 67.

U.S. Patent No. 6,804,502 ("*Burgener II*," Ex. 2004), cited directly in *Burgener* as providing details for the fabrication of the exact circuit relied upon by Dr. Thompson, discloses a circuit fabricated on an "Ultra-Thin-Silicon ('UTSi') substrate" wherein "the transistors used to implement the inventive RF switch are formed in an extremely thin layer of silicon in an insulating sapphire wafer." Ex. 2004, 7:39-50. And, using this UTSi technology, "the parasitic capacitance between the nodes of the RF switch 30 are greatly reduced as compared with bulk CMOS and other traditional integrated circuit manufacturing technologies." *Id.* at 7:58-62.

Further, *Burgener II* states that the transistors in the RF switch can be made using ultra-thin silicon-on-sapphire technology, which eliminates the need for “[t]raditional transistor isolation wells” that are used for thick silicon. *Id.*, 10:66-11:1. According to Mr. Berg, the POSTIA, if anything, would have been motivated to use the silicon-on-sapphire technology disclosed in *Burgener II* to fabricate the antenna switch disclosed in *Burgener*, rather than be motivated to look to what Dr. Thompson admits is a higher capacitance and therefore slower technology disclosed in *Okashita*. Ex. 2006, ¶ 68.

Burgener states in a separate section that “[o]ther semiconductor-on-insulator (SOI) techniques may be used to fabricate a dual-band transceiver integrated circuit as described above, for at least some frequency bands and power levels.” Ex. 1006, ¶ [0105]. According to Mr. Berg, this does not provide motivation to the POSITA to look to *Okashita*, for the same reasons as above. Ex. 2006, ¶ 69. Neither the Petition, nor Dr. Thompson, provides any analysis of which frequency bands and/or power levels would motivate the POSITA to consider other semiconductor-on-insulator techniques aside from the UTSi technology that *Burgener* specifically advocates for. *Id.*

Further, *Burgener* and *Burgener II*'s motivation to use UTSi would not have led the POSITA to look to other SOI technologies, and specifically would not have led the POSITA to look to relatively thick silicon on top of a buried oxide layer, as shown in *Okashita* and as claimed by Dr. Thompson. Ex. 2006, ¶ 70. Although other types of SOI may have been used to construct the circuit in *Burgener*, the POSITA would not have been led to the construction techniques in *Okashita* because, as compared to UTSi, its high capacitance leads to decreased performance. In my opinion, the POSITA would not have had a reasonable expectation of success merely substituting thin silicon-on-sapphire for a relatively thick silicon on insulator technology, because of this additional capacitance. *Id.*

Additionally, the three purported “motivations” that the Petition provides for the combination of *Burgener* and *Okashita* are either incorrect or impermissible hindsight. First, it states that the POSITA would have been motivated to use the intervening silicon layer from *Okashita* because it would reduce the operating temperature of the transistors. Pet., 60-61 (citing Ex. 1002, ¶ 214). But heat considerations are not an issue in *Burgener*. Ex. 2006, ¶ 71. *Burgener* only mentions thermal considerations one time, when discussing the need for stacked FETs in the power amplifier section (rather than the antenna switch relied upon by

Dr. Thompson). Ex. 1006, ¶ [0044]. And even there, *Burgener* only discusses dissipating heat “in specific resistive series coupling elements rather than within the FETs themselves.” *Id.* Because *Burgener* states that dissipating heat inside the FETs is *not* desirable (rather, heat should be dissipated in the resistive couplings), the POSITA would not have been motivated to fabricate the transistors using what Dr. Thompson contends is a higher capacitance fabrication technique merely to dissipate additional heat in the transistors. Ex. 2006, ¶ 71.

Second, the Petition states that the POSITA would have been motivated to fabricate *Burgener*’s circuit using *Okashita*’s teachings “to prevent leakage of radio frequency signals from the cascaded SOI FETs to other components of antenna switch 1700.” Pet. at 61-62 (citing Ex. 1002 ¶¶ 215-16). *Burgener* states that the circuit should be made using UTSi technology. Ex. 2006, ¶ 72. UTSi technology is fully insulating, and “[t]he fully insulating sapphire substrate enhances the performance characteristics . . . by reducing the deleterious substrate coupling effects associated with non-insulating and partially insulating substrates.” Ex. 2004, 7:39-64. Therefore, according to Mr. Berg, the POSITA would not have been motivated to turn to another, less insulating SOI technology and then to build trenches as disclosed in *Okashita* to achieve insulating benefits that are already achieved by

Burgener. Ex. 2006, ¶ 72.

Third, the Petition states that the POSITA would have been motivated to locate each set of FETs together in one isolated region “to ensure that these FETs have consistent performance characteristics” Pet. at 63 (citing Ex. 1002, ¶ 217). Other than hindsight bias garnered from Claims 2, 14, and 17 of the ’886 Patent which require at least one of the plurality of transistors to be located within an isolated island, the POSITA would not have been motivated to locate each set of *Burgener’s* FETS together in one isolated region. Ex. 2006, ¶ 73. Consistent performance characteristics can be obtained through a number of methods, and placing the transistors in an isolated island would increase the space necessary for the circuit. *Id.* This would specifically motivate the POSITA *not* to do this because, according to *Burgener*, it is desirable to integrate many devices and fabricate them “onto a single integrated circuit,” thereby solving a multitude of problems and gaining significant benefits. *Id.* (citing Ex. 1006, ¶ [0010]).

2. The Combination of *Burgener* and *Okashita* Does Not Teach the Required Electrical Isolation of Claim 3

As above, the Petition relies entirely on the disclosures of *Okashita* for the electrical isolation claim elements. For the same reasons explained with respect to Ground 2, *Okashita* does not disclose or provide a motivation to create the

limitations of Claim 3 of the '886 Patent. Therefore, the combination of *Burgener* and *Okashita* does not render Claim 3 obvious.

**F. GROUND 6: The Challenged Claims Are Not Obvious Over
*Burgener, Okashita, and Yu***

Ground 6 fails for the same reasons as Ground 5. In addition to *Burgener* and *Okashita*, the Petition adds *Yu* for claim elements not discussed in this Preliminary Response. Because *Okashita* and *Burgener* cannot be combined, and because *Okashita* does not disclose the electrical isolation claim element, Ground 6 fails for the same reasons as Ground 5.

VII. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board issue a Final Written Decision finding that Claims 3 and 8-19 not shown to be unpatentable.

Respectfully submitted,

Dated: July 7, 2025

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CERTIFICATE OF WORD COUNT

The undersigned hereby certifies that the portions of the above-captioned PATENT OWNER'S RESPONSE specified in 37 C.F.R. § 42.24 has 6,297 words in compliance with the 14,000 word limit set forth in 37 C.F.R. § 42.24. This word count was prepared using Microsoft Word for Office 365.

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IPR2024-01402
PATENT NO. 7,745,886

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