

UNITED STATES PATENT & TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD. and
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioners,

- against- Patent No. 7,745,886

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

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DATE: June 17, 2025

TIME: 8:58 a.m.

DEPOSITION of SCOTT E. THOMPSON, Ph.D.,
held via Zoom videoconference, taken by the
Patent Owner, pursuant to a notice, held
remotely via Zoom Videoconference, before
Roberta Caiola, a Notary Public of the State
of New York.

A P P E A R A N C E S:

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1 S. Thompson

2 THE REPORTER: The parties and
3 counsel participating in this deposition
4 acknowledge that I am not physically
5 present and will be reporting this
6 deposition remotely.

7 They further acknowledge that, in
8 lieu of an oath administered in person, the
9 witness will be sworn in remotely.

10 The parties and their counsel
11 consent to this arrangement and waive any
12 objections to this manner of reporting.

13 Dr. Thompson, would you please raise
14 your right hand.

15 (Witness complies.)

16 THE REPORTER: Do you swear that the
17 testimony that you are about to give will
18 be the truth, the whole truth, and nothing
19 but the truth?

20 THE WITNESS: Yes.

21 SCOTT E. THOMPSON, Ph.D., having been first
22 duly sworn by a Notary Public of the State of
23 New York, was examined and testified as
24 follows:
25

1 S. Thompson

2 EXAMINATION BY

3 MR. MERCADANTE:

4 Q. Good morning, Dr. Thompson.

5 A. Good morning.

6 Q. My name is Joseph Mercadante. I
7 will be taking your deposition today.

8 Am I correct in assuming that you
9 have had your deposition taken before?

10 A. Yes.

11 Q. Approximately how many times?

12 A. More than ten.

13 Q. So I will presume that you are
14 familiar with -- sorry about that.

15 I will presume that you are familiar
16 with the procedure. I will just go over a few
17 rules.

18 Number one, of course, is please
19 pause after my question, so that there is no
20 crosstalk, where you begin your answer before I
21 am done asking my question. It also gives your
22 attorney some time to object in between, which
23 is, of course, his right to do.

24 Do you understand that?

25 A. Yes.

1 S. Thompson

2 Q. If you don't understand my question,
3 please ask me to rephrase it, rather than
4 thinking about what I might be trying to ask
5 and trying to answer that question.

6 Does that make sense?

7 A. Yes.

8 Q. If you give me an answer to one of
9 my questions, I will presume that you
10 understood it.

11 Is that fair?

12 A. Yes.

13 Q. From time to time, as I mentioned
14 earlier, your attorney may object. Even if he
15 objects, you still must answer the question,
16 unless he specifically instructs you not to
17 answer.

18 Is that understood?

19 A. Yes.

20 Q. And Dr. Thompson, is there any
21 reason that you cannot give me full and
22 truthful testimony today?

23 A. No.

24 Q. Are you under the influence of any
25 drugs or alcohol that could prevent your

1 S. Thompson

2 ability to recall facts?

3 A. No.

4 Q. Dr. Thompson, what did you do to
5 prepare for this deposition?

6 A. I met with some lawyers at Finnegan
7 yesterday, and also a Zoom call on Friday.

8 Q. Okay. Was the Zoom call also with
9 the same lawyers at Finnegan?

10 A. Yes.

11 Q. Who did you meet with; what were
12 their names?

13 A. So, the four lawyers are Mr. Zang,
14 Mr. Goldberg, Mr. Watwe, and Mr. Chandran.

15 Q. And approximately how long did you
16 spend preparing for this deposition?

17 A. I don't know the exact number. I
18 would estimate maybe 40 hours.

19 Q. Okay. And when I say "this
20 deposition," I mean the deposition that we're
21 conducting today, which we understand is going
22 to encompass both the '886 and '609 Patents.

23 Is that fair?

24 A. That's fair. And that's how I
25 answered the questions.

1 S. Thompson

2 Q. Dr. Thompson, when did you first get
3 involved in this case?

4 A. I don't know the exact date. It was
5 probably six, eight months ago.

6 Q. And you understand, Dr. Thompson,
7 that, in addition to the IPRs that we're
8 discussing today and that you discussed last
9 week, that there's also an underlying District
10 Court action between my client and Samsung; is
11 that correct?

12 A. I understand that, yes.

13 Q. Have you reviewed any of the
14 materials from the District Court action?

15 A. I have not.

16 Q. And have you been retained to
17 provide opinions in the District Court action?

18 A. Not to my knowledge.

19 Q. Okay. And you have done -- you have
20 served as an expert in IPRs before; is that
21 correct?

22 A. I have.

23 Q. Have you also served as an expert in
24 litigations, either at the ITC or in District
25 Court?

1 S. Thompson

2 A. Yes.

3 Q. Approximately how many?

4 A. Four.

5 Q. And have you ever been to trial in
6 any of those four actions?

7 A. Yes.

8 Q. How many times?

9 A. Three.

10 Q. I'm sorry, did you say three? You
11 broke up a little bit.

12 A. Three.

13 Q. Did you testify in those trials?

14 A. Yes.

15 Q. Where were they located?

16 A. One was in California and two were
17 in Beijing.

18 Q. What was the scope, or what was the
19 subject matter of the two cases that were in
20 Beijing?

21 A. The Chinese Academy of Science had
22 some patents that they were asserting against
23 Intel products in China.

24 Q. And you represented Intel?

25 A. Yes.

1 S. Thompson

2 Q. What about the case in California,
3 what was the subject matter of that case?

4 A. It was on RFID chips.

5 Q. Who did you represent in that case?

6 A. Impinj.

7 Q. Impinj.

8 I've put two exhibits in the chat.

9 Exhibit 1 is the '886 patent and Exhibit 2 is
10 your declaration on the IPR on the '886 patent.

11 (Exhibit 1, United States Patent
12 Number 7,745,886, marked for
13 identification.)

14 (Exhibit 2, Declaration of Dr. Scott
15 E. Thompson, Ph.D., in Support of Petition
16 for Inter Partes Review of United States
17 Patent No. 7,745,886, marked for
18 identification.)

19 Q. I would like to talk about your
20 declaration first, but I wanted to preserve the
21 exhibit numbering, so I kept them as 1 and 2,
22 if that's okay with you?

23 A. Yes. That's fine.

24 Q. Can you please open up your
25 declaration, which is Exhibit 2?

1 S. Thompson

2 A. I have it open.

3 Q. Okay. Could you turn to your CV,
4 which begins on page 148 of the PDF?

5 A. I am there.

6 Q. And subsection C is a list of your
7 legal cases; is that correct?

8 A. It's a list of my legal cases, I
9 believe, in the last four or five -- five years
10 or so.

11 Q. And so aside from this case, are
12 there any cases from the last five years that
13 are not listed here that you were engaged to
14 provide either consulting work or expert
15 testimony on?

16 A. There would be another case that I
17 was recently retained on, since I submitted
18 this. I haven't done any work on that case
19 yet.

20 Q. What is that case?

21 A. The client is TSMC, and it's on the
22 ITC case.

23 Q. Do you recall the name of the
24 complainant in that case?

25 A. I'm not sure.

1 S. Thompson

2 Q. Is it related to this IFT versus
3 TSMC ITC case that you did in 2019?

4 A. No.

5 Q. Okay. Have you ever represented a
6 patent owner or patent holder in either a
7 litigation or an IPR?

8 A. Yes.

9 Q. When was that?

10 A. The Impinj case, they were the
11 patent owner. I worked for the patent owner in
12 that case.

13 Q. Who was Impinj's adversary in that
14 case?

15 A. NXP.

16 Q. Is that case still ongoing?

17 A. No.

18 Q. Do you recall when it was resolved?

19 A. About a year ago.

20 Q. Did you work only on the IPRs in
21 that case or did you also work in the District
22 Court?

23 A. I did both.

24 Q. Okay. What was the result of that
25 case; did it go to verdict?

1 S. Thompson

2 A. It did. Some -- somewhat complex.
3 You can Google online what -- how it turned
4 out.

5 Q. Okay. But to your knowledge, there
6 was no settlement in that case; is that
7 correct?

8 A. No, I believe there was a
9 settlement.

10 Q. Okay. And prior -- so the cases
11 that you've listed here on your CV go back to
12 about 2017.

13 When did you first get involved in
14 doing expert witness work in patent cases?

15 A. Yeah, most of my career, I've spent
16 doing what I call real engineering work.

17 The first one was probably 2005.
18 After I left Intel, Intel was being sued on
19 some patents on strained silicon, and I -- I
20 helped Intel out on that patent litigation
21 around the year 2005.

22 Q. And who was the patent owner in that
23 case?

24 A. AmberWave.

25 Q. Dr. Thompson, going back up a little

1 S. Thompson

2 higher in your CV, in your professional
3 experience.

4 You mentioned earlier that you
5 worked for Intel from -- your CV says it was
6 1992 to 2004.

7 Is that accurate?

8 A. It's accurate. It doesn't capture
9 all the subtleties, but it's accurate.

10 Q. Okay. After Intel, you decided to
11 teach; is that correct?

12 A. Can you repeat the question?

13 Q. After Intel, you decided to teach;
14 is that correct?

15 A. I decided to work at a university to
16 do teaching and research, and also work in the
17 industry in a different fashion.

18 Q. Okay. You founded and were the CTO
19 of a company called Suvolta, that's
20 S-U-V-O-L-T-A.

21 What was Suvolta?

22 A. It was a low-power chip technology
23 company.

24 Q. Does Suvolta currently exist?

25 A. It does not.

1 S. Thompson

2 Q. According to your CV, it was sold to
3 Fujitsu; is that correct?

4 A. That's correct.

5 Q. Did Suvolta have any patents?

6 A. Yes.

7 Q. Were you a named inventor on any of
8 those patents?

9 A. Yes.

10 Q. Approximately how many patent
11 applications did Suvolta have when it was sold?

12 A. I don't know the exact number, but
13 more than 100, I believe.

14 Q. So the low-powered chips that
15 Suvolta made, at least according to your CV,
16 this technology was used in an image sensor
17 that was designed by Fujitsu; is that correct?

18 A. That's correct.

19 Q. And what -- what was the intended
20 purpose of these low-powered chips that you
21 were designing at Suvolta?

22 A. Suvolta was designing integrated
23 circuit technology that could work at low
24 voltage, meaning less than half a volt, and so
25 the purpose of that would go in many products.

1 S. Thompson

2 The purpose of those circuits were
3 for memory, for analog applications, and
4 digital applications.

5 Q. I see.

6 So it wasn't a particular type of
7 product that you were targeting, it was just
8 these low-voltage applications were going to be
9 useful all over the place; is that correct?

10 A. That's correct.

11 Q. Do you believe that Suvolta's
12 technology is still in use?

13 A. I do.

14 Q. Where are you located today,
15 physically, Dr. Thompson?

16 A. I'm in the Finnegan office, outside
17 of D.C.

18 Q. Okay. Is anyone in the room with
19 you?

20 A. Yes.

21 Q. Is it Dr. Zang?

22 A. Dr. Zang, and two other lawyers.

23 Q. Who are the two other attorneys?

24 A. Mr. Goldberg and Mr. Chandran.

25 Q. Dr. Thompson, do you have anything

1 S. Thompson

2 open on your computer, aside from Zoom and
3 programs that view PDFs?

4 A. I only have the program that opens
5 PDF on my -- my iPad.

6 Q. So you have an iPad and a computer
7 that you're doing the deposition on; is that
8 correct?

9 A. That's correct. And my iPad, it's a
10 clean iPad I only use for litigations. There's
11 no email on that. There's no messaging app.
12 There's -- it's just a clean iPad with the PDF
13 viewer.

14 Q. Okay. It sounds like you know the
15 drill for remote depositions. Obviously, it
16 would be improper for somebody to try to
17 contact you while we're on the record.

18 I ask that, you know, to the extent
19 some chat window pops up or you get an email or
20 something like that, that, you know, you let me
21 know.

22 Is that fair?

23 A. That's fair. Like I said, it's
24 in -- the iPad is in airplane mode. The Wi-Fi
25 is off. I don't have the mail applications

1 S. Thompson

2 installed on my computer either.

3 Q. Okay. So this declaration that is
4 Exhibit 2 was signed by you several months ago;
5 is that correct?

6 A. I signed it September 24, 2024.

7 Q. Since you signed this declaration,
8 have you reviewed any additional materials that
9 impact your ultimate opinions as expressed in
10 your declaration?

11 A. No.

12 Q. Have you reviewed the institution
13 decision issued by the Board in this
14 proceeding?

15 A. I have.

16 Q. Have you reviewed anything else that
17 could be relevant to your ultimate opinions
18 since September 24, 2024?

19 A. I have not.

20 Q. And over the course of your
21 preparation, or at any other time, did you
22 notice any errors in your declaration, typos or
23 otherwise, or anything that you feel you need
24 to correct?

25 A. No. There -- I -- I don't think

1 S. Thompson

2 there's anything that I need to correct. There
3 may be one typo that -- I don't even remember
4 where it is. When I was studying it, I thought
5 there was a minor typo. But, if it comes up, I
6 will point that out, but I don't think it needs
7 to be corrected.

8 Q. Okay. To the extent anything comes
9 to mind, please let me know.

10 A. Okay.

11 Q. Do you know a gentleman named Dean
12 Neikirk, N-E-I-K-I-R-K?

13 A. I do not believe I do.

14 Q. Are you aware that Dr. Neikirk
15 submitted a declaration regarding claim
16 construction of the '886 patent on behalf of
17 Samsung in the underlying District Court
18 litigation?

19 A. I am not aware of that.

20 Q. Okay. You have not reviewed any
21 declaration from another expert in this
22 dispute; is that correct?

23 A. That's correct.

24 Q. Okay. Can you please turn to
25 Exhibit 1, it's the '886 patent?

1 S. Thompson

2 A. I have that open.

3 Q. Okay. Prior to your engagement in
4 this litigation, had you seen the '886 patent?

5 A. I had not.

6 Q. Are you familiar with either of the
7 inventors of the '886 patent on a personal and
8 professional level?

9 A. I am not.

10 Q. Okay. The assignee listed on the
11 first page of the '886 patent is Newport Fab
12 LLC.

13 Do you see that?

14 A. Yes.

15 Q. Are you aware that Newport Fab LLC
16 is a d/b/a of Tower Semiconductor?

17 A. Vaguely. I've seen Newport Fab in
18 the news. I don't -- I know part of its
19 history. I don't know its whole history.

20 Q. What do you know about Tower
21 Semiconductor?

22 A. They are a foundry. They are a very
23 small foundry. They specialize more in RF
24 chips.

25 Q. Do you know where they're based out

1 S. Thompson

2 of?

3 A. Tower?

4 Q. Tower, yes.

5 A. I'm not 100 percent sure, no.

6 Q. Okay. Do you know where Newport Fab
7 are located?

8 A. I'm not 100 percent sure.

9 Q. Turning back to your declaration.

10 I would like to talk about your
11 opinion on the level of ordinary skill in the
12 art, which is located on page 50, beginning at
13 paragraph 105. Let me know when you're there.

14 A. I'm there.

15 Q. Were you provided with the level of
16 ordinary skill in the art to be applied in this
17 case or did you reach this conclusion on your
18 own?

19 A. This was my opinion. I was not
20 provided with that, no.

21 Q. And it's your opinion that a person
22 of ordinary skill in the art, pertinent to the
23 '886 patent, and I'm reading directly from
24 paragraph 106 here, would have had "at least a
25 master's degree in electrical engineering or a

1 S. Thompson

2 similar field and at least two years of
3 experience working with semiconductor systems
4 and semiconductor dice."

5 Did I read that correctly?

6 A. You did.

7 Q. What would be the similar fields
8 that would qualify as a person of ordinary
9 skill in the art, education-wise, in your
10 opinion?

11 Strike that question. That was a
12 terrible question. Let me try again.

13 So a master's degree in electrical
14 engineering or similar field would qualify
15 someone as a person of ordinary skill in the
16 art, partially; is that correct?

17 A. Can you repeat the question?

18 Q. Sure.

19 You state that a person of skill in
20 the art would have had at least a master's
21 degree in electrical engineering or a similar
22 field; is that correct?

23 A. That's correct.

24 Q. What fields, in your opinion, are
25 similar enough to electrical engineering to

1 S. Thompson

2 qualify someone as a person of ordinary skill
3 in the art?

4 A. There would be several. Physics,
5 with emphasis on solid phase physics, would
6 qualify. Material science. Chemical
7 engineering, with the right course work, would
8 also qualify.

9 Q. Any others that you can think of,
10 sitting here today?

11 A. There would be others. I think a
12 lot of the engineering fields, with the right
13 course work, would qualify.

14 Q. You need to have an understanding of
15 semiconductors and how they work; is that fair?

16 A. That's fair.

17 Q. Some people would consider computer
18 engineering to be similar to electrical
19 engineering, but if someone has a master's
20 degree in computer engineering, but doesn't
21 understand how semiconductors work, they would
22 not be a person of skill in the art; is that
23 correct?

24 MR. ZANG: Objection. Form.

25 A. So, computer engineering, like, at

1 S. Thompson

2 the University of Florida is in the same
3 department as electrical engineering; so,
4 again, it comes down to what the focus is and
5 the course work.

6 If they had semiconductor experience
7 in course work, and working in the industry,
8 that would still be adequate.

9 Q. Okay. In your opinion, it is
10 possible for someone with a bachelor's degree
11 to be a person of skill in the art, if they
12 have sufficient experience; is that correct?

13 A. That's correct.

14 Q. And you state that you were at least
15 a person of ordinary skill in the art as of
16 December 10, 2007; is that correct?

17 A. Correct.

18 Q. In fact, it's likely that you were a
19 person of extraordinary skill in the art at
20 that time; is that correct?

21 A. I would like to think so.

22 Q. I would like to turn now to your
23 grounds of unpatentability, which are based
24 upon Okashita, Yu and Burgener.

25 MR. MERCADANTE: For the court

1 S. Thompson

2 reporter, that's O-K-A-S-H-I-T-A, Yu is
3 Y-U, Burgener is B-U-R-G-E-N-E-R.

4 Q. Dr. Thompson, you have a background
5 section in your declaration titled "Technology
6 Background and" state-of-the-art -- "State of
7 the Prior Art."

8 Is that correct?

9 A. Let me find that.

10 Q. Sure. It starts on page 16 of your
11 report, if that makes it easier for you.

12 A. It does. Thank you.

13 Q. In this section, you rely on some
14 additional documents, aside from Okashita, Yu
15 and Burgener to describe the technology
16 background and state of the prior art; is that
17 correct?

18 A. I'm just giving these documents as
19 support for my opinions and what the industry
20 looked like in this time frame.

21 Q. Sure. And so those -- the documents
22 relied upon in your background section, aside
23 from Okashita, Yu and Burgener, are not relied
24 upon to create your ultimate validity opinions;
25 is that correct?

1 S. Thompson

2 MR. ZANG: Objection. Form.

3 A. My validity opinions are -- for the
4 different grounds are explained in the report.
5 You can find it in the index.

6 The other references are just
7 background to show what a POSITA would know,
8 what was commonly known in the industry.

9 Q. Could you please turn to page 36 of
10 your declaration, Dr. Thompson?

11 A. Yes.

12 Q. I just have a couple of questions
13 about claim construction. The claim
14 construction section actually begins at page
15 35, but the paragraph I wanted to talk about is
16 on page 36.

17 You state in paragraph 74: "I have
18 been asked, for purposes of this declaration,
19 to apply the plain and ordinary meaning of the
20 claim terms as they would have been understood
21 by a person of ordinary skill in the art at the
22 earliest claimed priority date of the '886
23 patent."

24 Do you see that?

25 A. I do see that.

1 S. Thompson

2 Q. And you were asked to apply the
3 plain meaning by -- by whom?

4 MR. ZANG: Objection. Form.

5 A. The legal team ask -- asked me that.

6 Q. And so you and the legal team did
7 not believe that any claim construction was
8 necessary to understand the terms in the '886
9 patent claims; is that correct?

10 MR. ZANG: Objection. Form.

11 A. For my invalidity analysis, I can
12 only speak for myself, I don't believe anything
13 is needed other than plain ordinary meaning to
14 resolve the issues that I addressed in my
15 report.

16 Q. And the '886 patent describes and
17 claims something called cascaded transistors;
18 is that correct?

19 A. In the claim 1, element 1A, there's
20 an element, a plurality of cascaded
21 transistors.

22 Q. So the answer to my question is yes?

23 A. Can you repeat your question?

24 Q. The '886 patent describes and claims
25 something called cascaded transistors; is that

1 S. Thompson

2 correct?

3 A. It claims a plurality of cascaded
4 transistors fabricated in the device layer.

5 Q. Okay. And in your analysis of this
6 element, you propose a definition of cascaded
7 transistors; and that's in paragraph 115, if
8 you would like to refer to your report in
9 answering my question.

10 MR. ZANG: Objection.

11 Mischaracterization of the record.

12 A. So I don't give a definition, but I
13 say a POSITA would understand that cascaded
14 transistors are coupled in series, and I give
15 support for that, and I also refer to
16 Okashita's -- not Okashita, but the '886 spec,
17 where it also acknowledges transistors coupled
18 in series are considered cascaded.

19 Q. Where do you say that the POSITA
20 would understand that cascaded transistors are
21 coupled in series in your declaration?

22 A. When I say, "in my opinion," I'm
23 giving you an opinion of what a POSITA would
24 understand.

25 Q. So you state that: "'Cascaded

1 S. Thompson

2 transistors' refer to transistors 'arranged'
3 ... in a series or in a succession of stages so
4 that each stage derives from or acts upon the
5 product of the preceding.'" "

6 Did I read that correctly in
7 paragraph 115 of your declaration?

8 A. I believe you read that correctly,
9 yes.

10 Q. Okay. Then you cite to Exhibit 1007
11 at page 5; is that correct?

12 A. Correct.

13 Q. I'm going to have to go out of order
14 a little bit here, but I will mark Exhibit 1007
15 to the IPR as Exhibit 3 to this deposition.

16 (Exhibit 3, Pages from Webster's
17 College Dictionary, marked for
18 identification.)

19 Q. And I have placed that in the chat.

20 Let me know when you have Exhibit 3
21 and/or Exhibit 1007 from the declaration.

22 A. I have it.

23 Q. What is this exhibit, Dr. Thompson?

24 A. Pages from Webster's College
25 Dictionary.

1 S. Thompson

2 Q. Do you own Webster's Ninth New
3 Collegiate Dictionary or was this provided to
4 you?

5 A. This was provided.

6 Q. By whom?

7 A. One of the lawyers.

8 Q. And is it your understanding that
9 this is a technical dictionary, Dr. Thompson?

10 MR. ZANG: Objection. Form.

11 A. It can be. When I reviewed this,
12 it's the same language I would have used to
13 describe cascaded. It's -- it's what I think a
14 POSITA would understand cascaded to be. It's
15 what the '886 describes it to be.

16 Q. So the definition of cascade, in
17 Webster's Dictionary, is, in your opinion, the
18 plain meaning of the term "cascaded," as it's
19 used in the claims of the '886 patent; is that
20 correct?

21 MR. ZANG: Objection. Form.

22 A. If you look at the figure 4 of the
23 '886 patent, they show a standard series
24 connection of transistors, and that's the only
25 circuit configuration the '886 gives.

1 S. Thompson

2 A POSITA would understand that
3 string of transistors are connected in series,
4 and they're cascaded, and the current runs from
5 one transistor to the next down the string.

6 MR. MERCADANTE: Objection.

7 Non-responsive.

8 Q. I will ask the question again.

9 The definition of cascade, in
10 Webster's Dictionary, is, in your opinion, the
11 plain meaning of the term "cascaded," as it's
12 used in the claims of the '886 patent; is that
13 correct?

14 MR. ZANG: Repeated objection.

15 A. I'm simply using Webster's
16 Dictionary to support what I just said, how a
17 POSITA would understand what cascaded is.

18 Q. Okay. So you have, in my opinion,
19 two contrary statements in your declaration
20 that I'm trying to square.

21 In the claim construction section,
22 you say that no construction is needed and you
23 apply the plain meaning.

24 And then in your analysis, you apply
25 this definition of cascade.

1 S. Thompson

2 And so what I'm just trying to get
3 an understanding of is whether one of those two
4 statements is an error or if it's your opinion
5 that the definition is the plain meaning of the
6 word cascade, or cascaded?

7 MR. ZANG: Objection.

8 Mischaracterization.

9 A. So I'm not defining the word. I'm
10 just giving you -- and when I -- when I'm
11 showing the Webster's Dictionary, I'm just
12 giving you support.

13 Q. So there could be another definition
14 of cascaded that is not Webster's Dictionary,
15 that could define the plain meaning of the term
16 "cascaded," in your opinion?

17 MR. ZANG: Objection. Form.

18 A. In my opinion, the plain ordinary
19 meaning is all that's needed to resolve
20 invalidity, and a POSITA looking at the spec
21 would understand cascaded is series connected,
22 because the '886 spec says that, and that's
23 commonly how transistors are connected.

24 And I'm saying that's all that's
25 needed to resolve invalidity, and I'm just now

1 S. Thompson

2 giving some extra support to back it up.

3 What I'm saying is it's also
4 consistent with what's in the dictionary.

5 Q. In order to be series connected and,
6 therefore, cascaded, do transistors need to
7 always be series connected?

8 MR. ZANG: Objection. Form.

9 A. It depends on if you're talking
10 about reconfiguring, computing, and it depends
11 on a lot of things you're not specifying.

12 What I can tell you is the -- I
13 teach a circuits class at the University of
14 Florida. The most common -- one of the most
15 common circuits used are nanogates. And so
16 nanogates have a string of transistors just
17 like the figure 4 of the patent.

18 And, in a nanogate, that string is
19 considered in series and cascaded, and whether
20 the transistors are on or off, they're still
21 considered to be in series and cascaded.

22 Q. And you mentioned, I think, earlier
23 that cascaded transistors were well-known; is
24 that correct?

25 A. Connecting transistors in series has

1 S. Thompson

2 been done for 50 years. More than 50 years.

3 Q. And why would someone connect
4 multiple transistors in series; what does that
5 accomplish, technically?

6 MR. ZANG: Objection. Form.

7 A. There's many reasons why one would
8 connect transistors in series. The '886 patent
9 teaches one reason; and the voltage drop is
10 spread across the transistors is one reason.

11 Q. Are there any other reasons that you
12 can think of?

13 A. Yes. You want the current from one
14 transistor to be derived from another
15 transistor.

16 Q. What about speed, if you have --
17 like, let's say you had five series connected
18 small transistors in place of one large
19 transistor; are there instances in which that
20 configuration would be quicker to operate?

21 MR. ZANG: Objection. Form.

22 A. Again, it's going to depend on a lot
23 of conditions you're not telling me.

24 But there could be an example where
25 I put a large voltage across one transistor, it

1 S. Thompson

2 would be faster than that same voltage across
3 two transistors, but the reliability would not
4 be the same for the two circuits.

5 Q. You're right that we're somewhat
6 talking about the hypothetical.

7 This morning, I was having breakfast
8 with my four-year old, and I drew some
9 transistors on some of her notepaper, which
10 I've now put into the chat as Exhibit 4.

11 (Exhibit 4, drawings, marked for
12 identification.)

13 Q. Can you please open Exhibit 4,
14 Dr. Thompson?

15 A. I have Exhibit 4 open.

16 Q. Do you see on the first page of
17 Exhibit 4, I've drawn three transistors,
18 labeled them 1, 2, 3?

19 MR. ZANG: Objection. Form.

20 A. I do. What type of transistors are
21 these?

22 Q. Let's assume that they are MOS
23 transistors for the purposes of this
24 discussion.

25 A. And what are you doing to the body

1 S. Thompson
2 of the MOS of these transistors?

3 Q. Does it matter?

4 A. It could.

5 Q. Well, how about this: If it matters
6 in answering one of my questions, let me know.

7 Would you agree with me that on page
8 1, transistors 1, 2 and 3 are cascaded, in your
9 opinion?

10 MR. ZANG: Objection. Scope.

11 A. They're common electrodes for 1, 2
12 and 3?

13 Q. Let's assume yes.

14 A. So if I put a voltage, say
15 five volts, on the gauge, then all three
16 transistors will be turned on?

17 Q. That's correct.

18 A. And I'm going to put zero volts on
19 the left side of the diagram and I'm going to
20 put five volts on the right side of the
21 diagram?

22 Q. Either way. Does it matter?

23 A. It could. So --

24 Q. Well, let's assume that one side of
25 the diagram is five volts, the other side is

1 S. Thompson

2 ground, and that the control signal turns all
3 three transistors on or off.

4 A. Okay. So then, to make sure I
5 understand how your circuit works, the current
6 is going to come from the drain of the left,
7 it's going to go through transistor 3, to
8 transistor 2, to transistor 1, and then out --
9 out the left; is that correct?

10 Q. That is correct.

11 A. So based on what I described for
12 that operation, I would say those transistors
13 are in series.

14 Q. And, therefore, cascaded?

15 A. And, therefore, cascaded.

16 Q. If the control signal were off, are
17 the three transistors shown on page 1 still
18 cascaded, in your opinion?

19 MR. ZANG: Objection. Scope.

20 A. So this is not in my report. If
21 these -- if these three transistors were part
22 of a three-input NAND string, it's common for
23 transistors to be on and off in that string, an
24 engineering would still describe that NAND
25 string to be a cascaded or a series connected

1 S. Thompson

2 string of three MOS transistors.

3 Q. Okay. Can you please turn to page 2
4 of Exhibit 4?

5 A. Remind me what Exhibit 4 is?

6 Q. Exhibit 4 is the hand-drawn pictures
7 of transistors that we've been talking about.

8 A. Okay. Is there a question about
9 that?

10 Q. No. I was just waiting for you to
11 get to page 2.

12 A. Okay. Page 2. I'm sorry.

13 Q. Do you see four transistors on page
14 2, Dr. Thompson?

15 MR. ZANG: Objection. Form.

16 A. I do.

17 Q. And you will see that I've tied the
18 transistor labeled 4 to ground; is that
19 correct?

20 MR. ZANG: Objection. Form, and
21 scope.

22 A. I see a bottom terminal of
23 transistor 4 with a, I believe, a ground
24 signal. It does appear connected. I'm
25 assuming you -- you mean it to be connected to

1 S. Thompson

2 ground there.

3 Q. I do.

4 So transistors 1, 2 and 3 on page 2
5 are connected identically to those three
6 transistors on page 1, but their control
7 signals are not tied together.

8 Do you see that?

9 MR. ZANG: Objection. Form, and to
10 scope.

11 A. I do see that.

12 Q. Okay. And so I think you answered
13 earlier that, if you had a three-input NAND
14 gate, and some of the control signals were on
15 and some were not, that the person of skill in
16 the art would still understand that those
17 transistors, those three transistors, were
18 connected in series.

19 Is that an accurate summary of your
20 earlier testimony?

21 MR. ZANG: Objection. Scope, form,
22 and a mischaracterization.

23 A. I said earlier, for the circuit you
24 drew, for the case I analyzed with those
25 voltages, with no other current, past, present,

1 S. Thompson

2 that those three transistors were cascaded in
3 series, and it was true whether the gates were
4 on or off.

5 Q. And so, looking at page 2 of
6 Exhibit 4.

7 If transistor number 4 is off and,
8 therefore, there is no path to ground to
9 transistor 4, would you agree with me that
10 transistors 1, 2 and 3 are cascaded, regardless
11 of the state of their control signals?

12 MR. ZANG: Objection. Form, and to
13 scope.

14 A. So now you're describing a much
15 different circuit. Change of topography.

16 And, again, this is not something in
17 my report. If I remove 4 from the circuit
18 diagram, I cut the line, so I'm now back to the
19 same drawing we discussed in case 1, and I put
20 the same voltages on I had in case 1, that is a
21 series strength of 1, 2 and 3.

22 Now, in this topography, you changed
23 topography, you changed the current flows, so
24 the statements I've made for the previous
25 diagram do not apply to this diagram.

1 S. Thompson

2 Q. But in this diagram, if transistor 4
3 is off, it sounds like you do agree that
4 transistors 1, 2 and 3 are cascaded; is that
5 correct?

6 MR. ZANG: Objection. Form, scope,
7 mischaracterization.

8 A. That's not what I said. I said, if
9 you cut the line and you remove transistor 4
10 from that circuit, they are cascaded.

11 Q. If transistor 4 is turned on and
12 tied to ground, what is transistor 4 cascaded
13 with, if anything?

14 MR. ZANG: Objection. Scope. Form.

15 A. It's going to depend on a lot of
16 parameters you're not specifying.

17 What's happening now to the -- the
18 drain terminal of transistor 3 which you have
19 floating?

20 So, before I give you more answers
21 to that, I would need to know all of the bias
22 conditions and how the circuit is being used.

23 Q. If current flows from -- let's say
24 transistors 1 and 2 are on, transistor 3 is
25 off, and transistor 4 is on; are you with me so

1 S. Thompson

2 far?

3 A. 1 is on, 2 is on?

4 Q. Correct. 3 is off. 4 is on.

5 Current flows from transistor 1 to
6 2, through 4, to ground.

7 Are you with me?

8 A. It could, depending on bias.

9 Q. That wasn't a question. I'm setting
10 up the hypothetical.

11 I'm telling you to assume that
12 current is flowing through 1, through 2,
13 through 4, to ground.

14 Are you with me so far?

15 A. Current is flowing, but you would
16 need certain bias conditions for that to occur.

17 Q. And let's assume that those bias
18 conditions are met and that current is flowing
19 through 1, through 2, through 4, to ground,
20 would you consider and/or would the person of
21 ordinary skill in the art consider, transistors
22 1, 2 and 4 to be cascaded in that situation?

23 MR. ZANG: Objection. Form. Scope.

24 A. If I had 1, 2 and 4 on, and I,
25 again, take 3 and I cut the line there, so 3 is

1 S. Thompson
2 no longer in the -- in the circuits, then we're
3 back to the same case 1.

4 So 1, 2 and 4 are in series or
5 cascaded, the current flows through the same
6 stack.

7 Q. What if the line weren't cut, but,
8 rather, transistor 3 was simply off, would your
9 opinion change?

10 MR. ZANG: Objection. Form. Scope.

11 A. I would have to know more about the
12 circuit.

13 Q. Let's assume that transistor 3 is
14 not conducting current, would your opinion
15 change?

16 MR. ZANG: Objection. Form. Scope.

17 A. So this is an important proceeding,
18 so I would want to study this in detail before
19 I give you an answer on that. This is not
20 something that's in my report.

21 Q. So you can't answer?

22 A. I would want to study this with
23 textbooks and bias conditions, and give you a
24 set of assumptions so that we're grounded on
25 the same facts.

1 S. Thompson

2 Q. Okay. Just so we're clear, if
3 transistors 1, 2 and 4 are on and transistor 3
4 is off, and current is flowing through 1,
5 through 2, through 4, to ground, you cannot
6 tell me if transistors 1, 2 and 4 are cascaded?

7 MR. ZANG: Objection. Form. Scope.

8 A. No. I said if I -- if it's off, and
9 I break the connection there, then 1, 2 and 4
10 are in series.

11 Q. I understand that. And then I asked
12 you, if there is no broken connection, if
13 transistor 3 is simply off and not conducting
14 current, not being overwhelmed by a huge bias,
15 if transistor 3 is not conducting current, in
16 this hypothetical, and current is flowing from
17 1, to 2, to 4, to ground, are transistors 1, 2
18 and 4 cascaded?

19 MR. ZANG: Objection. Form. Scope.

20 A. Yes, that's something I would want
21 to study more before giving you an opinion on.

22 Q. Okay. Could you please turn to the
23 following page, page 3 of Exhibit 4,
24 Dr. Thompson.

25 Let me know when you're there.

1 S. Thompson

2 A. I'm here.

3 Q. I've also drawn three transistors on
4 page 3. It looks like my number 3 got a little
5 messed up.

6 But do you understand the transistor
7 on the left to be number 1 and the transistors
8 on the right to be numbers 2 and 3?

9 MR. ZANG: Objection. Form. Scope.

10 A. I understand there's three
11 transistors here. They're MOS transistors.
12 There's no body bias to these transistors. And
13 I see the network not connected to anything
14 either.

15 Q. Okay. So let's assume that the top
16 is five volts and the bottom is ground.

17 Are you with me so far?

18 MR. ZANG: Objection. Form. Scope.

19 A. So you're applying five volts DC to
20 the top -- top electrode there in that circle
21 and zero volts to the bottom electrode?

22 Q. That's correct.

23 A. Okay.

24 Q. If transistor 1 is off, transistors
25 2 and 3 are on, and conducting current --

1 S. Thompson

2 MR. ZANG: Repeated objections.

3 Q. -- are --

4 MR. MERCADANTE: Counsel, could you
5 just wait for me to finish my question?

6 MR. ZANG: Yes.

7 Q. If transistor 1 is off, transistors
8 2 and 3 are on, and conducting current, are
9 transistors 2 and 3 cascaded, in your opinion?

10 MR. ZANG: Objection. Form. Scope.

11 A. So, again, that's not in my report,
12 but I'm making certain assumptions on how these
13 terms are working.

14 But 2 and 3 are in series and
15 cascaded for the operation I'm envisioning.

16 Q. And if transistors 1, 2 and 3 are
17 all on and are all conducting current, is
18 transistor 1 in series or cascaded with either
19 transistor 2 or 3 or both of them?

20 MR. ZANG: Objection. Form. Scope.

21 A. Again, for the -- for the
22 transistors I'm assuming here, the body
23 potential I'm assuming, transistors 2 and 3 are
24 in a series. 1 is not in a series.

25 Q. So in your opinion, whether

1 S. Thompson

2 transistors are in series can depend on the
3 operating state of the individual transistors;
4 is that correct?

5 MR. ZANG: Objection. Form. Scope.

6 A. It would depend on many things. The
7 circuit being reconfigured is one variable.

8 But what I said was, if I take a
9 case like the circuit in the '886 patent,
10 figure 4, or in NAND gate, those transistors
11 are in series and cascaded independent of
12 the -- whether the transistors are on or off.

13 Q. And if we turn to page 2 of
14 Exhibit 4, that's the four transistor
15 configuration that we just got done talking
16 about.

17 Let me know when you're there.

18 A. Yes.

19 Q. Whether these transistors are
20 cascaded with one another depends upon their
21 input signals; is that correct?

22 MR. ZANG: Objection. Form. Scope.

23 A. Yeah. So that's what I would want
24 to study before giving you an opinion on that.

25 MR. MERCADANTE: We've been going

1 S. Thompson

2 about an hour. I would like to take a
3 five-minute break, if that's okay with
4 everybody else.

5 MR. ZANG: Works for us.

6 (Whereupon, a recess was taken.)

7 Q. Welcome back, Dr. Thompson.

8 A. Thank you.

9 Q. Have you ever heard of a transistor
10 configuration called cascoded transistors, it's
11 C-A-S-C-O-D-E-D, rather than cascaded, with an
12 A?

13 MR. ZANG: Objection. Scope.

14 A. I've heard that term.

15 Q. What is your understanding of what
16 cascoded transistors are?

17 MR. ZANG: Objection. Scope and
18 form.

19 A. So that's not in my report. I would
20 have to see context for how that would be used.

21 Q. Okay. So you don't -- without
22 context, you can't tell me what cascoded
23 transistors are, or do?

24 MR. ZANG: Objection. Form.

25 A. Well, again, these are important

1 S. Thompson

2 procedures; I would want to consult a number of
3 textbooks and give you an opinion with
4 confidence before I do that.

5 Q. So you don't have an opinion in your
6 declaration in this case on cascoded
7 transistors; is that correct?

8 MR. ZANG: Objection to form.

9 A. So the word you're saying is
10 C-A-S-C-O-D-E?

11 Q. D-E-D. Cascoded. Or cascode in the
12 singular, I suppose.

13 A. C-A-S-C-O-D-E-S -- D.

14 So, yeah, that word is not used in
15 my report.

16 MR. MERCADANTE: Okay. I put
17 Exhibit 5 into the chat, which is Exhibit 4
18 from the IPR, which is the Okashita patent.

19 (Exhibit 5, United States Patent
20 Number 6,836,172 B2, Okashita, marked for
21 identification.)

22 MR. MERCADANTE: For the record,
23 that's U.S. Patent 6836172.

24 Q. Dr. Thompson, let me know when you
25 have Okashita open.

1 S. Thompson

2 A. I have Okashita open.

3 Q. Your opinion is that Okashita
4 anticipates and also renders obvious some of
5 the challenged claims of the '886 patent; is
6 that correct?

7 A. So, for ground 1, I have Okashita
8 anticipates claims 1, 2, 4 and 5. And then for
9 ground 2, I have a single reference obvious for
10 Okashita for claims 1 through 7.

11 Q. And in the anticipation ground,
12 ground 1, do you rely at all on inherent
13 anticipation?

14 MR. ZANG: Objection to form.

15 A. In ground 1, I'm simply saying a
16 POSITA reading Okashita for those claims
17 understands reading the spec that those claim
18 elements are all there.

19 Q. By "all there," you mean all in
20 Okashita; is that correct?

21 A. They're all in Okashita, as
22 understood by reading the spec.

23 Q. Okay. But you do not rely on
24 inherent anticipation in ground 1; is that
25 correct?

1 S. Thompson

2 MR. ZANG: Objection to form.

3 A. I'm saying a POSITA reading the spec
4 understands the elements needed for the claim
5 in ground 1 are all present.

6 Q. Can you answer whether you are
7 relying on inherent anticipation in ground 1;
8 yes or no?

9 MR. ZANG: Objection. Form.

10 A. My aim, as an engineer, is to
11 read -- read the patent and explain to you what
12 a POSITA would understand. And it is my
13 opinion that a POSITA reading Okashita
14 understands those elements are all present for
15 claims 1, 2, 4 and 5.

16 Q. Without the use of inherency; is
17 that correct?

18 MR. ZANG: Objection. Form.

19 A. I'm saying a POSITA simply reading
20 the spec of Okashita understands those claim
21 elements are present.

22 Q. Do you have your declaration open,
23 Exhibit 2?

24 A. I do.

25 Q. Do you have the ability to word

1 S. Thompson

2 search that document on your iPad?

3 A. I do.

4 Q. Could you do a word search for the
5 term "inherent" and let me know how many hits
6 you receive?

7 A. I-N?

8 Q. I-N-H-E --

9 A. H-E --

10 Q. -- R-E --

11 A. R-E --

12 Q. -- N-T.

13 A. N-T. There are no hits.

14 Q. Okay. Could you turn back to
15 Okashita, please, Exhibit 5 to the deposition,
16 Exhibit 4 to the IPR?

17 A. I have Okashita open.

18 Q. Prior to being retained for this
19 case, had you seen this patent before?

20 A. I have.

21 Q. In what context had you seen this
22 patent prior to your being retained for this
23 case?

24 A. Okashita is a body-contacted SOI. I
25 probably had 50 patents on body-contacted

1 S. Thompson

2 transistors.

3 So, different transistor structures,
4 including SOI, is something I've studied for 30
5 years.

6 Q. So you came to understand, or came
7 to know about the Okashita patent outside of
8 the scope of litigation; is that correct?

9 A. I had -- I had seen the concept of
10 body-contacted SOI outside the context of
11 litigation, correct.

12 Q. Could you please turn to column 1 of
13 the text of Okashita, it's on page 25 of the
14 PDF?

15 A. I'm at column 1.

16 Q. Do you see there's a section called
17 "Description of the Related Art"?

18 A. I see descriptions of the drawings.

19 Q. Column 1, line 10, says "Description
20 of the Related Art"?

21 A. Oh, I see it, yes. "Description of
22 the Related Art," correct.

23 Q. In this section, particularly in the
24 second to last paragraph, there is citations to
25 two patents, a Japanese patent that ends in

1 S. Thompson

2 '786 and a U.S. patent that ends in '088.

3 Do you see that, around line 32,
4 34-ish?

5 A. Yes.

6 Q. Did you review those patents and
7 consider them in forming your opinions?

8 A. Are they on my "materials
9 considered" list?

10 Q. They are not.

11 A. Then I did not.

12 Q. Okay. This "Background of the
13 Invention" section also mentions GaAsFETs.

14 Do you understand that to mean
15 gallium arsenide?

16 A. I do.

17 Q. What are gallium arsenide FETs?

18 MR. MERCADANTE: And, I'm sorry, for
19 the court reporter, that's -- actually,
20 I'll just put it in the chat. It's easier
21 than spelling it on the record.

22 MR. ZANG: Objection. Scope.

23 A. They're a -- a type of transistor
24 where the semiconductor material is made --

25 (Reporter seeks clarification.)

1 S. Thompson

2 A. Gallium arsenide FETs are a type of
3 transistor where the semiconductor material is
4 gallium arsenide.

5 Q. And in what situations would the
6 person of skill in the art be motivated to use
7 gallium arsenide to construct transistors?

8 MR. ZANG: Objection. Scope.

9 A. So, I've used gallium arsenide field
10 effect transistors in my work. There can be a
11 few performance reasons why you would want to
12 use them; one being the electromobility can be
13 higher in gallium arsenide than it is in
14 silicon.

15 Q. I'm going to read from column 1,
16 starting at line 20 from Okashita. Here, he's
17 talking about prior art semiconductors, not his
18 own design.

19 He says: "Also, since a substrate
20 of the gallium arsenide FETs is made of
21 semi-insulating material having a high
22 resistance, the leakage of radio frequency
23 signals via the substrate can be suppressed."

24 Did I read that correctly, and do
25 you see that sentence?

1 S. Thompson

2 A. I do.

3 Q. Did I read it correctly?

4 A. I believe you did.

5 Q. Okay. What is leakage of radio
6 signals?

7 MR. ZANG: Objection. Form.

8 Q. I'm sorry, radio frequency signals.
9 Let me -- let me re-ask the
10 question.

11 What is leakage of radio frequency
12 signals?

13 MR. ZANG: Objection. Form.

14 A. In the context of a radio, the
15 leakages is current going in a region you don't
16 want the current to go.

17 Q. And that can cause the circuit to
18 misbehave; is that correct?

19 MR. ZANG: Objection. Form.

20 A. If you look at Figure 6 of
21 Okashita -- let me know when you're there.

22 Q. Hold on one second.

23 I'm there.

24 A. So he talks about three components
25 of leakage in Figure 6. There's an X leakage

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2 that's going from one device layer to another
3 device layer through the substrate.

4 There's another component, a leakage
5 called the Y leakage, going from a device layer
6 to another device layer.

7 And then there's a Z component
8 leakage, which I'm going to ignore for now.

9 So these are all unwanted currents,
10 and Okashita has a device structure that helps
11 reduce the leakage components of X, Y and Z.

12 Q. And the '886 patent uses the term
13 "device layer" in the claim.

14 Do you recall that?

15 A. In claim 1, where I wrote that as
16 1.a, it says "a plurality of cascaded
17 transistors fabricated in a device layer..."

18 Q. And -- hold on. I've lost the
19 declaration. One second.

20 We are going to talk about Okashita,
21 but I would like to refer to your report -- or,
22 I'm sorry, your declaration, because I find
23 that some of the colored annotations that you
24 made made it a little easier to understand the
25 figures in Okashita.

1 S. Thompson

2 So just give me one minute.

3 Apologies. I had a little mishap on my end.

4 A. So, thank you. I agree. It's
5 easier to look at these when they're annotated.

6 Q. Right.

7 So could you turn to pages 52 and 53
8 of your declaration? It's where you start to
9 discuss the plurality of cascaded transistors
10 elements in the anticipation ground.

11 Let me know when you're there.

12 A. You're referring to paragraph 115?

13 Q. I'm going to start at 112, is where
14 the section starts, and then there's a -- you
15 annotated Okashita Figures 7 and 9 at the very
16 top of page 53.

17 A. Okay. So I'm in paragraph 112, so
18 I'm ready.

19 Q. Okay. So I want to talk about that
20 diagram, your colored figures that's on the top
21 of page 53.

22 So, in your opinion, the claimed
23 device layer is the blue annotated region in
24 Figure 9 of Okashita; is that correct, the
25 p-type silicon layer?

1 S. Thompson

2 A. It's p-type silicon layer 23.

3 Q. Okay. And it's a device layer,
4 because that's the layer that the devices,
5 including the transistors, are fabricated in in
6 Okashita; is that correct?

7 MR. ZANG: Objection. Form.

8 A. In Okashita, transistors 1 and 2 are
9 fabricated in the blue p-type device layer,
10 correct.

11 Q. And the brown annotated layer that
12 is 22 is silicon oxide; is that correct?

13 A. 22 is a silicon oxide layer,
14 correct.

15 Q. And that's sometimes also referred
16 to as buried oxide?

17 A. In an SOI device, it's common to
18 refer to that as the BOX, or buried oxide,
19 correct.

20 (Reporter seeks clarification.)

21 THE WITNESS: Buried oxide. And
22 then BOX is all capital.

23 MR. MERCADANTE: I will also make a
24 comment for the record that I am blue-green
25 colorblind, so if I ever start referring to

1 S. Thompson

2 a color that does not seem to be the
3 correct color in your annotations, please
4 let me know; I have had that occur in
5 depositions before.

6 And I will say that the picture
7 behind you in the background is killing me.
8 As a colorblind individual, I'm used to
9 staring at those things and not seeing what
10 I'm supposed to see.

11 Anyway.

12 Q. So you mentioned, in an SOI device,
13 layer 22 in Okashita is sometimes referred to
14 as buried oxide, or BOX; is that correct?

15 A. That's correct.

16 Q. What is an SOI device; what does
17 that acronym stand for?

18 A. It stands for silicon on insulator.

19 Q. And the '886 patent that we've been
20 discussing so far also talks about silicon
21 insulators; is that correct?

22 A. Yes. In the title of '886, it uses
23 the term "silicon on insulator (SOI)."

24 Q. What is a silicon-on-insulator
25 device?

1 S. Thompson

2 MR. ZANG: Objection. Form.

3 A. A silicon on insulator is describing
4 silicon that's on top of an insulator.

5 So silicon insulator is referring to
6 a wafer type.

7 Q. And is a silicon-on-insulator wafer
8 generally more expensive than using bulk
9 silicon to create the same circuits?

10 MR. ZANG: Objection. Form.

11 A. It's a -- a complex question you're
12 asking. The starting wafer type, the starting
13 wafer itself of silicon on insulator is more
14 expensive than a bulk wafer.

15 When you get to the final product,
16 in circuits, the yield is a factor, too, so it
17 may not translate to the final product, is what
18 we're saying.

19 Q. And I was -- thank you for pointing
20 out that issue with my question.

21 The starting wafer type for silicon
22 on insulator is more expensive than bulk
23 silicon; is that correct?

24 MR. ZANG: Objection. Form.

25 A. At Intel, where I worked for about

1 S. Thompson

2 13 years, all our microprocessors were made on
3 bulk. We evaluated silicon on insulator
4 continuously, because IBM was pushing that
5 technology, and IBM made chips with that
6 technology; so it's kind of a -- like a
7 religious war, bulk versus SOI.

8 For the assumptions we had at Intel
9 for the starting wafer, we thought the starting
10 wafer was meaningfully more expensive than a
11 bulk wafer.

12 Q. And in Figure 7 of Okashita, which
13 you have annotated here on the left side of
14 page 53 of your report, it's your opinion that
15 transistors T1 and T2, which are annotated in
16 green, or let's call it teal, are cascaded
17 transistors, as claimed in the '886 patent; is
18 that correct?

19 A. T1 and T2 that are described in the
20 report are cascaded, and they are connected in
21 series.

22 Q. Are they cascaded because they are
23 connected in series?

24 MR. ZANG: Objection. Form.

25 A. The '886 patent states that

1 S. Thompson
2 transistors that are coupled in series are
3 cascaded, and so the POSITA would look at the
4 transistors in Figure 7 of Okashita and realize
5 they're in a series and, therefore, they're
6 cascaded.

7 Q. In Figure 7 of Okashita, if
8 transistor 1 is turned on and transistor 2 is
9 turned off, are they cascaded?

10 MR. ZANG: Objection. Scope and
11 form.

12 A. So, independent of bias condition,
13 T1 and T2 are connected in series. If T1 is
14 off, there's still an off-state leakage current
15 that flows through T1, from the drain to the
16 source, and in this circuit, that same
17 off-state leakage current would flow through
18 T2.

19 Q. I think you misunderstood my
20 hypothetical. I had asked if transistor T1 was
21 on, and transistor T2 was off, if you would
22 consider those two transistors to be cascaded?

23 MR. ZANG: Repeated, the same
24 objections.

25 A. For all cases of transistor 1 and 2,

1 S. Thompson

2 on/off, any combination you propose, my opinion
3 is these transistors are in series, because the
4 current can only flow from one transistor to
5 the next.

6 Q. Even if transistor 2 is off, it
7 receives current?

8 MR. ZANG: Objection. Scope, form.

9 A. So the -- if T2 is off, the current
10 is still going to come out of the source of T1
11 to the drain in T2.

12 Q. Would I be correct in referring to
13 transistor T2 in Okashita's Figure 7 as a
14 shunt?

15 A. Okashita calls that a shunt
16 transistor based on the purpose of the
17 circuits.

18 Q. What is a shunt; what does that
19 mean?

20 MR. ZANG: Objection. Form.

21 A. In this circuit, as Okashita
22 describes, the shunt transistor at times is
23 designed to be on, such that the output node
24 is -- is shunted, connected to ground.

25 Q. Would I be correct in defining shunt

1 S. Thompson

2 to mean a portion of a circuit that provides a
3 direct path to ground?

4 MR. ZANG: Objection. Form.

5 A. It shunts a -- a node to ground. In
6 this case, it's a direct path. In this case,
7 in Okashita, it's a direct path.

8 Q. Is a shunt always connected to
9 ground?

10 MR. ZANG: Objection. Form.

11 A. In Okashita's Figure 7, it's always
12 connected to AC ground.

13 Q. Would I be correct in referring to a
14 circuit feature as a shunt, if it were not
15 connected to ground?

16 MR. ZANG: Objection. Form.

17 A. I would have to look at the circuits
18 you have in mind when you were -- if you wanted
19 me to opine on those cases.

20 Q. Could you turn to page 58 of your
21 declaration, please. It's where you discuss
22 the claim element "thereby forming a
23 source/drain junction capacitance," in ground
24 1.

25 A. On the bottom of 58, I'm at where my

1 S. Thompson

2 report says "thereby forming a source/drain
3 junction capacitance."

4 Q. So it's your opinion that, in
5 Okashita, the source-drain junctions of the
6 transistors do not touch the buried oxide layer
7 and, therefore, a source-drain junction
8 capacitance is formed; is that correct?

9 A. In body-contacted SOI, it's common
10 that the source drains not contacting the BOX,
11 and when that happens, because there is an
12 intervening silicon layer, source-drain
13 capacitance is formed.

14 Q. So it's your opinion that, in
15 Okashita, that capacitance is formed when the
16 source-drain junctions do not touch the buried
17 oxide layer; is that correct?

18 MR. ZANG: Objection. Form.

19 A. The '88 (sic) patent itself teaches
20 that you can have the remaining semiconductor
21 layer under the source-drain that would result
22 in source-drain capacitance, and that is how a
23 POSITA would understand body-contact SOI.

24 MR. MERCADANTE: Objection.

25 Non-responsive. I will repeat the

1 S. Thompson

2 question.

3 Q. It's your opinion that, in Okashita,
4 capacitance is formed when the source-drain
5 junctions do not touch the buried oxide layer;
6 is that correct?

7 MR. ZANG: Objection. Form.

8 A. For Okashita, and this is what the
9 '88 stack also teaches, which I just said, in
10 Figure 9, I have a label source-drain junction
11 of transistor 1, the color red and orange. You
12 see a blue layer separating those junctions
13 from the BOX. They are 22, which is red.

14 So, because of that intervening blue
15 layer, simply the presence of that intervening
16 blue layer in Okashita, causes this device to
17 have source-drain junction capacitance.

18 Q. Does Okashita discuss a source-drain
19 junction capacitance anywhere in its
20 specification?

21 MR. ZANG: Objection. Form.

22 A. It does. In Figure 9, this is
23 body-contacted SOI, and Okashita is drawing the
24 junctions, the source-drain, to not contact the
25 BOX.

1 S. Thompson

2 He does that because he wants to
3 route a ground signal through the blue layer to
4 under the transistor, and so this is a
5 well-known structure. And so, simply drawing
6 this transistor, a POSITA would understand, by
7 the way Figure 9 is drawn, this structure has
8 junction capacitance.

9 Q. Other than the drawing in Figure 9
10 of Okashita, does he discuss anywhere else in
11 the document a source-drain junction
12 capacitance formed by the intervening silicon
13 layer over the buried oxide layer?

14 MR. ZANG: Objection. Form.

15 A. If you look at page 53 of Okashita,
16 in Figure 7 --

17 Q. Hold on. There's only 30 pages of
18 Okashita. Do you mean column?

19 A. No. I mean 53 of my report.

20 Q. Okay, sir.

21 A. Let me know when you're there.

22 Q. I am there.

23 A. So on the top of page 53, I'm
24 showing two figures for the embodiment of
25 Okashita; a circuit view and a cross-sectional

1 S. Thompson

2 view.

3 So, I explained in Figure 9 the
4 cross-section view, Okashita is showing that
5 the junctions don't contact the BOX, but also,
6 from the circuit view, you can see in Figure 7,
7 Okashita wants a blue region of the device
8 layer to be under the device, and you see that
9 because he's routing DC ground to the body
10 terminal of both transistors; and so, for that
11 to be effective to ground the body, you need a
12 blue layer under the transistor to ground that
13 layer.

14 And if the junctions touched the
15 BOX, that blue layer would not be ground to the
16 body; the ground potential would not be ground
17 to the body.

18 Q. Are you able to do any analysis or
19 calculation of how much capacitance would form
20 in Okashita, based on the intervening silicon
21 layer?

22 MR. ZANG: Objection. Form.

23 A. I give some figures for that in the
24 background section. It's going to depend on
25 bias. But there would be biases where you --

1 S. Thompson

2 you would expect the same capacitors to be
3 present in Okashita's device as compared to a
4 bulk transistor.

5 Q. Does the thickness -- I'm talking
6 about Okashita now in Figure 9.

7 Does the thickness of the
8 intervening p-type silicon layer impact the
9 amount of capacitance that would be formed in
10 this circuit?

11 MR. ZANG: Objection. Form.

12 A. It depends on the bias conditions.
13 And so I have that in the background section.

14 If I have the junctions for bias, or
15 very low bias, the thickness doesn't play an
16 important role. If you have very large reverse
17 bias on the junctions, the blue layer thickness
18 can affect the capacitance.

19 But there could be cases in Okashita
20 where the -- at certain bias points, the
21 capacitance would be the same in Okashita
22 versus bulk.

23 Q. Do you recall if Okashita
24 specifically discusses the thickness of the
25 p-type silicon layer 23 in its disclosure?

1 S. Thompson

2 A. I don't recall that, but, as I said,
3 in Figure 7, you can -- it's obvious he needs
4 it to be of a moderate thickness, because he's
5 routing ground under the transistor using the
6 blue layer.

7 Q. Could you please turn to paragraph
8 125 of your declaration?

9 A. I'm here.

10 Q. You say here that: "...it was well
11 known in the art that when an SOI transistor
12 has a silicon layer between the bottom of its
13 source and drain and the top of the buried
14 oxide layer, such structure has larger junction
15 capacitance than the normal SOI structure."

16 Do you see that?

17 A. I do.

18 Q. What is the normal SOI structure?
19 Would that mean a thinner silicon
20 layer?

21 A. No. The normal SOI structure is the
22 type that was in commercial production by IBM,
23 and that's been in production for about ten
24 years.

25 That structure has the source-drain

1 S. Thompson

2 contacting the BOX.

3 Q. If the source-drain junction did not
4 contact the buried oxide layer, but got very,
5 very, very close, would there still be a
6 capacitance --

7 MR. ZANG: Objection. Scope. Form.

8 MR. MERCADANTE: Could you wait for
9 me to finish my question, please?

10 MR. ZANG: Sure.

11 Q. If the source-drain junction did not
12 contact the buried oxide layer, but got very,
13 very close, would there still be a capacitance
14 formed under the source-drain junction?

15 MR. ZANG: Objection. Form. Scope.

16 A. It's going to depend on what you
17 mean by "very, very close." That's not a case
18 I had to consider for this invalidity.

19 Q. So you don't have an opinion on
20 that; is that correct?

21 A. Not without you defining what "very,
22 very close" means.

23 Q. What is deep trench isolation?

24 A. Where are you looking at -- using
25 that word, for context?

1 S. Thompson

2 Q. You can't answer what deep trench
3 isolation is?

4 A. I can, but it depends on context a
5 little bit. Deep trench can apply to a bipolar
6 transistor, so context is important here.

7 Q. In your opinion, is the circuit in
8 Okashita formed using deep trench isolation?

9 MR. ZANG: Objection. Form.

10 A. Is there anywhere in my report where
11 I discussed deep trench associated with
12 Okashita?

13 Q. You talk about trenches. You don't
14 use the phrase "deep trench."

15 I want to know if your opinion is
16 that Okashita shows deep trench isolation?

17 And if you can't answer, or you
18 don't know, that's fine. But that's my
19 question.

20 MR. ZANG: Repeated objection.

21 A. So it depends what context and how
22 you're using the word "deep trench."

23 I don't use that in my report. If
24 you use it in the context where it's normally
25 used, to isolate bipolar transistors, you

1 S. Thompson

2 wouldn't say Okashita has a deep trench
3 isolation in the context of how deep trench is
4 used for bipolar transistors.

5 Q. So you generally wouldn't use the
6 term "deep trench isolation" in the context of
7 MOS transistors; is that correct?

8 MR. ZANG: Objection. Form.

9 A. Again, that's not something I give
10 my opinion on. It depends on what paper you're
11 referring to and what application you're
12 targeting, and what voltage you're targeting.

13 Q. Can you use shallow trench isolation
14 with MOS transistors?

15 MR. ZANG: Objection. Form.

16 A. You certainly can use shallow trench
17 isolation for certain MOS transistors,
18 particularly ones operating around one volt.

19 Q. I'm sorry, you said one volt? You
20 broke up a little bit there?

21 A. One volt.

22 Q. Do the transistors in Okashita
23 operate around one volt?

24 MR. ZANG: Objection. Form.

25 A. Okashita's transistors, at least in

1 S. Thompson

2 column 3, are designed to operate, at least at
3 our voltage, around 3 volts for the gate.

4 MR. MERCADANTE: I'm about to change
5 gears to you. I know we've been going a
6 little bit less than an hour, but I would
7 like to take another five-minute break, and
8 then I think we can power through the rest
9 in the next session, if that's okay with
10 everybody.

11 THE WITNESS: That sounds great.

12 (Whereupon, a recess was taken.)

13 (Exhibit 6, United States Patent
14 Number 6,737,682, Yu, marked for
15 identification.)

16 Q. Dr. Thompson, during the break, I
17 put Exhibit 6 into the chat, which is Exhibit 5
18 to the IPR, which is the Yu Patent 6,737,682.

19 Could you open that up and let me
20 know when you're ready?

21 A. I'm ready.

22 Q. The circuit described in Yu is a Low
23 Voltage Triggering Silicon Controlled
24 Rectifier; is that correct?

25 A. A Low Voltage Triggering

1 S. Thompson

2 Floating-Well Silicon Controlled Rectifier.

3 Q. What is a silicon-controlled
4 rectifier?

5 A. It's a triggering circuit that
6 switches on and off, based on certain
7 conditions.

8 Q. What is a silicon-controlled
9 rectifier generally used for?

10 A. Switching on and off high voltage.

11 Q. And in 2002, when this Yu patent
12 application was filed, were silicon controlled
13 rectifiers generally used for switching on and
14 off high voltage?

15 A. It would depend on the circuit, but
16 it was one option to do that.

17 Q. So Yu discusses a low voltage
18 triggering silicon-controlled rectifier.

19 Am I correct in assuming that the
20 rectifier disclosed in Yu uses a low voltage to
21 trigger the switch of a high voltage?

22 MR. ZANG: Objection. Form.

23 A. The rectifier is designed to trigger
24 at low voltage.

25 Q. Could you please turn to column 1 of

1 S. Thompson

2 Yu. I have some questions about the first few
3 words, which are the "Field of the Invention"
4 of Yu.

5 Let me know when you're there.

6 A. I'm here.

7 Q. So it says: "The invention relates
8 to silicon-on-insulator devices and, more
9 particularly, to a method to form a low voltage
10 triggering, silicon-controlled rectifier SOI
11 device having improved ESD performance."

12 Do you see that?

13 A. Yes.

14 Q. What is ESD performance, or ESD
15 protection?

16 A. It stands for electrostatic
17 discharge, and so it's protecting -- this
18 circuit protects against high voltages.

19 Q. What is it used to protect; more
20 sensitive circuitry?

21 A. Correct.

22 Q. I have some questions about Figure 9
23 of Yu, but, again, like we did previously, I
24 would like to ask them in the context of your
25 declaration, where you provided some -- some

1 S. Thompson

2 coloring. Just give me a moment to get there.

3 Could you please turn to page 96 of
4 your declaration?

5 A. I am here.

6 Q. And do you see on the top of page
7 96, there's an annotated version of Figure 10
8 from Yu?

9 A. Yes.

10 Q. And it's your opinion that the
11 transistors in Yu that are labeled 60 and 65
12 are cascaded; is that correct?

13 A. Correct, 65 and 60 are cascaded
14 transistors.

15 Q. And where is the source-drain
16 junction of transistor 60 on this figure?

17 A. So the second transistor that has
18 the gate 65 has source drains to the right and
19 left of the gate. And the same thing for
20 transistor 60.

21 Q. So my first question -- the question
22 I asked was about transistor 60, so let's start
23 there and let's back it up.

24 So, for transistor 60, it's your
25 opinion that the source-drain junction is what?

1 S. Thompson

2 A. So, for 60, there's junctions on
3 both sides of 60. Those are your source and
4 drain for the transistor.

5 The junction is formed where the
6 source-drain touches the blue, and so the
7 junction is -- is -- is the line where the N+
8 touches the blue or where the -- N+ red touches
9 the blue or where the N+ orange touches the
10 blue.

11 Q. And so your opinion is the same for
12 transistor 65, but it would be the other N+
13 orange; is that correct?

14 The N+ orange labeled 100 and then
15 the N+ red labeled 105?

16 A. Correct. Where 105 and 100 touch
17 the blue, that delineates the region of the
18 source and drain from the well.

19 Q. And you have purple regions that say
20 STI on them, that are labeled 36; is that
21 correct?

22 A. I do.

23 Q. Are those isolation trenches, in
24 your opinion?

25 A. These are shallow trenches that are

1 S. Thompson

2 used for isolation, so I would consider them
3 isolation trenches, yes.

4 Q. And Figure 10 of Yu also shows a
5 cathode and an anode; is that correct?

6 A. It does.

7 Q. Are these the -- across the cathode
8 and the anode, is that the high voltage that
9 the rectifier is switching?

10 A. It can be. The circuit is designed
11 to have the high voltage on the anode side and
12 the low voltage on the cathode side.

13 Q. And could you please turn to
14 paragraph 202 of your declaration, it's on page
15 99?

16 A. Yes.

17 Q. So here you state that -- well, you
18 quote that it's an important feature of Yu
19 "that the doped regions are formed in the upper
20 part of the Wells 42 and 44 and do not extend
21 to the buried oxide layer 32."

22 Do you see that?

23 A. I see that.

24 Q. And then in the next paragraph, 203,
25 you state that: "For the same reasons that the

1 S. Thompson

2 structure of Okashita in ground 1 forms a
3 source/drain junction capacitance, the
4 corresponding structure in this ground, namely
5 the source-drain junctions of transistors 60,
6 65 separated from the BOX layer by the 'thick'
7 silicon layer also forms a source/drain
8 junction capacitance."

9 Do you see that?

10 A. I do see that.

11 Q. There, the word "thick" is in
12 quotes.

13 Do you know where that same from?

14 A. So, if you're looking in paragraph
15 202 of my report, I first start off by making
16 clear that the source drains don't contact the
17 buried oxide layer, and then I go on to explain
18 that is the original source layer in which the
19 doped regions are formed is thick enough so
20 that the doped regions do not completely
21 deplete the wells 42 and 44, so the thickness
22 is in reference to the depletion layer which is
23 forming the capacitance.

24 This is saying that the capacitance
25 is going to be the same value as a bulk wafer

1 S. Thompson

2 because the -- even in the depletion region,
3 that's where the charge is being stored for the
4 capacitor, that depletion layer is not touching
5 the BOX.

6 Q. What does it mean to not completely
7 deplete the wells? In Yu, I'm talking about.

8 A. So, it means you have free carriers
9 remaining in that layer and the properties are
10 to be set by free carriers.

11 Q. And that creates capacitance at the
12 junctions of the transistors; is that correct?

13 MR. ZANG: Objection. Form.

14 A. The free carriers?

15 Q. The lack of complete depletion.

16 MR. ZANG: Repeat objection.

17 A. No. The capacitance is created by
18 having the junction there. The depletion layer
19 is where the charge builds up as you apply
20 voltage.

21 Q. If the wells were completely
22 depleted, would there be a capacitance formed
23 on the junctions?

24 MR. ZANG: Objection. Form.

25 A. In Yu's structure and Okashita's

1 S. Thompson

2 structure, it would, yes.

3 Q. So I'm just talking about Yu.

4 If the wells were completely
5 depleted in Yu, there would still be a
6 capacitance formed on the junctions; is that
7 correct?

8 MR. ZANG: Objection to form.

9 A. So, Yu's wells are not completely
10 depleted, but I'm now coming up with a case in
11 my mind where I can get them completely
12 depleted by using high voltage, very high
13 voltage, outside the spec.

14 Yes, you still would have
15 capacitance.

16 Q. When you say "very high voltage,"
17 what kinds of voltages are you talking about?

18 A. Higher voltage than the transistor
19 was designed to operate, so I can extend the
20 depletion layer farther than Yu envisioned.

21 Q. Could you turn to paragraph 209 of
22 your report, please, it's on page 103?

23 A. Yes.

24 Q. And so it's your opinion that Yu
25 discloses the claim element wherein he said:

1 S. Thompson

2 "At least one of said plurality of cascaded
3 transistors is situated within an isolated
4 island in said device layer."

5 Do you see that?

6 A. Yes.

7 Q. In your opinion, what forms the
8 isolated island in Yu?

9 A. If you look at Figure 12 in my
10 report of Yu, on page 101.

11 Q. I'm there.

12 A. The blue region is the device layer.
13 So that's an isolated island for the device
14 layer where you're seeing two transistors being
15 built.

16 Q. And is that island defined by the
17 STI layers?

18 MR. ZANG: Objection. Form.

19 A. The device layer is silicon, and
20 it's defined by many properties; the thickness
21 of the layer.

22 Laterally, where it ends, going to
23 the right or left or up and down, in this
24 top-down view, that boundary is defined by a
25 shallow trench isolation.

1 S. Thompson

2 Q. So the shallow trench isolation in
3 Yu is what defines the isolated island, in your
4 opinion?

5 MR. ZANG: Repeated objection.

6 A. The shallow trench isolation abuts
7 up against the device layer, and it helps set
8 the boundary for the device layer.

9 Q. Is there anything aside from the
10 shallow trench isolation that defines the
11 isolated island, in your opinion, in Yu?

12 MR. ZANG: Objection. Form.

13 A. If you look at Figure 10, the device
14 layer is bounded by a BOX, a silicon oxide on
15 the bottom, also.

16 Q. And on the left and right of
17 Figure 10, it's bounded by the shallow trench
18 isolation, right?

19 A. Correct.

20 Q. And -- but this is only a
21 cross-section. So if we were looking at
22 Figure 10 from the top down, would the shallow
23 trench isolation region go all the way around
24 the boundary of what you claim is the isolated
25 island?

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2 MR. ZANG: Objection. Form.

3 A. The shallow trench isolation would
4 be on -- if I have a cross-section cut in the
5 opposite direction, you would see a shallow
6 trench isolation on the other side of the
7 device layer, correct.

8 Q. By "the other side," you mean the
9 left and right of a cross-section taken in the
10 other direction; is that correct?

11 MR. ZANG: Objection. Form.

12 A. I mean, if I take a cross-section of
13 Figure 12, vertically, the one we've been
14 looking at this horizontal; if you take a
15 cross-section of Figure 12, vertically, the
16 ends of that cross-section would have shallow
17 trench isolation.

18 Q. Okay. That's what I was confused
19 about.

20 (Exhibit 7, United States Patent
21 Number 2006/0270367 A1, Burgener, marked
22 for identification.)

23 Q. I've put Exhibit 7 in the chat,
24 which is Burgener. I believe it's Exhibit 1006
25 to the IPR. Let me know when you have Burgener

1 S. Thompson

2 open.

3 A. I have Burgener open.

4 Q. Burgener talks about an RF Front End
5 With Stacked Transistor Switch.

6 Is that correct?

7 A. That is correct.

8 Q. What is an RF front end?

9 A. It's circuits for radio frequency
10 for radio.

11 Q. Could you please turn to paragraph
12 106 of Burgener?

13 A. Yes.

14 Q. So, in this section, he's talking
15 about preferred fabrication techniques for his
16 circuit. Would you agree with me?

17 A. In 105 and 106, he's talking -- one
18 of the -- one of the topics he's talking about
19 is how the device would be fabricated.

20 Q. In the very last sentence of 106, he
21 says: "Using other manufacturing techniques,
22 or lower voltages and impedances, a need for
23 cascode or multiply-stacked FETs may be
24 avoidable." Do you see that?

25 A. I do see that.

1 S. Thompson

2 Q. So there's that term that we were
3 talking about earlier, "cascode."

4 Do you know what he's talking about
5 in this section of Burgener, in "avoiding
6 cascode or multiply-stacked FETs"?

7 MR. ZANG: Objection. Scope. Form.

8 A. This is not something I've opined on
9 in my report.

10 Q. Okay. And in the previous
11 paragraph, 105, he discusses a fabrication
12 technique called silicon on sapphire.

13 Do you see that?

14 A. I see that.

15 Q. What is silicon on sapphire? Are
16 you familiar with that technology?

17 A. I am. So in 105, the paragraph
18 talks about other silicon on -- on insulator
19 techniques may be used, as other SOI techniques
20 may be used.

21 And so, he's open to the idea that
22 this could be fabricated on the traditional
23 silicon on insulator, where the insulator is
24 silicon dioxide or where the insulator is
25 sapphire.

1 S. Thompson

2 Q. So, we'll get to that part. I
3 wanted to talk first about silicon on sapphire
4 and what it is.

5 Is silicon on sapphire just an SOI
6 technology where the insulator is sapphire?

7 MR. ZANG: Objection. Form.

8 A. One aspect of SOI is you're
9 replacing the insulator from silicon dioxide to
10 the material sapphire.

11 Q. Okay. And, cost-wise, how does
12 silicon on sapphire compare to another
13 silicon-on-insulator technology, like silicon
14 dioxide?

15 A. It comes down to, again, the --

16 Q. And I'm just talking about the cost
17 of the material, not the circuit that ends up
18 being constructed using that material.

19 A. Thank you.

20 So, generally, the cost of silicon
21 on sapphire is a more expensive technology.

22 Q. Okay. And Burgener does say that
23 you could use other manufacturing techniques,
24 other types of semiconductor on insulator,
25 correct, aside from silicon on sapphire?

1 S. Thompson

2 A. Correct.

3 Q. And he specifically says that you
4 could use these other techniques "for at least
5 some frequency bands and power levels."

6 Do you see that?

7 A. I do.

8 Q. Does he talk about what frequency
9 bands or power levels would be susceptible to
10 construction using other SOI technologies aside
11 from silicon on sapphire?

12 A. Well, it's going to depend on your
13 commercial performance targets.

14 Q. Since it's more expensive, is
15 silicon on sapphire generally higher
16 performing?

17 MR. ZANG: Objection. Form.

18 Q. Than silicon dioxide?

19 MR. ZANG: Objection. Form.

20 A. It -- it may not be. It depends on
21 a number of parameters.

22 Q. What does it depend on?

23 A. The quality of the transistor
24 fabricated in the device layer. It depends on
25 the X, Y, Z leakage in the device layer, as

1 S. Thompson

2 defined by Okashita's Figure 6. It depends on
3 your techniques for getting heat out of the
4 device.

5 One of the reasons sapphire is used,
6 it helps get the heat out of the devices a
7 little better than silicon dioxide.

8 Q. There is an attorney representing
9 NXP here, Mr. Wu, and earlier there was another
10 attorney representing NXP, Mr. Green.

11 Have you spoken or corresponded with
12 either of these attorneys, ever?

13 A. No.

14 Q. Have you been retained by NXP for
15 anything related to the '886 patent?

16 A. No.

17 Q. Have you had any conversations with
18 NXP, or any attorneys representing NXP,
19 relating to the '886 patent?

20 A. No.

21 MR. MERCADANTE: I have no further
22 questions for this proceeding, subject to
23 any redirect by your attorney.

24 MR. ZANG: Can we request for a
25 five-minute break?

1 S. Thompson

2 MR. MERCADANTE: Of course.

3 MR. ZANG: Thank you.

4 (Whereupon, a recess was taken.)

5 MR. ZANG: Counsel for petitioner
6 has no questions.

7 MR. MERCADANTE: Okay. So, I don't
8 think we need to designate the transcript
9 confidential. I think that my transistor
10 drawings are public, and everything else we
11 talked about is public; so I think we can
12 close -- you want to close this deposition
13 and we'll restart a new transcript for the
14 next one?

15 MR. ZANG: Sounds good to us.

16 And I just want to let you know, I
17 think last week Rich -- we told Rich that
18 we don't care whether you want to repeat
19 the initial questions; so it's up to you if
20 you want to repeat all the intro questions
21 today or not.

22 MR. MERCADANTE: Okay. We'll talk
23 about that when we get on the new
24 transcript.

25 (Time Noted: 11:39 a.m.)

DECLARATION

I HEREBY CERTIFY that having been
first duly sworn to testify to the truth, I
gave the above testimony.

I FURTHER CERTIFY that the foregoing
transcript is a true and correct transcript
of the testimony given by me at the time
and place specified hereinbefore.

SCOTT E. THOMPSON, Ph.D.

Subscribed and sworn to before me
this_____day of_____20_____.

NOTARY PUBLIC

CERTIFICATE

STATE OF NEW YORK)

: ss

COUNTY OF BRONX)

I, ROBERTA CAIOLA, a Certified
Shorthand Reporter, do hereby certify:

That SCOTT E. THOMPSON, Ph.D., the
witness whose deposition is hereinbefore set
forth, was duly sworn by me and that such
deposition is a true record of the testimony
given by the witness.

I further certify that I am not
related to any of the parties to this action by
blood or marriage, and that I am in no way
interested in the outcome of this matter.

IN WITNESS WHEREOF, I have hereunto
set my hand on June 18, 2025.

Roberta Caiola

ROBERTA CAIOLA

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ERRATA SHEET

CASE NAME: SAMSUNG vs. HARBOR

DATE OF DEPOSITION: June 17, 2025

WITNESS: SCOTT E. THOMPSON, Ph.D.

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Subscribed and sworn to before me

this ____ day of _____, 20____.

Notary Public

Commission Expires

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