

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

SAMSUNG ELECTRONICS CO., LTD. AND  
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioners,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Patent No. 7,745,886

Filing Date: September 29, 2008

Issue Date: June 29, 2010

Inventors: Robert L. Zwingman and Marco Racanelli

Title: SEMICONDUCTOR ON INSULATOR (SOI) SWITCHING CIRCUIT

---

**DECLARATION OF MR. JOHN BERG**

Case No. IPR2024-01402

---

**TABLE OF CONTENTS**

|                                                                                       | <b>Page(s)</b> |
|---------------------------------------------------------------------------------------|----------------|
| I. INTRODUCTION .....                                                                 | 1              |
| II. BACKGROUND AND QUALIFICATIONS .....                                               | 1              |
| III. COMPENSATION .....                                                               | 3              |
| IV. LEGAL PRINCIPLES .....                                                            | 3              |
| A. Claim Construction .....                                                           | 3              |
| B. Anticipation .....                                                                 | 6              |
| C. Obviousness .....                                                                  | 7              |
| V. LEVEL OF ORDINARY SKILL IN THE ART .....                                           | 7              |
| VI. THE '886 PATENT .....                                                             | 9              |
| VII. THE ALLEGED PRIOR ART .....                                                      | 12             |
| A. Okashita .....                                                                     | 12             |
| B. Yu .....                                                                           | 13             |
| C. Burgener .....                                                                     | 15             |
| VIII. CLAIM CONSTRUCTION .....                                                        | 17             |
| IX. CLAIMS 3 AND 8-19 ARE NOT UNPATENTABLE .....                                      | 17             |
| A. Ground 1: Okashita .....                                                           | 18             |
| B. Ground 2: Okashita Does Not Render Claim 3 Obvious .....                           | 18             |
| C. Ground 3: Okashita in Combination with Yu Does Not<br>Render Claim 3 Obvious ..... | 19             |

|     |                                                                                                                                                                                                               |    |
|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| 1.  | The Person of Ordinary Skill in the Art Would Not Have Been Motivated to Combine Yu and Okashita with a Reasonable Expectation of Success .....                                                               | 19 |
| D.  | Ground 4: Yu Does Not Anticipate Any Claim .....                                                                                                                                                              | 23 |
| 1.  | Yu Does Not Disclose “each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance” ..... | 24 |
| E.  | Ground 5: Burgener in Combination with Okashita Does Not Render Obvious Any Challenged Claim.....                                                                                                             | 27 |
| 1.  | There is No Motivation to Combine Burgener and Okashita .....                                                                                                                                                 | 27 |
| 2.  | The Combination of <i>Burgener</i> and <i>Okashita</i> Does Not Teach the Required Electrical Isolation of Claim 3.....                                                                                       | 33 |
| F.  | Ground 6 (Burgener in Combination with Okashita and Yu) Fails .....                                                                                                                                           | 33 |
| 1.  | There is No Motivation to Combine Burgener, Okashita, and Yu.....                                                                                                                                             | 33 |
| X.  | MATERIALS CONSIDERED .....                                                                                                                                                                                    | 35 |
| XI. | CONCLUSION.....                                                                                                                                                                                               | 35 |

## **I. INTRODUCTION**

1. I am over eighteen years of age and I would be competent to testify as to the matters set forth herein if I am called upon to do so.

2. I have been retained by Fabricant LLP, counsel for the Patent Owner Harbor Island Dynamic LLC to review U.S. Patent No. 7,745,886 (“the ’886 Patent”) entitled SEMICONDUCTOR ON INSULATOR (SOI) SWITCHING CIRCUIT, and to provide my technical review, analysis, insights, and opinions regarding the ’886 Patent in view of the prior art cited by Petitioners Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, “Samsung” or “Petitioner”). I submit this Declaration in support of Patent Owner’s Response in this IPR proceeding. I have personal knowledge of the matters stated herein and would be competent to testify to them if required.

## **II. BACKGROUND AND QUALIFICATIONS**

3. I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below.

4. This section summarizes my career history, education, publications, and other relevant qualifications. My full *curriculum vitae* (“CV”) is included as **Appendix A**.

5. I obtained a Bachelor of Science degree in Physics from the

Massachusetts Institute of Technology in 1980, and now I am focusing on analog CMOS circuit design, simulation, modeling, and processing.

6. I am currently an expert consultant in semiconductor design and manufacturing. Since 2010, I have performed this work as a Principal at Berg-Attenborough, Inc., a consulting firm that provides technical consulting and expert witness services to semiconductor companies and law firms. My work as an expert consultant has included developing advanced CMOS processes and multi-chip modules that incorporate logic circuits using SOI, memory devices such as dynamic random-access memory (“DRAM”), and flash memory, as well as performing device analysis and testing using scanning electron microscope (“SEM”) and transmission electron microscopy (“TEM”) technology. In addition to my work as an expert consultant, I have over 35 years of experience as an executive and as an engineer in the semiconductor industry.

7. As the Chief Technologist at American Semiconductor, I developed and designed CMOS sensors and systems built using bonded wafers and multi-chip modules using 45nm double-gate FET technology. Before joining ASI, I developed automated tools for the nano-imprint industry at Transfer Devices.

8. Prior to Transfer Devices, I was a Managing Director at Cypress Semiconductor, where I managed a business unit that designed five new

programmable logic chip product families in five years. Prior to Cypress, I was Vice President of Technology Development at Zilog, where I managed both technology development and design teams that built the company's 200mm wafer fabrication facility, designed Z8 microcontrollers, and engineered scaling of CMOS and embedded CMOS non-volatile memory technologies from 2um to 0.25um - the latter of which required co-development of CMP tools with the tool supplier.

9. In forming my opinions, I rely on my knowledge and experience in the fields relevant to this Declaration. I further rely on documents and information referenced in this Declaration.

### **III. COMPENSATION**

10. My compensation for time worked on this proceeding is not dependent on any issues related to the '886 Patent, the outcome of this proceeding, or the substance of my opinions. My compensation for time worked on this proceeding is at my customary rate of \$560 per hour. I have no financial interest in, or affiliation with, the Patent Owner or any of the real parties in interest.

### **IV. LEGAL PRINCIPLES**

#### **A. Claim Construction**

11. I understand that claim terms should be given their ordinary and customary meaning within the context of the patent in which the terms are used, i.e.,

the meaning that the term would have to a person of ordinary skill in the art (“POSITA”) in question at the time of the invention in light of what the patent teaches, unless it appears that the inventors were using them to mean something else. Additionally, the specification and prosecution history must be consulted to confirm whether the patentee has acted as his/her own lexicographer (i.e., provided special meaning to any disputed terms), or intentionally disclaimed, disavowed, or surrendered any claim scope).

12. I understand that a POSITA is deemed to read a claim term not only in the context of the particular claim in which the disputed term appears, but also in the context of the entire patent, including the specification and the prosecution history. The prosecution file history provides evidence of how both the Patent Office and the inventors understood the terms of the patent, particularly in light of what was known in the prior art. Further, where the specification describes a claim term broadly, arguments and amendments made during prosecution may require a narrower interpretation. For these reasons, the words of the claim must be interpreted in view of, and be consistent with, the entire specification. The specification is the primary basis for construing the claims and provides a safeguard such that correct constructions closely align with the specification. Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of

what the inventors actually invented and intended to envelop with the claims as set forth in the patent itself.

13. I understand that, to determine how a POSITA would have understood a claim term, one should look to those sources available that show what a POSITA would have understood disputed claim language to mean. Such sources include the words of the claims themselves, the remainder of the patent's specification, the prosecution history of the patent (all considered "intrinsic" evidence), and "extrinsic" evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art. I understand that one looks primarily to the intrinsic patent evidence, but extrinsic evidence may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient.

14. Additionally, the context in which a term is used in the Asserted Claim can be highly instructive. Likewise, other claims of the patent in question, both asserted and not asserted, can inform the meaning of a claim term. For example, because claim terms are normally used consistently throughout the patent, the usage of a term in one claim can often illuminate the meaning of the same term in other claims. Differences among claims can also be a useful guide in understanding the meaning of particular claim terms.

15. I understand that, while intrinsic evidence is of primary importance,

extrinsic evidence, e.g., all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises, can also be considered. For example, technical dictionaries may help one better understand the underlying technology and the way in which one of skill in the art might use the claim terms. Extrinsic evidence should not be considered, however, divorced from the context of the intrinsic evidence. Evidence beyond the patent specification, prosecution history, and other claims in the patent should not be relied upon unless the claim language is ambiguous in light of these intrinsic sources. Furthermore, while extrinsic evidence can shed useful light on the relevant art, I understand that it is less significant than the intrinsic record in determining the legally operative meaning of claim language.

**B. Anticipation**

16. I understand that to anticipate a claim, a prior art reference must disclose all elements of the claim within the four corners of the document, and it must disclose those elements arranged as in the claim. I understand that a reference may anticipate even if it does not expressly disclose all the elements if a POSITA reading the reference would at once envisage the claimed arrangement or combination.

17. I understand that if a reference fails to disclose even one element, it

does not anticipate that claim. I understand that references that must be modified to disclose a claim element do not anticipate that claim.

**C. Obviousness**

18. I understand that a patent claim is unpatentable as “obvious” if the subject matter of the claim as a whole would have been obvious to a POSITA as of the time of the invention at issue.

19. I understand that the question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) so-called secondary considerations where in evidence.

20. I further understand that the question is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious.

**V. LEVEL OF ORDINARY SKILL IN THE ART**

21. It is my understanding that I must address the issues set forth in this Declaration, from the viewpoint of a POSITA at the time of the invention to which the Asserted Patent pertains.

22. I understand that this hypothetical POSITA is considered to have the normal skills of a person in a certain technical field. I understand that factors that

may be considered in determining the level of ordinary skill in the art include: (1) the education level of the inventor; (2) the types of problems encountered in the art; (3) the prior art solutions to those problems; (4) rapidity with which innovations are made; (5) the sophistication of the technology; and (6) the education level of active workers in the field.

23. Considering the above factors, in my opinion, a POSITA would have (1) a Bachelor of Science degree or equivalent degree in electrical engineering, physics, materials science, or a similar field; and (2) at least two years of industry experience in semiconductor design and/or fabrication. I also agree that a person could also have qualified as a POSITA with some combination of (1) more formal education (such as Master of Science degrees) and less technical experience, or (2) less formal education and more technical or professional experience in the fields listed above.

24. I understand that Dr. Thompson has opined that a POSITA would have at least a master's degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems. Ex. 1002, ¶ 106. While our contentions are similar, I disagree that a master's degree represents the ordinary level of skill. The '886 Patent is directed to an audience of engineers working to design switching circuits using Semiconductor on Insulator. In the industry, it is

typical for such engineers to have a bachelor's degree. I myself supervised and managed a design team that implement such designs, with a bachelor's degree.

25. I understand that the '886 Patent is entitled to a December 10, 2007, priority date, and that is the relevant time period from which a POSITA would evaluate its disclosure and any prior art.

26. My qualifications and experience exceed those of a POSITA, under both my and Dr. Thompson's opinions. Nonetheless, my analysis and opinions herein regarding the Asserted Patent are given from the perspective of a POSITA.

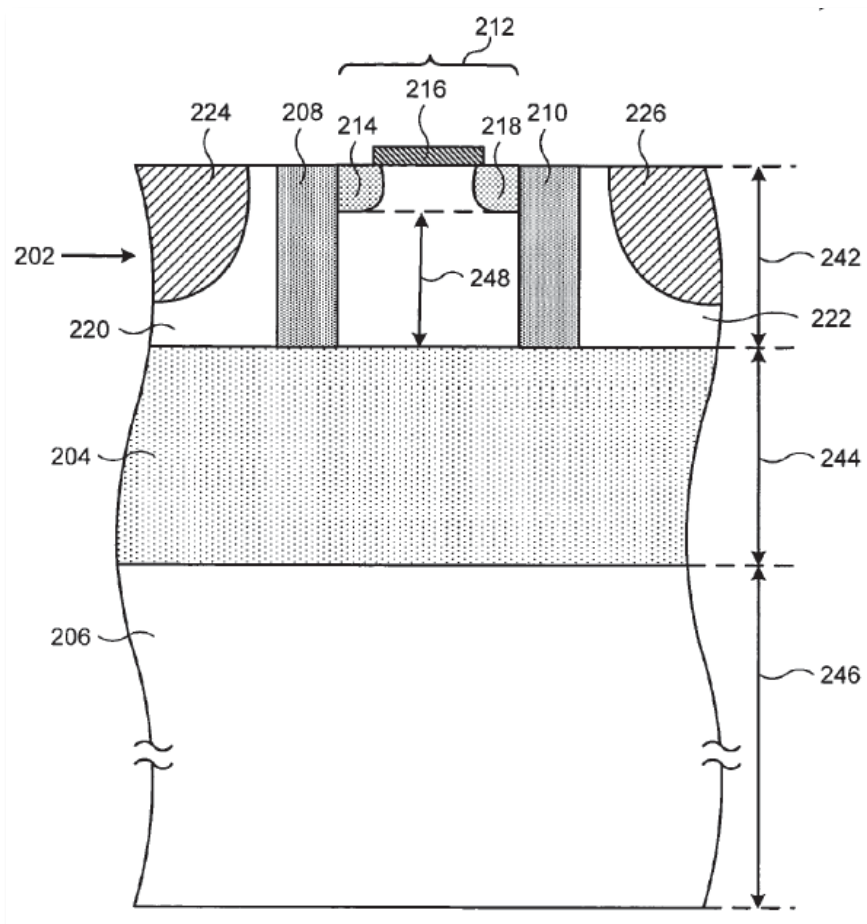
## **VI. THE '886 PATENT**

27. U.S. Patent No. 7,745,886 (Ex. 1001, the "'886 Patent") is titled "Semiconductor on Insulator (SOI) Switching Circuit" and issued on June 29, 2010. The '886 Patent names two inventors, Robert L. Zwingman and Marco Racanelli, and was filed by and issued to Newport Fab, LLC, a subsidiary of Tower Semiconductor, Inc., which manufactures semiconductor wafers in Newport Beach, California.

28. The '886 Patent describes and claims an improvement in switching circuitry that includes a number of transistors built using silicon on insulator, or SOI, technology. '886 Patent, Abstract. According to the '886 Patent, "it is difficult to electrically isolate semiconductor structures fabricated on a conventional bulk

silicon wafer” because electric current can flow under trenches. *Id.*, 1:29-36. This can be partially solved using silicon-on-insulator technology, but “circuits designed for fabrication in a bulk silicon wafer must be redesigned for fabrication in a conventional silicon on insulator wafer, which significantly increases manufacturing and integration complexity and cost.” *Id.*, 1:43-47.

29. An embodiment of the invention of the '886 Patent is shown in Figure 2, below:



'886 Patent, Fig. 2. According to the '886 Patent, Figure 2 shows a SOI cross section, where a device layer 202 sits atop a buried oxide layer 204 that acts as an insulator, which sits atop a conventional bulk semiconductor layer 206. *Id.* 3:49-67. Each of these three layers is made much thicker than in typical silicon devices. *Id.*, 3:49-4:3. A transistor 212 is built in the device layer, and “[b]ecause of the increased thickness of device layer 202, source 214 and drain 218 do not extend all the way through device layer 202 to contact the top surface of buried oxide layer 204.” *Id.* 4:8-11. The source/drain junctions of the transistor have capacitances, and these capacitances “behave similarly to the junction capacitances of a transistor implemented in a conventional bulk silicon wafer, instead of a conventional SOI wafer, in part because of the greater thickness of device layer 202 compared to the thickness of conventional device layer 102.” *Id.* 4:19-24.

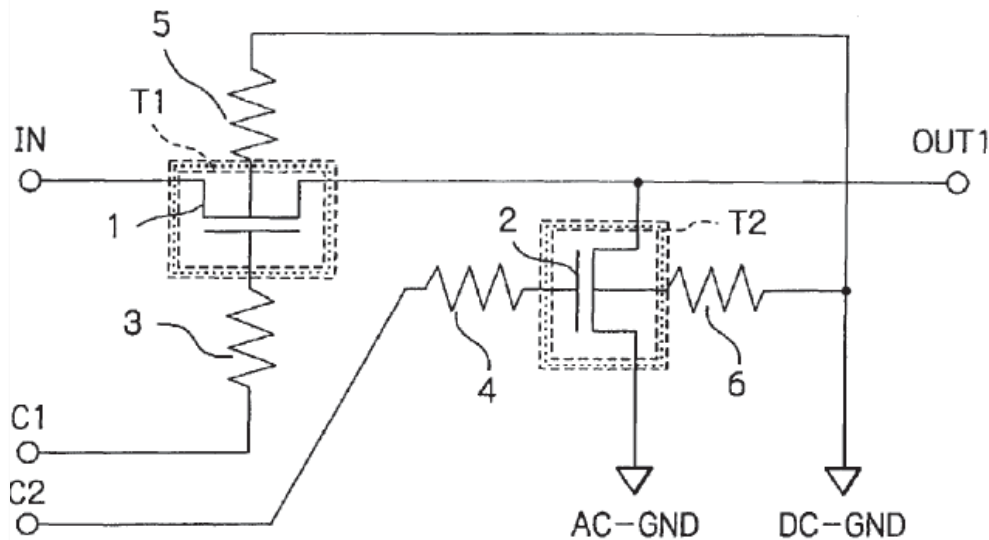
30. The '886 Patent provides several advantages, including that the thick layers aid in implementing high performance circuits, and that “[a]n engineer using design methodologies suitable for conventional bulk semiconductor devices and circuits, without using specialized design techniques or device models required for conventional SOI technology, can readily design and implement high performance circuits utilizing various embodiments of the invention’s SOI transistors and other SOI structures.” *Id.*, 8:22-31.

## **VII. THE ALLEGED PRIOR ART**

### **A. Okashita**

31. U.S. Patent No. 6,836,172 to Okashita issued on December 28, 2004 and is titled “Semiconductor Switch Apparatus Including Isolated MOS Transistors.” Okashita describes a semiconductor switch apparatus that includes “at least one shunt MOS transistor connected between one of the input terminal and the output terminal and the AC ground terminal.” Ex. 1004, Abstract. Okashita describes that prior art semiconductor switches using Gallium-Arsenide have a high resistance, and thus the leakage of radio signals via the substrate can be suppressed, but GaAs substrates are very expensive. *Id.*, 1:16-28. Okashita describes a system including a series MOS transistor T1 and a shunt MOS transistor 2, shown below in Figure 7:

*Fig. 7*

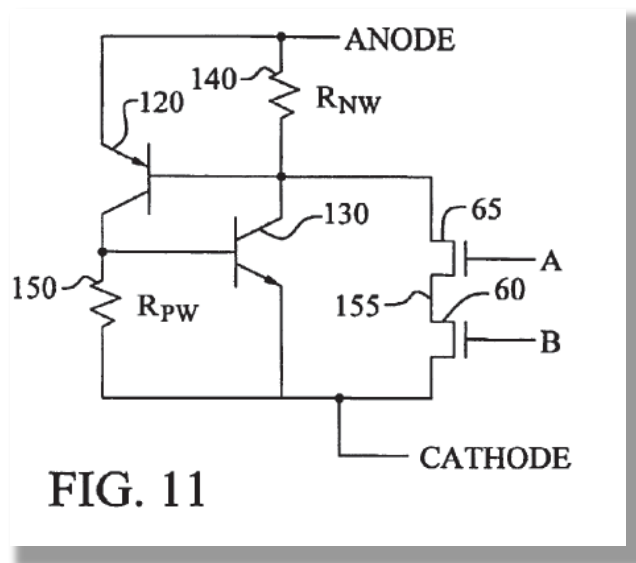


Ex. 1004, Fig. 7. According to *Okashita*, “a resistor 5 is connected between the back gate of the MOS transistor 1 and the DC ground terminal DC-GND of FIG. 3, and a resistor 6 is connected between the back gate of the MOS transistor 2 and the DC ground terminal DC-GND of FIG. 3.” *Id.*, 5:21-27.

## B. Yu

32. U.S. Patent No. 6,737,682 to Ta-Lee Yu issued on May 18, 2004 and is titled “High Voltage Tolerant and Low Voltage Triggering Floating-Well Silicon Controlled Rectifier On Silicon-On-Insulator For Input Or Output.” Yu discloses a particular type of thyristor, called a low voltage triggering, silicon-controlled

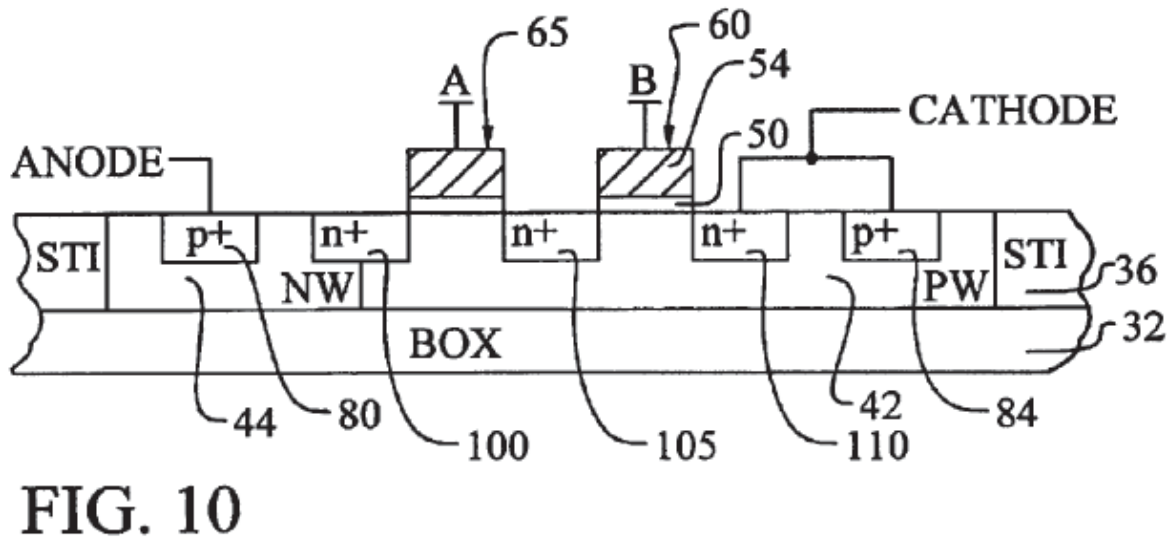
rectifier. Ex. 1005, 1:10-14. As recognized by Yu, these circuits are typically used for ESD (electrostatic discharge) protection. *Id.* 1:24-27. Figure 11 of Yu discloses the circuitry of the silicon-controlled rectifier in Yu, which includes a single cathode and anode, as well as two MOS transistors with control inputs A and B:



Ex. 1005, FIG. 11.

33. Yu describes that, during an ESD event, the devices 60 and 65 “operate due to the bipolar effect taking place between the source of the bottom NMOS device 60 and the drain of the top NMOS device 65,” and that the silicon-controlled rectifier is “triggered by the current generated when the stacked NMOS devices 60 and 65 enter avalanche breakdown.” *Id.* 6:40-45.

34. Yu also discloses a cross section of this circuit, shown in Figure 10:



Ex. 1005, FIG. 10.

35. Disclosed is a N-well 44 in which the anode is formed, and a P-well 42 in which the cathode is formed. *Id.*, 5:28-42. The N+ well 100 that forms the source of transistor 65 is located partly in the N-well 44 and partly in the P-well 42. *Id.*, 5:36-37.

### C. Burgener

36. U.S. Patent Application Publication No. US 2006/0270367 was published on November 30, 2006 and is titled “Integrated RF Front End With Stacked Transistor Switch.” Burgener discloses an “integrated circuit (IC)” that includes “all RF front end or transceiver elements for a portable communication

device,” such as a cellular telephone and other wireless communications device. Ex. 1006, Abstract, ¶ [0006]. The RF front end may be implemented by stacks of multiple Field Effect Transistors (FETs) connected in series to operate as a switching device. *Id.*, Abstract, ¶ [0009].

37. Burgener discloses an “antenna switch 1700” that directs input signals from an antenna to amplifiers, and output signals from the power amplifiers to the antenna, shown in Figure 17:

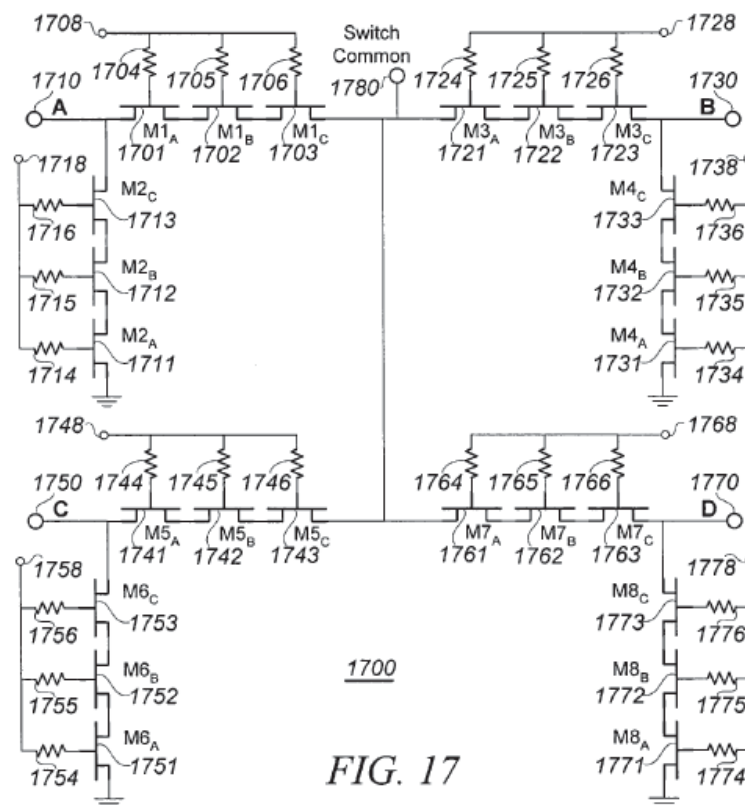


FIG. 17

Ex. 1006, FIG. 17. *Burgener* states “FIG. 17 is a simplified schematic of exemplary circuitry 1700 for an antenna switch. Further details regarding design and fabrication of such an RF switch may be found in U.S. Pat. No. 6,804,502, issued Oct 12, 2004 and entitled ‘Switch Circuit and Method of Switching Radio Frequency Signals.’” *Id.*, ¶ [0101]. U.S. Patent No. 6,804,502 (Ex. 2004, “*Burgener II*”) states that the transistors in the RF switch can be made using ultra-thin silicon-on-sapphire technology, which eliminates the need for “[t]raditional transistor isolation wells” that are used for thick silicon. Ex. 2004, 10:66-11:1.

#### **VIII. CLAIM CONSTRUCTION**

38. I have been instructed by counsel to apply the plain and ordinary meaning of all claim terms.

#### **IX. CLAIMS 3 and 8-19 ARE NOT UNPATENTABLE**

39. I have been instructed by counsel that Patent Owner will seek to cancel Claims 1-2 and 4-7 of the '886 Patent and, thus, I have considered their ultimate validity only with respect to Ground 4, where my opinion is that Yu does not anticipate any challenged claim.

**A. Ground 1: Okashita**

40. I have been instructed by counsel not to consider Ground 1, as it only relates to claims that Patent Owner will seek to cancel.

**B. Ground 2: Okashita Does Not Render Claim 3 Obvious**

41. I have been instructed not to consider Claims 1-2 and 4-7 of Ground 2.

42. Claim 3 of the '886 Patent requires the entire plurality of cascaded transistors to be located within an isolated island, whereas Claim 2 requires each transistor to be in its own isolated island. Dr. Thompson claims that Okashita anticipates Claim 2 because it shows each transistor in its own isolated island, but renders obvious Claim 3 with a modification. Ex. 1002, ¶¶ 140-141; 167-168.

43. I disagree with Dr. Thompson that Okashita renders Claim 3 obvious.

44. Dr. Thompson states that “a POSITA would have recognized that situating both MOS transistors 1, 1' within the same isolated island, as *Okashita* teaches, ensures consistent performance characteristics among the transistors.” Ex. 1002, ¶ 168. Dr. Thompson states that this would provide two benefits: better tracking of thermal temperature and consistent switching rate. *Id.*

45. I disagree with Dr. Thompson that Okashita provides the POSITA with a motivation to modify the isolated islands that isolate each transistor 1, 1' to place both the transistors in the same isolated island. *Okashita* specifically teaches that

“each of the MOS transistors 1, 1’, 2 and 2’ is isolated by the trench insulating layers T1 and T2, so that the leakage of radio frequency signals from the silicon layer 23 of the MOS transistor 1 *to that of the MOS transistor 1’*. . . can be sufficiently suppressed.” Ex. 1004, 8:47-54. (emphasis added).

46. In my opinion, since Okashita teaches the need to suppress leakage of radio signals between MOS transistor 1 and MOS transistor 1’, the POSITA would not have been motivated to remove the isolation trenches between these two transistors, as claimed by Dr. Thompson, merely to ensure more consistent performance.

**C. Ground 3: Okashita in Combination with Yu Does Not Render Claim 3 Obvious**

**1. The Person of Ordinary Skill in the Art Would Not Have Been Motivated to Combine Yu and Okashita with a Reasonable Expectation of Success**

47. I disagree with Dr. Thompson that the POSITA would have been motivated to combine Yu and Okashita, because Yu and Okashita are very different. Yu describes a silicon-controlled rectifier that is used to switch very high voltages. Ex. 1005, Abstract. The field of endeavor in Yu is specifically limited to “a method to form a low voltage triggering, silicon-controlled rectifier (SCR) SOI device having improved ESD performance.” *Id.* 1:10-13. ESD refers to electrostatic discharge.

48. Okashita, on the other hand, relates to “a semiconductor switch apparatus for radio frequency signals.” Ex. 1004, 1:7-8. Okashita discloses a switching circuit that works between, at most, -3V and 3V. *Id.* at 7:18-29. In fact, Okashita repeatedly refers to 3 volts as a high voltage. *Id.* at 3:11, 3:40.

49. Dr. Thompson does not account for these meaningful differences in use cases, merely stating that “a POSITA would have found it obvious to fabricate *Okashita*’s transistors using an SOI process, as *Yu* teaches, so the transistors would have been within the active area that is surrounded by a trench isolation region.” Ex. 1002, ¶ 178. Dr. Thompson goes on to state that silicon dioxide has lower thermal conductivity than silicon, so if the source/drain junctions of *Okashita* were to contact the silicon oxide layer, the transistors would operate at higher temperatures, which could negatively impact circuit performance. *Id.* ¶ 179.

50. The problems described by Okashita include:

In a mobile communication apparatus such as a mobile telephone apparatus using radio frequency signals such as GHz microwave signals, semiconductor switch apparatuses are used for switching the operation of an antenna circuit and a receiving and transmitting circuit.

A prior art semiconductor switch apparatus using GaAs FETs is very simple and therefore, can be constructed by one semiconductor chip. That is, since the GaAs FETs serve as passive elements such as resistors and capacitors, bias circuits for the GaAs FETs are unnecessary. Also, since a substrate of the GaAs FETs is made of semi-

insulating material having a high resistance, the leakage of radio frequency signals via the substrate can be suppressed. This will be explained later in detail.

In the above-described prior art semiconductor switch apparatus using GaAs FETs, however, since GaAs substrates are expensive, the manufacturing cost is very high.

In another prior art semiconductor switch apparatus using silicon MOS transistors, in order to suppress the leakage of radio frequency signals, a silicon-on-insulator (SOI) configuration is adopted (see: JP-A-2000-294786) or a resistor is inserted between the back gate of each of the MOS transistors and a ground terminal (see: U.S. Pat. No. 6,094,088). This also will be explained later in detail.

In the above-described prior art semiconductor switch apparatus using silicon MOS transistors, although the manufacturing cost can be low, suppression of the leakage of radio frequency signals is still insufficient, which also will be explained later in detail.

Ex. 1004, 1:11-40.

51. Meanwhile, Yu is concerned entirely with ESD protection and heat transfer for SOI devices:

The SCR and LVT-SCR devices of the prior present several difficulties in integration with a SOI process. In an SOI process, the devices must be formed in a relatively thin silicon layer overlying a buried insulator layer. This buried insulator layer, in turn, overlies the bulk substrate. The presence of the buried insulator layer improves MOS transistor performance, especially for very short channel devices, and reduces substrate coupling issues by

providing excellent device-to-device isolation. Typically, the STI regions are formed down to the buried insulator layer such that each active area is completely isolated from other active areas.

However, these characteristics cause several problems for SCR devices formed in an SOI process having STI isolation. First, the presence of the STI regions within the SCR and LVT-SCR devices reduces the lateral heat transfer property during an ESD event. Consequently, the devices fail at a lower energy dissipation level. Second, the STI pull-down impacts both low-current and high-current characteristics and influences the diode leakage characteristics. Third, the thickness of the silicon layer overlying the buried insulator can restrict the formation of the SCR device. If the silicon layer is relatively thin, then the heavily doped (n<sup>+</sup> and p<sup>+</sup>) regions will extend down to the buried insulator layer. In this case, the traditional SCR and LVT-SCR design will not work because the bipolar devices will not function.

Ex. 1005, 1:59-2:17.

52. These fields of art and pertinent problems not only have nothing to do with one another, they also have nothing to do with the problem solved by the '886 Patent. The '886 Patent relates to intentionally increasing the capacitance of structures built using SOI to mimic the characteristics of circuits designed to be built using bulk silicon, so that circuits designed for fabrication using bulk silicon do not need to be redesigned for use in SOI. '886 Patent, 1:37-50; 3:21-48.

53. I disagree that the POSITA would have been motivated to combine

Okashita and Yu with a reasonable expectation of success, for several reasons. First, the POSITA looking to modify the SOI process in Okashita would not have looked to Yu for that modification because Okashita is a low voltage wireless switching circuit and Yu discloses a high voltage silicon-controlled rectifier that is outside of that field of endeavor. Second, Okashita already provides teachings for an SOI process for a switching apparatus, and therefore there would be no motivation to look to a completely different process in Yu that solves a different problem and is designed to operate at very different voltages. Third, with respect to Claim 3, the POSITA would not have been motivated to look to Yu, which does not isolate the individual transistors from one another, as Okashita specifically teaches that “each of the MOS transistors 1, 1’, 2 and 2’ is isolated by the trench insulating layers T1 and T2, so that the leakage of radio frequency signals from the silicon layer 23 of the MOS transistor 1 *to that of the MOS transistor 1’*. . . can be sufficiently suppressed.” Ex. 1004, 8:47-54. (emphasis added).

54. Therefore, it is my opinion that the POSITA would not have been motivated to combine Okashita and Yu with a reasonable expectation of success.

**D. Ground 4: Yu Does Not Anticipate Any Claim**

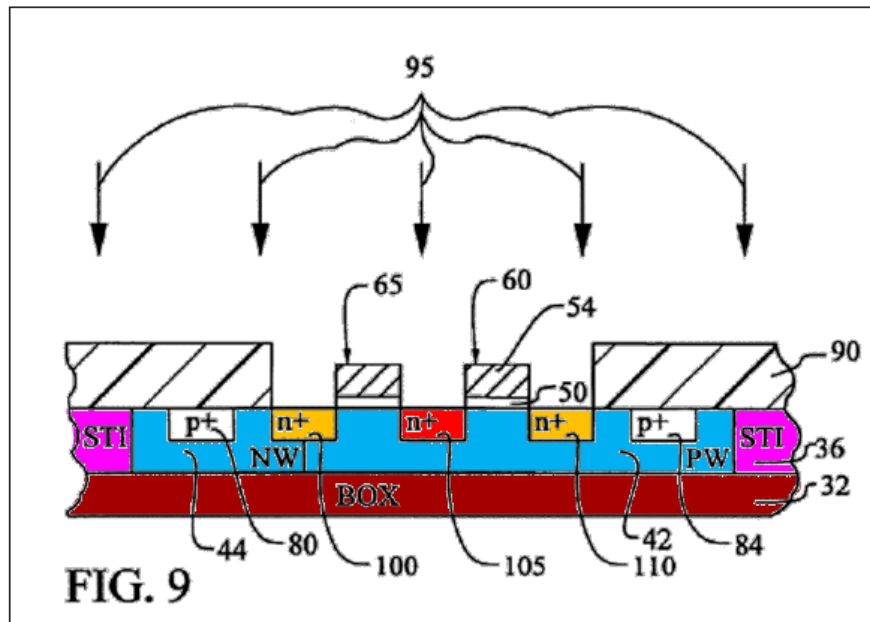
55. Petitioner and Dr. Thompson claim that *Yu* anticipates Claims 1, 2, and 3. I disagree. Although I understand from counsel that Patent Owner will seek to

cancel Claims 1 and 2, I have considered those claims in this section because they are relevant to my ultimate opinion that Yu does not anticipate Claim 3.

**1. Yu Does Not Disclose “each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance”**

56. In my opinion, *Yu* does not disclose “each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance” as required by Claim 1 of the ’886 Patent.

57. Dr. Thompson annotates Figure 9 of *Yu*, and I will use the same annotations for consistency. Below is Dr. Thompson’s annotations of Figure 9:



*Yu*, Fig. 9.

Ex, 1002, ¶ 201.

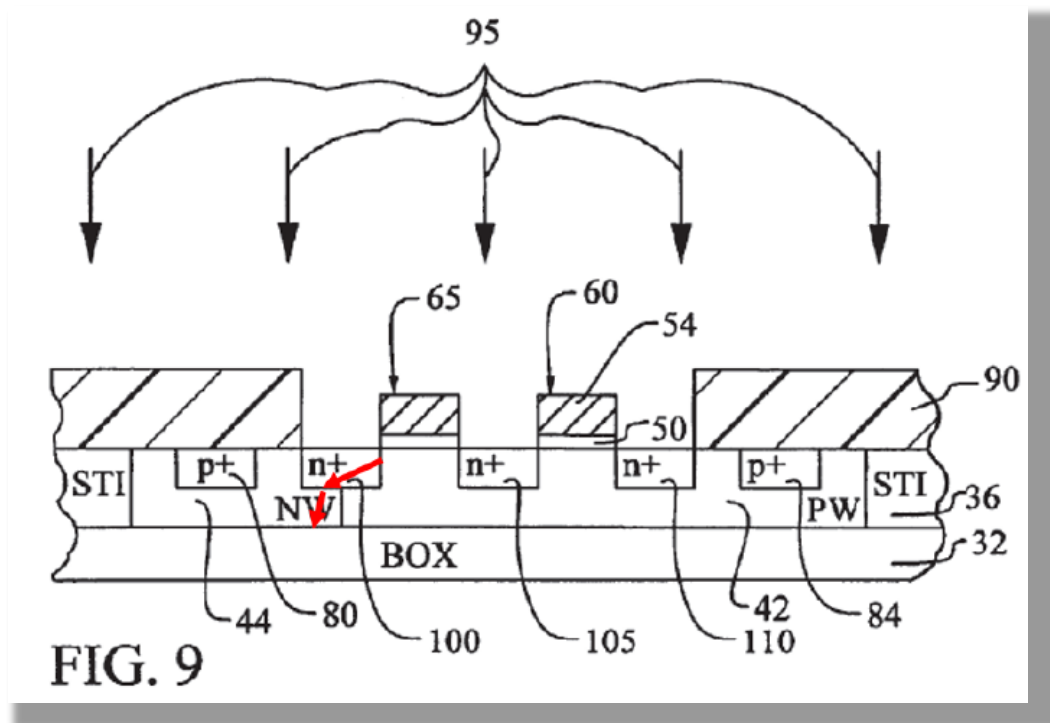
58. According to Dr. Thompson, the two “cascaded” transistors in *Yu* are labeled with annotations 60 and 65, and each of the transistors are connected to a common source which is the n+ doped region annotated in **red** and labeled as 105. Each transistor has its own drain, annotated in **yellow**. Ex. 1002, ¶¶ 200-201. Dr. Thompson also states that “a POSITA would have also recognized that the interfaces between these doped regions and the **silicon layer 34** form the **source/drain** junctions for the respective transistors.” *Id.* ¶ 201.

59. Claim 1 of the '886 Patent requires that “each” of the cascaded transistors has a source/drain junction that does not contact the buried oxide layer

and forms a source/drain junction capacitance. But in *Yu*, because of the presence of N-well 44, the transistor 65 does not have a source/drain junction capacitance even though neither the source, nor the drain, contact the buried oxide layer.

60. Although *Yu* does teach that the doped regions 80, 84, 100, 105, and 110 do not extend to the buried oxide layer, in my opinion this is insufficient to anticipate Claim 1.

61. Because the source region of the first transistor 100 is doped N+ and is partially located in the N-Well 44, it is, in fact, electrically in contact with the buried oxide layer, as prohibited by Claim 1 of the '886 Patent. This is shown, as annotated in Figure 9 of *Yu*, below:



62. Yu discloses that this doped region 100 is “coupled to the second well 44 . . . .” Ex. 1005, 5:41-53.

63. As *Yu* explains, the doped n+ regions form the source/drain junctions of the transistor, and as expressly stated by *Yu*, “doped region 100 is coupled to the second well 44” and, therefore, doped region 100 (the N+ well) *does* electrically contact the buried oxide layer, even if there is no physical contact. *Id.*, 5:51. Because of this electrical contact, no capacitance is formed. In my opinion, this lack of electrical contact and lack of capacitance on the drain of transistor 65 prevents the source/drain junction of transistor 65 from forming a source/drain junction capacitance and, therefore, Yu does not anticipate Claim 1.

**E. Ground 5: Burgener in Combination with Okashita Does Not Render Obvious Any Challenged Claim**

**1. There is No Motivation to Combine Burgener and Okashita**

64. In my opinion, there is no motivation to combine Burgener with Okashita. Although Burgener discloses that its integrated circuit may be fabricated using “semiconductor-on-insulator (SOI) techniques” (Ex. 1006, ¶ [0105]), I disagree with Dr. Thompson that the POSITA would have been motivated to use the specific SOI design in Okashita to create Burgener’s switch.

65. Dr. Thompson states that the POSITA would have been motivated to

build Burgener's integrated circuit using the teachings of Okashita for three reasons. First, he states that the POSITA would have been motivated to use the intervening silicon layer from Okashita because it would reduce the operating temperature of the transistors. Ex. 1002, ¶ 214. Second, he states that the POSITA would have been motivated to fabricate Burgener's circuit using Okashita's teachings "to prevent leakage of radio signals from the cascaded SOI FETs to other components of antenna switch 1700." *Id.* ¶¶ 215-16. Third, he states that the POSITA would have been motivated to locate each set of FETs together in one isolated region "to ensure that these FETs have consistent performance characteristics . . . ." *Id.* ¶ 217. I disagree with Dr. Thompson.

66. First, it is my opinion that the POSITA would not have been motivated to use the SOI process disclosed in Okashita to fabricate the circuits in Burgener because, if Dr. Thompson is to be believed, Okashita's configuration increases source/drain capacitance and, therefore, would create a slower switching circuit. But, in the event Dr. Thompson is correct that such capacitance exists, it is my opinion that this capacitance would create performance issues that the POSITA would consider unfavorable.

67. Dr. Thompson specifically relies on Burgener's Figure 17 for the disclosure of the "cascaded transistors" limitation. Ex. 1002, ¶ 221. Burgener states

that: “Fig. 17 is a simplified schematic of exemplary circuitry 1700 for an antenna switch. *Further details regarding design and fabrication of such an RF switch may be found in U.S. Pat. No. 6,804,502, issued Oct. 12, 2004 and entitled “Switch Circuit and Method of Switching Radio Frequency Signals.”* Ex. 1006, ¶ [0101] (emphasis added). In my opinion, given this express statement that the POSITA could look to the cited ’502 patent for fabrication details specifically related to this circuit, the POSITA would have not been motivated to further look to Okashita in order to fabricate Burgener’s transistors.

68. U.S. Patent No. 6,804,502 (“*Burgener II*,” Ex. 2004), cited directly in Burgener as providing details for the fabrication of the exact circuit relied upon by Dr. Thompson, discloses a circuit fabricated on an “Ultra-Thin-Silicon (‘UTSi’) substrate” wherein “the transistors used to implement the inventive RF switch are formed in an extremely thin layer of silicon in an insulating sapphire wafer.” Ex. 2004, 7:39-50. And, using this UTSi technology, “the parasitic capacitance between the nodes of the RF switch 30 are greatly reduced as compared with bulk CMOS and other traditional integrated circuit manufacturing technologies.” *Id.* at 7:58-62. Further, *Burgener II* states that the transistors in the RF switch can be made using ultra-thin silicon-on-sapphire technology, which eliminates the need for “[t]raditional transistor isolation wells” that are used for thick silicon. *Id.*, 10:66-

11:1. In my opinion, the POSTIA, if anything, would have been motivated to use the silicon-on-sapphire technology disclosed in *Burgener II* to fabricate the antenna switch disclosed in *Burgener*, rather than be motivated to look to what Dr. Thompson admits is a higher capacitance and therefore slower technology disclosed in *Okashita*.

69. I also understand that *Burgener* states in a separate section that “[o]ther semiconductor-on-insulator (SOI) techniques may be used to fabricate a dual-band transceiver integrated circuit as described above, for at least some frequency bands and power levels.” Ex. 1006, ¶ [0105]. I disagree that this provides a motivation to the POSITA to look to *Okashita*, for the reasons explained in the prior paragraph. I note that Dr. Thompson does not present any analysis of which frequency bands and/or power levels would motivate the POSITA to consider other semiconductor-on-insulator techniques aside from the UTSi technology that *Burgener* specifically advocates for.

70. Further, *Burgener* and *Burgener II*’s motivation to use UTSi would not have led the POSITA to look to other SOI technologies and specifically would not have led the POSITA to look to relatively thick silicon on top of a buried oxide layer, as shown in *Okashita* and as claimed by Dr. Thompson. Although other types of SOI may have been used to construct the circuit in *Burgener*, the POSITA would

not have been led to the construction techniques in Okashita because, as compared to UTSi, its high capacitance leads to decreased performance. In my opinion, the POSITA would not have had a reasonable expectation of success merely substituting thin silicon-on-sapphire for a relatively thick silicon on insulator technology, because of this additional capacitance.

71. Additionally, the three purported “motivations” that Dr. Thompson provides for the combination of Burgener and Okashita are either incorrect or impermissible hindsight. First, he states that the POSITA would have been motivated to use the intervening silicon layer from Okashita because it would reduce the operating temperature of the transistors. Ex. 1002, ¶ 214. I disagree that heat considerations are an issue in Burgener. Burgener only mentions thermal considerations one time, when discussing the need for stacked FETs in the power amplifier section (rather than the antenna switch relied upon by Dr. Thompson). Ex. 1006, ¶ [0044]. And even there, Burgener only discusses dissipating heat “in specific resistive series coupling elements rather than within the FETs themselves.” *Id.* Because Burgener states that dissipating heat inside the FETs is *not* desirable (rather, heat should be dissipated in the resistive couplings), the POSITA would not have been motivated to fabricate the transistors using what Dr. Thompson contends is a higher capacitance fabrication technique merely to dissipate additional heat in

the transistors.

72. Second, Dr. Thompson states that the POSITA would have been motivated to fabricate Burgener's circuit using Okashita's teachings "to prevent leakage of radio signals from the cascaded SOI FETs to other components of antenna switch 1700." Ex. 1002 ¶¶ 215-16. I disagree with Dr. Thompson. Burgener states that the circuit should be made using UTSi technology. UTSi technology is fully insulating, and "[t]he fully insulating sapphire substrate enhances the performance characteristics . . . by reducing the deleterious substrate coupling effects associated with non-insulating and partially insulating substrates." Ex. 2004, 7:39-64. Therefore, it is my opinion that the POSITA would not have been motivated to turn to another, less insulating SOI technology and then to build trenches as disclosed in *Okashita* to achieve insulating benefits that are already achieved by *Burgener*.

73. Third, Dr. Thompson states that the POSITA would have been motivated to locate each set of FETs together in one isolated region "to ensure that these FETs have consistent performance characteristics . . . ." Ex. 1002 ¶ 217. Other than hindsight bias garnered from Claims 2, 14, and 17 of the '886 Patent which require at least one of the plurality of transistors to be located within an isolated island, I do not understand why the POSITA would have been motivated to locate each set of Burgener's FETS together in one isolated region. Consistent

performance characteristics can be obtained through a number of methods, and placing the transistors in an isolated island would increase the space necessary for the circuit. This would specifically motivate the POSITA *not* to do this because, according to Burgener, it is desirable to integrate many devices and fabricate them “onto a single integrated circuit,” thereby solving a multitude of problems and gaining significant benefits. Ex. 1006, ¶ [0010].

**2. The Combination of *Burgener* and *Okashita* Does  
Not Teach the Required Electrical Isolation of Claim  
3**

74. Dr. Thompson relies entirely on the disclosures of *Okashita* for the electrical isolation claim elements. For the same reasons explained in Section IX.B, *Okashita* does not disclose or provide a motivation to create the limitations of claim 3 of the '886 Patent. Therefore, the combination of *Burgener* and *Okashita* does not render claim 3 obvious.

**F. Ground 6 (Burgener in Combination with *Okashita* and  
Yu) Fails**

**1. There is No Motivation to Combine Burgener,  
*Okashita*, and Yu**

75. Petitioner and Dr. Thompson also attempt to combine Yu with Burgener and *Okashita*. For the same reasons as in the previous Ground, it is my opinion that the POSITA would not have been motivated to add Yu to this

combination.

76. Dr. Thompson states that “a POSITA would have been motivated to ensure that an intervening silicon layer is sufficiently thick in the active area and that the cascaded FETs are completely within an isolated island of the active area, as *Yu* teaches, to ensure that the switching device does not fail at a lower energy dissipation level and to achieve the electrical benefits described by *Yu* (*see Yu*, 2:4-17)” and “[s]ince *Burgener*, *Okashita*, and *Yu* all disclose switching circuits with cascaded transistors having an SOI configuration (*see supra* §§VIII.A-VIII.C), a POSITA would have had a reasonable expectation of success in incorporating *Yu*’s teaching into *Burgener* and *Okashita*.” Ex. 1002, ¶ 262.

77. I disagree with Dr. Thompson that the POSITA would have been motivated to make this combination. For the same reasons stated above, it is my opinion that the POSITA would have been motivated by the express disclosures in *Burgener* that the antenna switch should be fabricated using UTSi technology and therefore would not have been motivated to look to the teachings of *Okashita*. Because, according to Dr. Thompson, the circuit in *Yu* would also increase capacitance and, therefore, slow down the circuit, there is no motivation for the POSITA to look to this technology.

78. Additionally, *Yu* does not disclose an antenna switch, but rather a high

voltage silicon-controlled rectifier. *See* Section IX.C. For this additional reason, it is my opinion that Yu is not analogous art to either Burgener or Okashita.

## **X. MATERIALS CONSIDERED**

79. In providing my technical review, analysis, insights, and opinions, I have considered the '886 Patent and its prosecution history.

80. I have also considered the Petition filed by the Petitioner in this proceeding and the relevant exhibits relied on by Petitioner, including the expert declaration submitted by Scott E. Thompson, Ph.D. I have also reviewed the transcript of the deposition of Dr. Thompson, dated June 17, 2025 (Ex. 2005).

81. In addition, I have reviewed the materials cited in this Declaration.

82. I have also considered my own experience and knowledge, as discussed above, and described more fully in my CV, in areas including semiconductor design, manufacturing, and other related technologies.

## **XI. CONCLUSION**

83. I declare under penalty of perjury that the foregoing is true and correct.

Dated: July 7, 2025

  
\_\_\_\_\_  
John Berg

# APPENDIX A

---

# JOHN BERG

---

• Palo Alto, California • 650.906.9657 • [johneberg2@gmail.com](mailto:johneberg2@gmail.com) •

---

## SUMMARY

As the Chief Technologist at American Semiconductor, Mr. Berg developed and designed CMOS sensors and systems built using bonded wafers and multichip modules using 45nm double-gate FET technology. Before joining ASI, Mr. Berg developed automated tools for the nano-imprint industry at Transfer Devices. Prior to Transfer Devices, Mr. Berg was a Managing Director at Cypress Semiconductor, where he managed a business unit that designed five new programmable logic chip product families in five years. Prior to Cypress, Mr. Berg was Vice President of Technology Development at Zilog, where he managed both technology development and design teams that built the company's 200mm wafer fabrication facility, designed Z8 microcontrollers, and engineered scaling of CMOS and embedded CMOS non-volatile memory technologies from 2um to 0.25um - the latter of which required co-development of CMP tools with the tool supplier. He received a Bachelor of Science degree in Physics from the Massachusetts Institute of Technology.

Mr. Berg has been an expert witness in semiconductor process development, silicon device physics, semiconductor design, CAD tools, lithography, semiconductor bonding including CMP, and business practices. He served as the plaintiff's expert witness in the Palmchip v. Ralink (Mediatek) microprocessor patent infringement. He was an expert witness for the plaintiff in Semi-Materials Co. Ltd. v. MEMC Pasadena Inc, in which he testified at jury trial twice and was deposed twice. In both cases, the plaintiff won, with more than \$19M being awarded to Mr. Berg's client. Mr. Berg also has testified in front of the US Patent Office in the re-examinations of three patents, all of which were successfully defended, and has been an expert in numerous IPR cases. He was deposed as a Cypress employee in Cypress Semiconductor v. Altera Corp., where Altera was sued for interference with contract, trade secret misappropriation, and unfair competition involving programmable logic devices. At Standard Microsystems, he did reverse engineering analysis on competitors' products; these analyses led to three successful licensing agreements with other semiconductor companies.

---

## PROFESSIONAL EXPERIENCE

### BERG-ATTENBOROUGH, INC.

SEPTEMBER 2010 - PRESENT

#### PRINCIPAL (2 EMPLOYEES)

Berg-Attenborough, Inc. is a consulting firm, which does technical consulting for Top 50 semiconductor companies and does expert witness work for patent and business issues.

#### *Key Achievements:*

- Developed wafer bonding and CMP for advanced photonics integrated circuit processing.
  - Fan-Out Wafer Level Packaging, FO-WLP consulting for Draper Laboratories
    - Successfully developed a 60+ chip multi-chip module including MPU, FPGA, DRAM, and FLASH.
    - Uncovered two temperature cycle reliability problems with the existing FO-WLP technology and instituted corrective actions to the process and design to eliminate these.
      - Modified interlayer dielectric and solder mask to correct die cracking
        - Problem uncovered by SEM and verified via SEM and reliability testing
      - Modified metal bus rules using Ansys and empirical data to ameliorate die cracking
-

### **PROFESSIONAL EXPERIENCE (CONT.)**

#### **AMERICAN SEMICONDUCTOR, INCORPORATED**

**2005-2014**

##### **CHIEF TECHNOLOGIST (22 EMPLOYEES)**

American Semiconductor is fabricating radiation-hard CMOS products for military and aerospace customers.

##### ***Key Achievements:***

- Hands-on in-fab development the front-end & back-end full wafer scale process for an antenna array product, which resulted in a Top Supplier of the Year Award from Boeing. A low temperature substrate-to-substrate bonding technique was developed specifically for this product.
- Hands-on in-fab development of the company's double-gate FET process, and successful transfer of the company's double-gate FET CMOS process from university laboratory into a CMOS production facility. This included CMP, lithography, and etching processes.
- Design of MCU/analog RF/sensor/memory flexible system-on-chip reference products:
  - Products includes hardware and software/firmware for system control and security/encryption
  - Process development included direct low temperature and high temperature direct wafer-to-wafer bonding techniques with and without through silicon vias (TSV's) to reduce system form factor.
  - Flip-chip, ball-bond, and wire-bonding used to assemble product.

#### **TRANSFER DEVICES, SANTA CLARA, CA**

**2004-2005**

##### **CHIEF OPERATING OFFICER (12 EMPLOYEES)**

Transfer Devices is a lithography start-up, which is commercializing technology developed in Professor Fabian Pease's laboratory at Stanford University.

##### ***Key Achievements:***

- Built a class 10 manufacturing clean room and delivered product to customers.
- Launched the ExaGlide 10r nano-patterning production tool development program
- Improved tool uptime from <10% to 95% and product yields from 50% to 99.9%

#### **NANTERO, WOBURN, MA**

**2003-2004**

##### **VICE PRESIDENT, NEW PRODUCT DEVELOPMENT (50 EMPLOYEES)**

Nantero is developing non-volatile random-access memory using carbon nanotube switches.

##### ***Key Achievements:***

- Hired and led the design team that taped out a 4Mb non-volatile memory chip, which resulted in a radiation-hardened non-volatile memory technology.

### **PROFESSIONAL EXPERIENCE (CONT.)**

#### **CYPRESS SEMICONDUCTOR, SAN JOSE, CA**

**1998-2002**

##### **MANAGING DIRECTOR, PROGRAMMABLE LOGIC (5500 EMPLOYEES)**

Cypress Semiconductor, a public company, is a broad line supplier of semiconductor components.

##### ***Key Achievements:***

- Program manager for Delta39K, 37K product lines, including hardware development, and software/firmware development on systems instantiated by customers.
- First Cypress multi-chip module product, using flip-chip and ball-bonding technologies.
- Hired, trained, and managed the ESD team at Cypress (3 technology and design engineers). Reduced the number of corporate ESD-related design errors from 50% to <5% by standardizing ESD design rules, testing and incorporating secondary breakdown into the ESD design, standardizing ESD design methodology, and instituting formal ESD design reviews into Cypress's design flow. Purchased test systems for in-house ESD testing.
- Integrated NAND FLASH IC and SRAM-based CPLD IC into 1<sup>st</sup> Cypress multichip module
- Developed and put into production the company's 0.25um BiCMOS and 0.18um SiGe HBT processes used for Datacommunications Products. Substantial materials and CMP work.
  - Provided PDK, CAD, and Device support.
- Increased revenues from \$38M to \$72M by increasing the number of PLD/FPGA product families to 6, including the Ultra37000, Delta39K, Quantum38K and PSI product families
- Designed CPLD products in TSMC's 0.13um technology which used copper interconnect.

#### **ZILOG CORPORATION NAMPAL, ID**

**1990-1998**

##### **VICE PRESIDENT, TECHNOLOGY DEVELOPMENT (1600 EMPLOYEES)**

Zilog was a pre-IPO company that successfully went public in 1991 and was later acquired by IXYS.

##### ***Key Achievements:***

- Trained and led the Nampa site's 15-person Design Department and 30-person Technology Development Department; delivered memory cells (SRAM, EEPROM, EPROM, NOR Flash), memory block compilers, and I/O cells for the company's design library for its system-on-chip and application-specific standard products.
  - Designed, built, and qualified the \$175M 200mm fabrication facility: 1<sup>st</sup> silicon yield.
    - 0.25um CMOS technology, including CMP, tungsten plugs, trench isolation, and low k dielectric. First dry-in/dry-out CMP metals and dielectric tools brought into production.
    - Solved the temperature cycle problem with the 200mm line within 90 days after initial observation. Solution involved modifying design rules for metallization and improved planarization.
  - Hired, trained, and led the design team that taped out 6 system-on-chip products per year for 8 years for the \$120M Z8 microcontroller business unit.
  - Worked with outside laboratories to ensure hardware design compliance to FCC's EMF/EMI requirements.
  - Modified design rules and design clocking scheme to improve 1<sup>st</sup> pass yields.
-

### **PROFESSIONAL EXPERIENCE (CONT.)**

**STANDARD MICROSYSTEMS CORPORATION, HAUPPAUGE, NY** **1980-1990**  
**ENGINEERING DIRECTOR (500 EMPLOYEES)**

Standard Microsystems was a public company in 1980, and later, was acquired by Microchip, Inc.

***Key Achievements:***

- Began career as a hands-on manufacturing CVD engineer working with Applied Materials deposition tools.
- Solved the company's Highly Accelerated Temperature/Humidity Stress Test (HAST) problem, that had been plaguing the company for five years, using optimizing thin film dopant concentration.
- Instituted DOE and six sigma process development practices in 1986.
- Hired, trained, and managed 26 sustaining and development engineers in the company's 2500 wpm wafer fab. Developed and transferred five 2um/sub-2um CMOS technologies into production.
- Reversed engineered Intel, TI, and National Semiconductor products to provide evidence of infringement against Standard Microsystem's patents. This included working with and coordinating external laboratories to provide deconstruction analysis.

---

### **EDUCATION**

|                  |                                                                                                                                 |                      |
|------------------|---------------------------------------------------------------------------------------------------------------------------------|----------------------|
| <b>2002-2003</b> | <b>STANFORD UNIVERSITY</b><br>M.S. Management, Graduate School of Business. Sloan Fellow.                                       | <b>PALO ALTO, CA</b> |
| <b>1998-2002</b> | <b>STANFORD UNIVERSITY</b><br>16 graduate credits in Electrical Engineering (GPA = 4.1) in circuit design                       | <b>PALO ALTO, CA</b> |
| <b>1975-1980</b> | <b>MASSACHUSETTS INSTITUTE OF TECHNOLOGY</b><br>BS Physics. Four-year National Merit Finalist and Scholar. Intercollegiate crew | <b>CAMBRIDGE, MA</b> |

## **PUBLICATIONS**

“MOS Transistor Technology from Planar to Nanowire Transistors,” Mantha, B. and Berg, J., Silicon Valley Engineering Council Journal, Volume 1, 2009, Pages 23-32.

“Substrate Bias Effects on Transiently Triggered Latchup in Bulk CMOS,” Chang, L. and Berg, J.; IEEE Transactions on Electron Devices, Volume 33, Issue 1, Jan. 1986 Pages 165 - 167

“A Derivative Method to Determine a MOSFET's Effective Channel Length and Width Electrically,” Chang, L. and Berg, J.; IEEE Electron Device Letters, Volume 7, Issue 4, Apr 1986 Pages 229 – 231.

“A Simplified Model to Predict the Linear Temperature Coefficient of a CMOS Inverter's Delay Time,” Chang, L., Khoa Vo and Berg, J.; IEEE Transactions on Electron Devices, Volume 34, Issue 8, Aug 1987 Pages 1834 – 1837.

---

## **CONFERENCE LEADERSHIP AND PRESENTATIONS**

Co-Chairman, 2007 IEEE San Francisco Bay Area Nanotechnology Symposium, July 2007.

“Rad-Hard Reconfigurable Bidirectional Level Shifter (ReBiLS) for NASA Space Applications in the Flexfet 0.18um SOI CMOS Technology,” K. DeGregorio, D. Wilson, S. Parke, J. Berg, M. Goldston, R. Hayhurst, D. Hackler 12th NASA Symposium on VLSI Design

Committee Member, Programmable Logic Sub-Committee, 2003 IEEE Solid State Circuits Conference, San Francisco, CA

“Measuring the Effective Channel Length of the Deep Submicron MOSFET and the Channel Broadening Effect,” S.H. Chung, Tim Carns, S.K. Lee, L. DeBruler, and J. Berg, Proceedings of the Thirteenth Biennial University/Government/Industry Symposium, IEEE Press, pp. 176-181, 1998.

### **PATENTS**

| <u>Patent Number</u> | <u>Title</u>                                                                                                     |
|----------------------|------------------------------------------------------------------------------------------------------------------|
| 8,913,402            | Triple-damascene interposer                                                                                      |
| 7,595,527            | Non-volatile electromechanical field effect devices and circuits and methods of forming same                     |
| 6,476,635            | Programmable number of metal lines and effective metal width along critical paths in a programmable logic device |
| 6,436,195            | Method of fabricating a MOS device                                                                               |
| 6,190,973            | Method of fabricating a high quality thin oxide                                                                  |
| 6,165,846            | Method of eliminating gate leakage in nitrogen annealed oxides                                                   |
| 6,156,653            | Method of fabricating a MOS device                                                                               |
| 5,978,127            | Light Phase Grating Device                                                                                       |
| 5,631,180            | Method of fabricating high threshold metal oxide silicon read-only-memory transistors                            |
| 5,498,896            | High threshold metal oxide silicon read-only-memory transistors                                                  |
| 5,389,565            | Method of fabricating high threshold metal oxide silicon read-only-memory transistors                            |
| 5,338,423            | Method of eliminating metal voiding in a titanium nitride/aluminum processing                                    |
| 5,317,187            | Ti/TiN/Ti contact metallization                                                                                  |
| 5,244,831            | Method of doping a polysilicon layer on a semiconductor wafer                                                    |
| 5,240,880            | Ti/TiN/Ti contact metallization                                                                                  |
| 4,895,520            | Method of fabricating a submicron silicon gate MOSFET, which has a self-aligned threshold implant                |
| 4,824,803            | Multilayer metallization method for integrated circuits                                                          |

---

### **PROFESSIONAL MEMBERSHIPS**

- National Science Foundation, Electronics & Nanotechnology Phase I & II SBIR Reviewer •
    - Gerson, Lehrman Group: Leader (Top 5%) Council member •
  - Chair Emeritus, and Founding Member, IEEE San Francisco Bay Area Nanotechnology Council •
    - IEEE National Chapter of the Year Award, 2013 •
    - Executive Committee Member, IEEE Santa Clara Valley Section •
    - Member, Silicon Valley Engineering Council Steering Committee •
      - Senior Member, IEEE •
      - Member, Sigma Xi •
    - Member, New York Academy of Science •
    - Chair, Vistage International 2010-2015 •
    - Security Clearance: Secret •
- 

### **SEMINARS, TUTORIALS & WORKSHOPS**

- ESD Association Tutorial: "Prevention of Electrostatic Discharge to Electronic Devices, Assemblies, and Systems." 1998 •
  - Juran Institute, "Juran Management Systems," 1989 •

**SOFTWARE**

**DESIGN TOOLS:**

**SYNOPSYS:** GALAXY DESIGN PLATFORM: DESIGN COMPILER, CUSTOM DESIGNER  
SE/DE/SDL, PRIMETIME, IC COMPILER, HSPICE, IC VALIDATOR, POWER  
COMPILER

**CADENCE:** AMS DESIGNER, ASSURA, SPECTRE, VIRTUOSO

**MENTOR GRAPHICS:** CALIBRE

**TCAD:**

**SILVACO:** ATHENA, ATLAS, VICTORY

**OTHER TOOLS:** VHDL, PYTHON, JSON, JMP, MATLAB, MICROSOFT OFFICE SUITE