

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD,
SAMSUNG ELECTRONICS AMERICA, INC., NXP
SEMICONDUCTORS, N.V.¹

Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,
Patent Owner.

Case No. IPR2024-01402
U.S. Patent No. 7,745,886

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

¹ NXP Semiconductors N.V. filed a petition and a motion for joinder in IPR2025-00954 that were granted and have been joined as petitioners in this proceeding.

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PETITIONER’S UPDATED EXHIBIT LIST

Exhibit	Description
Ex. 1001	U.S. Patent No. 7,745,886 to Zwingman (“’886 patent”)
Ex. 1002	Declaration of Scott Emmet Thompson, Ph.D. (“Thompson”)
Ex. 1003	Prosecution History of the ’886 patent (downloaded from Public PAIR)
Ex. 1004	U.S. Patent No. 6,836,172 to Okashita et al. (“ <i>Okashita</i> ”)
Ex. 1005	U.S. Patent No. 6,737,682 to Yu (“ <i>Yu</i> ”)
Ex. 1006	U.S. Patent Publication No. 2006/0270367 to Burgener et al. (“ <i>Burgener</i> ”)
Ex. 1007	Webster’s Ninth New Collegiate Dictionary, Merriam-Webster, Inc., Springfield, Massachusetts, U.S.A., 1985, p. 211.
Ex. 1008	“Fundamentals of Semiconductor Physics and Devices,” Rolf Enderlin and Norman J.M. Horing, World Scientific, 1996, pp. 535-539, 620-622.
Ex. 1009	“Electronics Circuits and Analysis,” Dinesh C. Dube, Alpha Science International Ltd., 2005, pp. 202-207.
Ex. 1010	“SOI Design: Analog, Memory and Digital Techniques,” Andrew Marshall and Sreedhar Natarajan, Kulwer Academic Publishers, 2003, pp. 1-46, 75-84, 125-179, 289-338, 340-358.
Ex. 1011	“CMOS Logic Circuit Design,” John P. Uyemura, Kluwer Academic Publishers, 2002, pp. 1-2, 19, 35-36, 78-83, 94-96, 359-362.
Ex. 1012	“The Stuff Dreams Are Made Of [Part 1],” Paul DeMone, May 8, 2002, Available at: https://www.realworldtech.com/cmos-basics
Ex. 1013	“SOI for Digital CMOS VLSI: Design Considerations and Advances,” Ching-Te Chuang et al., Proceedings of the IEEE, Vol. 86, No. 4, April 1998, pp. 689-720.
Ex. 1014	“1 Giga bit SOI DRAM with fully bulk compatible process and body-contacted SOI MOSFET structure,” Yo-Hwan Koh et al., 1997 International Electron Devices Meeting Technical Digest, Washington, DC, USA, 1997, pp. 579-582.

Exhibit	Description
Ex. 1015	U.S. Patent No. 6,121,148 to Bashir et al. (“Bashir”), published September 19, 2000.
Ex. 1016	“Speeding up Transistors: IBM to Make SOI Chips,” Katherine Derbyshire, Semiconductor Online, August 18, 1998.
Ex. 1017	“SOI-CMOS Device Technology,” Yasuhiro Fukuda, et al., Special Edition on 21st Century Solutions, OKI Technical Review 185, Vol. 68, March 2001, pp. 54-57.
Ex. 1018	“Impact of high-k gate stack material with metal gates on LF noise in n- and p-MOSFETs,” P. Srinivasan et al., Microelectronic Engineering 80 (2005) 226–229.
Ex. 1019	U.S. 2004/0150045 A1 to Nonaka et al., published August 5, 2004 (“Nonaka”).
Ex. 1020	U.S. Patent No. 6,498,371 B1 to Krishnan et al., published December 24, 2002 (“Krishnan”).
Ex. 1021	U.S. Patent No. 6,933,569 B2 to Koh et al., published August 23, 2005 (“Koh”).
Ex. 1022	“Temperature-Dependent Thermal Conductivity of Single-Crystal Silicon Layers in SOI Substrates,” M. Asheghi et al., Transactions of the ASME, Journal of Heat Transfer, Vol. 120, February 1998, pp. 30-36.
Ex. 1023	“Current Mode Digital Gates for Mixed Mode Reprogrammable Integrated System,” P. Pawlowski, Proceedings of the 1st IEEE International Conference on Circuits and Systems for Communications, 26-28 June, 2002, St. Petersburg State Polytechnic University Publishing House, 2002, pp. 178-181.
Ex. 1024	<i>Harbor Island Dynamic, LLC v. Samsung Electronics Co. Ltd. et al</i> , Case No. 2:24-cv-00140, Plaintiff’s Infringement Contentions Cover Pleading (July 18, 2024)
Ex. 1025	<i>Harbor Island Dynamic, LLC v. Samsung Electronics Co. Ltd. et al</i> , Case No. 2:24-cv-00140, Dkt. No. 38, Docket Control Order (E.D. Tex. August 2, 2024)
Ex. 1026	Supplemental Declaration of Scott Emmet Thompson, Ph.D. (“Thompson-Supp”)

Exhibit	Description
Ex. 1027	European Patent 2,220,697 B1, McKenzie et al., published November 9, 2019
Ex. 1028	“Modeling and characterization of deep trench isolation structures,” S. Lee, Microelectronics Journal 32 (2001) pp. 295-300.
Ex. 1029	U.S. Patent No. 4,786,960 to Jeuch, published November 22, 1988.
Ex. 1030	Chicago Manual of Style, 15 th ed., (2003), pp. 268-70.
Ex. 1031	Garner’s Dictionary of Legal Usage, Bryan A. Garner, 3d ed. (2011), pp. 730-34.

I. Introduction

HID's Patent Owner Response ("POR") reiterates the same arguments previously presented before institution. Although now HID proffers an expert (Mr. Berg) to echo its arguments, the Board should again reject these arguments for the reasons it did at institution. HID also introduces new arguments, but they mischaracterize the prior art and the Petition, and they lack legal, factual, and technical merit. HID fails to meaningfully address the core teachings of *Okashita*, *Yu*, and *Burgener*. It offers no credible or substantiated rationale to counter the Petition's showing that the prior art anticipates or would have rendered obvious claims 3 and 8–19, the only remaining challenged claims.² The Board should cancel these claims.

II. There Is No Material Dispute over Level of Ordinary Skill in the Art

HID contends that a POSITA would hold only a bachelor's degree with two years of relevant experience, rather than the master's degree proposed in the Petition. *Compare* POR §IV with Pet. §IV. This distinction is immaterial. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (holding "specific

² The Petition challenged claims 1-19 of the '886 Patent. HID cancelled claims 1-2 and 4-7 and only disputes the unpatentability of claims 3 and 8–19 (Grounds 2–6). POR, 1-2, 15.

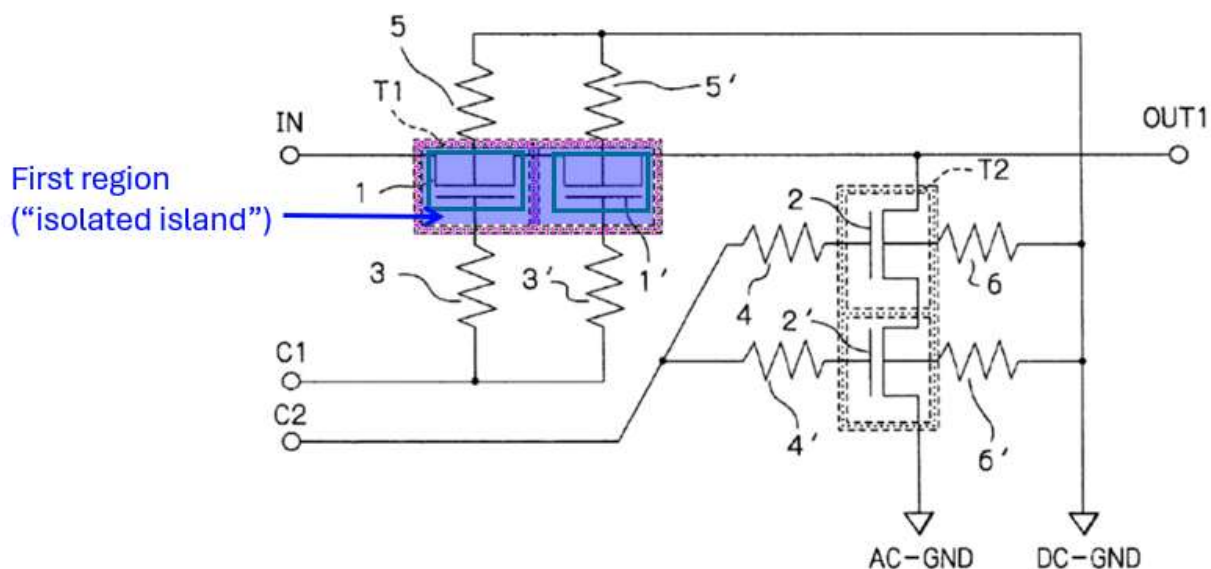
findings on the level of skill in the art” are unnecessary “where the prior art itself reflects an appropriate level and a need for testimony is not shown”) (*quoting Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985)). Both parties agree that a POSITA would have at least two years of experience in semiconductor design and fabrication, and HID never identifies any claim limitation or analysis that hinges on the degree level. *See* POR §§IV–VI.

III. Ground 2: *Okashita* Renders Obvious Claim 3.

A. HID’s Response Misrepresents the Petition and Fails to Address Its Actual Arguments.

In Ground 2, the Petition contends that independent claim 1 is obvious over *Okashita*. In doing so, the Petition relies on transistors 1 and 1' of *Okashita*’s Figures 19-20 for the “plurality of cascaded transistors.” Pet., 29-30. The Petition further contends that *Okashita* teaches the additional limitation of claim 3, namely that “said plurality of cascaded transistors is situated within an isolated island in said device layer.” *Id.*, 23-24. Indeed, as explained in the Petition and shown in the below annotated version of Figure 19, a POSITA reading *Okashita* would have understood that the trench T1 surrounding the plurality of MOS transistors 1, 1' effectively places these MOS transistors within an isolated “first region” in the silicon layer. Pet., 35 (citing Thompson, ¶167, *Okashita*, 8:47-54, 9:21-25, Figs. 19-20). The Petition also explains why it would have been obvious to configure *Okashita* in this way. Pet., 35-36.

Fig. 19



Rather than confront *Okashita*'s placement of MOS transistors 1, 1' in an isolated first region in the silicon layer (the claimed "isolated island in said device layer"), HID alleges that "the POSITA would not have been motivated to remove the isolation trenches between these two transistors." POR, 17-18. But Petitioner did not propose such (or any other) modification to the structure of *Okashita* in its discussion of claim 3. And whether or not isolation trenches exist between MOS transistors 1, 1' is irrelevant to whether the isolated first region in which MOS transistors 1, 1' are situated constitutes the claimed isolated island.

HID does not argue that *Okashita*'s **first region** is not an “isolated island.” See POR, 16-17. To the extent HID invokes the “isolated island” of cancelled claim 2 to imply that a trench running through **first region** between **transistors 1** and **1'**

would somehow preclude that region from qualifying as the “isolated island” recited in claim 3 (*see* POR, 16) by separating the first region into two islands, it offers no supporting explanation, which is contrary to Federal Circuit precedent. For example, in *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000), the Federal Circuit held that “an” means “one or more” in open-ended claims, stating that “[t]his court has repeatedly emphasized that an indefinite article ‘a’ or ‘an’ in patent parlance carries the meaning of ‘one or more.’” *See also AbTox, Inc. v. Exitron Corp.*, 122 F.3d 1019, 1023 (Fed. Cir. 1997) (explaining that the article “a” receives a singular interpretation only in rare circumstances when the patentee evinces a clear intent to so limit the article). The specification of the ’886 Patent does not clearly suggest that the inventors intended the article “an” to have any meaning other than its ordinary meaning—“one or more.” Thus, even if the first region in *Okashita* was two islands, it would still meet claim 3’s limitation of “an isolated island in said device layer” in which “said plurality of cascaded transistors is situated.” Both islands would together be isolated by the trench T1 surrounding the plurality of MOS transistors 1, 1'. The claim requires nothing more and does not preclude MOS transistors 1, 1' from also being isolated from each other.

IV. Ground 3: *Okashita* and *Yu* Render Obvious Claim 3.

Regarding Ground 3, HID does not dispute the prior art's disclosure of the claim elements but instead challenges the rationale for combining *Okashita* and *Yu*. POR, 18-23. HID's argument is without merit.

A. *Okashita* and *Yu* Are Analogous Art to the '886 Patent.

First, HID argues that *Okashita* and *Yu* are not analogous art because *Yu*'s invention is specifically confined to “a method to form a low voltage triggering, silicon-controlled rectifier (SCR) SOI device having improved ESD performance,” while *Okashita* is directed to “a semiconductor switch apparatus for radio frequency signals.”³ POR, 18-19. But HID selectively quotes from *Yu*'s stated field of invention (by omitting a portion of *Yu*'s statement that “[t]he invention relates to silicon-on-insulator (SOI) devices,” (*Yu* (Ex. 1005), 1:10-11), to suggest a divergence from *Okashita*. POR, 18–19. In reality, no divergence exists and HID's characterization is improper.

Under *In re Bigio*, 381 F.3d 1320 (Fed. Cir. 2004), the field of endeavor is determined by examining the subject matter described in the patent and prior art,

³ HID agrees that prior art is analogous to a challenged patent if it (1) is from the same field of endeavor, or (2) is reasonably pertinent to the problem addressed by the patent. POR, 22.

including structure and function—not by parsing differences in application labels. The '886 Patent, *Okashita*, and *Yu* all share a common focus on SOI device structures (cascaded transistors on an SOI substrate surrounded by trench isolation (see Pet., §§II.A, V.A.1, V.C.1-2; Thompson, §§VII.A, VIII.A-B), and HID's selective framing obscures this clear technological alignment. They are all in the same field of endeavor because they all relate to a semiconductor switching circuit with cascaded transistors having an SOI configuration. Pet., 7-8, 39-40; Thompson, ¶¶77-80, 90-91.

Specifically, the '886 Patent expressly states that its invention is “generally in the field of fabrication of semiconductor structures and circuits” and, more specifically, “in the field of fabrication of semiconductor on insulator (SOI) structures and circuits.” '886 Patent (Ex. 1001), 1:14–17. *Okashita* similarly discloses a semiconductor switch apparatus with series-connected MOS transistors implemented in SOI configuration. Pet., §V.A.1; Thompson, ¶77; *Okashita*, 1:7-15. And *Yu* likewise states that its invention “relates to silicon-on-insulator (SOI) devices,” and discloses a semiconductor switching device (or silicon-controlled rectifier–SCR) with cascaded transistors in an SOI configuration. Pet., §V.C.1; Thompson, ¶91; *Yu*, 1:9-13, 5:20-57.

Moreover, much like the switching circuits of the '886 Patent and *Okashita*, trenches isolate the cascaded transistors in *Yu*'s SOI switching device. Pet.,

§§V.A.1, V.C.2, Thompson, ¶¶77-81, 90-98. Despite this clear overlap, HID attempts to narrow the field by focusing on the end-use applications of each reference—RF switching versus ESD protection—which is not proper under Federal Circuit precedent.

Okashita and *Yu* are also “reasonably pertinent” to the problem addressed by the 886 Patent—namely, how to structure and isolate cascaded SOI transistors in a switching circuit. *See* ’886 Patent, e.g., 1:31-43 (explaining that the disclosed cascaded SOI transistor structure addresses the challenge of electrical isolation inherent in bulk silicon technology). As the Federal Circuit held in *In re ICON Health & Fitness*, 496 F.3d 1374, 1379-80 (Fed. Cir. 2007), art is analogous if it logically would have commended itself to the inventor’s attention in solving the problem at hand. *Okashita* pertains to using insulating trenches to electrically isolate cascaded MOS transistors in a semiconductor switching circuit having an SOI configuration. Pet., §V.A.1. And a POSITA working on SOI transistor layout in a switch apparatus like *Okashita*’s would have plainly found relevant *Yu*’s teachings of robust SOI transistor structures for a switching circuit. *See* Pet., §§V.C.1-2; Thompson, ¶¶89-98, 176-180.

B. The Petition Provides Compelling Rationale for Combining *Okashita* and *Yu* Consistent with *KSR* Precedent.

Second, HID contends that the Petition overlooks several “meaningful differences” between *Yu* and *Okashita*, and therefore, fails to establish a sufficient motivation to combine them. POR, 18. Specifically, HID alleges that *Yu*’s silicon-controlled rectifier is designed to switch “very high voltages,” whereas *Okashita*’s switch operates within a much narrower range of approximately -3V to 3V. POR, 18-19. However, this distinction in end-use application is immaterial to the question of motivation to combine. *In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012) (finding differences in the specific application or intended use of prior art references do not defeat motivation to combine); *cf. In re Paulsen*, 30 F.3d 1475, 1479 (Fed. Cir. 1994) (holding the intended use or purpose of a device does not limit its disclosure for obviousness purposes).

Yu’s switching device is intended for ESD protection, while *Okashita*’s switch toggles an antenna between transmit and receive paths. *See Yu*, 1:23–27; *Okashita*, 1:11–15. Despite these differing end-use applications, both devices operate (switch between ON and OFF states) at comparable voltages—*Yu*’s device turns on at approximately 3.3V (*Yu*, 6:4–31), and *Okashita*’s at 3V (*Okashita*, 7:34–39). Moreover, both employ similarly configured transistors: stacked SOI transistors formed within isolated islands surrounded by trench isolation. Given

these structural and operational parallels, as explained in the Petition (Pet. §V.C.2), a POSITA seeking to enhance *Okashita*'s switch would have been naturally guided to *Yu*'s teachings, particularly those addressing thermal and electrical performance.

The Petition's rationale for combining *Okashita* and *Yu* (see Pet., §V.C.2; Thompson, ¶¶176-180) aligns with the Supreme Court's guidance in *KSR Intern. Co. v. Teleflex Inc.*, 550 U.S. 398 (2007), which holds that combining known elements according to their established functions to yield predictable results is obvious. *Okashita* describes a switching circuit with cascaded transistors on SOI substrates, placed in isolated islands using trench isolation. Pet., §V.A.1; Thompson, ¶¶75-88. *Yu* discloses fabrication methods that improve thermal and electrical performance in similar trench isolated SOI transistors. Pet., §§V.C.1-2; Thompson, ¶¶89-98, 176-180. A POSITA looking to enhance *Okashita*'s design would logically apply *Yu*'s techniques—an example of routine optimization and common sense. The combination of *Okashita* and *Yu* reflects precisely the kind of predictable improvement and routine optimization that *KSR* recognized as supporting a motivation to combine.

HID argues that *Yu* and *Okashita* address different end-use, application-specific problems that “have nothing to do with one another [and] also have nothing to do with the problem solved by the '886 Patent,” and on that basis argues that a POSITA would not have been motivated to combine their teachings. POR,

19–22. This argument misapplies the standard for obviousness. As the Supreme Court explained in *KSR*: “The question is not whether the combination was obvious to the patentee but whether the combination was obvious to a person with ordinary skill in the art. Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.” 550 U.S. at 420. The Federal Circuit has repeatedly held that a reference need not solve the same problem as the challenged patent to be suitable for a combination. For example, in *In re Kahn*, 441 F.3d 977, 986 (Fed. Cir. 2006), the Federal Circuit explained that a motivation to combine may arise from any need or problem known in the field of endeavor, not just the specific issue addressed by the patent.

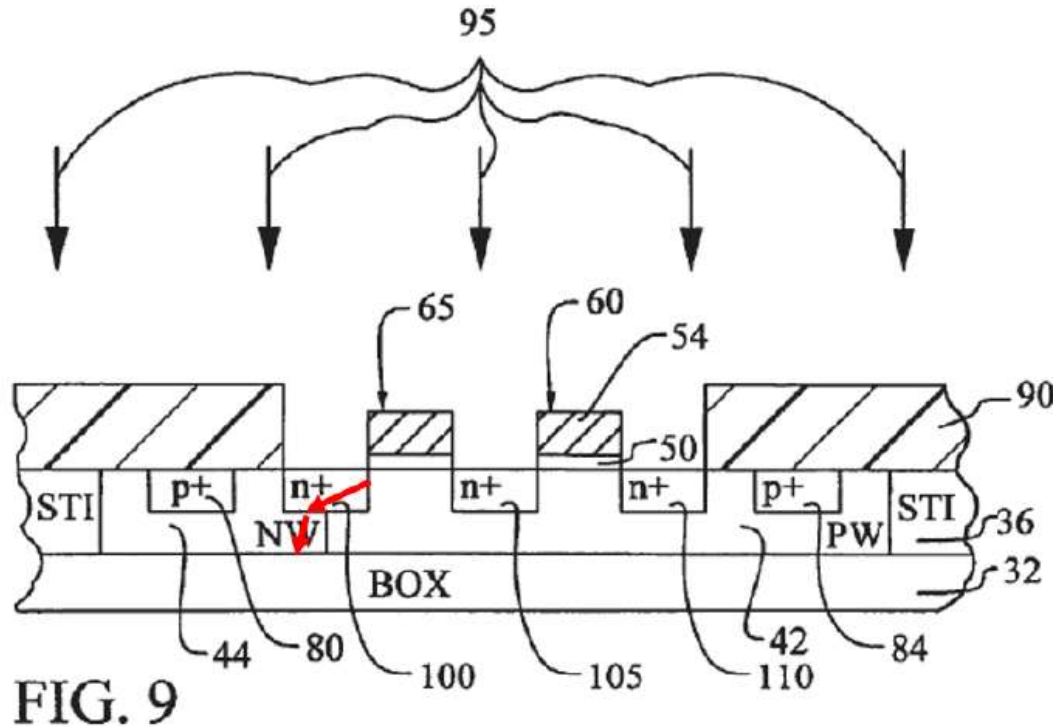
Here, both *Yu* and *Okashita* disclose switching devices that utilize cascaded SOI transistors formed in isolated islands surrounded by trench isolation—key structural and functional features shared with the ’886 Patent. *Yu* further teaches transistor configurations that enhance thermal and electrical performance in SOI switching devices (*see* Pet., §§V.C.1-2; Thompson, ¶¶89-98, 176-180), which a POSITA would recognize as directly applicable to *Okashita*’s architecture. That *Yu*’s device is used for ESD protection and *Okashita*’s for antenna switching is immaterial, particularly where the underlying transistor configuration and isolation structures are materially similar.

HID also contends that a POSITA would not have been motivated to consult *Yu* for the teachings of claim 3. POR, 22-23. In Ground 3, the Petition relies on *Okashita* to teach the limitations of claim 3 (“said plurality of cascaded transistors is situated within an isolated island in said device layer”), as previously discussed in Ground 2. Pet., §V.C.5. Additionally, the Petition presents a secondary argument that *Yu* also discloses the features of claim 3 and that a POSITA would have found it obvious to incorporate *Yu*’s teachings into *Okashita*, which would satisfy the claim’s requirements. *Id.* HID contends that a POSITA would lack motivation to consult *Yu* for claim 3 because, unlike *Yu*, *Okashita* isolates individual transistors using trenches to prevent radio signal leakage. POR, 22-23. But, because *Okashita* independently teaches the limitations of claim 3 and their benefits (Pet., §§V.C.5, V.B.3; *supra* III), HID’s argument regarding the lack of motivation in *Okashita* to look to *Yu* is immaterial.

V. Ground 4: *Yu* Anticipates Claim 3.

Regarding Ground 4, HID recycles its pre-institution argument that *Yu* does not anticipate claim 3 because *Yu*’s “source/drain junction of one of the transistors **electrically contacts** the buried oxide layer, as prohibited by the claims.” POR, 23 (emphasis added); POPR (Paper 7), 33. HID’s argument remains flawed.

A. HID's Argument Misrepresents the Requirements of the Claim.



Claim 1, from which claim 3 depends, recites “a transistor having a source/drain junction that **does not contact** said buried oxide layer, thereby forming a source/drain junction capacitance.” (emphasis added). In its Institution Decision, the Board rejected HID’s argument that *Yu* does not satisfy this limitation “[b]ecause the source region of the first transistor 100 is doped N+, and is partially located in the N-Well 44; it is, in fact, electrically in contact with the buried oxide layer as prohibited by Claim 1 of the ’886 Patent.” POR, 25.

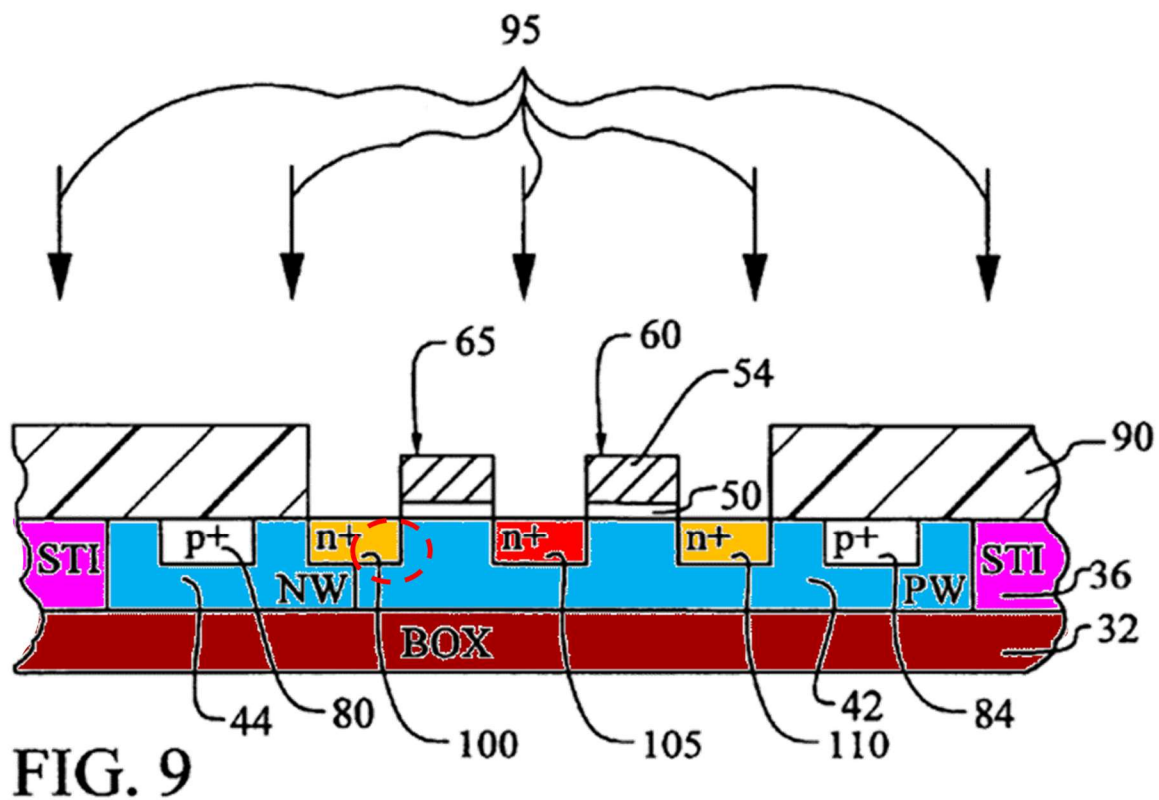
In rejecting HID’s argument, the Board found that the ’886 Patent precludes “*physical* contact,” not electrical contact. Paper 9 (“DI”), 23 (emphasis in original). The Board invited HID to submit “sufficient evidence of record to support its

position and persuasively rebut Petitioner’s evidence of record” if its position is that the alleged electrical connection prevents the formation of the required capacitance. *Id.* at 24. Rather than take up the Board’s invitation, HID simply reiterated its previous argument that “the doped region 100 (the N+ well) *does* electrically contact the buried oxide layer,” while incorporating Mr. Berg’s opinion repeating the same argument. POR, 26 (emphasis in original); Ex. 2006 (“Berg”), ¶¶61, 63. However, as the Board correctly found, claim 1 only precludes physical contact, not electrical contact. DI, 23. Dr. Berg’s admission confirms that *Yu*’s region 100 does not physically contact the BOX layer. Berg, ¶¶59, 63; POR, 26.

Meanwhile, Mr. Berg, in paragraph 59 of his declaration—which is not cited or incorporated into the POR—claims that due to the presence of N-well 44, “transistor 65 does not have a source/drain junction capacitance even though neither the source, nor the drain, contacts the buried oxide layer.” Berg, ¶59. HID failed to preserve this argument by omitting it from the POR. Therefore, the Board should disregard any argument relying solely on uncited portions of the declaration. The Federal Circuit and the Board have consistently held that arguments must appear in the briefs themselves and cannot be incorporated by reference from other documents. *See Blackberry Corp. v. Mobilemedia Ideas LLC*, IPR2013-00016, Paper 32 at 21 (P.T.A.B. Feb. 25, 2014); *Cisco Systems, Inc. v. C-*

Cation Technologies, LLC, IPR2014-00454, Paper 12 at 10 (P.T.A.B. Aug. 29, 2014); see Monsanto Co. v. Scruggs, 459 F.3d 1328, 1336 (Fed. Cir. 2006).

Moreover, as Dr. Thompson explains, Mr. Berg's assertion is incorrect. *Yu's* n+ doped region 100 is partially formed on p-well 42 and partially within n-well 44. *Yu*, 5:9-10. The portion of the n+ doped region overlapping p-well 42 (circled below using a dashed red line) forms a pn junction, which under operating conditions generates a depletion region and consequently a junction capacitance across the depletion region. Thompson-Supp, ¶¶5-9; Ex. 1011, 10, 11; *see* Ex. 1010, 43, 45.



Additionally, HID’s implied interpretation—that claim 1 requires both n⁺ doped regions 100 and 105 (source junction and the drain junction) of *Yu*’s transistor to not contact the buried oxide layer—is inconsistent with the plain language of the claim and the specification.

Claim 1 recites “a transistor having a source/drain junction that does not contact said buried oxide layer” (emphases added). The term “a source/drain junction” requires only one of the source junction or the drain junction, not both. Therefore, each transistor only requires either region 100 or region 105 not to contact the buried oxide layer. Three recognized principles support this interpretation.

First, as explained previously, the Federal Circuit has consistently held that in patent parlance, “a” means “one or more,” unless the specification clearly indicates a contrary intent. *KCJ*, 223 F.3d at 1356; *AbTox*, 122 F.3d at 1043.

Second, the use of a slash (“/”) between “source” and “drain” signals a disjunctive relationship—understood to mean “source or drain”—rather than a conjunctive one (source and drain). A slash (/) is used in technical writing to denote alternatives. Ex. 1030, 269 (6.112) (explaining that a slash between two terms signals a disjunctive relationship, functioning like “or”); *see also* Ex. 1031, 734 (“N. Virgule [/]”).

Third, the term “junction” is singular, indicating that the claim refers to a single junction, which may be either a source junction or a drain junction. Taken together, the indefinite article, the disjunctive slash, and the singular noun all point to a construction that only requires either the source junction or the drain junction (rather than requiring both) to not contact the buried oxide layer.

This interpretation aligns with the disclosure of the '886 Patent and reflects the patentee's intent. The specification distinguishes between singular and plural usage: when referring to one junction, it uses the singular form; when referring to both, it uses the plural. For example, “Each such semiconductor junction will have an associated junction capacitance, e.g. the source/drain junctions of transistor 212 have corresponding source/drain junction capacitances.” '886 Patent, 4:15-18. In contrast, claim 1 intentionally uses the singular: “a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance.” This deliberate phrasing indicates that the claimed invention covers configurations where either the source junction or the drain junction—without requiring both—lacks contact with the buried oxide layer, allowing a capacitance to form at that isolated junction.

Accordingly, even assuming—as HID alleges—that *Yu*'s region 100 contacts the buried oxide layer, region 105 does not. As a result, even under HID's restrictive reading, *Yu*'s cascaded transistors satisfy the requirements of claim 1.

VI. Ground 5: *Burgener* and *Okashita* Renders Obvious Claims 3 and 8-19.

Regarding Ground 5, HID argues that there would have been no motivation to combine *Burgener* and *Okashita*, and the resulting combination would not have taught claim 3. POR, 27-35. Both of HID's arguments are incorrect.

A. HID's Reliance on *Burgener-II* is Misplaced.

First, HID argues that a POSITA would not have been motivated to adopt *Okashita*'s SOI configuration to fabricate *Burgener*'s FETs, as proposed in the Petition. Instead, HID maintains that a POSITA would have favored ultra-thin silicon-on-sapphire (SOS) technology, as described in *Burgener-II* (Ex. 2004) (a reference cited in *Burgener*). POR, 27-32. But this is legally irrelevant.

HID previously raised this same argument in its Preliminary Response (POPR, 35-39), and the Board rejected it, explaining that "even if the ultrathin technique is preferred, it is well settled that an expression of preferences does not teach away from alternatives." DI, 26-27. Consistent with the Board's finding, the Federal Circuit has repeatedly held that obviousness does not require the best solution, but only requires that the proposed solution yields predictable results and that a POSITA would have had reason to pursue it. Thus, HID's assertion that a POSITA would have preferred *Burgener-II*'s technology over *Okashita*'s technology is legally irrelevant.

B. HID’s Argument Against Motivation to Combine Distorts *Okashita*’s Teachings.

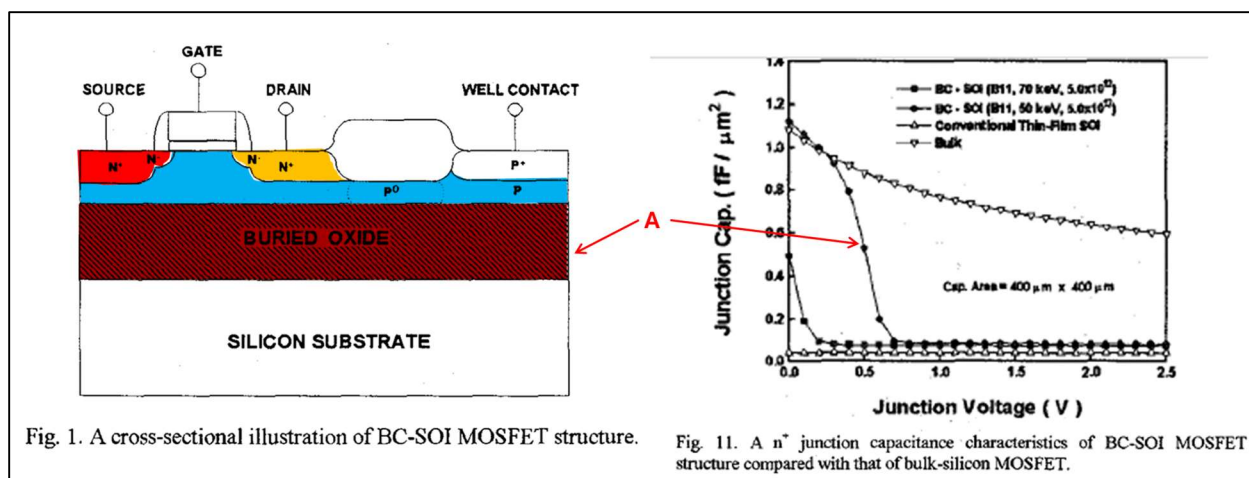
HID and Mr. Berg contend that, because of *Burgener*’s preference for Burgener-II’s UTSi technology, a POSITA would have disregarded *Okashita*, which purportedly features a “relatively thick silicon on top of a buried oxide layer, as shown in *Okashita* and as claimed by Dr. Thompson.” See POR, 32; Berg, ¶¶70. However, *Okashita* does not disclose the thickness of silicon layer 23 above its buried oxide layer 22, nor does it describe the silicon layer as “relatively thick” compared to the layer in Burgener-II, which is “less than 150 nm.” Ex. 2004, 10:62-63. Dr. Thompson likewise made no such characterization. To the extent HID is relying on *Okashita*’s figures to argue that the thickness of *Okashita*’s silicon layer is significantly different, such reliance is misplaced. Patent drawings are not drawn to scale unless explicitly stated. See *Hockerson-Halberstadt, Inc. v. Avia Grp. Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000) (“Patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent.”).

C. HID’s Capacitance-Based Objections Are Grounded in Uncorroborated Testimony from Mr. Berg.

HID contends that a POSITA would have lacked motivation to adopt *Okashita*’s SOI configuration—despite the Petition’s rationale (Pet., §V.E.2; Thompson, ¶¶211–221)—because it might increase source/drain junction

capacitance and “would create a slower switching circuit,” or “lead[] to decreased performance” that a POSITA would aim to avoid. *See* POR, 28-29, 32. But its claim—that incorporating *Okashita*’s SOI technology would create a slower switching circuit (and lead to decreased performance) —is based solely on Mr. Berg’s declaration, which merely reiterates HID’s arguments without offering any independent analysis or supporting evidence. *See* Berg, ¶¶66, 70.

Notably, *Burgener* does not suggest that increased capacitance would create a slower switching circuit or lead to decreased performance. Mr. Berg offers no explanation for why it would, especially when the ’886 Patent suggests otherwise. *See* ’886 Patent, 5:66–6:10 (explaining that the buried oxide and bulk silicon layers beneath the silicon layer helps reduce the capacitive load caused by increased junction capacitance). Additionally, Dr. Thompson presented data (see below) that shows junction capacitance in a transistor similar to *Okashita*’s transistor decreases as junction voltage increases, suggesting that a POSITA would be aware of techniques to mitigate any negative effects from increased junction capacitance. Thompson, ¶48; Thompson-Supp, ¶¶10-16.



Ex. 1014, 2 (Fig. 1), 5 (Fig. 11). As established in *Rohm and Haas Co. v. Brotech Corp.*, 127 F.3d 1089, 1092 (Fed. Cir. 1997), expert opinions must be grounded in specific evidence—not speculation. Contrary to HID’s unsupported claims, a POSITA would have recognized that any increase in capacitance is a predictable and can be managed through known design optimization.

D. Mr. Berg’s Unsupported and Conclusory Opinion Regarding Heat Dissipation Fails to Rebut Dr. Thompson’s Evidence-Based Opinion

HID and Mr. Berg assert that, contrary to Dr. Thompson’s opinion (Thompson, ¶¶213-214), a POSITA would lack motivation to add a silicon layer between *Burgener*’s transistor junctions and the buried oxide layer—based on *Okashita*’s teachings—to reduce operating temperature, because *Burgener* does not disclose that its antenna switch 1700 has thermal concerns, and further allege that such a modification would “dissipate additional heat in the transistors.” POR, 32-33; Berg, ¶71.

Even if *Burgener* does not expressly identify thermal management as a design concern, a POSITA would nonetheless have been motivated to incorporate *Okashita*'s SOI transistor teachings based on their general knowledge of the art. Courts have consistently held that obviousness may be supported by the knowledge of a POSITA even if the prior art does not explicitly state the problem being solved. *See KSR*, 550 U.S. at 418-420. A POSITA would have known that in high power switching circuits of mobile devices, such as *Burgener*'s antenna switch 1700, where power density and switching speed are important, thermal management of transistors is a routine design consideration. Thompson-Supp, ¶17; *see Burgener*, ¶¶[0005]-[0009]. Therefore, HID's argument that a POSITA would lack motivation due to the absence of express disclosure of thermal concerns in *Burgener* is unfounded.

HID's assertion that incorporation of an intervening silicon layer in *Burgener* would dissipate additional heat in the transistors (POR, 33) is speculative and contrary to basic semiconductor physics because, as Dr. Thompson explained, a POSITA would have understood that thermal conductivity is an important factor in managing heat flow away from active regions. Thompson, ¶¶51, 214; Thompson-Supp, ¶18. This Board should disregard it.

In contrast, Dr. Thompson's opinion is grounded in well-established physical principles and supported by evidence. Silicon has a thermal conductivity

roughly 100 times greater than silicon dioxide. Ex. 1013, 27–28; Thompson, ¶51.

As Dr. Thompson explained, inserting a silicon layer between the source/drain junctions and the buried oxide layer improves heat dissipation, which helps lower transistor operating temperatures and enhances reliability. Thompson, ¶¶51, 214; Thompson-Supp, ¶19. This aligns with *Okashita*'s teachings and reflects the motivations of a POSITA seeking to reduce temperature in *Burgener*'s switch 1700. The Board should credit Dr. Thompson's evidence-backed testimony over Mr. Berg's unsupported testimony.

E. HID's Substrate-Based Objections Do Not Refute the Petition's Motivation to Combine.

HID's reliance on Burgener-II's SOS technology (*see* POR, 32) does not undercut or diminish the motivations identified in the Petition. Pet., §V.E.2; Thompson, ¶¶211–218. SOS merely substitutes sapphire for the buried silicon oxide layer of *Okashita*'s SOI substrate, while maintaining the same core architecture. *See* Ex. 1010, 28-30; Ex. 1026, 1-7. A POSITA would have recognized that incorporating an intervening silicon layer between the source/drain junction and the insulator layer would result in lower device operating temperatures, regardless of whether the buried insulator is silicon oxide or sapphire. Since sapphire also has a significantly lower thermal conductivity than

silicon (Ex. 1027, ¶¶0041]), this motivation holds whether the insulator layer is SOI or SOS. Thompson-Supp, ¶¶20-22.

Fig. 9

Similar to *Okashita*'s SOI substrate, UTSi technology features a silicon layer—used to form CMOS devices—positioned over a sapphire substrate. *See* Ex. 2004, 9:57–67. Accordingly, a POSITA would have been motivated to incorporate

Okashita's trench isolation in *Burgener*, regardless of whether its substrate is SOI (as in *Okashita*) or sapphire (as in SOS-UTSi), to mitigate leakage through the device layer above the buried insulating layer.

Furthermore, *Burgener-II* discloses that its UTSi layer should be configured such that "the conduction path of any inter-device leakage current must pass through the [insulating] substrate." Ex. 2004, 9:57–67. A POSITA would understand that implementing *Okashita*'s trench isolation around CMOS devices formed in the silicon layer would effectively block lateral leakage through the silicon layer, thereby ensuring that any leakage current would be forced to traverse the insulating substrate to propagate. Accordingly, contrary to the assertions of HID and Mr. Berg, a POSITA would have even greater motivation to incorporate *Okashita*'s trench isolation around *Burgener*'s FETs if *Burgener*'s circuit 1700 is fabricated using SOS-UTSi technology, as HID alleges. Thompson-Supp, ¶23.

HID also alleges reliance on hindsight and argues that a POSITA would not have been motivated to locate a set of *Burgener*'s FETs together in an isolated region surrounded by a trench because it would increase the space needed for the circuit. POR, 34; Berg, ¶73. Contrary to this assertion, the Petition relies on multiple prior publications that explicitly disclose the performance benefits of isolating transistor groups. See Thompson, ¶¶52-60, 167-168, 217.

Mr. Berg’s assertion that adding trenches to *Burgener*’s circuit 1700 would increase its size (Berg, ¶73) is speculative and unsupported by the record. It also is contrary to what a POSITA would have known. Thompson-Supp, ¶24. A POSITA would have recognized that integrated microelectronic circuits require electrical isolation between adjacent semiconductor devices, which is typically achieved by either junction isolation or trench isolation. Thompson-Supp, ¶24; Ex. 1010, 34-36; Ex. 1028, 1; Ex. 1029, 1:16-22. A POSITA would also have known that trench isolation is known to reduce the size of the circuit compared to junction isolation and thereby lower die size and cost. Thompson-Supp, ¶24; Ex. 1010, 34–36; Ex. 1028, 1. These established principles contradict Mr. Berg’s unsupported opinion, which the Board should disregard. *See Rohm & Haas*, 127 F.3d at 1091-92.

Furthermore, even if the proposed combination introduced some layout tradeoff, a POSITA would be expected to evaluate that tradeoff in light of the performance benefits disclosed in the prior art. As the Federal Circuit has emphasized, “A person of ordinary skill in the art is also a person of ordinary creativity, not an automaton.” *KSR*, 550 U.S. at 421; *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021) (“It’s not necessary to show that a combination is ‘the best option, only that it be a suitable option.’”); *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006) (finding the presence of disadvantages “does not necessarily obviate motivation to combine”). HID’s argument therefore

fails to rebut the clear and well-supported rationale for the proposed combination set forth in the Petition.

F. HID's Claim 3 Argument Fails.

HID's claim 3 argument is premised on its Ground 2 argument, and it fails for the same reasons as HID's Ground 2 argument. *Supra* III.

VII. Ground 6: *Burgener, Okashita, and Yu* Render Obvious Claims 3 and 8-19.

A. HID's Arguments Mirror Those in Ground 5 and Fail for the Same Reasons.

HID relies on the same arguments for Ground 6 as it does for Ground 5.

POR, 35. These arguments fail for the same reasons provided above in Section VI.

VIII. Conclusion

For the reasons set forth above, and in the Petition, the challenged claims should be canceled.

Respectfully submitted,

Dated: October 9, 2025

By: / Joshua L. Goldberg / _____
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(c)(1), the undersigned hereby certifies that the foregoing Petitioner's Reply to Patent Owner's Response contains 5,178 words, excluding the parts exempted under 37 C.F.R. § 42.24(c) as measured by the word-processing system used to prepare this paper.

Dated: October 9, 2025

By: / Joshua L. Goldberg /
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATE OF SERVICE

The undersigned hereby certifies that a copy of the foregoing **Petitioner's Reply to Patent Owner's Response** was served on October 9, 2025, via email directed to counsel of record for Patent Owner at the following:

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