

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD,
SAMSUNG ELECTRONICS AMERICA, INC., NXP
SEMICONDUCTORS, N.V.¹

Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Case IPR2024-01402
U.S. Patent No. 7,745,886

PETITIONER'S UPDATED EXHIBIT LIST

¹ NXP Semiconductors N.V. filed a petition and a motion for joinder in IPR2025-00954 that were granted and have been joined as petitioners in this proceeding.

Pursuant to 37 C.F.R. § 42.63(e), Petitioner Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. hereby submits a current listing of Petitioner exhibits. Exhibits 1026-1031 are being filed today.

Exhibit	Description
1001	U.S. Patent No. 7,745,886 to Zwingman (“’886 patent”)
1002	Declaration of Scott Emmet Thompson, Ph.D. (“Thompson”)
1003	Prosecution History of the ’886 patent (downloaded from Public PAIR)
1004	U.S. Patent No. 6,836,172 to Okashita et al. (“ <i>Okashita</i> ”)
1005	U.S. Patent No. 6,737,682 to Yu (“ <i>Yu</i> ”)
1006	U.S. Patent Publication No. 2006/0270367 to Burgener et al. (“ <i>Burgener</i> ”)
1007	Webster’s Ninth New Collegiate Dictionary, Merriam-Webster, Inc., Springfield, Massachusetts, U.S.A., 1985, p. 211.
1008	“Fundamentals of Semiconductor Physics and Devices,” Rolf Enderlin and Norman J.M. Horing, World Scientific, 1996, pp. 535-539, 620-622.
1009	“Electronics Circuits and Analysis,” Dinesh C. Dube, Alpha Science International Ltd., 2005, pp. 202-207.
1010	“SOI Design: Analog, Memory and Digital Techniques,” Andrew Marshall and Sreedhar Natarajan, Kulwer Academic Publishers, 2003, pp. 1-46, 75-84, 125-179, 289-338, 340-358.
1011	“CMOS Logic Circuit Design,” John P. Uyemura, Kluwer Academic Publishers, 2002, pp. 1-2, 19, 35-36, 78-83, 94-96, 359-362.

Exhibit	Description
1012	“The Stuff Dreams Are Made Of [Part 1],” Paul DeMone, May 8, 2002, Available at: https://www.realworldtech.com/cmos-basics
1013	“SOI for Digital CMOS VLSI: Design Considerations and Advances,” Ching-Te Chuang et al., Proceedings of the IEEE, Vol. 86, No. 4, April 1998, pp. 689-720.
1014	“1 Giga bit SOI DRAM with fully bulk compatible process and body-contacted SOI MOSFET structure,” Yo-Hwan Koh et al., 1997 International Electron Devices Meeting Technical Digest, Washington, DC, USA, 1997, pp. 579-582.
1015	U.S. Patent No. 6,121,148 to Bashir et al. (“Bashir”), published September 19, 2000.
1016	“Speeding up Transistors: IBM to Make SOI Chips,” Katherine Derbyshire, Semiconductor Online, August 18, 1998.
1017	“SOI-CMOS Device Technology,” Yasuhiro Fukuda, et al., Special Edition on 21st Century Solutions, OKI Technical Review 185, Vol. 68, March 2001, pp. 54-57.
1018	“Impact of high-k gate stack material with metal gates on LF noise in n- and p-MOSFETs,” P. Srinivasan et al., Microelectronic Engineering 80 (2005) 226–229.
1019	U.S. 2004/0150045 A1 to Nonaka et al., published August 5, 2004 (“Nonaka”).
1020	U.S. Patent No. 6,498,371 B1 to Krishnan et al., published December 24, 2002 (“Krishnan”).
1021	U.S. Patent No. 6,933,569 B2 to Koh et al., published August 23, 2005 (“Koh”).
1022	“Temperature-Dependent Thermal Conductivity of Single-Crystal Silicon Layers in SOI Substrates,” M. Asheghi et al., Transactions of the ASME, Journal of Heat Transfer, Vol. 120, February 1998, pp. 30-36.

Exhibit	Description
1023	“Current Mode Digital Gates for Mixed Mode Reprogrammable Integrated System,” P. Pawlowski, Proceedings of the 1st IEEE International Conference on Circuits and Systems for Communications, 26-28 June, 2002, St. Petersburg State Polytechnic University Publishing House, 2002, pp. 178-181.
1024	<i>Harbor Island Dynamic, LLC v. Samsung Electronics Co. Ltd. et al</i> , Case No. 2:24-cv-00140, Plaintiff’s Infringement Contentions Cover Pleading (July 18, 2024)
1025	<i>Harbor Island Dynamic, LLC v. Samsung Electronics Co. Ltd. et al</i> , Case No. 2:24-cv-00140, Dkt. No. 38, Docket Control Order (E.D. Tex. August 2, 2024)
1026	Supplemental Declaration of Scott Emmet Thompson, Ph.D. in Support of Petition for Inter Partes Review of United States Patent No. 7,745,886 (“Thompson-Supp”)
1027	European Patent 2,220,697 B1, McKenzie et al., published November 9, 2019
1028	“Modeling and characterization of deep trench isolation structures,” S. Lee, Microelectronics Journal 32 (2001) pp. 295-300.
1029	U.S. Patent No. 4,786,960 to Jeuch, published November 22, 1988.
1030	Chicago Manual of Style, 15 th ed., (2003), pp. 268-70.
1031	Garner’s Dictionary of Legal Usage, Bryan A. Garner, 3d ed. (2011), pp. 730-34.

Respectfully submitted,

Dated: October 9, 2025

By: / Joshua L. Goldberg / _____
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATE OF SERVICE

The undersigned hereby certifies that a copy of the foregoing **Petitioner's Updated Exhibit List** and **Exhibits 1026-1031** were served on October 9, 2025, via e-mail directed to counsel of record for the Patent Owner at the following:

Joseph M. Mercadante
Alfred R. Fabricant
Richard Cowell
FABRICANT LLP
411 Theodore Fremd Avenue,
Suite 206 South
Rye, New York 10580
jmercadante@fabricantllp.com
ffabricant@fabricantllp.com
rcowell@fabricantllp.com
PTAB@fabricantllp.com

**Counsel for Patent Owner
Harbor Island Dynamic, LLC**

Eagle H. Robinson
Eric C. Green
NORTON ROSE FULBRIGHT US LLP
98 San Jacinto Boulevard, Suite 1100
Austin, TX 78701
eagle.robinson@nortonrosefulbright.com
eric.green@nortonrosefulbright.com

Richard S. Zembek
NORTON ROSE FULBRIGHT US LLP
1550 Lamar Street, Suite 2000
Houston, TX 77010
richard.zembek@nortonrosefulbright.com

Jiang Wu
NORTON ROSE FULBRIGHT US LLP

1045 W. Fulton Market
Chicago, IL 60607
jiang.wu@nortonrosefulbright.com

Counsel for Petitioner
NXP Semiconductors N.V.

Dated: October 9, 2025

/ William Esper /
William Esper
Senior Litigation Paralegal
Finnegan, Henderson, Farabow,
Garrett & Dunner LLP