

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD, AND
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Case No. IPR2024-01402
U.S. Patent No. 7,745,886

**SUPPLEMENTAL DECLARATION OF SCOTT E. THOMPSON, Ph.D.
IN SUPPORT OF PETITION FOR INTER PARTES REVIEW OF
UNITED STATES PATENT NO. 7,745,886**

TABLE OF CONTENTS

I.	Introduction.....	1
II.	Materials Considered	1
III.	Mr. Berg’s Assertion That Transistor 65 in <i>Yu</i> Lacks Source/Drain Junction Capacitance Is Incorrect.....	2
IV.	Junction Capacitance Does Not Undermine Motivation to Combine <i>Okashita</i> with <i>Burgener</i>	5
V.	Absence of Express Thermal Concerns in <i>Burgener</i> Does Not Preclude Motivation.....	10
VI.	Silicon Interlayer Reduces Operating Temperature in SOI Devices.....	11
VII.	Trench Isolation Reduces Leakage in SOI Devices.	12
VIII.	Conclusion	16

I. Introduction

1. I, Scott E. Thompson, Ph.D., provide the following supplemental declaration in connection with IPR2024-01402 concerning U.S. Patent No. 7,745,886 (“the ’886 patent”) (Ex. 1001).

2. I have been retained as an independent expert by Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. (“Petitioner” or “Samsung”). Previously, I submitted an opening declaration (Ex. 1002 (Thompson)) in support of Samsung’s Petition for *Inter Partes* Review.

3. I submit this supplemental declaration in response to the Patent Owner’s Response (“POR”) (Paper 18) filed by Harbor Island Dynamic, LLC (“Patent Owner” or “HID”). I was asked to address certain arguments raised by HID’s POR, as well as certain testimony provided by HID’s expert, Mr. John Berg, in his declaration (Ex. 2006). My lack of direct response to other points or issues raised in the POR or by Mr. Berg’s declaration should not be construed as agreement or admission. Nothing in the POR or Mr. Berg’s declaration changes the opinions that I expressed in my opening declaration.

II. Materials Considered

4. In forming my opinions in this supplemental declaration, I have reviewed and considered the Board’s Institution Decision (Paper 9), HID’s POR, Mr. Berg’s declaration, and all of the materials cited therein. I have further relied

upon my experience, professional background, and knowledge of the relevant art, as detailed in my opening declaration and curriculum vitae. All of the foregoing are incorporated herein by reference. In addition, I have relied upon the materials considered in my opening declaration (Thompson, §IV), as well as the additional documents listed below.

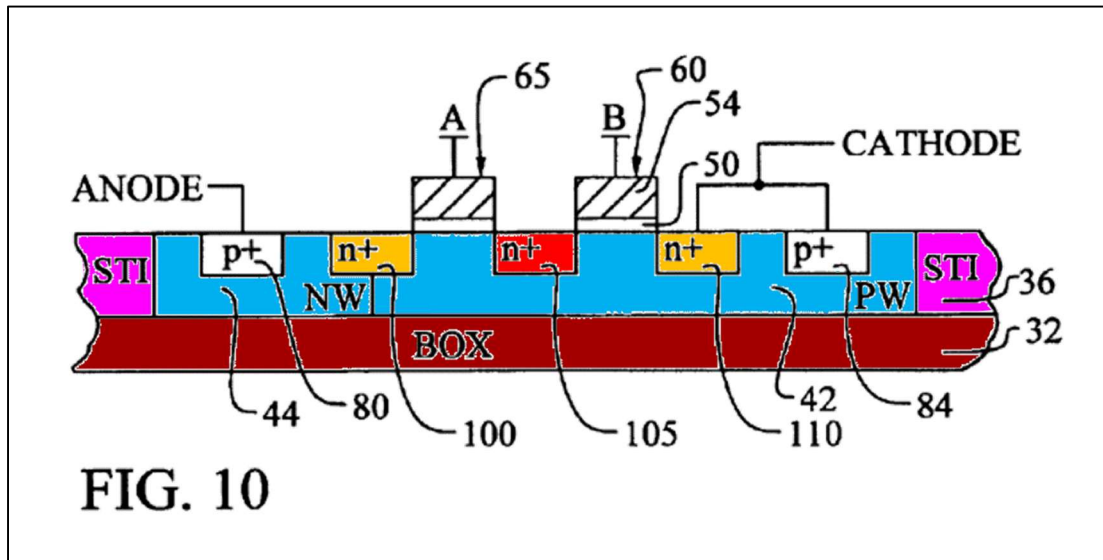
Exhibit	Description
Ex. 1027	European Patent 2,220,697 B1, McKenzie et al., published November 9, 2019.
Ex. 1028	“Modeling and characterization of deep trench isolation structures,” S. Lee, Microelectronics Journal 32 (2001) pp. 295-300.
Ex. 1029	U.S. Patent No. 4,786,960 to Jeuch, published November 22, 1988.
Ex. 1030	Chicago Manual of Style, 15 th ed., (2003), pp. 268-70.
Ex. 1031	Garner’s Dictionary of Legal Usage, Bryan A. Garner, 3d ed. (2011), pp. 730-34.

III. Mr. Berg’s Assertion That Transistor 65 in *Yu* Lacks Source/Drain Junction Capacitance Is Incorrect.

5. Mr. Berg contends that, in *Yu*, the presence of N-well 44 means “transistor 65 does not have a source/drain junction capacitance, even though neither the source nor the drain contacts the buried oxide layer.” Berg, ¶59. I disagree, as this assertion contradicts what a POSITA would commonly understand.

6. In *Yu*, a first transistor is formed by a gate 60, an N+ doped region 110, and an N+ doped region 105. *Yu*, 5:10-12, 44-46. And a second transistor,

connected in series with the first transistor, is formed by a gate 65, an N+ **doped region 105**, and an N+ **doped region 100**. *Yu*, 5:10-12, 44-57. *Yu* discloses that “[t]he doped regions ... 100, 105, and 110 ... do not extend to the **buried oxide layer 32**.” *Yu*, 6:46-49.



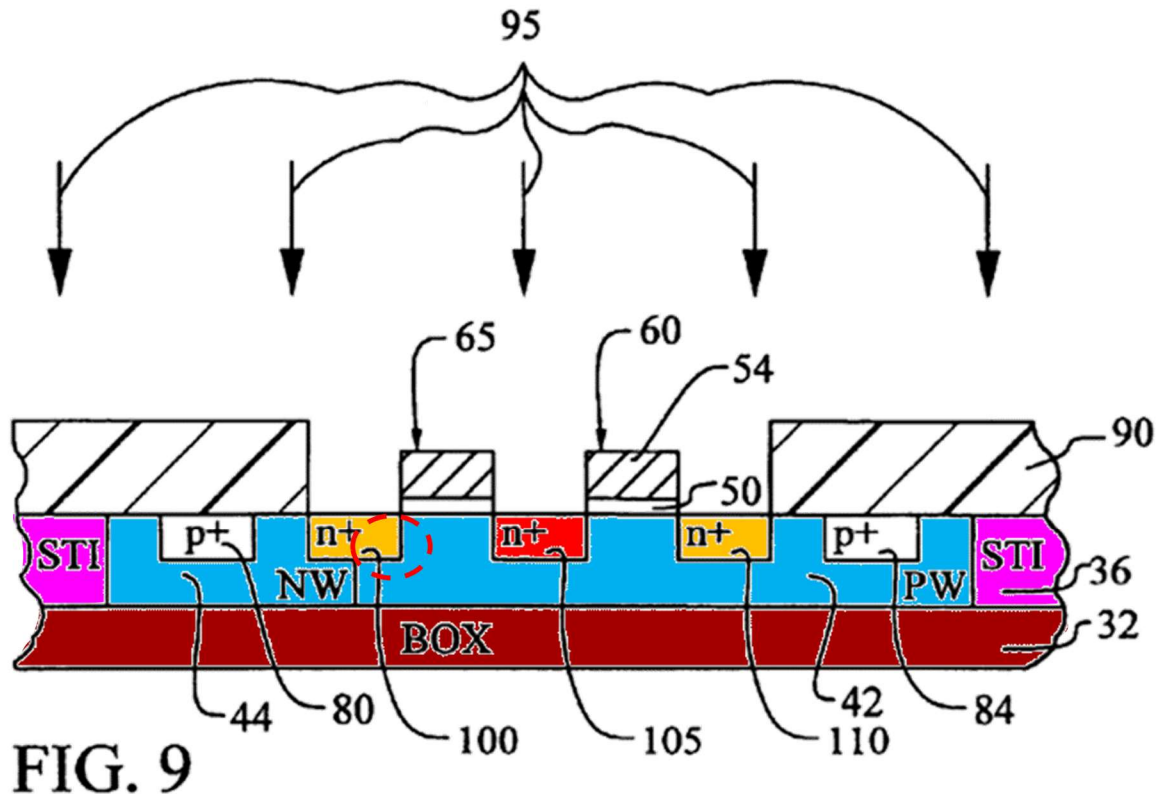
Yu, Fig. 10 (annotated).

7. These N+ doped regions **100**, **105**, and **110** serve as the **source** and **drains** of the first and second transistors. See *Yu*, 6:40-45. The specific N+ doped region that acts as the **source** and the **drain** depends on the biasing conditions during operation of the transistor. The doped region (or terminal) through which the charge carriers enter the transistor is the source and the doped region through which the charge carriers exit the transistor is the drain. Regardless of which doped regions act as the source and the drain, the interfaces between these doped regions

and the underlying silicon layer form source/drain junctions. *Yu*, 6:40-45, Fig. 11; *see* Ex. 1011, 10, 11.

8. *Yu* discloses that the N+ doped region 100 of its second transistor “is formed partly in the first well 42 and partly in the second well 44” and N+ doped region 105 is formed in the first well 42. *Yu*, 5:7-10. The first well 42 is a p-type p-well and the second well 44 is an n-type n-well. *Yu*, 4:17-20. I will refer to the first well 42 as a p-well 42 and the second well 44 as an n-well 44.

9. A POSITA would understand that, during operation of *Yu*’s second transistor, source/drain junction capacitance arises from the PN junctions formed between the N+ doped regions 100 and 105 (serving as the drain and source, respectively) and the underlying p-well 42. This capacitance results from the depletion region that develops at the interface between the N+ and P-type materials. Specifically, the portion of N+ region 100 located on the p-well 42 (highlighted with a dashed red circle in the figure below) forms a PN junction. *See* Ex. 1011, 10 (“pn junctions [] are formed by the drain-bulk and source-bulk interfaces in a MOSFET”), 11 (Fig. 1.36). A POSITA would also recognize that, during transistor operation, a depletion region forms at the interface between N+ region 100 and the p-well 42, resulting in junction capacitance across that region. *See* Ex. 1011, 10, 11; Ex. 1010, 43, 45.



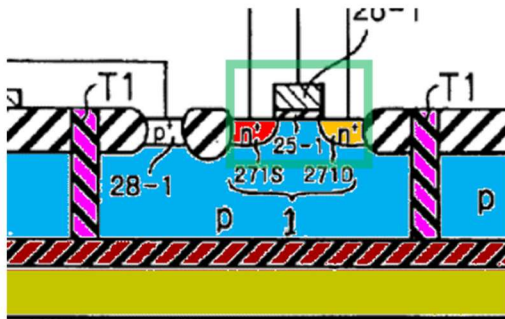
Yu, Fig. 9 (annotated).

IV. Junction Capacitance Does Not Undermine Motivation to Combine *Okashita* with *Burgener*.

10. Mr. Berg asserts that a POSITA would not have been motivated to apply *Okashita*'s SOI fabrication process to *Burgener*'s circuits, arguing that this combination would have increased the source/drain junction capacitance in *Okashita*'s transistor design, which in turn would have led to slower switching and performance degradation in *Burgener*'s device. Berg, ¶66. I disagree.

11. First, I disagree that implementing *Okashita's* teachings in *Burgener's* design would necessarily increase the junction capacitance of *Burgener's* FETs, as

Mr. Berg claims. As I previously explained (Thompson, ¶¶86-87), a POSITA would recognize that *Okashita*'s transistors 1 and 2 are body-tied (or body-contacted) SOI transistors. In these devices, the p-type body (or bulk) of transistor 1 is electrically connected—or “tied”—to a defined voltage through taken-out region 28-1, while the p-type body of transistor 2 is similarly tied via taken-out region 28-2. See *Okashita*, Fig. 9 (reproduced below). Ex. 1014 also reports on the electrical performance and junction capacitance of a body-contacted SOI transistor having a similar structure as *Okashita*'s transistors.



Okashita, Fig. 9

(cropped and enlarged to show transistor 1)

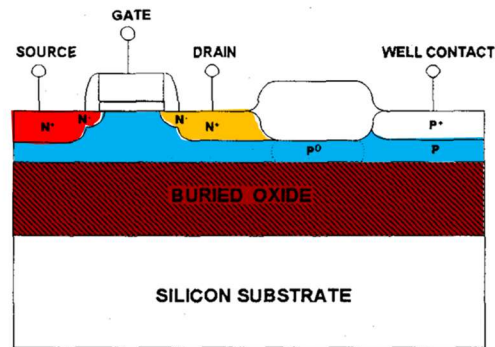


Fig. 1. A cross-sectional illustration of BC-SOI MOSFET structure.

Ex. 1014, Fig. 1

Okashita, Fig. 9 (cropped, enlarged, annotated); Ex. 1014, 3 (Fig. 1) (annotated).

12. Similar to *Okashita*'s transistor 1 (and transistor 2), the body-contacted (“BC”) SOI MOSFET of Ex. 1014 has an n⁺-type source and drain on a p-type silicon body. Additionally, the transistors of both *Okashita* and Ex. 1014 have a silicon between the source/drain junctions and the buried oxide layer, such that the source/drain junctions do not contact the buried oxide layer.

13. At junction voltages below approximately 0.7 volts, as shown in the data presented in Ex. 1014 (Fig. 11, below), the junction capacitance of a body-contacted SOI (BC-SOI) transistor (represented by the curve with data points marked by the symbol •) is higher than that of a thin-film SOI transistor (represented by the curve with data points marked by the symbol Δ). Notably, Mr. Berg characterizes *Burgener*'s transistor as a thin-film SOI transistor. See Berg, ¶¶68, 70. However, at higher junction voltages, the capacitance values of the two transistor types become comparable. While the precise voltage at which this convergence occurs depends on the specific design parameters of the BC-SOI transistor of Ex. 1014, a POSITA would understand from this data that *Okashita*'s body-contacted SOI transistors would similarly exhibit junction capacitance comparable to that of thin-film SOI transistors above a threshold voltage. Therefore, in my opinion, even assuming *Burgener*'s transistors are thin-film SOI devices as Mr. Berg asserts, a POSITA would recognize that implementing *Okashita*'s teachings would only increase junction capacitance if the transistors operate below that threshold voltage. At higher junction voltages, the modified *Burgener* transistors would not experience a significant increase in junction capacitance. Importantly, a POSITA would also understand that the junction capacitance of the modified *Burgener* transistors can be reduced by operating them at higher junction voltages.

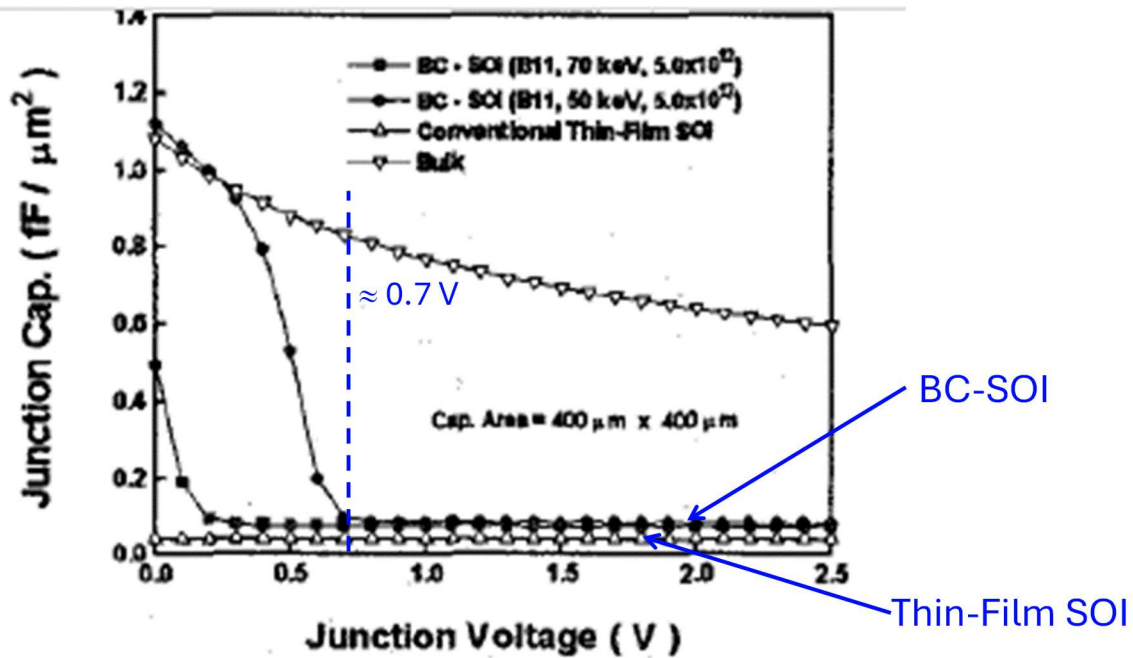


Fig. 11. A n^+ junction capacitance characteristics of BC-SOI MOSFET structure compared with that of bulk-silicon MOSFET.

Ex. 1014, 5 (Fig. 11) (annotated).

14. Similarly, based on the data presented in Ex. 1014 (below), a POSITA would understand that the gate-delay time of *Okashita's* body-contacted SOI (BC-SOI) transistors is slightly higher than that of thin-film SOI transistors at supply voltages below approximately 2.25 volts. However, at higher supply voltages, the delay times of the two transistor types become comparable. Ex. 1013 also reports a similar behavior of gate-delay time. Ex. 1013, 26 (Fig. 48). Therefore, even assuming *Burgener's* transistors are thin-film SOI devices, as Mr. Berg asserts, a POSITA would recognize that implementing *Okashita's* teachings in *Burgener's* design would result in only a small increase in delay time at low

supply voltages, and no significant increase at higher voltages. Moreover, a POSITA would understand that delay time can be reduced by operating the transistors at higher supply voltages.

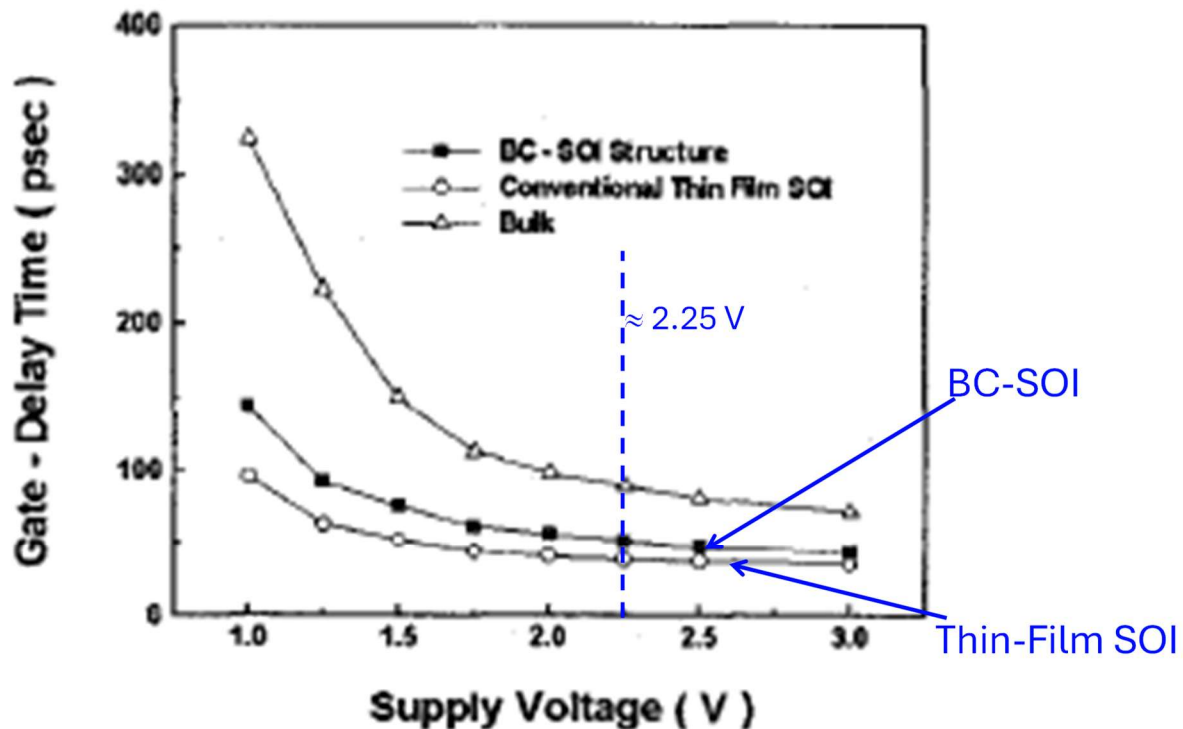


Fig. 12. Gate-delay time characteristics with supply voltage with field-stop implantation condition as a parameter with conventional and bulk counterparts.

Ex. 1014, 5 (Fig. 12) (annotated).

15. Furthermore, contrary to Mr. Berg's assertions, Ex. 1014 discloses that body-contacted SOI transistors, such as *Okashita's* transistors, offer several advantages over conventional thin-film SOI transistors. For instance, Ex. 1014 discloses that BC-SOI transistors exhibit a "relatively high isolation punchthrough voltage, high drain-to-source breakdown voltage compared with conventional thin-

film SOI MOSFET and [a] small junction capacitance compared with bulk MOSFET, resulting in high-speed circuit operation.” Ex. 1014, 2.

16. Therefore, in my opinion, even assuming that implementing *Okashita*’s teachings in *Burgener*’s transistors would increase junction capacitance as Mr. Berg contends, this would not have discouraged a POSITA from incorporating those teachings into *Burgener*’s design, as I previously explained. See Thompson, §XI.E. This is because a POSITA would have recognized the advantages of *Okashita*’s body-contacted SOI transistors over *Burgener*’s transistors and would also have been aware of established techniques to mitigate any increase in junction capacitance.

V. Absence of Express Thermal Concerns in *Burgener* Does Not Preclude Motivation.

17. Mr. Berg contends that a POSITA would lack motivation to apply *Okashita*’s teaching of inserting a silicon layer between the source/drain junctions and the buried oxide in *Burgener*’s SOI transistors to reduce operating temperature, because *Burgener* does not disclose any thermal concerns with its antenna switch 1700. Berg, ¶71. *Burgener*’s antenna switch 1700 is a “high power switching circuit[]” of a cellular phone. *Burgener*, ¶¶[0005]-[0006], [0009]. *Burgener* discloses that its device “operate[s] at relatively high frequencies of at least 900 MHz and/or 2.4 GHz,” and that “inductive voltages may greatly exceed the supply voltage.” *Burgener*, ¶¶[0009], [0039], [0101]-[0106]. In my opinion, a

POSITA would have been well aware of the importance of thermal management of the FETs of antenna switch 1700. A POSITA would have known that high-frequency, high-voltage switching generates significant heat, and in compact mobile environments where thermal dissipation is constrained, managing transistor temperatures is important to ensure performance, reliability, and device longevity. *See, e.g.*, Ex. 1010, 59-60, 192; Ex. 1013, 26-28; Ex. 1022, 1. Therefore, in my opinion, even in the absence of an express disclosure of thermal concerns in *Burgener*, a POSITA would recognize that such conditions necessitate thermal design considerations of the FETs.

VI. Silicon Interlayer Reduces Operating Temperature in SOI Devices.

18. Mr. Berg's assertion that incorporation of an intervening silicon layer in *Burgener*, based on *Okashita*'s teachings, would "dissipate additional heat in the transistors" is contrary to basic semiconductor physics in my opinion. As previously explained (*see* Thompson, ¶¶51, 214), a POSITA would have understood that because the source/drain junctions of SOI transistors are in contact with the buried oxide layer—which has a thermal conductivity approximately two orders of magnitude lower than silicon—heat removal is less efficient than when a silicon layer is inserted between the junctions and the buried oxide layer.

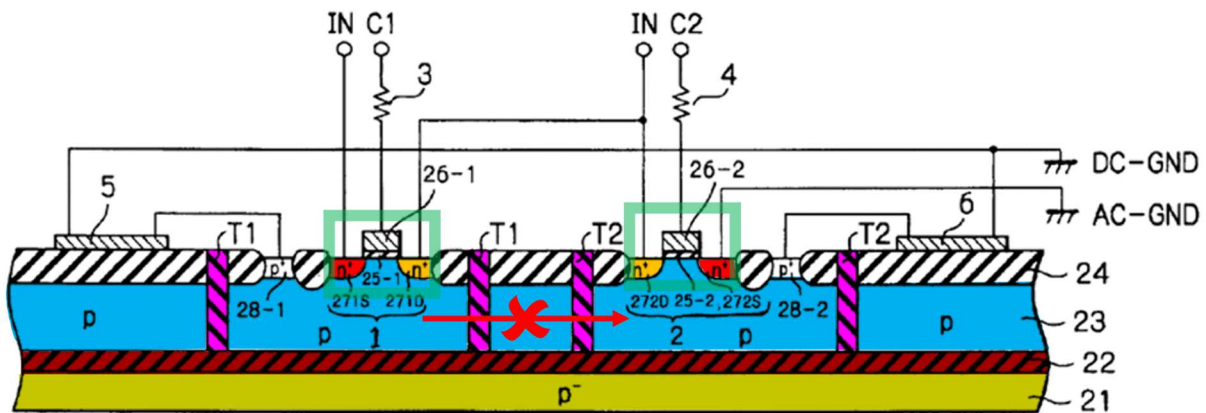
19. Thermal conductivity is a material property that directly influences how efficiently heat is removed from the source/drain junction of a transistor by

conduction. The thermal conductivity of silicon is significantly higher than silicon dioxide and sapphire. Ex. 1013, 27; Ex. 1027, 6-7. Materials with high thermal conductivity, such as silicon, facilitate efficient heat transfer, allowing heat to dissipate quickly from active regions (such as the source/drain junctions) of a device. In contrast, materials like silicon dioxide and sapphire, which have much lower thermal conductivity, impede heat flow. This resistance to heat flow causes heat to accumulate near the heat source, such as the transistor's source/drain junctions, resulting in elevated operating temperatures. Therefore, when a transistor's source/drain junctions are in direct contact with a high-conductivity material like silicon, thermal energy is removed more effectively than when those junctions are in contact with a much lower-conductivity materials like silicon dioxide or sapphire. This is the reason why I believe that introducing a silicon layer between the source/drain junctions and the underlying insulating layer—whether that underlying insulating layer is silicon dioxide (as in *Okashita*) or sapphire (as in *Burgener-II* (Ex. 2004))—enhances heat dissipation and lowers the transistor's operating temperature.

VII. Trench Isolation Reduces Leakage in SOI Devices.

20. Mr. Berg contends that a POSITA would not have been motivated to incorporate trenches around a set of FETs in *Burgener*'s switch to prevent leakage, as I previously explained (*see* Thompson, ¶215). Berg, ¶73. He argues that this is

Fig. 9



22. A POSITA would have understood that a silicon-on-sapphire (SOS) substrate is a type of semiconductor-on-insulator (SOI) substrate, where the buried

oxide (BOX) layer made of silicon dioxide is replaced with sapphire. *See* Ex. 1010, 28–29. Like the SOI substrate in *Okashita*, the SOS substrate used in UTSi technology features a silicon layer—used to fabricate CMOS devices—positioned above an insulating sapphire layer. *See* Ex. 2004, 9:57–67; Ex. 1010, 28–30. Given this structure, a POSITA would have recognized that incorporating trench isolation, as taught by *Okashita*, into *Burgener* would help electrically isolate different sets of transistors and prevent leakage through the shared silicon device layer, regardless of whether the underlying insulator is silicon dioxide or sapphire. Therefore, in my opinion, a POSITA would have been motivated to apply *Okashita*’s trench isolation techniques to *Burgener*’s circuit to mitigate leakage regardless of whether the substrate is SOI or SOS-UTSi.

23. Additionally, *Burgener-II* discloses that its UTSi layer should be configured such that “the conduction path of any inter-device leakage current must pass through the substrate.” Ex. 2004, 9:57–67. A POSITA would understand that implementing *Okashita*’s trench isolation around CMOS devices formed in the silicon layer would effectively block lateral leakage through the silicon layer, thereby ensuring that any leakage current would be forced to traverse the insulating substrate to propagate. Accordingly, in my opinion, a POSITA would have even greater motivation to incorporate *Okashita*’s trench isolation around *Burgener*’s

transistors if circuit 1700 is fabricated using SOS-UTSi technology as Mr. Berg alleges.

24. In my opinion, Mr. Berg's claim that adding trenches in *Burgener* would increase the circuit's footprint is incorrect and inconsistent with what a POSITA would understand. A POSITA would recognize that integrated microelectronic circuits require electrical isolation between adjacent semiconductor devices. *See* Ex. 1010, 34–35; Ex. 1028, 1 (“In integrated microelectronic circuits, electrical isolation is needed between adjacent semiconductor devices.”); Ex. 1029, 1:16–22. This isolation is typically achieved through either junction isolation or trench isolation. *See* Ex. 1010, 34–36; Ex. 1028, 1. It was well known that junction isolation consumes more silicon area than trench isolation. *See* Ex. 1010, 34 (“[Junction isolation) has the disadvantage of requiring a relatively large silicon area to isolate structures.”), 36 (“[Trench isolation) can be significantly more area efficient than junction isolation.”); Ex. 1028, 1 (“If high voltage devices were to be isolated with junction isolation, the inter-device separations would become too large and impractical. Thus, the use of deep trench isolation significantly reduces the device size and the die size, hence reducing the device cost.”). Accordingly, a POSITA would have understood that incorporating trench isolation in *Burgener*—based on *Okashita*'s teachings—

would reduce the size of antenna circuit 1700 (relative to using junction isolation), thereby decreasing die size and cost.

VIII. Conclusion

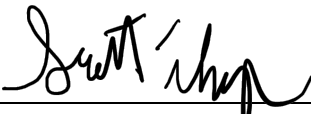
25. For the reasons set forth here and in my opening declaration, it is my opinion that one skilled in the art would have found claims 1–19 of the '886 patent anticipated by or obvious over the prior art.

26. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

27. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: October 8, 2025

Respectfully submitted,



Scott E. Thompson, Ph.D.