

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
SAMSUNG ELECTRONICS AMERICA, INC., AND
NXP SEMICONDUCTORS, N.V.¹

Petitioners,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Patent No. 7,745,886

Filing Date: September 29, 2008

Issue Date: June 29, 2010

Inventors: Robert L. Zwingman and Marco Racanelli
Title: SEMICONDUCTOR ON INSULATOR (SOI)
SWITCHING CIRCUIT

PATENT OWNER'S SUR-REPLY

Case No. IPR2024-01402

¹ NXP Semiconductors N.V. filed a petition and a motion for joinder in IPR2025-00954 that were granted and has been joined as a petitioner in this proceeding.

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LIST OF EXHIBITS

Exhibit No.	Description of Document
2001	Docket Control Order, Dkt. 38, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Aug. 5, 2024)
2002	Order Denying Samsung's Motion to Stay Pending <i>Inter Partes</i> Review, Dkt. 62, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Dec. 19, 2024)
2003	Defendants' Invalidity Contentions, served on September 26, 2024, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex.)
2004	U.S. Patent No. 6,804,502 entitled SWITCH CIRCUIT AND METHOD OF SWITCHING RADIO FREQUENCY SIGNALS to Burgener et al., issued October 12, 2004
2005	Deposition of Scott E. Thompson, Ph.D., taken on June 17, 2025
2006	Declaration of Mr. John Berg
2007	Email from Board authorizing Patent Owner to file a Motion to Amend

I. INTRODUCTION

Petitioner's Reply does nothing to dispel the obvious flaws in its Petition, other than present two new untimely (and incorrect) claim constructions, and present a supplemental expert declaration containing new theories that also do not render the claims anticipated or obvious.

Okashita does not render Claim 3 obvious, because it plainly shows each of the transistors in its own isolated island, rather than on the same isolated island as required by the claim.

Okashita and *Yu* cannot be combined, because they are not analogous art and Petitioner does not provide a sufficient rationale as to how they can be combined.

Yu does not anticipate, because one of the cascaded transistors has a source/drain junction that does not have the capacitance required by the claims.

Okashita cannot be combined with *Burgener*, and Petitioner's belated attempts to fix its Petition should be rejected.

II. LEVEL OF ORDINARY SKILL IN THE ART

HID agrees that, although the parties propose different levels of skill in the art, the distinction between the two proposed levels of skill are immaterial to the disputes raised herein.

III. CLAIM CONSTRUCTION

For the first time on Reply, Petitioner raises two new claim construction arguments.

First, that the “isolated island” in Claim 3 should be construed to mean “one or more” isolated islands so that the prior art showing two transistors located in two separate isolated islands can be shoehorned into the claim, despite obvious claim differentiation principles preventing this.

Second, Petitioner argues that “a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance” should be construed to mean “a source junction or a drain junction.” Both of these arguments fail on the merits, and should also not be considered because they were not included in the Petition. *See* 37 C.F.R. § 42.104(b)(4) (requiring Petition to set forth how the challenged claim is to be construed). Each of these claim construction positions are addressed below in the context of the relevant Grounds.

IV. GROUND 2: CLAIM 3 IS NOT OBVIOUS OVER *OKASHITA*

A. Petitioner’s Interpretation of Claim 3 Is Wrong

Petitioner admits that it has waived any argument that the structure of *Okashita* would have been modified to meet Claim 3. Rather, Petitioner appears to be relying on an unstated claim construction position that Claims 2 and 3 of the ’886

Patent are coextensive. But Petitioner's reading of the claims is incorrect, and because *Okashita* does not disclose the entire plurality of cascaded transistors to be located within the same isolated island, *Okashita* does not render this claim obvious.

Claim 3 of the '886 Patent requires the entire plurality of cascaded transistors to be located within an isolated island, whereas Claim 2 requires each transistor to be in its own isolated island:

1. A switching circuit comprising:

a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;

each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;

at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.

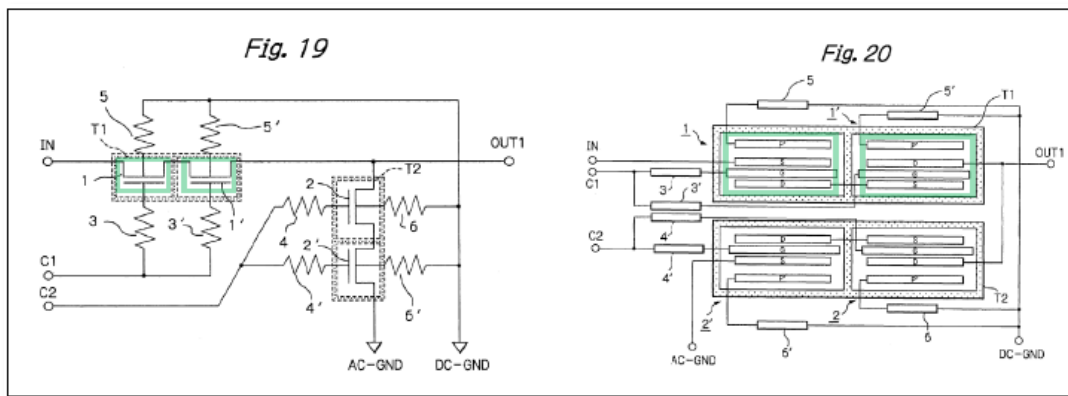
2. The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer.

3. *The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated*

island in said device layer.

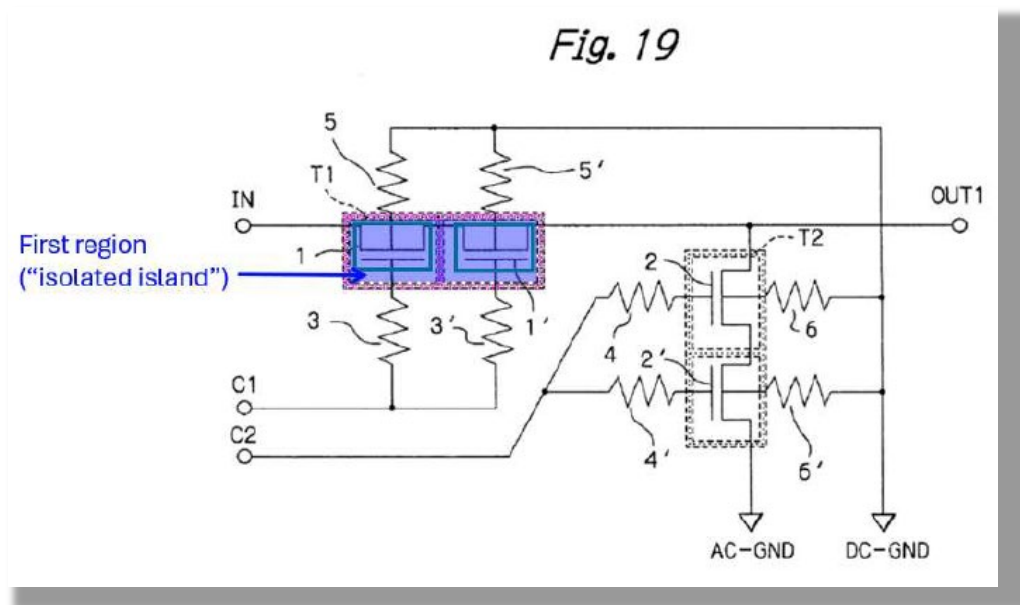
'886 Patent, Claims 1-3 (emphasis added).

The relevant disclosure of *Okashita* is not disputed. Figures 19 and 20 of *Okashita* disclose two transistors, labeled 1 and 1', that are each surrounded by trenches:



Ex. 1002, ¶ 150 (annotating *Okashita* Figs. 19 and 20)

On Reply, Petitioner proposes that the isolation trench separating these transistors can be ignored, and the region containing these two transistors can be characterized as an “isolated island.”



Paper 22 ("Reply") at 3

But an isolated island this is not, because the two transistors are also isolated from one another. Two islands, no matter how close to one another, cannot be a single island; this is true in semiconductor design, as it is true in geography. Petitioner has not presented any claim construction argument or other position that the plain language of the claims or the principles of claim differentiation should be ignored in this instance.

Petitioner also presents a belated claim construction that the "isolated island" in Claim 3 should be construed to mean "one or more" isolated islands. Reply at 4. This argument was not presented in the Petition, despite the obvious logical difference present in *Okashita*, and is therefore waived. A petition is required to

identify “in writing and with particularity . . . the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge to each claim.” 35 U.S.C. § 312(a)(3); *see also Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016). According to patent office guidance, a petitioner “may not submit new evidence or argument in reply that it could have presented earlier, e.g. to make out a prima facie case of unpatentability.” U.S. Patent Trial and Appeal Board, Consolidated Trial Practice Guide at 73 (Nov. 2019).

V. GROUND 3: THE CHALLENGED CLAIMS ARE NOT OBVIOUS OVER *OKASHITA* AND *YU*

A. *Yu* and *Okashita* Are Not Analogous Art

Petitioner argues that the radically different fields of invention between *Okashita* and *Yu* can be ignored because “they all relate to a semiconductor switching circuit with cascaded transistors having an SOI configuration.” Reply at 6 (citing Pet., 7-8, 39-40; Ex. 1002, ¶¶77-80, 90-91). But the mere use of cascaded transistors having an SOI configuration does not make *Okashita* and/or *Yu* analogous to the invention of the ’886 Patent. In order to do so, the references must be (1) from the same field of endeavor; and, if not (2) whether the reference is reasonably pertinent to the particular problem with which the inventor is involved. *K-Tec, Inc.*

v. Vita-Mix Corp., 696 F.3d 1364, 1375 (Fed. Cir. 2012). The prior art in this case is neither.

The '886 Patent is in the field of semiconductor design, and particularly a Silicon on Insulator design that allows for the use of circuits that were originally designed to be constructed using bulk silicon. '886 Patent, 1:42-50. In order to accomplish this, the '886 Patent teaches that the capacitance of certain structures built using SOI is intentionally increased, so as to mimic the characteristics of bulk silicon. *Id.*, 3:21-48. *Yu* and *Okashita*, as detailed in Patent Owner's Response, relate to SOI circuits that are used for a low voltage radio frequency switch (in the case of *Okashita*) and SOI circuits that are used for a silicon-controlled rectifier for high voltage applications, particularly for electrostatic discharge (in the case of *Yu*). Paper 18 ("POR"), 18-22.

Rather than dispute the technical merits of the teachings in the prior art as compared to the '886 Patent, Petitioner instead introduces case law purportedly stating that determining whether art is reasonably pertinent is not accomplished "by parsing differences in application labels." Reply at 5-6 (citing *In re Bigio*, 381 F.3d 1320 (Fed. Cir. 2004)). But that case supports Patent Owner's position. In *Bigio*, the Federal Circuit confirmed that in examining whether a reference is in the same

field of endeavor as a patent, the Board must consult both the “structure *and function* of the claimed invention as perceived by one of ordinary skill in the art.” *Bigio*, 381 F.3d at 1326 (emphasis added). Although in that case the Federal Circuit held that there was no error in determining that toothbrush prior art was analogous to a claim for a hairbrush, the clear test for determining whether art is in the same field of endeavor to a patent involves consultation to both the structure and function. Here, the structures and functions of the prior art are radically different from that of the ’886 Patent and, therefore, they are not from the same field of endeavor.

Even if not from the same field of endeavor, a reference can still be analogous to a patent if it would be “reasonably pertinent” to the problem addressed by the challenged patent. Here, *Yu* would not be reasonably pertinent to the particular problem in which the inventor is involved, namely, designing SOI transistors that can be used to operate circuits designed for use in bulk silicon. The “reasonably pertinent” inquiry would allow the use of art outside of the field of endeavor because “familiar items may have obvious uses beyond their primary purposes.” *KSR Int’l v. Teleflex Inc.*, 550 U.S. 398, 402 (2007). But here, the disclosure in *Yu* is not reasonably pertinent to the field of endeavor of the ’886 Patent, because it relates only to a high voltage silicon-controlled rectifier that does not use transistors that

would be operable using circuit designs for bulk silicon.

B. The Petition Does Not Provide a Sufficient Rationale for Combining *Yu* and *Okashita*

Petitioner’s Reply attempts to fill the massive holes in the original arguments presented by the Petition regarding the combination of *Yu* and *Okashita*, but it cannot.

The Reply notes that a “distinction in end-use application is immaterial to the question of motivation to combine.” Reply at 8. But this is not a case where two analogous or similar structures merely have different intended uses. Rather, the circuitry itself in *Yu* and *Okashita* is entirely different. POR 18-23. Petitioner relies entirely on hindsight to support its analysis that a POSITA, presented with the antenna circuit in *Burgener*, would look to the high voltage silicon-controlled rectifier in *Yu* for transistor design inspiration.

The Petition’s rationale for combining the references is based on impermissible hindsight and overly generic motivations to combine. And the Reply confirms as such, noting that “[a] POSITA looking to enhance *Okashita*’s design would logically apply *Yu*’s techniques—an example of routine optimization and common sense.” Reply at 9. But there is no explanation of *why* the POSITA would look to such radically different designs that are used for different purposes to arrive

at the claims, except for impermissible hindsight. Petitioner’s argument that “both *Yu* and *Okashita* disclose switching devices that utilize cascaded SOI transistors formed in isolated islands surrounded by trench isolation” (*id.* at 10) is the exact type of hindsight bias that the Federal Circuit has cautioned against. *Insite Vision Inc. v. Sandoz, Inc.*, 783 F.3d 853, 859 (Fed. Cir. 2015) (“Defining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness.”) (citation omitted); *see ActiveVideo Networks, Inc. v. Verizon Commc’ns, Inc.*, 694 F.3d 1312, 1327 (Fed. Cir. 2012) (“[T]he expert’s testimony on obviousness was essentially a conclusory statement that a person of ordinary skill in the art would have known, based on the ‘modular’ nature of the claimed components, how to combine any of a number of references to achieve the claimed inventions. This is not sufficient and is fraught with hindsight bias.”).

Petitioner’s argument with respect to Claim 3 is nonsensical. Petitioner apparently argues that since both *Okashita* and *Yu* disclose the features in Claim 3, the motivation to combine *Okashita* and *Yu* to reach the claimed invention is “immaterial.” Reply at 11 (“[B]ecause *Okashita* independently teaches the limitations of claim 3 and their benefits [], HID’s argument regarding the lack of motivation in *Okashita* to look to *Yu* is immaterial.”). This is incorrect for two

reasons. First, as discussed above, *Okashita* does not disclose the cascaded transistors in a single isolated island; rather, each transistor is in its own isolated island. Section IV.A. Second, even if both prior art references disclosed this particular feature (they do not), Ground 3 still requires *Okashita* and *Yu* to be combined with one another to meet all elements of the underlying independent Claim 1 and, therefore, obviousness of Claim 3 would fail without such a combination. Because *Okashita* specifically teaches that “each of the MOS transistors 1, 1’, 2 and 2’ is isolated by the trench insulating layers T1 and T2, so that the leakage of radio frequency signals from the silicon layer 23 of the MOS transistor 1 *to that of the MOS transistor 1’*. . . can be sufficiently suppressed” (Ex. 1004, 8:47-54. (emphasis added); Ex. 2006, ¶ 53), and because *Yu* does not contain such isolation, the POSITA additionally would not have looked to *Yu* when modifying *Okashita*.

VI. GROUND 4: THE CHALLENGED CLAIMS ARE NOT ANTICIPATED BY YU

In the Institution Decision, the Board stated that the limitation of Claim 1 stating “a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance” merely requires that the source/drain junction not physically contact the buried oxide layer. Paper 9 at 23-24. The Board recognized that “the alleged electrical connection in *Yu* prevents the capacitance

from being formed, notwithstanding the physical disconnection.” *Id.* at 24. On Reply, Patent Owner confirmed this understanding, and also submitted persuasive expert evidence explaining it. As noted by Mr. Berg, notwithstanding the physical disconnection between the layers in *Yu*, no such capacitance is formed. Mr. Berg opined that “because of the presence of N-well 44, the transistor 65 does not have a source/drain junction capacitance even though neither the source, nor the drain, contact the buried oxide layer.” Ex. 2006, ¶ 59. He further explained the basis for this opinion, which is that due to “the source region of the first transistor 100 is doped N+ and is partially located in the N-Well 44, it is, in fact, electrically in contact with the buried oxide layer, as prohibited by Claim 1 of the ’886 Patent.” *Id.* ¶ 61. This electrical contact, of course, is what prevents a capacitance from being formed and prevents *Yu* from anticipating Claim 1. As explained by Mr. Berg, “[b]ecause of this electrical contact, no capacitance is formed. In my opinion, this lack of electrical contact and lack of capacitance on the drain of transistor 65 prevents the source/drain junction of transistor 65 from forming a source/drain junction capacitance and, therefore, *Yu* does not anticipate claim 1.” *Id.* ¶ 63.

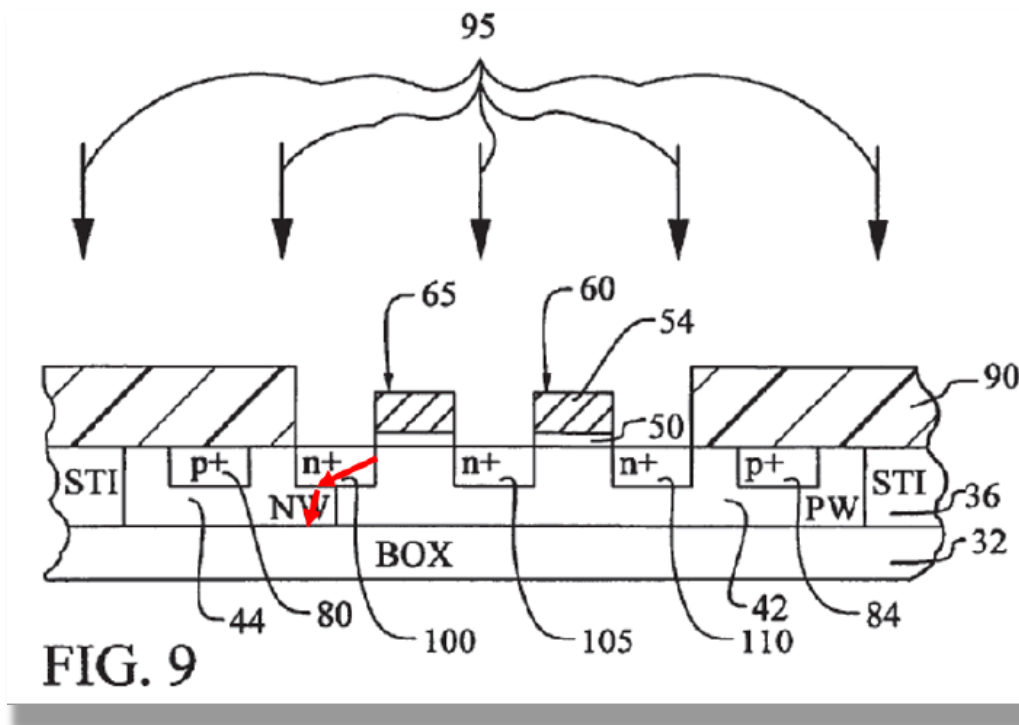
Petitioner claims that the additional expert evidence submitted by Patent Owner at the invitation of the Board should be stricken and not considered because

paragraph 59 of the Berg Declaration is “not cited or incorporated into the POR.” Reply at 13. But paragraph 59 merely summarizes Mr. Berg’s position that the transistor 65 in *Yu* does not have a source/drain junction capacitance required by the claim despite the physical disconnection. Mr. Berg’s explanation of this phenomenon, covered in detail in paragraphs 60 through 63 of his Declaration, are cited and discussed at length in the Patent Owner Response. *See* POR at 23-26. Therefore, the lack of electrical separation and, therefore, the lack of required capacitance between the transistors and the buried oxide layer in *Yu* was properly presented and preserved.

Petitioner presents two arguments on Reply: first, that despite the N-Well (labeled 44 in *Yu*), a capacitance actually is formed between the n+ doped region and overlapping p-well 42 (Reply at 14) and, second, a belated claim construction argument that the term “a source/drain junction” requires only one of the source junction or the drain junction, not both (*id.* at 15). Neither of these arguments were properly presented in the Petition, and therefore were waived. A petition is required to identify “in writing and with particularity . . . the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge to each claim.” 35 U.S.C. § 312(a)(3); *see also Intelligent Bio-Sys., Inc.*, 821 F.3d at

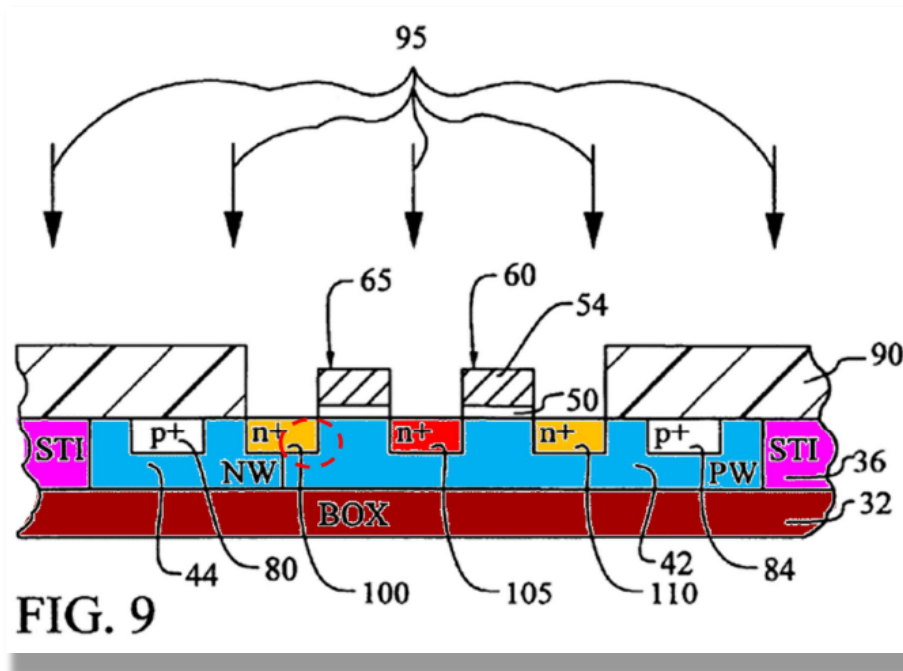
1369. According to patent office guidance, a petitioner “may not submit new evidence or argument in reply that it could have presented earlier, e.g. to make out a prima facie case of unpatentability.” U.S. Patent Trial and Appeal Board, Consolidated Trial Practice Guide at 73 (Nov. 2019).

In addition to being waived, both of these arguments are wrong. As to the existing capacitance on the source of the transistor 65, all meaningful capacitance is dissipated through the N-well, as shown by Mr. Berg in his annotated version of Figure 9:



Dr. Thompson’s new argument regarding the n+ and P-well forming a capacitance

in the dotted red circle is that the “portion of the n+ doped region overlapping the p-well 42 [] forms a pn junction, which under operating conditions generates a depletion region and consequently a junction capacitance across the depletion region.” Reply at 14 (citing Ex. 1026 ¶¶ 5-9). Neither Petitioner nor Dr. Thompson explain what these “operating conditions” are, or what junction capacitance is formed. Indeed, Dr. Thompson’s original opinion is that the doped regions 80, 84, 100, 105, and 110 do not extend to the buried oxide layer 32 and, therefore, the source/drain junctions of these transistors form source/drain junction capacitance. Ex. 1002, ¶¶ 202-203. This opinion, which is incorrect, does not contain any analysis whatsoever of the effect of the N-well 44.



Indeed, to the extent any junction capacitance is formed at all, it would be so infinitesimally small due to the neighboring N-well that it would have no impact whatsoever on device performance.

Petitioner's second new argument is that the claim term "a source/drain junction that does not contact said buried oxide layer" should be construed to mean "a source junction or a drain junction that does not contact said buried oxide layer." Reply at 15-16. In addition to being waived, this construction is inconsistent with the disclosure in the '886 Patent. The '886 Patent states that:

The source/drain junction capacitances of transistor 212 behave similarly to the junction capacitances of a transistor implemented in a conventional bulk silicon wafer, instead of a conventional SOI wafer, in part because of the greater thickness of device layer 202 compared to the thickness of conventional device layer 102. The better understood and more predictable junction capacitances in structure 200 result in more predictable behavior of transistor 212 such that, for example, computer simulation programs and bulk silicon wafer design kits that are well understood and widely used for conventional bulk silicon fabrication can be utilized to design and implement transistor 212 in the invention's SOI wafer.

'886 Patent, 4:19-32. Creating an "unbalanced" transistor where each of the source

capacitance and drain capacitance is variable (or nonexistent) does not further these design goals. Therefore, Petitioner's belated claim construction position fails in light of the intrinsic evidence.

VII. GROUND 5: THE CHALLENGED CLAIMS ARE NOT OBVIOUS OVER *BURGENER* AND *OKASHITA*

Petitioner cannot overcome the fundamental differences that would lead the POSITA *not* to combine *Burgener* and *Okashita*, and therefore Ground 5 fails as to all claims.

A. Patent Owner Did Not Repeat the Teaching Away Argument from Institution

A POSITA would not have been motivated to look to *Okashita* to build the transistors in *Burgener*. Although *Burgener* discloses that its integrated circuit may be fabricated using “semiconductor-on-insulator (SOI) techniques” (Ex. 1006, ¶ [0105]), the POSITA would not have been motivated to use the specific SOI design in *Okashita* to create *Burgener*'s switch. Ex. 2006, ¶ 64.

At institution, the Board noted that *Burgener* and *Okashita* do not teach away from one another. “[I]t is well settled that an expression of preferences does not teach away from alternatives.” Paper 9, at 27 (citation omitted). In its Response, Patent Owner did not make a teaching away argument. Instead, it provided persuasive and technically grounded expert testimony explaining why the

motivations to combine in the Petition are insufficient. Petitioner now notes that “HID previously raised this same argument in its Preliminary Response [], and the Board rejected it.” Reply at 17. But Patent Owner does not raise a teaching away argument in its Patent Owner Response, rather, it noted that the POSITA would not have been motivated to combine *Okashita* and *Burgener* for several reasons: (1) the increased capacitance would decrease performance (Ex. 2006, ¶ 70); (2) that the heat considerations contemplated by *Burgener* do not apply to the circuits at issue (*id.*, ¶ 71); (3) that there would be no need to prevent leakage of radio signals because UTSi technology is fully insulating (*id.*, ¶ 72); and (4) that there would be no need to locate *Burgener*’s FETs together in one isolated region (*id.*, ¶ 73). And *Burgener* expresses more than merely a preference for one design. In referencing the antenna switch of Figure 17 relied upon by Petitioner, it explicitly states that “[f]urther details regarding design and fabrication of such an RF switch may be found in U.S. Pat. No. 6,804,502, issued Oct. 12, 2004 and entitled ‘Switch Circuit and Method of Switching Radio Frequency Signals.’” Ex. 1006, ¶ [0101].

Patent Owner, far from repeating the teaching away argument it made at institution, presented expert testimony regarding the reasons why a POSITA would

not have been motivated to combine *Burgener* and *Okashita* with a reasonable expectation of success.

B. Okashita Discloses Traditional Isolation Wells, Which Are Not Used In *Burgener* Due To The Thin S-o-S Substrate

The POSITA would not have been motivated to look to *Okashita* because *Burgener II* states that the transistors in the RF switch can be made using ultra-thin silicon-on-sapphire technology, which eliminates the need for “[t]raditional transistor isolation wells” that are used for thick silicon. Ex. 2004, 10:66-11:1. Petitioner notes that *Okashita* “does not disclose the thickness of silicon layer 23 . . . , nor does it describe the silicon layer as ‘relatively thick.’” Reply at 18. But *Okashita*, as admitted by Dr. Thompson, discloses such isolation wells. Ex. 1002, ¶¶ 128-132. Patent Owner is not relying on the scale of any patent drawings; rather, it notes that *Burgener II*, which is cited directly in *Burgener* as providing details for the fabrication of the exact circuit relied upon by Dr. Thompson, eliminates the need for the very transistor isolation wells that Dr. Thompson admits are in *Okashita*. Ex. 2006, ¶ 68.

It is Dr. Thompson who referred to the intervening silicon layer in *Okashita* as “thick” in order to support his failed argument that it could be combined with *Yu*. Ex. 1002, ¶ 82 (“similar to the transistors in the ’886 patent, *Okashita*’s transistors

1 and 2 also show an *intervening thickness* of the silicon layer 23 between the bottom surfaces of their sources and drains and the buried oxide layer 22.”) (emphasis added). This perfectly encapsulates the slapdash approach of Dr. Thompson to all of this analysis – when he wants *Okashita*’s silicon layer to be thick in order to support its combination with *Yu*, his opinion is that. When Dr. Thompson wants *Okashita*’s silicon layer to be thin to support combination with *Burgener*’s thin Silicon-on-Insulator arrangement, his opinion is that. Dr. Thompson’s inconsistent opinions are not credible.

C. *Okashita*’s Design Would Add Undesirable Capacitance to the Circuit in *Burgener*

Unable to walk away from the basic principle that increased capacitance in a transistor will slow its operation, Petitioner resorts to referring to Mr. Berg’s testimony as “uncorroborated” and therefore somehow irrelevant. Reply at 18. Petitioner argues that *Burgener* “does not suggest that increased capacitance would create a slower switching circuit,” (*id.* at 19), apparently unaware of basic principles of electronic circuits. Higher capacitance “leads to decreased performance,” and as such, the POSITA would not have had a reasonable expectation of success in substituting the silicon-on-sapphire in *Burgener* for the SOI technology in *Okashita*. Ex. 2006, ¶ 70. Unable to prevent itself from using impermissible hindsight,

Petitioner also refers to the '886 Patent and notes that it explains that buried oxide beneath the silicon layer helps reduce the capacitive load caused by increased junction capacitance. Reply at 19 (citing '886 Patent, 5:66-6:10. To the extent disclosures in the '886 Patent are relevant to the combination of *Burgener* with *Okashita*, this disclosure supports Patent Owner's position. The patent states that the capacitive load from the source/drain junction capacitances "is advantageously reduced by taking advantage of the thick buried oxide layer" '886 Patent, 5:66-6:2. If reducing capacitance is "advantageous," then increased capacitance is obviously a disadvantage.

Petitioner now submits a supplemental expert declaration, stating that "a POSITA would be aware of techniques to mitigate any negative effects from increased junction capacitance." Reply at 19 (citing Ex. 1002 ¶ 48, Ex. 1026 ¶¶ 10-16). In the supplemental Thompson declaration, he admits that there would be a "small increase in delay time at low supply voltages, and no significant increase at higher voltages." Ex. 1026, ¶ 14. Though he states there is no "significant" increase, he does admit that there will be an increase in delay time due to the additional capacitance. Dr. Thompson next states that, even though delay time would be increased, this would not have discouraged a POSITA from incorporating

Okashita's transistors into *Burgener*'s design. *Id.* ¶¶15-16. He also notes without citation that “a POSITA would have recognized the advantages of *Okashita*'s body-contacted SOI transistors over *Burgener*'s transistors and would also have been aware of established techniques to mitigate any increase in junction capacitance.” *Id.* ¶ 16. But Dr. Thompson is silent as to what these “established techniques” are, and his opinion requires an additional undisclosed modification to *Burgener*, not only replacing the disclosed transistors with those of *Okashita*, but then redesigning the circuit to mitigate increase in junction capacitance. This obviousness combination is not only undisclosed, it is the definition of hindsight bias.

D. Heat Dissipation Is Not a Concern

Petitioner claims that the management of heat is a “routine design consideration,” despite *Burgener* expressly discussing thermal considerations with respect to other portions of the circuit only. Reply at 21. *Burgener* notes that, rather than dissipating heat in the FETs, the heat should be dissipated in the resistive couplings. Ex. 1006, ¶ [0044] (“impedance may be intentionally added to such couplings. For example, it may be desirable to more closely control a drive impedance, and to dissipate heat in specific resistive series coupling elements rather than within the FETs themselves.”).

E. Petitioner Does Not Meaningfully Address the Silicon-on-Sapphire Technology Disclosed in *Burgener*

Petitioner's final argument is that the silicon-on-sapphire technology in *Burgener II* is functionally equivalent to that of the SOI technology in *Okashita*, and therefore the motivation to combine exists regardless of whether the insulator layer is SOI or SOS. Reply at 22-23. Again, this argument is not in the Petition or the original Thompson Declaration. It is also wrong. *Burgener II* explains the benefits of silicon-on-sapphire technology, which would not inure to the circuits if the SOI technology in *Okashita* were substituted. *Burgener II* states:

Owing to the fully insulating nature of silicon-on-sapphire technology, the parasitic capacitance between the nodes of the RF switch 30 are greatly reduced as compared with bulk CMOS and other traditional integrated circuit manufacturing technologies. Consequently, the inventive RF switch exhibits improved switch isolation as compared with the prior art RF switch designs.

Ex. 2004, 7:57-64.

Dr. Thompson claims that a POSITA would have still been motivated to include the trenches from *Okashita* to build the transistors in *Burgener*, even if the substrate were the silicon-on-sapphire technology of *Burgener II*. Ex. 1026, ¶¶ 20-24. Again, this opinion is nowhere in Dr. Thompson's original Declaration. And

further, Dr. Thompson provides no analysis in his supplemental declaration regarding how the POSITA would construct such trenches in the silicon-on-sapphire technology of *Burgener* with a reasonable expectation of success. Neither Dr. Thompson nor Petitioner account for how such trenches would be built in this different substrate, and also ignore that the voltage generators used in *Burgener* are already low-noise: “a negative voltage generator will be helpful, preferably a low-noise circuit such as described in copending, published U.S. patent application Ser. No. 10/658,154, filed Sep. 8, 2003 and entitled ‘LowNoise Charge Pump Method and Apparatus.’ Such a low-noise charge pump is important for avoiding unintended emissions from the antenna.” Ex. 1006, ¶ [0101]. Since the input voltages in *Burgener* are already “low noise,” there exists no motivation for the POSITA to add the insulating trenches from *Okashita* to the antenna in *Burgener*.

VIII. GROUND 6: THE CHALLENGED CLAIMS ARE NOT OBVIOUS OVER *BURGENER*, *OKASHITA*, AND *YU*

Ground 6 fails for the same reasons as Ground 5.

IX. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board issue a Final Written Decision finding that Claims 3 and 8-19 not shown to be unpatentable.

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Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned hereby certifies that the portions of the above-captioned PATENT OWNER’S SUR-REPLY specified in 37 C.F.R. § 42.24 has 4,764 words in compliance with the 5,600 word limit set forth in 37 C.F.R. § 42.24. This word count was prepared using Microsoft Word for Office 365.

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