

Before The Patent Trial And Appeal Board
Oral Hearing
January 7, 2026

Harbor Island's Presentation

IPR2024-01402: U.S. 7,745,886

Problem to be Solved in the Art

SOI Has Benefits, But Circuits Must be Redesigned

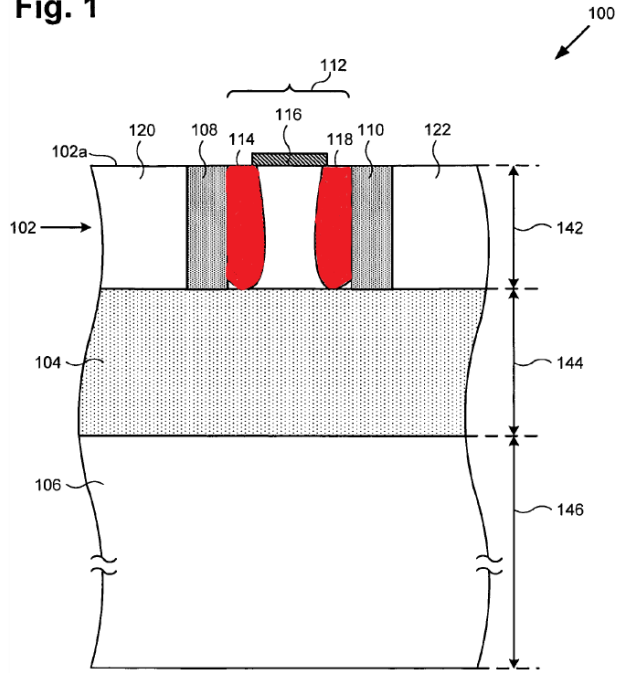
Each type of silicon wafer utilized for fabricating such semiconductor structures suffers from attendant drawbacks. For example, it is difficult to electrically isolate semiconductor structures fabricated on a conventional bulk silicon wafer, because although such semiconductor structures can be partially electrically isolated by virtue of, for example, their isolating trenches, electric current can still flow under such trenches, leading to, for example, voltage and current fluctuations. Neighboring semiconductor devices, e.g. neighboring cascaded transistors, in such structures thus tend to interfere with one another when fabricated on bulk silicon wafers. In contrast, it is easier to electrically isolate semiconductor structures or circuits implemented on a conventional silicon on insulator wafer, in which a buried oxide layer provides additional isolation. Unfortunately, circuits designed for fabrication in a bulk silicon wafer must be redesigned for fabrication in a conventional silicon on insulator wafer, which significantly increases manufacturing and integration complexity and cost.

Ex. 1001 ('886 Patent), 1:28-46

Problem to be Solved in the Art

Traditional SOI Has Low Capacitance

Fig. 1



In FIG. 1, a conventional semiconductor on insulator (“SOI”) wafer cross section is shown as structure **100**.

Ex. 1001 ('886 Patent), 2:29-30

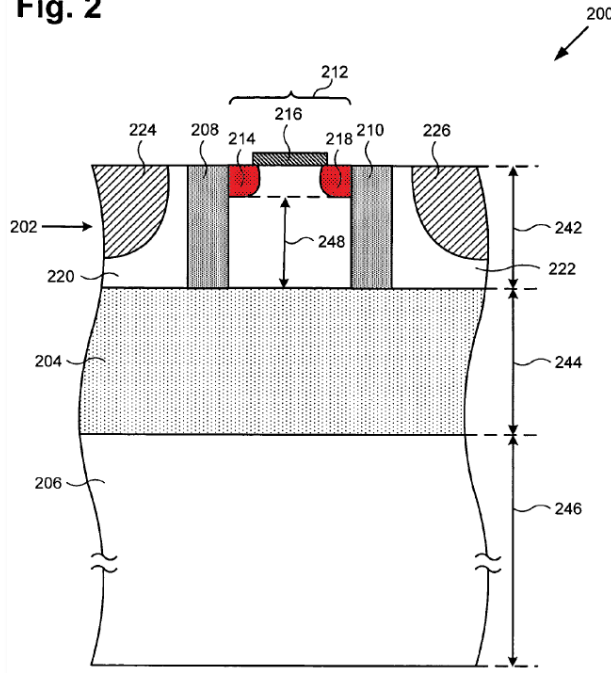
Source **114** and drain **118** typically extend all the way through device layer **102** and contact the top surface of buried oxide layer **104**. Because there is thus no, or almost no, semiconductor material, e.g. silicon, between source **114** or drain **118** and the top surface of buried oxide layer **104**, there is no, or almost no, semiconductor junction to create a capacitive load. Such low capacitance allows for, for example, higher speed operation or lower power consumption. However, such low or non-existent junction capacitance also prevents the utilization of well understood bulk silicon wafer design methodology, device models, and well developed design kits that take into account existence of certain amount of junction capacitance based on, for example, transistor sizes, device geometries and other factors. In other words, conventional SOI structure **100** must be designed and fabricated using only new, less developed, and less prevalent design methodologies, device models and design kits that are not as well developed, tested or understood, and which also introduce additional development costs and inefficiencies in the design and fabrication of SOI devices using conventional SOI structure **100** in FIG. 1.

Ex. 1001 ('886 Patent), 3:15-35

Solution to the Problems

Add Capacitance To Source and Drain

Fig. 2



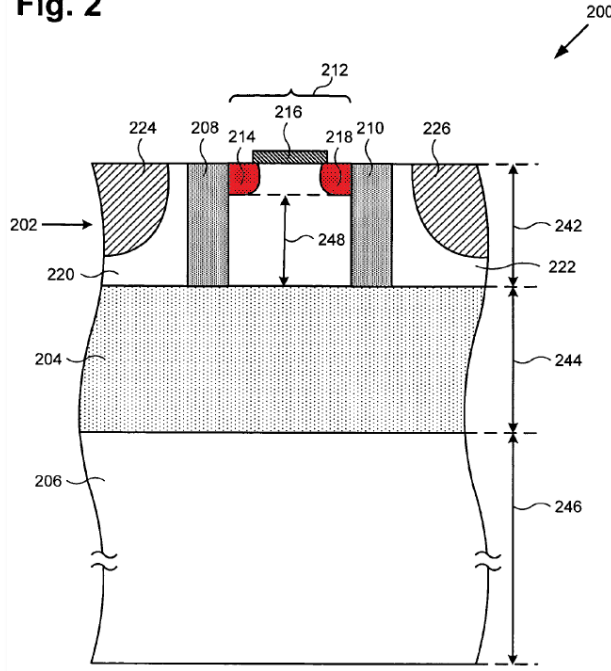
Instead, a layer with intervening thickness **248** remains between the bottom surfaces of source **214** and drain **218** and the top surface of buried oxide layer **204**. Consequently, a semiconductor junction is formed by source **214** and drain **218** within device layer **202**. Each such semiconductor junction will have an associated junction capacitance, e.g. the source/drain junctions of transistor **212** have corresponding source/drain junction capacitances.

Ex. 1001 ('886 Patent), 4:11-18

Solution to the Problems

Add Capacitance To Source and Drain

Fig. 2



The source/drain junction capacitances of transistor 212 behave similarly to the junction capacitances of a transistor implemented in a conventional bulk silicon wafer, instead of a conventional SOI wafer, in part because of the greater thickness of device layer 202 compared to the thickness of conventional device layer 102. The better understood and more predictable junction capacitances in structure 200 result in more predictable behavior of transistor 212 such that, for example, computer simulation programs and bulk silicon wafer design kits that are well understood and widely used for conventional bulk silicon fabrication can be utilized to design and implement transistor 212 in the invention's SOI wafer. Significantly, the behavior of transistor 212 is better understood and more predictable than the behavior of transistor 112 in FIG. 1 which, for example, practically lacks any source or drain junction capacitance because source 114 and drain 118 of transistor 112 extend all the way to the top surface of buried oxide layer 104.

Ex. 1001 ('886 Patent), 4:11-18

Challenged Claims

Claims 3 and 8-19 Remain

1. A switching circuit comprising:
a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;

each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;

at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.

3. The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer.

16. A wireless communications device comprising an antenna and a low noise amplifier, said wireless communications device further comprising:

a switching circuit controlled by a switch control signal and interposed between said antenna and said low noise amplifier, said switching circuit including:

a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer, each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;

at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.

Claim Construction

C. Claim Construction

The Board construes claims per *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), 37 C.F.R. §42.100(b). Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Here, no terms need construction to resolve the controversy in this forum.²

Petition at 5.

Claim 1 recites “a transistor having a source/drain junction that does not contact said buried oxide layer” (emphases added). The term “a source/drain junction” requires only one of the source junction or the drain junction, not both. Therefore, each transistor only requires either region 100 or region 105 not to contact the buried oxide layer. Three recognized principles support this interpretation.

Petitioner Reply at 15.

Claim Construction

The Source/Drain Junction Term

Claim 1 recites “a transistor having a source/drain junction that does not contact said buried oxide layer” (emphases added). The term “a source/drain junction” requires only one of the source junction or the drain junction, not both. Therefore, each transistor only requires either region 100 or region 105 not to contact the buried oxide layer. Three recognized principles support this interpretation.

Petitioner Reply at 15.

Petitioner’s second new argument is that the claim term “a source/drain junction that does not contact said buried oxide layer” should be construed to mean “a source junction or a drain junction that does not contact said buried oxide layer.” Reply at 15-16. In addition to being waived, this construction is inconsistent with the disclosure in the ’886 Patent. The ’886 Patent states that:

Sur-Reply, at 14.

Claim Construction

The Isolated Island Term

But Petitioner

did not propose such (or any other) modification to the structure of *Okashita* in its discussion of claim 3. And whether or not isolation trenches exist between MOS transistors 1, 1' is irrelevant to whether the isolated first region in which MOS transistors 1, 1' are situated constitutes the claimed isolated island.

HID does not argue that *Okashita*'s [first region](#) is not an “isolated island.” See POR, 16-17.

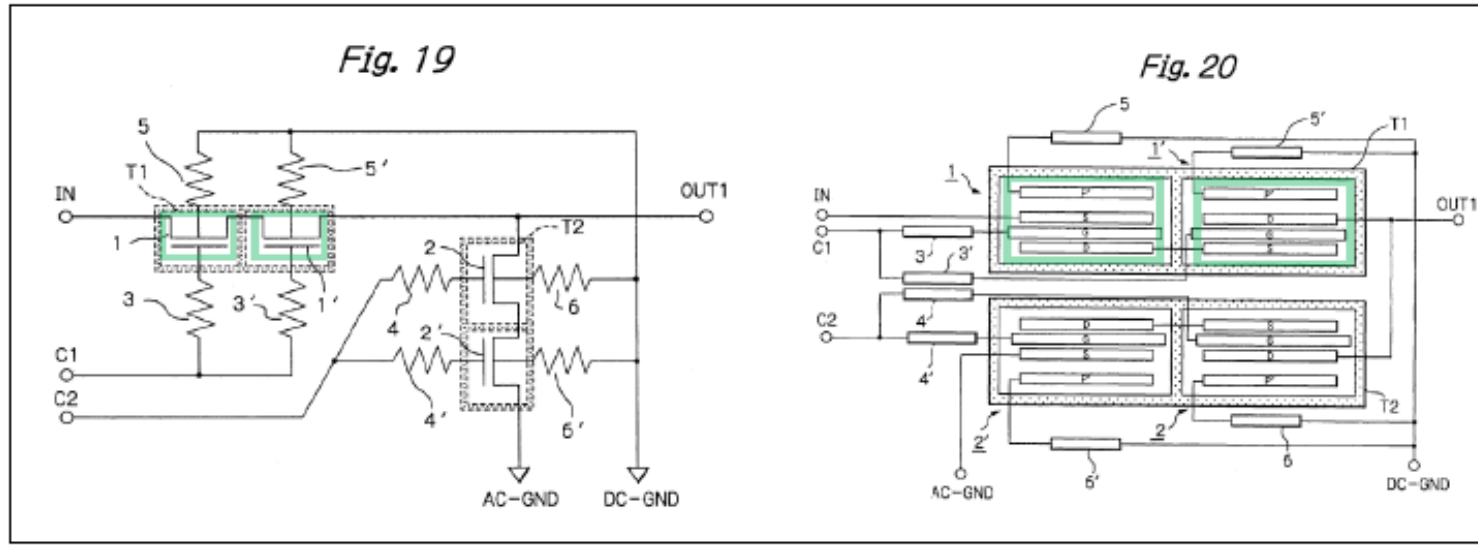
Petitioner Reply at 3.

Petitioner also presents a belated claim construction that the “isolated island” in Claim 3 should be construed to mean “one or more” isolated islands. Reply at 4. This argument was not presented in the Petition, despite the obvious logical difference present in *Okashita*, and is therefore waived. A petition is required to

Sur-Reply at 5.

Ground 2: Okashita Obviousness

Okashita's Isolated Islands



Ex. 1002, ¶ 150.

Ground 2: Okashita Obviousness

Okashita's Isolated Islands

In FIG. 20, which is a plan view of the semiconductor switch apparatus of FIG. 19, each of the MOS transistors 1, 1', 2 and 2' is isolated by the trench insulating layers T1 and T2, so that the leakage of radio frequency signals from the silicon layer 23 of the MOS transistor 1 to that of the MOS transistor 1' and the leakage of radio frequency signals from the silicon layer 23 of the MOS transistor 2 to that of the MOS transistor 2' can be sufficiently suppressed.

Ex. 1002, Okashita, 8:47-54.

POR at 16-18.

Ground 3: *Okashita* + *Yu*

No Motivation To Combine *Okashita* and *Yu*

47. I disagree with Dr. Thompson that the POSITA would have been motivated to combine *Yu* and *Okashita*, because *Yu* and *Okashita* are very different. *Yu* describes a silicon-controlled rectifier that is used to switch very high voltages. Ex. 1005, Abstract. The field of endeavor in *Yu* is specifically limited to “a method to form a low voltage triggering, silicon-controlled rectifier (SCR) SOI device having improved ESD performance.” *Id.* 1:10-13. ESD refers to electrostatic discharge.

48. *Okashita*, on the other hand, relates to “a semiconductor switch apparatus for radio frequency signals.” Ex. 1004, 1:7-8. *Okashita* discloses a switching circuit that works between, at most, -3V and 3V. *Id.* at 7:18-29. In fact, *Okashita* repeatedly refers to 3 volts as a high voltage. *Id.* at 3:11, 3:40.

Berg Decl., ¶¶ 47-48.

POR at 18-19.

Ground 3: *Okashita* + *Yu*

No Motivation To Combine *Okashita* and *Yu*

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to silicon-on-insulator (SOI) devices and, more particularly, to a method to form a low voltage triggering, silicon-controlled rectifier (SCR) SOI device having improved ESD performance.

(2) Description of the Prior Art

At present, the vast majority of integrated circuit products are formed on bulk semiconductor wafers. However, silicon-on-insulator (SOI) wafer-based products are under development as a majority technology for the future. SOI offers the advantages of improved short channel performance, improved isolation, and reduced power supply capability. However, ESD protection of SOI devices remains a significant challenge to manufacturers. One particular category of ESD devices is the silicon-controlled rectifier (SCR). The SCR is commonly used for ESD protection in bulk semiconductor technology. The present invention relates to SCR development in SOI technology.

Yu, Ex. 1005, 1:10-27.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor switch apparatus for radio frequency signals.

2. Description of the Related Art

In a mobile communication apparatus such as a mobile telephone apparatus using radio frequency signals such as GHz microwave signals, semiconductor switch apparatuses are used for switching the operation of an antenna circuit and a receiving and transmitting circuit.

A prior art semiconductor switch apparatus using GaAs FETs is very simple and therefore, can be constructed by one semiconductor chip. That is, since the GaAs FETs serve as passive elements such as resistors and capacitors, bias circuits for the GaAs FETs are unnecessary. Also, since a substrate of the GaAs FETs is made of semi-insulating material having a high resistance, the leakage of radio frequency signals via the substrate can be suppressed. This will be explained later in detail.

Okashita, Ex. 1004, 1:7-24.

Ground 3: *Okashita* + *Yu*

No Motivation To Combine *Okashita* and *Yu*

First, the POSITA looking to modify the SOI process in *Okashita* would not have looked to *Yu* for that modification because *Okashita* is a low voltage wireless switching circuit and *Yu* discloses a high voltage silicon-controlled rectifier that is outside of that field of endeavor. Second, *Okashita* already provides teachings for an SOI process for a switching apparatus, and therefore there would be no motivation to look to a completely different process in *Yu* that solves a different problem and is designed to operate at very different voltages. Third, with respect to Claim 3, the POSITA would not have been motivated to look to *Yu*, which does not isolate the individual transistors from one another, as *Okashita* specifically teaches that “each of the MOS transistors 1, 1', 2 and 2' is isolated by the trench insulating layers T1 and T2, so that the leakage of radio frequency signals from the silicon layer 23 of the MOS transistor 1 *to that of the MOS transistor 1' . . .* can be sufficiently suppressed.” Ex. 1004, 8:47-54. (emphasis added).

Berg Decl., ¶ 53.

POR at 22-23

Ground 3: *Okashita* + *Yu*

Okashita and *Yu* Are Not Analogous To The '886 Patent

52. These fields of art and pertinent problems not only have nothing to do with one another, they also have nothing to do with the problem solved by the '886 Patent. The '886 Patent relates to intentionally increasing the capacitance of structures built using SOI to mimic the characteristics of circuits designed to be built using bulk silicon, so that circuits designed for fabrication using bulk silicon do not need to be redesigned for use in SOI. '886 Patent, 1:37-50; 3:21-48.

Berg Decl., ¶ 52.

POR at 21.

Ground 3: *Okashita* + *Yu*

No Motivation To Combine *Okashita* and *Yu*

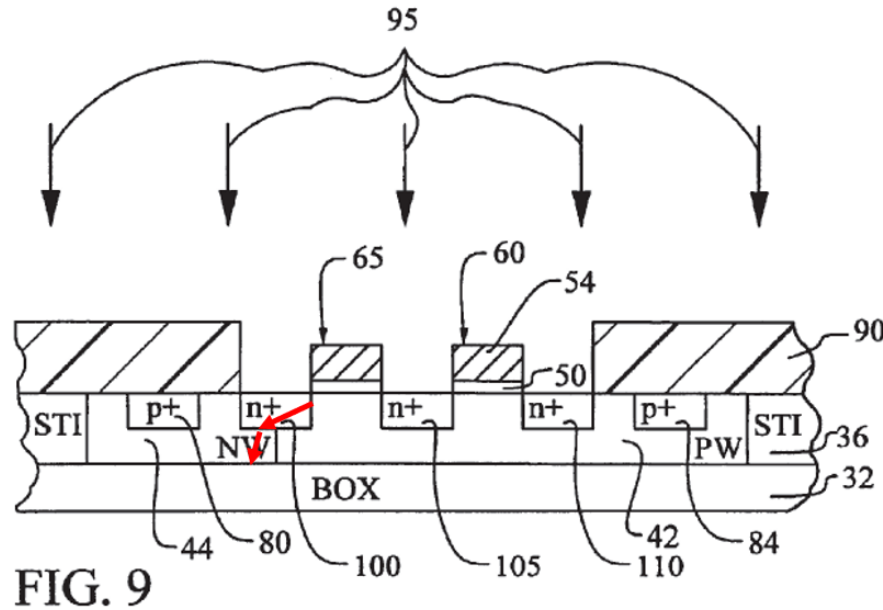
Petitioner's argument with respect to Claim 3 is nonsensical. Petitioner apparently argues that since both *Okashita* and *Yu* disclose the features in Claim 3, the motivation to combine *Okashita* and *Yu* to reach the claimed invention is "immaterial." Reply at 11 ("[B]ecause *Okashita* independently teaches the limitations of claim 3 and their benefits [], HID's argument regarding the lack of motivation in *Okashita* to look to *Yu* is immaterial."). This is incorrect for two

reasons. First, as discussed above, *Okashita* does not disclose the cascaded transistors in a single isolated island; rather, each transistor is in its own isolated island. Section IV.A. Second, even if both prior art references disclosed this particular feature (they do not), Ground 3 still requires *Okashita* and *Yu* to be combined with one another to meet all elements of the underlying independent Claim 1 and, therefore, obviousness of Claim 3 would fail without such a combination. Because *Okashita* specifically teaches that "each of the MOS transistors 1, 1', 2 and 2' is isolated by the trench insulating layers T1 and T2, so that the leakage of radio frequency signals from the silicon layer 23 of the MOS transistor 1 to that of the MOS transistor 1' . . . can be sufficiently suppressed" (Ex. 1004, 8:47-54. (emphasis added); Ex. 2006, ¶ 53), and because *Yu* does not contain such isolation, the POSITA additionally would not have looked to *Yu* when modifying *Okashita*.

Sur-Reply at 10-11

Ground 4: *Yu* Anticipation

Claim 3 Not Anticipated by *Yu*



Berg Decl., ¶ 61.

POR at 25-26

Ground 4: *Yu* Anticipation

Claim 3 Not Anticipated by *Yu*

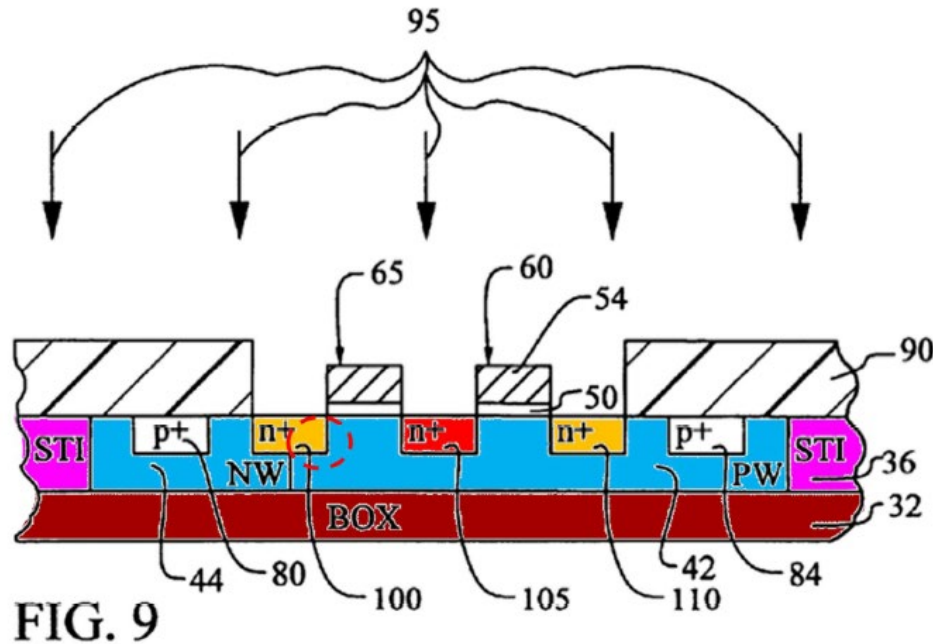
63. As *Yu* explains, the doped n+ regions form the source/drain junctions of the transistor, and as expressly stated by *Yu*, “doped region 100 is coupled to the second well 44” and, therefore, doped region 100 (the N+ well) *does* electrically contact the buried oxide layer, even if there is no physical contact. *Id.*, 5:51. Because of this electrical contact, no capacitance is formed. In my opinion, this lack of electrical contact and lack of capacitance on the drain of transistor 65 prevents the source/drain junction of transistor 65 from forming a source/drain junction capacitance and, therefore, *Yu* does not anticipate Claim 1.

Berg Decl., ¶ 63.

POR at 26.

Ground 4: *Yu* Anticipation

Supplemental Thompson Declaration



Supp. Thompson Decl., ¶ 9.

Ground 4: *Yu* Anticipation

Claim Construction

Petitioner's second new argument is that the claim term "a source/drain junction that does not contact said buried oxide layer" should be construed to mean "a source junction or a drain junction that does not contact said buried oxide layer." Reply at 15-16. In addition to being waived, this construction is inconsistent with the disclosure in the '886 Patent.

Sur-Reply, at 14.

Ground 4: *Yu* Anticipation

Source/Drain Junction

The source/drain junction capacitances of transistor **212** behave similarly to the junction capacitances of a transistor implemented in a conventional bulk silicon wafer, instead of a conventional SOI wafer, in part because of the greater thickness of device layer **202** compared to the thickness of conventional device layer **102**. The better understood and more predictable junction capacitances in structure **200** result in more predictable behavior of transistor **212** such that, for example, computer simulation programs and bulk silicon wafer design kits that are well understood and widely used for conventional bulk silicon fabrication can be utilized to design and implement transistor **212** in the invention's SOI wafer.

'886 Patent, 4:19-30.

Ground 5: Wireless Claims

No Motivation To Combine *Burgener* and *Okashita*

A POSITA would not have been motivated to look to *Okashita* to build the transistors in *Burgener*. Although *Burgener* discloses that its integrated circuit may be fabricated using “semiconductor-on-insulator (SOI) techniques” (Ex. 1006, ¶ [0105]), the POSITA would not have been motivated to use the specific SOI design in *Okashita* to create *Burgener*’s switch. Ex. 2006, ¶ 64.

POR, 28.

Ground 5: Wireless Claims

Burgener Points the POSITA to *Burgener II*

Dr. Thompson relies explicitly on *Burgener*'s Figure 17 for the disclosure of the “cascaded transistors” limitation. Ex. 1002, ¶ 221. *Burgener* states that: “Fig. 17 is a simplified schematic of exemplary circuitry 1700 for an antenna switch. Further details regarding design and fabrication of such an RF switch may be found in U.S. Pat. No. 6,804,502, issued Oct. 12, 2004 and entitled “Switch Circuit and Method of Switching Radio Frequency Signals.” Ex. 1006, ¶ [0101]. According to Mr. Berg,

POR, 30.

Ground 5: Wireless Claims

Burgener II Teaches UTSi Technology For Low Capacitance

The fully insulating sapphire substrate enhances the performance characteristics of the inventive RF switch by reducing the deleterious substrate coupling effects associated with non-insulating and partially insulating substrates. For example, improvements in insertion loss are realized by lowering the transistor on resistances and by reducing parasitic substrate resistances. In addition, switch isolation is improved using the fully insulating substrates provided by UTSi technology. Owing to the fully insulating nature of silicon-on-sapphire technology, the parasitic capacitance between the nodes of the RF switch 30 are greatly reduced as compared with bulk CMOS and other traditional integrated circuit manufacturing technologies. Consequently, the inventive RF switch exhibits improved switch isolation as compared with the prior art RF switch designs.

Burgener II, Ex. 2004, at 7:50-62.

Using the methods described in the patents referenced above, electronic devices can be formed in an extremely thin layer of silicon on an insulating synthetic sapphire wafer. The thickness of the silicon layer is typically less than 150 nm. Such an “ultrathin” silicon layer maximizes the advantages of the insulating sapphire substrate and allows the integration of multiple functions on a single integrated circuit. Traditional transistor isolation wells required for thick silicon are unnecessary, simplifying transistor process-

ing and increasing circuit density. To distinguish these above-referenced methods and devices from earlier thick-silicon embodiments, they are herein referred to collectively as “ultrathin silicon-on-sapphire.”

Burgener II, Ex. 2004, at 10:59-11:4.

Ground 5: Wireless Claims

Okashita's SOI Is Relatively Thick

70. Further, *Burgener* and *Burgener II*'s motivation to use UTSi would not have led the POSITA to look to other SOI technologies and specifically would not have led the POSITA to look to relatively thick silicon on top of a buried oxide layer, as shown in *Okashita* and as claimed by Dr. Thompson. Although other types of SOI may have been used to construct the circuit in *Burgener*, the POSITA would not have been led to the construction techniques in *Okashita* because, as compared to UTSi, its high capacitance leads to decreased performance. In my opinion, the POSITA would not have had a reasonable expectation of success merely substituting thin silicon-on-sapphire for a relatively thick silicon on insulator technology, because of this additional capacitance.

Berg Decl., ¶ 70.

POR, at 32.

Ground 5: Wireless Claims

Burgener's Discussion of Other SOI Techniques

Integrated Circuit Fabrication and Design

[0105] Integrated circuit fabrication details are not provided in the above description. In some preferred embodiments, including some which have output powers in excess of 1 W at around 2.4 GHz, the integrated circuits may be fabricated in accordance with ultrathin silicon on sapphire processing as described in U.S. Pat. No. 5,663,570, issued Sep. 2, 1997 and entitled “High-Frequency Wireless Communication System on a Single Ultrathin Silicon On Sapphire Chip.” Other semiconductor-on-insulator (SOI) techniques may be used to fabricate a dual-band transceiver integrated circuit as described above, for at least some frequency bands and power levels.

Burgener, Ex. 1006, at ¶ 105.

Ground 5: Wireless Claims

Reduced Operating Temperature

Burgener only mentions thermal considerations one time, when discussing the need for stacked FETs in the power amplifier section (rather than the antenna switch relied upon by Dr. Thompson). Ex. 1006, ¶ [0044]. And even there, Burgener only discusses dissipating heat “in specific resistive series coupling elements rather than within the FETs themselves.” *Id.* Because Burgener states that dissipating heat inside the FETs is *not* desirable (rather, heat should be dissipated in the resistive couplings), the POSITA would not have been motivated to fabricate the transistors using what Dr. Thompson contends is a higher capacitance fabrication technique merely to dissipate additional heat in the transistors.

Berg Decl., ¶ 71

Ground 5: Wireless Claims

Signal Leakage

72. Second, Dr. Thompson states that the POSITA would have been motivated to fabricate Burgener's circuit using Okashita's teachings "to prevent leakage of radio signals from the cascaded SOI FETs to other components of antenna switch 1700." Ex. 1002 ¶¶ 215-16. I disagree with Dr. Thompson. Burgener states that the circuit should be made using UTSi technology. UTSi technology is fully insulating, and "[t]he fully insulating sapphire substrate enhances the performance characteristics . . . by reducing the deleterious substrate coupling effects associated with non-insulating and partially insulating substrates." Ex. 2004, 7:39-64.

Therefore, it is my opinion that the POSITA would not have been motivated to turn to another, less insulating SOI technology and then to build trenches as disclosed in *Okashita* to achieve insulating benefits that are already achieved by *Burgener*.

Berg Decl., ¶ 72

Ground 5: Wireless Claims

Isolated Islands

73. Third, Dr. Thompson states that the POSITA would have been motivated to locate each set of FETs together in one isolated region “to ensure that these FETs have consistent performance characteristics” Ex. 1002 ¶ 217. Other than hindsight bias garnered from Claims 2, 14, and 17 of the ’886 Patent which require at least one of the plurality of transistors to be located within an isolated island, I do not understand why the POSITA would have been motivated to locate each set of Burgener’s FETS together in one isolated region. Consistent

performance characteristics can be obtained through a number of methods, and placing the transistors in an isolated island would increase the space necessary for the circuit. This would specifically motivate the POSITA *not* to do this because, according to Burgener, it is desirable to integrate many devices and fabricate them “onto a single integrated circuit,” thereby solving a multitude of problems and gaining significant benefits. Ex. 1006, ¶ [0010].

Berg Decl., ¶ 73