

Petitioner's Demonstratives

Samsung Electronics Co., Ltd., Samsung Electronics
America, Inc., and NXP Semiconductors, N.V.*

Petitioners

v.

Harbor Island Dynamic, LLC

Patent Owner

IPR2024-01402 - Patent No. 7,745,886

*NXP Semiconductors N.V. filed a petition and a motion for joinder in IPR2025-00954 and has been joined as petitioner in IPR2024-001402

Instituted Grounds

— Claims 1-18 of the '886 patent were challenged

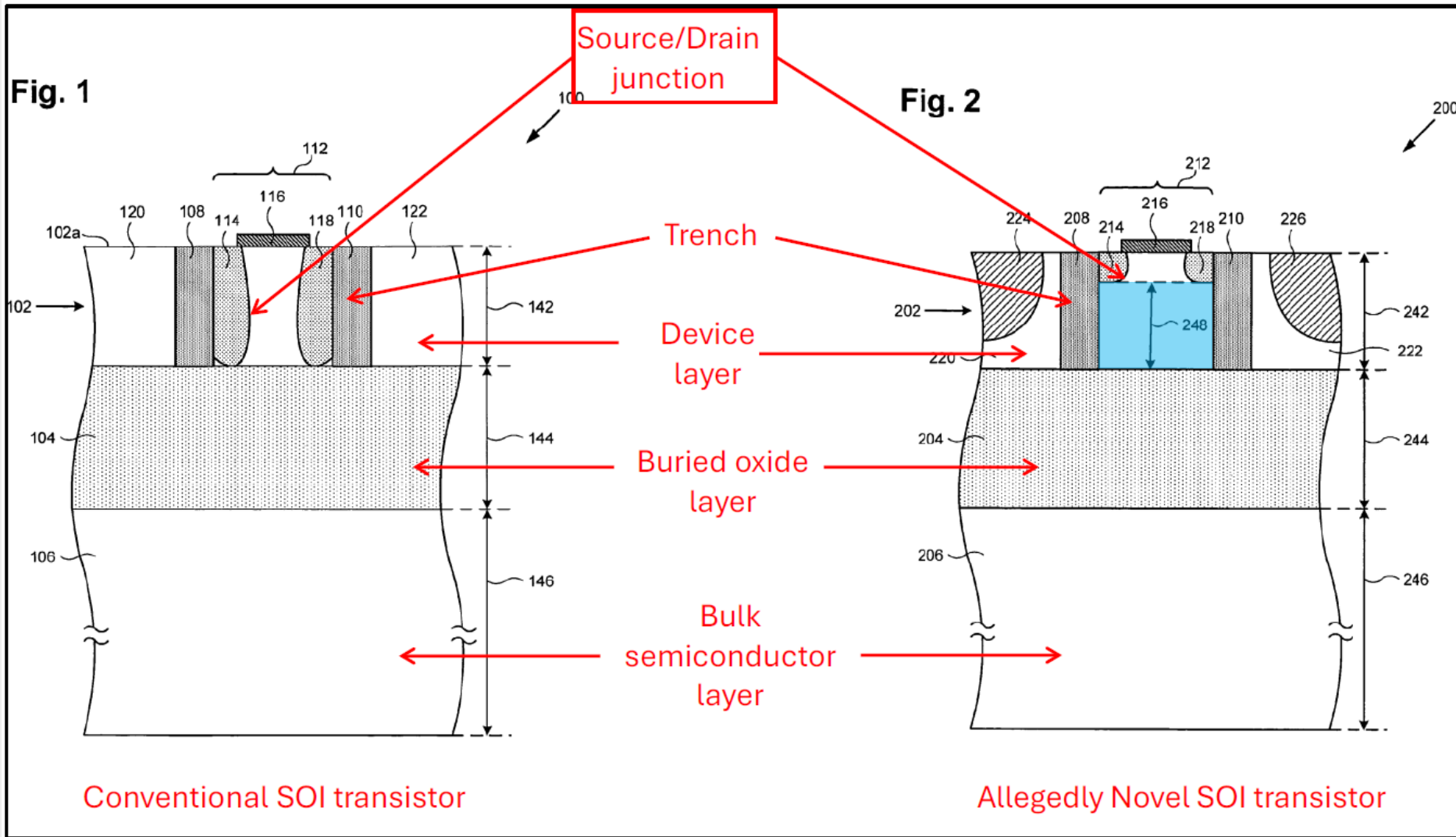
Ground	Challenged Claims	Basis	Prior Art
1	1, 2, 4, and 5	§102	<i>Okashita</i>
2	1-7	§103	<i>Okashita</i>
3	1-7	§103	<i>Okashita</i> and <i>Yu</i>
4	1-3	§102	<i>Yu</i>
5	1-19	§103	<i>Burgener</i> and <i>Okashita</i>
6	1-19	§103	<i>Burgener</i> , <i>Okashita</i> , and <i>Yu</i>

Remaining Grounds and Claims

– HID cancelled claims 1-2 and 4-7 post institution.

Ground	Challenged Claims	Basis	Prior Art
1	1, 2, 4, and 5	§102	<i>Okashita</i>
2	1-7 3	§103	<i>Okashita</i>
3	1-7 3	§103	<i>Okashita</i> and <i>Yu</i>
4	1-3 3	§102	<i>Yu</i>
5	1-19 3, 8-19	§103	<i>Burgener</i> and <i>Okashita</i>
6	1-19 3, 8-19	§103	<i>Burgener</i> , <i>Okashita</i> , and <i>Yu</i>

The '886 Patent's Alleged Invention – Intervening Silicon Layer Between Source/Drain Junction and Buried Oxide Layer



Intervening Silicon Layer Between Source/Drain Junction and Buried Oxide Layer Was Well-Known

Koh (1997)

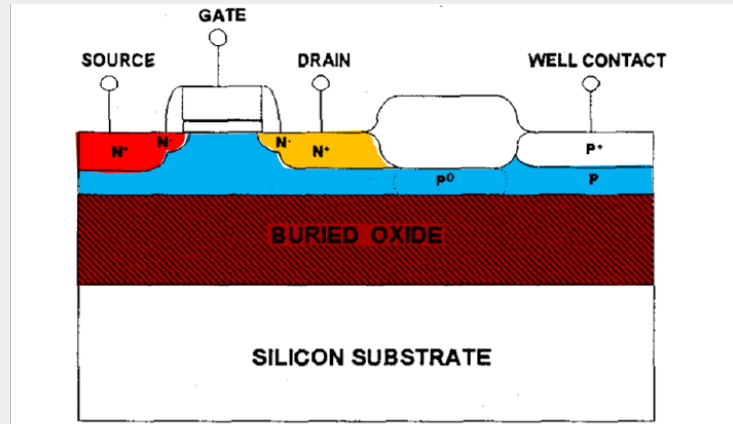


Fig. 1. A cross-sectional illustration of BC-SOI MOSFET structure.

Chuang (1998)

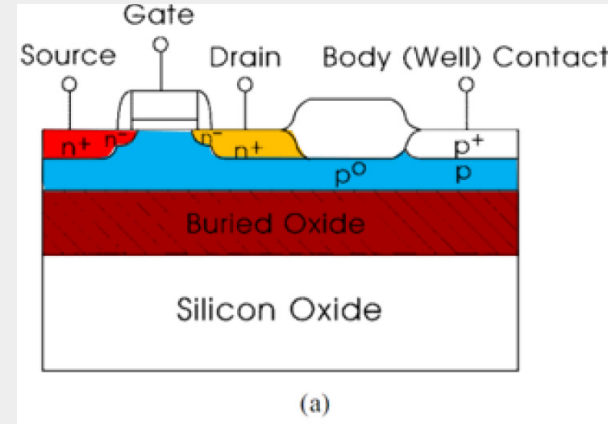
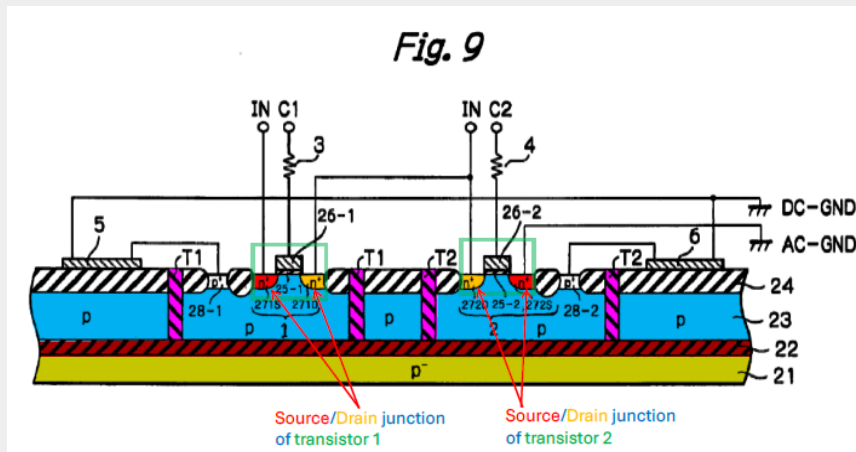


Fig. 48

Okashita (2004)



Yu (2004)

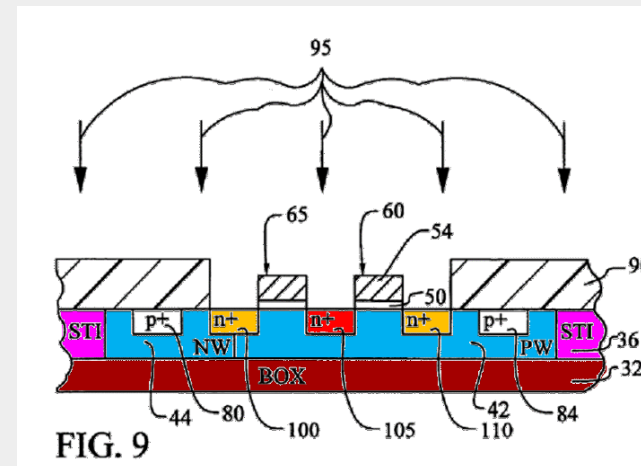


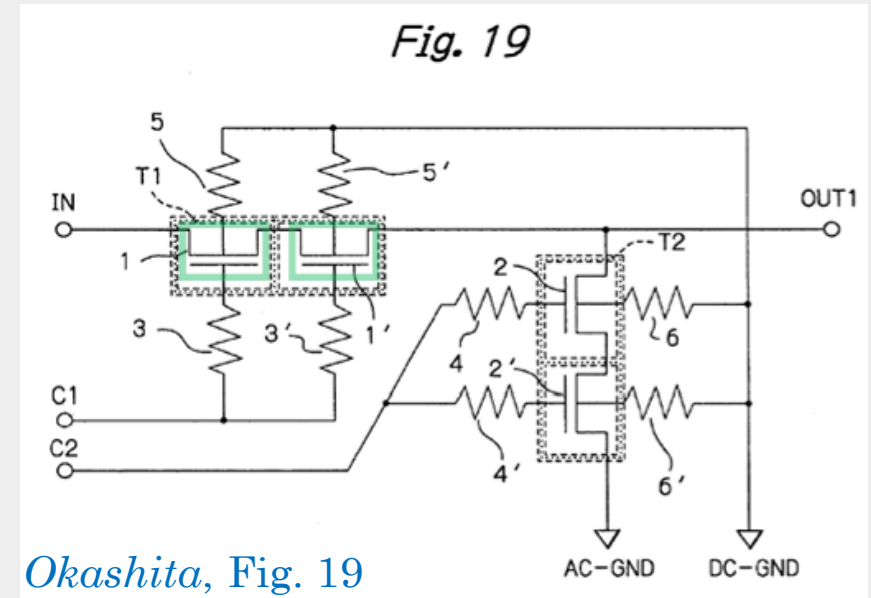
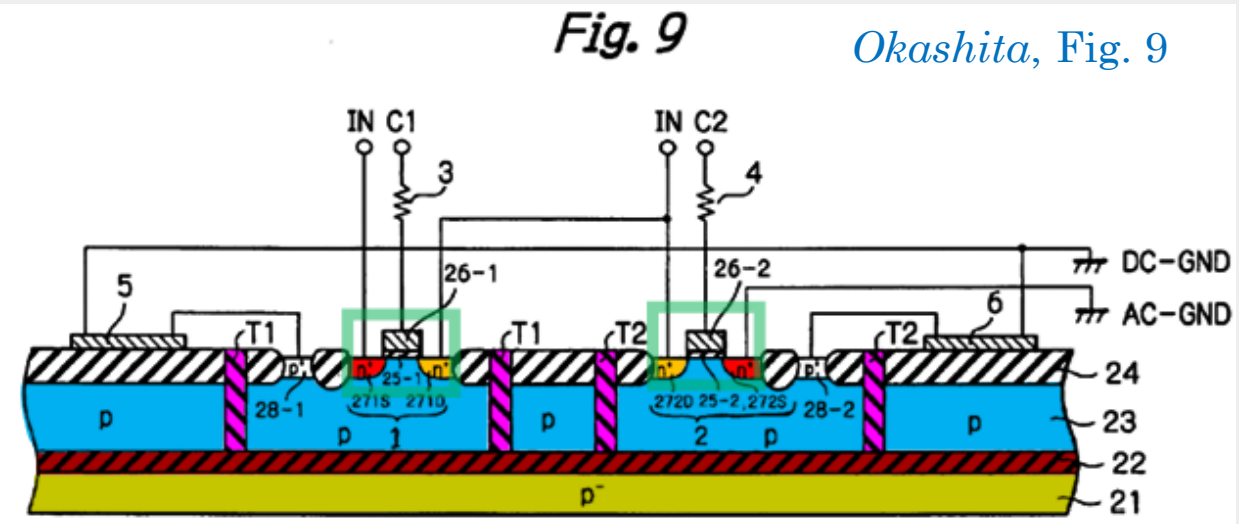
FIG. 9

Disputed Issues

- A. Ground 2:** *Okashita*'s disclosure of claim 3's "plurality of cascaded transistors [] situated within an isolated island."
- B. Ground 3:** Motivation to combine *Okashita* and *Yu*.
- C. Ground 4:** *Yu*'s disclosure of claim 1's "each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance."
- D. Ground 5, 6:** Motivation to combine *Burgener* and *Okashita*.

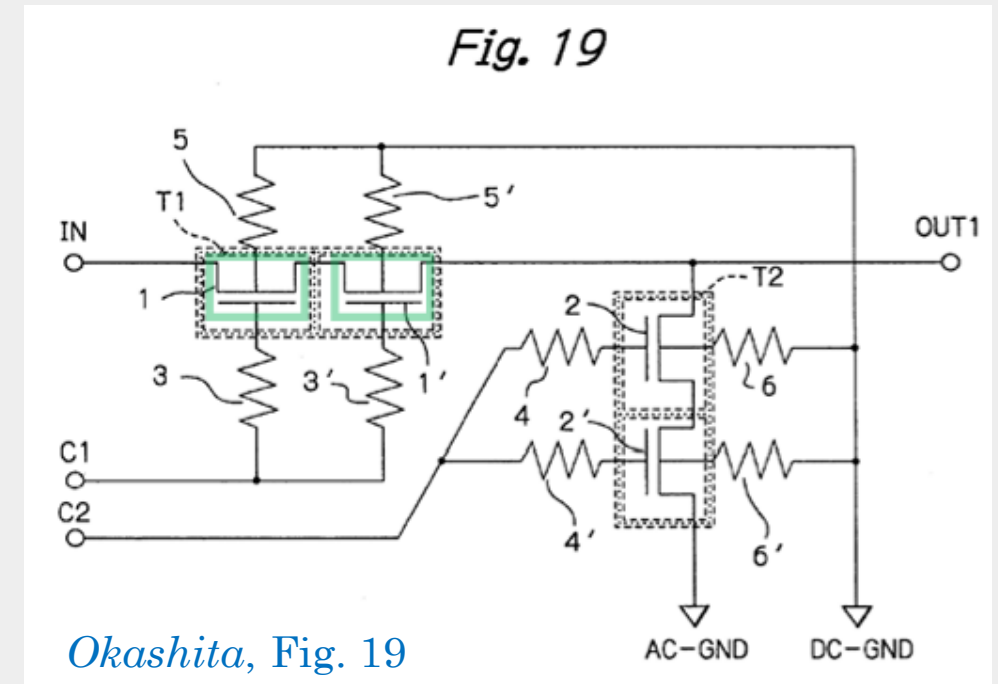
Okashita Discloses Independent claim 1 - Undisputed

1. A switching circuit comprising:
a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;
each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;
at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.



Dependent claim 3 and *Okashita*

3. The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer.

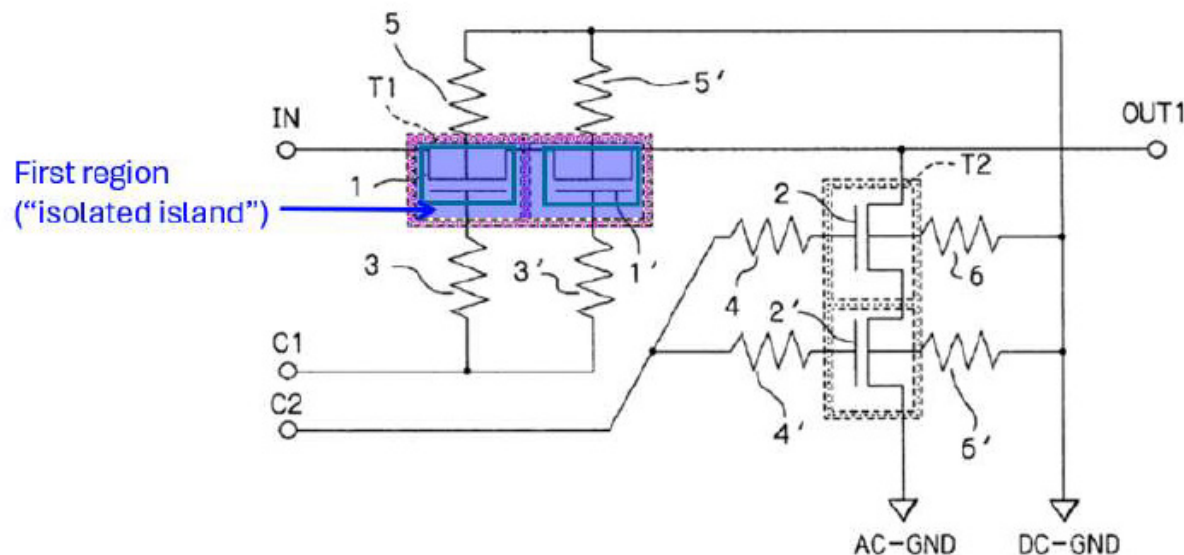


Claim 3's “plurality of cascaded transistors [] situated within an isolated island”

167. *Okashita* teaches the additional limitation of claim 3. For example, *Okashita* teaches (1) a plurality of MOS transistors “connected in series” and “formed within a first region of” the silicon layer and (2) a trench that surrounds the plurality of MOS transistors connected in series. *Okashita*, 10:43-67; *supra* §§-Thompson Decl., ¶167

Okashita, Fig. 19

Fig. 19



3. A semiconductor switch apparatus comprising:
 - an input terminal;
 - an output terminal;
 - an AC ground terminal;
 - a DC ground terminal;
 - a semiconductor substrate;
 - an insulating layer formed on said semiconductor substrate;
 - a semiconductor layer formed on said insulating layer;
 - a plurality of series MOS transistors formed within a first region of said semiconductor layer and connected in series between said input terminal and said output terminal;
 - a plurality of shunt MOS transistors formed within a second region of said semiconductor layer and connected in series between (a) one of said input terminal and said output terminal and (b) said AC ground terminal, said shunt MOS transistors being operated complementarily with said series MOS transistors;
 - a first trench insulating layer surrounding said series MOS transistors; and
 - a second trench insulating layer surrounding said shunt MOS transistors.

Okashita, claim 3

Okashita's Plurality of Series-Connected Transistors Are “Isolated” by the Surrounding Trench

In my opinion, a POSITA reading *Okashita* would have understood that trench T1 surrounding the plurality of MOS transistors 1, 1' effectively places these MOS transistors within an isolated “first region” in the silicon layer to minimize radio frequency signal leakage from, and to, the first region. See *Okashita*, 6:1-17, 8:47-54, 9:21-25; *supra* §§XI.B.1.e-XI.B.1.f.

Thompson Decl., ¶167

As explained hereinabove, according to the present invention, since a series MOS transistor and a shunt MOS transistor are isolated by trench insulating layers, the leakage of radio frequency signals can be further suppressed, that is, the transmission loss of radio frequency signals can be further suppressed.

Okashita, 9:20-25

Okashita's “first region” is “an isolated island”

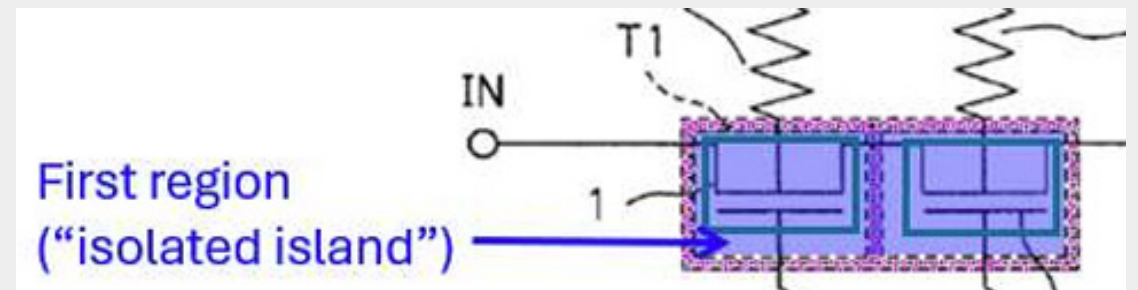


“This court has repeatedly emphasized that an indefinite article ‘a’ or ‘an’ in patent parlance carries the meaning of ‘one or more.’”

KCJ Corp. v. Kinetic Concepts, Inc., 223 F.3d 1351, 1356 (Fed. Cir. 2000)

“[E]ven if the first region in *Okashita* was two islands, it would still meet claim 3’s limitation of “an isolated island in said device layer” in which “said plurality of cascaded transistors is situated.” Both islands would together be isolated by the trench T1 surrounding the plurality of MOS transistors 1, 1'. The claim ... does not preclude MOS transistors 1, 1' from also being isolated from each other.”

Reply, 4



Reply, 3 (*Okashita's* Fig. 19 cropped)

Dependent claims 2 and 3

2. The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer.

3. The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer.

Okashita and *Yu* are Analogous Art

77. *Okashita* is analogous art to the '886 patent since both are from the same field of endeavor. *Okashita*, 1:7-15. For example, both relate to a semiconductor switching circuit with cascaded transistors having an SOI configuration. *See Okashita*, 1:43-61, 9:27-12:44; '886 patent, 1:14-17, 7:25-31, 8:63-10:55.

Thompson Decl., ¶77

90. *Yu* is analogous art to the '886 patent since both are from the same field of endeavor. For example, both patents relate to a semiconductor switching circuit with cascaded transistors having an SOI configuration. *See Yu*, 3:43-4:15, 5:44-57, 6:4-11, 55-60; *see* '886 patent, 8:63-10:55.

Thompson Decl., ¶90

Analogous Art Analysis



“The Board thus correctly set the field of the invention by consulting the **structure** and **function** of the claimed invention as perceived by one of ordinary skill in the art.”

In re Bigio, 381 F.3d 1320 (Fed. Cir. 2004)

1. Field of the Invention

The present invention is generally in the field of fabrication of semiconductor structures and circuits. More particularly, the invention is in the field of fabrication of semiconductor on insulator (SOI) structures and circuits.

'886 Patent, 1:13-17

Okashita and Yu are Analogous Art

- Function

1. A switching circuit comprising:
a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;

'886 Patent, 8:64-9:10

3. A semiconductor switch apparatus comprising:
an input terminal;
an output terminal;

Okashita, 10:43-67

1. A method to form a LVT-SCR device in the manufacture of an integrated circuit device comprising:

Yu, 7:38-39

An SCR is a “switching device.” Ex. 1011, 18;

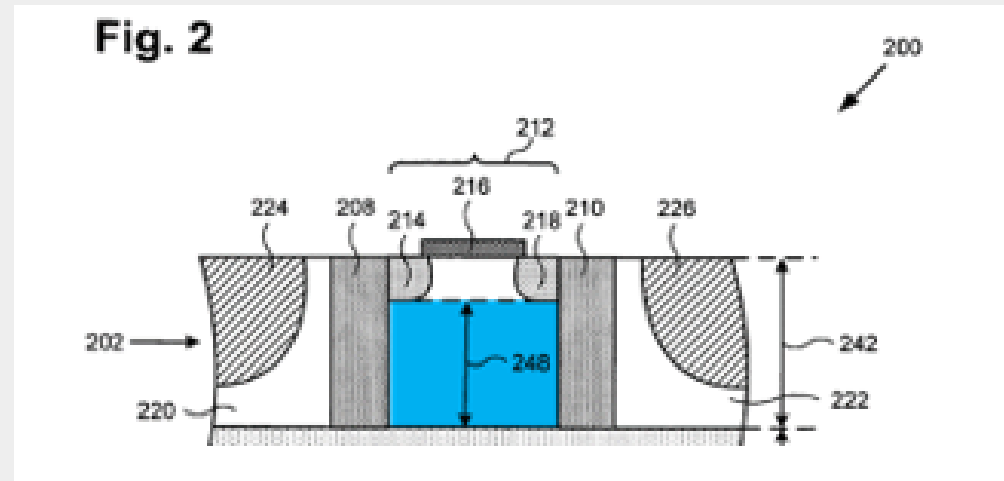
Thompson Decl., ¶90

The left drawing in Figure 2.36 shows how the layers 1 through 4 in the CMOS structure can be viewed as creating a 4-layer device with the pnpn layering. In power electronics, this is called a silicon-controlled rectifier (SCR) where it is used as a switching device between the top (*p*) and bottom (*n*) regions. From the qualitative viewpoint, the 4-layer structure blocks current flow from the

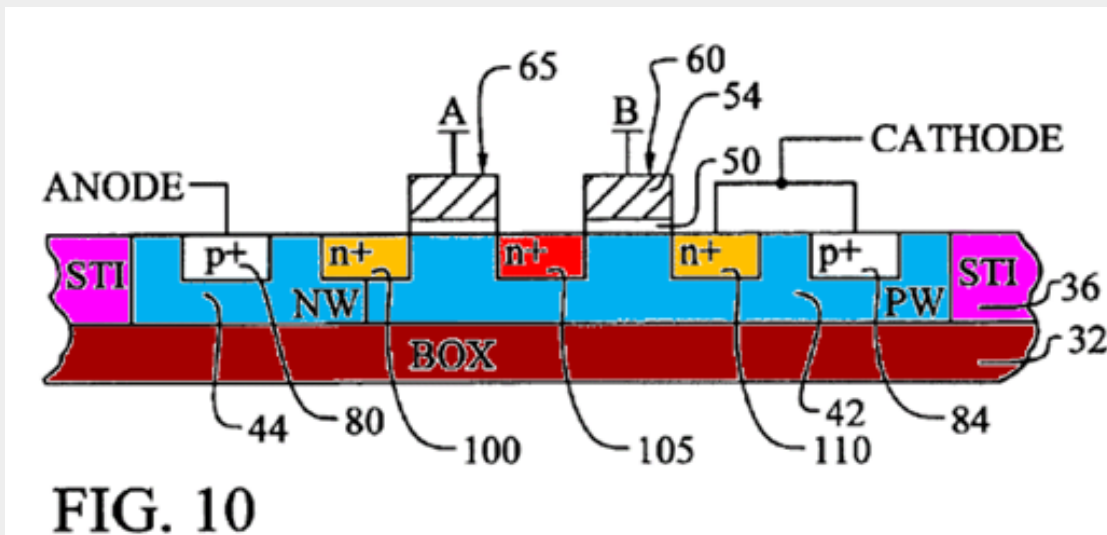
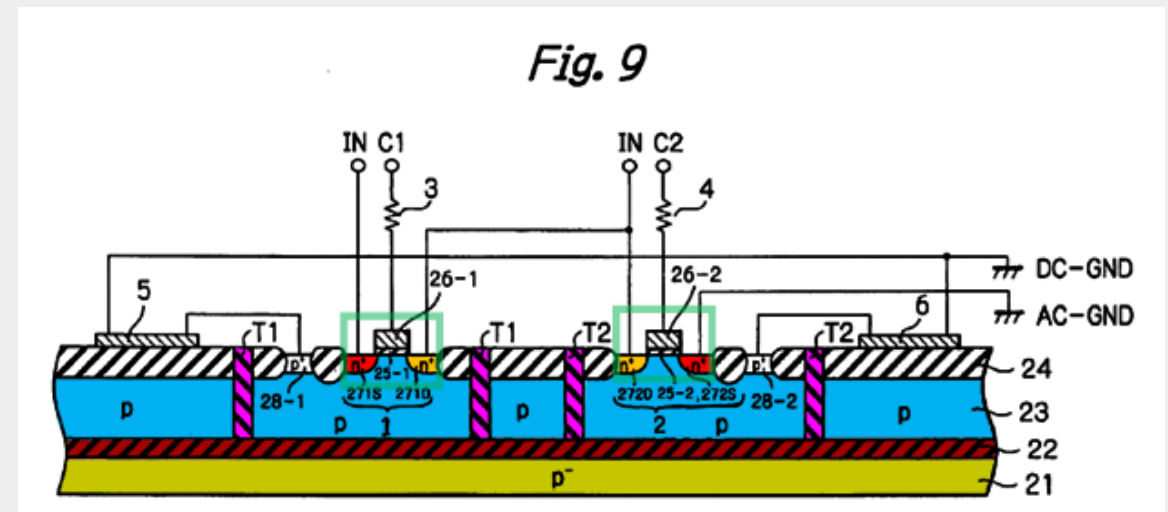
Ex. 1011, 18

Okashita and *Yu* are Analogous Art

- Structure



Petition, 3; '886 patent, Fig. 2

Petition 41; *Yu*, Fig. 10Petition 8, *Okashita*, Fig. 9

Field of Endeavor of '886 Patent and *Yu* are the same

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The present invention is generally in the field of fabrication of semiconductor structures and circuits. More particularly, the invention is in the field of fabrication of semiconductor on insulator (SOI) structures and circuits.

'886 Patent, 1:13-17

1. A switching circuit comprising:

a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;

each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;

at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.

'886 Patent, 8:64-9:10

(1) Field of the Invention

The invention relates to silicon-on-insulator (SOI) devices and, more particularly, to a method to form a low voltage triggering, silicon-controlled rectifier (SCR) SOI device having improved ESD performance.

Yu, 1:10-14

The preferred embodiments of the present invention disclose a method to form a LVT-SCR device on SOI with shallow trench isolation and having improved ESD performance. Further, the LVT-SCR device comprises novel, stacked MOS transistors to create a triggering mechanism having higher voltage tolerance. It should be clear to those experienced in the art that the present invention can be applied and extended without deviating from the scope of the present invention.

Yu, 3:43-52

The left drawing in Figure 2.36 shows how the layers 1 through 4 in the CMOS structure can be viewed as creating a 4-layer device with the pnpn layering. In power electronics, this is called a silicon-controlled rectifier (SCR) where it is used as a switching device between the top (*p*) and bottom (*n*) regions. From the qualitative viewpoint, the 4-layer structure blocks current flow from the

Ex. 1011, 18

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'886 Patent, 8:64-9:10

3. A semiconductor switch apparatus comprising:

an input terminal;

an output terminal;

an AC ground terminal;

a DC ground terminal;

a semiconductor substrate;

an insulating layer formed on said semiconductor substrate;

a semiconductor layer formed on said insulating layer;

a plurality of series MOS transistors formed within a first region of said semiconductor layer and connected in series between said input terminal and said output terminal;

a plurality of shunt MOS transistors formed within a second region of said semiconductor layer and connected in series between (a) one of said input terminal and said output terminal and (b) said AC ground terminal, said shunt MOS transistors being operated complementarily with said series MOS transistors;

a first trench insulating layer surrounding said series MOS transistors; and

a second trench insulating layer surrounding said shunt MOS transistors.

Okashita, 10:43-67

Field of Endeavor of '886 Patent and *Okashita* are the same

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each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;

at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.

'886 Patent, 8:64-9:10

According to the present invention, in a semiconductor switch apparatus including an input terminal, an output terminal, an AC ground terminal, a DC ground terminal, at least one series MOS transistor connected between the input terminal and the output terminal, and at least one shunt MOS transistor connected between one of the input terminal and the output terminal and the AC ground terminal, the series MOS transistor is formed within a first region of a semiconductor layer on an SOI configuration surrounded by a first trench insulating layer, and the shunt MOS transistor is formed within a second region of the semiconductor layer surrounded by a second trench insulating layer.

Okashita, 1:46-58

Petition, 7; Thompson Decl., ¶77; '886 patent, 1:13-17, 8:84-9:10; *Okashita*, 1:46-58.

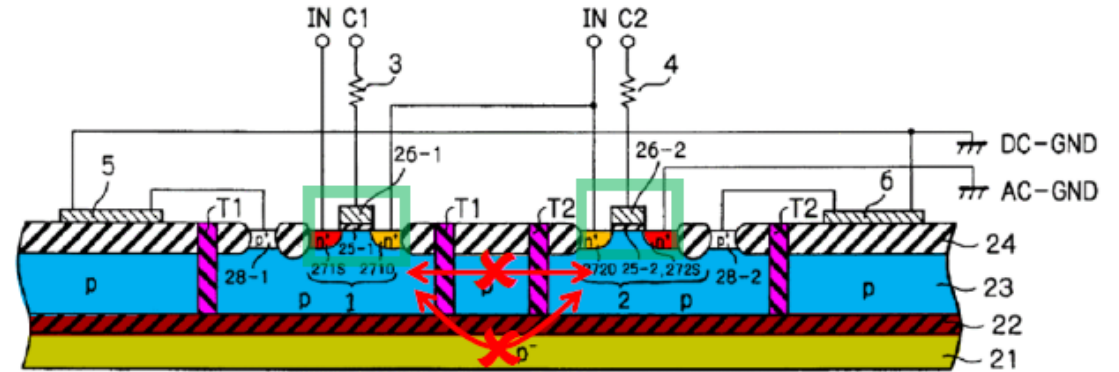
Okashita's “first region” is “an isolated island”

Each type of silicon wafer utilized for fabricating such semiconductor structures suffers from attendant drawbacks. For example, it is difficult to electrically isolate semiconductor structures fabricated on a conventional bulk silicon wafer, because although such semiconductor structures can be partially electrically isolated by virtue of, for example, their isolating trenches, electric current can still flow under such trenches, leading to, for example, voltage and current fluctuations. Neighboring semiconductor devices, e.g. neighboring cascaded transistors, in such structures thus tend to interfere with one another when fabricated on bulk silicon wafers. In contrast, it is easier to electrically isolate semiconductor structures or circuits implemented on a conventional silicon on insulator wafer, in which a buried oxide layer provides additional isolation. Unfortunately, circuits designed for fab-

insulative oxide. Trenches 108 and 110 typically extend through device layer 102 and contact the top surface of buried oxide layer 104, as shown in FIG. 1. In the region, or island, of device layer 102 between trenches 108 and 110 transistor 112 can be fabricated. Transistor 112 (an example of a “semiconductor device” in the present application), is electrically isolated from neighboring islands 120 and 122 by trenches 108 and 110, respectively, and buried oxide layer 104. This isolation is one conventional advantage of building semiconductor structures, such as transistor 112, on a SOI wafer, because the isolation allows such semiconductor structures to experience positive and negative voltage excursions without affecting neighboring devices and without shorting to ground.

'886 Patent, 2:65-3:11

Fig. 9 *Okashita*, Fig. 9 (annotated)



In FIGS. 8 and 9, since the SOI configuration is adopted, the leakage of radio frequency signals from the p-type silicon layer 23 surrounded by the trench insulating layer T1 for the series MOS transistor 1 via the silicon substrate 21 to the p-type silicon layer 23 surrounded by the trench insulating layer T2 for the shunt MOS transistor 2 can be suppressed.

Also, in FIGS. 8 and 9, since the series MOS transistor 1 is surrounded by the trench insulating layer T1 and the shunt MOS transistor 2 is surrounded by the trench insulating trench layer T2, the leakage of radio frequency signals from the p-type silicon layer 23 surrounded by the trench insulating layer T1 for the series MOS transistor 1 via the p-type silicon layer 23 between the trench insulating layers T1 and T2 to the p-type silicon layer 23 surrounded by the trench insulating layer T2 for the shunt MOS transistor 2 can be suppressed.

Okashita, 6:1-16

Yu is “reasonably pertinent” to the problem addressed by the ‘886 Patent

Each type of silicon wafer utilized for fabricating such semiconductor structures suffers from attendant drawbacks. For example, it is difficult to electrically isolate semiconductor structures fabricated on a conventional bulk silicon wafer, because although such semiconductor structures can be partially electrically isolated by virtue of, for example, their isolating trenches, electric current can still flow under such trenches, leading to, for example, voltage and current fluctuations. Neighboring semiconductor devices, e.g. neighboring cascaded transistors, in such structures thus tend to interfere with one another when fabricated on bulk silicon wafers. In contrast, it is easier to electrically isolate semiconductor structures or circuits implemented on a conventional silicon on insulator wafer, in which a buried oxide layer provides additional isolation. Unfortunately, circuits designed for fab-

Yu, Fig. 10

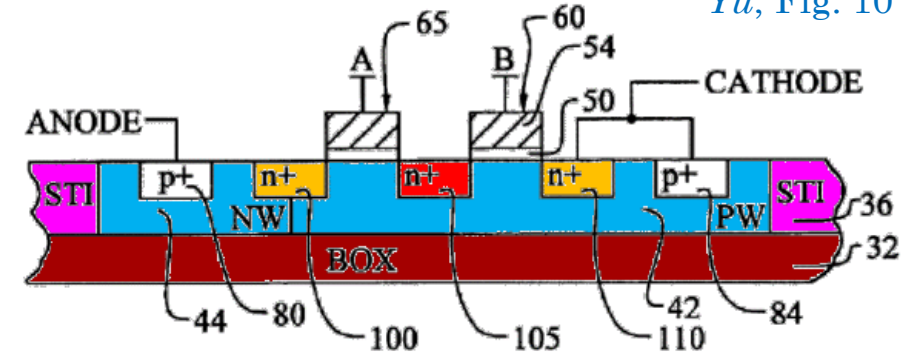


FIG. 10

The SCR and LVT-SCR devices of the prior present several difficulties in integration with a SOI process. In an SOI process, the devices must be formed in a relatively thin silicon layer overlying a buried insulator layer. This buried insulator layer, in turn, overlies the bulk substrate. The presence of the buried insulator layer improves MOS transistor performance, especially for very short channel devices, and reduces substrate coupling issues by providing excellent device-to-device isolation. Typically, the STI regions are formed down to the buried insulator layer such that each active area is completely isolated from other active areas.

Yu, 1:59-2:3

‘886 Patent, 1:29-43

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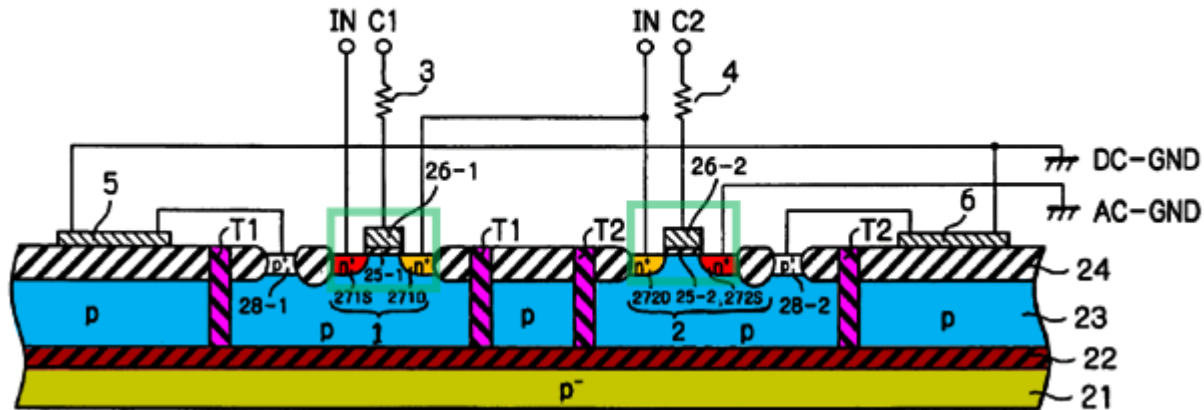
‘886 Patent, 2:65-3:11

Combination of *Yu* and *Okashita*

Both devices have transistors that are fabricated on an SOI structure

Thompson Decl. ¶176.

Fig. 9



Petition 8; *Okashita*, Fig. 9

In FIG. 9, reference numeral 21 designates a monocrystalline silicon substrate 21 on which a silicon oxide layer 22 is formed. Also, a p-type silicon layer 23 is grown on the silicon oxide layer 22, thus realizing an SOI configuration.

Okashita, 5:41-44

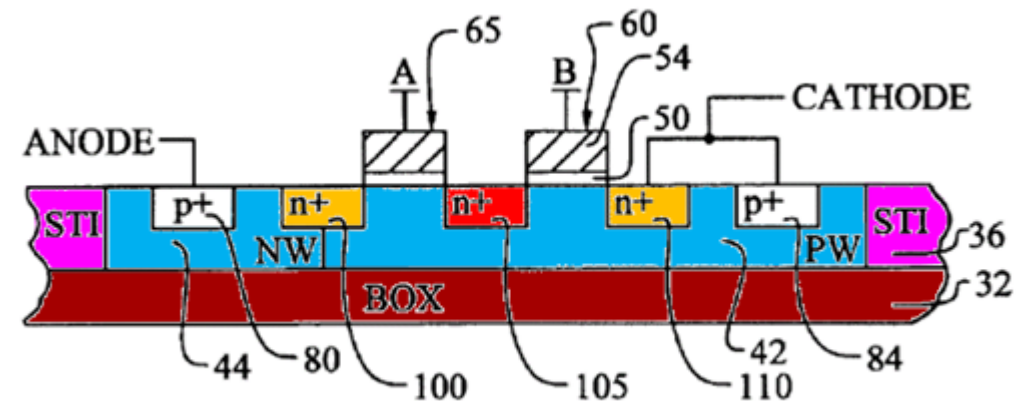


FIG. 10

Petition 41; *Yu*, Fig. 10

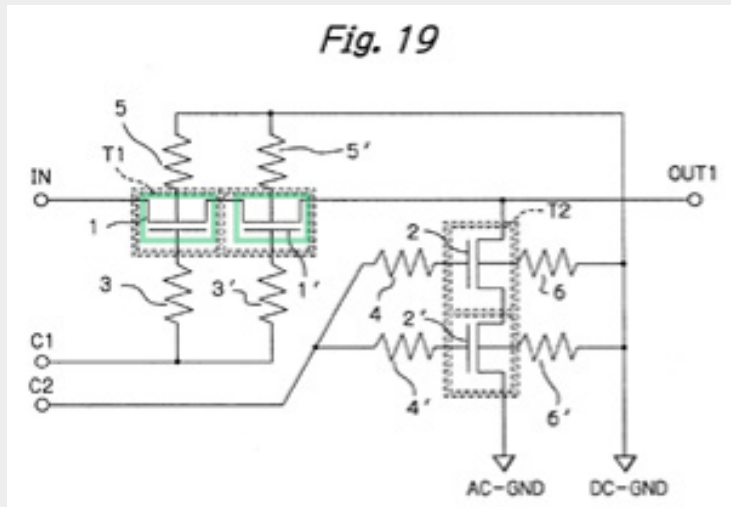
method of the present invention is shown. The present invention applies to any SOI system. In this case, the SOI system, shown in cross-sectional representation, comprises a buried oxide layer 32 overlying a substrate 30. For example,

Yu, 3:54-57

Combination of *Yu* and *Okashita*

The transistors in *Okashita* and *Yu* are also both “cascaded”

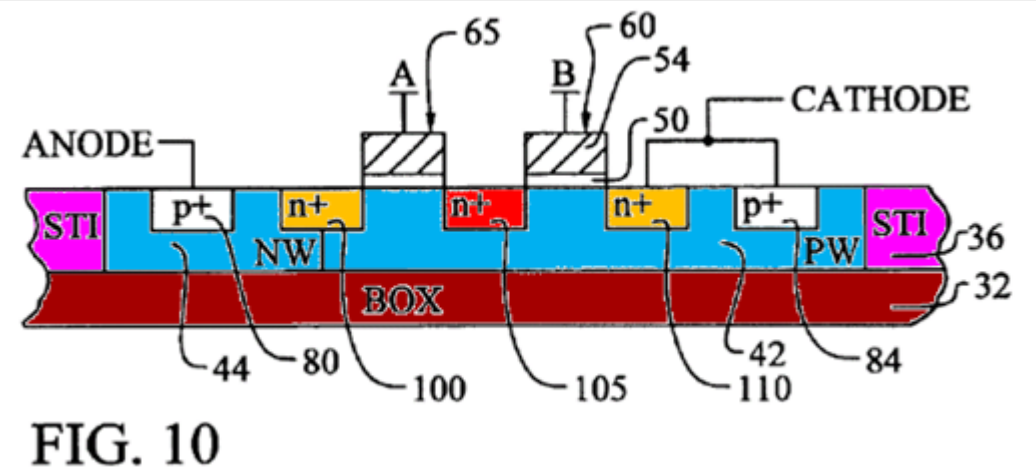
Thompson Decl. ¶176



Petition, 29; *Okashita*, Fig. 19

In FIG. 19, which illustrates a fourth embodiment of the semiconductor switch apparatus according to the present invention, a series MOS transistor 1' along with its gate protection resistor 3' and a resistor 5' is connected in series to the series MOS transistor 1 of FIG. 7, and a shunt MOS

Okashita, 8:30-34



Petition, 41; *Yu*, Fig. 10

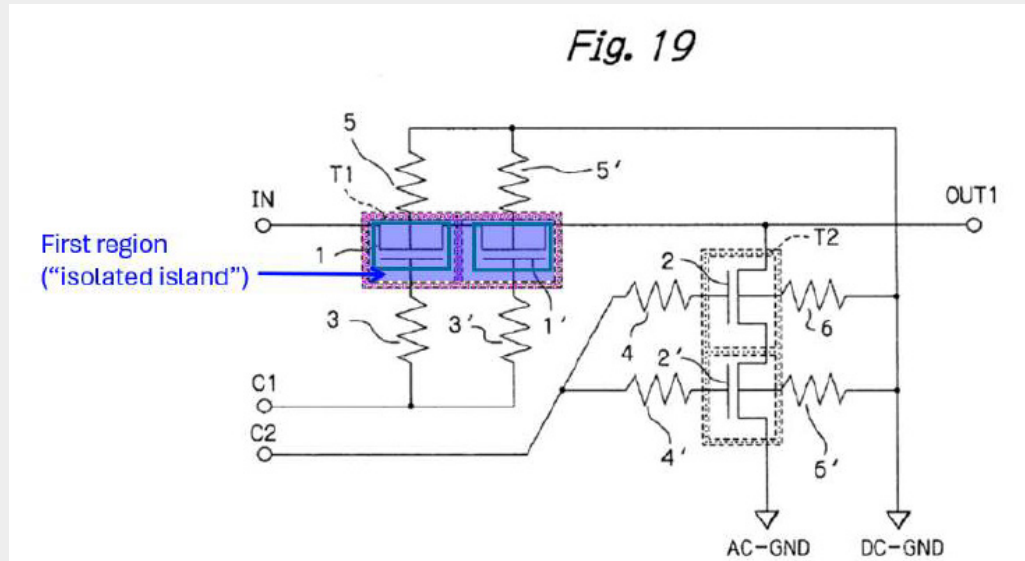
Two MOS transistors are formed by the gates 60 and 65. In particular, a first NMOS transistor is formed by first gate 60, third doped region 110, and fourth doped region 105. A second MOS transistor is formed by second gate 65, fourth doped region 105, and fifth doped region 100. The first and second transistors are in series between the third doped region 110 and the fifth doped region 100. Further, the fifth doped region 100 is coupled to the second well 44, and the third doped region 110 is coupled to the first doped region 105 to form the cathode. Therefore, the first and second NMOS transistors are cascaded, or stacked, between the cathode terminal and the second well 44. Finally, the first gate 60 is

Yu, 5:44-55

Combination of *Yu* and *Okashita*

The transistors in *Okashita* and *Yu* are also both ... situated within an isolated island that is surrounded by a **shallow trench isolation (STI) region 36**.

Thompson Decl. ¶176



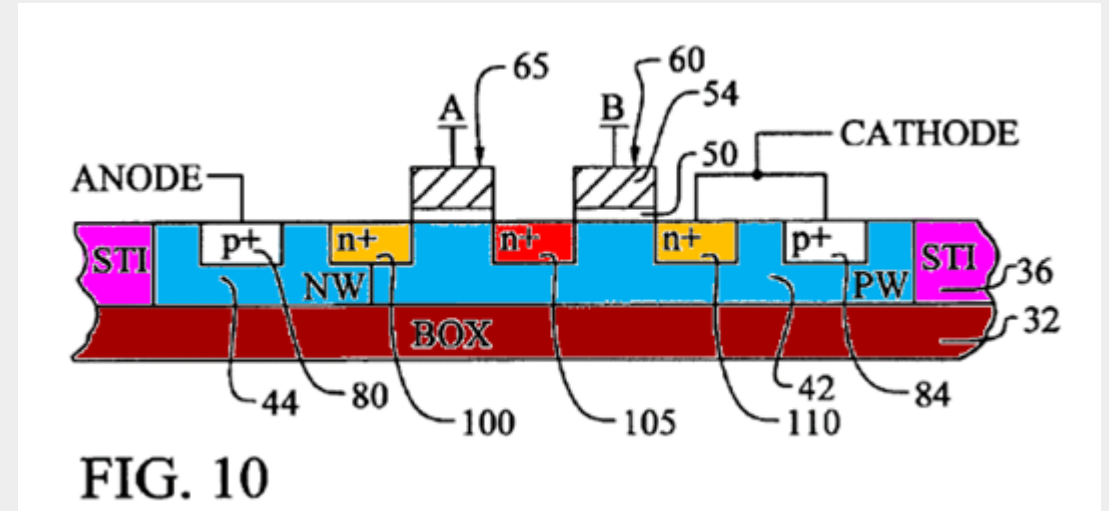
Reply, 3; *Okashita*, Fig. 19

a plurality of series MOS transistors formed within a first region of said semiconductor layer and connected in series between said input terminal and said output terminal;

Okashita, 10:54-57

a first trench insulating layer surrounding said series MOS transistors; and

Okashita, 10:64-65



Petition, 41; *Yu*, Fig. 10

Referring now to FIG. 4, shallow trench isolations (STI) 36 are formed in the silicon layer 60 using methods well known in the art. These STI regions 36 define active area regions of silicon layer 34 where active devices may be subsequently formed. Of particular importance to the

Yu, 4:8-12

Thompson Decl., ¶176; Petition, 42-43; Reply, 3;
Okashita, 10:54-57, 10:64-65; *Yu*, 4:8-12.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Combination of *Yu* and *Okashita*

[B]both devices operate (switch between ON and OFF states) at comparable voltages—*Yu*'s device turns on at approximately 3.3V (*Yu*, 6:4–31), and *Okashita*'s at 3V (*Okashita*, 7:34–39).

Reply, 8

The novel, LVT-SCR device provides a low triggering voltage level. This is because the NMOS stack will turn ON at a relatively low anode-to-cathode voltage. However, as a distinct advantage, the turn-ON voltage is a voltage threshold above the voltage A on the second gate 65. Further, since the two NMOS transistors are stacked, neither device must sustain the entire anode-to-cathode voltage during the OFF state.

In particular, the LVT-SCR device can be used in one of two ways. First, if the device is used to protect an input pin, then the voltage B on the first gate 60 is biased to ground. The voltage A on the second gate 65 is biased to the positive supply voltage of, for example, about 3.3 Volts. The anode is tied to the input pad, and that the cathode is tied to ground. Assuming that the anode is driven externally to about 5.0 Volts, then the center diffusion between the first and second NMOS transistors will be about 2.8 Volts. In this condition, the NMOS stack is OFF and, yet, neither of the NMOS transistors is required to sustain any voltage exceeding the 3.3 Volt level. Therefore, the operating mode is within a range for excellent, gate oxide injection (GOI) and hot carrier injection (HCI) reliability.

Second, the LVT-SCR device may be used as an output protection device. The anode is again coupled to the pad, while the cathode is coupled to ground. The voltage A of the second gate 65 is again coupled to the power supply level of about 3.3 Volts. In this case, however, the voltage B of the first gate 60 is coupled to the control signal of the output. That is, assuming that the anode is further coupled to an output driver on the same integrated circuit, then the B signal is coupled to the control signal of that output driver, such as an inverter buffer. Again, this configuration insures that the neither of the stacked NMOS devices 60 and 65 sustains a voltage above the internal supply of about 3.3 Volts.

Yu, 6:4-39

When a high voltage such as 3V is applied to the control terminal C, the transistors 321, 322, 323 and 324 are turned ON, OFF, OFF and ON, respectively. As a result, the voltages at the terminals C1 and C2 are 3V and -3V, respectively, so that the MOS transistors 1 and 2 are turned ON and OFF, respectively. Therefore, a radio frequency signal call be transmitted from the input terminal IN via the MOS transistor 1 to the output terminal OUT1. In this case, since the gate voltage of the MOS transistor 2 is very low (-3V), the MOS transistor 2 is not turned ON even if the amplitude of radio frequency signals at the input terminal IN is large.

On the other hand, when a low voltage such as 0V is applied to the control terminal C, the transistors 321, 322, 323 and 324 are turned OFF, ON, ON and OFF respectively. As a result, the voltages at the terminals C1 and C2 are -3V and 3V, respectively, so that the MOS transistors 1 and 2 are turned OFF and ON, respectively.

Okashita, 7:34-52

Combination of *Yu* and *Okashita*

Yu discloses fabrication methods that improve thermal and electrical performance in similar trench isolated SOI transistors. Pet., §§V.C.1–2; Thompson, ¶¶89–98, 176–180.

Reply, 9

The SCR and LVT-SCR devices of the prior present several difficulties in integration with a SOI process. In an SOI process, the devices must be formed in a relatively thin silicon layer overlying a buried insulator layer. This buried insulator layer, in turn, overlies the bulk substrate. The presence of the buried insulator layer improves MOS transistor performance, especially for very short channel devices, and reduces substrate coupling issues by providing excellent device-to-device isolation. Typically, the STI regions are formed down to the buried insulator layer such that each active area is completely isolated from other active areas.

However, these characteristics cause several problems for SCR devices formed in an SOI process having STI isolation. First, the presence of the STI regions within the SCR and LVT-SCR devices reduces the lateral heat transfer property during an ESD event. Consequently, the devices fail at a lower energy dissipation level. Second, the STI pull-down

Yu, 1:59-2:9

Referring again to FIG. 10, another important feature of the present invention is shown. The doped regions 80, 84, 100, 105, and 110, are formed in the upper part of the wells 42 and 44 and do not extend to the buried oxide layer 32.

That is, the original silicon layer in which the doped regions are formed is thick enough so that the doped regions do not completely deplete the wells 42 and 44. This version of the LVT-SCR device of the present invention is said to be a partially depleted device.

Yu, 6:46-54

Combination of *Yu* and *Okashita*

Indeed, a POSITA would have recognized that, due to the lower thermal conductivity of silicon dioxide compared to silicon, if the source/drain junctions of Okashita's cascaded transistors were to contact the silicon oxide layer, the transistors would operate at higher temperatures, which could then negatively impact circuit performance and "fail at a lower energy dissipation level" as taught by Yu. Yu, 2:4-17; see also Ex. 1010, 59-60; Ex. 1013, 27-28; see Ex. 1022, 1

Thompson Decl., ¶179

Self-heating is a serious disadvantage for SOI, particularly when applied to analog circuits, although self-heating can also reduce the performance of logic circuitry and cause an increase in leakage. Self-heating has two

Ex. 1010, 59

The buried oxide reduces thermal conductivity to the substrate (compared to bulk) resulting in locally increased temperature. This can impact circuit performance, and possibly reliability [2.27]. In addition to buried oxide, devices are relatively isolated from adjacent devices because of the use of trench isolation.

Ex. 1010, 60

Self-heating in SOI represents another design constraint. The thermal conductivity of silicon dioxide is about two orders of magnitude lower than that of silicon. If the

Ex. 1013, 27

First, the presence of the STI regions within the SCR and LVT-SCR devices reduces the lateral heat transfer property during an ESD event. Consequently, the devices fail at a lower energy dissipation level. Second, the STI pull-down

Yu, 2:6-9

as clock distribution network). Detailed thermal modeling and measurements have shown that under static operating conditions with the device always on, the rise in the channel temperature for SOI devices can be an order of magnitude higher than that for the bulk Si, sometimes in excess of 100°C [73]. The higher channel operating temperature causes negative differential conductance at high gate biases [71], degrades the device mobility, and reduces the maximum drain saturation current. This imposes a severe constraint for analog applications, where most devices can

Ex. 1013, 28

Independent claim 1 and Yu

1. A switching circuit comprising:
a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;
each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;
at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.

'886 patent, claim 1

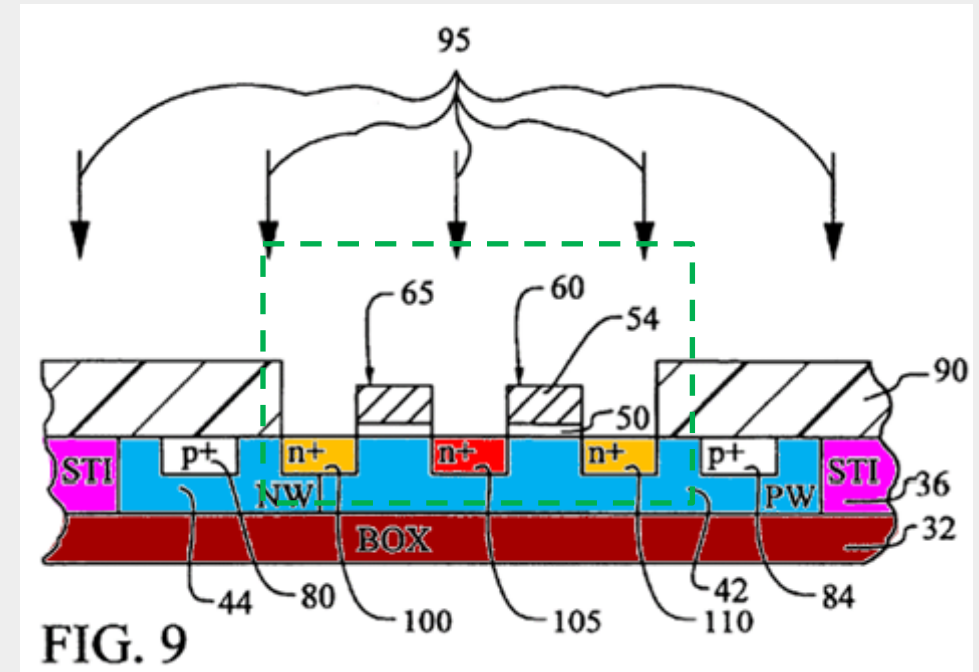


FIG. 3

Yu, Figs. 3, 9

Yu Discloses [1pre], [1a], and [1c] of Independent claim 1 - Undisputed

- [1a] 1. A switching circuit comprising:
a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;
- [1c] at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.

'886 patent, claim 1

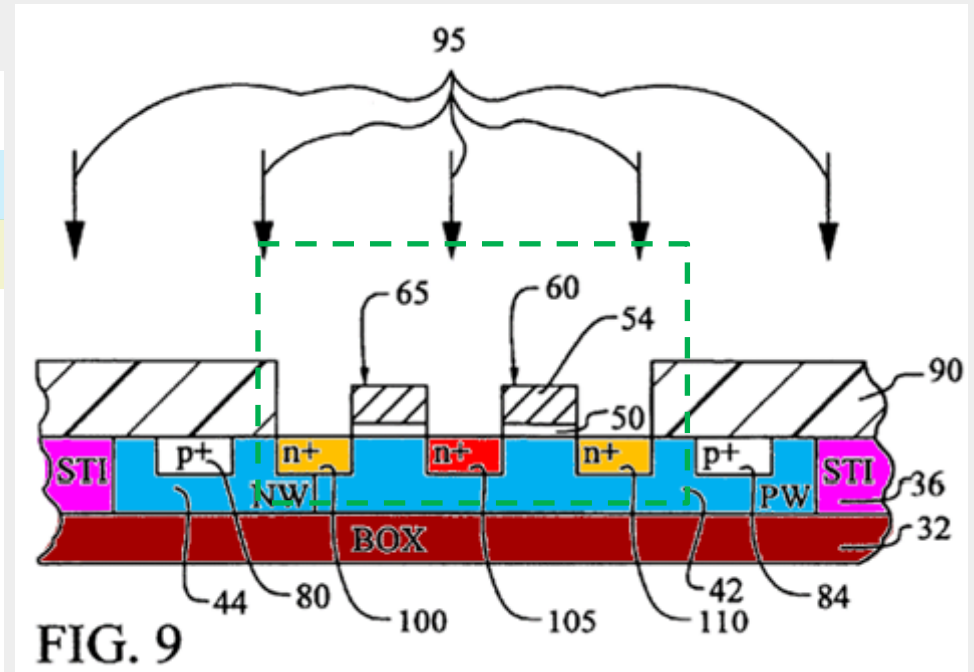


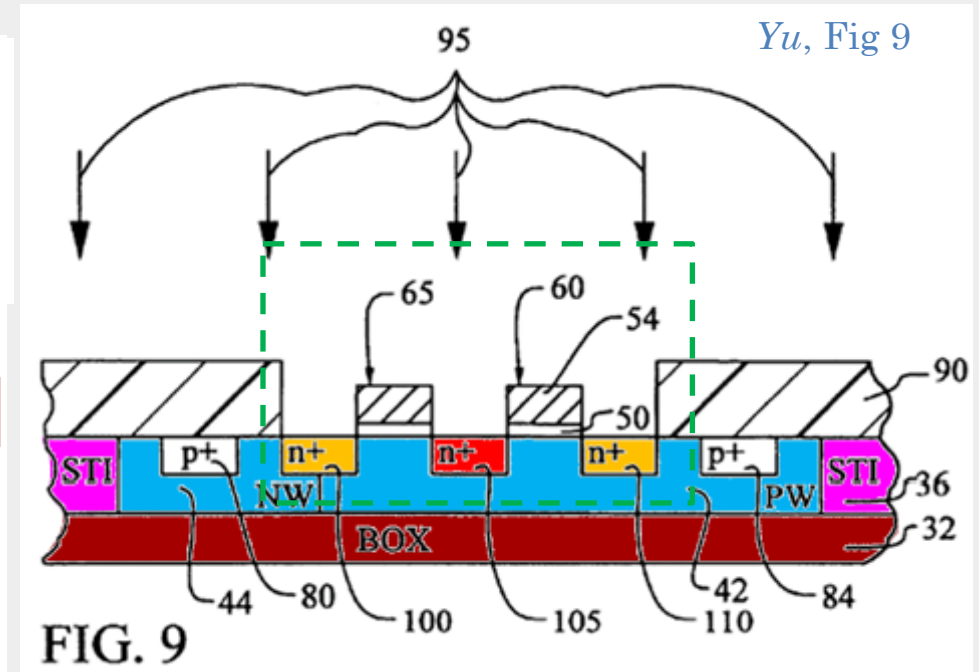
FIG. 3

Yu, Figs. 3, 9

“A Source/Drain Junction” of *Yu*’s Cascaded Transistors do not Contact the BOX layer

[1b] each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;

'886 patent, claim 1



Like '886 Patent, No Physical Contact in *Yu*

Patent Owner's argument is unpersuasive because claim 1 requires the source/drain junction not to contact the buried oxide layer. The '886 patent indicates that the contact precluded is *physical* contact, which provides the beneficial features. For example, the '886 patent states that prior art sources and drains "typically extend all the way through device layer [] and contact the top surface of [the] buried oxide layer," which leads to "no, or almost no, capacitive load." Ex. 1001, 3:15–21. The configuration taught in the '886 patent, in contrast, "do[es] not extend all the way through device layer 202 to contact the top surface of the buried oxide layer 204," providing "an associated junction capacitance." *Id.* at 4:8–18. Accordingly, the "source/drain junction capacitance" that is "thereby formed" in claim 1 appears to be due to the fact that the "source/drain junction [] does not contact said buried oxide layer." *Id.* at 9:1–4.

Institution Decision, 23-24

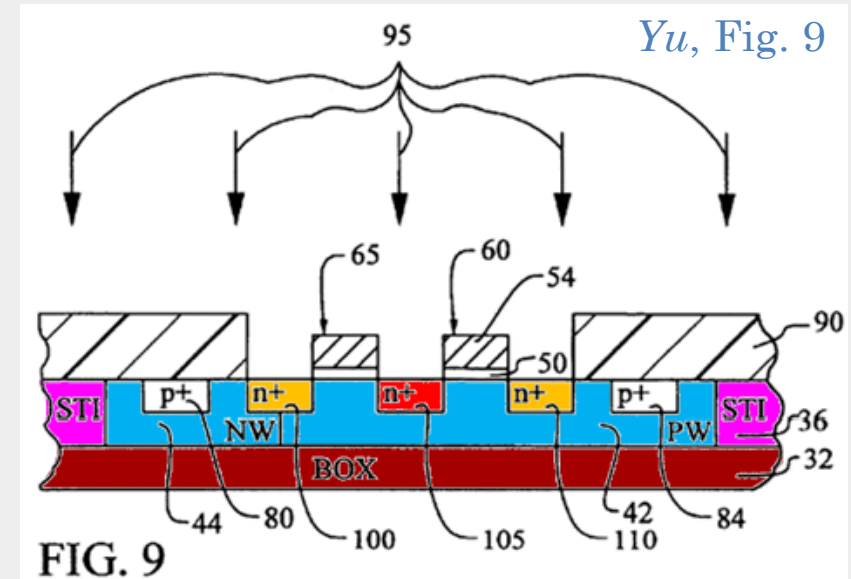


FIG. 9

Referring again to FIG. 10, another important feature of the present invention is shown. The doped regions 80, 84, 100, 105, and 110, are formed in the upper part of the wells 42 and 44 and do not extend to the buried oxide layer 32. That is, the original silicon layer in which the doped regions are formed is thick enough so that the doped regions do not completely deplete the wells 42 and 44. This version of the LVT-SCR device of the present invention is said to be a partially depleted device.

Yu, 6:46-54

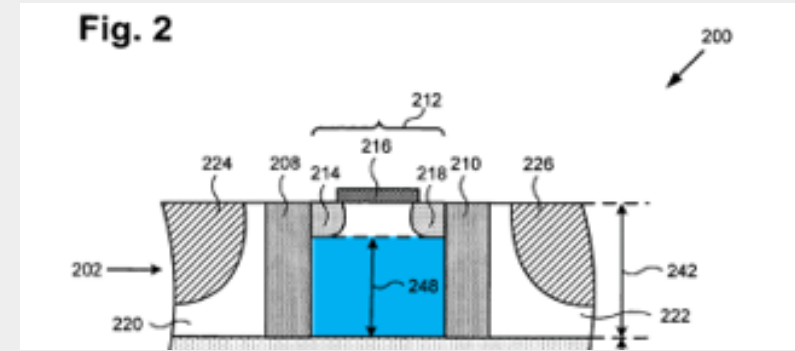
“A Source/Drain Junction” Requires Only One of the Source Junction or the Drain Junction, Not Both

1. A switching circuit comprising:
a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;

each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;

at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.

‘886 patent, claim 1



‘886 patent, Fig. 2

Structure 200 comprises semiconductor devices, such as for example transistor 212, which in one embodiment could be, for example, an NFET or a PFET transistor. Continuing with this example, transistor 212 comprises source 214, gate 216, and drain 218. Because of the increased thickness of device layer 202, source 214 and drain 218 do not extend all the way through device layer 202 to contact the top surface of buried oxide layer 204. Instead, a layer with intervening thickness 248 remains between the bottom surfaces of source 214 and drain 218 and the top surface of buried oxide layer 204. Consequently, a semiconductor junction is formed by source 214 and drain 218 within device layer 202. Each such semiconductor junction will have an associated junction capacitance, e.g. the source/drain junctions of transistor 212 have corresponding source/drain junction capacitances.

‘886 patent, 4:4-18.

“A Source/Drain Junction” Requires Only One of the Source Junction or the Drain Junction, Not Both



“This court has repeatedly emphasized that an indefinite article ‘a’ or ‘an’ in patent parlance carries the meaning of ‘one or more.’”

KCJ Corp. v. Kinetic Concepts, Inc., 223 F.3d 1351, 1356 (Fed. Cir. 2000)

“A Source/Drain Junction” Requires Only One of the Source Junction or the Drain Junction, Not Both

- The “/” between source and drain in “source/drain junction” means source or drain.

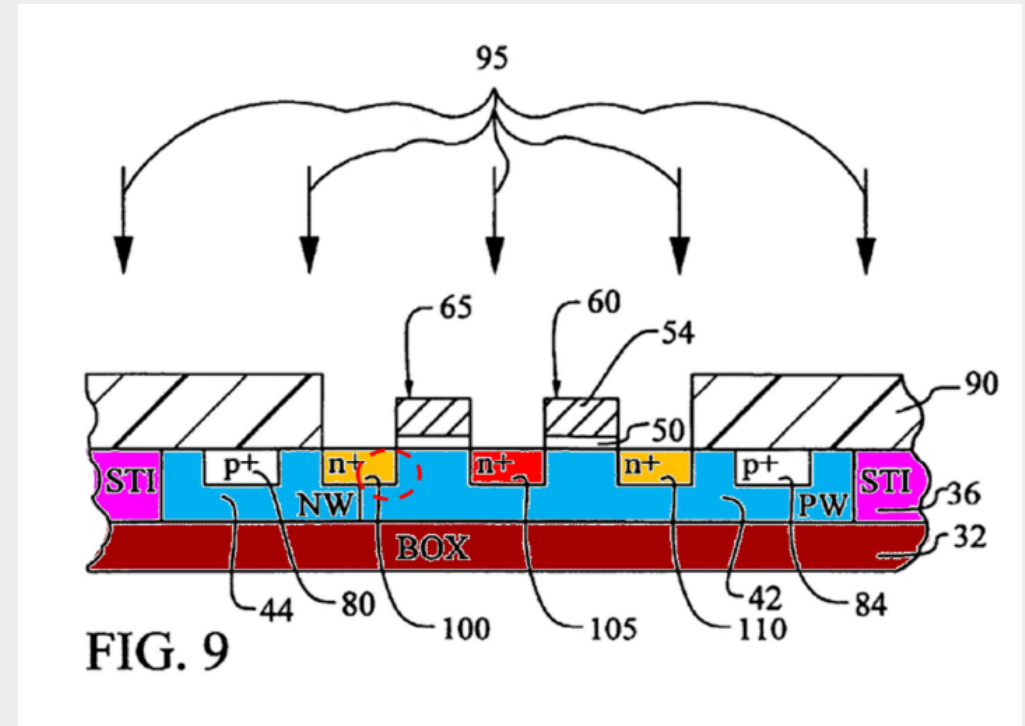
6.112 *Signifying alternatives.* A slash most commonly signifies alternatives. In certain contexts it proves convenient shorthand for or (but see 6.113). It is also used for alternative spellings or names. Where one or more of the terms separated by slashes is an open compound, a thin space before and after the slash is helpful.

Ex. 1030, 4 (6.112)

Junction Capacitance in *Yu*

9. A POSITA would understand that, during operation of *Yu*'s second transistor, source/drain junction capacitance arises from the PN junctions formed between the N+ doped regions 100 and 105 (serving as the drain and source, respectively) and the underlying p-well 42. This capacitance results from the depletion region that develops at the interface between the N+ and P-type materials. Specifically, the portion of N+ region 100 located on the p-well 42 (highlighted with a dashed red circle in the figure below) forms a PN junction. See Ex. 1011, 10 ("pn junctions [] are formed by the drain-bulk and source-bulk interfaces in a MOSFET"), 11 (Fig. 1.36). A POSITA would also recognize that, during transistor operation, a depletion region forms at the interface between N+ region 100 and the p-well 42, resulting in junction capacitance across that region. See Ex. 1011, 10, 11; Ex. 1010, 43, 45.

Thompson-Supp Decl., ¶9

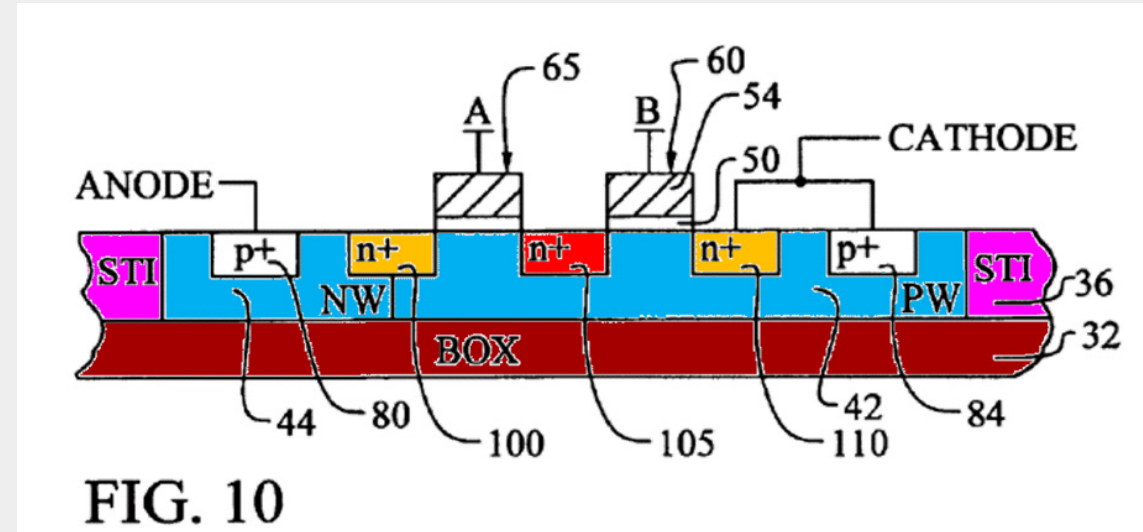


Reply, 14; *Yu*, Fig. 9

Yu Discloses the Limitations of Dependent Claim 3 - Undisputed

3. The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer.

'886 patent, claim 3



Yu, Fig. 10; Thompson-Supp Decl., ¶207

Fabrication of *Burgener's* FETs Using SOI Techniques

Integrated Circuit Fabrication and Design

[0105] Integrated circuit fabrication details are not provided in the above description. In some preferred embodiments, including some which have output powers in excess of 1 W at around 2.4 GHz, the integrated circuits may be fabricated in accordance with ultrathin silicon on sapphire processing as described in U.S. Pat. No. 5,663,570, issued Sep. 2, 1997 and entitled “High-Frequency Wireless Communication System on a Single Ultrathin Silicon On Sapphire Chip.” Other semiconductor-on-insulator (SOI) techniques may be used to fabricate a dual-band transceiver integrated circuit as described above, for at least some frequency bands and power levels.

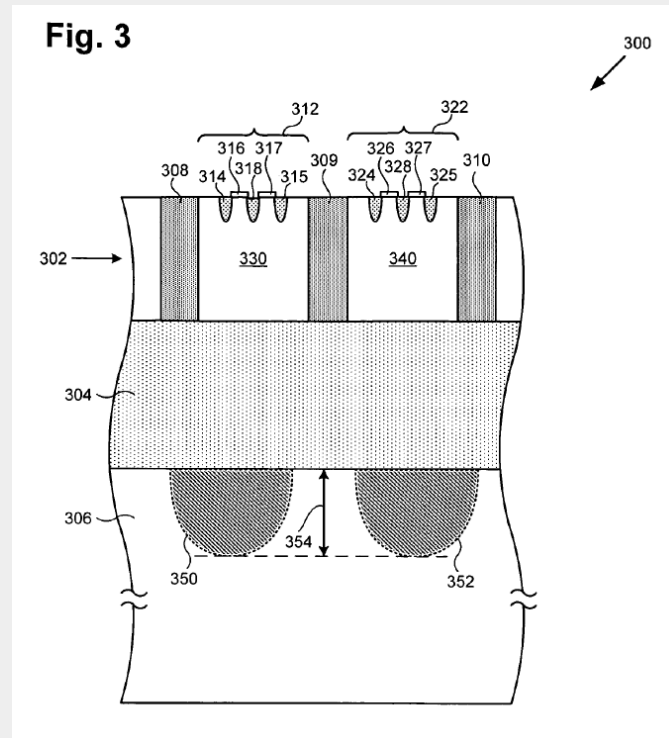
Burgener, ¶105

22. A POSITA would have understood that a silicon-on-sapphire (SOS)

substrate is a type of semiconductor-on-insulator (SOI) substrate, where the buried oxide (BOX) layer made of silicon dioxide is replaced with sapphire. *See* Ex. 1010, 28–29. Like the SOI substrate in *Okashita*, the SOS substrate used in UTSi technology features a silicon layer—used to fabricate CMOS devices—positioned above an insulating sapphire layer. *See* Ex. 2004, 9:57–67; Ex. 1010, 28–30. Given Thompson-Supp Decl., ¶22

No Evidence That *Okashita's* FET Configuration Increases Capacitance

- The '886 patent itself contradicts HID's unsupported assertion

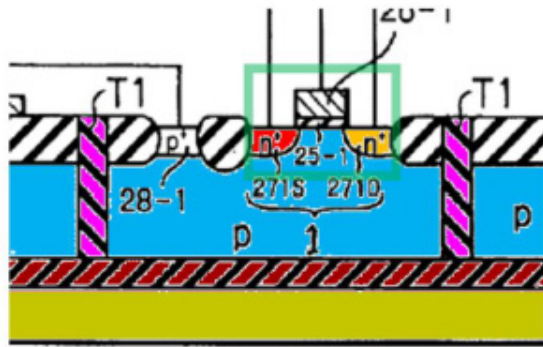


Because of the significantly greater thickness of device layer 302, semiconductor material, e.g. silicon, remains between the bottom surfaces of the sources and drains of transistors 312 and 322 and the top surface of buried oxide layer 304 (such remaining semiconductor corresponds to the semiconductor remaining in thickness 248 in structure 200) in islands 330 and 340. This remaining semiconductor would result in source/drain junction capacitance, similar to the junction capacitance of structure 200 as discussed above.

It should be noted that the effect of the resulting capacitive load from source/drain junction capacitances in structure 200 or structure 300 is advantageously reduced by taking advantage of the thick buried oxide layer 204 or 304 and the high resistivity of bulk silicon layer 206 or 306. For example, the greater thickness of buried oxide layer 304 can reduce the effect of junction capacitances in transistors 312 and 322, and the higher resistivity of bulk semiconductor layer 306 can further reduce such capacitances by facilitating the formation of thick depletion regions 350 and 352, thereby reducing the effect of source/drain junction capacitances loading transistors 312 and 322. Moreover, preserving the advantages of SOI structures, during operation of transistors 312 and 322, islands 330 and 340 can withstand large positive and negative voltage excursions because of the electrical isolation provided by adjacent trenches 308, 309, and 310, and buried oxide layer 304.

'886 patent, 5:57-6:15

Junction Capacitance in *Okashita's* BC-SOI FETs Depends on Junction Voltage



Okashita, Fig. 9
(cropped and enlarged to show transistor 1)

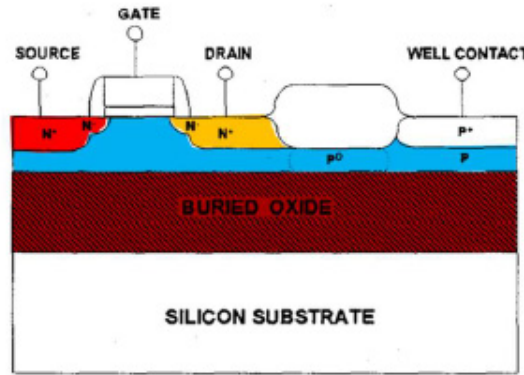


Fig. 1. A cross-sectional illustration of BC-SOI MOSFET structure.

Ex. 1014, Fig. 1

Thompson-Supp Decl., ¶11

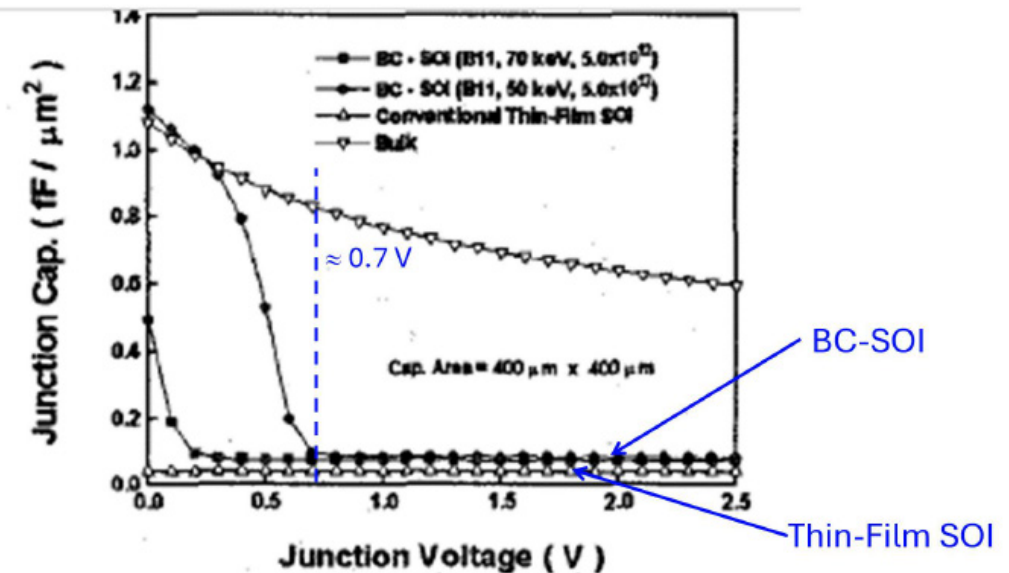


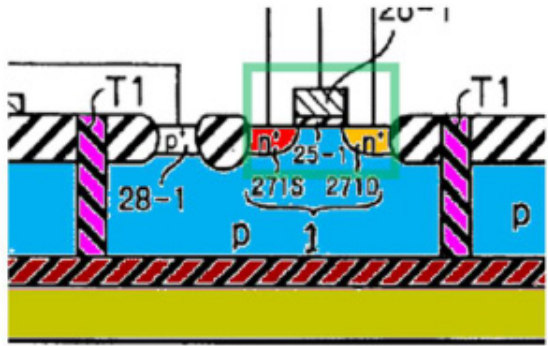
Fig. 11. A n^+ junction capacitance characteristics of BC-SOI MOSFET structure compared with that of bulk-silicon MOSFET.

Ex. 1014, 5; Thompson-Supp Decl., ¶13

13. At junction voltages below approximately 0.7 volts, as shown in the data presented in Ex. 1014 (Fig. 11, below), the junction capacitance of a body-contacted SOI (BC-SOI) transistor (represented by the curve with data points marked by the symbol •) is higher than that of a thin-film SOI transistor (represented by the curve with data points marked by the symbol Δ). Notably, Mr. Berg characterizes Burgener's transistor as a thin-film SOI transistor. See Berg, ¶¶68, 70. However, at higher junction voltages, the capacitance values of the two transistor types become comparable.

Thompson-Supp Decl., ¶13

Gate Delay in *Okashita's* BC-SOI FETs Depends on Supply Voltage



Okashita, Fig. 9

(cropped and enlarged to show transistor 1)

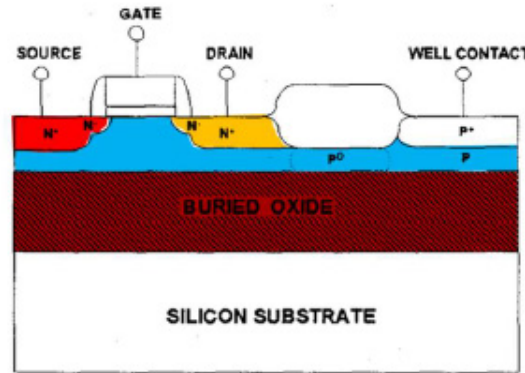


Fig. 1. A cross-sectional illustration of BC-SOI MOSFET structure.

Ex. 1014, Fig. 1

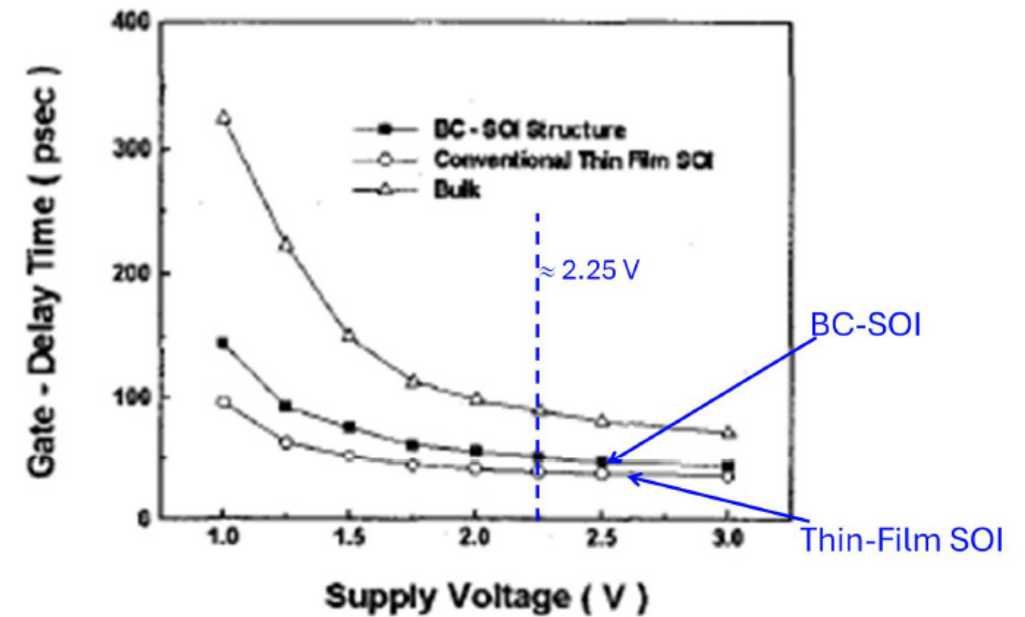


Fig. 12. Gate-delay time characteristics with supply voltage with field-stop implantation condition as a parameter with conventional and bulk counterparts.

Ex. 1014, 5 (Fig. 12) (annotated).

Thompson-Supp Decl., ¶14

14. Similarly, based on the data presented in Ex. 1014 (below), a POSITA would understand that the gate-delay time of *Okashita's* body-contacted SOI (BC-SOI) transistors is slightly higher than that of thin-film SOI transistors at supply voltages below approximately 2.25 volts. However, at higher supply voltages, the delay times of the two transistor types become comparable.

Thompson-Supp Decl., ¶14

Okashita's BC-SOI FETs Result in High-Speed Circuit

thin-silicon film beneath the field oxide. The BC-SOI structure has several advantages, such as relatively high isolation punchthrough voltage, high drain-to-source breakdown voltage compared with conventional thin-film SOI MOSFET and small junction capacitance compared with bulk MOSFET, resulting in high-speed circuit operation.

Ex. 1014, 2

15. Furthermore, contrary to Mr. Berg's assertions, Ex. 1014 discloses that body-contacted SOI transistors, such as *Okashita's* transistors, offer several advantages over conventional thin-film SOI transistors. For instance, Ex. 1014 discloses that BC-SOI transistors exhibit a "relatively high isolation punchthrough voltage, high drain-to-source breakdown voltage compared with conventional thin-film SOI MOSFET and [a] small junction capacitance compared with bulk MOSFET, resulting in high-speed circuit operation." Ex. 1014, 2.

Thompson-Supp Decl., ¶15

Thermal Considerations for FETs in *Burgener's* Antenna Switch

[0009] Integration of devices is generally desirable in order to improve various features of the resulting product, such as operating frequency and reliability, and may also reduce overall manufacturing costs, as well as likely reducing the volume occupied by the circuits. Field Effect Transistors (FETs) are extremely popular for both linear amplification and switching purposes in integrated circuits. However, integrated circuit (IC) FETs have a limited capability to withstand voltage between any two nodes, including gate-source, gate-drain, and drain-source node pairs. Such voltage withstand limitations may particularly impair the usefulness of IC FETs in high power switching circuits, in which inductive voltages may greatly exceed the supply voltage. As a particular example, the transmission output

Burgener, ¶[9]

[0044] FET stacks with at least nine FETs in series have been fabricated or simulated, and stacks of even more series FETs are certainly possible. Note that physical circuit couplings generally include finite capacitance, inductance, and resistance. For many purposes it is preferred that the FETs of the FET stack 200 be coupled with minimal impedance in series, drain to source. However, impedance may be intentionally added to such couplings. For example, it may be desirable to more closely control a drive impedance, and to dissipate heat in specific resistive series coupling elements rather than within the FETs themselves. It may also be desirable to add impedance between the FETs of the FET stack 200 so as to tune the conductance of the drive circuit.

Burgener, ¶[44]

1006, ¶ [0044]. And even there, Burgener only discusses dissipating heat “in specific resistive series coupling elements rather than within the FETs themselves.”

Id. Because Burgener states that dissipating heat inside the FETs is *not* desirable (rather, heat should be dissipated in the resistive couplings), the POSITA would not have been motivated to fabricate the transistors using what Dr. Thompson contends

Berg Decl., ¶71.

Thermal Considerations for SOI Transistors

Temperature rise can be significant even at relatively low power dissipations. As with bulk silicon, these effects are layout dependent.

Ex. 1010, 59

The buried oxide reduces thermal conductivity to the substrate (compared to bulk) resulting in locally increased temperature. This can impact circuit performance, and possibly reliability [2.27]. In addition to buried oxide, devices are relatively isolated from adjacent devices because of the use of trench isolation.

Ex. 1010, 60

Silicon-on-insulator (SOI) circuits promise advantages in speed and processing expense compared to circuits made from bulk silicon (e.g., Peters, 1993). The buried silicon-dioxide layer in SOI circuits has a very low thermal conductivity, which results in a large thermal resistance between the device and the chip packaging. This is a major problem for transistors that experience brief pulses of heating, such as ESD protection devices (e.g., Amerasekera et al., 1992), for which the temperature rise is dominated by conduction within micrometers of active regions. Lateral conduction parallel to the plane of the

Ex. 1022, 1

Self-heating in SOI represents another design constraint. The thermal conductivity of silicon dioxide is about two orders of magnitude lower than that of silicon. If the

Ex. 1013, 27

Thermal Considerations for SOI Transistors

previously explained (*see* Thompson, ¶¶51, 214), a POSITA would have understood that because the source/drain junctions of SOI transistors are in contact with the buried oxide layer—which has a thermal conductivity approximately two orders of magnitude lower than silicon—heat removal is less efficient than when a silicon layer is inserted between the junctions and the buried oxide layer.

Thompson-Supp Decl., ¶18

(continued)

Material	Thermal Conductivity W/(m K)	Coefficient of Thermal Expansion (CTE) (x10 ⁻⁶ m)
Copper	400	17
Aluminium	237	24
Nickel	90	13.6
Tungsten	160	4.3
Silver	419	18
Gold	318	14
GaN	130-225	3.1
Sapphire	40	8.4
Silicon	150	2.6
Diamond	900-1900	1.18

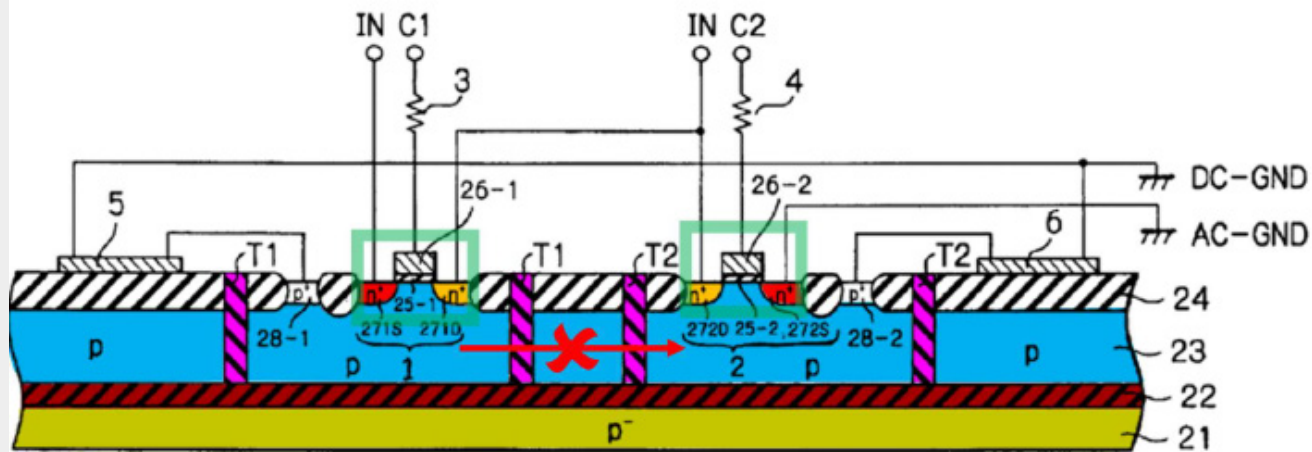
Ex. 1027, 7

conduction. The thermal conductivity of silicon is significantly higher than silicon dioxide and sapphire. Ex. 1013, 27; Ex. 1027, 6-7. Materials with high thermal conductivity, such as silicon, facilitate efficient heat transfer, allowing heat to dissipate quickly from active regions (such as the source/drain junctions) of a device. In contrast, materials like silicon dioxide and sapphire, which have much lower thermal conductivity, impede heat flow. This resistance to heat flow causes heat to accumulate near the heat source, such as the transistor's source/drain junctions, resulting in elevated operating temperatures. Therefore, when a

Thompson-Supp Decl., ¶19

Trenches Around *Okashita's* Transistors Prevent Leakage Through Silicon Above BOX Layer

Fig. 9



Reply, 23; Petition, 17

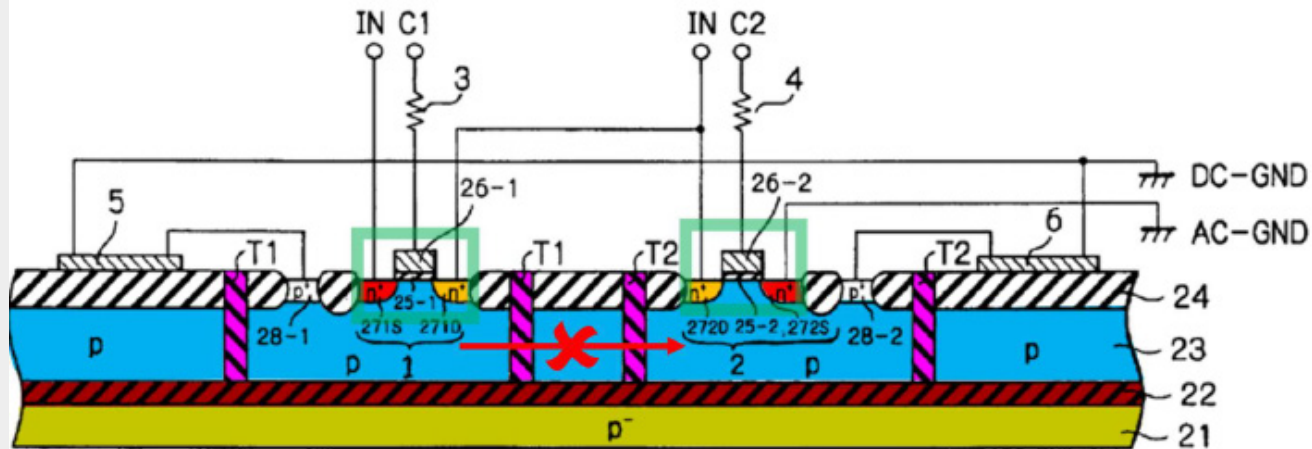
In FIGS. 8 and 9, since the SOI configuration is adopted, the leakage of radio frequency signals from the p-type silicon layer 23 surrounded by the trench insulating layer T1 for the series MOS transistor 1 via the silicon substrate 21 to the p-type silicon layer 23 surrounded by the trench insulating layer T2 for the shunt MOS transistor 2 can be suppressed.

Also, in FIGS. 8 and 9, since the series MOS transistor 1 is surrounded by the trench insulating layer T1 and the shunt MOS transistor 2 is surrounded by the trench insulating trench layer T2, the leakage of radio frequency signals from the p-type silicon layer 23 surrounded by the trench insulating layer T1 for the series MOS transistor 1 via the p-type silicon layer 23 between the trench insulating layers T1 and T2 to the p-type silicon layer 23 surrounded by the trench insulating layer T2 for the shunt MOS transistor 2 can be suppressed.

Okashita, 6:1-16

Implementing *Okashita's* Trenches in *Burgener* Prevents Inter-Device Leakage

Fig. 9

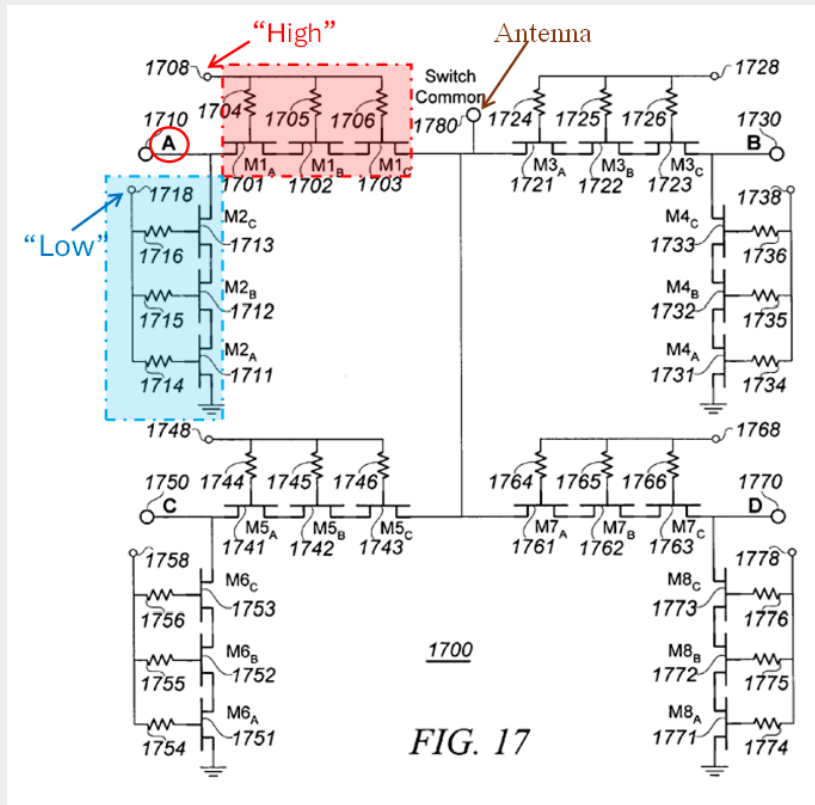


Reply, 23; Petition, 17

Fabrication of devices on an insulating substrate requires that an effective method for forming silicon CMOS devices on the insulating substrate be used. The advantages of using a composite substrate comprising a monocrystalline semiconductor layer, such as silicon, epitaxially deposited on a supporting insulating substrate, such as sapphire, are well-recognized, and can be realized by employing as the substrate an insulating material, such as sapphire (Al_2O_3), spinel, or other known highly insulating materials, and providing that the conduction path of any inter-device leakage current must pass through the substrate.

Ex. 2004 (*Burgener-II*), 9:57-67

Isolating FET Groups in *Burgener's* Antenna Switch Using *Okashita's* Isolation Trenches



Petition, 61; *Burgener*, Fig. 17

[0103] To couple an RF port to the common connection, a “high” voltage ($\sim V_{DD}$) is applied to the port’s corresponding “+” control node, while a “low” voltage ($\sim -V_{DD}$) is applied to the port’s corresponding “-” control node. Meanwhile, a “low” voltage is applied to each “+” control node corresponding to another RF port, and a “high” voltage is applied to each “-” control node corresponding to another RF port. Thereby, a selected RF port will be coupled to the common connection, while every other RF port will be coupled to ground. Thus, to couple RF port A 1710 to common connection 1780, a “high” voltage is applied to control nodes 1708, 1738, 1758, and 1778, while a “low” voltage is applied to all other control nodes (1718, 1728, 1748 and 1768).

Burgener, ¶103

Okashita's Transistors Use Trench Isolation, Not Isolation Wells

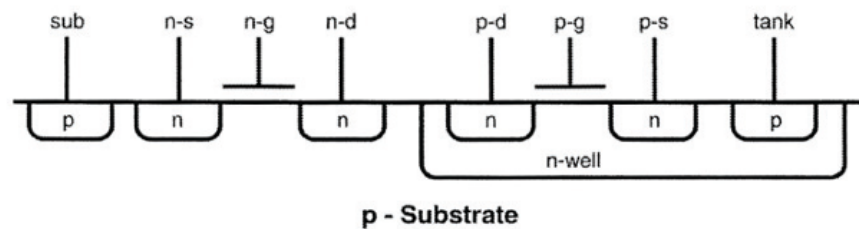


Figure 2.7: Simplified junction-isolated CMOS processed cross-section: The nMOS structure is generally constructed directly into the substrate or epitaxial material, and the pMOS normally is fabricated into an N-well diffused into the p-type silicon. The sources and drains are more heavily doped, shallower diffusions.

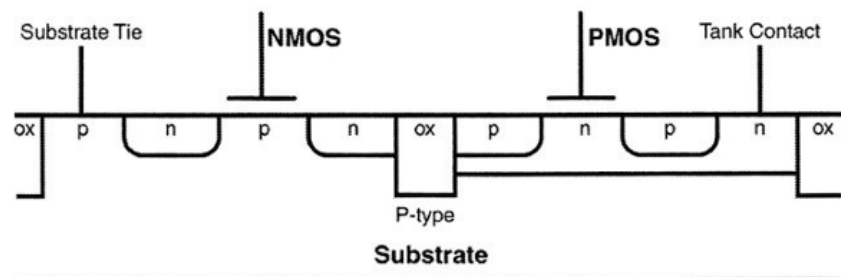


Figure 2.8: Simplified dielectric isolated CMOS process cross-section. Here the nMOS source/drains are diffused into a lightly doped P-type region, while the pMOS source drains are diffused into a lightly doped N-type region. Electrical isolation between structures is achieved with dielectrics, but the devices are electrically connected to the substrate either directly, or via a N-P junction diode.

Ex. 1010, 36

In integrated microelectronics circuits, electrical isolation is needed between adjacent semiconductor devices. Typical isolation technique consists of a combination of junction isolation and local oxidation of silicon (LOCOS). More recently, however, LOCOS isolation is being replaced with a shallow trench isolation (STI) process for deep sub-micron CMOS processes. In the case of high voltage devices for analog and power applications, LOCOS isolation in combination with deep trench isolation has been used [1–4]. If high voltage devices were to be isolated with junction isolation, the inter-device separations would become too large and impractical. Thus, the use of deep trench isolation significantly reduces the device size and the die size, hence reducing the device cost.

Ex. 1028, 1

2.3.1 Isolation Techniques

Bulk silicon processes use either junction isolation, or dielectric isolation. While both techniques are effective, junction isolation has the advantage of

Ex. 1010, 34

Trench Isolation Reduces Die Size Rather Than Increasing It

In integrated microelectronics circuits, electrical isolation is needed between adjacent semiconductor devices. Typical isolation technique consists of a combination of junction isolation and local oxidation of silicon (LOCOS). More recently, however, LOCOS isolation is being replaced with a shallow trench isolation (STI) process for deep sub-micron CMOS processes. In the case of high voltage devices for analog and power applications, LOCOS isolation in combination with deep trench isolation has been used [1–4]. If high voltage devices were to be isolated with junction isolation, the inter-device separations would become too large and impractical. Thus, the use of deep trench isolation significantly reduces the device size and the die size, hence reducing the device cost.

Ex. 1028, 1

2.3.1 Isolation Techniques

Bulk silicon processes use either junction isolation, or dielectric isolation. While both techniques are effective, junction isolation has the advantage of low cost. However, it has the disadvantage of requiring a relatively large silicon area to isolate structures, since lateral diffusion of an isolation tank is

Ex. 1010, 34-35.

It was well known that junction isolation consumes more silicon area than trench isolation. See Ex. 1010, 34 (“[Junction isolation) has the disadvantage of requiring a relatively large silicon area to isolate structures.”), 36 (“[Trench isolation) can be significantly more area efficient than junction isolation.”); Ex. 1028, 1 (“If high voltage devices were to be isolated with junction isolation, the inter-device separations would become too large and impractical. Thus, the use of deep trench isolation significantly reduces the device size and the die size, hence reducing the device cost.”).

Thompson-Supp Decl., ¶24