

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
SAMSUNG ELECTRONICS AMERICA, INC., and
NXP SEMICONDUCTORS, N.V.,¹

Petitioners,

v.

HARBOR ISLAND DYNAMIC, LLC,
Patent Owner.

IPR2024-01402
Patent 7,745,886 B2

Record of Oral Hearing
Held: January 7, 2026

Before HYUN J. JUNG, GREGG I. ANDERSON, and
ARTHUR M. PESLAK, Administrative Patent Judges.

1 NXP Semiconductors N.V. filed a petition and a motion for joinder in IPR2025-00954 that were granted and have been joined as petitioners in this proceeding.

APPEARANCES:

ON BEHALF OF THE PETITIONER:

JOSHUA L. GOLDBERG, ESQ.
of: Finnegan
1875 Explorer Street, Suite 800
Reston, VA 20190-6023
202-408-6092
joshua.goldberg@finnegan.com

ON BEHALF OF THE PATENT OWNER:

JOSEPH MERCADANTE, ESQ.
of: Fabricant LLP
411 Theodore Fremd Avenue, Suite 206 South
Rye, New York 10580
646-797-4343
jmercadante@fabricantllp.com

The above-entitled matter came on for hearing Wednesday, January 7, 2026, commencing at 1:30 p.m. EST, at the U.S. Patent and Trademark Office, 600 Dulany Street, Alexandria, Virginia.

P-R-O-C-E-E-D-I-N-G-S

1:28 p.m.

JUDGE ANDERSON: Okay, good -- or good afternoon. It's morning where I am. This is the hearing for IPR2024-01402, between Petitioner Samsung Electronics Company, Limited, Samsung Electronics America, Inc., and NXP Semiconductors, N.V., and Patent Owner being Harbor Island Dynamic, LLC, in honor of U.S. Patent number 7,745,886. As a, sort of, an intro to where we're going to end up here, I do note, and everyone has proceeded on a basis that a motion to amend cancelled Claims 1 and 2 and 4 through 7, so this proceeding will only relate to Claims 3 and 8 through 19. We will have a short break after this hearing, and we will have a hearing on IPR2024-1404. The same parties are involved, with the exception of NXP, which is not a part of the 1404 proceeding.

Couple of administrative or logistical matters. I am Judge Anderson, I am joined by Judge Jung, who is there with you in the hearing room, and Judge Peslak, who is also, like me, appearing remote. So, keep that in mind as you go through particularly your demonstrative exhibits, so that we can follow along, and in doing so, give us the slide number so that we can view them while you're making your arguments. This is a public hearing. Other persons including non-parties may be in attendance on the public line, so keep this in mind when you're making your arguments. Do not get into anything you do not want to have the public hear.

There are no objections to the demonstratives, so all parties are free to use those. Per our order, each party will have 60 minutes to present its argument. This applies to both proceedings. Petitioner has the burden to show unpatentability of the original claims or the remaining claims in the

1 case of the 1402 proceeding. Petitioner will proceed first, followed by
2 Patent Owner. Petitioner may reserve time to rebut Patent Owner's
3 opposition, and Patent Owner may reserve time for a sur-rebuttal. Judge
4 Jung will keep track of the time, which is reflected above his head at 60
5 minutes at this point, and -- but you should be aware of the time as you
6 proceed, and obviously, you're going to have a countdown to look at. So,
7 that should be pretty straightforward given that this is an in-person hearing,
8 for Counsel.

9 If you have an objection to an argument being made, for example, it's
10 beyond the scope of the papers, during your presentation -- save the
11 argument for your own presentation. In other words, I don't want to see
12 interruptions to Counsels' presentation. Okay. At this time, let's have
13 counsel introduce yourself, and anyone who may be present with you. Let's
14 start with Petitioner, Samsung.

15 MR. GOLDBERG: Good afternoon, Your Honor. Joshua Goldberg
16 for Petitioner Samsung, and with me I have my colleague, Biju Chandran. I
17 understand that counsel for NXP may be on the public line, but I'm not sure.

18 JUDGE ANDERSON: I'm going to find that out myself. Thank you.
19 Say your name again, please?

20 MR. GOLDBERG: Joshua Goldberg.

21 JUDGE ANDERSON: Okay, thank you. Patent Owner, please make
22 your introduction.

23 MR. MERCADANTE: Good afternoon, Your Honors. Joseph
24 Mercadante from Fabricant LLP, for the Patent Owner.

25 JUDGE ANDERSON: Thank you. With respect to NXP, is there
26 anyone on the public line for NXP? Okay. Well, they're -- I'm assuming

1 that no one will be participating from NXP, given the fact that they were
2 joined, NXP was joined on the condition that it will not request any
3 alterations to the trial schedule, and that they would adopt a secondary or
4 understudy role to Samsung. So, we will proceed on that basis. Does
5 Samsung have any comment on NXP one way or another?

6 MR. GOLDBERG: What you articulated is our understanding as
7 well, that they will not be actively participating in the hearing.

8 JUDGE ANDERSON: Okay. I just want to make sure that
9 everybody understands they're not here, and we don't want to have some
10 later objection that somehow they were unavailable or could not participate.
11 So, that's really the purpose of my question.

12 MR. GOLDBERG: Yeah, that's our understanding, as well.

13 JUDGE ANDERSON: Thank you, sir. And Patent Owner, are you
14 proceeding under that basis, as well?

15 MR. MERCADANTE: We are, Your Honor.

16 JUDGE ANDERSON: Okay. Very good. With that, Petitioner, you
17 may proceed with your presentation, and please advise us if you want to
18 reserve any time for rebuttal.

19 MR. GOLDBERG: Thank you, Your Honor. I'll reserve 20 minutes.

20 JUDGE ANDERSON: Very good. Proceed.

21 MR. GOLDBERG: Thank you. I'd like to start with Slide 3. As
22 Your Honor pointed out, there were several claims that were cancelled here,
23 so this slide is just showing what the grounds are that are currently at issue,
24 as modified by one of them falling out because of the claim cancellation, and
25 then several claims no longer existing. If we can go to the next slide, Slide
26 4?

1 So, on Slide 4, we can see here on the left what the patent itself admits
2 is a conventional SOI transistor, and then on the right, the allegedly novel
3 transistor. The core alleged invention of the patent is really just that that
4 blue area there, the silicon, is bigger. So, now there's this intervening silicon
5 layer between the source/drain junction and the buried oxide layer. That's
6 really the only thing that's allegedly novel here. The issue is, if we go to
7 Slide 5, having this bigger silicon layer between the source/drain junction
8 and the buried oxide layer is something that was well known in the art. We
9 can see four examples here. On the top left, we've got the Koh reference,
10 and you can see there the blue silicon layer separating the source and the
11 drain from the box layer. On the top right, the Chuang reference. Again, the
12 blue silicon layer is separating the source and the drain from the box layer.
13 The bottom left, Okashita, that's one of the primary references at issues
14 today. Again, we have the big blue silicon layer separating the source and
15 the drain from the box layer. And finally, Yu, another primary reference
16 here on the bottom right, again, showing the thick intervening blue silicon
17 layer between the source and the drain and the buried oxide layer. So, all of
18 this is well known.

19 JUDGE ANDERSON: Counsel?

20 MR. GOLDBERG: Yes.

21 JUDGE ANDERSON: Counsel, are Koh and Chuang of record?

22 MR. GOLDBERG: Yes, they are. Koh is Exhibit 1014, and Chuang
23 is Exhibit 1013. They are all of record, and they were referred to in the
24 petition at I think pages 12, 14, 15, and 51, and then in the Thompson
25 declaration at paragraph 47, 49, 119, and 200.

1 JUDGE ANDERSON: So, why are we looking at them? They're not
2 a basis for any challenge of any claim, right?

3 MR. GOLDBERG: Correct. They're not -- they're just showing the
4 level of skill in the art that this allegedly novel feature is something that is
5 very well known, even beyond in the Okashita and the Yu references, which
6 as we'll discuss, and as we showed in our petition, they actually anticipate
7 Claim 1, which has now been cancelled. So, we're actually talking about
8 some of the other claims at this point, because it seems like HID has actually
9 conceded that this allegedly novel point is well known within the art, and in
10 fact anticipated. If we go --

11 JUDGE ANDERSON: Please proceed.

12 MR. GOLDBERG: If we go to Slide 6, here are the disputed issues
13 that I want to talk about today. I'm going to actually go a little bit out of
14 order. I want to start with the Yu disputed issue, which is really just Yu's
15 disclosure of Claim 1's recitation of each of said plurality of cascaded
16 transistors having a source/drain junction that does not contact said buried
17 oxide layer, thereby forming a source/drain junction capacitance.

18 And if we could go to Slide 28, please? So, looking at Slide 28 here,
19 we've got independent Claim 1 reproduced along with Yu, and it's really just
20 that center limitation that's at issue. We can see if we go to Slide 29, I've
21 just blanked that out to show -- all these other parts of Claim 1, these are not
22 disputed by HID, so we are taking it as true they are in the reference, as was
23 previously recognized by the Board in its institution decision, as well.

24 If we go to Slide 30, here just showing that disputed limitation, we
25 can see the cascaded transitions. That's shown by the green dotted box
26 there, in the area of 65 and 60, and they have source/drain junctions, there's

1 actually several of them shown. The red over there being source, and then
2 the orange-ish colors being drains, and those forming junctions that do not
3 contact said buried oxide layer. We know that because again, we have that
4 blue silicon intervening, so it makes it so that neither the source nor the drain
5 are contacting the box layer. And then at the end here it says, thereby
6 forming a source/drain junction capacitance. And I think that is really
7 maybe where the core dispute is between the parties at this point.

8 If we go to the next slide, Slide 31, there was, I think, a dispute maybe
9 pre-institution about whether there was or was not contact between the
10 source and the drains and then the box layer, but the Board correctly
11 recognized, and we can see this on the left hand side of the slide, that the
12 '886 Patent states that prior art sources and drains typically extend all the
13 way through the device layer, and contact the top surface of the buried oxide
14 layer, which leads to no or almost no capacitive load. The configuration
15 taught in the '886 Patent, in contrast, does not extend all the way through
16 Device Layer 202 to contact the top surface of the buried oxide layer,
17 providing an associated junction capacitance. Accordingly, the source/drain
18 junction capacitance that is thereby formed in Claim 1 appears to be due to
19 the fact that the source/drain junction does not contact said buried oxide
20 layer.

21 So, we agree with all of that analysis that the Board set forth about the
22 '886 Patent. And although pre-institution the Patent Owner had been, I
23 think, taking the position that lack of physical contact wasn't what the claim
24 was about, that really isn't what the claim is talking about. The claim -- they
25 wanted to say that if there's electrical contact, that creates problems for the
26 claim, but the claim doesn't preclude electrical contact, it just precludes

1 physical contact, which is definitely happening in Yu. We can see again on
2 the right-hand side there, the source and the drain in red and in orange, they
3 do not physically contact the box layer. They are separated by that blue
4 silicon layer. And we can see also in the text of Yu, reading on the
5 highlight, that the doped regions 80, 84, 100, 105, and 110, these are the
6 sources and the drains, are formed in the upper part of the wells 42 and 44,
7 and do not extend to the buried oxide layer 32. That is the original silicon
8 layer in which the doped regions are formed is thick enough, so that the
9 doped regions do not completely deplete the wells 42 and 44. So, there is --

10 JUDGE ANDERSON: Counsel, let me back you up a little here. In
11 the decision at institution, we did not specifically construe cascaded
12 transistors. However, we noted that your expert -- I don't know whether he's
13 a doctor or a mister, but Thompson.

14 MR. GOLDBERG: Yes, Dr. Thompson.

15 JUDGE ANDERSON: Okay, thank you. And he referred to the
16 cascaded transistor limitation as meaning ranged in a series of or in
17 succession of stages so that each stage derives from or acts upon the product
18 of the preceding, I assume that's the preceding, transistor. Now, I just want
19 to clarify and make sure we all understand, is that the basis upon which
20 you're proceeding to say that Yu shows cascaded transistors?

21 MR. GOLDBERG: Yes, Your Honor. And I don't think that there's
22 any dispute between the parties about Yu's showing in that regard.

23 JUDGE ANDERSON: Okay, thank you.

24 MR. GOLDBERG: If we go to the next slide, Slide 32? I think that
25 what the core of the dispute on Yu is between the parties is really just about
26 whether the statement in the claim of a source/drain junction requires only

1 one of the source junction or the drain junction, or whether it requires both
2 of them to not form a source/drain junction capacitance. And the reason I
3 think that's really the core dispute is that we have not heard arguments from
4 Patent Owner that -- if you want to go back to Slide 31 for a second. We've
5 not heard arguments that source 105 or drain 110, that the junction there
6 does not form a capacitance. We've only heard this argument about the
7 drain 100. So, it seems like they're of the view that source 105 and drain
8 110, that the source and drain junction capacitance is there, even though they
9 haven't disputed them. So, I think that they concede that they exist. They
10 don't think that's good enough.

11 But if we go back to Slide 32, there's nothing in the claim that requires
12 that there be these capacitances on every source and every drain. We know
13 this because if we look at the claim language itself, on the left-hand side
14 here, we see each of said plurality of cascaded transistors. So, in other
15 words, each of the transistors, every one of the transistors, it has a
16 source/drain junction, and it uses it singular, junction, that does not contact
17 said buried oxide layer, thereby forming a source/drain junction, again
18 singular, capacitance.

19 This is different from in the specification where the specification
20 actually uses plural junctions. We can see on the bottom right-hand side,
21 starting where it says each such, about four lines up. Each such
22 semiconductor junction will have an associated junction capacitance. For
23 example, the source/drain junctions, plural, of transistor 212, so we're
24 talking about a single transistor here, has plural source/drain junctions, and
25 those have corresponding source/drain junction capacitances, plural. So,
26 each transistor in the specification, it has two, at least two source/drain

1 junction capacitances plural. The claim is only requiring one, and because
2 the claim only requires one, it really doesn't matter whether or not Yu
3 discloses one or more than one source/drain junction capacitance per
4 transistor. Either way, it discloses what's needed.

5 JUDGE ANDERSON: So, in your petition, you said that no claim
6 needs construction. How do you square that with now saying that only one
7 of the source or the drain needs to contact -- excuse me, not contact the
8 buried oxide layer?

9 MR. GOLDBERG: So, our view is that this term continues to not
10 need construction, but because Patent Owner introduced an argument that in
11 our view is taking an incorrect read of the claim, we are now coming back as
12 the Federal Circuit has clarified that we may do, and as the Board's Trial
13 Practice Guide has clarified that we may do, and setting forth why they're
14 wrong, why the Patent Owner is wrong, and why under a correct reading of
15 the claim, that the claim does not require the multiple source/drain junctions.
16 Again, we don't think that that's really even claim construction, because it's
17 just the plain wording of the claim itself does not say junctions, plural, it
18 says source/drain junction, singular.

19 JUDGE ANDERSON: Yeah, I can look it up if we need to, but do
20 you have a reference to where the Patent Owner made that argument that
21 you're now saying you're responding to in your reply?

22 MR. GOLDBERG: Yes. I can pull that for you in a moment, if you'd
23 like, Your Honor.

24 JUDGE ANDERSON: Yeah, please.

25 MR. GOLDBERG: So, this will be in page 23 of the Patent Owner
26 response. The Patent Owner is arguing that Yu does not anticipate the

1 claims because the figures and disclosures in Yu clearly show that the
2 source/drain junction of one of the transistors electrically contacts the buried
3 oxide layer, as prohibited by the claims. So, they're just identifying this one,
4 I think they're looking at the drain 100, and saying that by that one creating
5 an issue, that that creates an issue for the overall claim. And our point is,
6 that is irrelevant, because whether or not that one drain junction creates a
7 capacitance or not is not required by the claim. The claim only requires a
8 single junction capacitance be created, and that could be created not just by
9 the number 100, but also by number 105 and number 110.

10 JUDGE ANDERSON: What if the other of the source/drain elements
11 of the transistor did contact the box layer? Does that change any argument
12 that you're making here?

13 MR. GOLDBERG: So, if all of the sources and drains contacted,
14 physically contacted the box layer, then that would change the arguments,
15 but that is not the situation in the reference. That has not been argued by
16 Patent Owner. Just by looking, if we go back to Slide 31, we can see that it
17 is very clear that source 100 and drain 110 are completely separated from the
18 box layer by that blue silicon layer. The only reason I think that we have an
19 argument here at all is that in Yu, you can see, it's a little bit difficult, but on
20 the left part of the blue, it's labeled NW, at 44. So, that's the N-Well, and
21 then on the right, it's a P-Well 42. And Patent Owner's position is that the
22 N-Well allows charge to flow from drain 100 down to the box layer, and
23 therefore there wouldn't be a capacitance for that particular example of a
24 junction. They have not made that argument at all for the source 105 or the
25 drain 110 junctions, because it has the P-Well there. And that's why, from
26 our perspective, even if Patent Owner was right -- and in a moment, I'll get

1 to why they're wrong about the junction 100 and whether it creates
2 capacitance or not, they have not disputed that the junction at 105 and 110,
3 that both of those create capacitance. And that's all that's required by the
4 claim, because the claim only requires one source junction capacitance. It
5 does not require multiple. It does not require every junction to create a
6 source/drain capacitance.

7 JUDGE ANDERSON: Well, ultimately it doesn't make any
8 difference anyway, because none of the source drains contact the box layer,
9 isn't that right?

10 MR. GOLDBERG: That is our view, yes.

11 JUDGE ANDERSON: Okay.

12 MR. GOLDBERG: So, yeah, it should not ultimately matter. And on
13 that note, Your Honor, if we go to Slide 35, we have an explanation here
14 from our expert about why it is that you end up with the capacitance formed
15 on every one of these. And Your Honor is correct, the reason is that you
16 have this is because there is no physical contact between any of these
17 sources and drains and the box layer. Instead, they are always separated by
18 the blue silicon layer.

19 And if we read from the expert on the left-hand side here, he explains
20 that the portion of the n plus region 100, located on the p-well 42,
21 highlighted with the dashed red circle in the figure -- it says below, but it's
22 actually on the right on this slide here, forms a P/N junction. And he cites to
23 another exhibit that P/N junctions are formed by the drain bulk and source
24 bulk interfaces, and a MOSFET, which is what we're dealing with here. A
25 person of ordinary skill in the art would also recognize that during transistor
26 operation, a depletion region forms at the interface between n plus region

1 100 and the p-well 42, and this results in junction capacitance across the
2 region.

3 And how do we know that we have this depletion region forming?
4 That comes from the Yu reference itself at column 5, line 22 to 25. It
5 explains that the first embodiment region comprises n plus and p plus
6 regions, 80, 84, 100, 105, 110, those are the three that we've been talking
7 about, that partially deplete the wells 42 and 44. So, you're having that
8 partial depletion, that's creating the capacitance, that's really all that's
9 needed. And if that were somehow not enough, we even have the Patent
10 Owner themselves, in their sur-reply was recognizing that there may be at
11 least some capacitance. They said there's only meaningful capacitance
12 would be dissipated. But the fact that they're recognizing that there's any
13 capacitance at all is enough for the claim, because the claim does not specify
14 a particular level of capacitance, it just requires some level. And they've
15 even admitted by saying that it's only meaningful capacitance that would be
16 depleted. They've recognized that the reference has the capacitance, even on
17 that drain 100 there.

18 Can we go to Slide 36? Dependent Claim 3, I'm talking about that
19 because Claim 1 was cancelled. The Patent Owner doesn't have any further
20 arguments for you about dependent Claim 3. They, I guess, have conceded
21 that Yu discloses what's in Claim 3. So, unless there's any further question
22 on Yu, I'll move to the Okashita reference.

23 JUDGE JUNG: I have no questions.

24 JUDGE ANDERSON: No, you're good. Go ahead.

25 MR. GOLDBERG: Okay. Can we go to Slide 7, please? So again, I
26 want to remind the Board it is undisputed that Okashita discloses everything

1 in independent Claim 1. There are no special arguments, like we just went
2 through for Yu, about Claim 1. Patent Owner has conceded that Okashita is
3 teaching everything in Claim 1.

4 If we go to Slide 8, we can see Claim 3 here, and we can see where
5 the cascaded transistors in Claim 3 show up in the reference. For example,
6 in Figure 19 we can see them shown in green there. If we go to Slide 9, the
7 argument from Patent Owner about Okashita is that somehow the reference
8 does not disclose or render obvious a plurality of cascaded transistors
9 situated within an isolated island. And to go to Your Honor's question
10 earlier, again, there's no dispute about whether the transistors here are
11 cascaded or not. Really, the only dispute is whether the transistors are
12 situated within an isolated island.

13 And we can see here on the right-hand side, this is actually Claim 3 of
14 the Okashita reference, which conveniently in a lot of ways tracks Claim 3
15 and the '886 Patent. We can see it talking about a plurality of series MOS
16 transistors formed within a first region of said semiconductor layer and
17 connected in series. And then, if we go down a little bit lower, in red again,
18 we can see that there's a first trench insulating layer surrounding said series
19 MOS transistors. So, you have a plurality of transistors that are isolated by
20 this first trench insulating layer that surrounds them.

21 So right there, in our view, this is really enough. I think it's also
22 convenient that, you know, the claim talks about island, but I'll note, the '886
23 Patent itself, when it first introduces islands, and this happens at column 2,
24 lines 67 to column 3, line 2, it actually equates the word island to the word
25 region. So, this region that we're seeing in Claim 3 of Okashita, it is an
26 island, it is the island that's isolated that has a plurality of transistors as is

1 required by Claim 3 of the '886 Patent. And we have testimony about this
2 from our expert, Dr. Thompson, at the top left, explaining that Okashita
3 teaches the additional limitation of Claim 3. For example, Okashita teaches
4 a plurality of MOS transistors connected in series and formed within a first
5 region of the silicon layer, and a trench that surrounds the plurality of MOS
6 transistors connected in series.

7 And if we go to the next slide, Slide 10, we can see here some
8 additional testimony from our expert. Him explaining that in his opinion, a
9 person of ordinary skill in the art reading Okashita would have understood
10 that Trench T1, surrounding the plurality of MOS transistors, 1 and 1 prime,
11 effectively places the MOS transistors within isolated first region in the
12 silicon layer to minimize radiofrequency signal leakage from and to the first
13 region. So again, in our view, this is all the disclosure that's required. Claim
14 3 simply requires transistors that are isolated, and that is exactly what is
15 disclosed by the Okashita reference.

16 JUDGE ANDERSON: Does the fact that the Trench T1 shown in
17 Figure 19 of Okashita actually isolates transistor 1 and 1 prime, and
18 similarly in the other two here with respect to transistors 2 and 2 prime,
19 there's also a trench, T2, that separates the two transistors. Is that at issue
20 here as far as whether or not that precludes a series of connected transistors?

21 MR. GOLDBERG: So, Your Honor, I don't think the way that you
22 just framed it, I don't think that's in dispute. What Patent Owner I believe is
23 arguing is that the fact that there's that extra trench there in the middle, we
24 can call it, they're taking the view that that makes it so that it is no longer an
25 isolated island. And their view would be that now it's actually two islands,
26 and each of the islands has a transistor on it, as opposed to being in -- what

1 they would say the claim requires, I believe, is they would say that's a single
2 island that has to have multiple transistors on it. The claim does not say that.
3 The claim does not require that. All that the claim says, if we go to Slide 8,
4 all that the claim says is that said plurality of cascaded transistors is situated
5 within an isolated island in said device layer. It doesn't say that it has to be a
6 single island, it doesn't say that there's somehow precluded, that there be
7 extra trenches anywhere. The claim doesn't say that, nothing to that effect.

8 Patent Owner has tried to point to Claim 2. If we go to Slide 12.
9 And, they've tried to say well, Claim 2 is about what happens when you have
10 one transistor on an island, and that Claim 3 is somehow different because it
11 talks about plurality. And we don't disagree that Claims 2 and 3 have
12 different scope, but they don't preclude Claim 3 from having an extra trench
13 or something else that separates the multiple transistors. The meaningful
14 difference between Claims 2 and 3 is that while Claim 2 only requires that
15 one transistor be isolated, Claim 3 requires that a plurality of transistors be
16 isolated. And whether that --

17 JUDGE ANDERSON: So, there's not an issue here, in your view, that
18 there are not cascaded transistors here, because the Trench T1 or T2, in
19 respect to the transistors 2 and 2 prime, are separated by a trench? That
20 doesn't preclude them from being cascaded?

21 MR. GOLDBERG: No, I don't think that precludes them from being
22 cascaded, Your Honor, because they are still -- for example, you look at -- if
23 we go to Slide 8, we can see here that it's not like one of the transistors is on
24 earth and one of them is on mars. There's still these other electrical
25 connections within the circuit that are what provide for them being in series,
26 and therefore being cascaded. And that's all articulated in our petition, and

1 none of that has been disputed. I really do think that Patent Owner's
2 fundamental dispute, at least if you go by what their papers say, is they don't
3 like that there's that middle trench there. But again, the issue is that there's
4 nothing in the claims that precludes that middle trench from being there.

5 And if we go for a moment to Slide 11, final point that I want to make
6 on this. Even if we were to take them at their word that somehow there ends
7 up being multiple islands and that the claim has an island that's recited, if we
8 just look at basic Federal Circuit law here, it doesn't matter, because if you
9 have an indefinite article like a or an, that can mean one or more. So, even if
10 there are three multiple different islands, that would still meet the claim
11 limitation. And in our reply, we made that exact argument, that even if the
12 first region in Okashita was two islands, it would still meet Claim 3's
13 limitation of an isolated island in said device layer, in which said plurality of
14 cascaded transistors is situated. Both islands would together be isolated by
15 the Trench T1 surrounding the plurality of MOS transistors 1, 1 prime. The
16 claim does not preclude MOS transistors 1 and 1 prime from also being
17 isolated from each other.

18 And again, that is completely consistent and exactly what Okashita
19 Claim 3 says. If we go again back to Slide 9, we can see in Okashita Claim
20 3, you have the plurality of series MOS transistors, and a first trench
21 insulating layer surrounding said series MOS transistors. Because it doesn't
22 matter whether there's an extra trench or not, they're still surrounded in the
23 way that's required by the claim. And unless there's any questions on that,
24 I'll go to Slide 26, move to the next issue.

25 JUDGE JUNG: I have no questions.

1 MR. GOLDBERG: So, I just want to very briefly talk about the
2 combination of Yu and Okashita. I'm not sure that the core dispute that the
3 Patent Owner has been making is very relevant at this point. The reason
4 being that we were combining Yu and Okashita primarily and firstly to
5 address a potential issue with Claim 1. And in particular, we have the image
6 that we looked at of Okashita, and we could see from the image that the
7 source and the drain did not contact the box layer. But the reference itself
8 did not expressly say that in text. So, to the extent that there was any
9 possible argument or concern about that, we brought in Yu, and we
10 explained with our expert that Yu recognizes that there can be thermal issues
11 when you start to separate the source and the drain from the box layer, and
12 how are these issues addressed? Well, you can put the additional silicon
13 there, and that will address the thermal issues.

14 Now, this again was to address a potential issue with Claim 1 that
15 Patent Owner has not raised, so we don't think it's very relevant at this time.
16 But again, just very briefly, it seems that the main dispute that they are
17 making at this point is whether Yu and Okashita are analogous art or not.

18 And if we go to Slide 17, our view is that there really can't be any
19 meaningful dispute here, because if you look at the field of invention of the
20 '886 Patent on the left side -- and I'll start, before even getting to the
21 highlighted part, just at the higher-level field of the '886 Patent, it says that
22 the present invention is generally in the field of fabrication of semiconductor
23 structures and circuits. I don't think there can be any reasonable dispute that
24 every reference we're talking about today is in that field. Even if we go to
25 the narrower field that's highlighted, more particularly, the invention is in
26 the field of fabrication of semiconductor on insulator structures and circuits.

1 Yu and Okashita are both clearly in that field, as well. If we look at the
2 right-hand side of the slide, we've got the field of Yu, very similar. The
3 invention relates to silicon on insulator devices, and more particularly to a
4 method to form a low voltage triggering silicon-controlled rectifier, SOI
5 device having improved ESD performance. So, same field.

6 If we go to Slide 19, we can see the same thing for the Okashita
7 reference. On the lefthand side again, even the narrow field, the invention of
8 the '886 Patent is in the field of fabrication of semiconductor on insulator
9 structures and circuits. On the right-hand side, from Okashita, according to
10 the present invention, in a semiconductor switch apparatus, the series MOS
11 transistor is formed within a first region of a semiconductor layer on an SOI
12 configuration surrounded by a first trench insulating layer. So, it's again, the
13 same stuff that's being taught in these references. The same field. If there's
14 no questions on that, I'll go to Slide 37.

15 And I want to talk about the last dispute between the parties here. I'll
16 note that Patent Owner made a lot of technical arguments about the
17 combination of Okashita with Burgener. And I don't think that the Board
18 needs to get to pretty much any of those technical arguments that the Patent
19 Owner was making. The reason is, that all those technical arguments, they
20 were premised on an assumption that one of ordinary skill in the art looking
21 at Burgener would always look to Burgener II for its setup, and would never
22 look to other types of SOI setups. But if we look right here on the left-hand
23 side, this is Burgener, and toward the top of the paragraph and the middle of
24 the paragraph it talks about the possibility of doing things with U.S. Patent
25 5,663, 570, the parties have been referring to that as Burgener II. But, it

1 expressly says that other semiconductor on insulator techniques may be used
2 to fabricate a dual band transceiver integrated circuit, as described above.

3 So, the Burgener reference itself recognizes that you can use other
4 SOI technologies. You don't have to use what's in Burgener II. And as soon
5 as the Board recognizes that, all of these arguments that the Patent Owner
6 makes that are premised on Burgener II, about speed and about thickness,
7 and about all that, they all go away, because it doesn't matter. Burgener
8 discloses multiple options. One of those options is other SOI technologies.
9 Okashita is another SOI technology. That is all that's required in order to be
10 making this combination.

11 There is one other point that I want to make about the combination.
12 Patent Owner attacks one of the core reasons that we have for the
13 combination. They say that in Burgener, there are no thermal issues. You
14 don't have to worry about the transistors overheating or getting too hot or
15 anything like that, because in their view, Burgener itself does not expressly
16 recognize that those problems exist. But if we go to Slide 43, it doesn't
17 matter whether Burgener itself recognizes that these thermal issues exist.
18 KSR came out a long time ago. That got rid of the teaching suggestion
19 motivation, and here, we actually do have other references. We're not just
20 relying on our expert to say thermal issues exist. If we look here at the
21 bottom left, the buried oxide reduces thermal conductivity in the substrate,
22 compared to bulk, resulting in locally increased temperature. This can
23 impact circuit performance and possibly reliability. So, heat is an issue.

24 If we go to the top right on this slide, the buried silicon dioxide layer
25 and SOI circuit has a very low thermal conductivity, which results in a large
26 thermal resistance between the device and the chip packing. This is a major

1 problem for transistors. Bottom right, self-heating and SOI represents
2 another design constraint. If we go to the top left, temperature rise can be
3 significant even at relatively low power dissipations. So, heat is clearly an
4 issue in transistors. If we go to Slide 42, we can see Burgener here, and we
5 just heard about how even under low power, heat can be an issue. Well,
6 Burgener talks about high power switching circuits. We can see that on the
7 left-hand side of the slide, so it's even more of an issue.

8 And then Burgener, on the right-hand side, it talks about being
9 desirable. Desirable to more closely control a device impedance, and to
10 dissipate heat and specific resistive series coupling elements, rather than
11 within the FETs themselves. So, they don't want to be dissipating heat in the
12 FETs, that's the transistors. It's got to be dissipated somewhere else. So, this
13 heat dissipation is definitely an issue, as recognized by our expert, based on
14 the prior art that we just talked about, shown in Slide 43. Even Burgener
15 itself seems to recognize this. Mr. Berg, Patent Owner's expert, he also
16 recognized that it's not desirable to be dissipating heat into the FETs, so you
17 need to be doing the opposite. You've got to be getting rid of heat. So, that
18 is the reason to look to Okashita. That is the reason for the combination,
19 beyond the fact that Burgener itself just recognizes. It doesn't go into detail
20 on the SOI setups, and that any other SOI setup can be used, and Okashita is
21 an example of that. And unless there's any questions, I'll stop there.

22 JUDGE JUNG: I have no questions.

23 JUDGE ANDERSON: Yeah, I know some of your exhibits, and I
24 don't remember which slide it was, I can find it, but the exhibits that are not
25 relied on for any effort to cancel the claims that are in service, the exhibits
26 that are talking about heat dissipation, are all of those, -- I see some of them

1 are referred to in the supplemental Thompson declaration, are all of them
2 referenced in terms of supporting the opinions expressed there?

3 MR. GOLDBERG: They're all referenced either in the supplemental
4 Thompson declaration or in the original Thompson declaration.

5 JUDGE ANDERSON: Okay. Thank you. I have nothing further,
6 then.

7 MR. GOLDBERG: Thank you, Your Honors.

8 JUDGE JUNG: You have 19 minutes left for rebuttal.

9 MR. MERCADANTE: Your Honors, I'd like to reserve 15 minutes,
10 please.

11 JUDGE ANDERSON: Proceed, Counsel.

12 MR. MERCADANTE: Thank you, Your Honors. I'm going to take
13 the arguments in the same order that opposing counsel took them in. But
14 first, I'd just like to briefly go over the problem and the solution in the '886
15 Patent. The problem as identified in the '886 Patent, is that when you're
16 converting from using bulk silicon to SOI, silicon on insulator, it requires a
17 redesign of all your circuits. It says right here in the background, SOI was a
18 big topic at the time this patent application was filed. It had additional
19 insulation properties. But unfortunately, circuits designed for fabrication in
20 bulk silicon wafer must be redesigned for fabrication in a conventional SOI
21 wafer.

22 And the '886 Patent talks about what happens when you use SOI,
23 which is that you have a very low capacitance, as compared to the old silicon
24 technology which had a very high capacitance. So, one of the innovations in
25 this is to -- in the '886 Patent, is to basically imitate old bulk silicon by
26 creating additional capacitance. And that capacitance is created by having

1 the source/drain junctions not go all the way down to the insulator. So, it's a
2 novel and very interesting sort of way to trick your circuit simulations so
3 that you can use your old circuit designs that are already sitting in some
4 library. You can now build them in SOI, and they work exactly the same as
5 they would have worked in the old silicon, but now you have the insulation
6 benefits of SOI.

7 The innovation in this patent isn't just taking those source/drain
8 junctions and moving them away from the box. It's actually a way to trick
9 the circuits into acting like circuits that were designed for the old bulk
10 silicon. And that additional capacitance, in a way, is something that was not
11 being considered at the time, because obviously very few people want to add
12 capacitance to their circuits. It slows things down. It can create some
13 undesirable capacities. It can have a whole host of effects. People are
14 generally trying to not add capacitance to their transistors, unless there's a
15 design reason to do so. So that, I think, informs all of the arguments that we
16 have here today, but more importantly, I think is a more accurate and
17 complete summary of the patent. And apologies, the HDMI cable is playing
18 tricks on me. I'm going to move my papers and see if it helps.

19 So, with respect to Ground 4, I believe it is, the Yu anticipation
20 ground that we spoke about previously, there really is one and only one issue
21 there, which is -- I'm turning to Slide 17 of my presentation. There it is.
22 Slide 17 of my presentation. This is Figure 9 from Yu. What Yu discloses
23 is something very different from what's taught by the '886 Patent. There is
24 an insulator layer, but it's not all the same material. On the left, you can see
25 it right under that red arrow, there's an n-well. And on the right, there's a p-
26 well. And that is because Yu is a very particular kind of circuit that's

1 designed for what's called a silicon-controlled rectifier. And Yu discusses
2 that that rectifier is used for electrostatic discharge. So, it needs to be
3 designed, for some reason, because of that purpose, in this way. The experts
4 don't get into it. This is essentially an unbalanced transistor. Transistor 65
5 has no capacitance on that n+ well, where the red lines are, because all the
6 charge dissipates through the n-well into the buried oxide layer. There's no
7 capacitance there. It's an unbalanced transistor. And why that is, is not in
8 the record. Maybe it triggers faster because you're discharging a high
9 voltage, maybe it handles the current better. It's not in the record. But for
10 whatever reason, the design considerations behind Yu led the engineers to
11 design it this way. That's very different from what the '886 Patent is talking
12 about. Just because it has a buried oxide layer –

13 JUDGE ANDERSON: Stop right there, please. The fact is, that there
14 is that well, I can't remember, I think it's an n-well at 44, that does separate
15 the source and the drain from the box. So, what's your argument there? Is it
16 in fact that there's electrical contact that's being made?

17 MR. MERCADANTE: Yes, Your Honor.

18 JUDGE ANDERSON: Because if it is -- well, that's not what the
19 claim says. Tell me why it requires electrical contact.

20 MR. MERCADANTE: Claim 1 requires each of said plurality of
21 cascaded transistors having a source/drain junction that does not contact said
22 buried oxide layer, thereby forming a source/drain junction capacitance.
23 The capacitance is a requirement of the claim. Even though there's no
24 mechanical contact, there's no physical contact on the source of that
25 transistor that we saw in Yu and the buried oxide layer, there's still no
26 capacitance there, which is an express requirement of the claim. And they

1 don't claim otherwise. Patent Owner, unlike the next patent that we're going
2 to talk about this afternoon, Petitioner doesn't say that's a functional
3 limitation that can be ignored. They don't have a claim construction for this
4 capacitance term. The claim expressly requires a capacitance there.

5 And we pointed this out. This happened, this figure -- and I'm going
6 to actually put up the Thompson declaration, the original one. This is
7 Exhibit 1002, starting just about paragraph 201. This was his original figure.
8 He took the n-well and the p-well and he colored it all blue. I personally
9 think that was an attempt to deceive us, that those weren't actually there.
10 But it's either that, or it's sloppy. And what he says two paragraph later, in
11 paragraph 202 is, in my opinion, a POSITA would have known that if the
12 doped region 105 that forms the source and the doped regions 100 and 110
13 that form the drain, of Yu's first and second transistors do not extend to the
14 buried oxide layer, and the source drain junctions of these transistors do not
15 contact the buried oxide layer. And then, for the capacitance, he just says
16 because they don't touch, there's no capacitance. He doesn't take into
17 account the n-well at all.

18 And so, we pointed this out. We pointed this out in our Patent Owner
19 response. And that's when they came up with this claim construction that
20 say well, it actually doesn't matter that there's no capacitance on that n-well,
21 because you only need capacitance on one part of the transistor, right?
22 Either the source junction or the drain junction. That's good enough for the
23 claim. Well, that's wrong, because if we look at the '886 Patent in its
24 entirety, including the goals of the invention, there would be no way to reuse
25 old circuit designs designed for bulk silicon if you had this unbalanced
26 transistor. So, the only plausible reading of the claim, to the extent this

1 belated claim construction is considered at all, is that the source and the
2 drain have to have capacitance.

3 And then they say well, even if our claim construction isn't
4 considered, or even if our claim construction is wrong, there's actually a tiny
5 little bit of capacitance sitting there inside that dotted circle. That's the
6 supplemental Thompson declaration. So, he's changed his position again,
7 and now he says well, there's actually, in certain operating conditions that he
8 doesn't explain, there's actually a tiny little bit of capacitance there. Well,
9 there's capacitance between everything. There's capacitance between me
10 and Judge Jung sitting 15 feet away from me. If you hook up a wire to us,
11 you would be able to measure capacitance between there. That's not
12 meaningful for the purposes of the design and operation of the circuit. You
13 could point to any two places on an integrated circuit and say there's
14 capacitance between them. That's not what these claims are about. That's
15 not what the '886 Patent is about.

16 So, first, we think that this argument is an improper reaction to the
17 incredible sloppy thing that we see in their petition, which is just pointing to
18 the entire blue thing and saying there's capacitance there, even though there's
19 not. And then, we see number two --

20 JUDGE ANDERSON: Wait a minute, please. Isn't the whole concept
21 of the '886 Patent that there is a space between the source and the drain and
22 the box layer, right?

23 MR. MERCADANTE: That's correct, Your Honor.

24 JUDGE ANDERSON: And that that creates capacitance.

1 MR. MERCADANTE: That can create capacitance, yes. Not in Yu,
2 because the intervening layer is doped the same way as the source. But in
3 certain instances, yes, that creates capacitance.

4 JUDGE ANDERSON: Okay. So, it seems like the argument kind of
5 goes in circles, in my mind anyway, because here we're showing in Yu that
6 there is a space. We acknowledge that a space is what's needed, and that -- I
7 mean, it's there. There is a space. And sorry, I'm having a hard time feeling
8 a lot of sympathy for this argument. So, and I'm also concerned that there's
9 no construction of this term that says it's electrical contact as opposed to
10 physical contract. So, you need to address that for me.

11 MR. MERCADANTE: Okay. I'll take those two points in reverse
12 order. Turning back to Slide 6, which is just the claims. Claim 1 says
13 there's no contact between the source/drain junctions and the buried oxide
14 layer. Obviously, there's a dispute about whether that's one or both
15 junctions, but there's no contact. Thereby forming a source/drain junction
16 capacitance. So, in Yu, even though there's no contact, the capacitance is
17 not formed. So, the claim is not met merely by the lack of contact. You need
18 to have a lack of contact and also a capacitance. And in Yu, as explained by
19 our expert, I'm back to Slide 17, which is where I started, in Yu, the red
20 lines, as stated by Mr. Berg, dissipate the charge. There's no capacitance on
21 that element, which is a requirement of the claim, because the charge --
22 there's an n-plus dope, and it's connected to an n-well, and the charge gets
23 dissipated. You can't store charge there like you do on the other transistor.
24 Counsel said we don't dispute that a transistor 60, the two n-plus wells,
25 there's capacitance there. That's correct, we don't dispute that, because those
26 are n-plus doped, and they're sitting in a p-well. So, charge sits there, and

1 you have capacitance. The left side, the source of transistor 65, does not
2 have the capacitance required by the claim. It does not.

3 JUDGE ANDERSON: Okay. The capacitance is required only
4 because there's no electrical contact between the source/drain and the box
5 layer, right?

6 MR. MERCADANTE: The capacitance is formed by a lack of
7 contact between the junctions and the box layer.

8 JUDGE ANDERSON: So, why is it that this is an argument, and it's
9 not some construction of the term we're concerned with here, which is
10 contact between the source/drain junction and the oxide layer?

11 MR. MERCADANTE: We don't think there's a --

12 JUDGE ANDERSON: Doesn't that require a construction?

13 MR. MERCADANTE: We don't think there's a dispute about the
14 scope of the claim. Now, there's a dispute about the one junction versus two
15 junction issues, but as far as the contact, we don't really think there's a
16 dispute about the scope of the claim. You can have source/drain junctions
17 that don't contact the buried oxide layer and form a capacitance. And that's
18 within the scope of the claim. And you can have source/drain junctions that
19 don't contact the buried oxide layer but for some reason don't form a
20 capacitance, and that doesn't meet the claim, which requires a source/drain
21 junction capacitance. And that's what their expert is trying to clean up in his
22 supplemental declaration, which we've highlighted on Slide 19, by saying
23 actually, there is a tiny little bit of capacitance there, I was wrong before.
24 It's not a claim construction issue, because we seem to all agree that a mere
25 lack of contact is not enough when the claim expressly requires a lack of
26 physical contact and a source/drain junction capacitance, thereby forming a

1 source/drain junction capacitance. If the source/drain junction capacitance
2 isn't formed, you haven't met the claim.

3 JUDGE ANDERSON: I think I understand your position.

4 JUDGE JUNG: Mr. Mercadante, just to clarify, are you saying that in
5 the reference, there is no capacitance being formed at all? Like there's zero,
6 no capacitance?

7 MR. MERCADANTE: We are saying that Dr. Thompson's original
8 position, that there's a capacitance formed because of the existence of that
9 blue intervening layer, is incorrect. We are saying that his supplemental
10 opinion, which is that there's a tiny little bit of capacitance in that dotted
11 circle, is incomplete and unsupported. Because he says, under certain
12 operating conditions, there may be a small capacitance in that red circle, but
13 he doesn't explain what those operating conditions are, he doesn't explain
14 how much capacitance there would be, and more importantly, whatever tiny
15 little bit of capacitance may be sitting on the drain of that transistor 65
16 would create an unbalanced transistor due to the likely larger amount of
17 capacitance that's on the other side of that transistor, which again would
18 frustrate the original purpose of the '886 Patent, which is using your old
19 circuit designs in SOI.

20 JUDGE JUNG: But do you still believe -- there would still be some
21 innate capacitance, because there's still some dielectric effect between these
22 two layers?

23 MR. MERCADANTE: There may be, there may not be. It's not in
24 the record. All we have is the supplemental expert declaration to go on. We
25 don't think it's material for the purposes of the prior art and the '886 Patent,
26 but I cannot tell you for certain that there is absolutely no miniscule amount

1 of capacitance sitting there, just like I cannot tell you that there's no
2 capacitance between you and I right now. If you want to find a tiny little bit
3 of capacitance anywhere, you can do so, but there must be a meaningful
4 amount of capacitance when viewed through the lens of the '886 patent.

5 JUDGE JUNG: So, you can kind of see our problem with this
6 argument, is that there might be a little bit of capacitance there, right?

7 MR. MERCADANTE: To the extent Dr. Thompson's supplemental
8 opinion is considered, there very well may be, although we still think that it's
9 incomplete. But certainly -- I don't think this is a problem because I think
10 that when viewed through the lens of the '886 Patent, this is not what the
11 '886 Patent is talking about. Yu is an extremely narrow sort of one-off
12 design for this silicon control rectifier.

13 JUDGE JUNG: Okay. One last thing, do you make any assertion or
14 argument that the Thompson supplemental declaration on this point was
15 improper, procedurally improper?

16 MR. MERCADANTE: We did not move to strike it, but we think it
17 goes to the weight, Your Honor. We certainly think that the way that the
18 position between the petition and the reply has sort of shifted and there's
19 been a lot of moving and parroting here, the belated claim construction after
20 the petition said that no construction was necessary, we certainly think that
21 goes to the weight of Dr. Thompson's opinion and also his credibility.

22 JUDGE JUNG: Okay, thank you.

23 MR. MERCADANTE: I'm now going to move to Ground 2, which is
24 the Okashita argument for Claim 3. I'd like to again start by looking at the
25 petition. So, we saw Counsel put up Claim 3 of Okashita and try to walk
26 through the isolation. The petition itself seems to us to recognize that Claim

1 3 requires all of the cascaded transistors to be in the same isolated island.
2 That's why it says isolated island. And they actually say a POSITA would
3 have recognized that modifying Okashita would have certain benefits. And
4 they say it was well known in the art to situation multiple transistors in the
5 same region. To us, that's a motivation to modify Okashita. That's an
6 admission that in Okashita the cascaded transistors are sitting on separate
7 islands. And they say, well, it would have been obvious to modify them to
8 put them on the same island, as in Claim 3.

9 Claim 3, I'm going to bring up the '886 Patent, Claims 2 and 3,
10 because that's central to the analysis here. Claim 2 requires at least one of
11 said plurality of cascaded transistors is situated within an isolated island, and
12 then Claim 3 requires all of the cascaded transistors to be situated within an
13 isolated island, singular. If you're putting them on separate islands, that's
14 Claim 2. Claim 3 says you put them all on the same island. And if we look
15 at what they say about Okashita, they recognize in their petition, as shown
16 here, that each of these cascaded transistors, on Slide 10 for the judges, are
17 on their own isolated island.

18 Again, this, we think reeks as a belated claim construction. They kind
19 of used Okashita in their petition for both ways. They used it for Claim 2,
20 and they said well, yeah, they're each on their own isolated island, and then
21 they said well, for Claim 3, they're both on the same isolated island. And
22 you can't really have it both ways. So, looking at Claim 3, we think that
23 their argument -- in order to be successful with Okashita, you must modify
24 Okashita to get rid of that intermediate trench. In islands, in semiconductor
25 design, an isolated island is the same as an isolated island in geography,
26 right? If I'm standing on Maui and someone else is standing on the big

1 island, in Hawaii, we're not on the same isolated island. We're on different
2 isolated islands. That's Claim 2. And there's no motivation, as stated in
3 their position, to modify Okashita to put these transistors on the same island,
4 because Okashita directly says in plain English that you are trying to prevent
5 radio leakage between the two transistors. So that line, that trench in
6 between the two transistors is incredibly important. So, there's no way that
7 the person of ordinary skill in the art reading Okashita would have been
8 modified to get rid of that line, that trench in between the two, because
9 Okashita specifically says that that's important. The only motivation they
10 have in their petition to modify Okashita to reach Claim 3, is impermissible
11 hindsight. That's all they have. Okashita says, you want to isolate each
12 individual transistor, not to put them all on the same island.

13 JUDGE ANDERSON: So, you're not -- I asked Petitioner's Counsel
14 about the cascaded transistors. You're not disputing that Yu and/or
15 Okashita, well, I guess we're looking at Okashita on the cascaded transistors.
16 We're not arguing about that for the purposes of what we're doing.

17 MR. MERCADANTE: We are not, Your Honor. Those positions
18 were raised at institution. For the remainder of this proceeding, post
19 institution, we have not taken any position regarding the scope of the
20 cascaded transistors or the disclosure of the cascaded transistors in any of
21 the prior art. We have not disputed that.

22 JUDGE ANDERSON: Okay. So, as far as isolating the -- let me get
23 the claim language right. Isolated island. The plurality of cascaded
24 transistors is situated within an isolated island in the device layer. So, your
25 argument is that because there's the trench -- I'm looking at Figure 19 right
26 now, of Okashita. Because there's a Trench T1 that includes a middle

1 portion there that goes between the two transistors, 1 and 1 prime, that that is
2 not an isolated island?

3 MR. MERCADANTE: That's correct, Your Honor. That's two
4 isolated islands.

5 JUDGE ANDERSON: Okay. So, is an isolated island electrically
6 connected between two transistors? Let me rephrase that. If the two
7 transistors, 1 and 1 prime, are electrically connected, are they isolated for
8 purposes of this claim?

9 MR. MERCADANTE: Yes.

10 JUDGE ANDERSON: You think they are?

11 MR. MERCADANTE: We think they are, Your Honor, yes.

12 JUDGE ANDERSON: And why would that be?

13 MR. MERCADANTE: Well, isolation talks about -- when we talk
14 about isolation in silicon, we talk about preventing the propagation of
15 signals from places where they should be to places where they shouldn't be.
16 If you're going to connect a wire between the two, then that wire is going to
17 carry the proper signal from point A to point B, where it's connected. But
18 spontaneous emissions and switching noise and things like that would still
19 be blocked by each of the isolated islands.

20 JUDGE ANDERSON: Yeah, it's about interference, right?

21 MR. MERCADANTE: Correct.

22 JUDGE ANDERSON: So --

23 MR. MERCADANTE: I mean, if you were to read an isolated island
24 to mean that there could be no electrical connections outside of it, then you'd
25 have a pretty bad chip, because you couldn't really use anything in an
26 isolated island for anything. There needs to be electrical connections within

1 and between the isolated islands, but those are designed for the signals that
2 you want, where the isolated islands are designed to block the signals that
3 you don't want, such as switching noise, and if these things are close to
4 antennas, there may be RF signals coming into the chip from elsewhere that
5 you don't want to interfere with the individual transistors. But I don't think
6 that a wire connecting two isolated regions would necessarily prevent those
7 regions from being isolated.

8 JUDGE ANDERSON: Yeah, arguably it's a connection, right?

9 MR. MERCADANTE: It is a connection, but they're still isolated
10 islands, regardless of whether there's a bridge between them, Your Honor.
11 Just as in geography.

12 JUDGE ANDERSON: And yet you argue in Yu that Figures 9 and 10
13 allow electrical connection, and therefore there is contact, and here you're
14 saying even though here is an electrical connection, these are still isolated
15 islands, right?

16 MR. MERCADANTE: Yes. The argument in Yu is about the
17 connection between -- the vertical connection between the different layers in
18 the silicon. There's wires connected between the transistors in Yu. It doesn't
19 stop there from being capacitance, even when those transistors are on. It's a
20 different situation. A wire connecting two transistors together is different
21 from the situation we're talking about in Yu with the capacitance.

22 JUDGE ANDERSON: Fair enough.

23 JUDGE JUNG: Mr. Mercadante, before you go on, all your
24 arguments for Claim 3, are they predicated on an isolated island being just a
25 single isolated island?

26 MR. MERCADANTE: Yes.

1 JUDGE JUNG: Can you address Mr. Goldberg's point that an
2 isolated island can also mean more than one island?

3 MR. MERCADANTE: In this instance, we don't think that's a proper
4 reading of the claim, because -- and I'll bring up Okashita again, because if
5 an isolated island could be read as one or more isolated islands -- again, we
6 think this claim construction is belated and improper, but to the extent that
7 the panel entertains it, we think that reading an isolated island to be multiple
8 isolated islands would make Claims 2 and 3 coextensive.

9 JUDGE JUNG: Why is that, exactly?

10 MR. MERCADANTE: Because if you had a transistor on an isolated
11 island, if you had each transistor on its own isolated island, that would be
12 within the scope of Claim 2, and also Claim 3.

13 JUDGE JUNG: What if the plurality of cascaded transistors is
14 situated within a plurality of isolated islands? Wouldn't that fall within
15 Claim 3, but not Claim 2?

16 MR. MERCADANTE: No, because Claim 2 says at least one.

17 JUDGE JUNG: Okay. All right. So, if we go your way, in the final
18 written decision we're going to have to say something about why an isolated
19 island is singular. So, our analysis would be that we read Claim 3 to require
20 a singular isolated island because, what's the because?

21 MR. MERCADANTE: Because, A, first, it's singular in the claim,
22 and, B, the very nature of the isolation requires isolation. Nothing else. So,
23 it seems to me that reading this to mean one or more isolated islands is
24 incongruent with the claim language itself.

25 JUDGE JUNG: Okay.

1 MR. MERCADANTE: If there's no more questions about Grounds 2
2 or 4, I'm going to spend a little bit of time on Ground 3, which is Okashita in
3 combination with Yu, and then the rest of the time on the wireless claims. I
4 understood Counsel's presentation on Claim 3 to basically mean that it
5 doesn't matter. That they were using Yu to pull in some description about
6 the capacitance, and therefore it's not really relevant, but this is still an active
7 ground for Claim 3. And so, I think it needs to be addressed. I know
8 obviously, Ground 4 is Yu's anticipation. I'm not going to repeat those
9 arguments for this. We've already talked about the technical aspect of
10 Okashita with respect to Claim 3, but I do want to talk about the motivation
11 to combine Okashita and Yu, because unless it's going to be withdrawn, this
12 is still an active part of this proceeding.

13 We think that -- well, first of all, Counsel said our entire basis for this
14 ground is saying that these, Okashita and Yu are not analogous to the '886
15 Patent. That's incorrect. Our argument is that there's no motivation to
16 combine Okashita and Yu, and a sub-argument of that is that they're not
17 analogous art. We've talked about Yu and this unbalanced transistor and this
18 silicon-controlled rectifier. I don't want to belabor that point, but the main
19 reason that there's no motivation to combine Okashita and Yu is that Yu
20 already discloses a transistor. Yu discloses a transistor that makes a silicon-
21 controlled rectifier. And Okashita already discloses cascaded transistors that
22 are isolated from one another, for the purpose of Okashita, which is a
23 wireless circuit. And other than impermissible hindsight, there's no real
24 reason that the person of ordinary skill in the art would have looked from
25 Okashita to Yu or vice versa. They're just kind of both throwing them both
26 up in the air and saying yeah, you could take these teachings and combine

1 them, because our expert says that there would be less heat, or something
2 like that.

3 But it's really not the case, because these are transistors that are built
4 and designed for very different purposes. They're so different in fact, that
5 they're not analogous. Now, this is not a core part of the argument like it
6 was yesterday, with the silicon trenches. It really doesn't matter whether
7 they're analogous or not to the '886 Patent, because Okashita and Yu are so
8 different from one another. And that's why there's no motivation to combine
9 them. And --

10 JUDGE JUNG: Okay, just to be clear, they're different, but not so
11 different they're not analogous art? But they're so different --

12 MR. MERCADANTE: No, we still maintain that they're not
13 analogous to the '886 Patent, but it's not a core -- rather than spend time on
14 the analogous argument, our argument is broader than that. Which is, the
15 proffered reasons and motivations to combine Okashita and Yu are overly
16 generic and based on hindsight, and improper. Due to the difference
17 between the circuits in Okashita in Yu, putting aside the '886 patent. If we
18 use the '886 Patent as a guide, through impermissible hindsight, we can get
19 to Claim 3 using Okashita and Yu, but the combination as guided by that
20 hindsight is improper.

21 And then lastly, Ground 5, which is where we pull in, where
22 Petitioner pulls in Burgener and combines it with Okashita for the wireless
23 claims. The wireless claims, which are the two independent claims, I
24 believe it's 9 and 16, and their dependence, take the circuit from Claim 1, the
25 cascaded transistor with the isolation, and then place them in certain wireless

1 configurations between antennas and switches or power amplifiers. Be that
2 as it may, I'm going to colloquially refer to them as the wireless claims.

3 And the main argument here, which I think was elucidated very nicely
4 by Opposing Counsel, is whether the person of ordinary skill in the art who
5 was looking at the wireless circuits in Burgener would turn to the transistors
6 in Okashita to build those circuits. Burgener is an antenna switch. It
7 discloses transistors, but it doesn't tell you how to build them, and according
8 to Samsung, you would look to the SOI technology in Okashita to build
9 those transistors in Burgener and arrive at the wireless claims in the '886
10 Patent.

11 At the institution phase, we made a different color of this same
12 argument, which was that -- at institution, we had stated that Burgener and
13 Okashita teach away from one another, because Burgener explicitly points
14 you to this other patent that provides details regarding design and fabrication
15 of an RF switch. And that patent, this '502 Patent that's highlighted here on
16 Slide 23, is what we've colloquially referred to as Burgener II. It's the same
17 inventor. Now, post-institution, we've not made the teaching away
18 argument. We don't claim that this is teaching away, but we still claim that
19 the existence of Burgener II, and the explicit recitation of Burgener II in
20 Burgener as giving you information as to how to build the transistors does
21 not provide a motivation to the person of ordinary skill in the art to instead
22 ignore Burgener II and look to Okashita, as Samsung claims that you're
23 supposed to do. That's at core the argument, that there's no motivation to
24 combine Burgener and Okashita, because Burgener tells you, if you want to
25 build these transistors, go look at my other patent, Burgener II.

1 And now, if we look at Burgener II, it actually teaches this silicon on
2 sapphire technology. SOS is what some of us referred to it in the paper as.
3 Burgener II uses this UTSI, it's this incredibly nuanced type of silicon that
4 uses sapphire as an insulator layer. And one of the reasons it talks about
5 why you would use sapphire as your insulating layer is because it reduces
6 parasitic capacitance, and eliminates the needs for traditional transistor
7 isolation wells. That's what Burgener II tells you. Burgener I says, go look
8 at Burgener II. Burgener II says, we use silicon on sapphire, it's great.
9 There's no capacitance, you don't need isolation wells. So, why would a
10 person of ordinary skill in the art looking at this say I'm going to ignore all
11 this stuff and I'm just going to go look at Okashita to build my transistors,
12 using a different silicon insulator technology that has capacitance, except for
13 hindsight. That's the only reason that the person of ordinary skill in the art
14 would ignore all of the stuff that Burgener and Burgener II teach you and
15 say actually, we're going to look at this total other patent over here,
16 Burgener, that uses a different isolation technology, that uses isolation wells,
17 that doesn't use silicon on sapphire, that has a large amount of capacitance,
18 which the '886 Patent teaches us what not really something people were
19 doing at the time, when you could just look at the patent that is cited directly
20 in Burgener, and it gives you the technology that he wants you to use to
21 build these circuits. That's the motivation right there. The motivation in
22 Burgener is to use what's in Burgener II, not to go look at Okashita.

23 JUDGE ANDERSON: Yeah, but Burgener itself, exhibit, the one that
24 is relied on for the challenge, it says that, in reference to Burgener II, I think,
25 that other semiconductors -- I'm looking at paragraph 105 of Burgener.
26 Other semiconductor on insulator techniques may be used to fabricate a dual

1 band transceiver integrated circuit as described above. So, it specifically
2 references the SOA technology.

3 MR. MERCADANTE: It specifically references other types -- oh, I'm
4 sorry, Your Honor. I didn't mean to interrupt. Please finish your question.

5 JUDGE ANDERSON: Why wouldn't a person of ordinary skill in the
6 art use that to connect Okashita and Yu for that matter? Go ahead.

7 MR. MERCADANTE: It does state that there may be instances
8 where you would want to use other SOI technologies. It does not explain
9 what those instances are. It does not explain under what conditions you
10 would want to ignore the discussion in Burgener II and go look at other
11 technologies. And even if you were to use other SOI technologies, there's
12 no evidence in record, aside from impermissible hindsight, as to why you
13 would go look at Okashita, because Okashita has all this capacitance, has all
14 these thick layers. And everything in Burgener and Burgener II is about
15 getting rid of these things. So, yes, there is the statement in Burgener, which
16 we don't dispute, that says in certain other instances and for certain power
17 levels you might want to go look at other SOI technologies, but that doesn't
18 specifically lead you to Okashita, for all the technical reasons that we've
19 discussed.

20 We talked about heat earlier. One of the things that Dr. Thompson
21 relies on a lot is that well, if you didn't use Burgener II, and instead you used
22 Okashita, you know, you would get rid of more heat. Well, Burgener
23 teaches that -- and here is the citation, Your Honor, on Slide 26, that I was
24 looking for earlier that you mentioned in Burgener. It says, other
25 semiconductor on insulator techniques may be used to fabricate a dual band
26 transceiver integrated circuit, as described above, for at least some frequency

1 bands and power levels. That's it. One sentence that says you might want to
2 use other technologies. It doesn't specifically lead you to anything in
3 Okashita. And I was about to talk about the heat that opposing counsel
4 brought up, that's one of their main arguments for the motivation to
5 combine, is if you used Okashita to build the transistors in Burgener, you
6 know, there would be better heat dissipation. Well, Burgener talks about
7 dissipating heat already. And he says that, Burgener talks about dissipating
8 heat in the resistive series couplings in the power amp. He wants to
9 dissipate the heat in the resistors rather than dissipate the heat in the
10 transistors. He specifically says at paragraph 44, heat should be dissipated
11 in specific resistive series coupling elements, rather than within the FETs
12 themselves.

13 So, we think that the primary reason that Dr. Thompson says you
14 would look to Okashita from Burgener, the dissipation of heat, is already
15 addressed in Burgener. And he says he doesn't want to dissipate the heat in
16 the FETs, he wants to do it in the resistors before the power gets to the
17 FETs. There's also some discussion of signal leakage by Dr. Thompson, that
18 well, if you used Okashita and the trenches, there would be less leakage of
19 radio signals, because Burgener is a wireless system, and we think that's
20 also, A, impermissible hindsight, and, B, incongruent with the teachings of
21 Burgener II, which says that if you used the silicon on sapphire, you don't
22 need trenches at all because it's fully insulating. I'm low on time. I've hit all
23 the points that I wanted to hit. Unless Your Honors have any questions for
24 me, I'll reserve the rest of my time.

25 JUDGE JUNG: I have no questions.

26 JUDGE ANDERSON: That's fine. You've got your 15 minutes.

1 MR. MERCADANTE: Thank you.

2 JUDGE ANDERSON: 18 minutes.

3 MR. GOLDBERG: Before I get started, Your Honors, I just wanted
4 to note that counsel for NXP, through one of my colleagues here, noted that
5 they are and have been on the public line, but the system would not let them
6 unmute to announce themselves when you were asking if they were here
7 before. So, they just wanted to have me confirm that they did join remotely,
8 and that they are in an understudy role, so are not otherwise participating.

9 JUDGE ANDERSON: I appreciate that very much. Thank you,
10 Counsel.

11 MR. GOLDBERG: So, I'll try to be brief here. I want to start with
12 the Yu reference. The testimony in the supplemental Thompson declaration
13 that's been discussed, it wasn't there because he screwed up in his original
14 declaration. It was there because Patent Owner's expert, Mr. Berg, made
15 some points that were wrong, and Dr. Thompson was addressing those
16 points, explaining why they were invalid, and explaining that the gap, the
17 lack of contact between the source and drain and the box layer, does indeed
18 create capacitance, contrary to what Mr. Berg was arguing. And this
19 happens on all of the sources and drains, including the 100, that's at issue
20 between the parties. When given the opportunity, HID's counsel did not
21 dispute that there is at least some capacitance between all of the sources and
22 drains and the box layer. And that ends the story. The claim does not require
23 a specific level of capacitance. I'm not aware of any claim construction
24 doctrine that says you get to just input particular levels, because that's,
25 according to Patent Owner, generally something that the patent relates to.
26 It's not in the claim, so it's not required.

1 Alternatively, as we discussed earlier, the Board could simply apply
2 the plain language, singular, and find that, again, Patent Owner did not
3 dispute that the drain and source 105 and 110, that there's capacitance there.
4 So, the Board could simply just find, based on that admission, that Yu
5 discloses what is needed for the claims.

6 On the Claim 2 and Claim 3 issue, if we could pull up Slide 12?
7 When asked about how Your Honors would write an opinion to say that it
8 has to be just a single island in Claim 3, it can't be more than one, I think the
9 only response was well, there's some difference between Claim 2 and Claim
10 3. Respectfully, any difference between Claim 2 and Claim 3 does not relate
11 to this issue of one island versus multiple islands. The difference between
12 Claim 2 and Claim 3 is that in Claim 2, there's only one transistor that needs
13 to be isolated, whereas in Claim 3 there needs to be a plurality of transistors
14 that are isolated. One way that I think we can think about this is, and we
15 went through a lot of issues with COVID recently, and in various places
16 people needed to be isolated. And Claim 2 requires that one person be
17 isolated. Claim 3 would require that multiple people be isolated. And let's
18 say multiple people are isolated because they're in one building. The fact
19 that maybe one person is in one room in the building, and a different person
20 is in a different room in the building, does not change anything. Everybody
21 is isolated. And in the same way, in the reference, all the transistors are
22 isolated by that outer trench that is shown there. It doesn't matter if there's
23 some extra trench in the middle, because the claim does not preclude there
24 being some extra trench in the middle. It says nothing about extra isolation.
25 All it requires is that there be some isolation of those transistors.

1 Lastly, on the combination with Burgener, you know, we heard from
2 Counsel about how, well, Burgener II, it's named, so you would use that.
3 But again, Burgener itself recognizes that other SOI technologies can be
4 used. It wouldn't say that if other SOI technologies couldn't be used. So,
5 right there, that's what gets us to Okashita. Interestingly, though, even if one
6 was to go to Burgener II and look at it, Burgener II also recognizes that it's
7 not limited to the UTSI technology that Patent Owner relies upon. If you
8 look at Burgener II, it's Exhibit 2004 at Column 13, around lines 55 to 58, it
9 says that, in one exemplary environment, the fully integrated RF switch 100
10 is fabricated on UTSi substrates, although other insulating substrate
11 technologies can be used. So, we don't think you need to get there, that the
12 Burgener reference itself allows for going to other technologies, but even
13 Burgener II allows for going to other technologies. And unless there's any
14 questions, I will stop there, Your Honors.

15 JUDGE JUNG: Just one question. Did you cite column 13, lines 50
16 to 55 in your briefing before? Or did you just --

17 MR. GOLDBERG: I noted it just now. I'm not sure if we had
18 previously cited it, Your Honor.

19 JUDGE JUNG: All right. Thank you.

20 JUDGE PESLAK: Mr. Goldberg?

21 MR. GOLDBERG: Yes?

22 JUDGE PESLAK: Talking about (audio interference) removed.

23 MR. GOLDBERG: I'm sorry, you were breaking up a little bit. Could
24 you repeat that?

25 JUDGE PESLAK: I'm sorry. Is that better?

26 MR. GOLDBERG: Yes.

1 JUDGE PESLAK: Sorry. We were talking about the (audio
2 interference).

3 MR. GOLDBERG: I'm sorry, we lost you again, Your Honor.

4 JUDGE PESLAK: Is that better?

5 MR. GOLDBERG: Yes.

6 JUDGE PESLAK: Did I hear you say that in Okashita there is an
7 overall trench that would isolate both, or is it -- my understanding was there
8 was two separate isolated trenches for 1 and 1 prime.

9 MR. GOLDBERG: So, Your Honor, if you want to look at Figure 19
10 of Okashita? There's the label at T1. That surrounds 1 and 1 prime. So, that
11 one trench that wraps all the way around both of the transistors, and then it
12 also has an extra part of it that goes down the middle, and would separate the
13 two. But because it has that one trench that goes all the way around both,
14 that meets the claim language.

15 JUDGE PESLAK: Then, this, whether an can be construed as
16 requiring more than one is really irrelevant to what's shown in Figure 19,
17 correct?

18 MR. GOLDBERG: That is our view. The only reason that we are
19 talking about that issue at all is because it's something that Patent Owner had
20 brought up, that they think that there's two islands, and that creates an issue.
21 And our point is just even if you wanted to look at it as two separate islands,
22 it still doesn't matter, because the claim would also cover that.

23 JUDGE ANDERSON: That was the only thing, really. Thank you.

24 MR. GOLDBERG: Thank you, Your Honors.

25 JUDGE ANDERSON: Thank you, Counsel. Patent Owner, you have
26 rebuttal time remaining. I'm not sure how long.

1 MR. MERCADANTE: Thank you.

2 JUDGE ANDERSON: Judge Jung has advised that you have 18
3 minutes.

4 MR. MERCADANTE: Thank you, Your Honors. I'm going to take
5 those two issues out of order. I'm again looking at the '886 patent, Claims 2
6 and 3. It seems to me that the panel understands this issue by this point. I
7 just wanted to say that Claim 3's requirement that the plurality, said
8 plurality, all of the cascaded transistors, is situated within an isolated island,
9 to us implies a single isolated island, because that's what does the isolation.

10 With respect to the citation to Burgener II which was brought up by
11 opposing counsel, it's highlighted right here. It's a single line in Burgener II.
12 Judge Jung, you're correct that it's not cited in any of the papers. And this
13 sort of open-ended patent drafting language does not provide the motivation
14 to the person of ordinary skill in the art to look to Okashita just because it
15 says you could potentially use other SOI technologies in view of the gobs of
16 evidence about the benefits of what Burgener II refers to as UTSI. Unless
17 there are any further questions from the panel, that's all that I have.

18 JUDGE ANDERSON: Thank you, Counsel.

19 MR. MERCADANTE: Thank you.

20 JUDGE ANDERSON: With that, let me just say that as to this
21 proceeding, we all appreciate the arguments made. Very well done, and
22 helpful to us in reaching a final decision. With that -- and thank you to the
23 NXP counsel. I know you can't speak on your own behalf, which is
24 unfortunate, but I'm glad that you were able to participate, even if only by
25 phone. With that, unless any party has anything further, we are adjourned.
26 We will reconvene in 10 minutes, which I have as a little bit after, that's

1 about 20 after the hour. So, let's just make it 20 after the hour. And we will
2 reconvene for the hearing on the 1404 case. Thank you. We are adjourned
3 until 20 after.

4 (Whereupon, the above-entitled matter went off the record at
5 3:11 p.m.)

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Patent 7,745,886 B2

PETITIONER:

Joshua Goldberg
Abhay Watwe
Chen Zang
Biju Chandran
Shawn Chang
FINNEGAN
joshua.goldberg@finnegan.com
abhay.watwe@finnegan.com
chen.zang@finnegan.com
biju.chandran@finnegan.com
shawn.chang@finnegan.com

PATENT OWNER:

Joseph Mercadante
Richard Cowell
FABRICANT LLP
jmercadante@fabricantllp.com
rcowell@fabricantllp.com