

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS
AMERICA, INC., AND NXP SEMICONDUCTORS, N.V.

Petitioners,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Patent No. 7,745,886

Filing Date: September 29, 2008

Issue Date: June 29, 2010

Inventors: Robert L. Zwingman and Marco Racanelli

Title: SEMICONDUCTOR ON INSULATOR (SOI)
SWITCHING CIRCUIT

PATENT OWNER'S NOTICE OF APPEAL

Case No. IPR2024-01402

Pursuant to 35 U.S.C. §§ 141 and 142 and 37 C.F.R. §§ 90.2 and 90.3, Patent Owner Harbor Island Dynamic LLC (“HID” or “Patent Owner”) hereby provides notice that it appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision entered March 16, 2026 (Paper 32, attached hereto as Exhibit A) and from all underlying orders, decisions, rulings, and opinions regarding U.S. Patent No. 7,745,886 (the “’886 patent”) in Case No. IPR2024-01402. This notice is accompanied by a Motion for Extension of time under 37 C.F.R. § 90.3 due to excusable neglect. For the limited purpose of providing the Director with the information requested in 37 C.F.R. § 90.2(a)(3)(ii), Patent Owner anticipates that the issues on appeal may include, but are not limited to: the Board’s claim constructions; its application of those constructions; any implied claim constructions; its obviousness determinations including that claims 3 and 8-19 of the ’886 patent are unpatentable under 35 U.S.C. § 103; any findings related to secondary considerations of non-obviousness; the findings, rulings and conclusions supporting or relating to those determinations; and any other issues decided adversely to Patent Owner in any orders, decisions, rulings, or opinions in IPR2024-01402.

Simultaneous with this submission, a copy of this Notice of Appeal is being

filed with the Clerk of the United States Court of Appeals for the Federal Circuit and are being submitted electronically through the Court's CM/ECF system, together with the requisite fee in the amount of \$600.00. In addition, a copy of this Notice of Appeal is being filed with the Patent Trial and Appeal Board and served upon counsel of record for Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.

Respectfully submitted,

Dated: May 26, 2026

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EXHIBIT A

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
SAMSUNG ELECTRONICS AMERICA, INC., and
NXP SEMICONDUCTORS, N.V.¹,
Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,
Patent Owner.

IPR2024-01402
Patent 7,745,886 B2

Before HYUN J. JUNG, GREGG I. ANDERSON, and
ARTHUR M. PESLAK, *Administrative Patent Judges*.

ANDERSON, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ NXP Semiconductors N.V. filed a petition and a motion for joinder in IPR2025-00954 that were granted. NXP Semiconductors N.V. has been joined as a petitioner in this proceeding.

I. INTRODUCTION

A. Background and Summary

Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1–19 of U.S. Patent No. 7,745,886 B2 (Ex. 1001, “the ’886 patent”). Petitioner filed a Declaration of Dr. Scott E. Thompson, Ph.D., in support of the Petition. Ex. 1002 (“Thompson Dec.”). Harbor Island Dynamic, LLC (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). On April 4, 2025, we instituted this *inter partes* review as to the Challenged Claims and all grounds presented in the Petition. Paper 9 (“Inst. Dec.”). Following institution, Patent Owner filed a Response to the Petition (“PO Resp.”) limited to the patentability of the challenged claims. Paper 18. In support of the Patent Owner’s Response, Patent Owner filed a Declaration of John Berg. Ex. 2006. Patent Owner also filed an Unopposed Motion to Amend, cancelling claims 1, 2, and 4–7. Paper 19 (“Mot.”). We grant the motion. This proceeding is therefore limited to the patentability of claims 3 and 8–19 (“challenged claims”).

Petitioner filed a Reply (“Pet. Reply”). Paper 22. Petitioner filed a Supplemental Declaration of Dr. Scott E. Thompson, Ph.D. with the Reply. Ex. 1026 (“Thompson Supp. Dec.”). Patent Owner filed a Sur-reply (“Sur-reply”). Paper 24. An oral hearing was held on January 7, 2026, and the transcript (“Tr.”) was entered into the record. Paper 31.

We have jurisdiction under 35 U.S.C. § 6. This is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of the Challenged Claims. For the reasons discussed below, we determine that Petitioner

establishes by a preponderance of the evidence that all challenged claims are unpatentable.

B. Real Parties in Interest

The parties assert that they are the sole real parties in interest. Pet. 88; Paper 5, 2 (Patent Owner’s Mandatory Notice).

C. Related Matters

The parties have identified the following pending district court cases:

- *Harbor Island Dynamic, LLC v. Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.*, Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex.) (“District Court Litigation”); and
- *Harbor Island Dynamic, LLC v. NXP Semiconductor, N.V. et al.*, Case No. 2:24-cv-00717-JRG-RSP (E.D. Tex.).

Pet. 88; Paper 5, 2.

D. Prior Art and Asserted Grounds

Petitioner’s grounds rely on the following prior art references:

Name	Reference	Exhibit No.
Yu	U.S. Pat. 6,737,682 B1, iss. May 18, 2004	1005
Okashita	U.S. Pat. 6,836,172 B2, iss. Dec. 28, 2004	1004
Burgener	U.S. Pat. App. Pub. 2006/0270367 A1, pub. Nov. 30, 2006	1006

Petitioner asserts that the challenged claims would have been unpatentable on the following grounds:

Claim(s) Challenged ²	35 U.S.C. §	Reference(s)/Basis
3	103	Okashita

² Challenged claims remaining after Motion to cancel claims 1, 2, and 4–7.

Claim(s) Challenged ²	35 U.S.C. §	Reference(s)/Basis
3	103	Okashita, Yu
3	102	Yu
3, 8–19	103	Burgener, Okashita
3, 8–19	103	Burgener, Okashita, Yu

E. Overview of the '886 Patent

The '886 patent is directed to a circuit for correcting distortion of radio signals, in particular:

a switching circuit including a number of transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer. Each transistor has a source/drain junction that does not contact the buried oxide layer, thus forming a source/drain junction capacitance. The disclosed switching circuit also includes at least one trench extending through the device layer and contacting a top surface of the buried oxide layer, thus electrically isolating at least one of the transistors in the switching circuit so as to reduce voltage and current fluctuations in the device layer. The disclosed switching circuit may be coupled to a power amplifier or a low noise amplifier and an antenna in a wireless communications device, and be controlled by a switch control signal in the wireless communications device.

Ex. 1001, code (57).

F. Challenged Claims

Claims 3 and 8–19 remain subject to the challenge. Claims 1, 12, and 16 are independent. Claims 1 and 3 are reproduced below.

[1.pre]³ A switching circuit comprising:

[1a] a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;

[1b(i)] each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer,

[1b(ii)] thereby forming a source/drain junction capacitance;

[1c(i)] at least one trench extending through said device layer and contacting a top surface of said buried oxide layer,

[1c(ii)] thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.

3. The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer.

The issues raised are limited to the following elements recited in claims 1 and 3. The issue raised with respect to claim 1 is whether the prior art teaches or suggests, in limitations 1b(i) and 1b(ii), a source drain junction that “does not contact said buried oxide layer, thereby forming a source/drain junction capacitance.” *See, e.g.*, PO Resp. 23–24 (Ground 4). The issue with respect to claim 3 is whether the prior art teaches or suggests that the “cascaded transistors” are “situated within an isolated island in said device layer.” *Id.* at 15–16 (Ground 2). Patent Owner argues that the

³ Limitations are identified by letter, letter and number, or letter, number and subsections (i) etc. in the Petition. *See, e.g.*, Pet. 9–18 showing for cancelled claim 1 and limitations [1pre] through [1c(ii)].

Petition lacks a reasonable basis for the combinations used. *Id.* at 18–23 (Ground 3).

II. ANALYSIS

Petitioner’s grounds are based upon the prior art teachings of Okashita, Yu, Burgener, alone or combinations thereof. Pet. 6. Patent Owner offers specific arguments against each of the remaining grounds, with each argument based on the limitations of claims 1 and 3. *See* PO Resp. 1–2.

A. Legal Standards Used in the Merits Analysis

“Under 35 U.S.C. § 102(b), a prior art reference will anticipate if it ‘disclose[s] each and every element of the claimed invention . . . arranged or combined in the same way as in the claim.’” *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1341 (Fed. Cir. 2016) (alterations in original) (footnote omitted). In *Blue Calypso*, the Federal Circuit went on to explain that “a reference can anticipate a claim even if it ‘d[oes] not expressly spell out’ all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would ‘at once envisage’ the claimed arrangement or combination.” *Id.* (quoting *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015)) (alteration in original).

A claim is unpatentable under 35 U.S.C. § 103 if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (citing 35 U.S.C. § 103 (2000)). The question of obviousness is resolved on the basis of underlying

factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner asserts:

A person of ordinary skill in the art (“POSITA”) would have had at least a master’s degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems and semiconductor dice. Additional relevant work experience can compensate for less education, and vice versa.

Pet. 6 (citing Ex. 1002 ¶¶ 105–107).

Patent Owner proposes a slightly different level of ordinary skill, arguing that a bachelor’s degree, not a master’s degree, is all that is required because that is the “target audience for the ’886 Patent.” PO Resp. 11.

Patent Owner does not otherwise dispute Petitioner’s proposed level of skill. *Id.*

We used Petitioner’s proposed definition in the Institution Decision. Inst. Dec. 13. Neither party argues any issue as dependent on the level of ordinary skill or the differences between the proposals. Accordingly, the issues here are not dependent on the level of ordinary skill and the result is the same regardless of which definition is adopted. On this record, there is no reason to change from Petitioner’s definition used in the Institution Decision.

C. Claim Construction

Under 37 C.F.R. § 42.100(b), we apply the claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). That is, “the words of a claim ‘are generally given their ordinary and customary meaning,’” which is “the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.” *Id.* at 1312–13. Petitioner and Patent Owner both assert that no terms require express construction. Pet. 5; PO Resp. 11–12.

1. “cascaded transistors”

In the Institution Decision we specifically identified “cascaded transistors” as a term that might require construction during trial. Inst. Dec. 17–18. At the hearing, the Petitioner argued that “cascaded transistors” means “[ar]ranged in a series of or in succession of stages so that each stage derives from or acts upon the product of the preceding [transistor]” and that there is no dispute that the limitation is taught by the prior art. Tr. 9:15–22. Patent Owner takes no position as to whether or not the prior art discloses “cascaded transistors.” *Id.* at 33:13–21 (“For the remainder of this proceeding, post institution, we have not taken any position regarding the scope of the cascaded transistors or the disclosure of the cascaded transistors in any of the prior art. We have not disputed that.”). Because Patent Owner takes no position on the issue, there is no dispute that “cascaded transistors” are shown in the prior art, construction is not necessary. *Realtime, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am.*

Sci. & Eng'g, Inc., 200 F.3d 795, 803 (Fed. Cir. 1999) (alteration in original)).

2. “isolated island”

Patent Owner disputes Petitioner’s contention that the prior art teaches or suggests claim 3’s recitation of “said plurality of cascaded transistors is situated within an isolated island.” Pet. 35–36; PO Resp. 16–17. Although the parties dispute whether an “isolated island” is shown in the prior art, neither party proposes a construction for the term “isolated island.” We agree that the arguments presented do not require construction of “isolated island.” The issues can be determined on the plain meaning of the term in view of the arguments made. *See* Section II.D below.

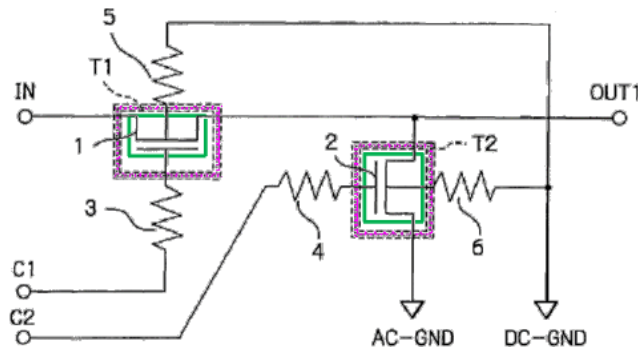
D. Asserted Obviousness of Claim 3 over Okashita (Ground 2)

Petitioner asserts that remaining claim 3 is obvious over Okashita. Pet. 28–36. Petitioner relies on the embodiment shown in Figures 7 and 9 of Okashita. We provide a brief overview of Okashita before turning to the dispute between the parties.

1. *Okashita (Exhibit 1004)*

Figure 7 of Okashita, with annotations provided by Petitioner, is reproduced below:

Fig. 7



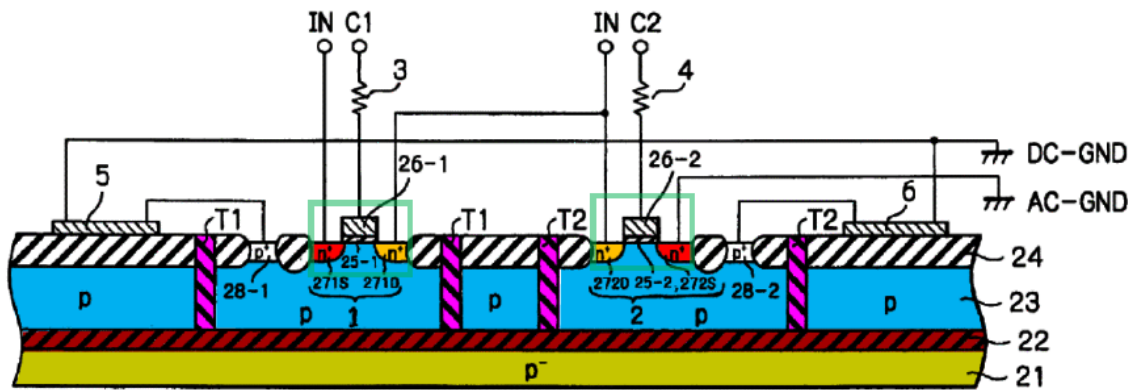
Pet. 7 (providing the above annotated copy of Ex. 1004, Fig. 7). Figure 7 of Okashita depicts a semiconductor switch apparatus. Ex. 1004, 5:21–23. Series transistor 1 (green-colored box) is connected between input terminal IN and output terminal OUT1, and shunt transistor 2 (green-colored box) is connected between output terminal OUT1 and AC ground terminal AC-GND. *Id.* at 4:11–17.⁴ Control terminals C1 and C2 are connected to the gates of transistors 1 and 2, respectively, and the back gates of the transistors are connected to DC ground terminal DC-GND. *Id.* at 4:17–23. Okashita states that the features in Figure 7 that distinguish it over the prior art are resistors 5 and 6, as well as isolation trenches T1 and T2 (purple-colored boxes). *Id.* at 5:29–35. The resistors and trenches are for “preventing radio frequency signals from superposing on each other.” *Id.*

Figure 9 of Okashita is a cross-sectional view of the semiconductor switch apparatus of Figure 7. Ex. 1004, 2:24–25; 5:36–40. An annotated version of Figure 9 of Okashita is reproduced below:

⁴ Okashita does not explicitly describe all of the elements of the circuit in Figure 7. Thus, we cite Okashita’s earlier descriptions of functionally similar elements.

i-

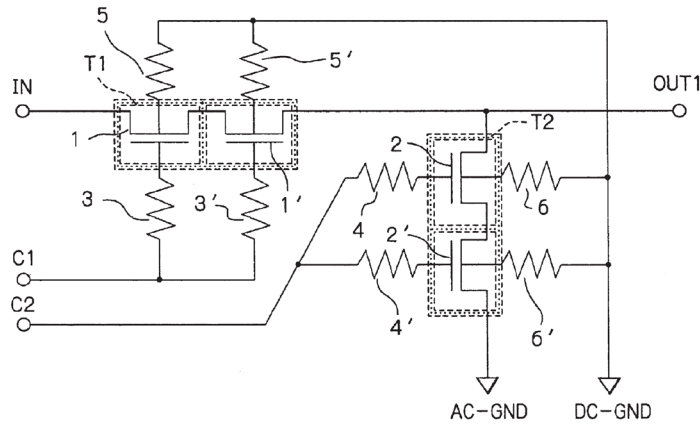
Fig. 9



Pet. 8 (providing the above annotated copy of Ex. 1004, Fig. 9). The semiconductor depicted in Figure 9 of Okashita is a semiconductor-on-insulator configuration, with base silicon substrate 21 (colored gold), silicon oxide layer 22 (colored red), and p-type silicon layer 23 (colored blue). Ex. 1004, 5:41–44. Transistor 1 is depicted as made of a gate (25-1, 26-1), source (271S, colored red), and drain (271D, colored yellow). *See id.* at 5:55–63. Notably, none of the gate, source, or drain extends down to silicon oxide layer 22. *Id.* at Fig. 9. In contrast, isolating trench T1 (colored purple) extends down to silicon oxide layer 22, surrounding p-type silicon layer 23. *Id.* at 5:46–54, Fig. 9.

Figure 19 of Okashita is reproduced below:

Fig. 19



Ex. 1004, Fig. 19. Figure 19 of Okashita is similar to Figure 7 discussed above, with the difference being that in Figure 19, transistor 1 is connected in series with transistor 1', and transistor 2 is connected in series with transistor 2'. *Id.* at 8:30–37. Adding the second transistor to each of the existing transistors serves to modify the threshold voltage required to turn on transistors 2 and 2'. *Id.* at 8:38–46 (explaining that, in Figure 19, the threshold voltage to turn on transistors 2 and 2' is $\Delta V_{in}/4 > V_{th}$ instead of $\Delta V_{in}/2 > V_{th}$, as there are now four transistors instead of 2).

2. “*plurality of cascaded transistors is situated within an isolated island in said device layer*” (“isolated island” limitation) (claim 3)

Petitioner asserts that claim 3 would have been obvious in view of Okashita. Pet. 28–39. With respect to claim 1, from which claim 3 depends, the obviousness ground relies on an embodiment disclosed in Figures 19 and 20 of Okashita. *Id.* at 28–33. Further, claim 2 introduces the term “isolated island,” which also appears in claim 3, and Petitioner asserts that Okashita

teaches an isolated island. *Id.* at 35 (citing Ex. 1002 ¶ 166; Ex. 1004, 8:30–37, 8:47–54).

In *Okashita*, each of the transistor pairs 1 and 1' and 2 and 2' are isolated by the trench insulating layers T1 and T2, respectively, “so that the leakage of radio frequency signals . . . can be sufficiently suppressed.” Ex. 1004, 8:47–54. Based on *Okashita*'s teaching, Petitioner alleges a person of ordinary skill in the art would have understood that the trench T1 surrounding the plurality of MOS transistors 1, 1' effectively places these MOS transistors within an isolated “first region” in the silicon layer to minimize radio frequency signal leakage from, and to, the first region. Pet. 35 (citing Ex. 1002 ¶ 167; Ex. 1004, 8:47–54, 9:21–25, Figs. 19–20).

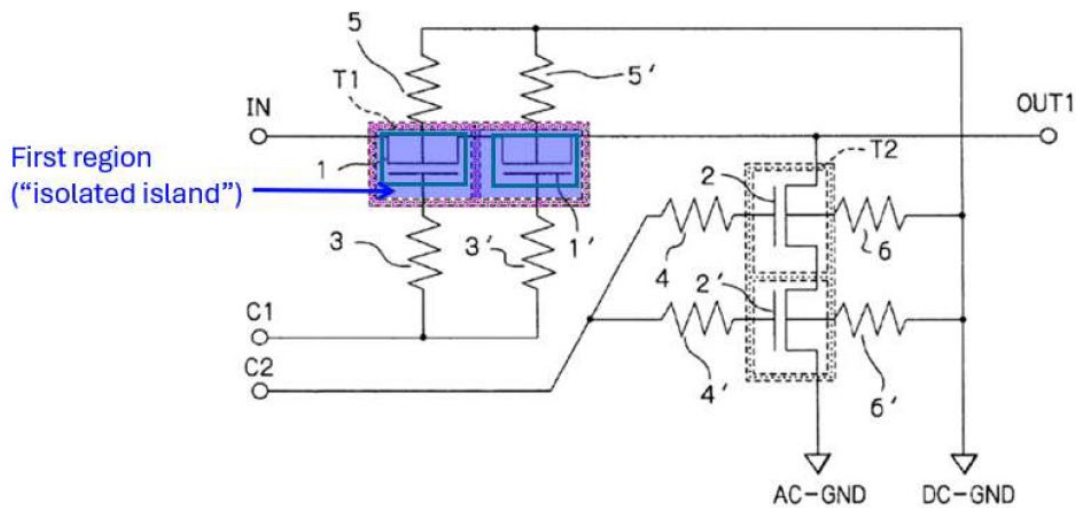
Patent Owner argues that *Okashita* does not disclose the “isolated island” and that Petitioner's argument that the limitation is obvious admits as much. PO Resp. 17. Citing to the Berg Declaration, Patent Owner argues that *Okashita* teaches that “each of the MOS transistors 1, 1', 2 and 2' is isolated by the trench insulating layers T1 and T2, so that the leakage of radio frequency signals from the silicon layer 23 of the MOS transistor 1 *to that of the MOS transistor 1'* . . . can be sufficiently suppressed.” *Id.* (citing Ex. 2006 ¶ 45 (quoting Ex. 1004, 8:47–54)) (alteration in original). Patent Owner concludes that

Since *Okashita* teaches the need to suppress leakage of radio signals between MOS transistor 1 and MOS transistor 1', the [person of ordinary skill in the art] would not have been motivated to remove the isolation trenches between these two transistors, merely to ensure more consistent performance. Ex. 2006, ¶ 46. Therefore, the Petition has not articulated a motivation to modify *Okashita* to reach the invention of Claim 3.

Id. at 18.

Petitioner responds that it is not arguing a motive to modify Okashita, a position Patent Owner ultimately agrees with. Pet. Reply 3; *see also* PO Sur-reply 2 (agreeing that Petitioner is not arguing a motive to modify Okashita). Rather, Petitioner argues it would have been obvious to a person of ordinary skill in the art that the trench T1 teaches an “isolated island.” Pet. Reply 2–3. This argument is illustrated by an annotation of Figure 19 reproduced below.

Fig. 19



Id. at 3. As stated above, Petitioner reasserts a person of ordinary skill in the art “would have understood that the trench T1 surrounding the plurality of MOS transistors 1, 1' effectively places these MOS transistors within an isolated ‘first region’ in the silicon layer.” *Id.* at 2. *See also* Pet. 35 (citing Ex. 1002 ¶ 167; Ex. 1004, 8:47–54, 9:21–25, Figs. 19–20).

Petitioner alleges that “‘an’ as used in claim 3 means ‘one or more’ in open-ended claims.” Pet. Reply 4. Quoting from *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000), Petitioner asserts that

“an indefinite article ‘a’ or ‘an’ in patent parlance carries the meaning of ‘one or more.’” *Id.*

At the hearing, Patent Owner argued that even if the transistors 1 and 1’ of Okashita are electrically connected they are still each a separate “isolated island.” Tr. 34:5–35:11. Patent Owner argues that two electrically connected transistors like 1 and 1’, as shown above in Okashita Figure 19, cannot be characterized as “an isolated island.” PO Sur-reply 4–5.

Patent Owner further argues that a new improper claim construction argument is being advanced by Petitioner. PO Sur-reply 4. Patent Owner argues claim 3 recites “an isolated island” which it alleges is “singular in the claim.” Tr. 36:1–24. According to Patent Owner, because the two transistors 1 and 1’ or 2 and 2’ of Okashita’s Figure 19 are “isolated from one another” they “cannot be a single island.” PO Sur-reply 5.

Petitioner’s argument regarding claim interpretation is in response to arguments raised by Patent Owner and is not new or waived. Patent Owner argues “[t]he Petition claims that Okashita anticipates Claim 2^[5] because it shows each transistor in its own isolated island but renders obvious Claim 3 with a modification to the structure of the isolated island.” PO Resp. 16 (citing Ex. 1002 ¶¶ 140–141); *see also* Pet. 35–35 (Petitioner’s showing regarding claim 3 under Ground 2). Petitioner responds specifically to Patent Owner’s argument that claim 2’s recitation of the “isolated island” would somehow preclude the regions defined by Trenches T1 and T2 from qualifying as the “isolated island.” Pet. Reply 2.

⁵ As noted above, cancelled claim 2 recites the term “isolated island” and was shown in the Petition in connection with Ground 1, anticipation of claim 2 by Okashita. Pet. 7 (introducing Ground 1), 23–24 (showing regarding claim 2).

Both transistors 1 and 1' or 2 and 2' would together be isolated by the Trenches T1 and T2, respectively, surrounding the plurality of MOS transistors 1, 1' and 2 and 2'. Nothing precludes the two transistors from constituting an “isolated island.” Isolating the two transistors from the surrounding materials is sufficient to form an “isolated island.” Isolating each of the transistors from each other within the “isolated island” does not change the fact that the “isolated island” itself exists.

We agree with Petitioner that a person of ordinary skill in the art would have understood that the trench T1 surrounding the plurality of MOS transistors 1, 1' effectively places these MOS transistors within an isolated “first region” in the silicon layer to minimize radio frequency signal leakage from, and to, the first region. Pet. 35 (citing Ex. 1002 ¶ 167; Ex. 1004, 8:47–54, 9:21–25, Figs. 19–20). Indeed, Okashita says that Trenches T1 and T2 “isolate” the transistor 1 and 1' and 2 and 2' respectively. Ex. 1004, 8:47–50. Petitioner has met its burden and, beyond a mere denial, Patent Owner does not argue that Okashita's first region is not an “isolated island” and has not rebutted Petitioner's showing. See PO Resp. 16–17; see also PO Sur-reply 2 (“showing two transistors located in two separate isolated islands can be shoehorned into the claim”).

3. Conclusion on Ground 2

We determine that Petitioner has established by a preponderance of the evidence that claim 3 would have been obvious over Okashita.

E. Obviousness of claim 3 over Okashita and Yu (Ground 3)

Petitioner asserts that remaining claim 3 is obvious over Okashita and Yu. Pet. 44–49. Petitioner relies on the embodiment shown in Figures 7 and 9 of Okashita as shown in Grounds 1 and 2 for limitations 1pre, 1a,

1c(i), and 1c(ii). *Id.* at 44, 46. The combination of Okashita and Yu is the basis for the showing for limitations 1b(i), 1b(ii), and claim 3. *Id.* at 44–46.

Patent Owner’s only argument against Ground 3 is an alleged lack of any motive to combine Okashita and Yu. PO Resp. 18–23. We provide a brief overview of Yu before analyzing the sole dispute.

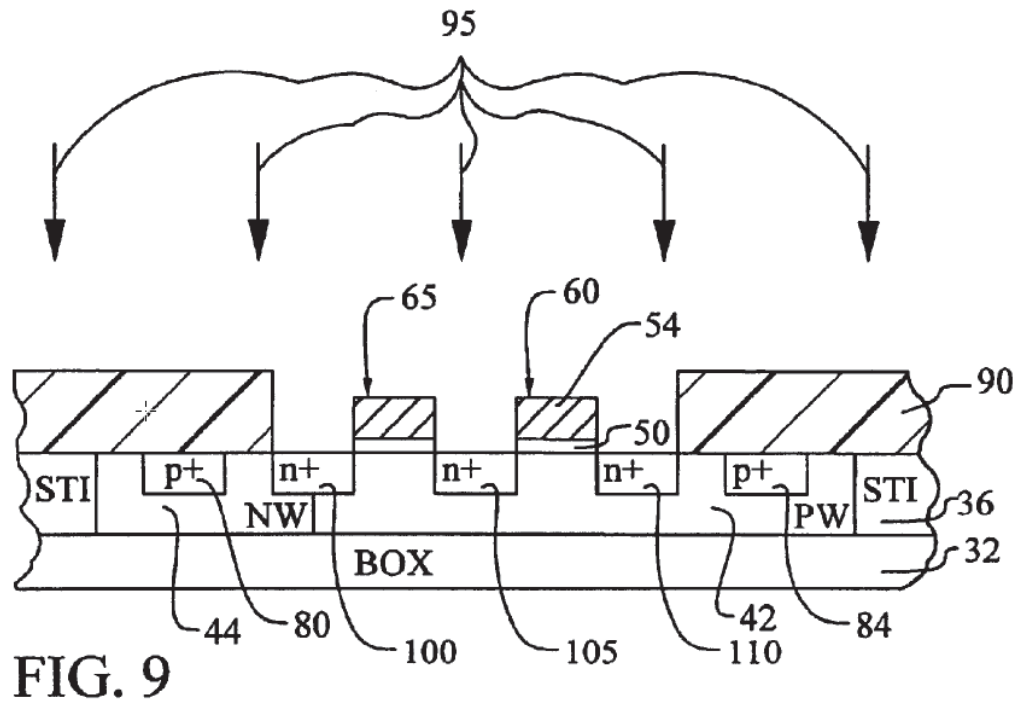
1. Yu (Exhibit 1005)

Yu discloses “a low-voltage triggering, silicon-controlled rectifier” (LVT-SCR) that is fabricated using an SOI system. Ex. 1005, 1:10–13. An LVT-SCR is a “switching device.” *Id.* at 6:4–11. As Yu explains, the SOI system includes a silicon layer 34 formed on a buried oxide layer 32, which is formed on a substrate 30, as shown in Yu’s Figure 3. *Id.* at 3:63–65, Fig. 3. Yu teaches that prior art SCR (“silicon-controlled rectifier”) devices fabricated using a bulk semiconductor use shallow trench isolation (“STI”) to define areas for active devices, or OD areas. *Id.* at 1:23–33. Forming SCR devices in an SOI process with STI, however, presents problems including a lower energy dissipation level causing device failure, influencing diode leakage characteristics, restricting formation of the SCR device, and, if the silicon layer is relatively thin, the bipolar devices may not function. *Id.* at 2:4–17.

To address these problems, Yu teaches that it is important not only to form the STI regions in the silicon layer 34 of the SOI to define an active area, but to keep the STI regions outside of the active area of the planned LVT-SCR device. Ex. 1005, 4:8–15. STI regions “do not extend into the LVT-SCR device nor do they separate the first or second type doped regions” formed in first and second well layers 42 and 44. *Id.* at 5:16–19, Fig. 9. By forming the STI regions down to the buried insulator layer, each

active area may be completely isolated. *Id.* at 1:67–2:3. STI regions define “active area regions of silicon layer 34 where active devices may be subsequently formed.” *Id.* at 4:8–12. The STI regions are not formed within the area of the planned SCR devices. *Id.* at 4:12–14.

Figure 9 of Yu is reproduced below.



Ex. 1005, Fig. 9. As shown in Figure 9, “doped regions 80, 84, 100, 105, and 110, are formed in the upper part of the wells 42 and 44 and do not extend to the buried oxide layer 32.” *Id.* at 6:46–54, Fig. 10. “[T]he original silicon layer . . . is thick enough so that the doped regions do not completely deplete the wells 42 and 44.” *Id.* at 6:46–54.

2. Motivation to Combine Okashita and Yu

Petitioner argues that both Okashita and Yu “have transistors fabricated on an SOI structure.” Pet. 42 (citing Ex. 1004, 1:47–58, 5:41–46, Fig. 9; Ex. 1005, 3:53–4:3, Fig. 3; Ex. 1002 ¶ 176). Petitioner alleges both

have cascaded transistors. *Id.* (citing Ex. 1004, 8:30–34; Ex. 1005, 5:44–57). Petitioner also points out that the transistors are also both “situated within an isolated island that is surrounded by a shallow trench isolation (STI) region 36,” in the case of Okashita. *Id.* (citing Ex. 1004, 4:8–10, 6:50–51, Fig. 10; Ex. 1002 ¶ 176).

Petitioner alleges that a person of ordinary skill in the art would have been motivated to combine Yu with Okashita because a person of ordinary skill in the art would want to

ensure that *Okashita*’s trench isolation regions are not formed within the active area and to maintain a sufficient thickness in the silicon layer so that the transistors’ source/drain interfaces do not extend to the silicon oxide layer, as taught by *Yu* [citing Pet. 39–41 (overview of *Yu*)] because doing so would achieve similar thermal and electrical benefits as described by *Yu* in *Okashita*’s switching device.

Pet. 43 (citing Ex. 1005, 2:4–17; Ex. 1002 ¶¶ 177–178).

Based on the Thompson Declaration, Petitioner alleges that the lower thermal conductivity of silicon dioxide compared to silicon, if the source/drain junctions of *Okashita*’s cascaded transistors were to contact the silicon oxide layer, the transistors would operate at higher temperatures, which could then negatively impact circuit performance and “fail at a lower energy dissipation level” as taught by *Yu* (2:4–17).

Pet. 43 (citing Ex. 1002 ¶¶ 97–98, 179; Ex. 1010⁶, 59–60; Ex. 1013⁷, 27–28).

⁶ Andrew Marshall et al., *SOI Design: Analog, Memory and Digital Techniques*, copyright 2002 and 2003.

⁷ Ching-Te Chuang et al., *SOI for Digital CMOS VLSI: Design Considerations and Advances*, Proceedings of the IEEE, Vol. 86, No. 4, April 1998.

Because of the significant similarities between Okashita and Yu, Petitioner concludes a person of ordinary skill in the art “would have had a reasonable expectation of success in fabricating Okashita’s transistors based on Yu’s SOI process.” Pet. 43 (citing Ex. 1002 ¶ 180). Additionally, Petitioner alleges the combination “would have been a straightforward use of a known technique to enhance a similar device in the same manner.” *Id.* at 43–44 (citing *KSR*, 550 U.S. at 417–18; Ex. 1002 ¶ 180).

Patent Owner argues that there are “meaningful differences” between Okashita and Yu that mean there is a lack of “a sufficient motivation to combine with a reasonable expectation of success.” PO Resp. 18 (citing Ex. 2006 ¶¶ 47–54). Patent Owner thus argues that Okashita and Yu are not analogous because they are not in the same field of endeavor.⁸ *Id.* at 21. Yu is “a method to form a low voltage triggering, silicon-controlled rectifier (SCR) SOI device having improved ESD^[9] performance.” *Id.* (citing Ex. 1005, 1:10–13). Conversely, according to Patent Owner, Okashita is a semiconductor switch which works in a low voltage environment, between -3V and 3V. *Id.* at 19 (citing Ex. 1004, 7:18–29, 3:11, 3:40; Ex. 2006 ¶ 48).

Patent Owner cites to problems identified in Okashita relating to semiconductor switching in, for example, a mobile telephone. PO Resp. 19 (citing Ex. 1004, 1:11–40). Patent Owner emphasizes that Yu is concerned with ESD protection and heat transfer problems. *Id.* at 20–21 (citing Ex. 1005, 1:59–2:17). Patent Owner cites to several reasons there would be

⁸ The parties agree that that “prior art is analogous to a challenged patent if it (1) is from the same field of endeavor, or (2) is reasonably pertinent to the problem addressed by the patent.” Pet. Reply 5 n.3; PO Resp. 22; PO Sur-reply 6–7.

⁹ ESD is electrostatic discharge. Ex. 2006 ¶ 47.

no expectation of success in combining Yu with Okashita, including differences in voltage circuits, addressing different problems, that Yu does not isolate transistors, as required by claim 3, and the Trenches T1 and T2 (*see* Section II.D above) are to suppress radio frequency leakage (Ex. 1004, 8:47–54; Ex. 2006 ¶ 53). *Id.* at 22–23.

Petitioner responds by arguing that Okashita and Yu are analogous art. Pet. Reply 5–7. Furthermore, Petitioner asserts that “motivation to combine may arise from any need or problem known in the field of endeavor, not just the specific issue addressed by the patent” and the references to be combined need not address the same problem. *Id.* at 10 (citing *In re Kahn*, 441 F.3d 977, 986 (Fed. Cir. 2006)). Petitioner additionally argues that “Yu further teaches transistor configurations that enhance thermal and electrical performance in SOI switching devices (*see* Pet.[39–43]; [Ex. 1002] ¶¶ 89–98, 176–180), which a [person of ordinary skill in the art] would recognize as directly applicable to Okashita’s architecture.” *Id.*

Patent Owner argues that the structure and function of Okashita and Yu are different and, therefore, Okashita and Yu are not in the same field of endeavor. PO Sur-reply 7–8. In addition, according to Patent Owner, Yu is not reasonably pertinent to the “field of endeavor of the ’886 patent” because it relates to “a high voltage silicon-controlled rectifier that does not use transistors.” *Id.* at 8.

We find that Petitioner has sufficiently shown Yu is analogous art to Okashita. Both references are directed to the manufacture of semiconductors, which we find to be the field of endeavor. Ex. 1004, 1:47–58; Ex. 1005, 1:16–26. More specifically, we agree with Petitioner and find that both references are in the same field of endeavor because they relate to

manufacture of semiconductor circuits with cascaded transistors having an SOI configuration. Pet. Reply 6 (citing Pet. 7–8, 39–40; Ex. 1002 ¶¶ 77–80, 90–91). Because we find the references relied upon are in the same field of endeavor, we need not reach whether they are reasonably pertinent to the problem faced by the inventor.

We also find that Petitioner has shown rational underpinnings for combining Okashita and Yu. Pet. 43–44. That the references have differences is not the test. Rather, the test is whether a person of ordinary skill in the art would have had motivation to combine them. We find there is sufficient motivation. *Id.* at 43 (citing Ex. 1005, 2:4–17; Ex. 1002 ¶¶ 177–178).

3. Conclusion on Ground 3

Patent Owner does not argue any other reason that Ground 3 has not been sufficiently shown. Based on the full record, we determine that Okashita and Yu teach or suggest all the limitations of claim 3 and that one of ordinary skill in the art would have combined the references in the manner asserted with a reasonable expectation of success. We thus determine that Petitioner has established by a preponderance of the evidence that claim 3 would have been obvious over the combination of Okashita and Yu.

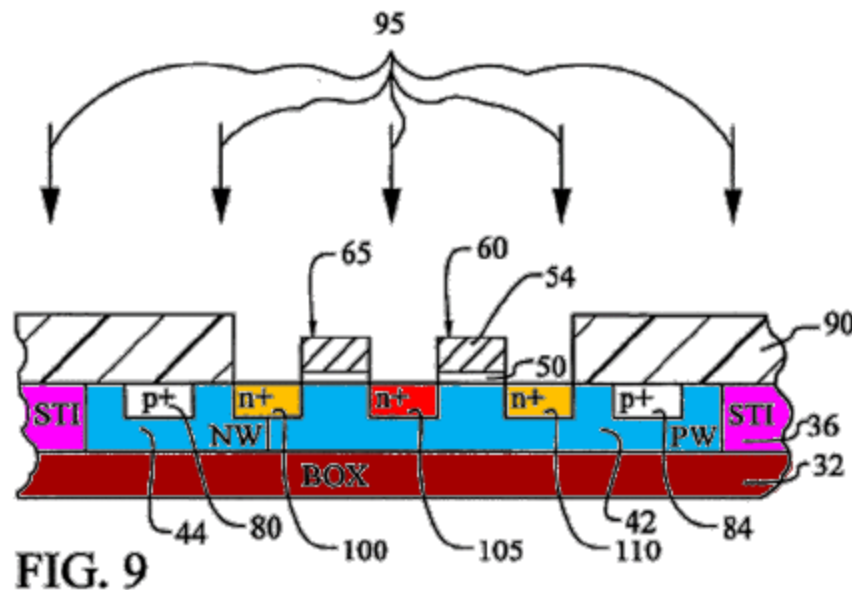
F. Anticipation of Claim 3 by Yu (Ground 4)

Petitioner asserts that remaining claim 3 is anticipated by Yu. Pet. 49–56. Patent Owner’s only argument against Ground 4 is that the “Figures and disclosures in Yu clearly show that the source/drain junction of one of the transistors electrically contacts the buried oxide layer, as

prohibited by the claims.” PO Resp. 23. Patent Owner’s argument is based on claim 1 limitations 1b(i) and 1b(ii), reproduced immediately below. *Id.* at 23–24. *See also* Tr. 24:19–20 (Ground 4 “one and only one issue”).

1. “each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance” (limitations 1b(i) and 1b(ii))

Petitioner refers to the annotated version of Figure 9 of Yu reproduced below to illustrate its position.

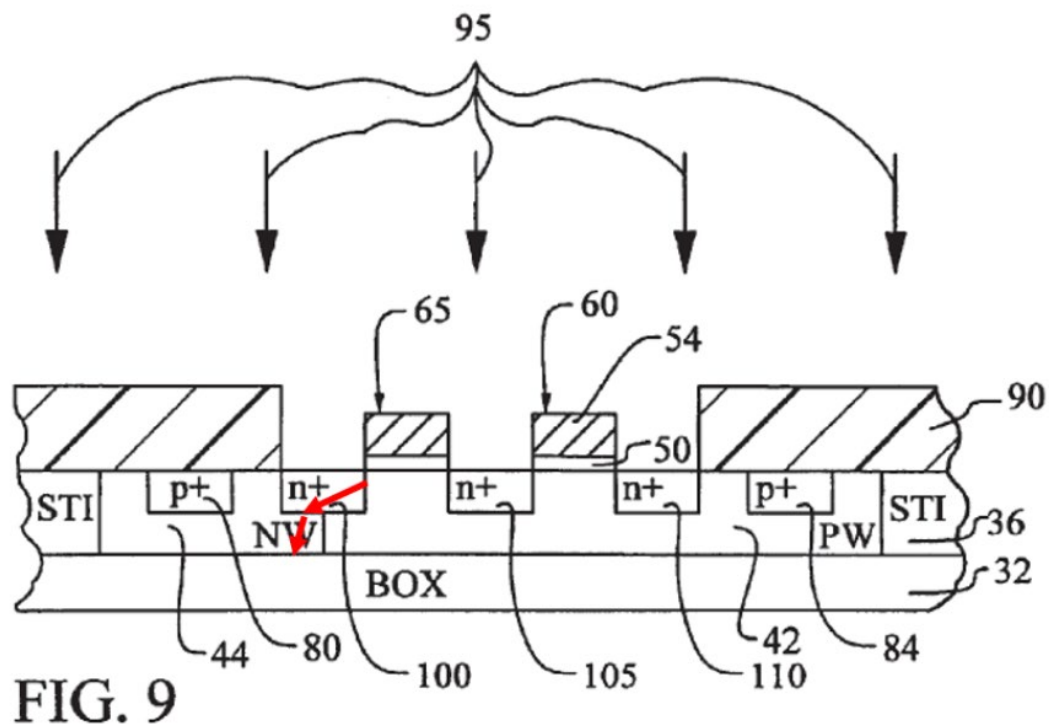


Pet. 51. Figure 9 of Yu discloses two transistors in a semiconductor-on-insulator configuration. The first transistor is formed by gate 60, doped region 110 (colored yellow), and doped region 105 (colored red). The second transistor is formed by gate 65, doped region 105 (colored red), and doped region 100 (colored yellow). The doped regions 100, 105, and 110 are depicted within silicon wells 42 and 44, but not extending all the way down to buried oxide layer 32 (labeled “BOX,” colored brown). *Id.*; Ex. 1005, 6:46–54. The transistors are depicted as surrounded by shallow

trench isolations 36 (labeled “STI,” colored purple), which extend down to buried oxide layer 32. Pet. 51; Ex. 1005, 5:16–19, 4:8–12, 3:63–64.

Petitioner’s position is that doped region 105 is the source for both transistors and the doped regions 100 and 110 are the respective drains for the transistors. Pet. 51–52. Petitioner asserts that none of the doped regions extend to buried oxide layer 32, meeting the limitation, “a source/drain junction that does not contact said buried oxide layer.” *Id.* at 52 (citing Ex. 1005, 6:46–54; Ex. 1002 ¶ 202).

Patent Owner argues that Yu’s “source/drain junction of one of the transistors *electrically* contacts the buried oxide layer, as prohibited by the claims.” PO Resp. 23 (emphasis added). Patent Owner’s annotation of Yu’s Figure 9 is reproduced below.



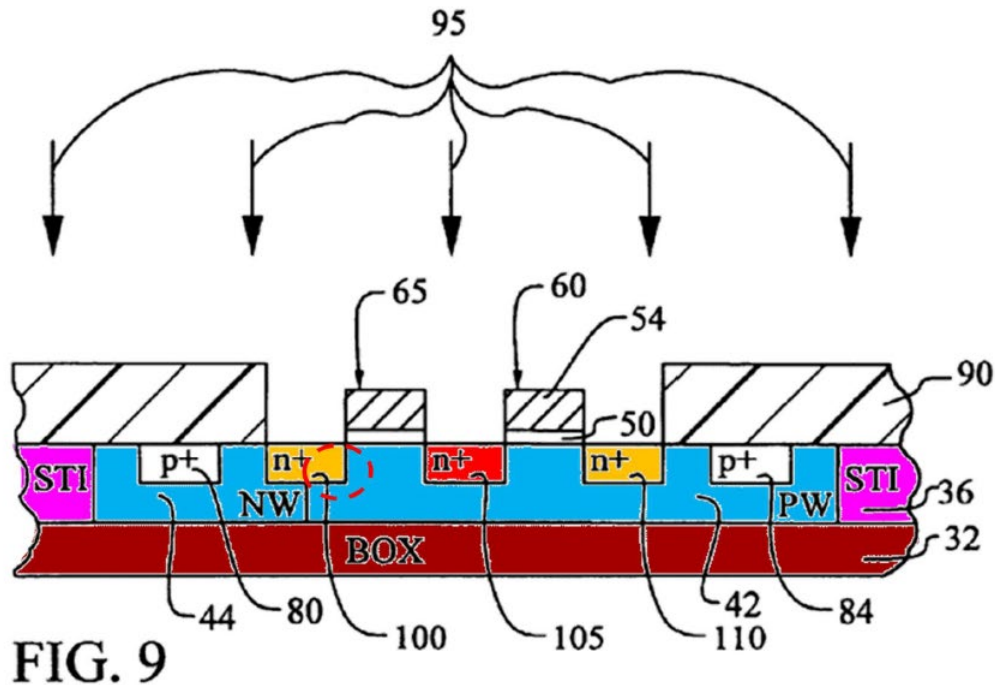
Id. at 25. Based on Yu’s description referencing Figure 10, which like Figure 9 illustrates the STI region 36 and the buried oxide layer 32, Patent

Owner argues “the *fifth doped region 100 is coupled to the second well 44*, and the third doped region is coupled to the first doped region to form the cathode.” *Id.* at 26 (citing Ex. 1005, 5:41–53). Patent Owner adds that Yu explains that “‘doped region 100 is coupled to the second well 44’ and, therefore, doped region 100 (the N+ well) *does* electrically contact the buried oxide layer, even if there is no physical contact.” *Id.* (citing Ex. 2006 ¶ 63).

Petitioner responds by referencing our Institution Decision, which found that the claim precluded “*physical* contact,” not electrical contact. Pet. Reply 12 (citing Inst. Dec. 23). Moreover, as Petitioner points out, the Institution Decision specifically notified Patent Owner “to submit ‘sufficient evidence of record to support its position and persuasively rebut Petitioner’s evidence of record’ if its position is that the alleged electrical connection prevents the formation of the required capacitance.” *Id.* at 12–13 (quoting Inst. Dec. 24). Further, Petitioner cites the Berg Declaration for additional support that Yu does not teach “physical contact” between the “cascaded transistors having a source/drain junction” and the “buried oxide layer.” *Id.* at 13 (citing Ex. 2006 ¶¶ 59, 63 (“as expressly stated by *Yu*, ‘doped region 100 is coupled to the second well 44’ and, therefore, doped region 100 (the N+ well) *does* electrically contact the buried oxide layer, even if there is no physical contact.” (citing Ex. 1005, 5:51))).

Paragraph 59 of the Berg Declaration is cited to support Petitioner’s position on “physical contact.” Pet. Reply 13. Paragraph 59 asserts that “due to the presence of N-well 44, ‘transistor 65 does not have a source/drain junction capacitance *even though neither the source, nor the drain, contacts the buried oxide layer.*’” *Id.* (quoting Ex. 2006 ¶ 59) (emphasis added). As to the portion of paragraph 59 asserting there is not

capacitance, Petitioner's response is based in part on a second annotation of Yu's Figure 9 reproduced below.



Id. at 14. Using the second annotation of Figure 9 above, Petitioner argues

Moreover, as Dr. Thompson explains, Mr. Berg's assertion is incorrect. Yu's n⁺ doped region 100 is partially formed on p-well 42 and partially within n-well 44. Yu, 5:9–10. The portion of the n⁺ doped region overlapping p-well 42 (circled [above] using a dashed red line) forms a pn junction, which under operating conditions generates a depletion region and consequently a junction capacitance across the depletion region.

Id. (citing Ex. 1026 ¶¶ 5–9; Ex. 1011,¹⁰ 10, 11; Ex. 1010, 43, 45).

In addition to precluding contact with the buried oxide layer by the cascaded transistors, claim 1 additionally requires formation of “a source/drain junction capacitance.” In the Institution Decision, we recognized that “Patent Owner's position may be that the alleged electrical

¹⁰ John P. Uyemura, *CMOS Logic Circuit Design*, copyright 2001, 2002.

connection in Yu prevents the capacitance from being formed, notwithstanding the physical disconnection.” Inst. Dec. 24. Patent Owner argues that this was our finding. PO Sur-reply 11. This is incorrect as we specifically stated the preceding recognition was only based on attorney argument, not evidence of record. Inst. Dec. 24. Regardless, Patent Owner argues that even were Yu to teach electrical contact, which we disagree with, such contact “prevents a capacitance from being formed and prevents *Yu* from anticipating Claim 1.”

The capacitance argument was explained at the hearing where Patent Owner asserted that “a mere lack of contact is not enough when the claim expressly requires a lack of physical contact and a source/drain junction capacitance, thereby forming a source/drain junction capacitance.”

Tr. 29:24–30:2. Patent Owner acknowledged that the Thompson Supplemental Declaration supports the presence of “a tiny little bit of capacitance.” *Id.* at 29:21–23, 30:9–11 (as to Thompson Supplemental Declaration stating “there’s a tiny little bit of capacitance in that dotted circle, is incomplete and unsupported.”).

Claim 1 requires the source/drain junction not to contact the buried oxide layer. As we determined in the Institution Decision,

the ’886 patent indicates that the contact precluded is *physical* contact, which provides the beneficial features. For example, the ’886 patent states that prior art sources and drains “typically extend all the way through device layer [] and contact the top surface of [the] buried oxide layer,” which leads to “no, or almost no, capacitive load.” Ex. 1001, 3:15–21. The configuration taught in the ’886 patent, in contrast, “do[es] not extend all the way through device layer 202 to contact the top surface of the buried oxide layer 204,” providing “an associated junction capacitance.” *Id.* at 4:8–18. Accordingly, the “source/drain junction capacitance” that is “thereby formed” in claim 1 appears

to be due to the fact that the “source/drain junction [] does not contact said buried oxide layer.” *Id.* at 9:1–4.

Inst. Dec. 23–24 (alterations in original). Despite our invitation to do so, Patent Owner has not provided any evidence or persuasive argument that what is claimed is “electrical contact.”

Upon the development of a full record after trial, we are not persuaded that the alleged electrical connection in Yu prevents the capacitance from being formed, notwithstanding the physical disconnection. Indeed, as recognized by Patent Owner and further based on the Thompson Supplemental Declaration, electrical contact would result in some capacitance. *See* Tr. 30:24 (“All we have is the supplemental expert declaration to go on.”). Patent Owner did not move to strike the Thompson Supplemental Declaration and did not depose Dr. Thompson on the Supplemental Declaration. Rather, Patent Owner argues that we should give no weight to the Supplemental Declaration. *Id.* at 31:16–17.

We give the Thompson Supplemental Declaration weight. It is supported by additional evidence, including Exhibits 1010 and 1011. *See* Ex. 1026 ¶¶ 5–9. For example, Uyemura explains a pn junction “formed by the drain-bulk and source-bulk interfaces in a MOSFET introduce a component of leakage current that is often important in high-performance circuit design.” Ex. 1011, 10¹¹. Conversely, Patent Owner has not provided sufficient evidence of record to support its position and persuasively rebut Petitioner’s evidence of record. Accordingly, Patent Owner’s argument is unpersuasive on this record.

¹¹ Pagination is what Petitioner provides not the actual page of the reference.

2. Conclusion Ground 4

Patent Owner does not argue any other reason that Ground 4 has not been sufficiently shown. Based on the full record, we determine that Yu discloses each and every limitation of claim 3. We thus determine that Petitioner has established a preponderance of the evidence that claim 3 would have been anticipated by Yu.

G. Obviousness of Claims 3 and 8–19 over Burgener and Okashita (Ground 5)

Petitioner asserts that remaining claims 3 and 8–19 would have been obvious in view of Burgener and Okashita. Pet. 57–83. Patent Owner’s arguments focus on whether there was a motive to “build Burgener’s Antenna Switch Using the Technology of Okashita.” PO Resp. 27–34.

In addition, Patent Owner argues that Burgener and Okashita do not teach claim 3 as discussed above. PO Resp. 34–35. Patent Owner bases this argument on Ground 2 analyzed above. *Id.* at 34. We addressed this issue above. *See* Section II.D above.

At a high level, Petitioner’s ground takes Burgener’s integrated circuit and proposes to manufacture it using the techniques described in Okashita. *See* Pet. 60 (“Instead of using a conventional [silicon-on-insulator] structure [as taught in Burgener], a [person of ordinary skill in the art] would have been motivated to add an intervening silicon layer between the source/drain junction and the buried oxide layer, as Okashita discloses.”).

We will briefly discuss Burgener before providing our analysis of the issue raised by Patent Owner.

1. *Burgener (Exhibit 1006)*

Figure 17 of Burgener is reproduced below:

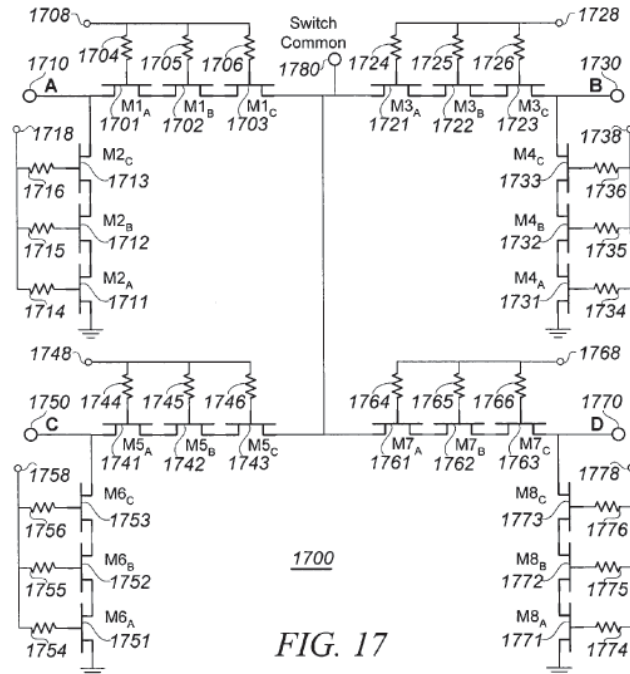


FIG. 17

Ex. 1006, Fig. 17. Figure 17 is a schematic diagram of antenna switch 1700. *Id.* ¶ 101. The antenna switch is shown as having four components labeled A, B, C, D, each connected to switch common 1780. As explained in Burgener, RF port A (1710) has “+” control node 1708 and “-” control node 1718, which turn on and off transistor stacks 1701–1703 and 1711–1713. *Id.* ¶¶ 101–104. Each of the ports is connected to either a receive or a transmit element of a dual-band transceiver. *Id.* ¶¶ 89, 91; *see also id.* at Fig. 12 (showing antenna switch 1700 in context). Burgener explains that “fabrication details are not provided” but that “preferred embodiments . . . may be fabricated in accordance with ultrathin silicon on sapphire processing” or that “other semiconductor-on-insulator . . . techniques may be used.” *Id.* ¶ 105.

2. Motivation to Combine Burgener and Okashita

Petitioner asserts that it would have been obvious to a person of ordinary skill in the art to fabricate Burgener’s antenna switch using the principles taught in Okashita—namely, the isolating trenches and an intervening silicon layer between the source/drain junctions and the buried silicon oxide layer. Pet. 60. Petitioner asserts that a person of ordinary skill in the art would have had a reason to take advantage of Okashita’s design: (1) to “reduce the operating temperature of the transistors,” which will “enhance their performance and reliability,” (2) to “prevent leakage of radio frequency signals,” and (3) to “minimize the effect of mismatch.” *Id.* at 60–63.

Patent Owner’s first argument is that a person of ordinary skill in the art would not look to Okashita because Okashita’s “configuration increases source/drain capacitance and, therefore, would create a slower switching circuit.” PO Resp. 29. Citing the Berg Declaration, Patent Owner argues this capacitance would cause unfavorable “performance issues.” *Id.* (citing Ex. 2006 ¶ 66). According to Patent Owner, Burgener teaches how to fabricate a RF switch so that a person of ordinary skill in the art would not need to look to Okashita. *Id.* at 30. Further, Burgener II,¹² cited in Burgener, teaches an “‘Ultra-Thin-Silicon (‘UTSi’) substrate’ wherein ‘the transistors used to implement the inventive RF switch are formed in an extremely thin layer of silicon in an insulating sapphire wafer.’” *Id.* at 30 (citing Ex. 2004, 7:39–50). Relying on the Berg Declaration, Patent Owner argues that a person of ordinary skill in the art “if anything, would have been

¹² Burgener et al., US 6,804,502 B2, issued October 12, 2004. Ex. 2004.

motivated to use the silicon-on-sapphire [SOS] technology disclosed in *Burgener II* to fabricate the antenna switch disclosed in *Burgener*, rather than be motivated to look to what Dr. Thompson admits is a higher capacitance and therefore slower technology disclosed in *Okashita*.” *Id.* at 31 (citing Ex. 2006 ¶ 68).

Patent Owner also argues “*Burgener* states in a separate section that ‘[o]ther semiconductor-on-insulator (SOI) techniques may be used to fabricate a dual-band transceiver integrated circuit as described above, for at least some frequency bands and power levels.’” PO Resp. 31 (citing Ex. 1006 ¶ 105) (alteration in original). Relying on the Berg Declaration, Patent Owner asserts that “this does not provide motivation to the [person of ordinary skill in the art] to look to *Okashita*.” *Id.* (citing Ex. 2006 ¶ 69). Further, Patent Owner argues that a person of ordinary skill in the art would not have had a reasonable expectation of success in adopting the *Okashita* design because of the relatively thick SOI technology and its associated high capacitance as compared to thin UTSi technology. *Id.* at 32 (citing Ex. 2006 ¶ 72).

As to the three reasons for taking advantage of *Okashita*’s design, Patent Owner argues that the first reason, heat considerations, is not an issue with *Burgener*. PO Resp. 32 (citing Ex. 2006 ¶ 71). As to reason two, prevention of leakage of radio frequency signals, *Burgener II* is cited by Patent Owner as enhancing performance characteristics and “reducing the deleterious substrate coupling effects associated with non-insulating and partially insulating substrates.” *Id.* at 33 (citing Ex. 2004, 7:39–64). As a result, Patent Owner argues that there is no motivation to look to *Okashita*. *Id.* As to the third reason, “minimize the effect of mismatch,” Patent Owner

argues that this is a hindsight reason based on claims 2, 14, and 17 of the '886 patent. *Id.* at 34 (citing Ex. 2006 ¶ 73).

Petitioner responds that the arguments reflect preferences and do not militate against its obviousness showing. Pet. Reply 17–18 (citing Inst. Dec. 26–27). Further, Petitioner contends that the thickness of the silicon wafer is not disclosed in Okashita and the patent drawings are not “precise proportions of the elements” where the specification is silent. *Id.* at 18 (citing *Hockerson-Halberstadt, Inc. v. Avia Grp. Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000)). Thus, Petitioner argues, the conclusion Patent Owner draws about Okashita’s silicon wafer is unsupported.

As to Patent Owner’s contention that Okashita would increase capacitance and create a slower switching circuit, Petitioner alleges that the Berg Declaration is unsupported. Pet. Reply 19. Further, the Thompson Declaration and Supplemental Declaration “shows junction capacitance in a transistor similar to Okashita’s transistor decreases as junction voltage increases, suggesting that a [person of ordinary skill in the art] would be aware of techniques to mitigate any negative effects from increased junction capacitance.” *Id.* (citing Ex. 1002 ¶ 48; Ex. 1026 ¶¶ 10–16). We find the Thompson testimony more credible because his opinions have more evidentiary support. *Id.* at 20 (citing *Rohm and Haas Co. v. Brotech Corp.*, 127 F.3d 1089, 1092 (Fed. Cir. 1997). *See also* 37 C.F.R. § 42.65(a).

The Berg Declaration testimony states that Burgener does not “dissipate additional heat in the transistors” and is not a motivation to combine Okashita and Burgener. Ex. 2006 ¶ 71. Petitioner asserts that the conclusion in the Berg Declaration is unsupported. Pet. Reply 20–22 (citing Ex. 1002 ¶¶ 213–214 (citing Ex. 2006 ¶ 71). Petitioner also argues:

In contrast, Dr. Thompson's opinion is grounded in well-established physical principles and supported by evidence. Silicon has a thermal conductivity roughly 100 times greater than silicon dioxide. Ex. 1013, 27–28; Thompson, ¶ 51. As Dr. Thompson explained, inserting a silicon layer between the source/drain junctions and the buried oxide layer improves heat dissipation, which helps lower transistor operating temperatures and enhances reliability. [Ex. 1002] ¶¶ 51, 214; [Ex. 1026] ¶ 19.

Pet. 21–22. As above, we find the Thompson testimony more credible because the opinions have more evidentiary support and are otherwise reasonable conclusions based on the evidence.

We agree with Petitioner's position regarding the SOS UTSi technology. Pet. Reply 22–26; *see* Ex. 1026 ¶ 22 (SOS).

In sum, Patent Owner's arguments against the combinability of Burgener and Okashita are not persuasive on this record.

3. Conclusion Ground 5

Patent Owner does not argue any other reason that Ground 5 has not been sufficiently shown. Based on the full record, we determine that Okashita and Burgener teach or suggest all the limitations of claims 3 and 8–19, and that one of ordinary skill in the art would have combined the references in the manner asserted with a reasonable expectation of success. We thus determine that Petitioner has established a preponderance of the evidence that claims 3 and 8–19 would have been obvious over Okashita and Burgener.

*H. Obviousness of Claims 3 and 8–19 over Burgener, Okashita, and Yu
(Ground 6)*

Petitioner asserts that remaining claims 3 and 8–19 would have been obvious in view of Burgener, Okashita, and Yu. Pet. 83–86. Patent Owner relies on its positions asserted above in Ground 5. PO Resp. 35.

For the reasons stated in our analysis of Ground 5 we determine that Petitioner has established a preponderance of the evidence that claims 3 and 8–19 would have been obvious over Burgener, Okashita and Yu.

III. CONCLUSION¹³

Weighing the competing evidence and testimony, we determine that Petitioner establishes by a preponderance of the evidence that the remaining Challenged Claims of the '886 patent are unpatentable.

¹³ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

In summary:

Remaining Claim(s) Challenged¹⁴	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
3	103	Okashita	3	
3	103	Okashita, Yu	3	
3	102	Yu	3	
3, 8–19	103	Burgener, Okashita	3, 8–19	
3, 8–19	103	Burgener, Okashita, Yu	3, 8–19	
Overall Outcome			3, 8–19	

¹⁴ Ground 1 challenging claims 1, 2, 4 and 5 as anticipated by Okashita was not reached because Patent Owner cancelled claims 1–2 and 4–7 in its unopposed Motion to Amend. Similarly, to the extent those claims were asserted in the grounds below they are removed.

IV. ORDER

For the foregoing reasons,

ORDERED that Patent Owner's Unopposed Motion to Amend (Paper 19) is granted, and claims 1, 2, and 4–7 are canceled;

FURTHER ORDERED that Petitioner has shown by a preponderance of the evidence that claims 3 and 8–19 are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2024-01402
Patent 7,745,886 B2

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CERTIFICATE OF SERVICE

A copy of Patent Owner's Notice of Appeal is being served via email on Petitioner's attorneys of record on the 26th day of May, 2026, the same day as the filing of the above-identified document in the United States Patent and Trademark Office/Patent Trial and Appeal Board, by serving Petitioner's correspondence address of record with the USPTO as follows:

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