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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/724,916	03/16/2007	Kevin Q. Yin	

22888
BEVER HOFFMAN & HARMS, LLP
39500 Stevenson Place
Suite 209
Fremont, CA 94539

CONFIRMATION NO. 4749
POA ACCEPTANCE LETTER



Date Mailed: 08/26/2016

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/18/2016.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/rmtturner myles/



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/724,916	03/16/2007	Kevin Q. Yin	

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

CONFIRMATION NO. 4749
POWER OF ATTORNEY NOTICE



OC000000085362236

Date Mailed: 08/26/2016

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/18/2016.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/rmtturner myles/

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fax to:
571-273-6500

- OR -

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below:** If you have a Customer Number to represent the fee address. **When to check the second box below:** If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☒ Customer Number: 22888

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
7,772,673	11/724,916

Completed by (check one):

☐ Applicant/Inventor	/E. Eric Hoffman/ Signature
☒ Attorney or Agent of record 38186 (Reg. No.)	E. Eric Hoffman Typed or printed name
☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)	(925) 895-3545 Requester's telephone number
☐ Assignee recorded at Reel Frame 	August 18, 2016 Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below".

☐ * Total of forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND COMPLETE D FORMS TO THIS ADDRESS. **SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	26687212
Application Number:	11724916
International Application Number:	
Confirmation Number:	4749
Title of Invention:	DEEP TRENCH ISOLATION AND METHOD FOR FORMING SAME
First Named Inventor/Applicant Name:	Kevin Q. Yin
Customer Number:	25700
Filer:	Edward Eric Hoffman/Carrie Reddick
Filer Authorized By:	Edward Eric Hoffman
Attorney Docket Number:	0150150
Receipt Date:	18-AUG-2016
Filing Date:	16-MAR-2007
Time Stamp:	21:14:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		TSJ-0150150-PTO-CHG-Adrs- POA-MF-CHG-Adrs-FILED.pdf	543129 4fb335e8e85beec2e1dce6a2015f890bba1435da0	yes	3

Multipart Description/PDF files in .zip description			
Document Description		Start	End
Change of Address		1	1
Power of Attorney		2	2
Maintenance Fee Address Change		3	3

Warnings:

Information:

Total Files Size (in bytes):	543129
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☒

Practitioners associated with Customer Number:

22888

OR

☐

Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number

Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☒

The address associated with Customer Number:

22888

OR

☐	Firm or Individual Name			
	Address			
	City	State	Zip	
	Country			
	Telephone	Email		

Assignee Name and Address: Newport Fab, LLC
4321 Jamboree Road
Newport Beach, CA 92660

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	<i>Ronit Vardi</i>	Date	1/11/2016
Name	Ronit Vardi	Telephone	(949) 435-8000
Title	Chief Financial Officer		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

CHANGE OF CORRESPONDENCE ADDRESS <i>Patent</i> Address to: Mail Stop Post Issue Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450	Patent Number	7,772,673
	Issue Date	2010-08-10
	Application Number	11/724,916
	Filing Date	2007-03-16
	First Named Inventor	Kevin Q. Yin
	Attorney Docket Number	TSJ-0150150

Please change the Correspondence Address for the above-identified patent to:

☒ The address associated with Customer Number: 22888

OR

☐ Firm or Individual Name

Address

City	State	ZIP
Country		
Telephone	Email	

This form cannot be used to change the data associated with a Customer Number. To change the data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB/124).

This form will not affect any "fee address" provided for the above-identified patent. To change a "fee address" use the "Fee Address Indication Form" (PTO/SB/47).

I am the:

☐ Patentee.

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☒ Attorney or agent of record. Registration Number 38186.

Signature /E. Eric Hoffman/

Typed or Printed Name E. Eric Hoffman

Date August 18, 2016

Telephone (925) 895-3545

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Post Issue, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/724,916	08/10/2010	7772673	0150150	4749

25700 7590 07/21/2010
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 469 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Kevin Q. Yin, Irvine, CA;
Amol Kalburge, Irvine, CA;
David J. Howard, Irvine, CA;
Arjun Kar-Roy, Irvine, CA;
Dieter Dornisch, Carlsbad, CA;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25700 7590 03/26/2010
 FARJAMI & FARJAMI LLP
 26522 LA ALAMEDA AVENUE, SUITE 360
 MISSION VIEJO, CA 92691



Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Christina Carter Ellis (Depositor's name)
 Christina Carter Ellis (Signature)
 June 18, 2010 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/724,916	03/16/2007	Kevin Q. Yin	0150150	4749

TITLE OF INVENTION: DEEP TRENCH ISOLATION AND METHOD FOR FORMING SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$0	\$0	\$1510	06/28/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHEN, JACK S J	2893	438-427000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Farjami & Farjami LLP

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Newport Fab, LLC dba Jazz Semiconductor

(B) RESIDENCE: (CITY AND STATE OR COUNTRY)

Newport Beach, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☒ Advance Order - # of Copies 2

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-0731 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature Michael Farjami
 Typed or printed name Michael Farjami

Date June 18, 2010
 Registration No. 38,135

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

06/21/2010 EEX00026 11724916
 1510.00 0P
 01 FC:1501
 02 FC:8001



FARJAMI & FARJAMI LLP
AN INTELLECTUAL PROPERTY LAW FIRM

www.farjami.com



26522 La Alameda Avenue, Suite 360
Mission Viejo, California 92691
tel: (949) 282-1000
fax: (949) 282-1002

FACSIMILE TRANSMISSION COVER SHEET

Date: June 18, 2010
To: United States Patent and Trademark Office
Examiner: Chen, Jack S J; Art Unit: 2893
Fax: (571) 273-2885
Re: **Application Serial No.: 11/724,916**
Filing Date: 3/16/2007; First-Named Inventor: Yin
Attorney Docket No.: 0150150
From: Farjami & Farjami LLP

Number of pages including the cover sheet: 5

Message:

Enclosed please find the Issue Fee and Fee for Two Copies of the Issued Patent.

Payment for Issue Fee in the Amount of \$1,516.00 is hereby enclosed on Form PTO-2038.

Thank you.

The documents accompanying this facsimile contain PRIVILEGED AND CONFIDENTIAL information intended only for use of the individual or entity named above. If you are not the intended recipient, disclosure, copying, distribution or use of the contents of this facsimile information is prohibited. If you have received this facsimile in error, please immediately notify us by telephone and return the original facsimile to us at the above address via U.S. Postal Service. We will reimburse you for all expenses incurred.



Attorney Docket No.: 0150150

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): **Yin, et al.**

Application Serial No.: **11/724,916**

Filed: **March 16, 2007**

Title: **Deep Trench Isolation and Method for Forming Same**

Group Art Unit: **2893**

Examiner: **Chen, Jack S J**

Notice of Allowance: **March 26, 2010**

ISSUE FEE AND FEE FOR TWO COPIES OF THE ISSUED PATENT

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

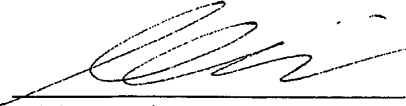
Enclosed, please find the completed "Issue Fee Transmittal" form and a "Payment by Credit Card" form (PTO-2038) in the amount of \$1,516.00 to cover the issue fee and fee for two (2) copies of the issued patent. The drawings filed in the present application have been accepted as formal drawings by the Examiner.

Attorney Docket No.: 0150150

An early issuance of the present application is respectfully requested.

Respectfully Submitted;
FARJAMI & FARJAMI LLP

Dated: 6/18/10


Michael Farjami, Esq.
Reg. No. 38,135
FARJAMI & FARJAMI LLP
Attorneys for Applicant

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Tel: (949) 282-1000
Fax: (949) 282-1002

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed: Mail Stop Issue Fee, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450, or being facsimile transmitted to the USPTO at (571) 273-2885, on the date indicated below.

Date: 6/18/10

Christina Carter Ellis
Name of Person Mailing or Transmitting Paper and/or Fee

Christina Carter Ellis
Signature



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

25700 7590 03/26/2010
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER	
CHEN, JACK S J	
ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 03/26/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/724,916	03/16/2007	Kevin Q. Yin	0150150	4749

TITLE OF INVENTION: DEEP TRENCH ISOLATION AND METHOD FOR FORMING SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$0	\$0	\$1510	06/28/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25700 7590 03/26/2010

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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11/724,916 03/16/2007 Kevin Q. Yin 0150150 4749

TITLE OF INVENTION: DEEP TRENCH ISOLATION AND METHOD FOR FORMING SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional NO \$1510 \$0 \$0 \$1510 06/28/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
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CHEN, JACK S J 2893 438-427000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/724,916	03/16/2007	Kevin Q. Yin	0150150	4749
25700	7590	03/26/2010		
FARJAMI & FARJAMI LLP 26522 LA ALAMEDA AVENUE, SUITE 360 MISSION VIEJO, CA 92691				
			EXAMINER CHEN, JACK S J	
			ART UNIT	PAPER NUMBER
			2893	
DATE MAILED: 03/26/2010				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 332 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 332 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	11/724,916	YIN ET AL.	
	Examiner	Art Unit	
	Jack Chen	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 7/23/09.
2. ☒ The allowed claim(s) is/are 1-9 and 21-28.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date ____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413), Paper No./Mail Date ____. 7. ☐ Examiner's Amendment/Comment 8. ☒ Examiner's Statement of Reasons for Allowance 9. ☐ Other ____.
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DETAILED ACTION

Reasons For Allowance

2. Claims 1-9 and 21-28 are allowable over the prior art of record.
3. The following is an examiner's statement of reasons for allowance: Applicants' arguments have been considered in view of amended claims 1, 21 and subsequent to an updated search of relevant prior art, are persuasive. This application is therefore allowed for reasons deemed to be of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (8:00am-4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne N. Monbleau can be reached on (571)272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2893

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jack Chen
Primary Examiner
Art Unit 2893

/Jack Chen/
Primary Examiner, Art Unit 2893

EAST Search History

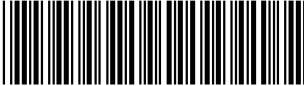
EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	5	("6107161"). URPN.	USPAT	OR	OFF	2010/03/24 10:02
L4	1401	(257/506).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/24 10:06
L5	256	(257/509).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/24 10:07
L6	1194	(257/510).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/24 10:07
L7	166	(257/511).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/24 10:07
L8	294	(257/517).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/24 10:08
L9	178	(257/518).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/24 10:08
L10	322	(257/520).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/24 10:08
L11	16	("5683075"). URPN.	USPAT	OR	OFF	2010/03/24 10:14
L12	29528	chamfer\$4 near2 (corner\$1 or edge \$1 or edging\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/24 10:25
L13	1235	deep adj trench adj isolation	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/24 10:25
L14	1	12 and 13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/24 10:25

L15	18827	chamfer\$4 near2 (side\$1 or spot\$1 or area\$1 or angle \$1 or place\$1 or border\$1 or boundar\$3 or perimeter\$1 or peripher\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/24 10:26
L16	54486	trench\$2 near2 isolat\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/24 10:26
L17	15	15 and 16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/03/24 10:27
L18	185	(257/e27.001). CCLS.	US-PGPUB; USPAT	OR	OFF	2010/03/24 10:50

3/ 24/ 10 10:50:55 AM

C:\ Documents and Settings\ jchen1\ My Documents\ EAST\ workspaces\ 11724916.wsp

<i>Index of Claims</i> 	Application/Control No. 11724916	Applicant(s)/Patent Under Reexamination YIN ET AL.
	Examiner Jack Chen	Art Unit 2893

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant										☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE													
Final	Original	12/17/2008	04/12/2009	03/24/2010											
1	1	÷	✓	=											
2	2	÷	✓	=											
3	3	÷	✓	=											
4	4	÷	✓	=											
5	5	÷	✓	=											
6	6	÷	✓	=											
7	7	÷	✓	=											
8	8	÷	✓	=											
9	9	÷	✓	=											
	10	÷	-	-											
	11	÷	-	-											
	12	÷	-	-											
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	20	÷	-	-											
10	21		✓	=											
11	22		✓	=											
12	23		✓	=											
13	24		✓	=											
14	25		✓	=											
15	26		✓	=											
16	27		✓	=											
17	28		✓	=											

Issue Classification 	Application/Control No. 11724916	Applicant(s)/Patent Under Reexamination YIN ET AL.
	Examiner Jack Chen	Art Unit 2893

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
257		510				H	0	1	L	21 / 04 (2006.01.01)								
CROSS REFERENCE(S)																		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	
257	520	E27.001																

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		17												
2	2		18												
3	3		19												
4	4		20												
5	5	10	21												
6	6	11	22												
7	7	12	23												
8	8	13	24												
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	10	15	26												
	11	16	27												
	12	17	28												
	13														
	14														
	15														
	16														

NONE		Total Claims Allowed:	
		17	
(Assistant Examiner)	(Date)		
/Jack Chen/ Primary Examiner.Art Unit 2893	3/24/10	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Search Notes 	Application/Control No. 11724916	Applicant(s)/Patent Under Reexamination YIN ET AL.
	Examiner Jack Chen	Art Unit 2893

SEARCHED			
Class	Subclass	Date	Examiner
257	510, 520, e27.001	3/24/10	jc

SEARCH NOTES		
Search Notes	Date	Examiner
east	4/12/09	jc
east updated	3/24/10	jc

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
all	of above	3/24/10	jc

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Attorney Docket No.: 0150150

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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JUL 23 2009

In re Application of: Yin, et al.

Art Unit: 2893

Serial No.: 11/724,916

Examiner: Chen, Jack S. J.

Filed: 03/16/2007

For: **Deep Trench Isolation and Method for
Forming Same**

AMENDMENT AND RESPONSE TO NON-FINAL OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the Non-Final Office Action dated April 16, 2009 in the above-referenced patent application. Please enter and consider the following amendments and remarks.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Page 1 of 14

051AZ0003J

In the Claims:

Claim 1 (currently amended): A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;

wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer ~~filling~~ within said trench.

Claim 2 (original): The semiconductor die of claim 1, wherein a trench corner width at said at least one trench chamfered corner is less than a trench side width along said plurality of sides.

Claim 3 (currently amended): The semiconductor die of claim 1, wherein said at least one trench chamfered corner comprises a portion of said trench situated ~~is formed~~ between a chamfered corner of an outside wall of said trench and a corner of an inside wall of said trench.

Claim 4 (original): The semiconductor die of claim 1, wherein a field oxide region overlies said trench.

Claim 5 (currently amended): The semiconductor die of claim 1, wherein said trench further comprises an oxide liner situated on an inside wall ~~walls~~ and an outside wall ~~walls~~ of said trench.

Claim 6 (original): The semiconductor die of claim 2, wherein said trench side width along said plurality of sides is approximately 1.0 micron.

Claim 7 (original): The semiconductor die of claim 1, wherein said semiconductor die is enclosed in a semiconductor package.

Claim 8 (original): The semiconductor die of claim 1, wherein said electronic device is a bipolar transistor.

Claim 9 (original): The semiconductor die of claim 1, wherein said electronic device is a silicon-germanium bipolar transistor.

Claim 10-20 (canceled)

Claim 21 (currently amended): A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

at least one trench situated in a substrate of said semiconductor die, said at least one trench having four sides surrounding said electronic device, wherein a respective one of four trench chamfered corners connects each pair of said four sides;

each of said four trench chamfered corners causing a reduction in a thickness of a polysilicon layer ~~filling~~ within said at least one trench.

Claim 22 (previously presented): The semiconductor die of claim 21, wherein a trench corner width at each of said four trench chamfered corners is less than a trench side width along each of said four sides of said at least one trench.

Claim 23 (currently amended): The semiconductor die of claim 21, wherein said each of said four trench chamfered corners comprises a portion of said at least one trench situated ~~is formed~~ between a respective chamfered corner of an outside wall of said at least one trench and a corner of an inside wall of said at least one trench.

Claim 24 (previously presented): The semiconductor die of claim 21, wherein a field oxide region overlies said at least one trench.

Claim 25 (currently amended): The semiconductor die of claim 21, wherein said at least one trench further comprises an oxide liner situated on an inside wall ~~walls~~ and an outside wall ~~walls~~ of said at least one trench.

Claim 26 (previously presented): The semiconductor die of claim 21, wherein said semiconductor die is enclosed in a semiconductor package.

Claim 27 (previously presented): The semiconductor die of claim 21, wherein said electronic device is a bipolar transistor.

Claim 28 (previously presented): The semiconductor die of claim 21, wherein said electronic device is a silicon-germanium bipolar transistor.

REMARKS

Prior to the present amendment, claims 1-9 and 21-28 were pending in the present application. By this amendment, Applicants have amended claims 1, 3, 5, 21, 23, and 25. Thus, claims 1-9 and 21-28 remain in the present application. Reconsideration and allowance of pending claims 1-9 and 21-28 in view of the above amendments and the following remarks are requested.

A. **Rejection of Claims 1-9 and 21-28 under 35 USC §112, second paragraph**

The Examiner has rejected claims 1-9 and 21-28 under 35 USC §112, second paragraph. The Applicants have amended claims 1, 3, 5, 21, 23 and 25 and submit that the requirements of 35 USC §112, second paragraph, have been met.

B. **Rejection of Claims 1-3, 7-8, 21-23, and 26-27 under 35 U.S.C. §102(b)**

The Examiner has rejected claims 1-3, 7-8, 21-23, and 26-27 under 35 USC §102(b) as being anticipated by U.S. patent number 6,107,161 to Kitaguro et al. (hereinafter "Kitaguro"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by amended independent claims 1 and 21, is patentably distinguishable over Kitaguro.

The present invention, as defined by amended independent claim 1, is a semiconductor die including at least one deep trench isolation region for isolating an electronic device, where the at least one deep trench isolation region comprises a trench situated in a substrate of the semiconductor die, the trench including a plurality of sides surrounding the electronic device, and at least one trench chamfered corner formed between and connecting the plurality of sides, and where the at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within the trench. In an embodiment of the present invention as shown in Figure 2, for example, Structure 200, which can be a portion of a semiconductor die, includes deep trench isolation region 202 for isolating bipolar device 204. Deep trench isolation region 202 includes trench 208, which is situated in substrate 206 and has sides 228a, 228b, 228c, and 228d (hereinafter "sides 228a through 228d") surrounding bipolar device 204. Further shown in Figure 2, trench chamfered corners 240 are formed between and connecting sides 228a through 228d of trench 208. Trench chamfered corners 240 cause a reduction in the thickness of polysilicon filling 212.

As disclosed in the present application, the thickness of polysilicon filling 212 is significantly reduced by reducing trench corner width 230, which represents the perpendicular distance, i.e., the minimum distance, between chamfered edge 232 and each of corners 223 of inside wall 222 of trench 208. *See, e.g.,* page 11, lines 14-17 and Figure 2 of the present application.

In contrast to the present invention as defined by amended independent claim 1, Kitaguro does not disclose a semiconductor die including at least one deep trench isolation region for isolating an electronic device, where the at least one deep trench isolation region comprises a trench situated in a substrate of the semiconductor die, the trench including a plurality of sides surrounding the electronic device, and at least one trench chamfered corner formed between and connecting the plurality of sides, and where the at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within the trench. Kitaguro specifically discloses a semiconductor wafer 20 having a die 22 surrounded by four side walls 28. Side walls 28 are divided at scribing lines 24 and consist of cutting planes 30 being formed approximately flat by the cutting of a dicing saw and walls 32. Walls 32 are formed within cutting groves 26 and are connected by connecting parts 32a. *See, e.g.,* Figure 2 and related text of Kitaguro.

In the outstanding Office Action, the Examiner argues that connecting parts 32a are trench chamfered corners. However, connecting parts 32a of Kitaguro are not chamfered as required by amended independent claim 1, but are, conversely, rounded. Kitaguro significantly states: "In this embodiment, the connection parts 32a are formed in a circular arc shape." *See, e.g.,* Figure 2 and col. 5, lines 4-5 of Kitaguro.

Thus, Kitaguro fails to disclose a trench chamfered corner as specified by amended independent claim 1, where the trench chamfered corner causes a reduction in the thickness of a polysilicon layer within the trench. In Kitaguro, the circular arc shape of connection parts 32a causes an *increase* in the width of cutting groves 26 to protect

Attorney Docket No.: 0150150

connection parts 32a from the blade of a dicing saw rather than reducing the thickness of a material that may be situated within cutting groves 26 (*See* col. 6, lines 62-67 and col. 7, line 1 of Kitaguro reproduced below).

In other words, the walls 32 formed within the cutting groves 26 are located *further apart* from the scribing lines 24 in the vicinity of the intersections 34. So that, the blade of the dicing saw is never contacted with the connection parts 32a of the walls 32 formed within the cutting groves 26 in the vicinity of the intersections 34 of the scribing lines 24.

Thus, by requiring connection parts 32a to have a circular arc shape so as to cause an in the width of cutting groves 26 to protect connection parts 32a from the dicing saw, Kitaguro teaches away from the present invention as defined by amended independent claim 1.

Thus, at the time the invention defined by amended independent claim 1 was made, the invention would not have been made obvious to a person of ordinary skill in the art by Kitaguro. Thus, amended independent claim 1 is patentably distinguishable over Kitaguro. Thus, claims 2-3 and 7-8 depending from amended independent claim 1 are, *a fortiori*, also patentably distinguishable over Kitaguro for at least the above reasons and also for additional limitations contained in each dependent claim.

Amended independent claim 21 includes similar limitations as amended independent claim 1. Therefore, for reasons similar to those set forth above, amended independent claim 21 is also patentably distinguishable over Kitaguro. Thus, claims 22-23 and 26-27 depending from amended independent claim 21 are, *a fortiori*, also

Attorney Docket No.: 0150150

patentably distinguishable over Kitaguro for at least the above reasons and also for additional limitations contained in each dependent claim.

C. Rejection of Claims 6, 9, and 28 under 35 USC §103(a)

The Examiner has rejected claims 6, 9, and 28 under 35 USC § 103(a) as being unpatentable over Kitaguro. As discussed above, amended independent claims 1 and 21 are patentably distinguishable over Kitaguro. Thus, claims 6 and 9 depending from amended independent claim 1 and claim 28 depending from amended independent claim 21 are, *a fortiori*, also patentably distinguishable over Kitaguro for at least the above reasons and also for additional limitations contained in each dependent claim.

D. Rejection of Claims 1-9 and 21-28 under 35 USC §103(a)

The Examiner has rejected claims 1-9 and 21-28 under 35 U.S.C. § 103(a) as being unpatentable over alleged Applicants' "admitted prior art" in view of U.S. patent number 5,933,749 to Tzung-Han Lee (hereinafter "Lee"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by amended independent claims 1 and 21, is patentably distinguishable over Lee.

In contrast to the present invention as defined by amended independent claim 1, Lee does not disclose a semiconductor die including at least one deep trench isolation region for isolating an electronic device, where the at least one deep trench isolation region comprises a trench situated in a substrate of the semiconductor die, the trench

including a plurality of sides surrounding the electronic device, and at least one trench chamfered corner formed between and connecting the plurality of sides, and where the at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within the trench. Lee discloses trench 23 including right-angle top corner 25, where trench 23 is formed by etching substrate 20, oxide layer 21, and silicon nitride layer 22. *See, e.g.,* Figure 2c and related text of Lee. In Lee, right-angle top corner 25, exposed oxide layer 21, and substrate 20 are etched away to form grading corner 26 so as to avoid charge accumulation and leakage current. *See, e.g.,* Lee, Figures 2b and 2c, and related text.

In the outstanding Office Action, the Examiner argues that:

[T]he subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to form the trench having the chamfered corner as taught by Lee in the device of Applicant's admitted prior art in order to prevent leakage current and short circuit (col. 1, lines 54-56), etc. *See*, Examiner's comments on page 8 of the Office Action dated April 16, 2009.

However, Lee teaches that the charge accumulation and leakage current is caused by the 90 degree angle of the "after-etched top corner." *See, e.g.,* Figure 1b and related text, col. 1, lines 39-51, and col. 2, lines 24-28 of Lee.

Thus, Lee fails to disclose a trench chamfered corner as specified by amended independent claim 1, where the trench chamfered corner causes a reduction in the thickness of a polysilicon layer within the trench. As is apparent from Figures 2c and 2d of Lee, grading corner 26 cannot reduce the thickness of a material that may be situated within trench 23.

Attorney Docket No.: 0150150

For the foregoing reasons, Applicants respectfully submit that, at the time the invention defined by amended independent claim 1 was made, the invention would not have been made obvious to a person of ordinary skill in the art by Lee. Thus, amended independent claim 1 is patentably distinguishable over Lee. Thus, claims 2-9, depending from amended independent claim 1 are, *a fortiori*, also patentably distinguishable over Lee for at least the above reasons and also for additional limitations contained in each dependent claim.

Amended independent claim 21 includes similar limitations as amended independent claim 1. Therefore, for reasons similar to those set forth above, Applicants respectfully submit that at the time the invention defined by amended independent claim 21 was made, the invention would not have been made obvious to a person of ordinary skill in the art by Lee. Thus, claims 22-28 depending from amended independent claim 21 are, *a fortiori*, also patentably distinguishable over Lee for at least the above reasons and also for additional limitations contained in each dependent claim.

Page 12 of 14

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PAGE 16/18 * RCVD AT 7/23/2009 2:39:32 PM [Eastern Daylight Time] * SVR:USPTO-EFXXRF-6/4 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):07-04

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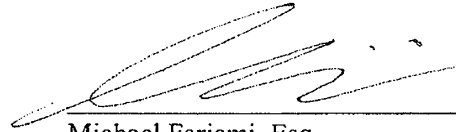
E. Conclusion

For all the foregoing reasons pending claims 1-9 and 21-28 are patentably distinguishable over the cited art, and an early allowance of pending claims 1-9 and 21-28 is respectfully requested.

Attorney Docket No.: 0150150

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 7/23/09



Michael Farjami, Esq.
Reg. No. 38,135

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Facsimile: (949) 282-1002

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FACSIMILE TRANSMISSION COVER SHEET

Date: July 23, 2009

To: United States Patent and Trademark Office
Examiner: Chen, Jack S. J. Art Unit: 2893

Fax: (571) 273-8300

Re: **Application Serial No.: 11/724,916**
Filing Date: 3/16/2007; First-Named Inventor: Yin
Attorney Docket No.: 0150150

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 18

Message:

Enclosed please find the Amendment and Response to Non-Final Office Action dated April 16, 2009.

Payment for First Month Extension Fee in the Amount of \$130.00 is hereby enclosed on Form PTO-2038.

Thank you.

The documents accompanying this facsimile contain PRIVILEGED AND CONFIDENTIAL information intended only for use of the individual or entity named above. If you are not the intended recipient, disclosure, copying, distribution or use of the contents of this facsimile information is prohibited. If you have received this facsimile in error, please immediately notify us by telephone and return the original facsimile to us at the above address via U.S. Postal Service. We will reimburse you for all expenses incurred.

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AMENDMENT COVER SHEET

IN RE APPLICATION OF: Yin, et al.SERIAL NO.: 11/724,916 FILED: 03/16/2007FOR: Deep Trench Isolation and Method for Forming Same

HONORABLE COMMISSIONER FOR PATENTS
P.O. Box 1450, Alexandria, VA 22313-1450

Sir/Madam:

Transmitted herewith is a paper in the above-identified application. Any necessary extension of time period set for this paper is hereby requested.

☐ No additional fee is required.☒ The fee has been calculated as shown below:☒ EXTENSION FEE

	RATE Non-Small Entity	RATE Small-Entity	FEE
FIRST MONTH AFTER TIME PERIOD SET	130.00	65.00	\$130.00
SECOND MONTH AFTER TIME PERIOD SET	490.00	245.00	\$
THIRD MONTH AFTER TIME PERIOD SET	1,110.00	555.00	\$
FOURTH MONTH AFTER TIME PERIOD SET	1,730.00	865.00	\$

☒ TOTAL EXTENSION FEE \$ 130.00☐ FEE FOR EXTRA CLAIMS added by Amendment in this response:

	Column 1	Column 2	Column 3			
	Number of Claims after Amendment	Number Previously Paid for	Number of Extra Claims	RATE Non-Small Entity	RATE Small Entity	FEE
TOTAL CLAIMS		MINUS **28	* = 0	x 52	x 26	\$
INDEPENDENT		MINUS ***3	* = 0	x 220	x 110	\$
First presentation of multiple dependent claim				+ 390	+ 195	\$

TOTAL FEE FOR EXTRA CLAIMS \$ 0.00

* If the entry in Column 1 is less than the entry of Column 2, write "0" in Column 3.

** If the number of Total Claims previously paid for is less than 20, write "20" in this space.

*** If the number of Independent Claims previously paid for is less than 3, write "3" in this space.

07/24/2009 MNGUYEN 00000019 11724916

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Attorney Docket No.: 0150150

- ☐ Total fee for Supplemental Information Disclosure Statement \$
- ☒ Enclosed is the total fee of \$ 130.00 (Payment by Credit Card, Form PTO-2038 Enclosed).
- ☐ Please charge Deposit Account No. 50-0731 in the amount of \$
- ☒ The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Date: 7/23/09

By: [Signature]
Michael Farjami, Reg. No. 38,135

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Date
Jembier Davalos
Signature
Jembier Davalos
Name of Person Performing Facsimile Transmission

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Facsimile: (949) 282-1002

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/724,916		Filing Date 03/16/2007		☐ To be Mailed	
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APPLICATION AS FILED – PART I						OTHER THAN SMALL ENTITY			
(Column 1)		(Column 2)		SMALL ENTITY ☐		OR		SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A		N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A		N/A		N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A		N/A		
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$	=	OR	X \$	=		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=	OR	X \$	=		
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL		TOTAL				

APPLICATION AS AMENDED – PART II						OTHER THAN SMALL ENTITY					
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR		SMALL ENTITY	
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)			
Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=	OR	X \$	=		
Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=	OR	X \$	=		
☐ Application Size Fee (37 CFR 1.16(s))											
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
						TOTAL ADD'L FEE		TOTAL ADD'L FEE			

(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR		SMALL ENTITY	
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)			
07/23/2009					X \$	=	OR	X \$	=		
Total (37 CFR 1.16(i))	* 17	Minus	** 20	= 0	X \$	=	OR	X \$52 =	0		
Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$	=	OR	X \$220 =	0		
☐ Application Size Fee (37 CFR 1.16(s))											
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
						TOTAL ADD'L FEE		TOTAL ADD'L FEE	0		

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Legal Instrument Examiner:
/DAVID SASFAI/



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/724,916	03/16/2007	Kevin Q. Yin	0150150	4749
25700 7590 04/16/2009 FARJAMI & FARJAMI LLP 26522 LA ALAMEDA AVENUE, SUITE 360 MISSION VIEJO, CA 92691			EXAMINER CHEN, JACK S J	
			ART UNIT 2893	PAPER NUMBER
			MAIL DATE 04/16/2009	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 11/724,916	Applicant(s) YIN ET AL.	
	Examiner Jack Chen	Art Unit 2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 15 January 2009.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-9 and 21-28 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-9, 21-28 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election of invention of Group I in the reply filed on 1/15/09 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).
2. Claims 10-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
4. Claims 1-9 and 21-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 1, the phrase "wherein said at least one trench chamfered corner *causes a reduction in a thickness of a polysilicon layer filling said trench*" does not positively recite the structure of the device. It is unclear (it appears it is an intend outcome) if the polysilicon layer is being formed or not.

Re claim 21, the phrase "each of said four trench chamfered corners *causing a reduction in a thickness of a polysilicon layer filling said at least one trench*" does not positively recite the structure of the device. It is unclear (it appears it is an intend outcome) if the polysilicon layer is being formed or not.

Re claims 3 and 23, it is unclear as to which portion(s) is considered as the chamfered corner of the outside wall of the trench and/or which portion(s) is considered as the corner of the inside wall of the trench

Re claims 5 and 25, the phrase “inside walls and outside walls of said trench” is unclear and indefinite since applicant has not defined the inside walls and/or outside walls of the trench.

The remaining claims are rejected for depending from the above rejected claims.

For the purpose of patentability, these claims will be interpreted as best understood.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 7-8, 21-23, 26-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Kitaguro et al., US/6,107,161.

Re claim 1, Kitaguro et al. disclose a semiconductor comprising: a trench 26 situated in a substrate of said semiconductor die 22 (figs. 1-2), said trench having a plurality of sides surrounding said electronic device 22 (fig. 2), and at least one trench chamfered corner 32a formed between and connecting said plurality of sides (fig. 2); wherein said at least one trench chamfered corner 32a (capable of performing the same function and/or having the same outcome if the polysilicon is formed) causes a reduction in a thickness of any subsequently formed material filling said trench (figs. 1-2; and/or examiner can also consider the instant claim does

Art Unit: 2893

not require the formation of polysilicon layer within the trench), see figs. 1-16 and cols. 1-8 for more details.

Re claim 2, wherein a trench corner width 32a (the arc portion) at said at least one trench chamfered corner 32a is less than a trench side width along said plurality of sides (fig. 2).

Re claim 3, wherein said at least one trench chamfered corner 32a is formed between a chamfered corner of an outside wall (i.e., the outside wall of the adjacent device) of said trench and a corner of an inside wall of said trench (fig. 2).

Re claim 7, inherently shows semiconductor die is enclosed in a semiconductor package for IC.

Re claim 8, wherein said electronic device is a bipolar transistor (i.e., NPN), see fig. 1.

Re claim 21, Kitaguro et al. disclose a semiconductor comprising at least one trench 26 situated in a substrate of said semiconductor die 22 (figs. 1-2), said at least one trench 26 having four sides surrounding said electronic device 22 (fig. 2), wherein a respective one of four trench chamfered corners 32a connects each pair of said four sides (fig. 2); each of said four trench chamfered corners (capable of performing the same function and/or having the same outcome if the polysilicon is formed) causing a reduction in a thickness of any subsequently formed material filling said at least one trench (figs. 1-2; and/or examiner can also consider the instant claim does not require the formation of polysilicon layer within the trench), see figs. 1-16 and cols. 1-8 for more details.

Re claim 22, wherein a trench corner width 32a (the arc portion) at each of said four trench chamfered corners 32a is less than a trench side width along each of said four sides of said at least one trench (fig. 2).

Re claim 23, wherein said each of said four trench chamfered corners 32a is formed between a respective chamfered corner of an outside wall (i.e., the outside wall of the adjacent device) of said at least one trench and a corner of an inside wall of said at least one trench (fig. 2).

Re claim 26, inherently shows semiconductor die is enclosed in a semiconductor package for IC.

Re claim 27, wherein said electronic device is a bipolar transistor (i.e., NPN), see fig. 1.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

Art Unit: 2893

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 6, 9 and 28 rejected under 35 U.S.C. 103(a) as being unpatentable over Kitaguro et al., US/6,107,161.

Kitaguro et al. disclosed in above; however, Kitaguro is silent to the width of the trench and the type of the device (silicon-germanium bipolar transistor).

The width of the trench is considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in *In re Aller*, the selection of reaction parameters such as temperature and concentration would have been obvious:

“Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed Acritical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.”

In re Aller 105 USPQ233, 255 (CCPA 1955). See also *In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmischer* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sola* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any width range suitable to device of Kitaguro et al. in order to optimize the device.

In addition, using silicon germanium for the bipolar transistor has been known in the semiconductor. The selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in *Sinclair & Carroll Co., Inc. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945). "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig - saw puzzle." 65 USPQ at 301.). and The substitution of a alternative art-recognized device structure (i.e., silicon-germanium bipolar transistor) is a mere substitution suitable for the intended use of Kitaguro et al. (MPEP §2144.07)

10. Claims 1-9 and 21-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Lee, US/5,933,749.

Applicant's admitted prior art discloses a semiconductor comprising: a trench 108 situated in a substrate of said semiconductor die 104 (fig 1), said trench having a plurality of sides surrounding said electronic device 104 (fig. 1), and at least one trench having a plurality of sides (fig. 1), See fig. 1 and pages 2-3 and 7-10 for more details.

Applicant's admitted prior art disclosed above; however, applicant's admitted prior art fails to show the trench having at least one trench chamfered corner formed between and connecting the plurality of sides.

Lee teaches a semiconductor device, which comprises a the trench 23 having at least one trench chamfered corner 26 (fig. 2C) formed between and connecting the plurality of sides, wherein said at least one trench chamfered corner 26 (capable of performing the same function and/or having the same outcome if the polysilicon is formed) causes a reduction in a thickness of any subsequently formed material filling said trench (fig. 2C; and/or examiner can also considers the instant claim does not require the formation of polysilicon layer within the trench); see figs. 1-2d and cols. 1-4 for more details.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to form the trench having the chamfered corner as taught by Lee in the device of Applicant's admitted prior art in order to prevent leakage current and short circuit (col. 1, lines 54-56), etc.

Re claims 2 and 22, Lee shows a trench corner width 26 at said at least one trench chamfered corner 26 is less than a trench side width along said plurality of sides (fig. 2C).

Re claims 3 and 23, Lee shows at least one trench chamfered corner 26 is formed between a chamfered corner of an outside wall (i.e., the outside wall of the adjacent device) of said trench and a corner of an inside wall of said trench (fig. 2C).

Re claims 4 and 24, Applicant's admitted prior art shows a field oxide region overlies the trench (page 7, lines 20-21).

Re claims 5 and 25, Applicant's admitted prior art shows the trench further comprises an oxide liner 110 (fig. 1) situated on inside walls and outside walls of said trench.

Re claims 7 and 26, Applicant's admitted prior art inherently shows semiconductor die is enclosed in a semiconductor package for IC.

Re claims 8 and 27, applicant's admitted prior art shows electronic device is a bipolar transistor (i.e., NPN), see fig. 1.

Re claims 6, 9 and 28; Lee and Applicant's admitted prior art disclosed in above; however, both of them are silent to the width of the trench and the type of the device (silicon-germanium bipolar transistor).

The width of the trench is considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in *In re Aller*, the selection of reaction parameters such as temperature and concentration would have been obvious:

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed Acritical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

In re Aller 105 USPQ233, 255 (CCPA 1955). See also *In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmischer* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sola* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any width range suitable to device of Applicant's admitted prior art taken with Lee in order to optimize the device.

In addition, using silicon germanium for the bipolar transistor has been known in the semiconductor. The selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in *Sinclair & Carroll Co., Inc. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945). "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig - saw puzzle." 65 USPQ at 301.). and The substitution of a alternative art-recognized device structure (i.e., silicon-germanium bipolar transistor) is a mere substitution suitable for the intended use of Kitaguro et al. (MPEP §2144.07).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (8:00am-4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne N. Monbleau can be reached on (571)272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2893

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jack Chen
Primary Examiner
Art Unit 2893

/Jack Chen/
Primary Examiner, Art Unit 2893

Notice of References Cited	Application/Control No. 11/724,916		Applicant(s)/Patent Under Reexamination YIN ET AL.	
	Examiner Jack Chen		Art Unit 2893	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,933,749	08-1999	Lee, Tzung-Han	438/435
*	B	US-6,107,161	08-2000	Kitaguro et al.	438/462
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims 	Application/Control No. 11724916	Applicant(s)/Patent Under Reexamination YIN ET AL.
	Examiner Jack Chen	Art Unit 2893

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	12/17/2008	04/12/2009						
	1	÷	✓						
	2	÷	✓						
	3	÷	✓						
	4	÷	✓						
	5	÷	✓						
	6	÷	✓						
	7	÷	✓						
	8	÷	✓						
	9	÷	✓						
	10	÷	-						
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	17	÷	-						
	18	÷	-						
	19	÷	-						
	20	÷	-						
	21		✓						
	22		✓						
	23		✓						
	24		✓						
	25		✓						
	26		✓						
	27		✓						
	28		✓						

Search Notes 	Application/Control No. 11724916	Applicant(s)/Patent Under Reexamination YIN ET AL.
	Examiner Jack Chen	Art Unit 2893

SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
east	4/12/09	jc

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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BIB DATA SHEET

CONFIRMATION NO. 4749

SERIAL NUMBER 11/724,916	FILING or 371(c) DATE 03/16/2007 RULE	CLASS 438	GROUP ART UNIT 2893	ATTORNEY DOCKET NO. 0150150		
APPLICANTS Kevin Q. Yin, Irvine, CA; Amol Kalburge, Irvine, CA; David J. Howard, Irvine, CA; Arjun Kar-Roy, Irvine, CA; Dieter Dornisch, Carlsbad, CA; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 04/13/2007						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/JACK S J CHEN/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 9	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 2
ADDRESS FARJAMI & FARJAMI LLP 26522 LA ALAMEDA AVENUE, SUITE 360 MISSION VIEJO, CA 92691 UNITED STATES						
TITLE Deep trench isolation and method for forming same						
FILING FEE RECEIVED 1000	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees		
				☐ 1.16 Fees (Filing)		
				☐ 1.17 Fees (Processing Ext. of time)		
				☐ 1.18 Fees (Issue)		
				☐ Other _____		
			☐ Credit			

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	27826	chamfer\$4 near2 (corner\$1 or edge \$1 or edging\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/12 14:34
L2	1089	deep adj trench adj isolation	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/12 14:35
L3	1	1 and 2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/12 14:35
L4	196850	bipolar\$1 or bi-polar \$1 or (bi adj polar \$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/12 14:37
L5	208	1 and 4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/12 14:37
L6	17368	chamfer\$4 near2 (side\$1 or spot\$1 or area\$1 or angle \$1 or place\$1 or border\$1 or boundar\$3 or perimeter\$1 or peripher\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/12 15:07
L7	48941	trench\$2 near2 isolat\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/12 15:08

L8	1	6 with 7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/12 15:08
L9	40096	1 or 6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/12 15:09
L10	5	9 with 7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/12 15:10
L11	8	9 same 7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/12 15:12
L12	9003	9 with (trench\$2 or hole\$1 or via\$1 or groov\$3 or opening \$1 or openning\$1 or recess\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/12 15:15
L13	17	12 and 7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/12 15:15
L14	16960	9 same (trench\$2 or hole\$1 or via\$1 or groov\$3 or opening\$1 or openning\$1 or recess\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/12 15:19
L15	25	14 and 7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/12 15:19

L16	5970	((438/110) or (438/113) or (438/196) or (438/207) or (438/318) or (438/353) or (438/354) or (438/355) or (438/359) or (438/361) or (438/424) or (438/427) or (438/430)).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2009/04/12 15:30
L17	33	16 and 9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/12 15:31
L18	1	("6107161").PN.	US-PGPUB; USPAT	OR	OFF	2009/04/12 16:29
L19	0	18 and 4	US-PGPUB; USPAT	OR	OFF	2009/04/12 16:30
L20	0	18 and (SiGe or (silicon adj germanium))	US-PGPUB; USPAT	OR	OFF	2009/04/12 16:31
L21	0	18 and package	US-PGPUB; USPAT	OR	OFF	2009/04/12 16:32

4/12/09 6:31:50 PM

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FACSIMILE TRANSMISSION COVER SHEET

Date: January 15, 2009

To: United States Patent and Trademark Office
Examiner: Chen, Jack S J; Art Unit: 2893

Fax: (571) 273-8300

Re: **Application Serial No.: 11/724,916**
Filing Date: 3/16/2007; First-Named Inventor: Yin
Attorney Docket No.: 0150150

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 9

Message:

Enclosed please find the Amendment and Response to Office Action dated December 18, 2008.

Thank you.

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AMENDMENT COVER SHEET

IN RE APPLICATION OF: Yin, et al.SERIAL NO.: 11/724,916 FILED: 03/16/2007FOR: Deep Trench Isolation and Method for Forming Same

HONORABLE COMMISSIONER FOR PATENTS
P.O. Box 1450, Alexandria, VA 22313-1450

Sir/Madam:

Transmitted herewith is a paper in the above-identified application. Any necessary extension of time period set for this paper is hereby requested.

- ☒ No additional fee is required.
☐ The fee has been calculated as shown below:

☐ EXTENSION FEE

	RATE Non-Small Entity	RATE Small-Entity	FEE
FIRST MONTH AFTER TIME PERIOD SET	130.00	65.00	\$
SECOND MONTH AFTER TIME PERIOD SET	490.00	245.00	\$
THIRD MONTH AFTER TIME PERIOD SET	1,110.00	555.00	\$
FOURTH MONTH AFTER TIME PERIOD SET	1,730.00	865.00	\$

- ☐ TOTAL EXTENSION FEE \$ 0.00
☐ FEE FOR EXTRA CLAIMS added by Amendment in this response:

	Column 1	Column 2	Column 3			
	Number of Claims after Amendment	Number Previously Paid for	Number of Extra Claims	RATE Non-Small Entity	RATE Small Entity	FEE
TOTAL CLAIMS	17	MINUS **20	* = 0	x 52	x 26	\$
INDEPENDENT	2	MINUS ***3	* = 0	x 220	x 110	\$
First presentation of multiple dependent claim				+ 390	+ 195	\$

TOTAL FEE FOR EXTRA CLAIMS \$ 0.00

- * If the entry in Column 1 is less than the entry of Column 2, write "0" in Column 3.
** If the number of Total Claims previously paid for is less than 20, write "20" in this space.
*** If the number of Independent Claims previously paid for is less than 3, write "3" in this space.

-1-

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- ☐ Total fee for Supplemental Information Disclosure Statement \$
- ☐ Enclosed is the total fee of \$0.00 (Payment by Credit Card, Form PTO-2038 Enclosed).
- ☐ Please charge Deposit Account No. 50-0731 in the amount of \$
- ☒ The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731. A duplicate copy of this sheet is enclosed.

Date:

1/15/09

By:

Michael Farjami, Reg. No. 38,135

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1/15/09

Signature

Marci M. Sweda

Name of Person Performing Facsimile Transmission

Michael Farjami, Esq.
Farjami & Farjami LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, CA 92691
Telephone: (949) 282-1000
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-2-

05JAZ0003J

Attorney Docket No.: 0150150

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re Application of: Yin, et al.

Art Unit: 2893

Serial No.: 11/724,916

Examiner: Chen, Jack S. J.

Filed: 03/16/2007

For: **Deep Trench Isolation and Method for
Forming Same**

AMENDMENT AND RESPONSE TO OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the Office Action dated December 18, 2008 in the
above-referenced patent application. Please enter and consider the following
amendments and remarks.

Page 1

05JAZ0003J

In the Claims:

Claim 1 (original): A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;

wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer filling said trench.

Claim 2 (original): The semiconductor die of claim 1, wherein a trench corner width at said at least one trench chamfered corner is less than a trench side width along said plurality of sides.

Claim 3 (original): The semiconductor die of claim 1, wherein said at least one trench chamfered corner is formed between a chamfered corner of an outside wall of said trench and a corner of an inside wall of said trench.

Claim 4 (original): The semiconductor die of claim 1, wherein a field oxide region overlies said trench.

Claim 5 (original): The semiconductor die of claim 1, wherein said trench further comprises an oxide liner situated on inside walls and outside walls of said trench.

Claim 6 (original): The semiconductor die of claim 2, wherein said trench side width along said plurality of sides is approximately 1.0 micron.

Claim 7 (original): The semiconductor die of claim 1, wherein said semiconductor die is enclosed in a semiconductor package.

Claim 8 (original): The semiconductor die of claim 1, wherein said electronic device is a bipolar transistor.

Claim 9 (original): The semiconductor die of claim 1, wherein said electronic device is a silicon-germanium bipolar transistor.

Claims 10-20 (canceled)

Claim 21 (new): A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

at least one trench situated in a substrate of said semiconductor die, said at least one trench having four sides surrounding said electronic device, wherein a respective one of four trench chamfered corners connects each pair of said four sides;

each of said four trench chamfered corners causing a reduction in a thickness of a polysilicon layer filling said at least one trench.

Claim 22 (new): The semiconductor die of claim 21, wherein a trench corner width at each of said four trench chamfered corners is less than a trench side width along each of said four sides of said at least one trench.

Claim 23 (new): The semiconductor die of claim 21, wherein said each of said four trench chamfered corners is formed between a respective chamfered corner of an outside wall of said at least one trench and a corner of an inside wall of said at least one trench.

Claim 24 (new): The semiconductor die of claim 21, wherein a field oxide region overlies said at least one trench.

Claim 25 (new): The semiconductor die of claim 21, wherein said at least one trench further comprises an oxide liner situated on inside walls and outside walls of said at least one trench.

Claim 26 (new): The semiconductor die of claim 21, wherein said semiconductor die is enclosed in a semiconductor package.

Claim 27 (new): The semiconductor die of claim 21, wherein said electronic device is a bipolar transistor.

Claim 28 (new): The semiconductor die of claim 21, wherein said electronic device is a silicon-germanium bipolar transistor.

Attorney Docket No.: 0150150

REMARKS

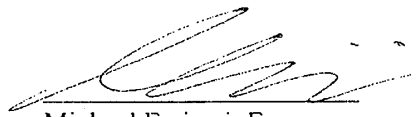
Prior to the present amendment and response, claims 1-20 were pending in the present application. Claims 1-9 have been elected for prosecution, while non-elected claims 10-20 have been canceled, and new claims 21-28 have been added. In summary, claims 1-9 and 21-28 now remain in the present application.

Applicant respectfully requests an early examination and/or allowance of claims 1-9 and 21-28 remaining in this application.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Dated: 1/15/09

FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Telephone: (949) 282-1000
Facsimile: (949) 282-1002

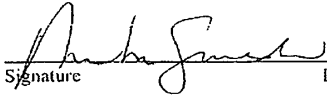

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Page 6

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/724,916		Filing Date 03/16/2007		☐ To be Mailed	
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APPLICATION AS FILED – PART I						OTHER THAN SMALL ENTITY			
(Column 1)		(Column 2)		SMALL ENTITY ☐		OR		SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A		N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A		N/A		N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A		N/A		
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =		OR	X \$ =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL		TOTAL				

APPLICATION AS AMENDED – PART II						OTHER THAN SMALL ENTITY					
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR		SMALL ENTITY	
AMENDMENT	01/15/2009	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 17	Minus	** 20	= 0	X \$ =		OR	X \$52=	0	
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X \$ =		OR	X \$220=	0	
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =		
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/724,916	03/16/2007	Kevin Q. Yin	0150150	4749
25700 7590 12/18/2008 FARJAMI & FARJAMI LLP 26522 LA ALAMEDA AVENUE, SUITE 360 MISSION VIEJO, CA 92691			EXAMINER CHEN, JACK S J	
			ART UNIT 2893	PAPER NUMBER
			MAIL DATE 12/18/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/724,916	YIN ET AL.	
	Examiner	Art Unit	
	Jack Chen	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 16 March 2007.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☐ Claim(s) _____ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☒ Claim(s) 1-20 are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892) 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5) ☐ Notice of Informal Patent Application 6) ☐ Other: _____.
---	--

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
 - I. Claims 1-9, drawn to semiconductor device, classified in class 257, subclass 288+.
 - II. Claims 10-20, drawn to a fabrication method, classified in class 438, subclass 427.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the process as claimed can be used to make another and materially different product, such as trench capacitor, etc.
3. Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and examination burden if restriction were not required because one or more of the following reasons apply:
 - (a) the inventions have acquired a separate status in the art in view of their different classification;

- (b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;
- (c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);
- (d) the prior art applicable to one invention would not likely be applicable to another invention;
- (e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include

(i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention.**

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected invention.

If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the

Art Unit: 2893

inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (8:00am-4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne N. Monbleau can be reached on (571)272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

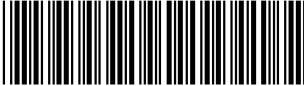
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Application/Control Number: 11/724,916
Art Unit: 2893

Page 5

Jack Chen
Primary Examiner
Art Unit 2893

/Jack Chen/
Primary Examiner, Art Unit 2893
December 17, 2008

Index of Claims 	Application/Control No. 11724916	Applicant(s)/Patent Under Reexamination YIN ET AL.
	Examiner Jack Chen	Art Unit 2893

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	12/17/2008								
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	2	÷								
	3	÷								
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
11/724,916	03/16/2007	2812	1000	0150150	20	2

CONFIRMATION NO. 4749

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA92691

FILING RECEIPT

Date Mailed: 04/16/2007

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Kevin Q. Yin, Irvine, CA;
Amol Kalburge, Irvine, CA;
David J. Howard, Irvine, CA;
Arjun Kar-Roy, Irvine, CA;
Dieter Dornisch, Carlsbad, CA;

Assignment For Published Patent Application

Newport Fab, LLC dba Jazz Semiconductor

Power of Attorney:

Michael Farjami--38135
Farshad Farjami--41014

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 04/13/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is
US11/724,916

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

Title

Deep trench isolation and method for forming same

Preliminary Class

438

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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U.S. PTO
11/724916
03/16/2007

Attorney Docket No.: 0150150

PATENT APPLICATION COVER SHEET

MAIL STOP PATENT APPLICATION
COMMISSIONER FOR PATENTS
P.O. BOX 1450; ALEXANDRIA, VA 22313-1450

CUSTOMER NUMBER

25700

PATENT TRADEMARK OFFICE

Transmitted herewith is the patent application of:

Inventor(s): Kevin Q. Yin, Amol Kalburge, David J. Howard, Arjun Kar-Roy and Dieter Dornisch

For: "Deep Trench Isolation and Method for Forming Same"

This application is a ☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application
No.: _____.

Enclosed are:

- ☒ Nine (9) Sheets of drawings
- ☒ Request for Non-Publication (Form PTO/SB/35 (11-00))
- ☒ Separate Payment Form PTO-2038 for \$40.00 is Attached for Assignment of the invention to:
Newport Fab, LLC dba Jazz Semiconductor
- ☐ The enclosed payment includes \$_____ for the recording of the assignment
- ☐ Applicant(s) claim(s) small entity status
- ☐ Information Disclosure Statement
- ☐ Preliminary Amendment
- ☒ Declaration and Power of Attorney
- ☒ The filing fee has been calculated as shown below:

	(Col. 1)	(Col. 2)
FOR:	No. Filed	No. Extra
BASIC FEE		
SEARCH FEE		
EXAMINATION FEE		
APPLICATION SIZE FEE (Total Number of Sheets)	(36 -100)/50=	0
TOTAL CLAIMS	20 -20 =	0
INDEPENDENT CLAIMS	2 -3 =	0
MULTIPLE DEPENDENT CLAIMS PRESENTED		

If the difference in Col. 1 is less than zero,
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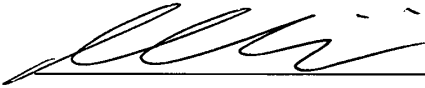
SMALL ENTITY	
RATE	FEE
	\$150.00
	\$250.00
	\$100.00
x \$125.00=	\$
x \$25.00=	\$
x \$100.00=	\$
+\$180.00=	\$
TOTAL	\$

OTHER THAN A SMALL ENTITY	
RATE	FEE
	\$300.00
	\$500.00
	\$200.00
x \$250.00=	\$
x \$50.00=	\$
x \$200.00 =	\$
+\$360.00 =	\$
TOTAL	\$1,000.00

- ☒ Enclosed is a payment in the amount of \$1,000.00 by credit card (Form PTO-2038 attached).
- ☐ Please charge Deposit Account No. 50-0731 in the amount of \$ _____.
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MICHAEL FARJAMI, ESQ.

Date: 3/16/07


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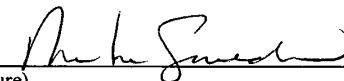
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Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, CA 92691
(949) 282-1000


(Signature)
Marci M. Sweda
(Typed or Printed Name of Person Mailing Paper or Fee)

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PATENT TRADEMARK OFFICE

Attorney Docket No.: 0150150

UNITED STATES PATENT APPLICATION

FOR

**DEEP TRENCH ISOLATION AND METHOD
FOR FORMING SAME**

INVENTORS:

**KEVIN Q. YIN
AMOL KALBURGE
DAVID J. HOWARD
ARJUN KAR-ROY
DIETER DORNISCH**

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(Signature) Marci M. Sweda

(Typed or Printed Name of Person Mailing Paper or Fee)

**PREPARED BY:
FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, CA 92691
(949) 282-1000**

Customer No.: 25700

05JAZ0003J

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention is generally in the field of semiconductor fabrication. More particularly, the invention is in the field of isolation region formation in semiconductor
5 substrates.

2. BACKGROUND ART

Deep trench isolation regions can be formed to provide electrical isolation for electronic devices in a semiconductor die, such as, for example, electrical isolation for bipolar devices in a semiconductor die, where the die includes both bipolar and
10 Complementary-Metal-Oxide-Semiconductor (CMOS) devices. A deep trench isolation region may also electrically isolate a bipolar transistor (i.e. a bipolar device) from adjacent bipolar transistors fabricated on the same semiconductor substrate. A deep trench isolation region can also be utilized, for example, to electrically isolate a collector of a bipolar transistor from neighboring regions of the substrate, thereby reducing
15 collector-to-substrate capacitance. Deep trench isolation regions may be formed on a substrate after formation of, for example, field oxide isolation regions, a buried layer, and an epitaxial layer of silicon.

In a conventional deep trench isolation process flow, a trench can be formed in a semiconductor substrate and sidewalls and bottom surface of the trench can be lined with
20 an oxide liner. A conformal layer of polycrystalline silicon (also referred to as polysilicon) can be deposited over the substrate so as to fill the trench. However, for a rectangular-shaped trench, a thick layer of polysilicon can be required to adequately fill

the trench with polysilicon. However, depositing a thick layer of polysilicon can significantly reduce polysilicon fill process throughput and require more frequent deposition furnace cleaning as a result of increased polysilicon flaking, thereby increasing manufacturing cost.

- 5 Thus, there is a need in the art for providing an improved deep trench isolation process and region in a semiconductor substrate to, for example, increase throughput and reduce manufacturing cost.

SUMMARY OF THE INVENTION

Deep trench isolation and method for forming same substantially as shown in
and/or described in connection with at least one of the figures, as set forth more
5 completely in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a top view of an exemplary conventional deep trench isolation region in a semiconductor die.

Figure 2 shows a top view of an exemplary deep trench isolation region in a semiconductor die in accordance with one embodiment of the present invention.

Figure 3 shows a flowchart illustrating the steps taken to implement an embodiment of the present invention.

Figure 4A illustrates a cross-sectional view, which includes a portion of a wafer processed according to an embodiment of the invention, corresponding to an initial step in the flowchart in Figure 3.

Figure 4B illustrates a cross-sectional view, which includes a portion of a wafer processed according to an embodiment of the invention, corresponding to an intermediate step in the flowchart in Figure 3.

Figure 4C illustrates a cross-sectional view, which includes a portion of a wafer processed according to an embodiment of the invention, corresponding to an intermediate step in the flowchart in Figure 3.

Figure 4D illustrates a cross-sectional view, which includes a portion of a wafer processed according to an embodiment of the invention, corresponding to an intermediate step in the flowchart in Figure 3.

Figure 4E illustrates a cross-sectional view, which includes a portion of a wafer processed according to an embodiment of the invention, corresponding to an intermediate step in the flowchart in Figure 3.

Figure 4F illustrates a cross-sectional view, which includes a portion of a wafer processed according to an embodiment of the invention, corresponding to a final step in the flowchart in Figure 3.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is directed to deep trench isolation and method for forming same. The following description contains specific information pertaining to the implementation of the present invention. One skilled in the art will recognize that the present invention may be implemented in a manner different from that specifically discussed in the present application. Moreover, some of the specific details of the invention are not discussed in order not to obscure the invention.

The drawings in the present application and their accompanying detailed description are directed to merely exemplary embodiments of the invention. To maintain brevity, other embodiments of the present invention are not specifically described in the present application and are not specifically illustrated by the present drawings.

It is noted that although a bipolar device is utilized as an example of an electronic device to illustrate the present invention, the invention's deep trench isolation region can be utilized to isolated electronic devices other than bipolar devices. Figure 1 shows a top view of structure 100, which includes conventional deep trench isolation region 102 and bipolar device 104. Structure 100, which can be a portion of a semiconductor die, also includes substrate 106, which can be a silicon substrate. Conventional deep trench isolation region 102 includes trench 108, oxide liner 110, and polysilicon filling 112 and bipolar device 104 includes emitter 128, which is situated over active region 130 and collector 132. Structure 100 can include a field oxide region overlying conventional deep trench isolation region 102 and a field oxide region separating active region 130 from collector 132, which are not shown in Figure 1 to simplify illustration of conventional

deep trench isolation region 102. Structure 100 can also include a number of adjacent deep trench isolation regions surrounding respective bipolar devices, which are not shown in Figure 1 to preserve brevity.

As shown in Figure 1, bipolar device 104, which is enclosed by conventional deep trench isolation region 102, includes emitter 128, which is situated over active region 130, and collector 132. Bipolar device 104 also includes a base (not shown in Figure 1), which is situated under emitter 128. For example, bipolar device 104 can be a vertical bipolar transistor, such as a vertical NPN or PNP transistor. Bipolar device 104 can be formed on an epitaxial layer (not shown in Figure 1), which can be formed over substrate 106. The epitaxial layer (not shown in Figure 1) can overlie a buried layer (also not shown in Figure 1), which can be formed in substrate 106. Bipolar device 104, which can be fabricated in a manner known in the art, is isolated by conventional deep trench isolation region 102 from surrounding bipolar devices situated on substrate 106. Conventional deep trench isolation region 102 also reduces collector-to-substrate capacitance by isolating collector 132 of bipolar device 104 from the neighboring substrate.

Also shown in Figure 1, trench 108 is situated in substrate 106 and has outside wall 114, which has corners 118, inside wall 116, which has corners 120, and sides 117a, 117b, 117c, and 117d (hereinafter “sides 117a through 117d”). Trench 108 has a rectangular shape, wherein each of corners 118 of outside wall 114 and corners 120 of inside wall 116 form a right angle. Trench 108 has trench corner width 122, which represents the perpendicular distance, i.e., the minimum distance, between corners 118 of outside wall 114 and corners 120 of inside wall 116, and trench side width 124, which

represents the perpendicular distance between outside wall 114 and inside wall 116 along each of sides 117a through 117d. For example, trench corner width 122 can be approximately 1.4 microns and trench side width 124 can be approximately 1.0 micron. Trench 108 can have a depth of, for example, approximately 7.0 microns. The distance
5 between opposite sides 117a and 117c of trench 108 can be, for example, approximately 3.0 microns and the distance between opposite sides 117b and 117d can be, for example, approximately 5.0 microns. Trench 108 can be formed by utilizing a suitable mask and etch process as is known in the art.

Also shown in Figure 1, oxide liner 110 is situated on outside and inside walls 114
10 and 116 and bottom surface (not shown in Figure 1) of trench 108 and can comprise silicon oxide, which can be thermally grown in trench 108. For example, oxide liner 110 can have a thickness of approximately 1000.0 Angstroms. Further shown in Figure 1, polysilicon filling 112 is situated in trench 108 and can be formed by conformally depositing a layer of polysilicon (polycrystalline silicon) over top surface 126 of substrate
15 106. In order to sufficiently fill corner regions 119 of trench 108 with polysilicon, the thickness of the deposited polysilicon layer can be approximately 1.5 microns for a trench side width (i.e. trench side width 124) of approximately 1.0 micron. However, depositing an approximate 1.5 micron thick layer of polysilicon requires a long cycle time, which significantly reduces polysilicon fill process throughput and, thereby, increases
20 manufacturing cost. Also, a polysilicon deposition thickness of approximately 1.5 microns can cause a significant amount of polysilicon flaking, which correspondingly increases the amount of polysilicon particles in the deposition furnace. As a result, the

deposition furnace requires more frequent cleaning, which also increases manufacturing cost.

It is again noted that although a bipolar device (i.e. a bipolar transistor) is utilized as an example of an electronic device to illustrate the present invention, the invention's

5 deep trench isolation region can be utilized to isolated electronic devices other than bipolar devices. Figure 2 shows a top view of structure 200 including deep trench isolation region 202, in accordance with one embodiment of the present invention.

Structure 200, which can be a portion of a semiconductor die, also includes bipolar device 204 and substrate 206, which can be a silicon substrate. Deep trench isolation region 202

10 includes trench 208, oxide liner 210, and polysilicon filling 212 and bipolar device 204 includes emitter 214, which is situated over active region 216, and collector 218.

Structure 200 can include a field oxide region overlying deep trench isolation region 202 and a field oxide region separating active region 216 from collector 218, which are not shown in Figure 2 to simply illustration of the invention. Structure 200 can also include a

15 number of adjacent deep trench isolation regions surrounding respective bipolar devices, which are not shown in Figure 2 to preserve brevity.

As shown in Figure 2, bipolar device 204, which is enclosed by deep trench isolation region 202, includes emitter 214, which is situated over active region 216, collector 218, and a base (not shown in Figure 2), which is situated under emitter 214.

20 For example, bipolar device 204 can be a vertical bipolar transistor, such as a vertical NPN or PNP transistor. In one embodiment, bipolar device 204 can be a vertical silicon-germanium (SiGe) bipolar transistor, such as a vertical NPN SiGe transistor. Bipolar

device 204 can be formed in a manner known in the art on an epitaxial layer (not shown in Figure 2), which can be formed over substrate 206. The epitaxial layer (not shown in Figure 2) can overlie a buried layer (also not shown in Figure 2), which can be formed in substrate 206. Bipolar device 204 is isolated by deep trench isolation region 202 from
5 surrounding bipolar devices situated on substrate 206. Deep trench isolation region 202 reduces collector-to-substrate capacitance by isolating collector 218 of bipolar device 204 from the neighboring substrate, i.e., portions of substrate 206 situated outside of deep trench isolation region 202.

Also shown in Figure 2, trench 208 is situated in substrate 206 and has outside
10 wall 220, which has chamfered corners 224, inside wall 222, which has corners 223, and sides 228a, 228b, 228c, and 228d (hereinafter "sides 228a through 228d"). Further shown in Figure 2, trench chamfered corners 240 are formed between and connecting sides 228a through 228d. Trench chamfered corners 240 are also formed between chamfered corners 224 of outside wall 220 and corners 223 of inside wall 222 of trench 208. In the present
15 invention, trench chamfered corners 240 significantly reduce trench corner width 230, which represents the perpendicular distance, i.e., the minimum distance, between chamfered edge 232 and each of corners 223 of inside wall 222 of trench 208.

Trench corner width 230 can be determined by appropriately selecting length 234 of chamfered edge 232 at chamfered corners 224 of outside wall 220. In the present
20 embodiment, length 234 of chamfered edge 232 can be selected such that trench corner width 230 is less than trench side width 236, which represents the perpendicular distance, i.e., the minimum distance, between outside wall 220 and inside wall 222 along each of

sides 226a through 226d of trench 208. For example, for a trench side width of approximately 1.0 micron, trench corner width 230 can be approximately 0.9 microns. In one embodiment, trench corner width 230 can be less than or equal to trench side width 236. Chamfered edge 232 can form equal angles with respect to adjacent sides of trench 208, such as sides 228a and 228d. In another embodiment, chamfered edge 232 may form a different angle with respect to each adjacent side of trench 208. Each of corners 223 of inside wall 222 of trench 208 can form, for example, an approximate right angle.

Trench 208 can have a size of, for example, 3.0 microns by 5.0 microns, which corresponds to the respective distances between opposite sides of trench 208. For example, the distance between opposite sides 228a and 228c of trench 208 can be approximately 3.0 microns. For example, the distance between opposite sides 228d and 228b of trench 208 can be approximately 5.0 microns. Trench 208 can have a depth of, for example, approximately 7.0 microns.

Further shown in Figure 2, oxide liner 210 is situated on outer and inner walls 220 and 222 and a bottom surface (not shown in Figure 2) of trench 208 and can comprise thermal oxide. For example, oxide liner 210 can have a thickness of approximately 1000.0 Angstroms. Also shown in Figure 2, polysilicon (i.e. polycrystalline silicon) filling 212 is situated on oxide liner 210 and fills trench 208. Polysilicon filling 212 can be formed by conformally depositing a layer of polysilicon over top surface 238 of substrate 206. In order to sufficiently fill trench 208, the thickness of the deposited polysilicon layer can be approximately 0.7 microns for a trench side width (i.e. trench side width 236) of approximately 1.0 micron, a trench corner width (i.e. trench corner width

230) of approximately 0.9 microns, and a depth of approximately 7.0. In contrast, a deposited polysilicon layer thickness of approximately 1.5 microns is required to fill trench 108 in conventional deep trench isolation region 102, which has a trench corner width of approximately 1.4 microns and a substantially similar trench side width and
5 depth as trench 208.

Thus, by forming trench chamfered corners 240 to reduce the trench corner width to approximately 0.9 microns compared to a trench corner width of approximately 1.4 microns for conventional trench 108, an embodiment of the present invention advantageously reduces the deposited polysilicon layer thickness from approximately 1.5
10 microns to approximately 0.7 microns. Since deposited polysilicon layer thickness is reduced by approximately one half, the present embodiment can increase polysilicon fill process throughput for trench 208 by approximately 100 percent compared to the polysilicon fill process throughput for conventional trench 108 in Figure 1. Also, since the invention significantly reduces the deposited polysilicon layer thickness, polysilicon
15 flaking is significantly reduced, thereby significantly increasing the average time between consecutive polysilicon deposition furnace cleanings.

Thus, by forming trench chamfered corners to reduce trench corner width by approximately 40 percent, e.g., from approximately 1.4 microns to approximately 0.9 microns, the invention significantly increases polysilicon fill process throughput and also
20 significantly increases the average time between polysilicon deposition furnace cleaning. As a result, the present invention advantageously reduces manufacturing cost. The fabrication of the invention's deep trench isolation region, such as deep trench isolation

region 202 in Figure 2, is further discussed below in relation to Figures 3, 4A, 4B, 4C, 4D, 4E, and 4F.

Figure 3 shows a flowchart illustrating an exemplary method according to an embodiment of the present invention. Certain details and features have been left out of flowchart 100 that are apparent to a person of ordinary skill in the art. For example, a step may consist of one or more substeps or may involve specialized equipment or materials, as known in the art. Steps 370 through 380 indicated in flowchart 300 are sufficient to describe an embodiment of the present invention's deep trench isolation region 202 in Figure 2; other embodiments of the invention may utilize steps different from those shown in flowchart 300. It is noted that the processing steps shown in flowchart 300 are performed on a wafer, which, prior to step 370, includes field oxide regions, a buried layer, and an epitaxial layer situated over the buried layer. The wafer may be referred to as a semiconductor die or simply a die in the present application.

Moreover, structures 470 through 480 in Figures 4A through 4F illustrate the result of performing, on the semiconductor structure discussed above, steps 370 through 380 of flowchart 300, respectively. For example, structure 470 shows the semiconductor structure discussed above after processing step 370, structure 472 shows structure 470 after the processing of step 372, structure 474 shows structure 472 after the processing of step 374, and so forth. It is noted that although formation of only one deep trench isolation region is specifically discussed herein to preserve brevity, multiple deep trench isolation regions can be formed in a substrate, such as substrate 206 in Figure 2, utilizing the innovative process of the present invention.

Referring now to Figure 4A, structure 470 of Figure 4A shows structure 200 along line 4-4 in Figure 2 prior to formation of deep trench isolation region 202 and bipolar device 204. Structure 470 also includes field oxide regions, a buried layer, and an epitaxial layer, which are not shown in structure 200 in Figure 2. In structure 470, buried layer 404, epitaxial layer 406, and field oxide regions 408 and 410 are formed in substrate 402, which corresponds to substrate 206 in structure 200 in Figure 2. Buried layer 404 is formed in substrate 402 in a manner known in the art and can comprise, for example, heavily doped N-type material. Epitaxial layer 406 can comprise single-crystal silicon, which can be epitaxially grown on substrate 402 in a manner known in the art. Field oxide regions 408 and 410 comprise silicon oxide and may be formed in substrate 402 in a manner known in the art.

Continuing with step 370 in Figure 3 and structure 470 in Figure 4A, at step 370 of flowchart 300, silicon nitride ("nitride") layer 414 is deposited on top surface 418 of substrate 402 and hard mask 416 is formed on nitride layer 414. Nitride layer 414 can be formed, for example, by depositing a layer of nitride on top surface 418 of substrate 402 in a low pressure chemical vapor deposition (LPCVD) process and can have a thickness of approximately 1500.0 Angstroms, for example. Hard mask 416 can comprise densified oxide, which can be formed by depositing TEOS oxide on nitride layer 414 in an LPCVD process and densifying the TEOS oxide in a manner known in the art. In one embodiment, hard mask 416 can comprise high-density plasma (HDP) oxide. The thickness of hard mask 416 can be, for example, approximately 4500.0 Angstroms. The result of step 370 of flowchart 300 is illustrated by structure 470 in Figure 4A.

Referring to step 372 in Figure 3 and structure 472 in Figure 4B, at step 372 of flowchart 300, a photoresist mask is deposited and patterned on hard mask 416. The patterned photoresist mask is utilized to form trench 420 having an initial depth and trench chamfered corners, and the photoresist mask is then removed. Trench 420 corresponds to trench 208 in Figure 2, which has trench chamfered corners 240 formed between and connecting sides 228a through 228d of trench 208. The photoresist mask can be deposited and patterned on hard mask 416 in a manner known in the art to achieve a trench opening in the photoresist mask having a side width substantially equal to a critical dimension (CD) and a corner width.

In a first etch step, trench 420 can be formed by utilizing an etchant such as CF₄/CHF₃/Ar or other appropriate etchant and adjusting the etchant chemistry to sequentially etch through hard mask 416, nitride layer 414, field oxide region 408, and etch a short distance into epitaxial layer 406. The resulting trench 420 formed by the etch step discussed above defines outside wall 422, inside wall 424 and bottom surface 426.

Outside and inside walls 422 and 424 of trench 420 correspond, respectively, to outside and inside walls 220 and 222 of trench 208 in Figure 2. Bottom surface 426 of trench 420 can extend into epitaxial layer 406 to an initial depth a short distance below field oxide region 408. Field oxide portions 409 and 411, which are situated adjacent to sidewalls 422 and 424, respectively, are formed as a result of the etch step discussed above.

In a second etch step, the photoresist mask can be removed from hard mask 416 and polymer residue formed as a result of the first etch step discussed above can be removed from outside and inside walls 422 and 424 of trench 420 in a wet strip utilizing

an appropriate etchant as known in the art. Trench side width 423 of trench 420, which corresponds to trench side width 236 of trench 208 in Figure 2, is determined by the CD of the trench opening patterned in the photoresist mask discussed above, and can be, for example, approximately 1.0 micron. The result of step 372 of flowchart 300 is illustrated
5 by structure 472 in Figure 4B.

Referring to step 374 in Figure 3 and structure 474 in Figure 4C, at step 374 of flowchart 300, hard mask 416 is utilized to perform a trench etch to define a final depth of trench 420. The trench etch can be performed by utilizing an appropriate etchant to etch silicon in epitaxial layer 406 to increase the depth of trench 420 to a final depth of,
10 for example, approximately 7.0 microns. In one embodiment, the trench etch discussed above can be utilized to increase the depth of trench 420 to a final depth of between approximately 3.0 and approximately 7.0 microns. During the trench etch, a portion of hard mask 416 is also removed, which reduces the thickness of hard mask 416 by approximately one half. By way of example, hard mask 416 can be reduced from an
15 initial thickness of approximately 4500.0 Angstroms to a thickness of approximately 2250.0 Angstroms as a result of the trench etch. After performance of the trench etch discussed above, a post trench clean can be performed by utilizing a diluted HF dip or other appropriate etchant to remove approximately 200.0 Angstroms of oxide from outside and inside walls 422 and 424 of trench 420. The result of step 374 of flowchart
20 300 is illustrated by structure 474 in Figure 4C.

Referring to step 376 in Figure 3 and structure 476 in Figure 4D, at step 376 of flowchart 300, hard mask 416 is removed, a channel stop implant is performed, and oxide

liner 428 is thermally grown on outside and inside walls 422 and 424 and bottom surface 426 of trench 420 and over nitride layer 414 situated on substrate 402. In the present embodiment, hard mask 416 can be removed in an anisotropic dry etch process that is selective to silicon and nitride and utilizes an etchant such as C₄F₈/CO/Ar or other appropriate etchant. As a result of the high selectivity of the anisotropic dry etch process, the etchant does not significantly damage nitride layer 414 or silicon situated at bottom surface 426 of trench 420. By utilizing an anisotropic dry etch to remove hard mask 416, the present embodiment of the invention can maintain a uniform trench side width of approximately 1.0 micron, for example. In contrast, in a process utilizing a wet etch to remove hard mask 416, portions of field oxide 408 can be etched, which can undesirably alter the shape of trench 420. After removal of hard mask 416, outside and inside walls 422 and 424 of trench 420 can be cleaned by utilizing, for example, a plasma etch and an HF strip to remove polymer by-products formed on the outside and inside walls during etching of hard mask 416.

In the channel stop implant performed in step 376, a dopant such as boron, for example, can be implanted in bottom surface 426 of trench 420 to prevent current leakage. A wet strip can be performed to eliminate carbon and metal contamination resulting from the channel stop implant. Also, prior to thermally growing oxide liner 428, a thirty-second HF preclean can be performed to appropriately clean outside and inside walls 422 and 424 and bottom surface 426 of trench 420.

Next, oxide liner 428 is formed by thermally growing oxide on outside and inside walls 422 and 424 and bottom surface 426 of trench 420. The layer of thermal oxide can

be densified by utilizing, for example, a temperature of approximately 750° C and an inert gas such as nitrogen to complete formation of oxide liner 428. By way of example, oxide liner 428 can have a thickness of approximately 1000.0 Angstroms. Since oxide liner 428 comprises thermally grown oxide, oxide liner 428 is not formed on nitride layer 414 situated on top surface 418 of silicon substrate 402. By not forming oxide liner 428 on nitride layer 414, a buffered oxide etchant ("BOE") wet strip does not need to be performed in a subsequent step to remove oxide liner 428. As a result, field oxide lateral etching or undercutting caused by a BOE wet strip is eliminated, thereby providing a substantially flat final topography over a subsequently formed deep trench isolation region. The result of step 376 of flowchart 300 is illustrated by structure 476 in Figure 4D.

Referring to step 378 in Figure 3 and structure 478 in Figure 4E, at step 378 of flowchart 300, a layer of polysilicon is conformally deposited over substrate 402 to fill trench 420 and etched in an etch back process. As a result of forming trench chamfered corners to reduce the trench corner width of trench 420 to approximately 0.9 microns, the layer of polysilicon can be conformally deposited over substrate 402 at a reduced thickness of approximately 0.7 microns. In contrast, as discussed above, a polysilicon deposition thickness of approximately 1.5 microns is required to adequately fill conventional trench 108 in Figure 1. By reducing the polysilicon deposition thickness from approximately 1.5 microns to approximately 0.7 microns, the invention achieves a significant increase in polysilicon fill process throughput and a significant increase in average time between polysilicon deposition furnace cleaning, which advantageously

reduces manufacturing cost.

In the etch back process, a break-through etch is first performed utilizing, for example, a CF₄ etch chemistry to break through an oxide skin that is usually formed on the layer of polysilicon. Next, a main etch is performed utilizing, for example, an SF₆/O₂ etch chemistry, followed by an over etch utilizing, for example, a Cl₂/HBr etch chemistry.

As a result of the etch back process discussed above, the layer of polysilicon is etched back to depth 430 inside trench 420 to form polysilicon filling 432, which corresponds to polysilicon filling 212 in Figure 2. Depth 430 can be, for example, approximately 1500.0 Angstroms below interface 434, which is situated at a boundary of field oxide portion 409 (or field oxide portion 411) and nitride layer 414. Since the respective etch chemistries utilized to perform the main etch and the over etch discussed above are highly selective to oxide, minimal etching of oxide liner 428 occurs during the polysilicon etch back process. The result of step 378 of flowchart 300 is illustrated by structure 478 in Figure 4E.

Referring to step 380 in Figure 3 and structure 480 in Figure 4F, at step 380 of flowchart 300, oxide is grown inside trench 420 to form continuous field oxide region 440 and nitride layer 414 is removed. As a result, grown oxide in trench 420 merges with field oxide portions 409 and 411 to form continuous field oxide region 440. By way of example, field oxide region 440 can have a thickness of approximately 4100.0 Angstroms. Since substantially no lateral etching occurs in field oxide portions 409 and 411, substantially no cavities are formed on top surface 436 of field oxide region 440, which is formed when field oxide portions 409 and 411 are joined by oxide grown in trench 420. Nitride layer 414 (shown in Figures 4A through 4E) can be removed by

utilizing a phosphoric etch process or other appropriate etch process as known in the art.

Thus, as a result of the above processing steps, deep trench isolation region 442, which corresponds to deep trench isolation region 208 in Figure 2, is formed underneath field oxide region 440. A bipolar device, such as bipolar device 204 in Figure 2 can be formed in active regions 444 and 446 in Figure 4F. For example, emitter 214 of bipolar device 204 can be formed in active region 444 and collector 218 of bipolar device 204 can be formed in active region 446. Thus, deep trench isolation region 442 can electrically isolate a bipolar device formed in active regions 444 and 446 from adjacent bipolar devices.

Thus, as discussed above, the present invention provides a deep trench isolation region with trench chamfered corners, which significantly reduce trench corner width. As a result, the invention's deep trench isolation region significantly increases polysilicon fill process throughput and the average time between polysilicon deposition furnace cleaning, thereby advantageously reducing manufacturing cost. It is understood to those of ordinary skill in the art that although the invention has been described in reference to a "wafer," such wafer can be diced and singulated into individual dies and thereafter packaged using various semiconductor packaging techniques and processes. As such, the invention is manifestly applicable to fabricating wafers and/or dies, which may or may not be later packaged, in accordance with the teachings of the invention as described above.

From the above description of the invention it is manifest that various techniques can be used for implementing the concepts of the present invention without departing

from its scope. Moreover, while the invention has been described with specific reference to certain embodiments, a person of ordinary skill in the art would appreciate that changes can be made in form and detail without departing from the spirit and the scope of the invention. Thus, the described embodiments are to be considered in all respects as

5 illustrative and not restrictive. It should also be understood that the invention is not limited to the particular embodiments described herein but is capable of many rearrangements, modifications, and substitutions without departing from the scope of the invention.

Thus, deep trench isolation and method for forming same have been described.

CLAIMS

1. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

5 a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;

wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer filling said trench.

10 2. The semiconductor die of claim 1, wherein a trench corner width at said at least one trench chamfered corner is less than a trench side width along said plurality of sides.

3. The semiconductor die of claim 1, wherein said at least one trench
15 chamfered corner is formed between a chamfered corner of an outside wall of said trench and a corner of an inside wall of said trench.

4. The semiconductor die of claim 1, wherein a field oxide region overlies said trench.

20

5. The semiconductor die of claim 1, wherein said trench further comprises an oxide liner situated on inside walls and outside walls of said trench.

6. The semiconductor die of claim 2, wherein said trench side width along said plurality of sides is approximately 1.0 micron.

7. The semiconductor die of claim 1, wherein said semiconductor die is
5 enclosed in a semiconductor package.

8. The semiconductor die of claim 1, wherein said electronic device is a bipolar transistor.

10 9. The semiconductor die of claim 1, wherein said electronic device is a silicon-germanium bipolar transistor.

10. A method for forming a deep trench isolation region in a substrate of a semiconductor die, said method comprising steps of:

15 forming a trench in said substrate, said trench having a plurality of sides and at least one trench chamfered corner formed between and connecting said plurality of sides; depositing a layer of polysilicon over said substrate to fill said trench; wherein said at least one trench chamfered corner causes a reduction in a thickness of said polysilicon layer.

20

11. The method of claim 10, wherein a trench corner width at said at least one trench chamfered corner is less than a trench side width along said plurality of sides.

12. The method of claim 10, wherein said at least one trench chamfered corner is formed between a chamfered corner of an outside wall of said trench and a corner of an inside wall of said trench.

5

13. The method of claim 10 further comprising a step of forming an oxide liner on inside walls and outside walls of said trench prior to depositing said layer of polysilicon.

10 14. The method of claim 10 further comprising a step of etching back said layer of polysilicon in said trench.

15 15. The method of claim 10 further comprising a step of forming a hard mask over said substrate prior to forming said trench in said substrate.

16. The method of claim 11, wherein said trench side width along said plurality of sides is approximately 1.0 micron.

17. The method of claim 10, wherein said trench has a depth of approximately
20 7.0 microns.

18. The method of claim 10, wherein said step of forming said trench in said

substrate comprises etching through a field oxide region formed in said substrate.

19. The method of claim 10, wherein said deep trench isolation region surrounds an electronic device formed over said substrate.

5

20. The method of claim 19, wherein said electronic device is a bipolar transistor.

ABSTRACT

According to one exemplary embodiment, a semiconductor die including at least one deep trench isolation region for isolating an electronic device (for example, a bipolar device) includes a trench situated in a substrate of the semiconductor die, where
5 the trench has sides surrounding the electronic device, and where the trench has at least one trench chamfered corner formed between and connecting the sides of the trench. The at least one trench chamfered corner is formed between a chamfered corner of an outside wall of said trench and a corner of an inside wall of the trench. A trench corner width at the at least one trench chamfered corner is less than a trench side width
10 along the sides of the trench.

Fig. 1

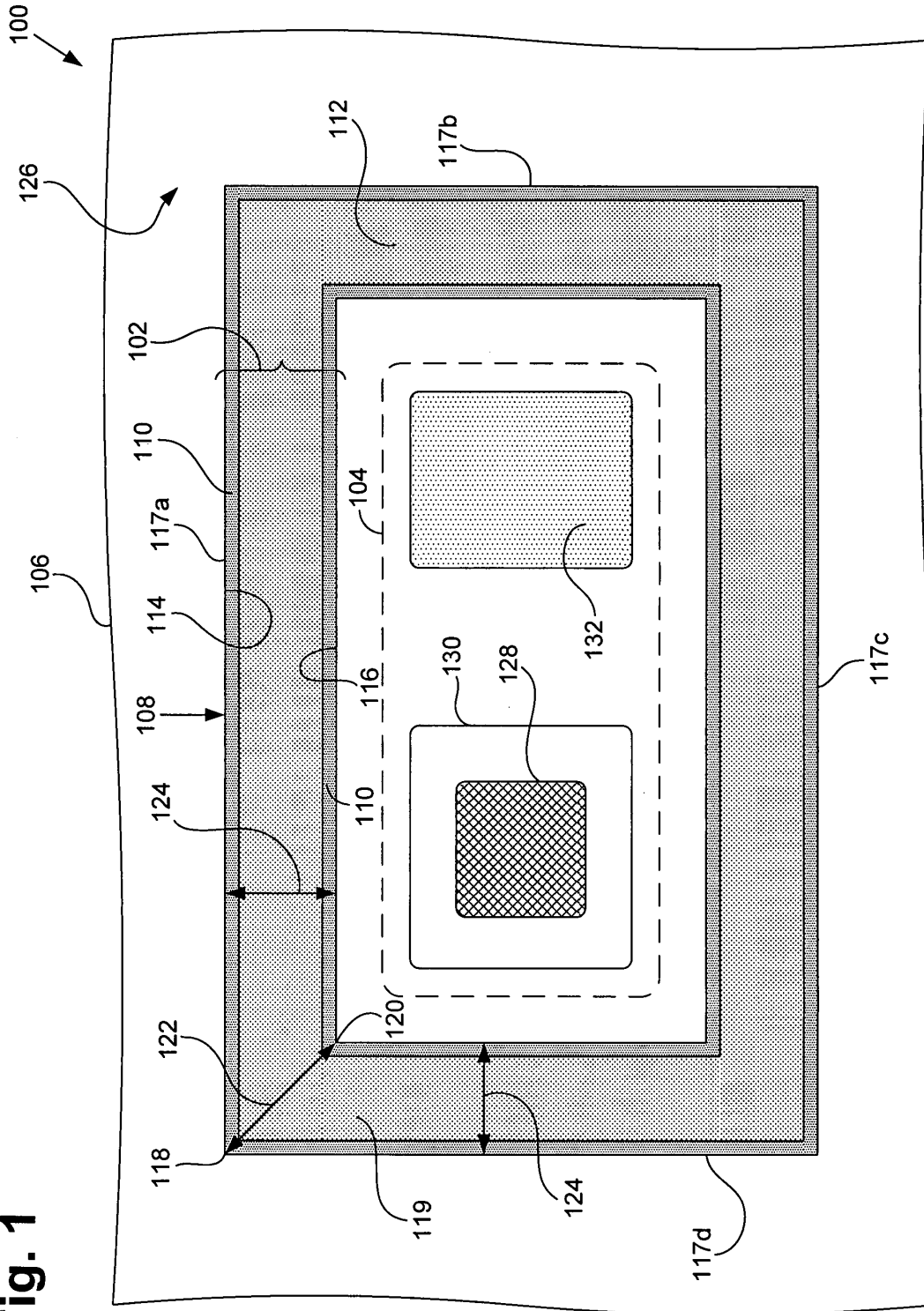


Fig. 2

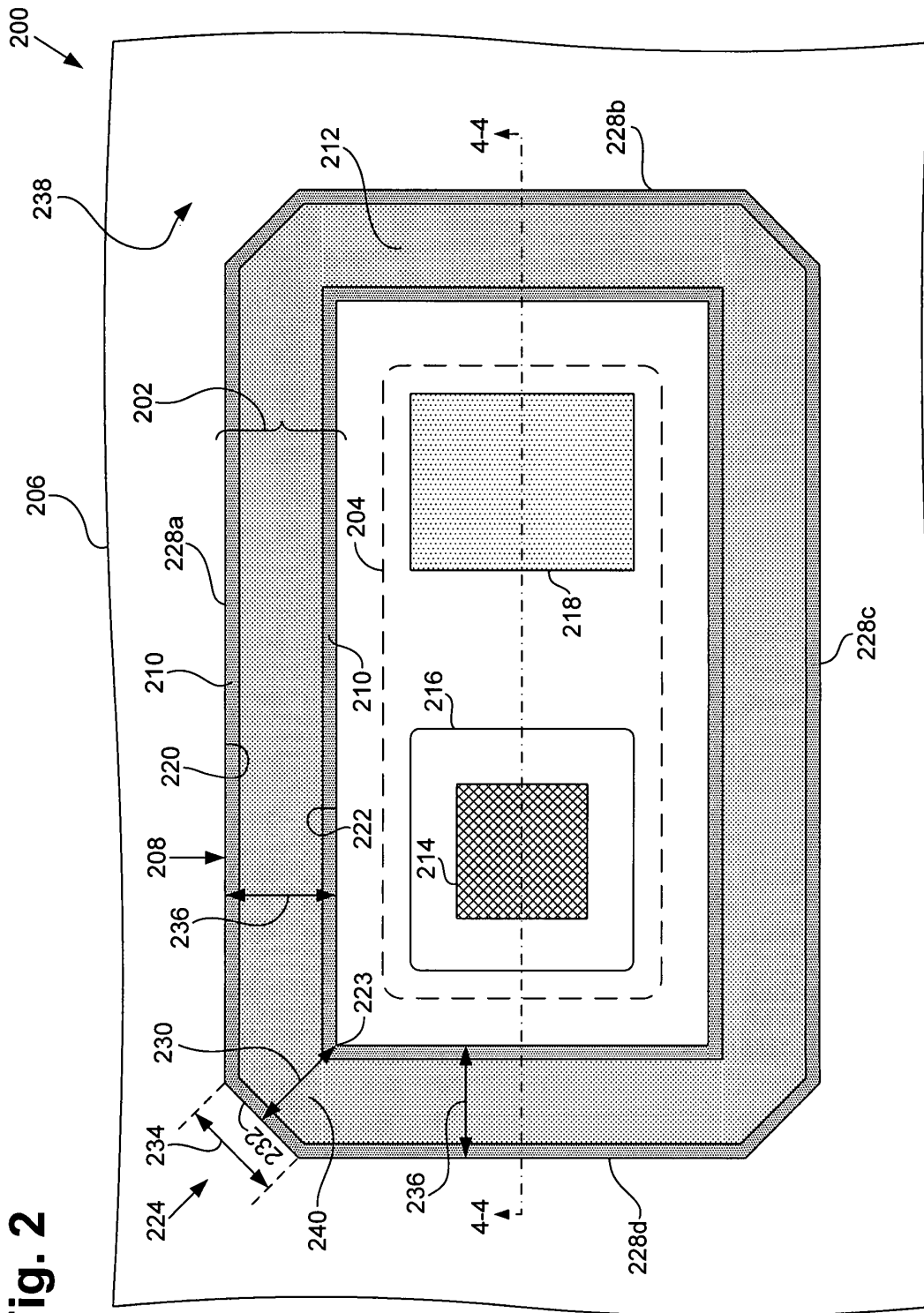


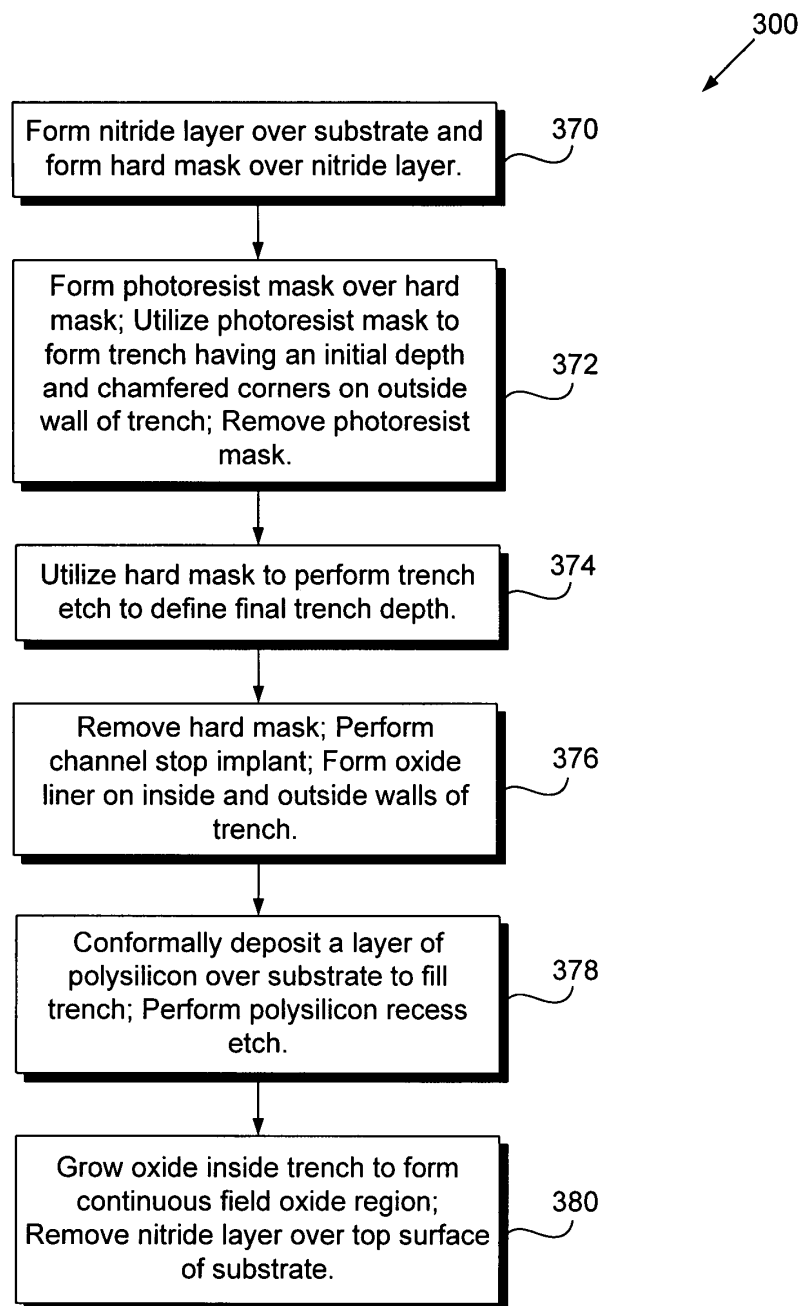
Fig. 3

Fig. 4A

470

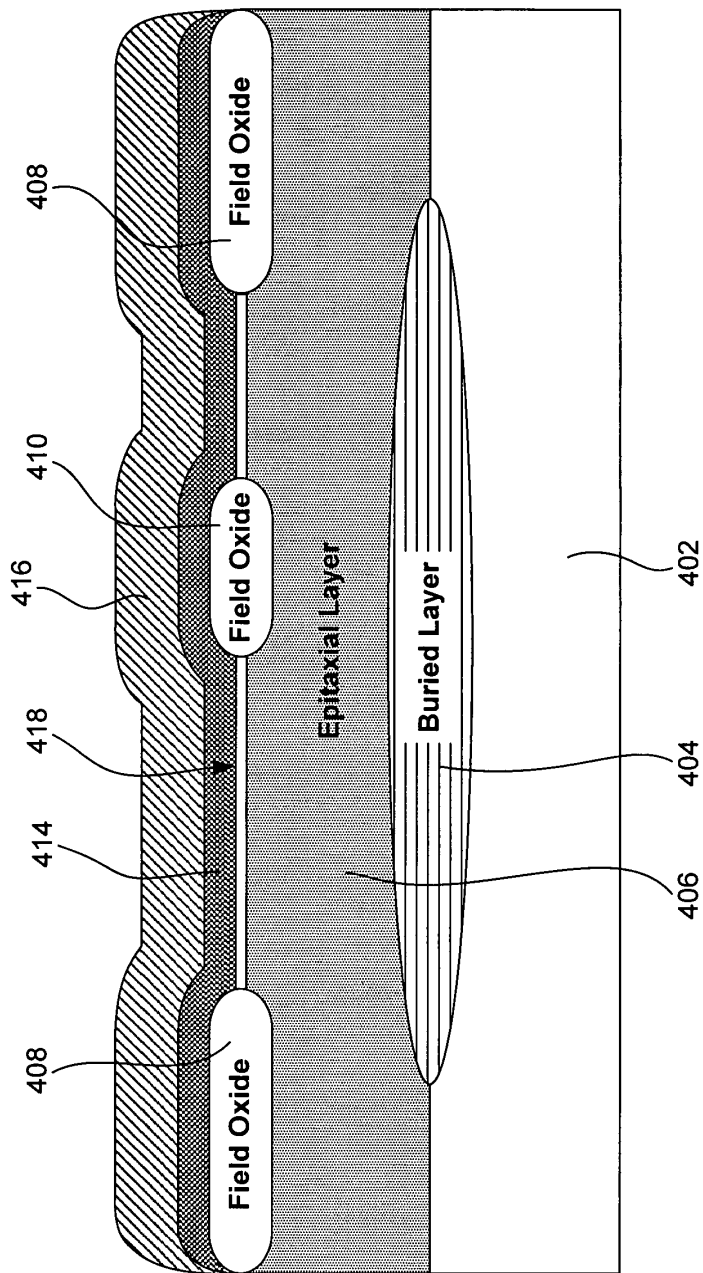


Fig. 4B

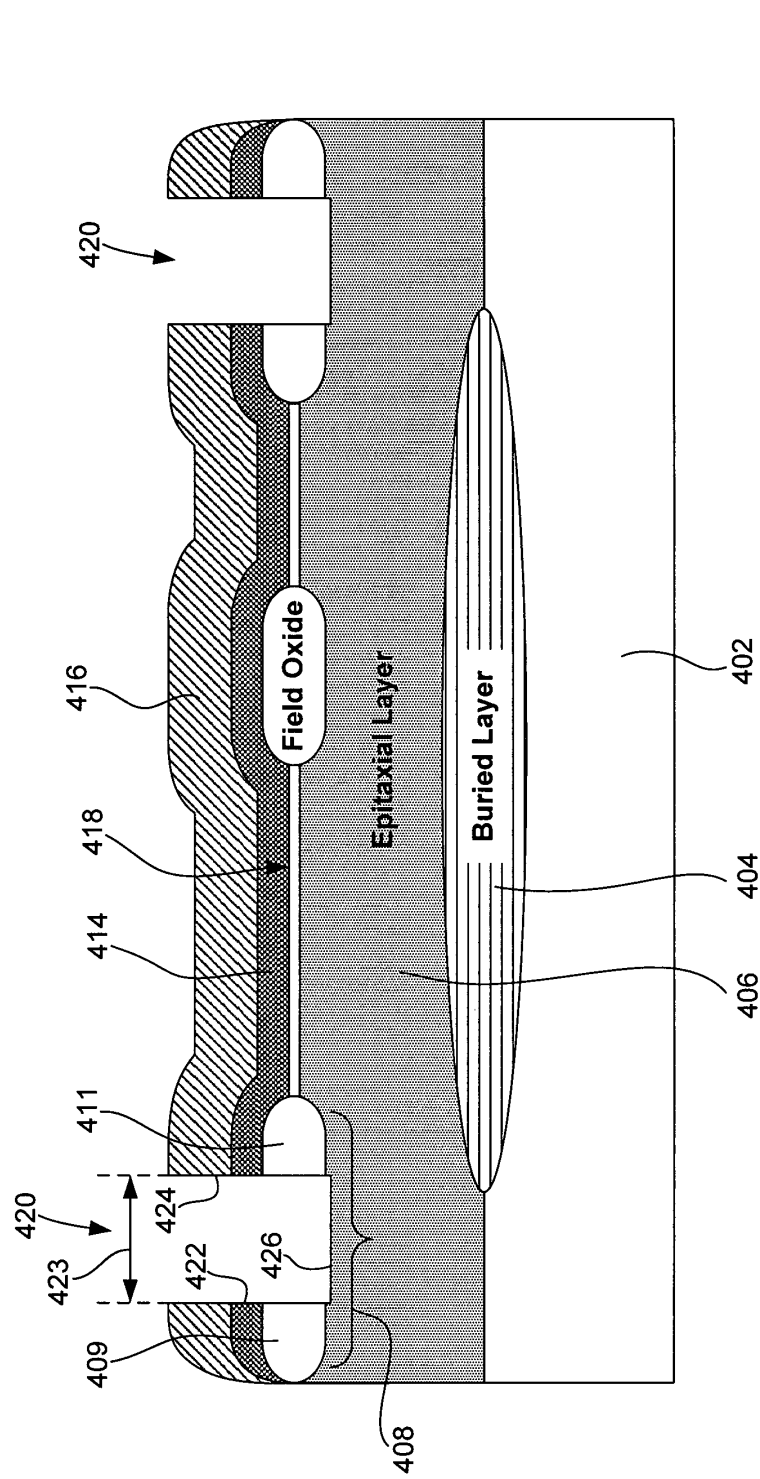


Fig. 4C

474

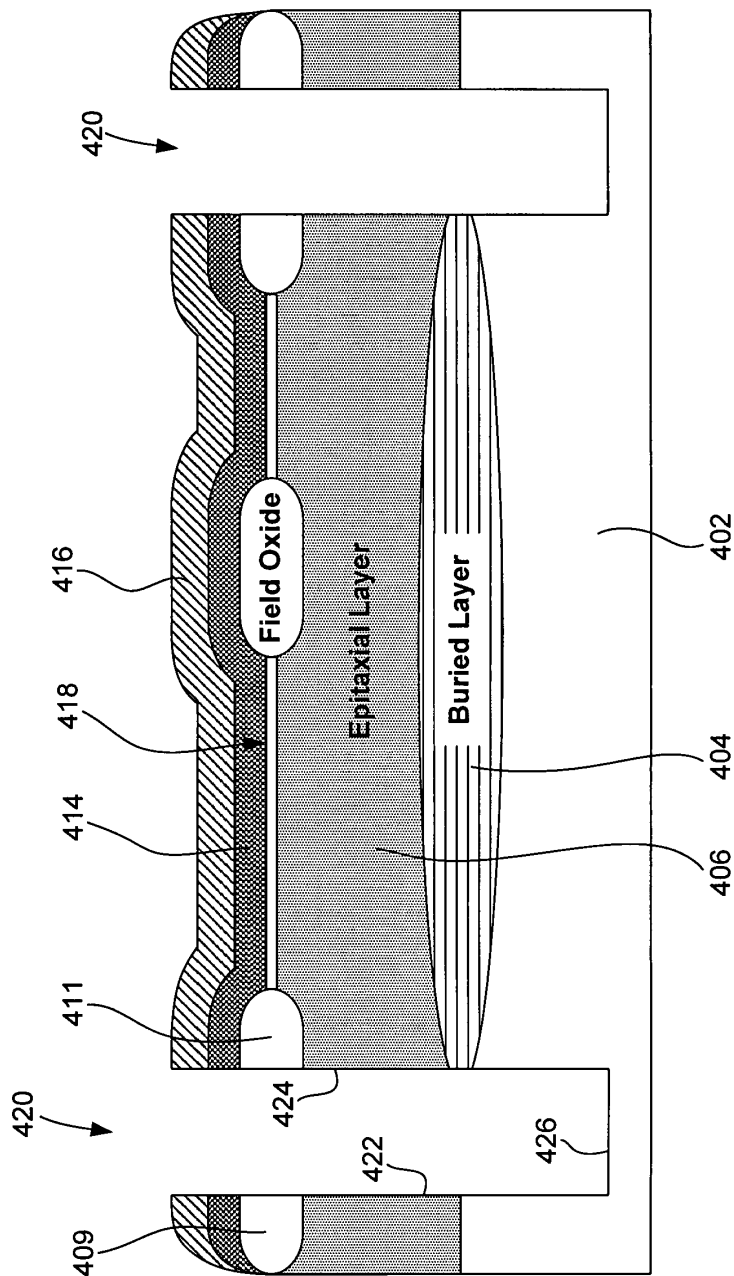


Fig. 4D

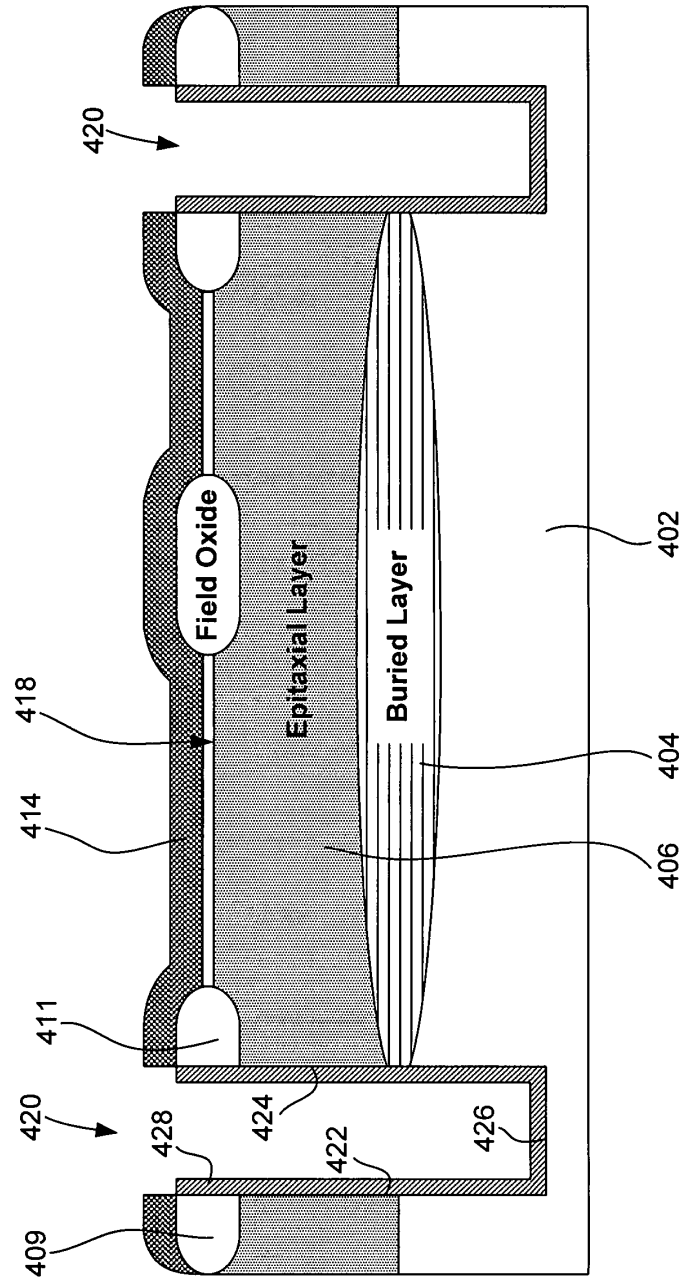
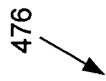


Fig. 4E

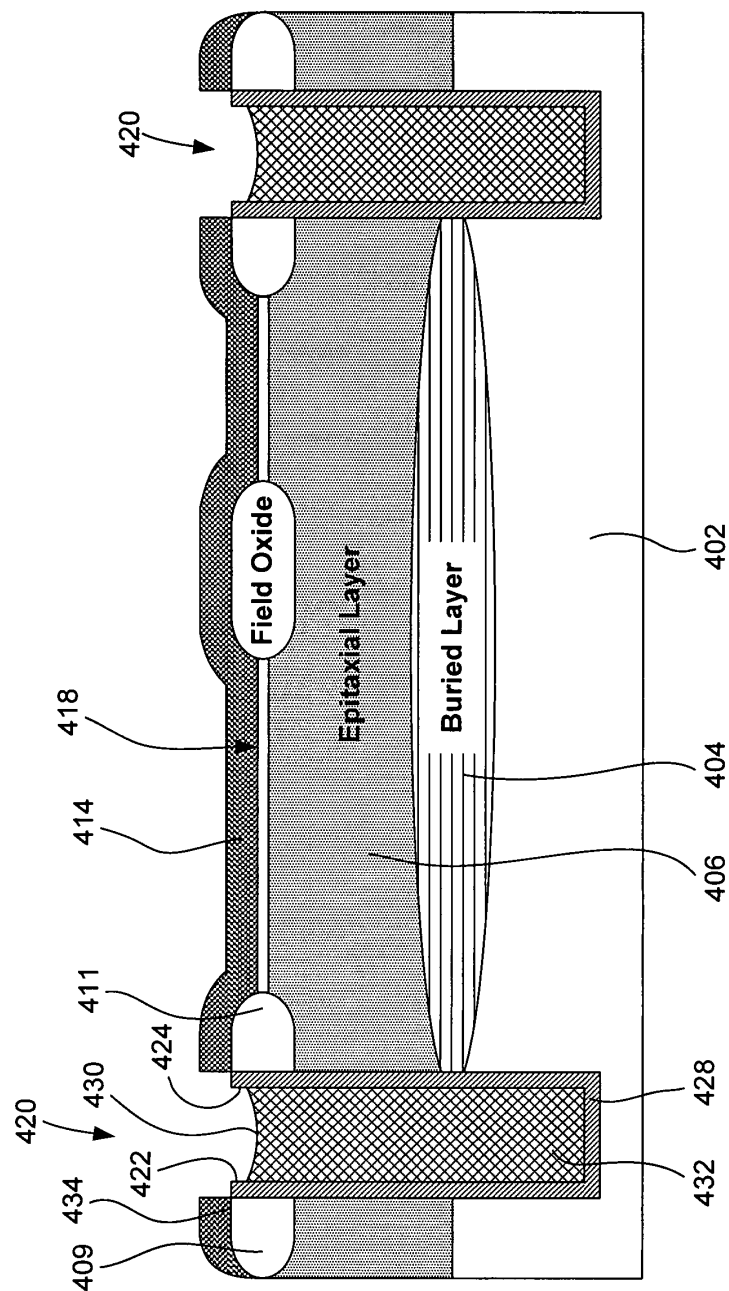
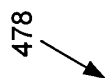
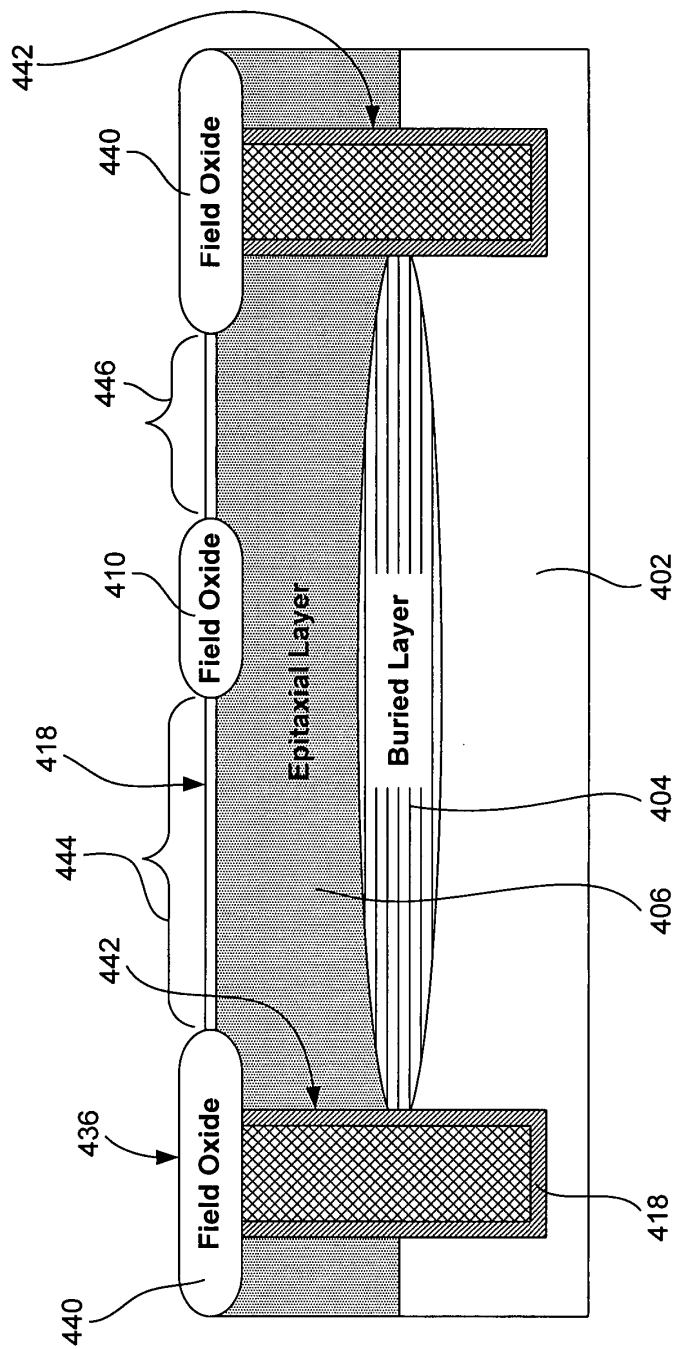


Fig. 4F

480



United States Patent Application
COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **DEEP TRENCH ISOLATION AND METHOD FOR FORMING SAME.**

The specification of which

a. XX is attached hereto

b. _____ was filed on _____ as application serial no. _____ and was amended on _____ (if applicable) (in the case of a PCT-filed application) described and claimed in international no. _____ filed _____ and as amended on _____ (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56 (see the last page attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, Sections 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

a. XX no such applications has been filed.

b. _____ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC Section 119

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

ALL FOREIGN APPLICATIONS, IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

I hereby claim the benefit under Title 35, United States Code, Sections 119 and 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

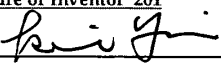
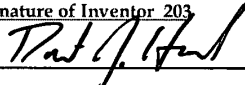
MICHAEL FARJAMI, Reg. No. 38,135
FARSHAD FARJAMI, Reg. No. 41,014

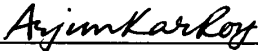
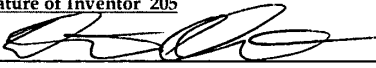
I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/firm/organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct them to the contrary.

Please direct all correspondence in this case to FARJAMI & FARJAMI LLP at the address indicated below:

FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Telephone: (949) 282-1000
Customer No.: 25700

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

201	FULL NAME FIRST Name: KEVIN OF INVENTOR		Middle Initial(s): Q.	LAST Name: YIN	
	City of Residence IRVINE	State or Foreign Country CALIFORNIA		Country of Citizenship USA	
	Post Office Address 161 Weathervane	City Irvine	State or Country CA	Zip Code 92603	
202	FULL NAME FIRST Name: AMOL OF INVENTOR		Middle Initial(s):	LAST Name: KALBURGE	
	City of Residence IRVINE	State or Foreign Country CALIFORNIA		Country of Citizenship INDIA	
	Post Office Address 4371 Rafael Street	City Irvine	State or Country CA	Zip Code 92604	
203	FULL NAME FIRST Name: DAVID OF INVENTOR		Middle Initial(s): J.	LAST Name: HOWARD	
	City of Residence IRVINE	State or Foreign Country CALIFORNIA		Country of Citizenship USA	
	Post Office Address 19 Springwater	City Irvine	State or Country CA	Zip Code 92604	
Signature of Inventor 201 		Signature of Inventor 202		Signature of Inventor 203 	
Date 3/13/07		Date		Date 3/13/2007	

204	FULL NAME FIRST Name: ARJUN OF INVENTOR		Middle Initial(s):	LAST Name: KAR-ROY	
	City of Residence IRVINE		State or Foreign Country CALIFORNIA		Country of Citizenship USA
	Post Office Address 59 Edgewood		City Irvine	State or Country CA	Zip Code 92618
205	FULL NAME FIRST Name: DIETER OF INVENTOR		Middle Initial(s):	LAST Name: DORNISCH	
	City of Residence CARLSBAD		State or Foreign Country CALIFORNIA		Country of Citizenship GERMANY
	Post Office Address 2732 York Road		City Carlsbad	State or Country CA	Zip Code 92010
206	FULL NAME FIRST Name: OF INVENTOR		Middle Initial(s):	LAST Name:	
	City of Residence		State or Foreign Country CALIFORNIA		Country of Citizenship
	Post Office Address		City	State or Country CA	Zip Code
Signature of Inventor 204 		Signature of Inventor 205 		Signature of Inventor 206	
Date 3/13/2007		Date 3/13/2007		Date	

37 C.F.R. Section 1.56 - Duty to disclose information material to patentability.

A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by Sections 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

Prior art cited in search reports of a foreign patent office in a counterpart application, and

The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

It refutes, or is inconsistent with, a position the applicant takes in:

Opposing an argument of unpatentability relied on by the Office, or

Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

Each inventor named in the application;

Each attorney or agent who prepares or prosecutes the application; and

Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

United States Patent Application
COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **DEEP TRENCH ISOLATION AND METHOD FOR FORMING SAME.**

The specification of which

a. XX is attached hereto

b. _____ was filed on _____ as application serial no. _____ and was amended on _____ (if applicable) (in the case of a PCT-filed application) described and claimed in international no. _____ filed _____ and as amended on _____ (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56 (see the last page attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, Sections 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

a. XX no such applications has been filed.

b. _____ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC Section 119

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

ALL FOREIGN APPLICATIONS, IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

I hereby claim the benefit under Title 35, United States Code, Sections 119 and 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

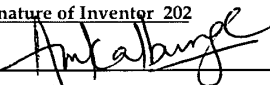
MICHAEL FARJAMI, Reg. No. 38,135
 FARSHAD FARJAMI, Reg. No. 41,014

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/firm/organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct them to the contrary.

Please direct all correspondence in this case to FARJAMI & FARJAMI LLP at the address indicated below:

FARJAMI & FARJAMI LLP
 26522 La Alameda Ave., Suite 360
 Mission Viejo, California 92691
 Telephone: (949) 282-1000
Customer No.: 25700

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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	Post Office Address 19 Springwater	City Irvine	State or Country CA	Zip Code 92604	
Signature of Inventor 201		Signature of Inventor 202 		Signature of Inventor 203	
Date		Date 03/14/2007		Date	

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	City of Residence IRVINE		State or Foreign Country CALIFORNIA		Country of Citizenship INDIA
	Post Office Address 59 Edgewood		City Irvine	State or Country CA	Zip Code 92618
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	Post Office Address 2732 York Road		City Carlsbad	State or Country CA	Zip Code 92008
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	City of Residence		State or Foreign Country CALIFORNIA		Country of Citizenship
	Post Office Address		City	State or Country CA	Zip Code
Signature of Inventor 204		Signature of Inventor 205		Signature of Inventor 206	
Date		Date		Date	

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The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

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It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

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Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

Each inventor named in the application;

Each attorney or agent who prepares or prosecutes the application; and

Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

PATENT APPLICATION SERIAL NO. _____ 6

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

03/20/2007 LWONDIM1 00000030 11724916

01 FC:1011	300.00 OP
02 FC:1111	500.00 OP
03 FC:1311	200.00 OP

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 498-267/60033

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875 Effective December 8, 2004

Application or Docket Number

11724916

APPLICATION AS FILED - PART I

FOR		(Column 1)	(Column 2)
NUMBER FILED			NUMBER EXTRA
BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A
SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A
TOTAL CLAIMS (37 CFR 1.16(i))		20 minus 20 =	0
INDEPENDENT CLAIMS (37 CFR 1.16(h))		2 minus 3 =	0
APPLICATION SIZE FEE (37 CFR 1.16(e))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			

SMALL ENTITY	
RATE (\$)	FEE (\$)
N/A	150.00
N/A	\$250
N/A	\$100
X\$ 25	
X100	
+180=	
TOTAL	

OTHER THAN SMALL ENTITY	
RATE (\$)	FEE (\$)
N/A	300.00
N/A	\$500
N/A	\$200
X\$50	
X200	
+360=	
TOTAL	1000

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

	CLAIMS REMAINING AFTER AMENDMENT (Column 1)	HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)
Total (37 CFR 1.16(j))	Minus	**	=
Independent (37 CFR 1.16(h))	Minus	***	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

SMALL ENTITY	
RATE (\$)	ADDITIONAL FEE (\$)
X\$ 25	
X100	
+180=	
TOTAL ADD'L FEE	

OTHER THAN SMALL ENTITY	
RATE (\$)	ADDITIONAL FEE (\$)
X\$50	
X200	
+360=	
TOTAL ADD'L FEE	

	CLAIMS REMAINING AFTER AMENDMENT (Column 1)	HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)
Total (37 CFR 1.16(j))	Minus	**	=
Independent (37 CFR 1.16(h))	Minus	***	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

SMALL ENTITY	
RATE (\$)	ADDITIONAL FEE (\$)
X\$ 25	
X100	
+180=	
TOTAL ADD'L FEE	

OTHER THAN SMALL ENTITY	
RATE (\$)	ADDITIONAL FEE (\$)
X\$50	
X200	
+360=	
TOTAL ADD'L FEE	

- * If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
- ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
- *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

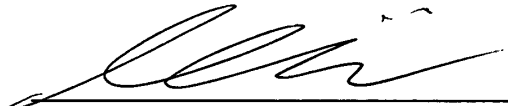
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

NONPUBLICATION REQUEST UNDER 35 U.S.C. 122(b)(2)(B)(i)	First Named Inventor Kevin Q. Yin	
	Title	Deep Trench Isolation and Method for Forming Same
	Attorney Docket Number	0150150

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing.

I hereby request that the attached application not be published under 35 U.S.C. 122(b).

3/16/07
 Date


 Signature

(949) 282-1000
 Telephone number

Michael Farjami, Esq.
 Typed or printed name

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing**.

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

This collection of information is required by 37 CFR 1.213(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.